Design and measurement of fully digital ternary content addressable memory using ratioless static random access memory cells and hierarchical-AND matching comparator

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A 36-bit x 32-entry fully digital ternary content addressable memory (TCAM) using the ratioless static random access memory (RL-SRAM) technology and fully complementary hierarchical-AND matching comparators (HAMCs) was developed. Since its fully complementary and digital operation enables the effect of device variabilities to be avoided, it can operate with a quite low supply voltage. A test chip incorporating a conventional TCAM and a proposed 24-transistor ratioless TCAM (RL-TCAM) cells and HAMCs was developed using a 0.18 μm CMOS process. The minimum operating voltage of 0.25 V of the developed RL-TCAM, which is less than half of that of the conventional TCAM, was measured via the conventional CMOS push-pull output buffers with the level-shifting and flipping technique using optimized pull-up voltage and resistors.

1. Introduction

The content addressable memory (CAM) is a specialized memory that searches for specified data and provides the address if the data is found in the stored entry. The ternary content addressable memory (TCAM) is an advanced CAM; it can store the three values of '0','1', and 'X' ("Don't care") and it can perform the longest prefix matching with wildcard masks.[1-3] Since the TCAM features super high-speed searching by parallel hardware processing, it is mainly used in mission-critical network routers for classifying fast packets.[4-9]

Figure 1(a) shows a conventional TCAM cell with two 6-transistor static random access memory (6T-SRAM) cells in which the data comparator drives the common match line dynamically and the NOR-type match line sense amplifier (MLSA) detects whether the entry is matched or not.[10-11] Figure 1(b) shows a block diagram of the conventional TCAM. The TCAM is mainly composed of search register, TCAM cell array, MLSA, and priority encoder (PE). In addition, row decoder and peripheral circuit are employed to store the data in the TCAM cell array. The match lines are precharged in every search cycle; however, most of the match lines are discharged.[1] This is because most of the entries are unmatched with the commonly used search data.[12] The dynamic operation of the MLSA is a key to achieve high-speed search operation; therefore, it is commonly employed in the TCAM for a network router. On the other hand, the demand for the reduction in power consumption has also increased.[10,13] To reduce the charging and discharging power, a technique for reducing the precharge level of the match line to the intermediate voltage level [4], a technique for setting a flag to disable the precharge operation for the unused entry [14], a technique for pre-searching with the segmented subentries, [15] and other various technologies in the circuit-level and/or system-level approaches are also proposed.[16-26] TCAMs are expected to be applied to the big data processing; however, their huge power consumption is a serious constraint.[27] On the other hand, from the viewpoint of the application to the parallel search engine for the big data processing system, technologies to reduce the power consumption in the standby state by using nonvolatile elements in memory cells have been introduced.[15,16,21,28]

In this paper, we propose a fully digital TCAM technology to reduce the power by an essential approach to lower the supply voltage of the whole TCAM circuit. Since the 6-transistor SRAM cells and the MLSA in the conventional TCAM suffer from device variabilities especially in the low-supply voltage range, we have developed the ratioless

TCAM cell and a fully complementary hierarchical-AND matching comparator (HAMC).[29,30] We have developed a test chip including the proposed TCAM and conventional TCAM and confirmed the operation of the power supply voltage of 0.25 V.[31] In addition to the design of RL-TCAM, we also disclose the technique of measuring the TCAM function with a digital LSI tester in such an ultra low-voltage region in this paper.

This paper consists of the following sections. In Sec. 2, a new ratioless TCAM cell design is proposed. In Sec. 3, RL-TCAM using HAMC is proposed. In Sec. 4, the test chip design and the measurement results are explained. In Sec. 5, the measurement technique in an ultra low-voltage region is introduced.

2. Ratioless TCAM cell design

We already developed the ratioless 12-transistor SRAM (RL-12T-SRAM), as shown in Fig. 2, in which the design margin, such as the static noise margin, is no longer considered.[30] The fully complementary and digital operation of the RL-12T-SRAM enables the effect of device variabilities to be avoided; therefore, it can operate with a quite low supply voltage. Figure 3 shows the developed ratioless TCAM (RL-TCAM) cell. In a TCAM cell, high-speed read operation and the handling of the half-select state as in the SRAM are unnecessary; therefore, the read bit-line (RB) driver in the conventional RL-12T-SRAM cell shown in Fig.2 can be eliminated. As a result, the number of transistors for 1-bit storage is reduced from 12 to 8. The comparison between the conventional TCAM cell design and the developed RL-TCAM cell design is summarized in Table I. In the SRAM cell design, twice the number of transistors is required to construct a ratioless cell; on the other hand, in the RL-TCAM cell design, the number of transistors is reduced from 32 to 24, as shown in Fig.3. In addition, the layout area becomes less than 1.5 times that of the conventional TCAM cell. This is because the ratioless design allows the minimum dimension for each transistor to be employed.

3. RL-TCAM design with fully complementary hierarchical-AND matching comparator

Since the dynamic operation of the MLSA scheme in the conventional TCAM suffers from device variabilities, especially in the low supply voltage range, we have developed a fully complementary HAMC for the RL-TCAM. Figure 4 shows the delay time and the

optimized W_p/W_n ratio for 180 nm CMOS logic gates for (a) $V_{dd} = 1.8$ V and for (b) $V_{dd} = 0.25$ V. Because the delay time and the optimized W_p/W_n ratio of NOR gates are too large to use in the low-voltage region, we have designed the HAMC with just the series connection of the AND (NAND and INVERTER) gates. Figure 5(a) shows a block diagram of the developed RL-TCAM. The RL-TCAM cell array is configured with 36-bit x 32 entries. Figure 5(b) shows an RL-TCAM entry in which the AND gates in the HAMC are embedded. The equivalent numbers of transistors of a TCAM cell including the number of transistors in the matching circuit are also summarized in Table I. The number of equivalent transistors for the conventional TCAM cell is 16.3, because 9 transistors are added as an MLSA for an entry. On the other hand, that for the proposed RL-TCAM cell using HAMC to support the fully digital operation is increased from 24 to 26.9.

Figure 6 shows the comparison of simulated power consumption versus supply voltage between the conventional TCAM with MLSA and RL-TCAM with HAMC using the Monte Carlo analysis. In the conventional scheme, all of the match lines are precharged and most of the match lines are discharged in every cycle. On the other hand, in the RL-TCAM, static logic enables low voltage operation and prevents the waste of power. As a result, the power consumption can be reduced by about 15 to 25%, and the minimum operating voltage can be halved.

Table. II summarizes the comparison of the energy efficiency for one search operation between previously proposed TCAMs and this work[14,15,32]. Despite the disadvantage of the process technology, our design achieves an energy efficiency of 1.03 fJ/bit/search at the supply voltage of 0.25 V. Its performance is comparable to that of TCAMs with advanced process technologies and/or nonvolatile devices.

4. Test chip development and experimental results

A test chip incorporating a conventional TCAM with 6T-SRAM cells and MLSA, and a proposed RL-TCAM with RL-TCAM cells and HAMC was developed using a 180 nm CMOS as shown in Fig.7. Figure 8 shows the measured results of the TCAMs that are tested with the randomly generated data and search keys. Although the operating speed is almost the same in the Vdd > 0.6 V, the minimum operating voltage of RL-TCAM reaches 0.25 V, which is less than the half of that of the conventional TCAM of 0.60 V. This voltage scaling achieves the marked power reduction for the one search operation to 17.4%

($=0.25^2/0.6^2$). These measured results agree with the measured results of SRAMs evaluated in Ref. 30.

5. Measurement technique in ultra low-voltage region

An LSI having a very low power supply voltage such as 0.25 V cannot simply be measured using an FGPA-based digital tester whose logic threshold is about 0.3 V at least.[33] Therefore, we applied a pull-up voltage source and pull-up resistors for the output signals of the CMOS output buffer circuit to adjust the output signal levels, as shown in Figure 9. Figure 10 shows the measured output waveform in this configuration. As shown in this figure, in spite of the supply voltage for the DUT is 0.25 V, the signal level is successfully shifted. However, the observed high and low levels of the output waveform (V_{OL} and V_{OH}) are flipped. This is because when the pull-up resistor is connected to the CMOS output buffer, the circuit acts as a complementary open-drain circuit. Figure 11(a) and 11(b) show equivalent circuits for this situation. The output NMOS and PMOS transistors act as pull-down transistors in both cases of the low level output (V_{OL}) and the high level output (V_{OH}), respectively. As shown in Fig. 11(b), a large gate-source voltage is applied to the output PMOS transistor; therefore, the ON resistance value of the PMOS transistor (R_{PON}) becomes smaller than that of the NMOS transistor (R_{NON}) as shown in Fig. 11(a). Figure 12 shows the simulated results of the ON resistance of PMOS and NMOS (R_{PON} and R_{NON}) versus the pull-up voltage ($V_{PULL-UP}$) when the pull-up resistance ($R_{PULL-UP}$) is 15 kΩ. As shown in this figure, the resistance of the PMOS is always lower than that of the NMOS. As a result, the level of the V_{OH} is lower than that of the V_{OL}. Figure 13 shows the relationship between $R_{PULL-UP}$ and the levels of the V_{OH} and V_{OL}. When the $R_{PULL-UP}$ is sufficiently large, V_{OL} and V_{OH} are the same as the ground level (GND) and chip supply voltage (V_{chip}), respectively. When the $R_{PULL-UP}$ becomes low, both V_{OL} and V_{OH} become $V_{PULL-UP}$. By appropriately selecting the $R_{PULL-UP}$ (1 kΩ – 1 MΩ), it is possible to obtain the flipped output signal, which meets the minimum threshold voltage of the digital LSI tester.

6. Conclusions

RL-TCAM using 24-transistor ratioless TCAM cells with fully complementary HAMC was developed for ultra low-supply-voltage operation. The minimum operating voltage of

0.25 V of the developed RL-TCAM, which is less than half of that of the conventional TCAM, was confirmed by measurements of the test chip. In order to measure the TCAM functions in the ultra low-voltage region via CMOS output buffers using the digital LSI tester, the level-shifting and flipping technique using the optimized pull-up voltage and the resistors are employed.

Acknowledgments

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Fig. Captions

Fig. 1. Conventional TCAM. (a) Conventional TCAM cell with MLSA. (b) Block diagram of conventional TCAM.

Fig. 2. Ratioless 12-transistor SRAM cell[30].

Fig. 3. Ratioless TCAM cell.

Fig. 4. Delay time and optimized W_p/W_n ratio for CMOS logic gates. (a) V_{dd} = 1.8 V. (b) V_{dd} = 0.25 V.

Fig. 5. RL-TCAM design. (a) Block diagram of RL-TCAM. (b) An entry of the RL-TCAM including HAMC.

Fig. 6. Comparison of the simulated power in the matching operation.

Fig. 7. Photo of developed test chip. (a) Conventional TCAM. (b) RL-TCAM.

Fig. 8. Measured T_{pd} and minimum operating voltage.

Fig. 9. Measurement environment for ultra low-supply voltage operation.

Fig. 10. Measured operating output waveforms.

Fig. 11. Equivalent circuits for the output buffer with the pull-up circuit. (a) V_{OL}. (b) V_{OH}.

Fig. 12. Simulated results of the R_{PON} and R_{NON} versus $V_{PULL-UP}$.

Fig. 13. Simulated results of the output voltage levels (V_{OL} and V_{OH}) versus $R_{PULL-UP}$.

Table I. Summary of the comparison between conventional TCAM cell and RL-TCAM cell.

	Conv. Design	RL Design	Overhead
SRAM cell (TRs)	6	12	x 2
TCAM cell (TRs)	16	24	x 1.5
TCAM cell (Area) (μm^2)	70.4	102	x 1.45
TCAM cell with matching circuit (TRs)	16.3	26.9	x 1.65

Table II. Comparison of energy efficiency for search operation.

	Ref. 32	Ref. 14	Ref. 15	This work
Process (nm)	65	65	90 (w/MTJ)	180
Supply voltage (V)	1.2	1	1.2	0.25
Energy efficiency (fJ/bit/search)	0.77	1.98	1.04	1.03
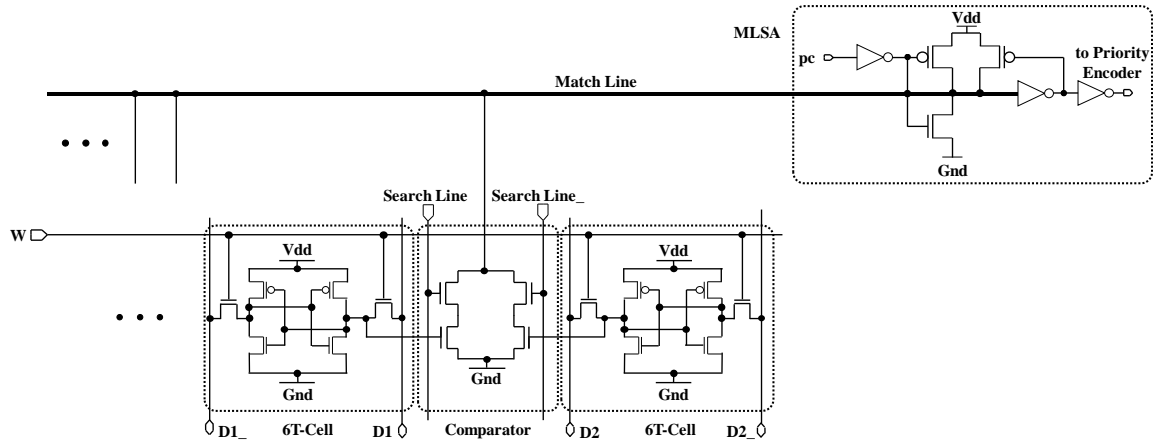
(a)
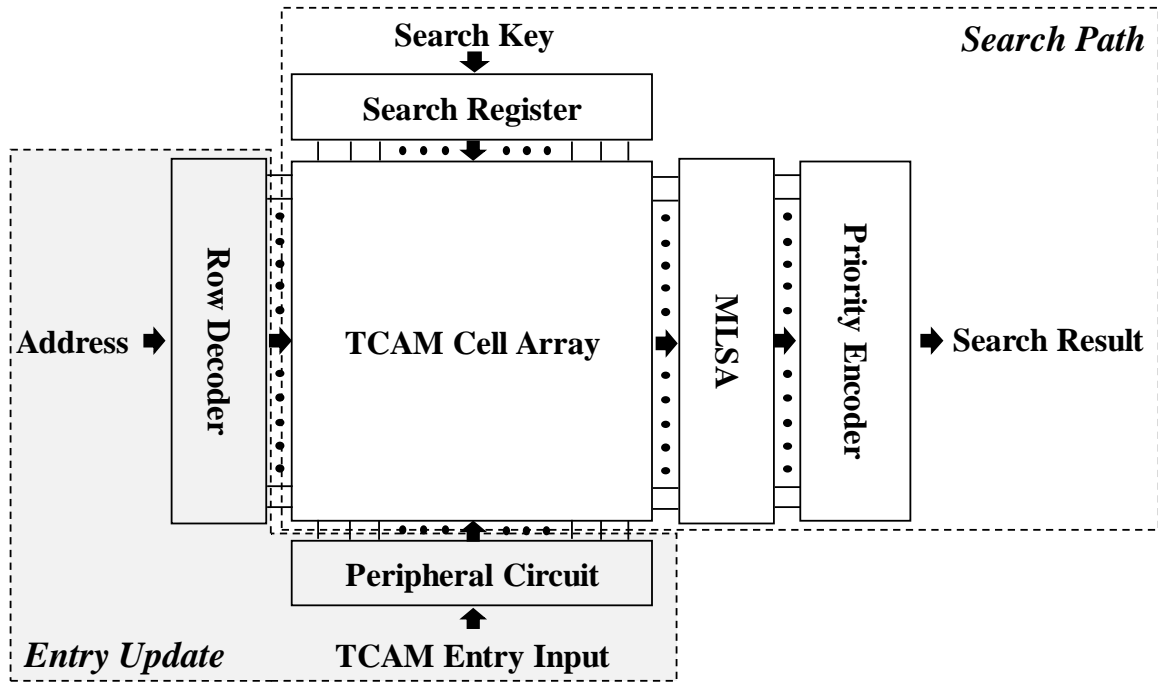
(b)

Fig. 1.
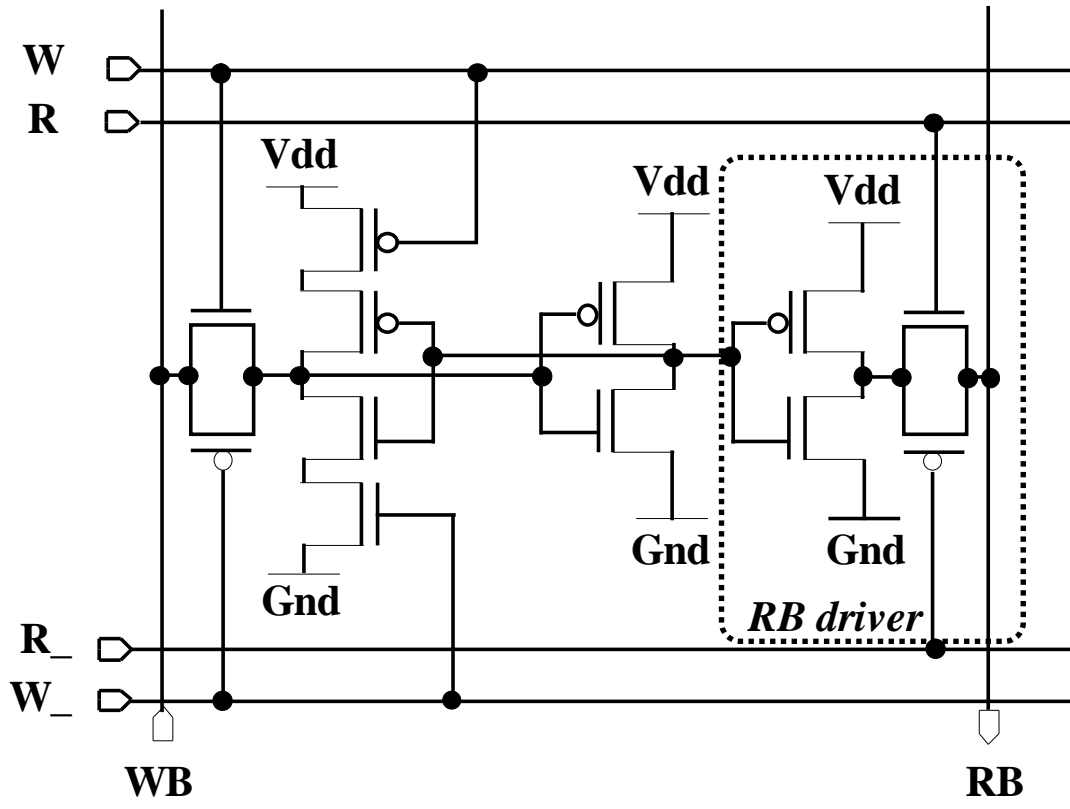
Fig. 2.
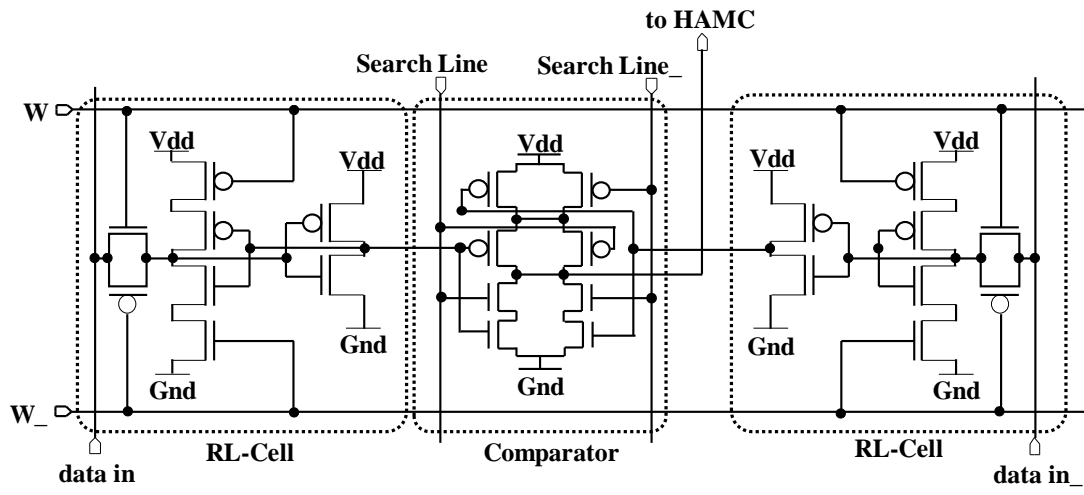
Fig 3.
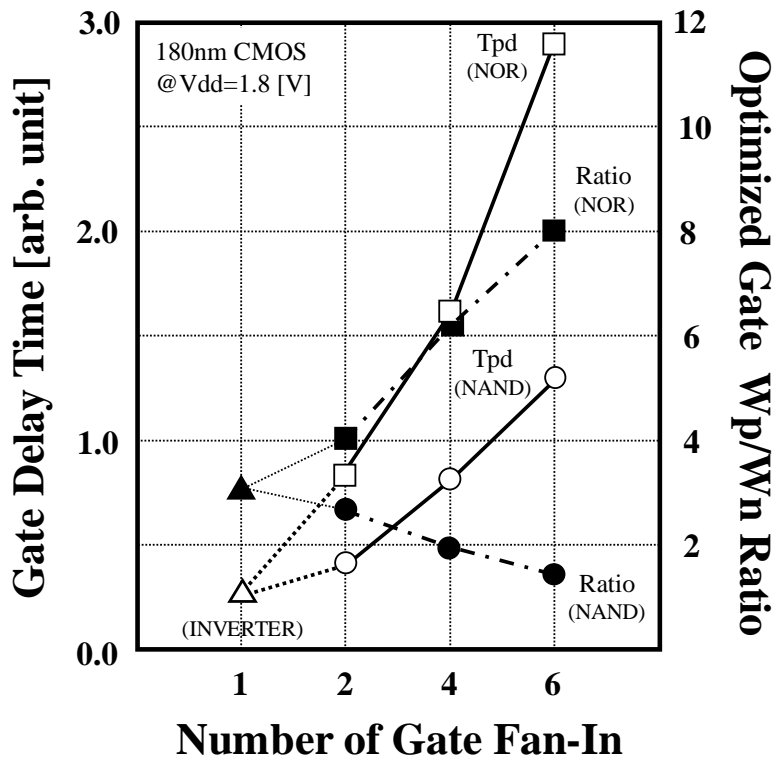
(a)
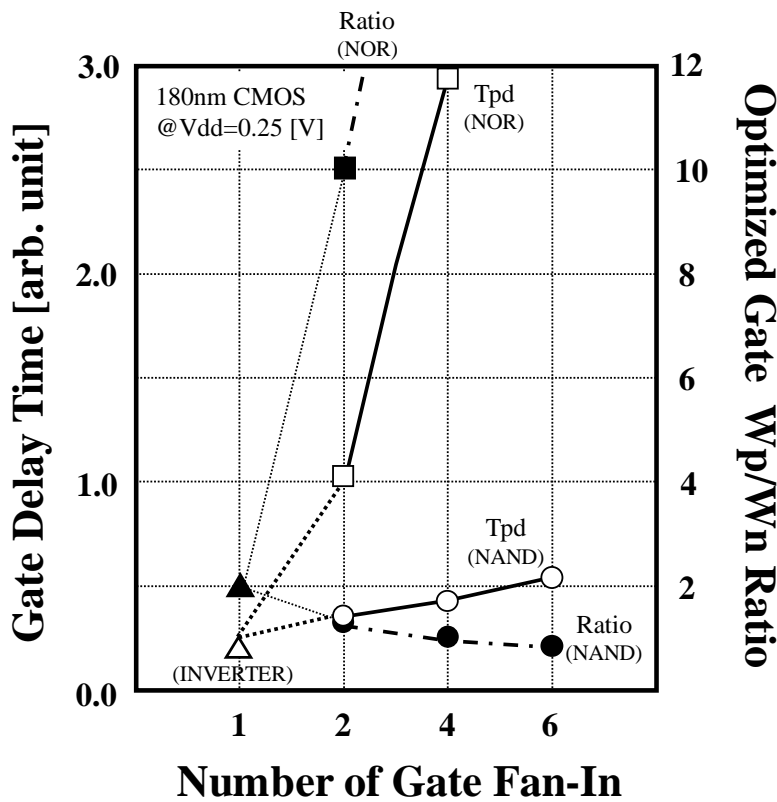
(b)

Fig. 4.
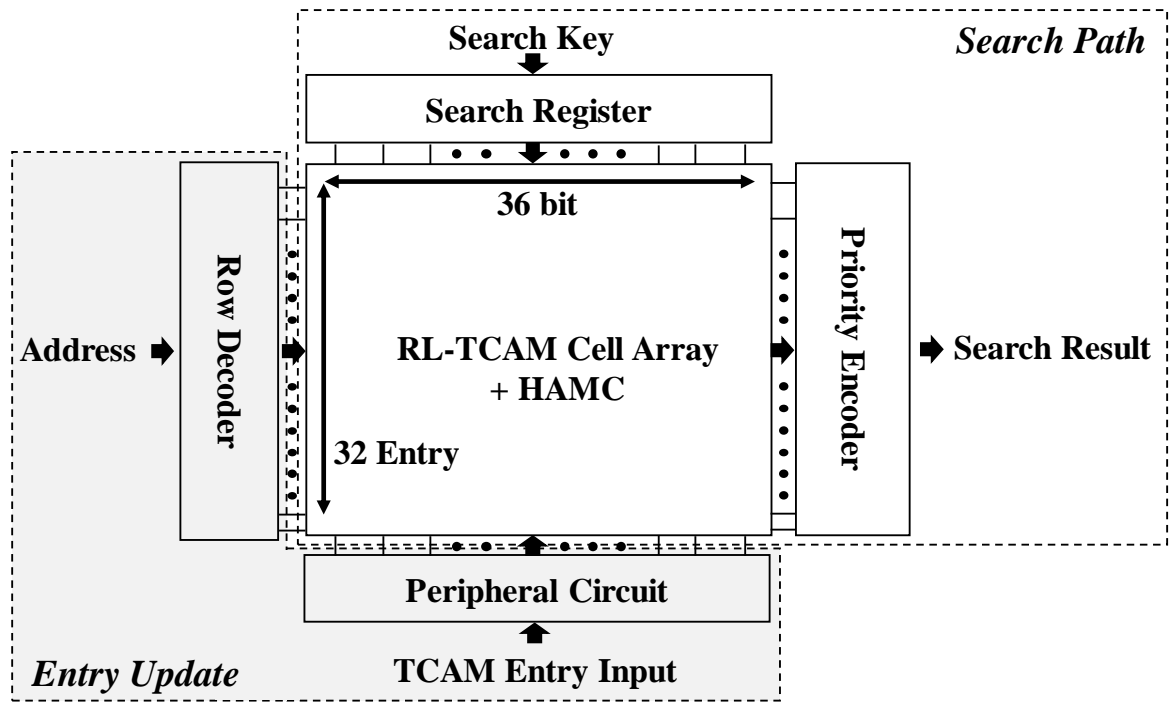
(a)
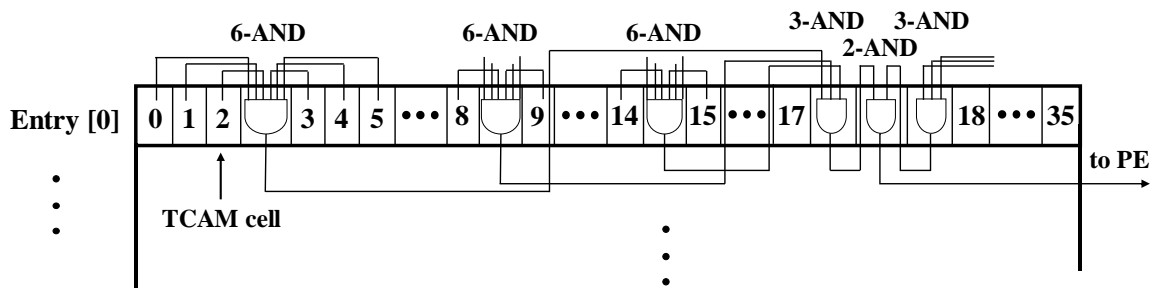
(b)

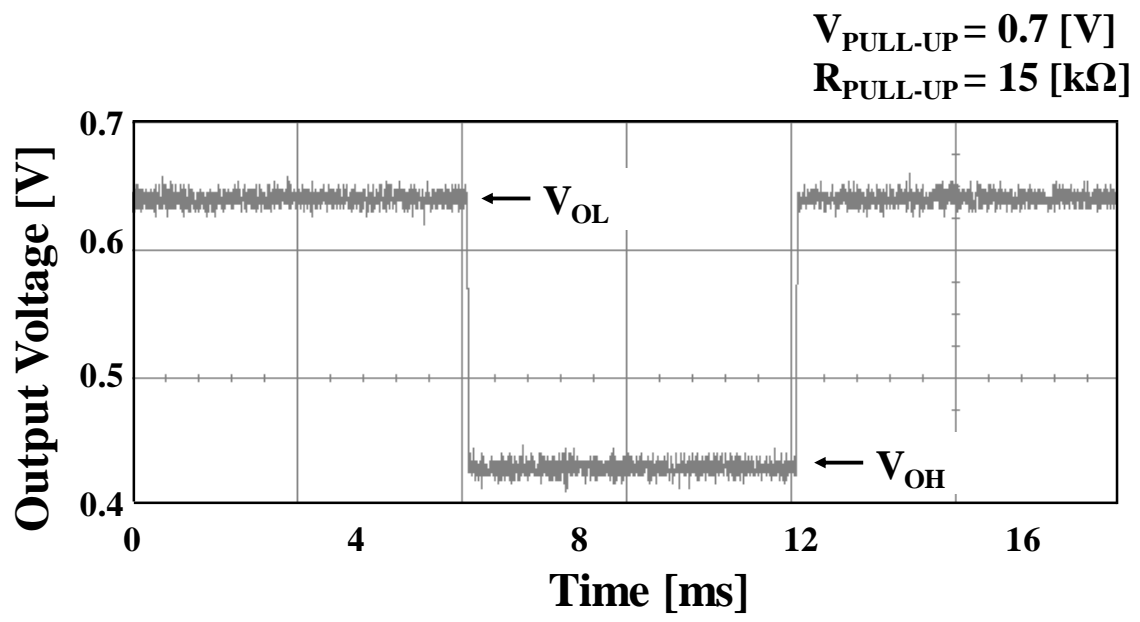Fig. 5.

Fig. 6.

Fig. 7.

Fig. 8.
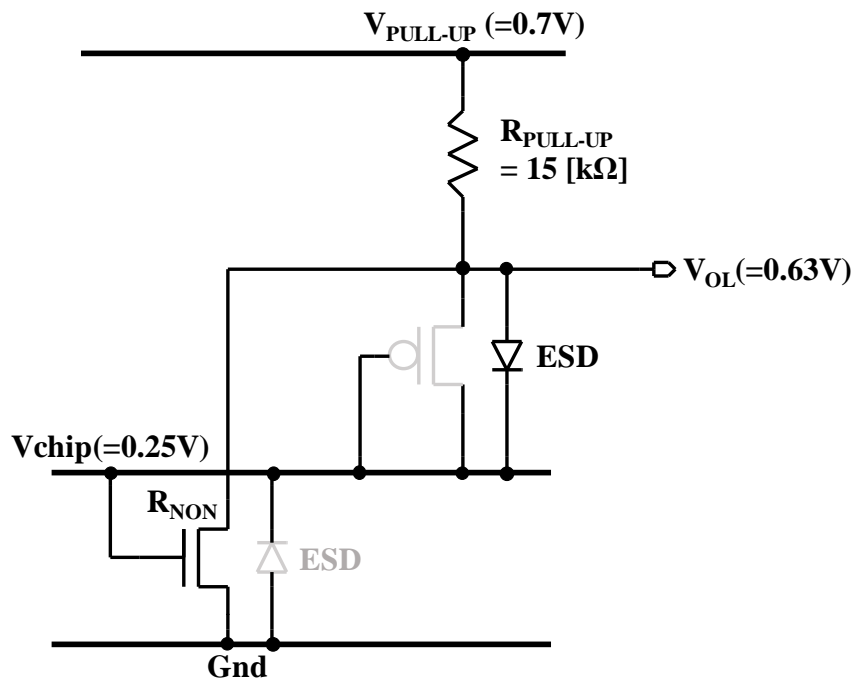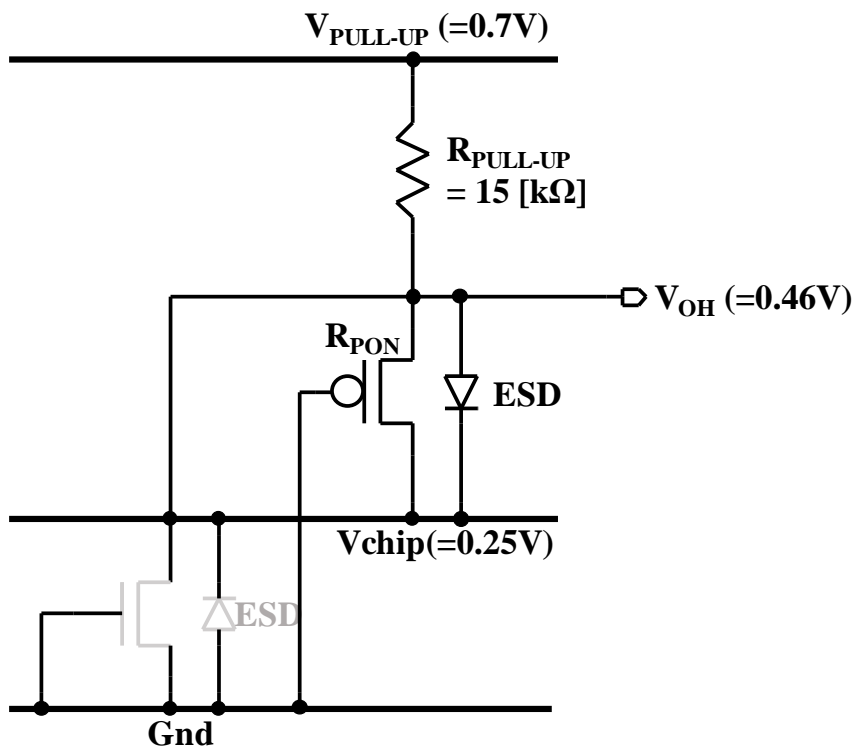
Fig. 9.
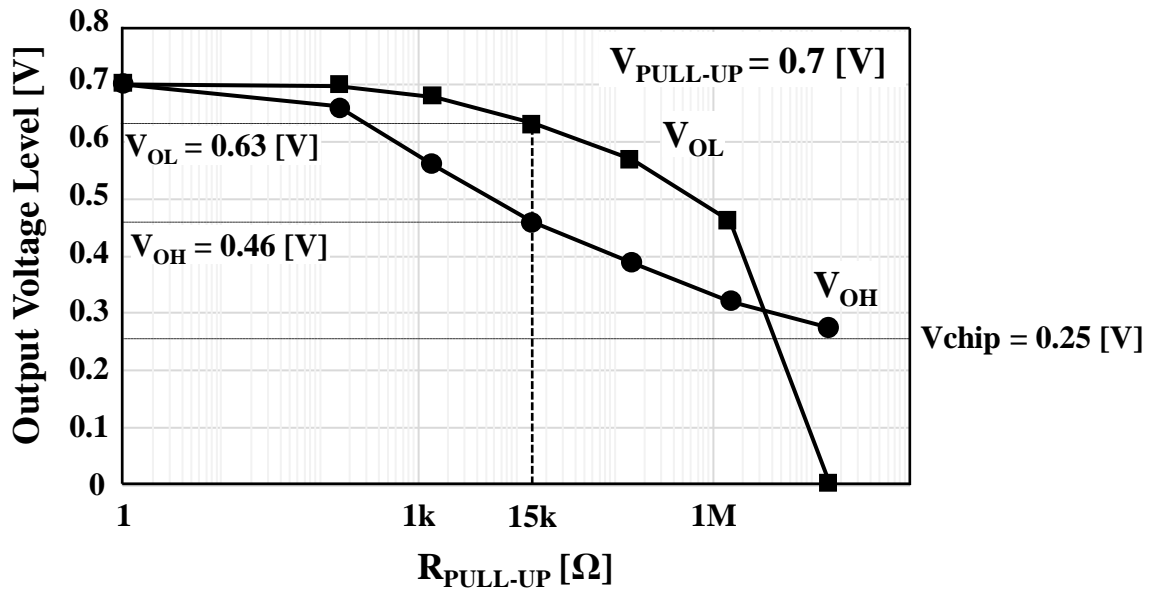
$V_{PULL-UP} = 0.7$ [V]
$R_{PULL-UP} = 15$ [kΩ]

Fig. 10.

(a)

(b)

Fig. 11.

21

Fig. 12.

Fig 13.