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On-Chip Test Clock Validation Using A Time-to-Digital Converter in FPGAs

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***Abstract*— While on-chip delay measurement combining logic BIST with a variable test clock is an effective way to secure field reliability of VLSI/FPGAs, validation of the variable test clock generated on the chip is important to guarantee measurement accuracy. This paper addresses a method of on-chip test clock validation using a TDC (Time-to-Digital Converter) for FPGAs. The proposed method has two operation modes, one is a resolution measurement mode and the other is a phase difference measurement mode. The resolution measurement mode is performed first to check the resolution of the TDC circuit. The phase difference measurement mode checks the timing difference between the original clock and the generated test clock. Evaluation experiments using a real FPGA device shows that the resolution of the proposed clock validation method using a TDC is 50.46 ps. For a variable test clock with resolution of 96.15 ps, it was confirmed that INL (Integral Non-Linearity) of the clock is within 10% and it was inconsistent with a result observed by an oscilloscope.**

Keywords—FPGA; Built-In Self-Test; Delay testing; Variable test clock; Time-to-Digital Converter;

I. INTRODUCTION

FPGAs have been widely used in various digital systems. When they are used in a safety-critical or mission-critical system such as an automotive or social infrastructure system, high reliability is required to the FPGAs [1-3]. On-line testing is indispensable to assure high reliability during field operation, because aging phenomena more likely occur for deep sub-micron devises even for FPGAs. Periodical delay testing including on-chip delay measurement in field is effective for detection of aging of the devices like BTI (Bias Temperature Instability) and HCI (Hot Carrier Injection) which cause delay degradation of the chip [4-7]. By alerting to the system before the increased circuit delay exceeds an allowable limit, a system can avoid aging-induced failures.

Circuit delay can be measured using delay test scheme with logic BIST. Several BIST-based delay test methods have been proposed for FPGAs [10-13]. In [10], a path delay fault detection technique using BIST was proposed for FPGAs. In [11] and [12], delay testing methods were proposed that check the difference of arrival time of several paths having the same circuit structure and the same expected delay value. A method in [13] is for path delay measurement using a TDC (Time-to-Digital Converter) and an RO (Ring Oscillator). For FPGAs, however, it is difficult to know a configuration of logic blocks of the user circuit and wire delays at the design stage. The BIST-based delay measurement has advantages that a real delay of the user circuit can be checked without external equipment such as an oscilloscope and can be measured even in field.

A degradation detection technology, named DART, has been proposed that can detect circuit degradation by performing self-test repeatedly in field [14]. The DART measures a circuit delay using a variable test clock generated on the chip where the interval of two test clock signals can be changed. All techniques employed in the DART are fully digital but they were originally developed for ASICs. Hence they cannot be applied to FPGAs as it is or an accuracy regarding its measurement cannot be secured. In order to utilize the techniques on FPGAs, a method of variable test clock generation for FPGAs has been developed [15]. The method, which relies on a phase-shift function of an embedded PLL in an FPGA, measures the fastest operation speed and a delay margin of the user circuit by operating the circuit repeatedly with different test clock intervals. While the test clock with a specific timing is generated inside the chip, an accuracy of the test clock can be checked by observing external validation equipment such as an oscilloscope. However, there are some problems in evaluating the accuracy using the external equipment because of measurement errors. As it is impractical to guarantee the accuracy of all chips using the external equipment, it is desired to validate the generated test clock inside the chip. Although methods for test clock validation using a ADC (Analog-to-Digital Converter) or a TDC (Time-to-Digital Converter) have been proposed [16,17], these methods are inadequate to validate a fine change within one clock interval.

This paper proposes a method of test clock validation using a TDC for FPGAs. The proposed method can check the accuracy of variable test clock generated on a chip for delay measurement. Unlike clock validation using the TDCs for ASICs, TDCs for FPGAs are greatly influenced by wire delay. The proposed method employs the TDC circuit in [18] developed for FPGAs. The proposed method has two operation modes, one is resolution measurement mode and the other is phase difference measurement mode. The resolution measurement mode is performed first to check the resolution of the TDC circuit. After that, the phase difference measurement mode is performed to check the timing difference between the original clock and the generated test clock. In evaluation experiments using Altera Cyclone IV FPGA, the proposed method showed that the resolution of the proposed clock validation method is 50.46 ps. For a variable test clock with resolution of 96.15 ps, it was confirmed that INL (Integral Non-Linearity) of the clock is within 10% and it was inconsistent with a result observed by an oscilloscope.

This paper is organized as follows: Section 2 describes on-chip delay measurement and a TDC circuit that can be realized in FPGAs. Section 3 describes the proposed method for test clock validation using the TDC circuit. Section 4 shows evaluation experiments with an Altera Cyclone IV. Section 5 concludes this paper.

II. On-Chip Delay Measurement in FPGAs

A. Logic BIST-Based At-Speed Delay Testing

Figure 1 shows a structure of delay measurement circuit using scan-based logic BIST. For a CUT (circuit under test), which is a user logic, scan design is applied with general EDA tools, and assumes LoC (Launch-off-Capture) test scheme for at-speed testing which applies two clock signals (double capture) between scan-shift operations as shown in Figure 2. While scan-enable signal *SE* is set to 1, the circuit works in the scan-shift mode where scan-in and scan-out operations are performed simultaneously. In the scan-in operation, random test patterns generated by an LFSR (Linear Feedback Shift Register) are shifted-in to the scan chains. In the scan-out operation, test responses stored in the scan flip-flops are sent to a MISR (Multiple Input Signature Register). On the other hand, while the SE is set to 0, the circuit works in the function mode where launch and capture operations are performed. In the launch operation the inserted test patterns in the scan chains are applied to the CUT. In the capture operation the test responses are stored to flip-flops on the scan chains. A pass/fail decision is made by comparing the expected test responses with the values compressed by the MISR. At-speed delay testing is performed by adjusting an interval between the launch and capture cycle to the same as the system clock. The test timing generator is a circuit, which has a role to change the interval between the launch and capture cycle, will be described in the next Section. Note that TS in Figure 1 is a digital temperature sensor which is not dealt with in this paper.

Figure 3 shows a relationship between a path delay and a variable test clock in the LoC test scheme. In on-chip delay measurement, the timing of the launch clock is shifted from the original one step by step while the timing of the capture clock is fixed to the original one. As a result, the interval of launch and capture clocks is getting shorter and shorter. Since same test patterns are applied repeatedly, the test passes as long as the interval is larger than the path delay sensitized by the test patterns. When the interval became shorter than the path delay, the test fails. The test timing of the fail test with the largest clock interval gives information on the lower bound of the path delay. Thus, the maximal path delay can be measured by repeating the test with variable test timing.

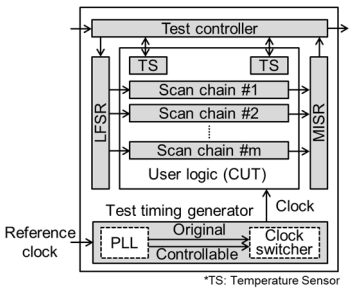


Figure 1. Circut structure of logic BIST-based delay measurement.

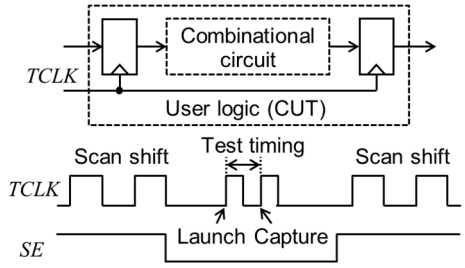


Figure 2. Test timing of Launch-off-Capture scheme.

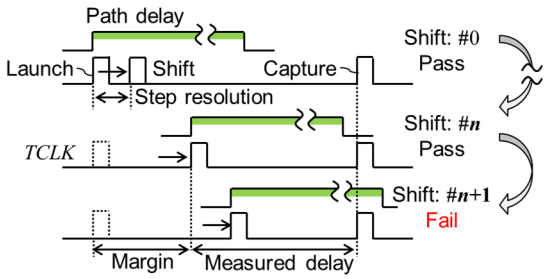


Figure 3. Test timing with variable test timing.

B. Variable Test Timing Generation on FPGAs

For FPGAs, the variable test timing can be implemented using a dynamic phase shift function of an embedded PLL [15]. The dynamic phase shift function can delay a signal of the output clock of the PLL in real time without re-configuration. Resolution of the phase shift, which is the minimum shift value, depends on a voltage-controlled oscillator (VCO) of the PLL. The method generates a variable test timing utilizing two output clocks of the PLL as shown in Figure 1. One is the original clock used for the capture clock. The other is the controlled clock shifted by the dynamic phase shift function, and is used as a launch clock. The launch and capture clocks can be generated by taking a pair out of the original and controllable clocks one by one.

Figure 4 shows waveforms related to generation of the variable test timing. $SCLK$ is a scan clock and CLK is the original clock of the PLL. $DCLK_i (i = 0,1,2,\ldots,N)$ is a controllable clock using the phase shifting function, where N is the number of times of phase shifting, and PS is the minimum value of phase shifting. $TCLK_i$ is a generated test clock, which is the same period as $SCLK$ in the scan shift mode. One cycle of $DCLK_i$ is used as the launch cycle, and one cycle of CLK is used as the capture cycle in the capture mode. t_i is a generated test timing which is a period between the launch clock given by $DCLK_i$ and the capture clock given by CLK. After initialization of the PLL, the phase shifting of the PLL is performed. $DCLK_0$ is adjusted toward the original clock CLK to be the same as the test timing of the system clock. A first test timing t_0 of $TCLK_0$ is the same as the normal clock. When phase shifting is performed one time, t_1 of $DCLK_1$ is delayed the amount of PS. Then, the generated test timing t_N is calculated by subscribing $PS*N$ from the initial clock interval. The relation between the number of the phase shifts N and the generated test timing t_N is shown as follow.

$$t_N = initial\ clock - (PS * N) \qquad (1)$$

By repeating phase shifting, the test timing becomes smaller and smaller, that is, the test clock becomes faster. Thus, the test timing generation method using the dynamic phase shift function can change the test timing that is the interval of two clock signals for delay measurement.

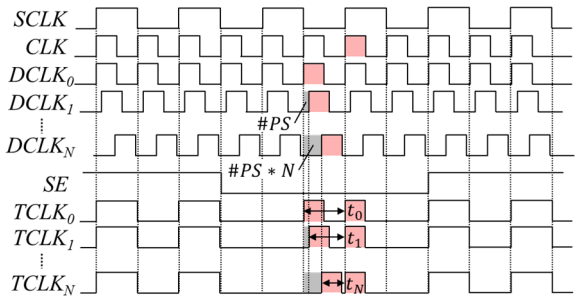


Figure 4. Waveform of variable test timing generation

C. *Time-to-Digital Converter in FPGAs* [18]

A TDC circuit, which is a kind of ADC, was developed as a method to measure a phase difference of two analog values and to output it in a digital value. In this case, two analog values are arrival time of clock signals. When a general TDC for ASICs is used for an FPGA, high resolution or high measurement accuracy cannot be derived because it is difficult for FPGAs to estimate a delay time greatly influenced by wire delay.

Figure 5 shows a TDC for FPGAs proposed in [18]. The TDC consists of some counters and delay elements such as a buffer. *En* signal is set to 1 during measurement. By counting up a rising edge of the input clock during the period of *En* = 1, the time to be measured is converted to the counter value. Figure 6 shows waveforms of the TDC. T_{Period} denotes a period of an input clock, TDC_{En} is a signal which inputs to *En*. τ is a delay value of one delay element, and TDC_{Out} denotes a counter value that outputs after measurement. $C_i (i = 0,1,2, \dots, N-1)$ is a clock signal input to each counter via delay element. When *En* = 1, each counter counts up according to the rising edge of the delayed input clock. $\Delta\tau$ is a delay amount per 1 bit of TDC count. In FPGAs, since τ is very large, and variations due to manufacturing variation or placement and routing are also large, the TDC using only τ cannot derive its resolution. On the other hand, by setting T_{Period} and TDC_{En} to the same length, and counting up according to the delayed input clock, $\Delta\tau$ can be calculated. Then, the TDC using $\Delta\tau$ can derive its resolution. Thus, the TDC can be regarded as a counter-based circuit which has a clock of delay time $\Delta\tau$ as an input. Let *N* be the number of stages of the counter. The minimum resolution (LSB: least significant bit) measurable with the TDC is calculated by the following equation (2).

$$LSB = \frac{T_{Period}}{N} \qquad (2)$$

Increasing the input clock speed or the number of stages of the counter improves the resolution of the TDC. Furthermore, by taking an average of the count values of more than one TDC, the measurement accuracy can improve too. Note that the larger *N* is, the longer the delay line of the TDC is. Due to pulse-shrinking at the delay line, there is a limitation to increasing the resolution by increase of *N*. In the [18], a TDC with 6.7 ps resolution has realized in Altera Stratix IV FPGAs.

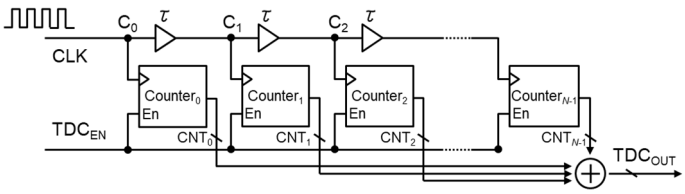


Figure 5. TDC for FPGAs [18]

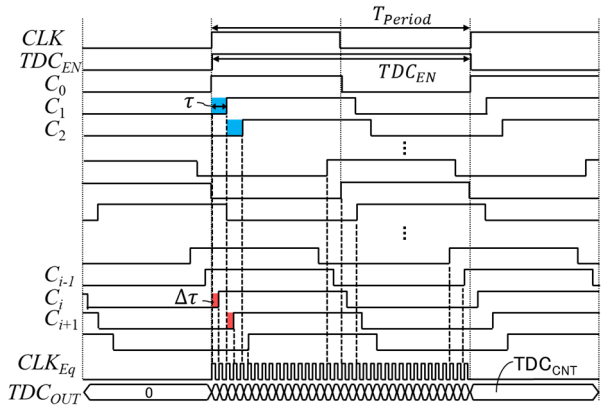


Figure 6. Waveform of the TDC.

III. Test Clock Validation Method Using a TDC

A. *Overviews of the Proposed Variable Test Clock Generater*

Figure 7 shows a circuit architecture for test clock generation and validation including a test timing generator, a TDC, and a TDC controller. The TDC and the TDC controller fulfills a role of the test clock validation circuit. The original clock *CLK* is an output from a PLL and a controllable clock *DCLK* is generated using a phase shift function. These two clock signals are connected to the inputs of the validation circuit. By setting the TDC_{En} signal to 1 during measurement, the validation circuit works to validate its own resolution of the TDC. Figure 8 shows a circuit structure of the validation circuit which has the following two measurement modes switched by TDC_{Mode} signal.

1) Resolution measurement mode of the TDC.

2) Phase difference measurement mode of the variable clock.

Figure 9 shows waveforms to explain a relationship between the control timing of the TDC_{En} signal in each mode and a measurement target period. In the proposed method, the resolution measurement mode is performed first. The test clock validation circuit measures the resolution by making an input clock period T_{Period} and the time of TDC_{En} = 1 equal. After that, the phase difference measurement mode is performed for validation of the test clock by using the measured resolution. Details of each mode are described in the next section.

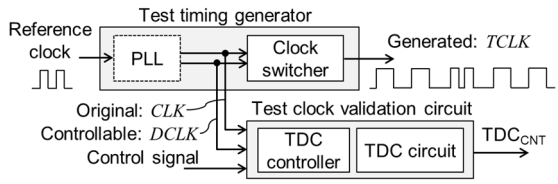


Figure 7. Variable test timing generator and validation circuit.

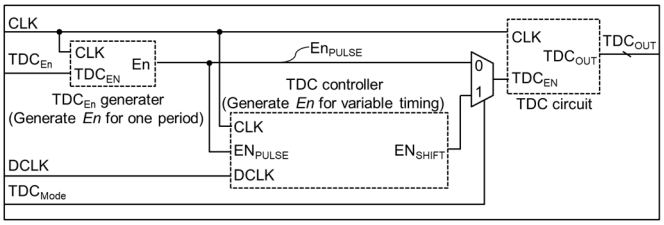
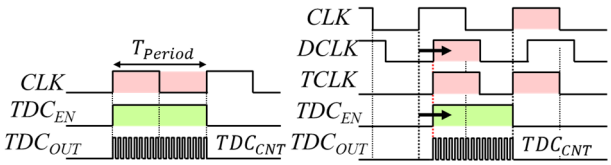


Figure 8. The proposed test clock validation circuit using a TDC.



(a) (b)

(a) Resolution measurement mode of TDC.
(b) Phase difference measurement mode of variable test clock.

Figure 9. Relation between *TDC_En* signal input to TDC and target pulse to be validated.

B. Resolution measurement mode of TDC

In the resolution measurement mode of the TDC, a delay amount per 1 bit of the TDC counter, TDC_{Res}, is measured by referring the measurement period as a known value. Figure 9(a) shows a relationship between the control timing of the TDC_{En} signal and the measurement target period. The CLK is assumed to be 100 MHz for simple explanation. When the period of TDC_{En} is the same as the period T_{Period} of the input clock, both TDC_{En} and T_{Period} are 10 ns and can be treated as a known value. TDC resolution TDC_{Res} can be calculated as the following equation (3) by using the total count value of the TDC counter which is the measured value TDC_{CNT} and equation (2).

$$TDC_{Res} = \frac{T_{Period}}{TDC_{CNT}} \qquad (3)$$

C. Phase difference measurement mode of variable test clock

In the phase difference measurement mode of the variable clock, the phase difference of the variable test clock is measured using TDC resolution TDC_{Res}. Since the TDC is not re-configured in the resolution measuring mode and this mode, the delay elements of the TDC are fixed during measurement. Therefore, resolution TDC_{Res} takes a common value in both modes. Figure 9(b) shows a relationship between the control timing of the TDC_{En} signal and the measurement target period. As described in Section II.B, test clock *TCLK* is selected from *CLK* and *DCLK*. The phase difference is the timing difference between these two clocks. In the proposed circuit, control is performed so that t_i (i = 0, 1, 2, ..., N) shown in Figure 4 and equation (1) is the same as TDC_{En}. Thus, a phase difference TDC_{OUT} that is the measurement target period can be calculated from the TDC_{Res}, the total count value of the TDC_{CNT}, and the following equation (4).

$$TDC_{OUT} = TDC_{Res} \times TDC_{CNT} \qquad (4)$$

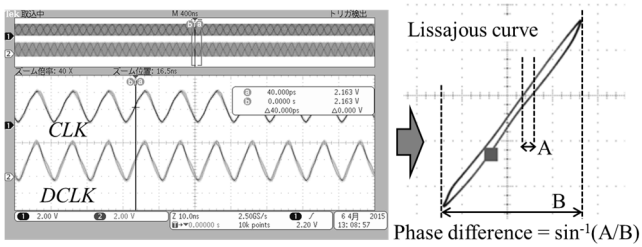
Every time phase shift of the variable test clock generation circuit is repeated, TDC_{En} and TDC_{CNT} decrease. By using the proposed circuit, it is possible to measure a decreasing phase of the variable clock from the total count value of the TDC.

IV. Evaluation Experiment

A. Experiment Setup

For experiment to make sure the proposed method, the variable test timing generator and the test clock validation circuit were implemented on the Cyclone IV FPGA device in 60 nm technology. An oscilloscope used for comparative evaluation of measurement values is Tektronix DPO 3034. Since the VCO frequency of the PLL is 1.3 GHz, the controllable minimum step resolution of dynamic phase shift is about 96.15 ps. Note that the step resolution depends on the VCO frequency of the embedded PLL of the FPGA [15]. The initial clock of the test timing generator is 100 MHz (10 ns). The number of stages of the TDC is 200 stages. A bit width of the TDC counter is 1 bit, that is, it is equivalent to single flip-flop, and a bit width of the counter for totalization is 32 bits. Since the maximum count value of the TDC is 200 (200 stages × 1 bit), the theoretical value of resolution LSB is calculated as 50.00 ps from the equation (2). In order to improve measurement accuracy, eight sets of the TDC are implemented on the FPGA and an average of the measurement count values of the TDCs is calculated. An accuracy of the variable test clock is evaluated using the test clock validation circuit. Evaluating FPGA resource usage, one TDC that is shown in Figure 5 consisted of 652 LUTs and 200 registers. The proposed test clock validation circuit including eight TDCs spent 5300 LUTs and 1617 registers.

Furthermore, in order to evaluate an actual accuracy of the phase shift step resolution in the test timing generator, the variable test timing is checked with an oscilloscope too. A phase difference between the original clock and the controllable clock is validated using the Lissajous waveform as shown in Figure 10. When phase shift is performed, a difference between the two waveforms (CLK and DCLK) gradually expands, and the amount of phase difference can be calculated from the Lissajous waveform of the oscilloscope.



(a) (b)

(a) Waveforms of CLK(original) and DCLK(controlled).
(b) Lissajous curve.

Figure 10. Validation of the phase shift of variable test clock using oscilloscope.

B. Evaluation of Resolution of TDC

The resolution of the TDC is evaluated at the resolution measurement mode. The measurement period is one cycle of the original clock CLK which is the output of the PLL. Since the clock is 100 MHz, the period of 10 ns is measured using the TDC, and its resolution is calculated from the output count.

Table 1 shows an average of count numbers of the eight TDCs for ten times measurement, and a calculated resolution of one TDC from the measured values. It can be confirmed that

the average value of the resolution when using a plurality of TDC circuits is 50.46 ps. Since a theoretical value (LSB) of the resolution is 50.00 ps, a difference from the theoretical value is 0.46 ps.

Table 1. EVALUATION OF RESOLUTION OF THE TDC

	Measured values per one TDC (Average of the eight TDC)	
#	TDC count value	Resolution of TDC [ps]
1	198.88	50.28
2	198.25	50.44
3	198.50	50.38
4	198.13	50.47
5	197.88	50.54
6	197.88	50.54
7	197.88	50.54
8	198.00	50.51
9	197.88	50.54
10	198.50	50.38
Ave.	198.18	50.46

C. Evaluation of Variable Test Clock

A decreasing phase difference of the variable clock is measured using the variable clock phase difference measurement mode. The resolution of the TDC was 50.46 ps in this mode. Figure 11 and Table 2 show phase difference validation results of variable clocks when the phase shift is repeated up to 20 times. There is no phase difference between CLK and DCLK before performing the phase shift. While the theoretical value of the initial phase shift is 10000.00 ps (10 ns), measurement results using the TDC was 9984.89 ps. The difference of 15.11 ps occurs at the initial measurement. The measured value at the first phase shift is the same value as at the initial time, and the count value has not changed. While the theoretical value for 20 times phase shift was 8077.00 ps (10 ns - 96.15 ps × 20 times), the measured value was 8016.93 ps, i.e. the difference was 60.07 ps. These errors are caused by a difference between the theoretical resolution (50.00 ps) and the actual resolution (50.46 ps) measured. It is also conceivable an influence of a fine delay in controlling the TDC_{En} of the TDC. It could be confirmed that the clock validation circuit using the TDC validates the decrease in the phase difference when the phase shift is repeated.

Table 2. PHASE SHIFT VALUES IN VARIABLE TEST CLOCK USING PROPOSED VALIDATION CIRCUIT

	Phase shift value [ps]		
	Ideal value		Measured value
#	Phase difference	10ns – (Phase difference)	
0	0.00	10000.00	9984.89
1	96.15	9903.85	9984.89
2	192.30	9807.70	9896.58
3	288.45	9711.55	9795.66
4	384.60	9615.40	9581.21
5	480.75	9519.25	9530.74
6	576.90	9423.10	9455.05
7	673.05	9326.95	9291.06
8	769.20	9230.80	9234.29
9	865.35	9134.65	9177.52
10	961.50	9038.50	9082.91
~	~	~	~
20	1923.00	8077.00	8016.93

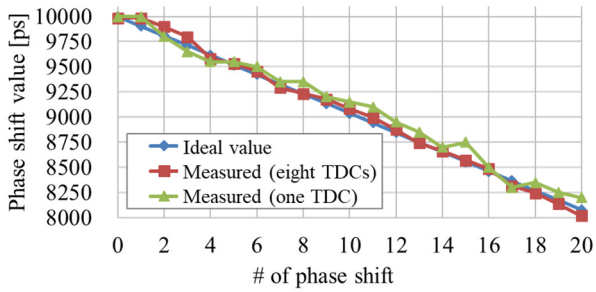


Figure 11. Evaluation of the variable test clock.

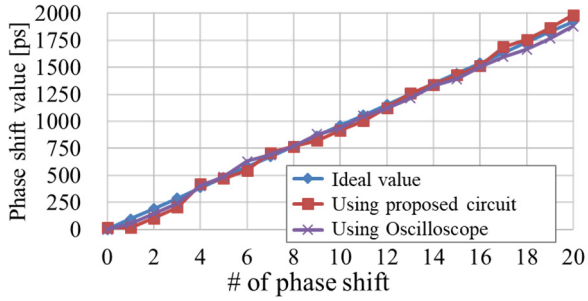
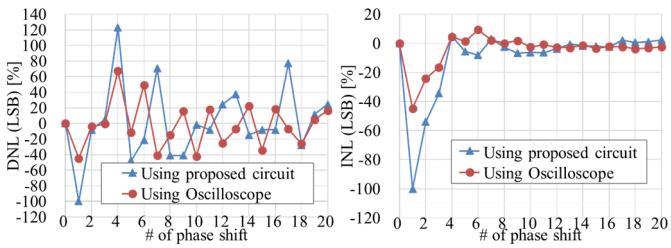


Figure 12. Evaluation of the variable test clock.

Table 3. EVALUATION OF PHASE SHIFT VALUES IN VARIABLE TEST CLOCK

	Phase shift value [ps]			
	Ideal value (step: 96.15 ps)	Measured value using proposed circuit (TDC)		Measured value using oscilloscope
#	Phase difference	Measured	Difference from ideal	Difference from ideal
0	0.00	15.11	15.11	0.00
1	96.15	15.11	-81.04	-43.02
2	192.30	103.42	-88.88	-46.62
3	288.45	204.34	-84.11	-47.07
4	384.60	418.79	34.19	17.82
5	480.75	469.26	-11.49	6.59
6	576.90	544.95	-31.95	54.20
7	673.05	708.94	35.89	14.79
8	769.20	765.71	-3.49	0.85
9	865.35	822.48	-42.87	15.86
10	961.50	917.09	-44.41	-24.80
~	~	~	~	~
20	1923.00	1983.07	60.07	-43.46



(a) DNL (b) INL

Figure 13. Evaluation of DNL and INL.

Figure 12 and Table 3 show measurement results of clock validation as an increasing phase difference measured by the proposed circuit and the oscilloscope. A theoretical value of the phase difference when performing 20 times phase shift takes 1923.00 ps, the measured value using the TDC was 1983.07 ps, the difference was 60.07 ps. The difference from the oscilloscope measurement value is -43.46 ps. Figure 13 shows

the evaluation results using the differential nonlinearity error DNL (Differential Non-Linearity) and the integral nonlinearity error INL (Integral Non-Linearity). In the DNL evaluation shown in Figure 13(a), a maximum DNL of the validation result using the oscilloscope is 67.49%, and that of using proposed circuit is 123.04%, there is a large difference. The shift amount of the minimum step of the phase shift is 96.15 ps, and the LSB of the implemented TDC is 50.46 ps. Because the resolution of TDC is insufficient, it is considered that the value of DNL became large. In the INL evaluation shown in Figure 13(b), maximum INL of the validation result using the oscilloscope is -44.74%, and that of using proposed circuit is 100.00%, there is a large difference. However, when the number of phase shifts is 4 time or later, both the INL using the oscilloscope and the that of using the validation circuit are within ± 10%. It is suggested that a measurement similar to validation using an oscilloscope can be realized by using the proposed method. From the evaluation results, it is confirmed that the resolution of the test clock validation circuit using the TDC is insufficient, but the variable phase difference can be measured inside a chip.

Therefore, although the proposed test clock validation circuit has not very high resolution, it was confirmed that it can be realized as a circuit to validate the variable test timing inside a chip. The implemented TDC has 50.46 ps resolution in Altera Cyclone IV FPGA, and may not be enough to validate a test clock of recent FPGAs. However, the TDC in [18] realized in Altera Stratix IV FPGAs has 6.7 ps resolution. Thus, by replacing the TDC used in the proposed method to another one with higher resolution, it is expected that finer test clock validation can be realized.

V. Conclusions

This paper proposed a test clock validation method using a TDC for FPGAs. The proposed method has two measurement modes, which are the resolution measurement mode of the TDC and the phase difference measurement mode of the variable test clock. Since a resolution of TDC a common value in the two modes, the proposed circuit is realized as a test clock validation circuit that can validate a resolution of the TDC. Evaluation experiments confirmed that a resolution of the TDC implemented on an FPGA is 50.46 ps, and that a change of a phase difference of a variable test clock can be checked using the phase difference measurement mode. Therefore, although the proposed test clock validation circuit is not high resolution, it was confirmed that the proposed circuit can be realized as a circuit that can validate the variable test timing inside the chip. Future researches include further improvement of accuracy and resolution of the validation circuit and development of a variable test clock generator with higher resolution. Furthermore, by analyzing the measurement results of TDC, we aim to improve the reliability of test techniques such as a delay measurement in FPGAs.

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