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博 士 論 文 概 要

論 文 題 目

Speed Optimization and Capacitor Mismatch Calibration for High-Resolution High-Speed Pipelined A/D Converters

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Wide applications of digital signal processing in high-resolution image and video system, asynchronous digital subscriber loop and wireless communication require high-resolution, high-speed pipelined analog-to-digital converters (ADCs) with low power dissipation, small chip area and easy integration in standard CMOS technology. Currently, for charge-transfer pipelined ADCs, speed improvement and capacitor mismatch calibration are two important research issues.

For high speed, conversion ratio can be improved through advanced analog or digital calibrations, the conventional stage's complete settling characteristics' optimization and parallel pipelined ADCs. However, these schemes require additional power dissipation and chip area because of the modification to the analog channel and utilization of complicated digital algorithms, the increase of op-amps' design complexity and the employment of multi-analog-channels, respectively. For high resolution, the capacitor mismatch can be calibrated on digital or analog domain. However, digital calibrations require large auxiliary hardware circuits, increase the system complexity and generally degrade the continuity of the conversion process because of background periodic re-calibrations. Analog calibrations require additional analog circuits and extra clock phases, which result in additional power dissipation and chip area and greatly degrade the conversion speed.

To overcome above drawbacks and obtain low power and small area, the implementation of novel speed optimization and novel capacitor mismatch calibration without additional power dissipation and chip area is considered as the subject of this dissertation. Two pipelined ADCs based on novel incomplete settling principle and novel capacitor mismatch

calibration technique, respectively, are proposed to achieve speed improvement and high resolution with low power and small area.

The dissertation is organized with five chapters as follows.

In chapter 1, the background of this dissertation is introduced and the research status is overviewed briefly. Moreover, the contribution and organization of this dissertation are provided.

In chapter 2, pipelined ADCs' basic design issues, speed optimization methods and error calibration techniques are overviewed as preliminaries of this dissertation. The published speed improvement methods focus on the conventional stage's complete settling characteristics' optimization and parallel pipelined ADCs. The reported error calibration techniques are mainly on digital or analog domain. However, these methods and techniques are all at odds with requirements for low power and small area. The speed optimization methods inherently result in additional power dissipation and chip area, respectively, because of high performance requirements for op-amps and the employment of multi-analog-channel. Meanwhile, the digital calibrations require large auxiliary hardware circuits, increase the system complexity and generally degrade the conversion process's continuity. The analog calibrations require additional analog circuits and extra clock phases, which increase power dissipation and chip area and greatly degrade the conversion speed. Therefore, to obtain low power and small area, the implementation of novel speed optimization and novel capacitor mismatch calibration without additional power dissipation and chip area is very important.

In chapter 3, based on the novel speed optimization principle of incomplete settling, this dissertation presents a 15-bit 10-MS/s pipelined

ADC where the op-amp's settling process ends before its input terminal voltage arrives within the accuracy tolerance required by the complete settling. The conventional complete settling stage is improved to the incomplete settling structure simply through dividing the conventional sample clock into two parts for discharging sample and feedback capacitors and completing the sample, respectively. This improvement can optimize the time during both slewing period and linear period without additional power consumption and chip area. The proposed ADC verifies the validity of optimizing conversion speed with low power and small area through the incomplete settling and obtains a performance improvement of 30%.

In chapter 4, based on one novel capacitor mismatch calibration technique, this dissertation proposes a 12-bit 3.7-MS/s pipelined ADC. The conventional stage is improved to an algorithmic circuit involving charge summing, capacitors' exchange and charge redistribution, simply through introducing some extra switches into the analog circuit. This improvement can reduce the nonlinear error from the capacitor mismatch to the second order without additional power dissipation and chip area. Furthermore, three clock phases are employed to improve the ADC's conversion speed compared with analog calibration methods that require no-less-than 4 clock phases. This presented ADC verifies the validity of obtaining high resolution with low power and small area through this novel capacitor mismatch calibration technique and obtains a performance improvement of 42%.

In chapter 5, the conclusion of this dissertation is made. The proposed two ADCs achieve speed improvement and high resolution, respectively, with low power and small area.