CMOS Analog Integrated Circuit Design Techniques for Low-Powered Ubiquitous Device

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Abstract

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With the continuously expanding of market for ubiquitous devices such as wireless sensor nodes, portable devices, and implantable medical devices, low-power design is becoming a critical priority in integrated circuit design. Low-power design can increase lifetime and/or achieve a smaller size. Therefore, one of the focuses of this dissertation is to improve the low-power design techniques.

On the other hand, the advancement in low-power design makes it possible that ubiquitous device can be powered by low-power energy source such as ambient energy or small size batteries. In many well supplied devices the problem related to power is essentially related to cost. However for low-powered devices the problem of power is not only economics but also becomes very essential in terms of functionality. Due to the usual very small amount of energy or unstable energy available the way the engineer manages power becomes a key point in this area. Therefore, another focus of this dissertation is to try finding ways to improve the power management problem.

Complementary metal oxide-semiconductor (CMOS) has become the predominant technology in integrated circuit design due to its high density, power savings and low manufacturing costs. The whole integrated circuit industry will still continue to benefit from the geometric downsizing that comes with every new generation of semiconductor manufacturing processes. Therefore, only several CMOS analog integrated circuit design techniques are proposed for low-powered ubiquitous device in this dissertation.

In the first chapter, the motivations and the backgrounds of this dissertation are

presented.

In the second chapter, the first key cell circuit, a low-power sub-1-V self-biased low-voltage reference, is proposed for low-power electronic applications based on body effect. A voltage reference with low sensitivity to the temperature and supply voltage is one of the key issues in analog circuit design for ubiquitous device. A metal-oxide-semiconductor field effect transistor (MOSFET) can be operated at a lower voltage by forward-biasing the source-substrate junction. This approach has been investigated in detail and used to design an ultra-low power CMOS voltage reference for operation at sub-1 V. The issues of CMOS latchup and leakage have been investigated in detail because of the forward biasing of the substrates of MOSFETs in CMOS. The proposed reference has very low temperature dependence by using a MOSFET with body effect compared with other reported low-power references. An HSPICE simulation shows that the reference voltage and the total power dissipation are 181 mV and 1.1 μW, respectively. The temperature coefficient of the reference voltage is 33 ppm/°C at temperatures from -40 to 100 °C. The supply voltage can be as low as 0.95 V in a standard CMOS 0.35 μm technology with threshold voltages of about 0.5 V and -0.65 V for n-channel and p-channel MOSFETs, respectively. Furthermore, the supply voltage dependence is -0.36 mV/V (Vdd=0.95$\sim$3.3 V).

In the third chapter, the second key cell circuit, a fast lock charge pump phase-locked loop (CPPLL) without extra power dissipation is proposed. The low-power PLL design technique is also one of the key issues in analog circuit design. To realize fast lock without extra power dissipation, a continuous-time phase frequency detector (PFD) based on the conventional tri-state PFD is proposed. The locking time of the PLL can be substantially reduced with the proposed continuous-time scheme. During the period that the best tracing and acquisition properties are required, the bandwidth of the PLL is expanded to decrease the locking time with the proposed continuous-

time PFD. Afterwards, the bandwidth of the PLL is recovered to the original value to minimize output jitter due to external noise. Therefore, no extra power is consumed compared with conventional PLL. Any conventional tri-state PFDs can be improved with the proposed continuous-time architecture. The proposed architecture is realized in a standard CMOS 0.35 μm technology. The simulation results demonstrate that the proposed continuous-time PFD is effective to get more speedy locking time without extra power dissipation.

In the fourth chapter, a novel energy management circuit is proposed for self-powered ubiquitous sensor modules using a variable and weak ambient energy. Energy is requested by any kind of devices to become functional. Hence many concerns are applied to power management schemes for any system engineers. In this chapter, the background of ambient energy source and the properties of the selected ambient energy for ubiquitous sensor modules are reviewed firstly. Then, an energy management circuit is proposed for self-powered ubiquitous sensor modules using vibration-based energy. With the proposed circuit, the sensor modules work with low duty cycle operation. Moreover, a two-tank circuit as a part of the energy management circuit is proposed to solve the problem that the average power density of ambient energy always varies with time while the power consumption of the sensor modules is constant and larger than it. In addition, the long start-up time problem is also avoided with the timing control of the proposed energy management circuit. The CMOS implementation and silicon verification results of the proposed circuit are also presented. Its validity is further confirmed with a vibration-based energy generation. The sensor module is used to supervise the vibration of machines and transfer the vibration signal discontinuously. A piezoelectric element acts as the vibration-to-electricity converter to realize battery-free operation.

In the fifth chapter, a high efficiency charge pump power management circuit

is proposed. Charge pump circuits are frequently used in semiconductor integrated circuits to provide a voltage that is higher than the voltage of a power supply. If the output voltage of energy source for low-powered ubiquitous device is small, then the high efficiency charge pump circuit is one of good solutions to convert a small or weak input voltage to a higher stable DC voltage as power supply voltage for ubiquitous device. In addition, the proposed circuit is particularly useful in flash and EEPROM non-volatile memories because that programming or erasing the memory cells needs very high positive and negative voltages. Besides, the charge pump circuit has become an important circuit technique in low-supply-voltage system in order to increase dynamic range and simplify circuit design. The proposed circuit can reduce the equivalent on-resistance of the charge-transfer transistors and can avoid the body effect due to the two pumping branches architecture. Therefore, its voltage pumping efficiency is much higher than that of the conventional designs. Moreover, the maximum gate-source, gate-drain and drain-source voltages of all transistors in the proposed charge pump circuit do not exceed the power supply voltage Vdd. The proposed charge pump circuit has been realized in a standard CMOS N-Well 0.35 μm technology. The measured results demonstrate that the proposed charge pump circuit has very high voltage pumping efficiency without overstress and the proposed charge pump circuit can be realized in any low-voltage single-well standard CMOS technologies.

In the sixth chapter, the conclusions and the scope for future works are presented.

Keywords: *CMOS, Low-Voltage, Low-Power, Ubiquitous, Voltage Reference, Body Effect, PLL, Fast Lock, PFD, Continuous-Time, Frequency Jump, WSN, Battery-Free, Ambient Energy, Power Management, Self-Powered, Vibration-Based Energy, Two-Tank, Sensor Modules, Piezoelectric Element, Charge Pump, Overstress, High Efficiency, Level Shifter.*

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GLOSSARY

CMOS: Complementary Metal Oxide-Semiconductor.

MOSFET: Metal-Oxide-Semiconductor Field Effect Transistor.

DSP: Digital Signal Processor

MPU: Microprocessor Unit

CPPLL: Charge Pump Phase-Locked Loops.

PFD: Phase Frequency Detector.

VCO: Voltage-Controlled Oscillator

DFF: D Flip Flop

VLSI: Very Large Scale Integration.

WSN: Wireless Sensor Network.

T.C.: Temperature Coefficient.

ZTC: Zero-Temperature Coefficient.

VDEC: VLSI Design and Education Center

Chapter 1

INTRODUCTION

This chapter reviews the motivations, low-voltage low-power analog LSI design techniques and potential ambient energy sources for ubiquitous device.

1.1 Motivations

The power consumption of integrated circuit has been increasing at an enormous rate in this few years. For example, the power consumption of microprocessor is heading towards 1000 watts as shown in Fig. 1.1 [1].

Hence, with the continuously expanding of market for ubiquitous devices low-power design is becoming a critical priority in integrated circuit design. Low-power design can increase lifetime and/or achieve a smaller size. Therefore, one of the focuses of this dissertation is to improve low-power design techniques.

On the other hand, the advancement in low-power design makes it possible that ubiquitous device can be powered by low-power energy source such as ambient energy or small size batteries as shown in Fig. 1.2 [2]. In many well supplied devices the problem related to power is essentially related to cost. However for the low-powered devices the problem of power is not only economics but also becomes very essential in terms of functionality. Due to the usual very small amount of energy or unstable energy available the way the engineer manages power becomes a key point in this area [3]. Therefore, another focus of this dissertation is to try finding ways to improve the power management problem.

Complementary metal oxide-semiconductor (CMOS) has become the predomi-

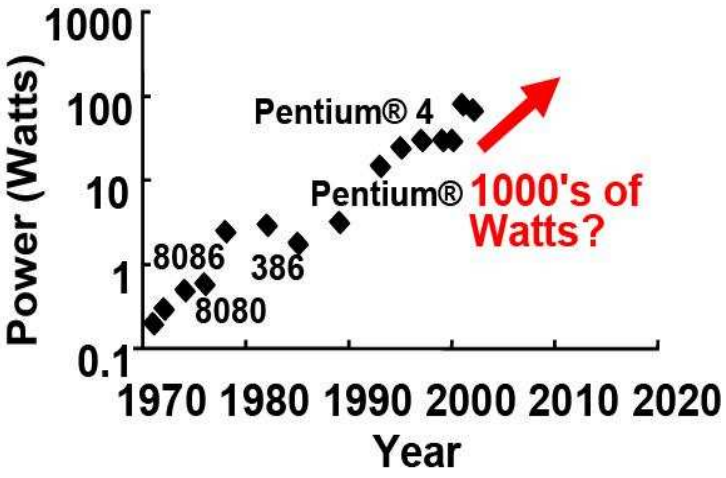

Figure 1.1: Microprocessor power trend.

nant technology in integrated circuit design due to its high density, power savings and low manufacturing costs. The whole integrated circuit industry will still continue to benefit from the geometric downsizing that comes with every new generation of semiconductor manufacturing processes. Therefore, only several CMOS analog integrated circuit design techniques are proposed for low-powered ubiquitous devices in this dissertation.

1.2 Low-Voltage Low-Power Analog LSI Design Techniques

As CMOS technology scaling down, low-power design becomes a central priority for ubiquitous devices. On the other hand, the supply voltage are dramatically reduced as shown in Fig. 1.3 [4]. Digital integrated circuits designs can fully benefit from the continuing down-scaling of CMOS processes as well as from the ongoing reduction of supply voltage. In contrast to digital integrated circuits designs, analog integrated circuits often cannot be designed with minimum length components for reasons of gain, offset, etc. Furthermore, a low voltage supply does not necessarily decrease the dissipation of the analog integrated circuits because it often leads to more complex

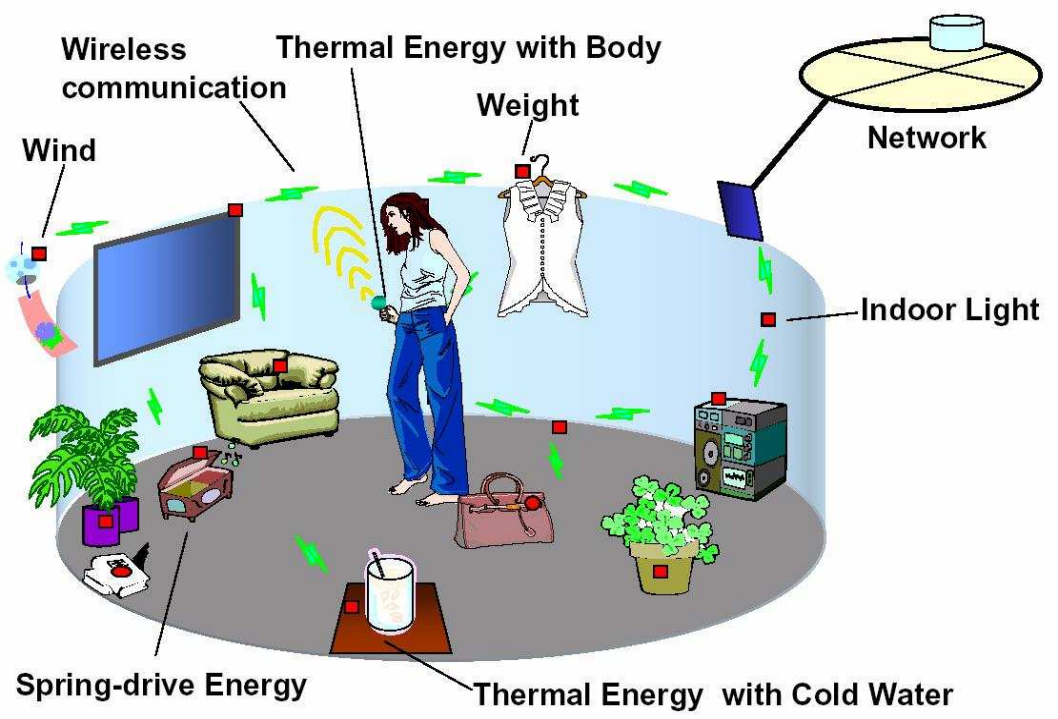

Figure 1.2: Image of future ubiquitous world.

designs, resulting in additional quiescent current. To obtain compact, low-voltage, power-efficient analog integrated circuits, simple library cells with good performance need to be developed.

Extremely low-power design was first explored in the 1970s for the applications such as wristwatch and calculator circuits. Ultra-low-voltage CMOS digital operation was demonstrated in [5]. The predicted CMOS logic operating at a supply voltage of 200 mV at room temperature and derived the fundamental limits of voltage scaling.

Low-power design drew attention beginning in 1990 with expansion in portable electronic market. An overview describing change in power dissipation of CMOS circuits changed since 1980 has been given in [6]. Commercial digital signal processor (DSP) and microprocessor unit (MPU) were used as examples.

At low-voltage low-power integrated circuit design, the main constraints faces are

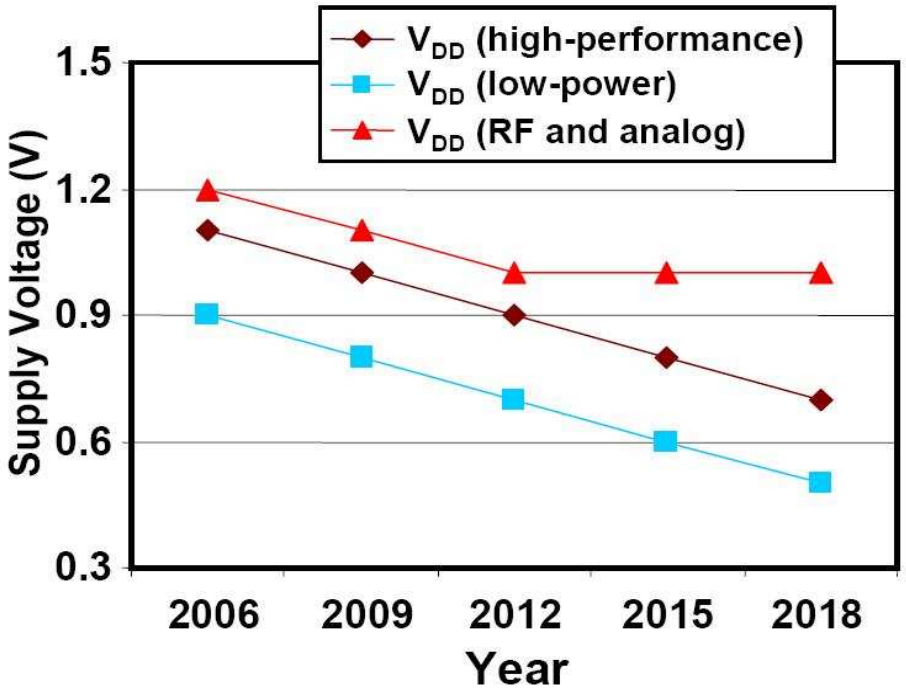

Figure 1.3: Supply voltages scaling of CMOS technology.

the device noise level and the threshold voltage (Vt). Reduction in Vt is dependent on the device technology. Many new design techniques for low-voltage and low-power analog circuits are available, for instance, MOSFETs operating in the sub-threshold region, bulk driven transistors, self-cascode structures and floating gate approach. These techniques will be briefly introduced as follows.

A. Forward Body-Bias Method

In general, the substrate terminal of MOSFET is tied to its source terminal. On the other hand, a forward bias can be applied between the source and substrate of a MOSFET when used as a four-terminal device as shown in Fig. 1.4. Under the forward body-bias, the MOSFET threshold voltage is reduced. The back gate forward body-bias method is compatible with standard CMOS process. In addition, the threshold voltage of MOS transistors can be reduced electrically without any

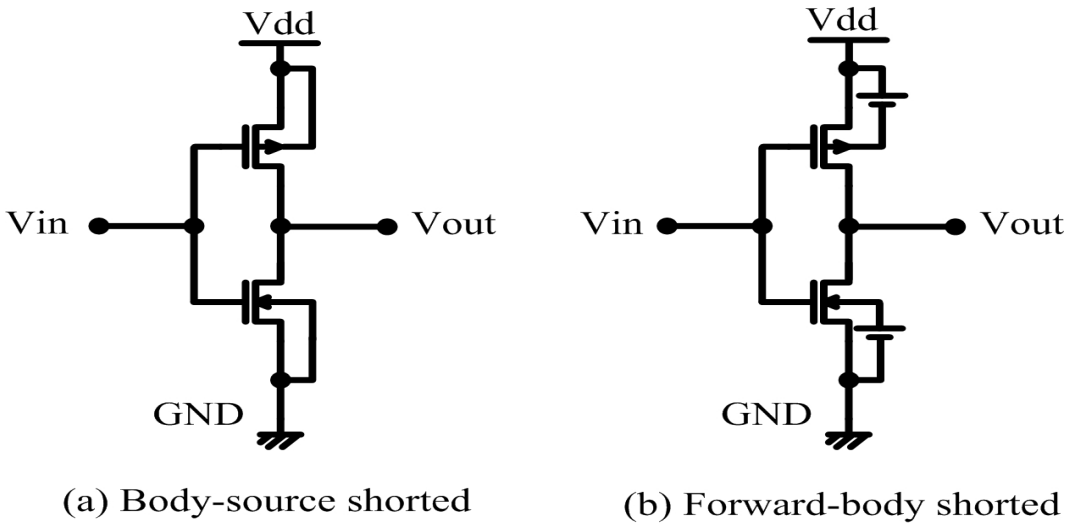

Figure 1.4: Forward biased MOSFETs.

technology modification which provided an important solution to the threshold voltage limitation. Recently, back-gate forward bias technique has been used extensively to design low power digital and analog circuits [7].

B. Sub-Threshold Circuits

Circuits operating in the sub-threshold region have drew attention in recent years because of the need for low-voltage and low-power circuits in human implantable biomedical instruments. In sub-threshold region, MOSFETs have low saturation voltages. This gives larger voltage swings at low-supply voltage even in cascaded MOSFET structures. Similar to a bipolar transistor, the transconductance is expected to be large. However, it may be noted that the current Ids itself is low in sub-threshold region, and transconductance cannot be high as in the case of bipolar transistors [8].

C. Bulk-Driven MOSFETs

As shown in Fig. 1.5, a MOSFET input pair is biased in saturation mode so as to have a continuous drain current. In addition, the input signals Vin1 and Vin2 are applied at the bulk terminals. By using the bulk-driven transistors, the requirement

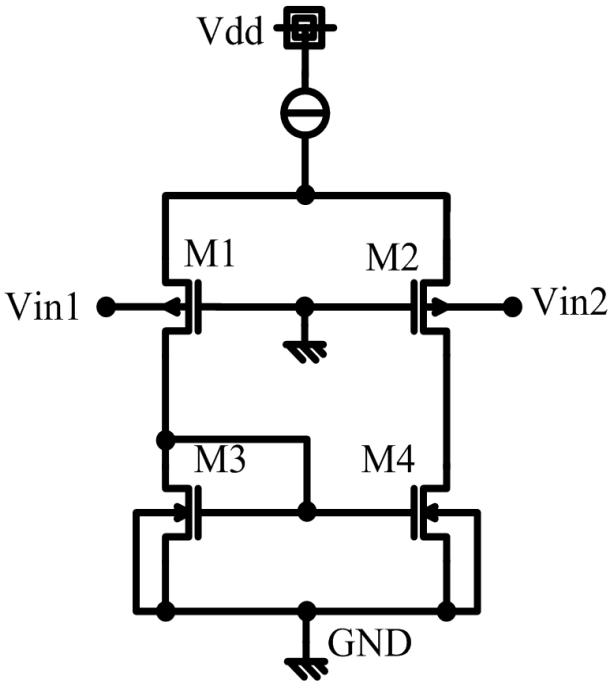

Figure 1.5: Bulk-driven MOSFETs.

of Vt is avoided. The voltage swing for low-voltage supply is increased and minimum operational supply voltage is pushed to its limit [9].

D. Floating-Gate MOSFETs

The floating-gate MOSFET is similar to the conventional MOSFET in the sense that the floating-gate is equivalent to the gate of a conventional transistor, except that the floating-gate voltage Vfg is not controlled directly but by the control gates through capacitance coupling as shown in Fig. 1.6. By some programming techniques, the equivalent Vt can be changed seen from the control gates to have a low Vt MOSFET, but the relatively complex programming circuits and/or higher programming voltage limit its low voltage application [9].

E. Self-Cascode MOSFETs

Self-cascode configuration as shown in Fig. 1.7 can provide a high output impedance with large voltage headroom than conventional cascade structures [9].

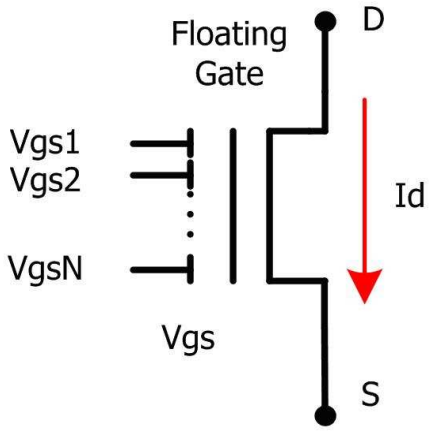

Figure 1.6: Floating-gate MOSFETs.

F. Adaptive Body-Bias Generator

In some digital circuits, various modules or sub-circuits are not necessarily required to operate under a fixed clock. Some of the modules or sub-circuits may be in standby or operating at low performance level, while the other modules or sub-circuits may keep working at their highest performance level. When operation or the switching frequency is high, low threshold voltage is needed. When operation or the switching frequency is low, a high threshold voltage is helpful to reduce the total leakage current. In such a circuit, varying body-bias can achieve optimized performance and power consumption. Thus, an adaptive body-bias generator is highly desirable to vary the body-bise of CMOS circuit. Therefore, a simple adaptive body-bias techniques is proposed in [7]. Adaptive body-bias voltage is generated for various operation frequencies. When operational frequency decreases, body-bias voltage is switched from a forward body-bias to a reverse body-bias [7].

G. Silicon on Insulator (SOI)

Unlike CMOS-based chips that are doped with impurities that enable a chip to store capacitance that must be discharged and recharged, SOI chips are formed by setting transistors on a thin silicon layer that is separated from the silicon substrate

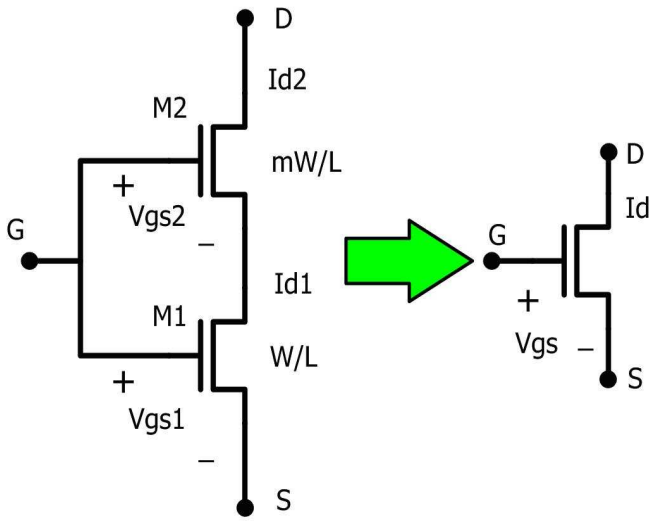

Figure 1.7: Self-cascode MOSFETs.

by an insulating layer of thin silicon oxide or glass, which minimizes capacitance or the energy consumed from the transistor as shown in Fig. 1.8 [10].

One can choose an appropriate technique a combination of these techniques for the intended analog circuit design. However, how to design such low voltage/low power analog circuit is one of most challenging works. There are not well-established design technologies and theories regarding such topics.

1.3 Energy Source for Ubiquitous Device

Table 1.1 illustrates the finite power density of state-of-the-art energy sources [11]. Based on continued advances in power management techniques, it is projected that the power consumption of future low to medium throughput DSPs will be scaled to 10's to 100's of microwatts. Several low-power wireless platforms with power consumption on the order of several to tens of mill watts have recently become commercially available.

Solar cells offer excellent power density in direct sunlight. However, in dim office lighting, or areas with no light, they are inadequate. Power scavenged from thermal gradients is also substantial enough to be of interest if the necessary thermal gradients

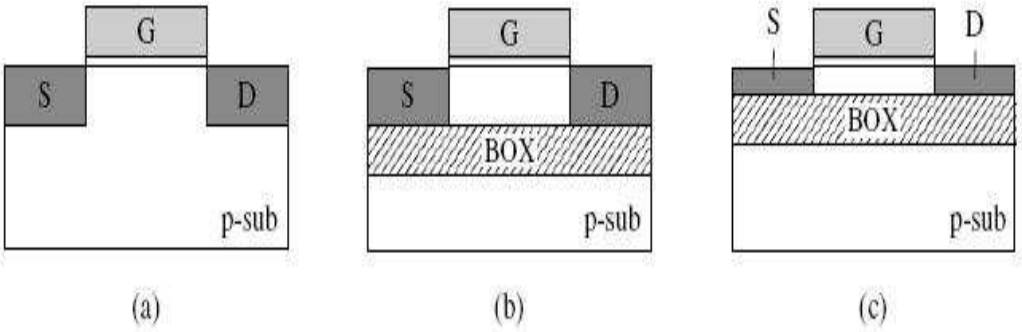

Figure 1.8: nMOST structures for bulk (a), PD-SOI (b), and FD-SOI (c).

Table 1.1: Average power density of various energy storage and scavenging devices.

Power Source	Power Density $\frac{\mu W}{cm^3}$	Lifetime
Lithium Battery	100	1 year
Micro Fuel Cell	110	1 year
Solar Cell	10-15000	∞
Vibrational Converter	375	∞
Air Flow	380	∞
Temperature Gradients	50	∞

are available. Fuel cells represent a potentially large improvement over batteries as an energy reservoir. However, once started, they are not easily turned off.

Therefore, if the lifetime of a sensor node is more than a few years, and sufficient light energy is not available, vibration conversion is an alternative. Low-level mechanical vibrations are available in many environments, and therefore have a potentially wider application domain than some of the sources such as solar, temperature gradient, batteries [11].

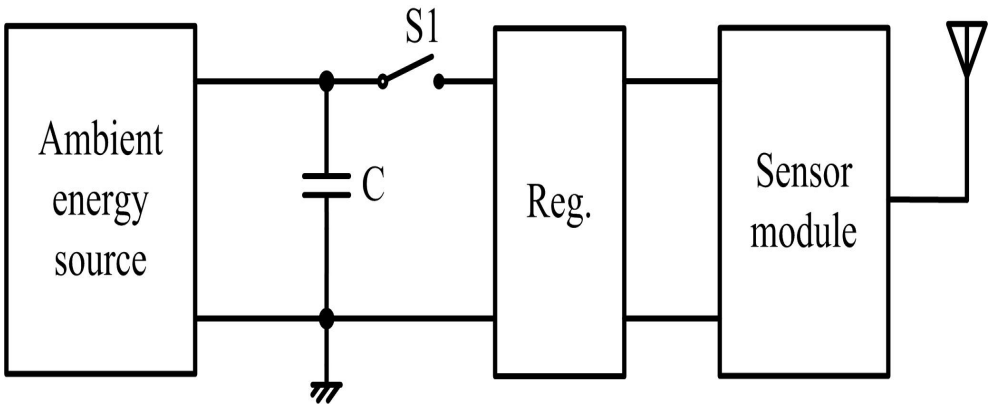

Figure 1.9: Conventional system block diagram [11].

1.4 Conventional Power Management Method

The block diagram of a conventional ubiquitous sensor module is depicted in Fig. 1.9 [11]. A large capacitor C is used to store the ambient energy and a voltage regulator is used to generate a stabilized DC voltage as supply voltage of sensor module. If the energy stored in C is large enough, the switch S1 is turned on to power on the sensor module for a fixed period and then the switch is turned off. Next cycle is repeated in the same way to guarantee that the sensor module can work well with this low duty cycle operation when the input energy is abundant enough [11].

1.5 Our Contributions

Some of the novel ideas proposed in these dissertation are divided into two sections: CMOS low-power design techniques section and power management section. The novel ideas proposed in these dissertation are:

In the low-power design techniques section:

1. A very low-power voltage reference is proposed using body effect.

2. A continuous-time PFD is proposed to realize a fast lock PLL without extra power consumption.

In the power management section:

1. A power management circuit is proposed to manage a variable and weak ambient energy source.

2. A high efficiency charge pump power management circuit is proposed to convert a small or weak input voltage to a higher and stable voltage as power supply voltage for ubiquitous device.

1.6 Thesis Organization

The organization of the dissertation is as follows:

Chapter 1 presents the motivations and backgrounds such as the investigation of low-voltage low-power analog LSI design technologies, energy sources and conventional power management method for ubiquitous device.

Chapter 2 presents a low-power voltage reference using body effect.

Chapter 3 discuses a PLL with proposed continuous-time PFD to realize fast lock without extra power consumption.

Chapter 4 presents a power management circuit to manage a variable and weak ambient energy source.

Chapter 5 describes a high efficiency charge pump power management circuit.

Chapter 6 discusses the conclusions and future works.

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Chapter 2

A LOW-POWER SUB-1-V LOW-VOLTAGE REFERENCE USING BODY EFFECT

In this chapter, the first key cell circuit, a low-power sub-1-V self-biased low-voltage reference, is proposed for low-power electronic applications based on body effect. A voltage reference with low sensitivity to the temperature and supply voltage is one of the key issues in analog circuit designs and the ubiquitous devices demand a novel ultra-low power low-voltage voltage reference. A metal-oxide-semiconductor field effect transistor (MOSFET) can be operated at a lower voltage by forward-biasing the source-substrate junction. This approach has been investigated in detail and used to design an ultra-low power CMOS voltage reference for operation at sub-1 V. The issues of CMOS latchup and leakage have been investigated in detail because of the forward biasing of the substrates of MOSFETs in CMOS. The proposed reference has a very low temperature dependence by using a MOSFET with body effect compared with other reported low-power references. An HSPICE simulation shows that the reference voltage and the total power dissipation are 181 mV and 1.1 μW, respectively. The temperature coefficient of the reference voltage is 33 ppm/°C at temperatures from -40 to 100 °C. The supply voltage can be as low as 0.95 V in a standard CMOS 0.35 μm technology with threshold voltages of about 0.5 V and -0.65 V for n-channel and p-channel MOSFETs, respectively. Furthermore, the supply voltage dependence is -0.36 mV/V (Vdd=0.95$\sim$3.3 V).

2.1 Introduction

A voltage reference with low sensitivity to the temperature and supply voltage is one of the key issues in analog circuit design. The recent advances in Wireless Sensor Network (WSN) technologies have opened up the possibility of powering the sensor nodes by scavenging ambient energies from sunshine, weak electric waves and vibration [1, 2]. These wireless sensor nodes have to operate with low-power supplies. To design such ultra-low-power LSIs, a precision voltage reference with low power dissipation is required. It is expected that the supply voltage of CMOS circuits will be scaled down to about 1 V or less in few years. The conventional bandgap structures will become impractical at that time.

Because the ultra-low-power operation is the stringent energy constraint for the WSN application, the purpose of this work is to propose a low-voltage low-power reference for the ubiquitous sensor nodes. The power dissipation of the whole circuit should be as small as possible [2]. The proposed circuit in this paper can operate at a supply voltage down to 1 V in a standard CMOS 0.35 μm technology with threshold voltages of about 0.5 V and -0.65 V for n-channel and p-channel MOSFETs, respectively. The circuit can work over a large temperature range. Furthermore, no analog process options are required.

Most reported designs on voltage references are lack of low-voltage low-power operation and structurally complicated. Considering CMOS voltage references, the temperature coefficient (T.C.) of a design technique using subthreshold MOSFETs is 119 ppm/°C with a power dissipation of about 4.3 μW from a 1.2 V supply voltage [3]. A CMOS voltage reference, which is based on the weighted difference of the gate-source voltage of two MOSFETs operating in saturation region, is presented in [4]. The minimum supply voltage of this circuit is 1.4 V and the supply current is 9.7 μA. Another new CMOS voltage reference consisting of two pairs of transistors is presented based on gate work function differences in poly-si [5]. Unfortunately,

different conductivity type and impurity concentration of gate electrodes MOSFETs are needed. The voltage references based on threshold voltage subtraction between two MOSFETs [6,7] and threshold voltage summation [8] have been presented. However, both techniques require additional fabrication steps in CMOS technology. The zero-temperature coefficient (ZTC) point has also been used for the design of CMOS voltage references. It is not suitable for the ultra-low-power application due to the several tens microwatts power dissipation [9]. A pure CMOS threshold voltage reference is proposed in [10]. The voltage references based on peaking current source are presented in [11,12]. However, the minimum supply voltages of these circuits are all larger than 1 V.

The body effect describes the change in the threshold voltage by the change in the source-substrate voltage. It is utilized as a bulk-driven differential input stage of an amplifier [13]. Among all the published technologies, little work has been done on how to modify the temperature coefficient of a MOSFET by using body effect and how to realize a low temperature dependence reference by using body effect.

In this paper, the temperature performance of a MOSFET with body effect and the principle of a low temperature dependence voltage reference by using body effect are discussed. A new approach for designing a low-voltage low-power precision voltage reference has been proposed by using forward-biased or reverse-biased body effect.

Later parts of this chapter are organized as follows. Section 2 briefly introduces the conventional architecture. Section 3 discusses the proposed architectures and their principle. Simulation results are given in section 4. The comparison with other reported low-voltage references is discussed in section 5, followed by conclusions in section 6.

2.2 Conventional Architecture

The conventional bandgap voltage reference cannot be designed to have a supply voltage lower than 1.2 V because these circuits generate a voltage of 1.2 V. Therefore,

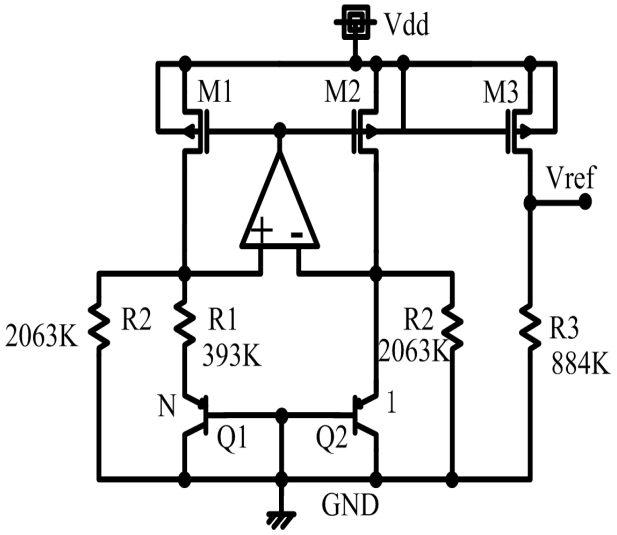

Figure 2.1: A CMOS bandgap reference with sub-1-V operation.

some circuit techniques to scale down the reference voltage are used, and hence the supply voltage can be lower than 1 V [14–17]. One of these circuits is shown in Fig. 2.1 [14].

The reference voltage is given by [14]

$$V_{ref} = \frac{R_3}{R_2}\left[V_{EB2} + \frac{R_2}{R_1} V_T \ln(N)\right], \tag{2.1}$$

where V_T ($= kT/q$, about 26 mV at T = 300 K)is the thermal voltage, k is Boltzmann's constant, q is the electron charge, T is absolute temperature and N is the emitter area ratio of Q1 to Q2. Although these circuits can lower the supply voltage, they suffer from the problem caused by the mismatch between the two R2s in practical IC design. Moreover, these bandgap voltage references require three current branches. Even if the high-gain amplifier can enforce $V_{ds1} = V_{ds2}$, V_{ds3} may not equal to V_{ds1} and V_{ds2}. Therefore, this causes an error voltage, which is supply voltage and temperature dependent, to the reference voltage. In addition, it is hard to reduce the total power dissipation further. From Eq. (2.1), if a larger R1 is required to reduce the total power dissipation, the values of R2 and R3 will be increased correspondingly.

Therefore, a new approach to realize a low-voltage low-power reference is required. The body effect is utilized to realize a sub-1-V self-biased low-voltage low-power reference for micropower electronic applications in the next section.

2.3 Proposed Architectures and Principle

In this section, the architectures and the temperature performance of a MOSFET with body effect, and the principle of a low temperature dependence reference using body effect are discussed.

2.3.1 Proposed Architecture Using Forward-Biased Body Effect

A proposed circuit is shown in Fig. 2.2. It is composed of four MOSFETs (M1-M4) and one resistor (Rb). MOSFETs M1 and M2 are operating in the subthreshold region. The current mirror, composed of M3 and M4, enforces both current branches having a fixed ratio of the current. The diode-connection devices, M1, M2 and Rb, define the current level. The amplifier is used to enforce the two inputs having equal voltage. The reference voltage V_{ref} is the voltage across Rb; the current Ib is the current flow through Rb. Note that the start-up circuit is not shown here.

In this proposed circuit, the substrate node of M1 is connected to its gate node. The substrate-source PN junction of M1 is forward-biased by its gate-source voltage. This circuit has only two current branches and the reference voltage V_{ref} can be directly derived from the the source node of M1 through such back-gate connection, with only one resistor needed. Another proposed circuit with the same principle is shown in Fig. 2.3 by using p-channel MOSFETs M1 and M2.

2.3.2 Principle

The circuit in Fig. 2.2 is used to demonstrate our design principle. Assuming that the channel length is sufficiently long and V_{ds} is the drain-source voltage, the repre-

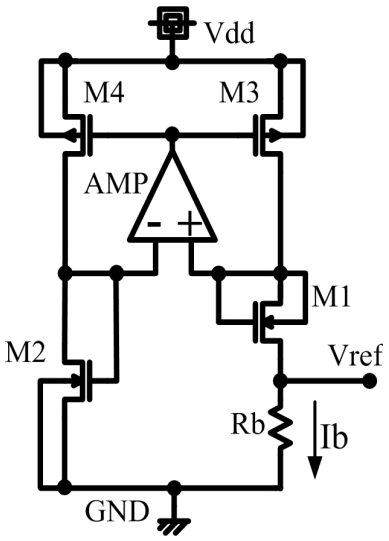

Figure 2.2: Proposed N-MOSFET type reference.

sentation for the gate-to-source voltage in a subthreshold n-channel MOSFET is [18]

$$V_{gs} = V_{th} + nV_T \ln\left[\frac{I_D}{\left(\frac{W}{L}\right)I_t}\right], \tag{2.2}$$

where V_{gs} and V_{th} are the gate-source voltage and threshold voltage of n-channel MOSFET, respectively. Also, n is the subthreshold slope factor, W is the transistor effective width of the channel, L is the transistor effective length of the channel, I_D is the drain current, and I_t is the drain current when $V_{gs} = V_{th}$, $W/L = 1$ and $V_{ds} \gg V_T$.

For n-channel MOSFET devices with substrate bias, the threshold voltage can be expressed in the general form as [18]

$$V_{th} = V_{th0} + \gamma\left(\sqrt{2\phi_B + V_{sb}} - \sqrt{2\phi_B}\right). \tag{2.3}$$

In this equation, V_{th0} is the threshold voltage with zero biased source-substrate voltage, γ is the substrate back-bias factor, ϕ_B is the bulk Fermi potential, and V_{sb} is the source-substrate voltage.

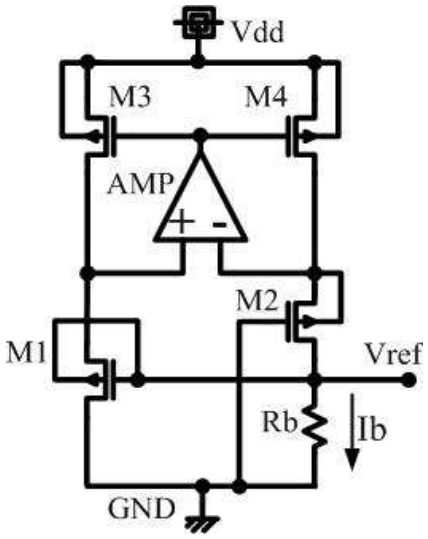

Figure 2.3: Proposed P-MOSFET type reference.

Hence, V_{ref} can be expressed as

$$\begin{aligned} V_{ref} &= V_{gs2} - V_{gs1} \\ &= \gamma\big(\sqrt{2\phi_B} - \sqrt{2\phi_B + V_{sb1}}\big) + nV_T \ln K, \end{aligned} \tag{2.4}$$

where

$$K = \frac{I_{D2}\big(\frac{W}{L}\big)_1}{I_{D1}\big(\frac{W}{L}\big)_2} = \frac{\big(\frac{W}{L}\big)_4\big(\frac{W}{L}\big)_1}{\big(\frac{W}{L}\big)_3\big(\frac{W}{L}\big)_2}. \tag{2.5}$$

Figure 2.2 shows that $V_{sb1} = -V_{gs1}$. Substitute it into Eq. (2.4). Therefore, only V_{gs1}, ϕ_B and V_T are dependent of temperature in Eq. (2.4). Differentiating Eq. (2.4) with respect to temperature T gives

$$\begin{aligned} \frac{\partial V_{ref}}{\partial T} &= \frac{1}{2}\gamma\Big[\big(2\phi_B\big)^{-\frac{1}{2}}\Big(2\frac{\partial \phi_B}{\partial T}\Big) - \big(2\phi_B - V_{gs1}\big)^{-\frac{1}{2}}\Big(2\frac{\partial \phi_B}{\partial T} - \frac{\partial V_{gs1}}{\partial T}\Big)\Big] \\ &\quad + n\frac{V_T}{T}\ln K. \end{aligned} \tag{2.6}$$

In Eq. (2.6), the T.C. of the first term is unknown; on the other hand, the second term has a positive T.C.. Therefore, the temperature performances of ϕ_B and V_{gs1} with a forward-biased body effect should be considered.

Firstly, we discuss the T.C. of V_{gs1} with a forward-biased body effect.

The simple relationship between the surface potential and the gate-source voltage in the subthreshold region is given by [19]

$$V_{gs1} \approx V_{th1} + n(T)[\phi_s(T) - 2\phi_B(T)], \tag{2.7}$$

where ϕ_s is the surface potential. The temperature model of the threshold voltage is [19]

$$V_{th1} = V_{th1}(T_0) + (K_{T1} + K_{T2}V_{bs1})\left(\frac{T}{T_0} - 1\right), \tag{2.8}$$

where $V_{th1}(T_0)$ is the threshold voltage value at T_0, K_{T1} is the T.C. for threshold voltage, and K_{T2} is the body-bias coefficient of the V_{th1} temperature effect. The quantity for $\phi_s(T) - 2\phi_B(T)$ as a function of the temperature results

$$\phi_s(T) - 2\phi_B(T) = [\phi_s(T_0) - 2\phi_B(T_0)]\frac{T}{T_0}, \tag{2.9}$$

and $n(T) \approx n(T_0)$ for temperature in the certain range we consider [3].

Substituting $V_{bs1} = V_{gs1}$, Eq. (2.8) and Eq. (2.9) into Eq. (2.7) and differentiating Eq. (2.7) with respect to temperature T yields

$$\frac{\partial V_{gs1}}{\partial T} \approx \frac{n(T_0)[\phi_s(T_0) - 2\phi_B(T_0)] + K_{T1} + K_{T2}V_{gs1}}{T_0\left[1 - K_{T2}\left(\frac{T}{T_0} - 1\right)\right]}. \tag{2.10}$$

Denote that

$$K_{gs} = \frac{\partial V_{gs1}}{\partial T} \ . \tag{2.11}$$

It is known that ϕ_s belongs to $(\phi_B, 2\phi_B)$ in the subthreshold region, and the typical values of K_{T1} and K_{T2} are -0.11 and 0.022, respectively [19]. $\left[1 - K_{T2}\left(\frac{T}{T_0} - 1\right)\right] > 0$ with T ranging from -40 to 100 °C. V_{gs1} is a subthreshold region gate-source voltage (about 0.3 V) and $n(T_0) \approx 2$. Hence, $K_{gs} < 0$ means that the V_{gs} of an n-channel MOSFET with back-gate connection has a negative T.C..

Secondly, we discuss the T.C. of $\phi_B(T)$.

The expression of $\phi_B(T)$ is [3]

$$\phi_B(T) = \phi_B(T_0)\frac{T}{T_0} - \frac{3kT}{2q}\ln\left(\frac{T}{T_0}\right) + \frac{E_g(T)}{2q} - \frac{E_g(T_0)}{2q}\frac{T}{T_0}, \tag{2.12}$$

where E_g is the energy gap of the silicon, expressed in eV, is [3]

$$E_g(T) = 1.16 - \frac{702\times10^{-6}}{T+1108}T^2. \tag{2.13}$$

Differentiating of Eq. (2.12) with respect to temperature T and denoting that

$$K_B = \frac{\partial\phi_B(T)}{\partial T} = \frac{\phi_B(T_0)}{T_0} - \frac{3k}{2q}\ln\left(\frac{T}{T_0}\right) - \frac{3k}{2q} - 702\times10^{-6}\frac{T^2+2216T}{2q(T+1108)^2} - \frac{E_g(T_0)}{2qT_0}. \tag{2.14}$$

$\phi_B(T_0)$ can be calculated by [3]

$$\phi_B(T_0) = \frac{kT_0}{q}\ln\left[\frac{N_{CH}}{n_i(T_0)}\right], \tag{2.15}$$

where N_{CH} is channel doping concentration, and $n_i(T)$ is the intrinsic carrier concentration.

K_B is about -0.7 mV/°K at T = 300 K by using Eqs. (2.14) and (2.15) . The V_{gs} has a negative T.C. on the order of -2 mV/K. Hence, the first term of Eq. (2.6) has a negative T.C..

Therefore, to make the T.C. of V_{ref} equal to zero at a selected temperature T_0, is to make

$$\left.\frac{\partial V_{ref}}{\partial T}\right|_{T=T_0} = 0. \tag{2.16}$$

Thus K can be calculated by

$$K = \exp\left\{\frac{1}{2}\gamma\left[\left(2\phi_B - V_{gs1}\right)^{-\frac{1}{2}}\left(2\frac{\partial\phi_B}{\partial T} - \frac{\partial V_{gs1}}{\partial T}\right) - \left(2\phi_B\right)^{-\frac{1}{2}}\left(2\frac{\partial\phi_B}{\partial T}\right)\right]\Big/\left(n\frac{V_T}{T}\right)\right\}\Bigg|_{T=T_0}. \tag{2.17}$$

Substituting Eqs. (2.11) and (2.14) into Eq. (2.17) gives

$$K = \exp\left\{\frac{1}{2}\gamma\left[\frac{2K_B(T_0) - K_{gs}(T_0)}{\sqrt{2\phi_B(T_0) - V_{gs1}(T_0)}} - \frac{2K_B(T_0)}{\sqrt{2\phi_B(T_0)}}\right]\Big/\left(\frac{nk}{q}\right)\right\}. \tag{2.18}$$

Remember that K is the product of the size ratio of M1 to M2 and the size ratio of M4 to M3.

Note that the source-substrate junction of M1 is forward biased. Hence, the threshold of M1 is reduced and the M1 must work in subthreshold region to avoid turning on the PN junction.

The gate-source voltage temperature characteristics of M1 with and without forward-biased connection are shown in Fig. 2.4. The horizontal axis is temperature; the vertical axis is V_{gs}. The difference between V_{gs2} and V_{gs1} with forward-biased connection is the reference voltage V_{ref}. It is evident that the threshold of M1 is reduced and the difference between V_{gs2} and V_{gs1} without forward-biased connection increases with temperature increasing as usual. On the other hand, the difference between V_{gs2} and V_{gs1} with forward-biased connection (V_{ref}) almost keeps constant with temperature increasing. From Eq. (2.10), the last term of numerator and the denominator are the factors introduced by the forward-biased body effect. Since the K_{T2} is 0.022 and Vgs1 is about 0.3 V, the last term of numerator has very little influence to the T.C. of Vgs1. The T.C. of Vgs1 is mainly influenced by the denominator. The K_{T2} and T_0 are constants in the denominator of Eq. (2.10), therefore, the denominator decreases almost linearly with temperature increasing. Furthermore, the denominator is positive within the temperature range we are considering and the absolute value of the denominator decreases almost linearly with temperature increasing. Hence, the T.C. of Vgs1 with forward-biased body effect is linear and a litter larger than the T.C. of Vgs1 without body effect. So, the T.C. of a MOSFET M1 with forward-biased connection can be modified the same as the T.C. of a MOSFET M2 without forward-biased connection if an appropriate K is selected. Therefore, a V_{ref} voltage independent of temperature can be obtained by using Eq. (2.18). In general, the size ratios of M1 to M2 and M4 to M3 are selected due to the trade-off between the total power dissipation and the layout matching characteristics.

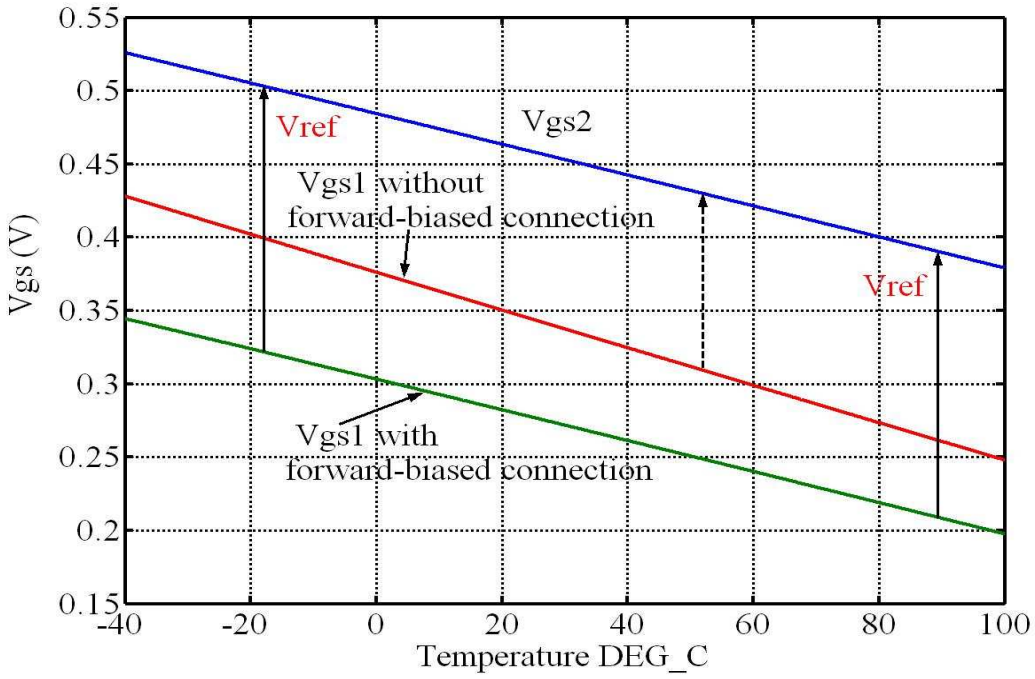

Figure 2.4: V_{gs} comparison with forward-biased connection.

2.3.3 Voltage Reference Using Reverse-Biased Body Effect

A low temperature dependence voltage reference also can be realized by using a reverse-biased body effect. The proposed circuit is depicted in Fig. 2.5. It is composed of six MOSFETs and one resistor (Rb). MOSFETs M1, M2, Md1 and Md2 are operating in the subthreshold region. The current mirror composed of M3 and M4 enforces both current branches having a fixed ratio of the current. The diode-connection devices M1, M2 and Rb define the current level. The amplifier is used to enforce the two inputs having equal voltage. The reference voltage V_{ref} is the voltage across Rb; the current Ib is the current flow through Rb. Note that the start-up circuit is not shown here.

In this circuit, the substrate nodes of all MOSFETs are connected to their source nodes except M1. The substrate-source PN junction of M1 is reverse-biased by Md1.

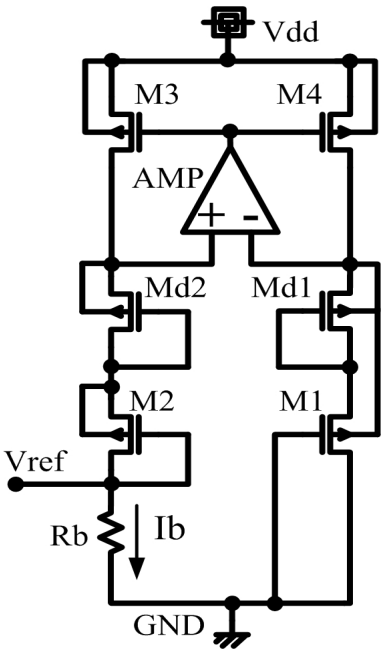

Figure 2.5: Proposed voltage reference using reverse-biased body effect.

Let V_{sgMd1} be the same as V_{sgMd2}, then the voltage V_{ref} is given by

$$V_{ref} = V_{sgM1} - V_{sgMd2}. \tag{2.19}$$

To simplify the analysis, the source-gate voltage of Md1 can be expressed as [3]

$$V_{sgd1} = V_{th}(T_0) + K_{Md1}\big(\frac{T}{T_0} - 1\big), \tag{2.20}$$

where K_{Md1} is the T.C. of V_{sgMd1} and it is a negative quantity. Based on the Eqs. (2.7), (2.8), (2.9) and (2.20), the temperature performance of V_{sgM1} with reverse-biased connection is then equal to

$$\begin{aligned}\frac{\partial V_{sgM1}}{\partial T} \approx & \frac{K_{T1} + n(T_0)[\phi_s(T_0) - 2\phi_B(T_0)]}{T_0} \\ & + \frac{K_{T2}}{T_0}\big[K_{Md1}\big(\frac{T}{T_0} - 1\big) + V_{sgMd1}\big].\end{aligned} \tag{2.21}$$

In this equation, the first term is the T.C. of M1 without body effect; the second term is the additional effect caused by the reverse-biased body effect. Note that

the source-substrate junction of M1 is reverse-biased. Hence, the absolute value of threshold voltage of M1 is increased.

The source-gate voltage temperature characteristics of M1 with and without reverse-biased connection are shown in Fig. 2.6. The horizontal axis is temperature; the vertical axis is V_{sg}. The difference between V_{sg1} with reverse-biased connection V_{sg2} is the reference voltage V_{ref}. It is evident that the threshold voltage of M1 is increased and the difference between V_{sg1} without reverse-biased connection and V_{sg2} increases with temperature increasing as usual. On the other hand, the difference (V_{ref})between V_{sg1} with reverse-biased connection and V_{sg2} almost keeps constant with temperature increasing. From Eq. (2.21), since the second term $\frac{K_{T2}}{T_0}\left[K_{Md1}\left(\frac{T}{T_0}-1\right)+V_{sgMd1}\right]$ is positive and decreases with temperature, it causes that the T.C. of M1 with reverse-biased connection is smaller than the T.C. of M1 without reverse-biased connection. So, the T.C. of a MOSFET M1 with reverse-biased connection can be modified the same as the T.C. of a MOSFET M2 without reverse-biased connection if an appropriate size ratio of M1 to M2 and M3 to M4 is selected. Therefore, a V_{ref} voltage independent of temperature can be obtained by using a reverse-biased body effect.

In summary, the merits of the voltage reference using body effect are: (1) The body effect is utilized to modify the threshold voltage of a MOSFET to get an appropriate quantity of V_{ref}. (2) The temperature coefficient of a MOSFET with body effect can be modified. (3) The biased voltage between source and substrate node is a dynamic voltage varying with temperature.

2.4 Circuit Implementation and Simulation Results

In this paper, the proposed reference using forward-biased body effect is used to verify the principle.

The minimum required power supply for the proposed circuit is given by

$$Vdd_{min} = V_{gs2} + V_{ds4}. \tag{2.22}$$

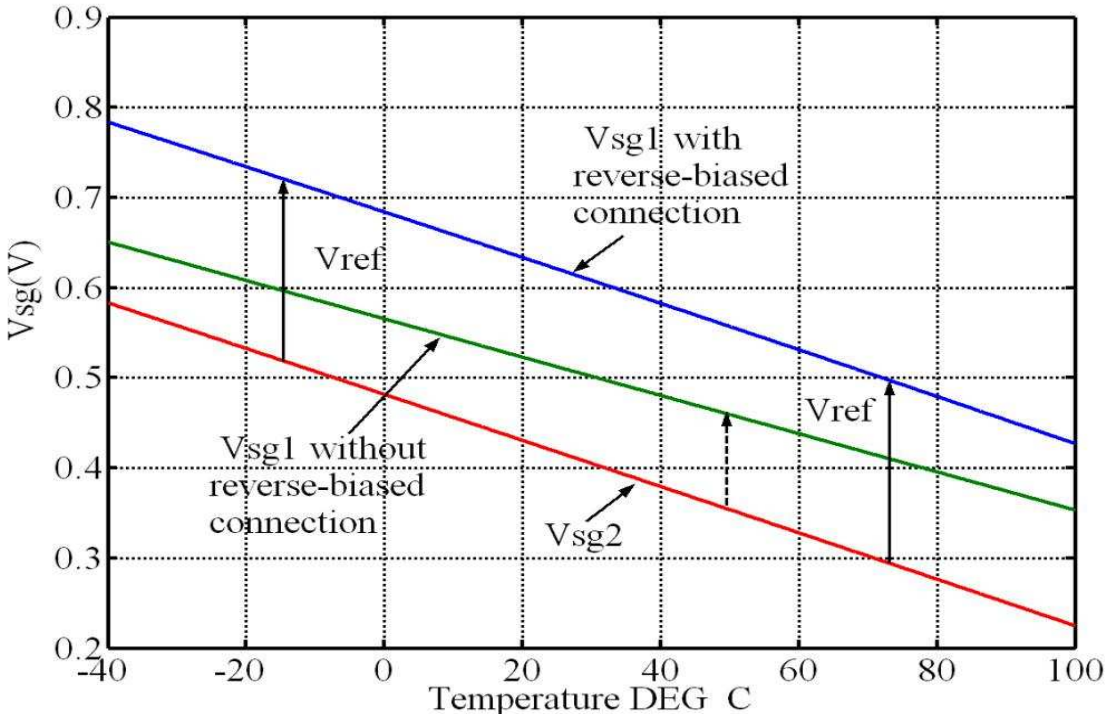

Figure 2.6: V_{sg} comparison with reverse-biased connection.

2.4.1 Voltage Reference

The detailed sizes of MOSFETs as well as resistor value for the voltage reference are shown in Table 2.1. The K is equal to 13.2. T_0 is designed as 300 K.

The supply voltage dependence of the proposed voltage reference is shown in Fig. 2.7. The supply voltage dependence at T=300 K is -0.36 mV/V.

The typical temperature dependence of the proposed voltage reference is shown in Fig. 2.8. The typical value of V_{ref} is 181 mV at a 0.95 V supply voltage. The reference voltage variation is 0.28 mV (0.15 %) within the temperature range from -40 to 100 °C. And the corner analysis results are shown in Table 2.2. The typical T.C. of V_{ref} is 11 ppm/°C. However, the absolute values of V_{ref} vary according to different corner analysis because of the threshold voltage variation. This problem will be solved as the technology advancements [10].

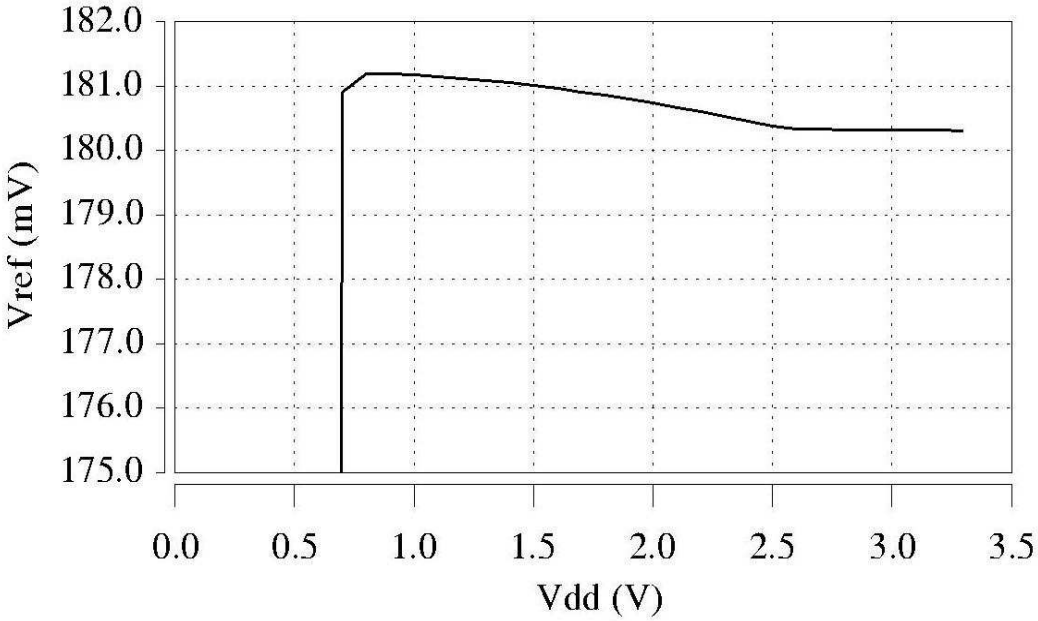

Figure 2.7: Supply voltage dependence of V_{ref}.

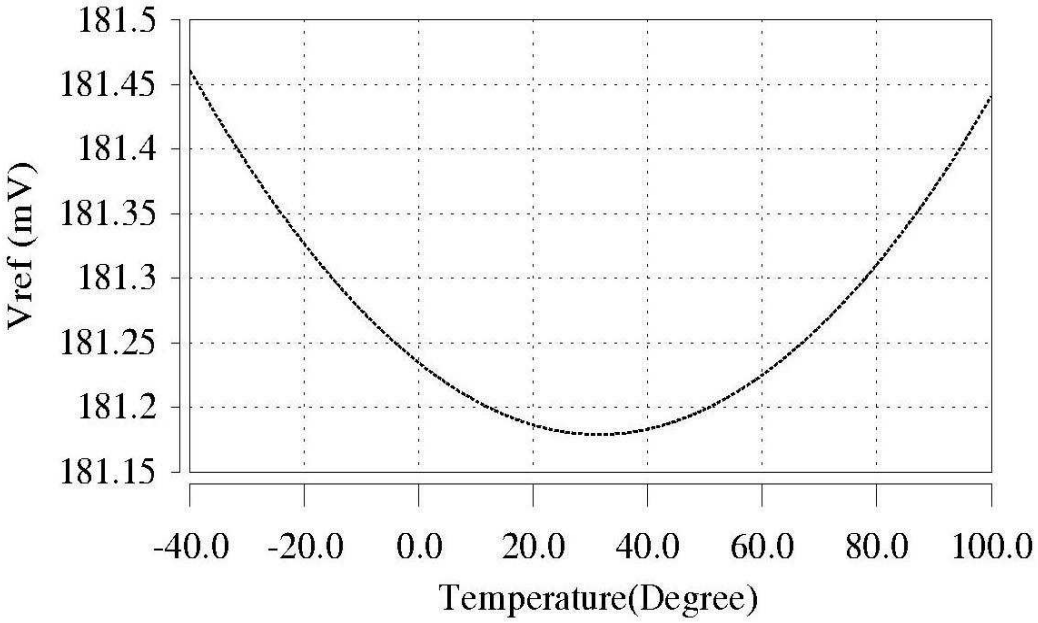

Figure 2.8: Temperature dependence of V_{ref} at a 0.95 V supply voltage.

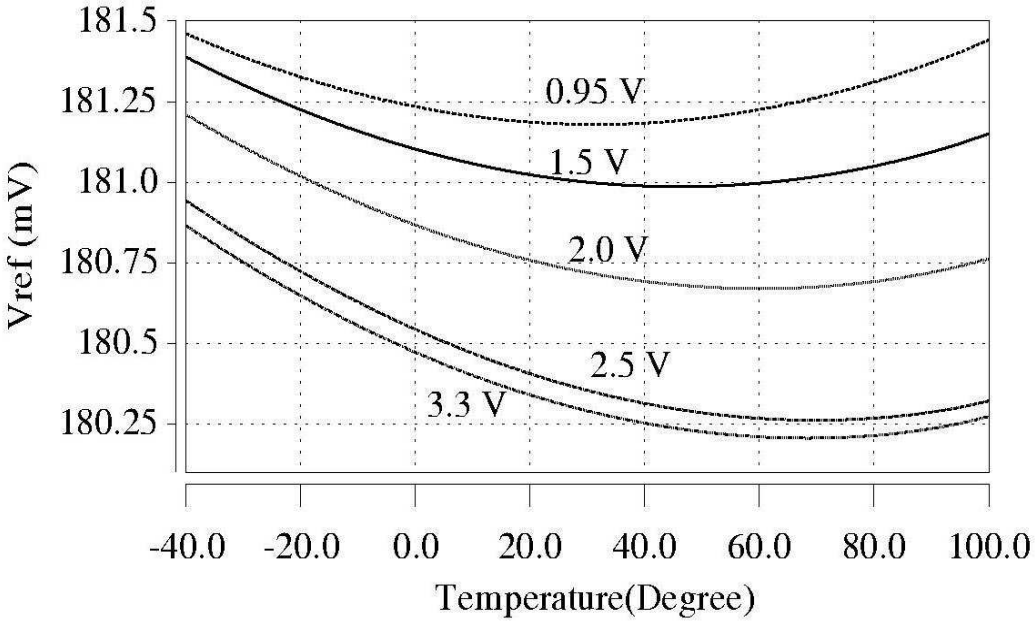

Figure 2.9: Temperature dependences of V_{ref} at different supply voltages.

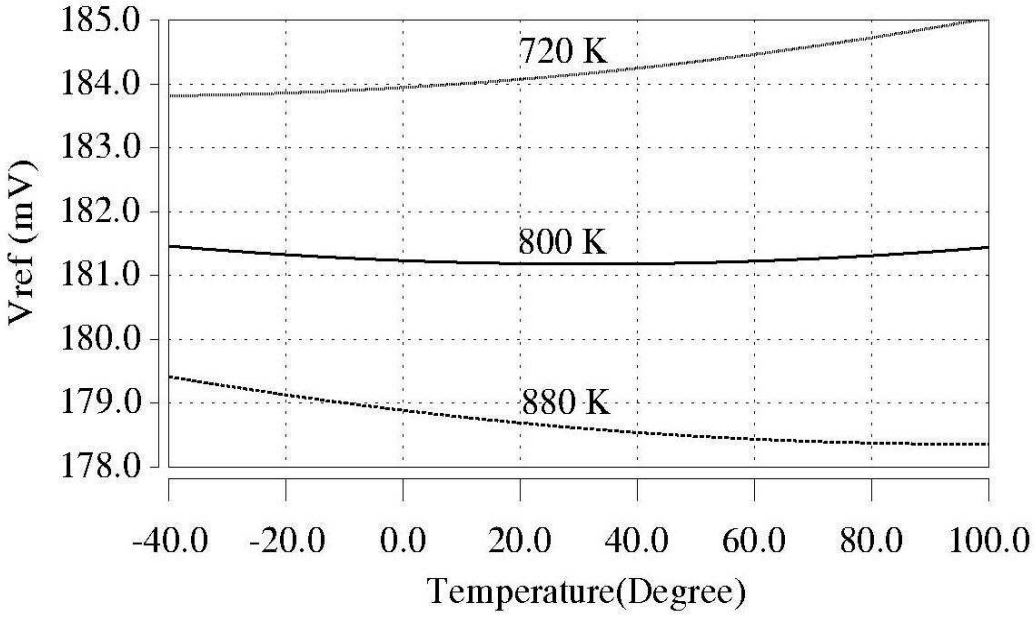

Figure 2.10: Temperature dependences of V_{ref} with different values of Rb.

Table 2.1: Circuit parameters.

Element	Value
M1	188/10 μm
M2	50/10 μm
M3	10/10 μm
M4	35/10 μm
Rb	800 kΩ

Table 2.2: Corner analysis.

Type	T.C.	V_{ref}
TT	11 ppm/°C	181.18 mV
SS	33 ppm/°C	211.2 mV
SF	33 ppm/°C	211.2 mV
FS	24 ppm/°C	151.2 mV
FF	24 ppm/°C	151.1 mV

The temperature dependences of V_{ref} at different supply voltages (Vdd= 0.95, 1.5, 2.0, 2.5, 3.3) are shown in Fig. 2.9. The voltage V_{ref} at 300 K are 181.2 mV and 180.3 mV at a 0.95 V and 3.3 V supply voltage, respectively. The T.C. at Vdd=0.95 V is 11 ppm/°C and increases to 21 ppm/°C at Vdd=3.3 V.

The temperature dependences of V_{ref} with different values of Rb is shown in Fig. 2.10. The results are tabulated in Table 2.3. The T.C. at Rb=800 K is 11 ppm/°C and increases to 35 ppm/°C at Rb=720 K.

The substrate leakage current of M1 is shown in Fig. 2.11. The leakage current increases with temperature increasing even if $Vsb1$ decreases with temperature increasing. The leakage current is 200 pA at 100°C with a $Vsb1$ of 200 mV. It is negligible compared with Ib (226 nA).

Table 2.3: Performances with different values of Rb.

Rb	V_{ref}	T.C.
800 K	181.2 mV	11 ppm/°C
880 K	178.7 mV	12 ppm/°C
720 K	184.1 mV	35 ppm/°C

2.4.2 Amplifier

The amplifier proposed in [20] is adopted for the proposed reference. The common-mode feedback is implemented in the input differential pair stage of the amplifier to reduce the minimum supply voltage.

2.5 Comparison with Other Reported Low-Voltage References

The circuit proposed by Banba in Fig. 2.1 is simulated with the same standard 0.35 μm CMOS process to be compared with ours. The results compared with other reported low-voltage references are tabulated in Table 2.4. Note that the reported voltage references [3, 12, 16] are chip measurement results. As shown in the table, the minimum supply voltage, the supply current and the power dissipation including both amplifier and start-up circuit of the proposed reference are the lowest, and at the same time it can provide comparable performance on T.C. with sub-1-V supply operation. Moreover, the supply voltage dependence of the proposed circuit is the best because the proposed reference only has two current branches. In addition, the architecture of the proposed reference is simple.

2.6 Conclusions

A new approach for designing a low-voltage low-power precision voltage reference has been proposed by using forward-biased or reverse-biased body effect. The simulation results demonstrate that the variations in the reference voltage can be kept very

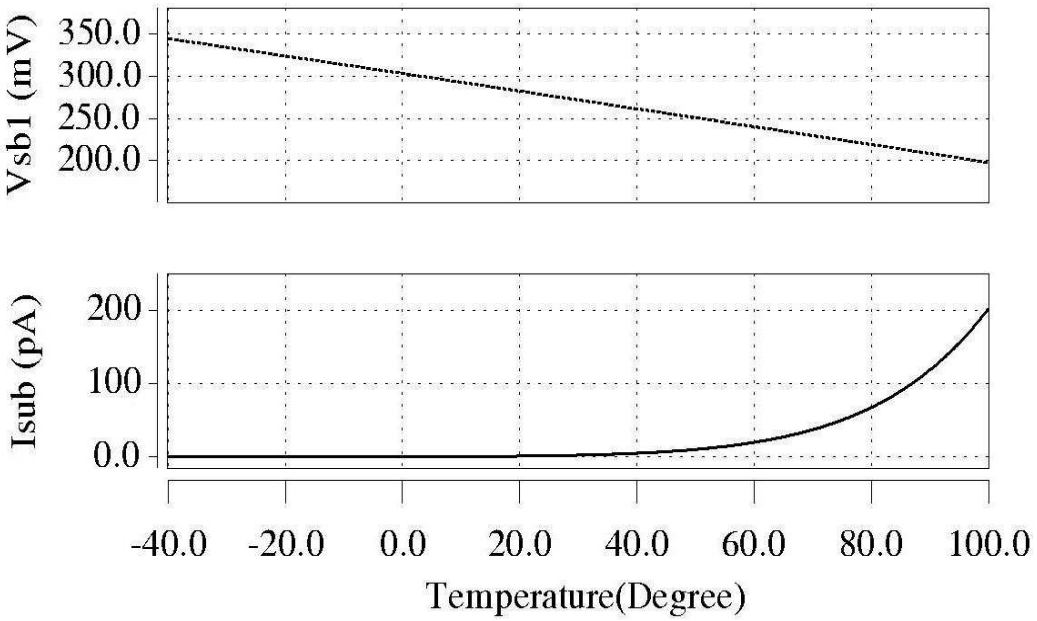

Figure 2.11: Substrate leakage current.

small within a temperature range from -40 to 100 °C by modifying the T.C. of a MOSFET with body effect. The proposed reference can operate at a supply voltage down to 0.95 V in a standard CMOS 0.35 μm technology with threshold voltages of about 0.5 V and -0.65 V for n-channel and p-channel MOSFETs, respectively. The minimum power dissipation is 1.1 μW and the supply voltage dependence is -0.36 mV/V (Vdd=0.95$\sim$3.3 V). No particular analog process options are required. This circuit with a simple architecture is suitable for low-voltage micro-power electronic applications.

Table 2.4: Comparison with other reported low-voltage references.

	This work	Banba [14]	Leung [16]	Cheng [12]	Giustolisi [3]
Technology	0.35 μm CMOS		0.6 μm CMOS	0.35 μm CMOS	1.2 μm CMOS
V_{th}	V_{thp}= -0.65 V V_{thn}= +0.50 V		V_{thp}= -0.91 V V_{thn}= +0.53 V	-	V_{thp}= -1.05 V V_{thn}= +0.77 V
Min. Vdd	0.95 V	1.20 V	0.98 V	1.4 V	1.2 V
Supply Current	1.2 μA	1.95 μA	18.0 μA	2.3 μA	3.6 μA
P_{Vdd}	1.1 μW	2.34 μW	17.6 μW	3.2 μW	4.3 μW
V_{ref}	181 mV	519 mV	603 mV	580 mV	295 mV
T.C.	33 ppm/°C	17 ppm/°C	15 ppm/°C	62 ppm/°C	119 ppm/°C
Supply Voltage Dependence at 27°C	-0.36 mV/V	-3.8 mV/V	4.2 mV/V	3.9 mV/V	-

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Chapter 3

A FAST LOCK PHASE-LOCKED LOOP USING A CONTINUOUS-TIME PHASE FREQUENCY DETECTOR

In this chapter, the second key cell circuit, a fast lock charge pump phase-locked loop (CPPLL) is proposed. The low-power PLL design technique is also one of the key issues in analog circuit designs. To realize fast lock without extra power dissipation, a continuous-time phase frequency detector (PFD) based on the conventional tri-state PFD is proposed. The locking time of the PLL can be substantially reduced with the proposed continuous-time scheme. During the period that the best tracing and acquisition properties are required, the bandwidth of the PLL can be increased to decrease the locking time with the proposed continuous-time PFD. Afterwards, the bandwidth of the PLL is recovered to the original value to minimize output jitter due to external noise. Therefore, the proposed architecture can achieve fast lock without extra power dissipation. Any conventional tri-state PFDs can be improved with the proposed continuous-time architecture. The proposed architecture is realized in a standard CMOS 0.35 μm technology. The simulation results demonstrate that the proposed continuous-time PFD is effective to get more speedy locking time without extra power dissipation.

3.1 Introduction

The PLLs find wide applications in high-speed data communication systems such as clock-and-data recovery, microprocessor-clock generation, and frequency synthesis. The PLLs efficiently perform clock recovery or clock generation with low-noise or low-jitter clock signals and at the same time need to achieve fast locking [1, 2].

However, there exits a tradeoff in selecting the PLL bandwidth. The transfer function from the input noise source to the PLL output is lowpass. Therefore, the loop bandwidth should be made as narrow as possible to minimize output phase jitter due to external noise. The transfer function from internal oscillator noise source to the PLL output is found to be highpass. Therefore, the loop bandwidth should be made as wide as possible to minimize output jitter due to internal oscillator noise and to obtain best tracking and acquisition properties [3].

In the conventional PLL design, a narrow-band loop filter is used to reduce output jitters at a cost of large capacitor and resistor. In order to improve the locking time characteristics, various structures have been proposed for the developments of the conventional PLLs [2–7]. However, the proposed schemes might cause some problems such as a larger power dissipation, larger chip size, or a significant amount of phase noise.

Currently, the research works about PFDs mainly focus on how to reduce dead zone with high frequency operation [8–10]. The PFD is used to detect phase difference of two inputs and generates two pulse signals for driving the charge pump. The two output signals are discontinuous signals in the conventional technologies. In this paper, a continuous-time PFD is proposed to generate continuous signals based on the conventional tri-state PFD to drive the following charge pump circuit. With the proposed scheme, when the phase difference is larger than a preset value, the loop bandwidth of the PLL is expanded to obtain best tracking and acquisition properties. After the phase difference is reduced within the preset value, the loop bandwidth of the PLL is recovered to the original value to minimize output phase jitter due to external noise [11].

This chapter is organized as follows. Section 2 introduces the proposed architecture and its principle. Simulation results are given in section 3. The comparison with other reported PLLs is discussed in Section 4 followed by conclusions in section 5.

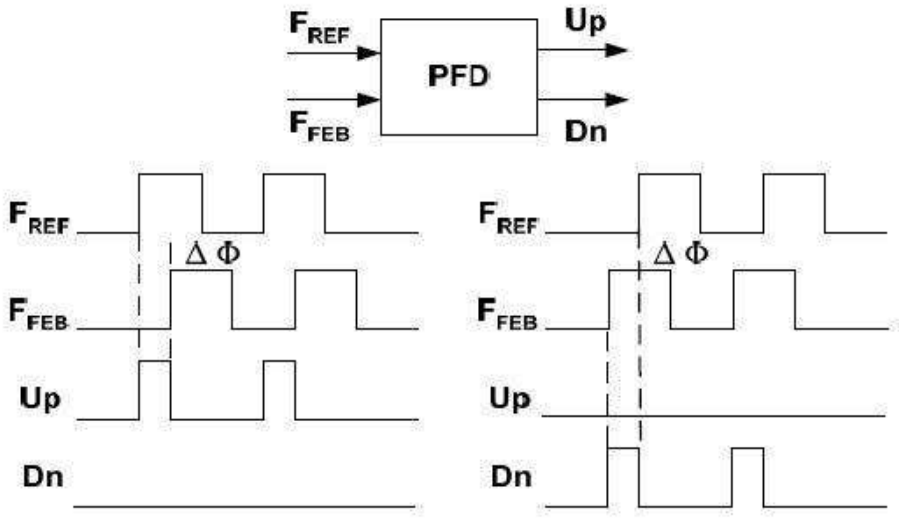


Figure 3.1: Timing diagram of conventional PFD.

3.2 Proposed Architecture and Principle

A charge pump PLL is composed of five major blocks: PFD, charge pump, loop filter, voltage-controlled oscillator (VCO) and frequency divider. The PFD is a tri-state machine. The timing diagram of the conventional PFD is depicted in Fig. 3.1. The PFD can detect the phase and frequency difference between F_{FEF} and F_{FEB}. Then, it generates an Up signal if F_{FEF} leads F_{FEB} or a Dn signal if F_{FEF} lags F_{FEB}.

The open loop transfer function of the conventional charge pump PLL is given by [12]

$$G_s = \frac{I_{cp} \cdot F(s) \cdot K_{VCO}}{2\pi \cdot s \cdot N}, \tag{3.1}$$

where I_{cp} is the charge pump current, $F(s)$ is the transfer function of the loop filter, K_{VCO} is the VCO gain and N is the frequency divider modulus.

For a third-order PLL, the loop bandwidth is approximately [1]

$$\omega_{BW} \cong \frac{I_{cp} \cdot K_{VCO} \cdot R_2}{2\pi \cdot N}. \tag{3.2}$$

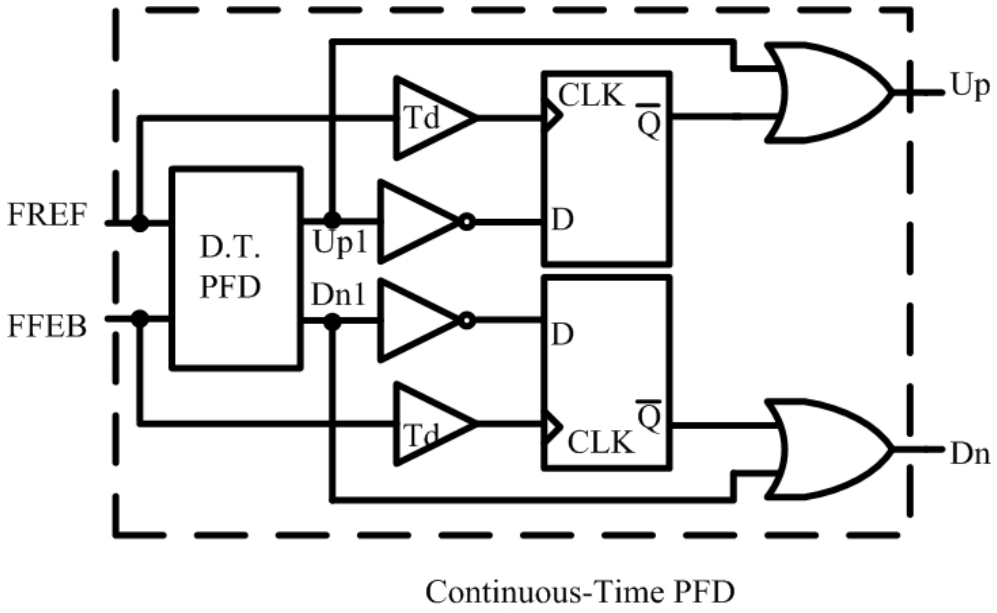


Figure 3.2: Block diagram of proposed continuous-time PFD.

The natural frequency (ω_N) and the damping factor (ζ) are given by [1]

$$\omega_N \cong \sqrt{(I_{cp}K_{VCO})/(2\pi NC_2)}, \tag{3.3}$$

$$\zeta \cong \omega_N R_2 C_2/2, \tag{3.4}$$

where C_2 and R_2 are the capacitance and resistor in the loop filter.

3.2.1 Proposed Continuous-Time PFD

The block diagram of the proposed continuous-time PFD is shown in Fig. 3.2. It is based on the conventional tri-state PFD [13] and is composed of a conventional PFD, two delay cells, two D flip-flops (DFFs), two OR gates and two inverters.

The delay cells are used to generate a delay Td which should be larger than the dead zone of the conventional tri-state PFD. The reference frequency and feedback frequency are delayed by Td and then feed two DFFs with input CLK, respectively. The outputs of conventional PFD Up1 and Dn1 are distributed into the input D of

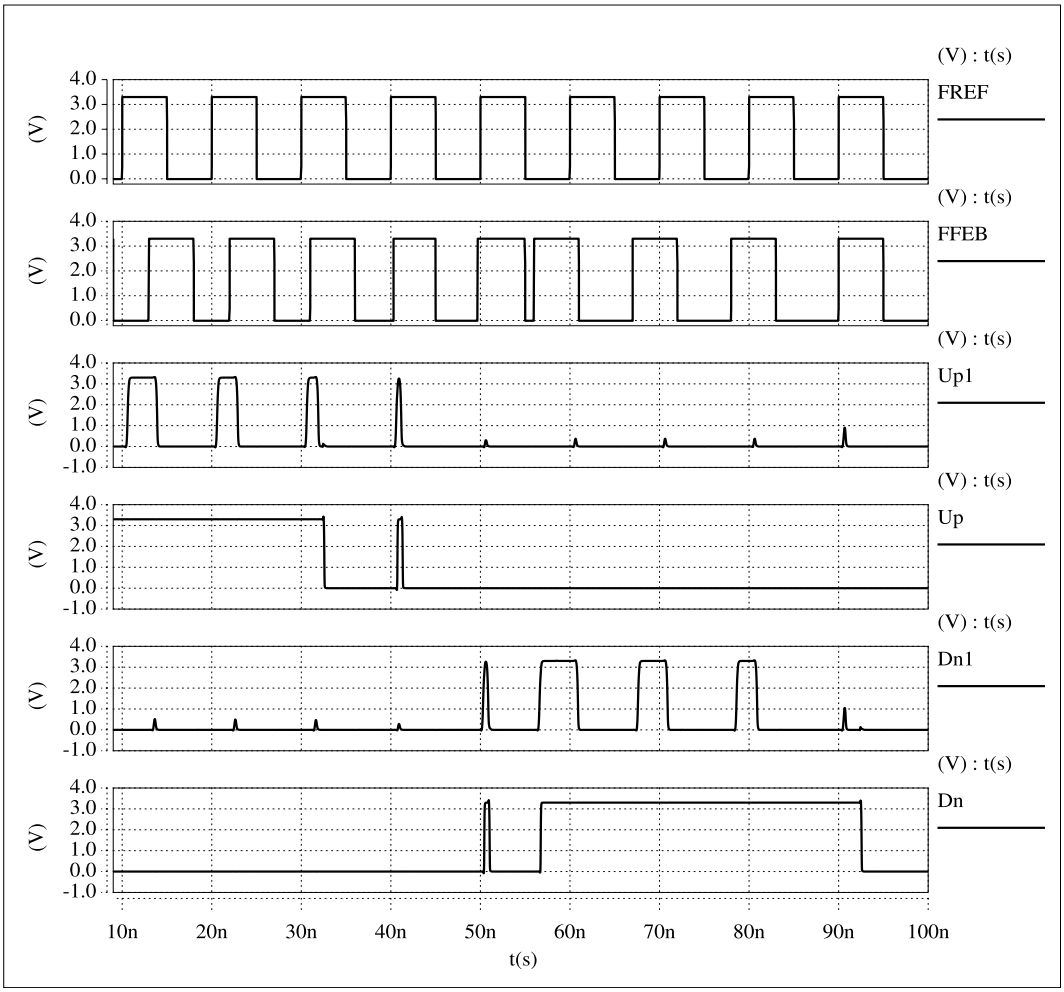


Figure 3.3: Timing diagram of proposed continuous-time PFD.

two DFFs via two inverters, respectively. Afterwards, $\bar{Q}$ of DFF with Up1 and Dn1 are connected to the OR gates, respectively. Then, the two OR gates generate the final output signals Up and Dn for driving the charge pump circuit.

Therefore, when the pulse width of Up1 or Dn1 is larger than Td, $\bar{Q}$ of DFF is high and its state is sustained during this whole period of reference frequency to realize coarse-tuning. If the following pulse width is still larger than Td, the high state is sustained during the following period. If the following pulse width is less than

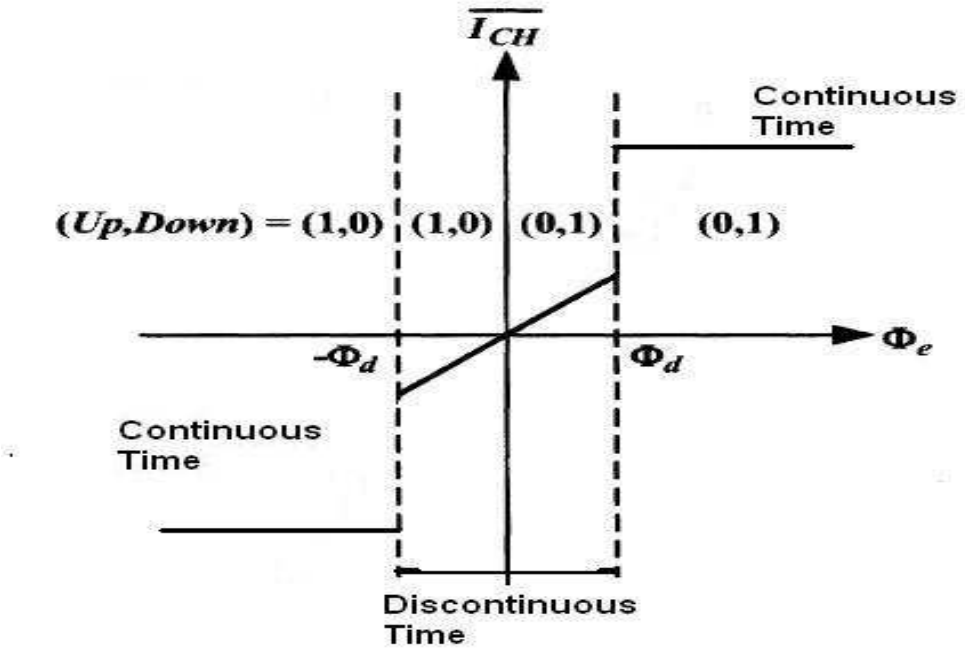


Figure 3.4: Transfer function curve of proposed continuous-time PFD.

Td, $\bar{Q}$ of DFF is low. The continuous-time architecture is disabled and the output pulse width of Up or Dn is the same as the narrow width of Up1 or Dn1 to realize fine-tuning. Therefore, the proposed architecture can achiever fast lock without extra power dissipation.

The timing diagram of the proposed continuous-time PFD is shown in Fig. 3.3. As shown in this figure, Up1 and Dn1 are discontinuous signals. For the Up and Dn signals, when the pulse width of Up1 or Dn1 is larger than Td, the corresponding output of Up or Dn is a continuous signal. When the pulse width of Up1 or Dn1 is less than Td, the corresponding output of Up or Dn becomes a discontinuous signal with the same pulse width as Up1 or Dn1.

The transfer function curve of proposed continuous-time PFD is depicted in Fig. 3.4. According to the timing diagram, the continuous-time architecture is activated only when the pulse width of Up1 or Dn1 is larger than Td. The proposed architecture is

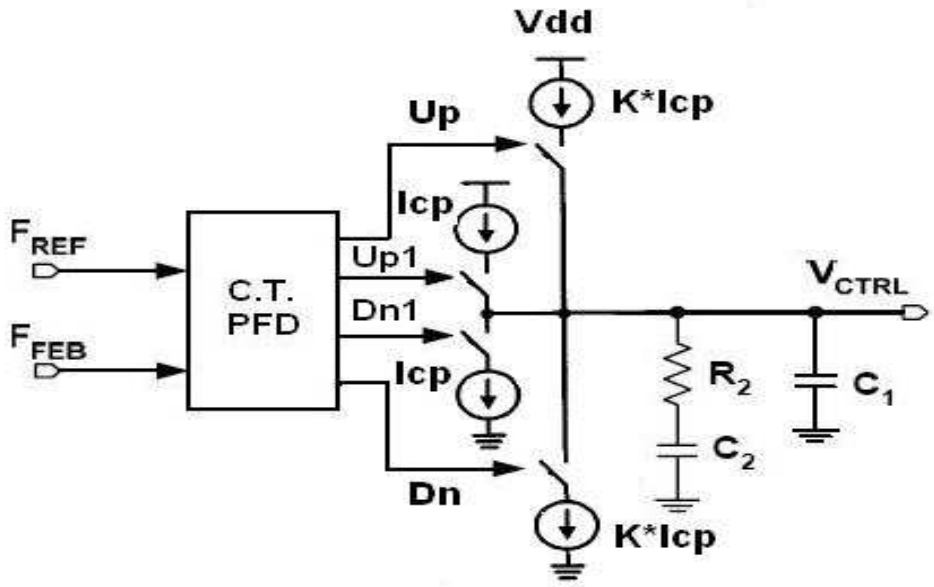


Figure 3.5: Proposed PLL using continuous-time PFD.

used to realize coarse-tuning because more current will be charged into or discharged from the loop filter. Therefore, the phase difference can be reduced rapidly to decrease the locking time. When the pulse width of Up1 or Dn1 is reduced within Td, only the conventional PFD works to realize fine-tuning. As illustrated in Fig. 3.4, the average charge pump current of the continuous-time operation is much larger than that of the discontinuous-time operation. The gain of conventional PFD with charge pump is given by

$$K_d = \frac{I_{cp}}{2\pi}. \tag{3.5}$$

Therefore, when the pulse width of Up1 or Dn1 is larger than Td, the transfer function of the proposed continuous-time PFD with charge pump can be expressed as

$$|K_d| = KI_{cp}, \qquad (|\Phi_e| \geq \Phi_d) \tag{3.6}$$

where K means that the charge pump current in the continuous-time operation is K

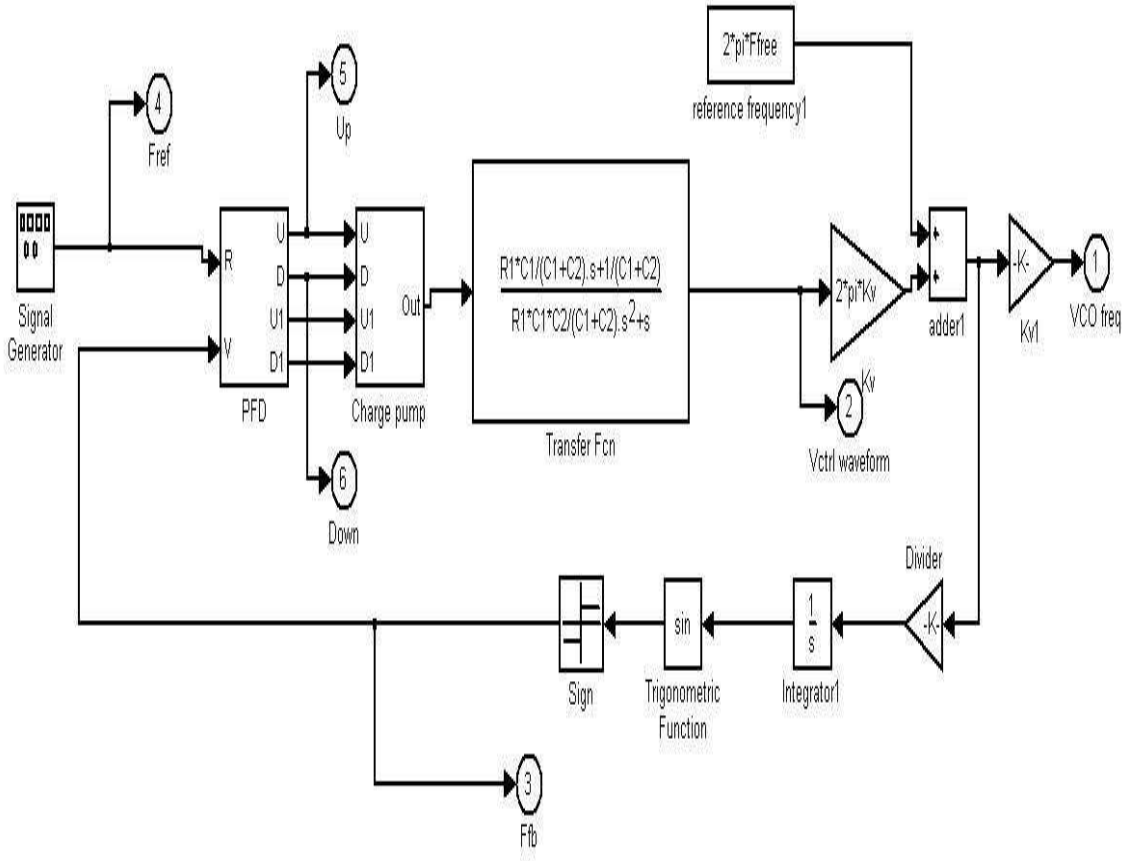


Figure 3.6: The whole proposed PLL behavioral model.

times larger than the charge pump current in the discontinuous-time operation.

3.2.2 Proposed PLLs with Continuous-Time PFD

The proposed continuous-time architecture can be used to improve any conventional tri-state PFDs. A PLL has been shown using the proposed continuous-time PFD in Fig. 3.5. In this proposed PLL, a continuous-time PFD takes the place of the conventional discontinuous-time PFD. In the charge pump circuit, the first and the second charge/discharge current paths are controlled by the discontinuous-time signals and the continuous-time signals, respectively. When the PLL is in the out of lock state

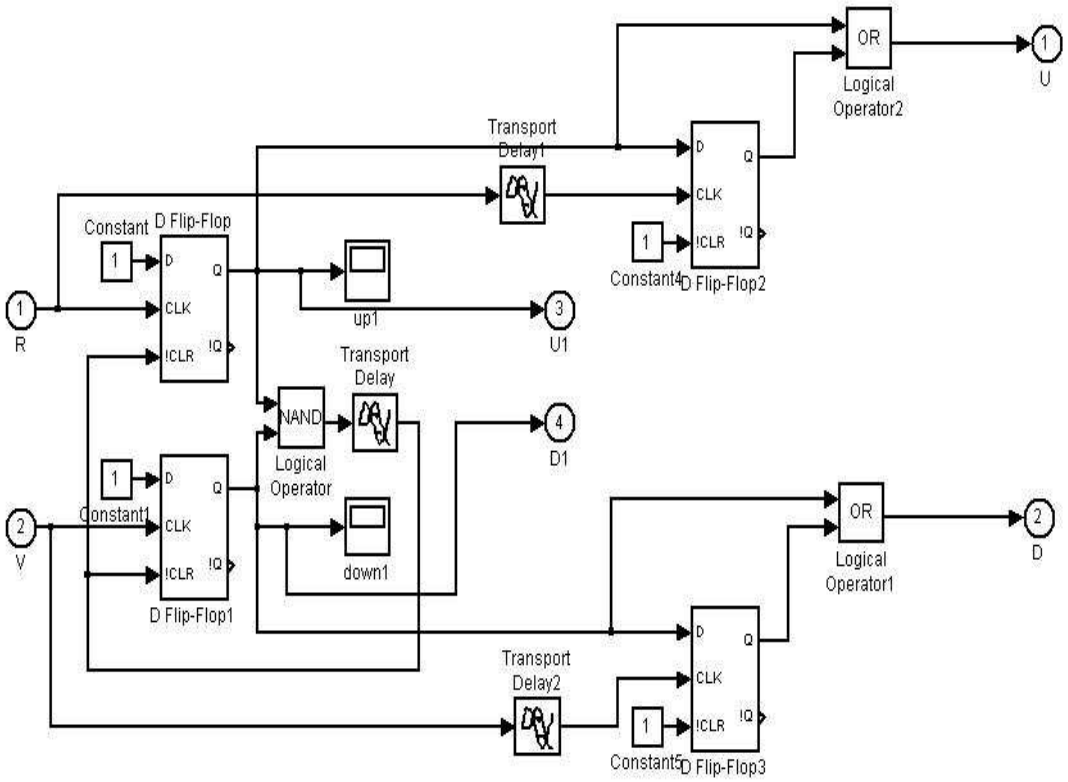


Figure 3.7: The proposed PFD behavioral model.

and the phase difference is large, the continuous-time circuit is activated. Therefore, more current will be injected into the loop filter. The locking time is reduced. When the PLL is in the near locking state, the pulse width of Up1 or Dn1 is less than Td. Only the conventional PFD exists to realize the fine tuning.

The Td can be calculated as

$$Td = \frac{C_1 \cdot \Delta f}{I_{cp} \cdot K_{VCO}}, \tag{3.7}$$

where Δf is the output frequency jumping.

Hence, the loop bandwidth of the proposed PLL is approximately

$$\omega_{BW1} \cong \frac{K \cdot I_{cp} \cdot K_{VCO} \cdot R_2}{N}, \tag{3.8}$$

Figure 3.8: Conventional PLL Vctrl voltage.

which is $2\pi K$ times larger than the bandwidth of the conventional PLL in Eq. (3.2). It shows that the bandwidth can be expanded further with a large K in Eq. (3.8).

In the proposed PLL, the natural frequency (ω_{N1}) and the damping factor (ζ_1) now become

$$\omega_{N1} \cong \sqrt{(KI_{cp}K_{VCO})/(NC_2)}, \tag{3.9}$$

$$\zeta_1 \cong \omega_{N1}R_2C_2/2, \tag{3.10}$$

which are $\sqrt{2\pi K}$ times larger than the natural frequency and damping factor of the conventional PLL in Eq. (3.3) and Eq. (3.4) .

The locking time is [14]

$$T_L \cong \frac{2\pi}{\omega_{N1}}. \tag{3.11}$$

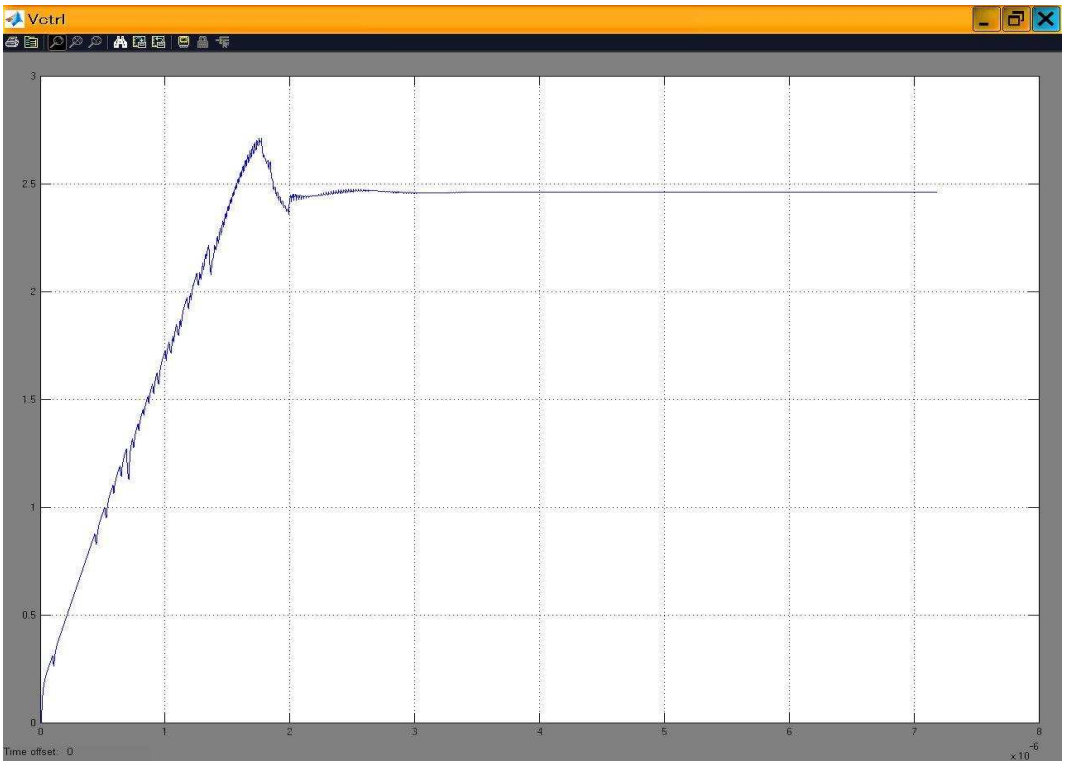


Figure 3.9: Proposed PLL Vctrl voltage.

Hence, the locking time is decreased due to a larger natural frequency and damping factor when the continuous-time circuit is activated.

3.3 Simulation Results

The principle of proposed PLL is confirmed in MATLAB Simulink. The whole proposed PLL and the proposed PFD behavioral models are shown in Fig. 3.6 and Fig. 3.7. The MATLAB simulation results of VCO control voltages of conventional PLL and proposed PLL with K=1 are depicted in Fig. 3.8 and Fig. 3.9. The locking times of the conventional PLL and proposed PLL with K=1 are 5.50 μs and 2.0 μs within 1% final frequency. Therefore, the behavioral model simulation results confirmed the effectiveness of the proposed PLL.

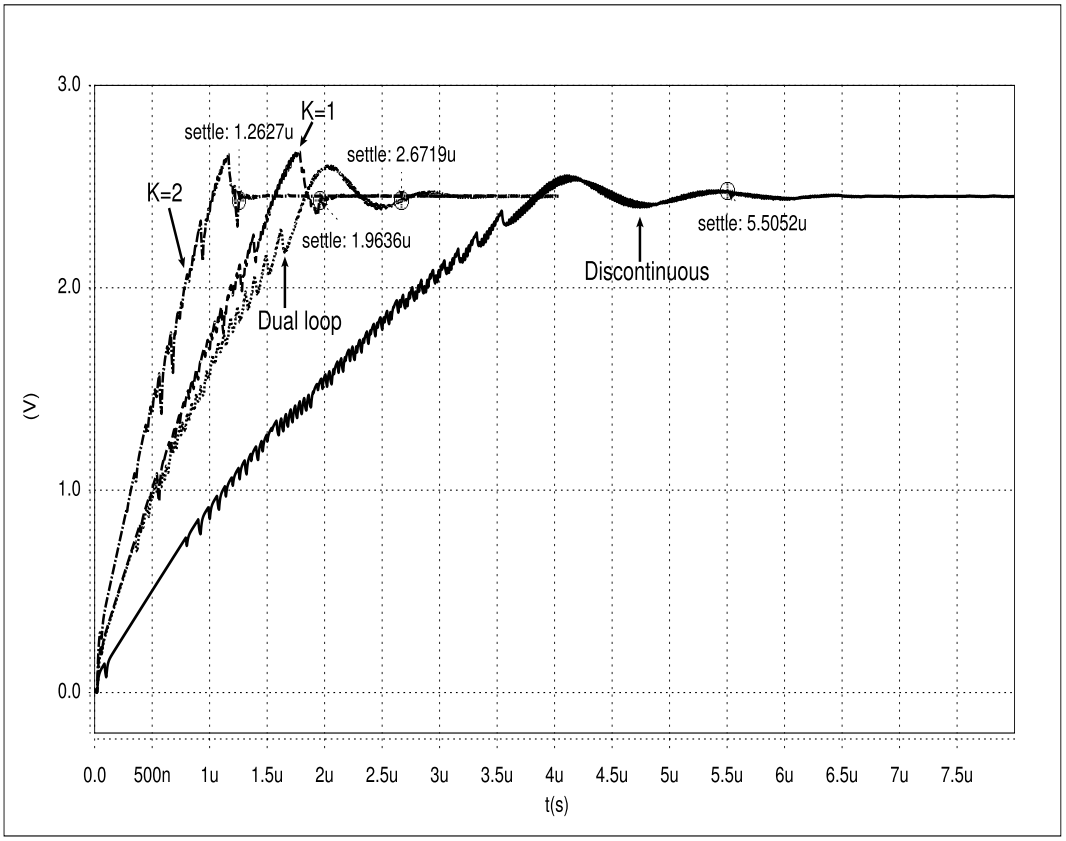
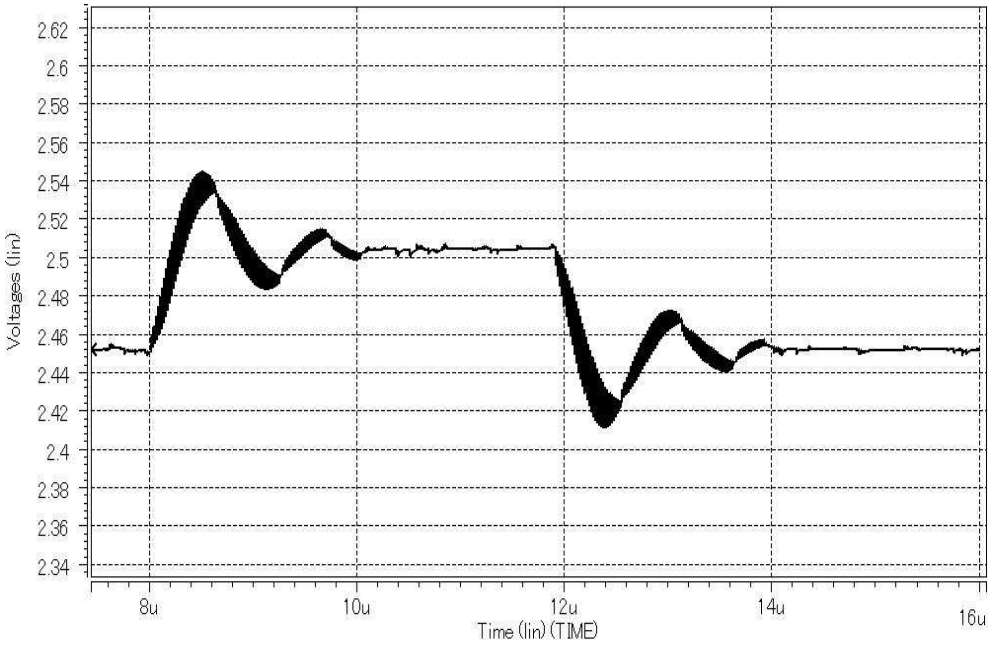


Figure 3.10: Comparsion of Vctrl voltages.

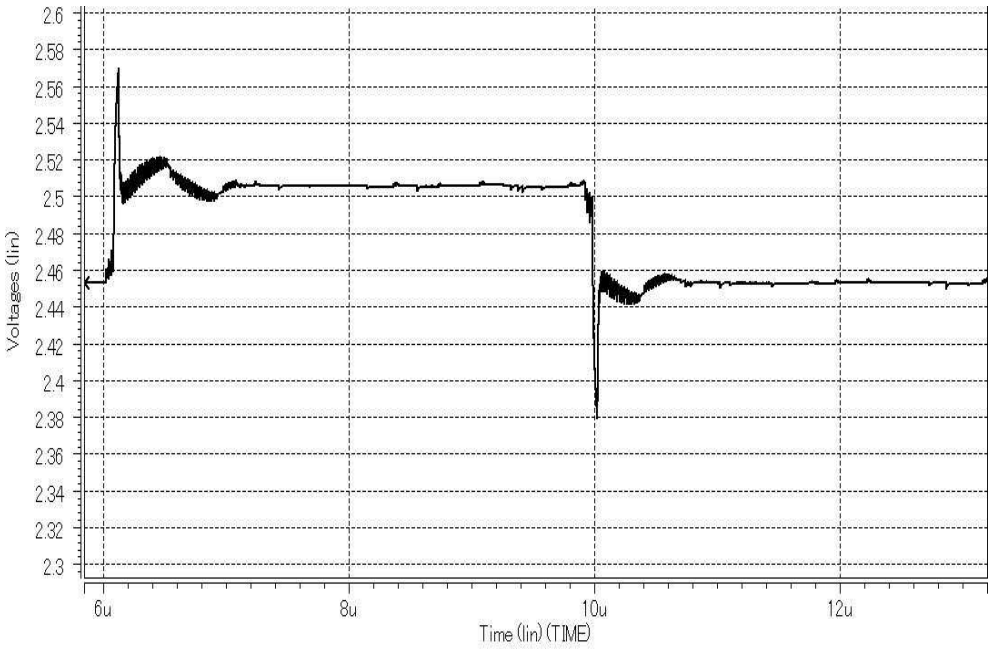
The proposed PLL has been realized in a standard 0.35 μm CMOS process with a 3.3 V supply voltage. I_{cp} and N are designed as 30 μA and 8, respectively. The output frequency of VCO is 400 MHz.

The VCO control voltages of the conventional discontinuous-time PLL, the proposed PLL with K=1 and K=2 and the dual-loop PLL [6] are shown in Fig. 3.10. The locking times of the proposed PLL with K=1 and K=2 and the dual-loop PLL [6] are 1.96 μs, 1.26 μs and 2.67 μs compared with the 5.50 μs of the conventional discontinuous-time PLL. There are 64.4 % and 77.1 % reductions of the locking times.

The frequency jump waveforms of the conventional PLL and the proposed PLL are depicted in Fig. 3.11. The locking times of the positive switching waveform and



(a) Frequency jump waveform of conventional PLL.



(b) Frequency jump waveform of proposed PLL.

Figure 3.11: Frequency jump waveforms.

Table 3.1: Comparison with reported PLLs.

Items	Proposed PLL with K=1	Proposed PLL with K=2	Con. D.T. PLL	Dual loop [6]
Technology	0.35 μm CMOS			
Supply voltage	3.3 V			
Charge pump current	30 μA			
Output frequency	400 MHz			
Divider modulus	8			
Locking time	1.96 μs	1.26 μs	5.50 μs	2.67 μs
Locking time @ 10 MHz frequency jump	0.13/0.1 μs	-	0.76/0.64 μs	-

the negative switching waveform of the conventional PLL are 0.76 μs and 0.64 μs compared with 0.13 μs and 0.10 μs of the proposed PLL for a frequency jump of 10 MHz. There are about 82.9 % and 84.4% reductions of the locking times.

3.4 Comparison with Other Reported PLLs

The summary of comparison with other reported PLLs is listed in Table 3.1. According to this table, the locking times of the proposed PLLs are substantially reduced. In addition, the proposed PLL has very simple architecture which can reduce the power dissipation and chip size.

3.5 Conclusions

A continuous-time phase frequency detector (PFD) based on the conventional tri-state PFD is proposed for fast lock charge pump phase-locked loops (CPPLLs) in this chapter. When the PLL is in the out of lock state and the phase difference is large, the continuous-time circuit is activated. More current will be injected into the

loop filter, therefore, the locking time is reduced. When the PLL is in the near locking state, only the conventional PFD exists to realize the fine tuning. Any conventional tri-state PFDs can be improved with the proposed continuous-time architecture. The simulation results demonstrate that the proposed continuous-time PFD is effective to reduce the locking time without extra power dissipation.

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Chapter 4

AN ENERGY MANAGEMENT CIRCUIT FOR SELF-POWERED UBIQUITOUS SENSOR MODULES USING VIBRATION-BASED ENERGY

In this chapter, a novel energy management circuit is proposed for self-powered ubiquitous sensor modules using a variable and weak ambient energy. Energy is requested by any kind of devices to become functional. Hence many concerns are applied to power management schemes for any system engineers. In this chapter, the background of ambient energy source and the properties of the selected ambient energy for ubiquitous sensor modules are reviewed firstly. Then, an energy management circuit is proposed for self-powered ubiquitous sensor modules using vibration-based energy. With the proposed circuit, the sensor modules work with low duty cycle operation. Moreover, a two-tank circuit as a part of the energy management circuit is utilized to solve the problem that the average power density of ambient energy always varies with time while the power consumption of the sensor modules is constant and larger than it. In addition, the long start-up time problem is also avoided with the timing control of the proposed energy management circuit. The CMOS implementation and silicon verification results of the proposed circuit are also presented. Its validity is further confirmed with a vibration-based energy generation. The sensor module is used to supervise the vibration of machines and transfer the vibration signal discontinuously. A piezoelectric element acts as the vibration-to-electricity converter to realize battery-free operation.

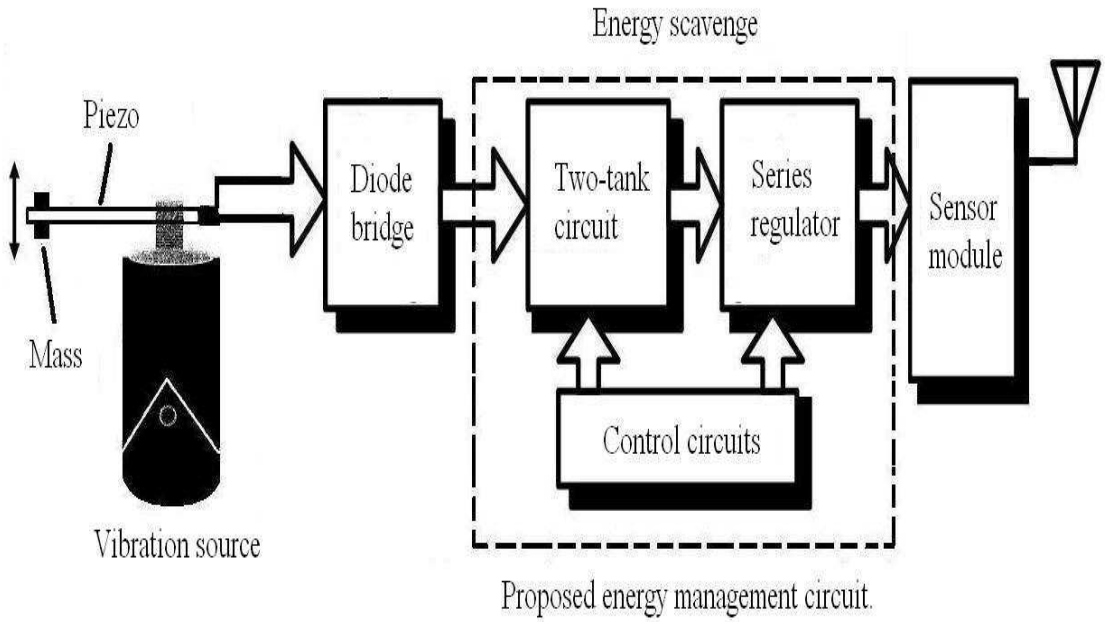


Figure 4.1: Proposed system block diagram of the sensor module.

4.1 Introduction

Wireless Sensor Network (WSN) has become a popular research topic in recent years. A WSN is composed of a large number of wireless sensor nodes that are densely scattered in a sensor field to transmit data from one to ten meters in range. Advances in low power Very Large Scale Integration (VLSI) design have opened up the possibility of powering the ubiquitous sensor modules by scavenging ambient energy, thus, eliminating the need for batteries and extending the lifetime of sensor modules infinitely [1, 2]. There are many potential ambient energy sources, such as solar power [3], vibration-based power [1, 2, 4–7], thermoelectric power [8–11], fluid flow power, and electromagnetic field power [12].

Any kind of device needs energy to become functional. In many easy-to-supply devices the problem related to energy is essentially associated with cost. However in

the WSN world the problem of energy goes beyond economics and becomes essential in terms of functionality. Due to the usual small amount of energy available the way the engineer manages energy becomes a key point in this industry [13]. In truth, several problems resulted from the circuit designs are not fully addressed in the conventional architecture.

One of these problems is that there is a lack of an effective energy management circuit in the sensor module. The power consumption of the sensor module, larger than the average power density of ambient energy, remains constant while the ambient energy varies according to its environment. For example, the solar power density is 150 μW/cm^3 in a cloudy day. It is much less than that of a power density of 1500 μW/cm^3 in a sunny day [1]. The scavenged vibration-based energy always varies with different equipments. Even the scavenged energy from the same equipment will also vary according to their working conditions. Among all the published technologies, little work has been done on how to efficiently manage the scavenged ambient energy to deal with the variations of ambient energies.

Therefore, when the input energy is overabundant, the surplus energy is wasted due to the limited capacity of the only capacitor; when it is insufficient, the sensor module will not work well. Hence, a novel energy management circuit is desired to target commonly occurring vibrations in typical office buildings, manufacturing and assembly plant environments, and homes in order to maximize the potential applicability of the sensor module [2].

The second problem is that a large super capacitor (for example, on the order of 1 Farad, size: ϕ21.5$\times$8mm [14]) used in most approaches would lead to a very long start-up time before the sensor module working [2]. Given the assumption that the average current of scavenged energy is on the order of 0.1 mA and the full charging voltage of the capacitor is 3.3 V, therefore, the start-up time will be over 9 hours. During this period, the switch S1 is always turned off and the sensor module does not work in the conventional system. If the sensor module is used in, for example, family security

application, the security information during this period will be missed. Obviously, this long start-up time problem caused by using large super capacitor makes this approach impracticable.

The focus of this paper is to try finding paths to solve these problems, what at the end means to increase the expected life-time of the sensor modules. Therefore, an energy management circuit is proposed for self-powered ubiquitous sensor modules using vibration-based energy. A 2-stage two-tank circuit as a part of the energy management circuit is utilized to solve the energy variation problem. The 2-stage two-tank circuit is mainly composed of a small capacitor and a bigger capacitor. With an appropriate timing control, the small capacitor is quickly charged to a predetermined voltage to avoid the long start-up time problem firstly, and then the bigger capacitor is slowly charged to a predetermined voltage subsequently to deal with the variation of ambient energy. Moreover, the 2-stage two-tank circuit can be expanded to an N-stage two-tank circuit. A high level of integration is realized because the proposed energy management circuit is integrated onto one chip. The proposed energy management circuit scavenges the vibration-based ambient energy (low level vibrations) and regulates it as the supply voltage of sensor module to realize a self-powered operation. In addition, the proposed energy management circuit determines the period during which the vibration signal is detected and transferred to the air by the sensor module.

This chapter is organized as follows. Section 2 discusses the proposed energy manage circuit. Silicon verification results are given in section 3, followed by conclusions in section 4.

4.2 Proposed Energy Management Circuit

In this section, the principle of the proposed two-tank circuit and the operations of the control circuits are presented. In addition, some simulation results are given.

4.2.1 System Requirements

The proposed circuit must meet such requirements:

1. To realize a self-powered operation, the proposed circuit can operate without any batteries or any separate voltage sources.

2. The scavenged energy can power on the sensor module for about 100 ms with a 3 mW power dissipation.

3. The proposed circuit can be realized with a standard CMOS process. The breakdown voltage of the CMOS process is 3.3 V and the supply voltage of the sensor module is 1.5 Vdc.

4.2.2 Proposed Two-Tank Circuit and Principle

The proposed system block diagram of the sensor module is depicted in Fig. 4.1. A proposed energy management circuit takes the places of the large capacitor C and voltage regulator in the conventional sensor module. The proposed circuit includes a two-tank circuit, control circuits and a series regulator. The two-tank circuit is used to effectively manage the scavenged ambient energy. The series regulator generates a regulated DC voltage as a supply voltage of the sensor module. The sensor module monitors the signal generated by the piezoelectric element and transfers the detected signal to the air. The control circuits determine the system timing sequence.

4.2.2.1 Vibration to Electricity Conversion

The sensor module scavenges vibration-based energy as power supply with piezoelectric elements due to it's high power density compared with other methods. A survey of different power sources demonstrated that the power density of vibrations is 250 μw/cm^3 [1, 2]. The piezoelectric element can be mounted on any equipment which have low level vibrations. In order to reduce the volume of the sensor module, the same piece of piezoelectric element provides the energy and detected signal. It is

realized by the control circuits.

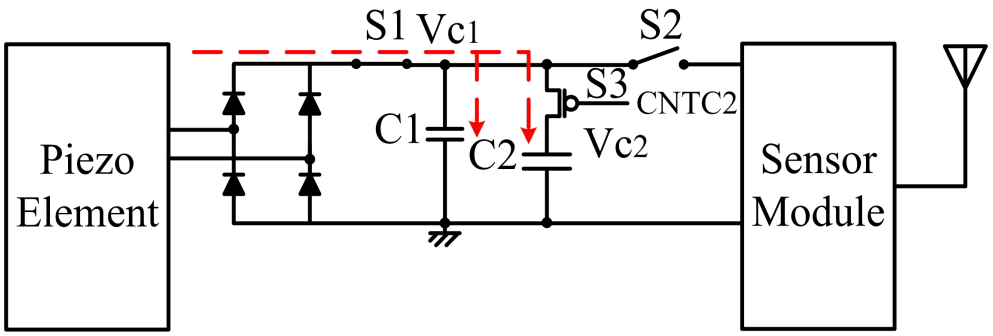
For our ubiquitous sensor module, a PZT piezoelectric element (size: 9 ×33 mm) acts as the vibration-to-electricity converter [15]. The element is driven with a low level vibration at 60 Hz with a typical acceleration magnitude of 2.25 m/s^2, which is equivalent to those measured on a small microwave oven. For one piece of this element, the average continuous output power is over one hundred microwatts and the amplitude of output voltage is a several volts sinusoidal wave based on our test results. For example, if the load is 120 KΩ, the output power is over 140 μW and the output voltage is about 6 VAC [4].

4.2.2.2 Proposed 2-Stage Two-Tank Circuit

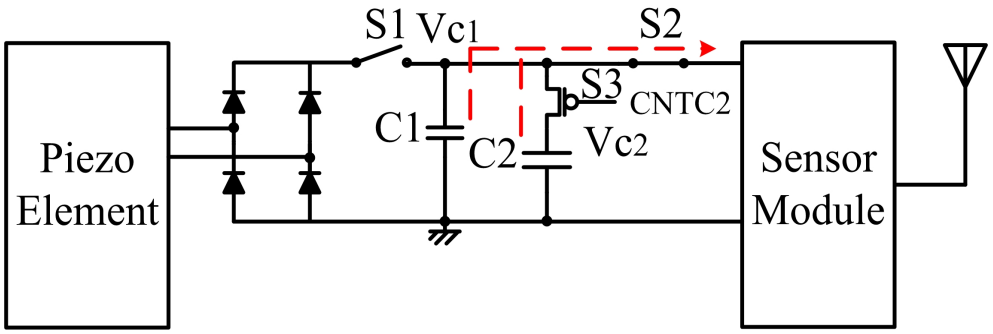
As we know, the power consumption of the sensor module is on the order of several milliwatts. However, the energy source can provide only several hundred microwatts with several pieces of such elements in parallel connection. Therefore, the sensor module has to work with a low duty cycle operation. The operation of this module includes two phases. The first phase is called scavenging energy phase in which the energy scavenged from the piezoelectric element is stored in the two-tank circuit. The second phase is called transmission phase in which the energy stored in the two-tank circuit is discharged to the sensor module.

A parallel 2-stage two-tank circuit is shown in Fig. 4.2. In this figure, Vc1 refers to the voltage across C1 and Vc2 refers to the voltage across C2. The waveforms of Vc1 and Vc2 in start-up state is shown in Fig. 4.3(a) and the waveforms of Vc1 and Vc2 in fully charged state is shown in Fig. 4.3(b). The fully charged state starts from when Vc2 reaches Vfull. In this paper, the upper limit Vfull of Vc1 and Vc2 is 3.3 V due to the breakdown voltage. Vmin is 2.0 V due to the voltage loss of series regulator.

During the scavenging energy phase, S1 is turned on; S2 and S3 are turned off initially. Hence, only C1 is quickly charged to Vfull (3.3 V) within several seconds.



(a) Scavenging energy phase.

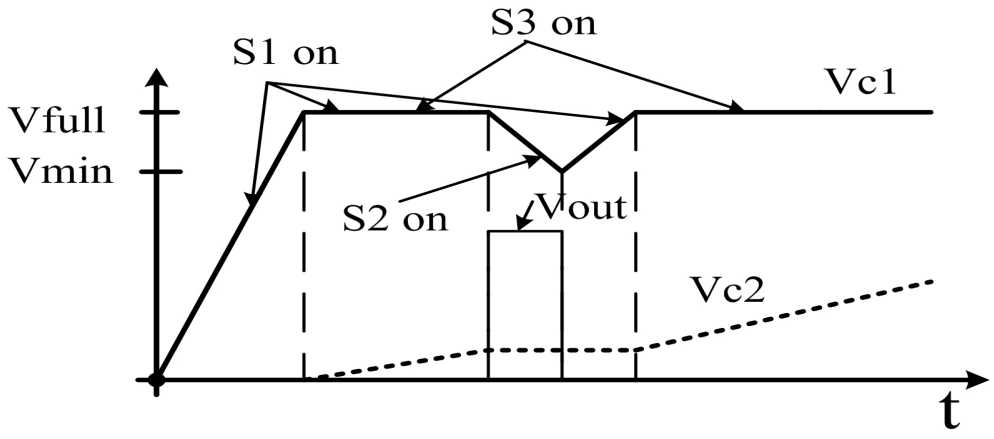


(b) Transmission phase.

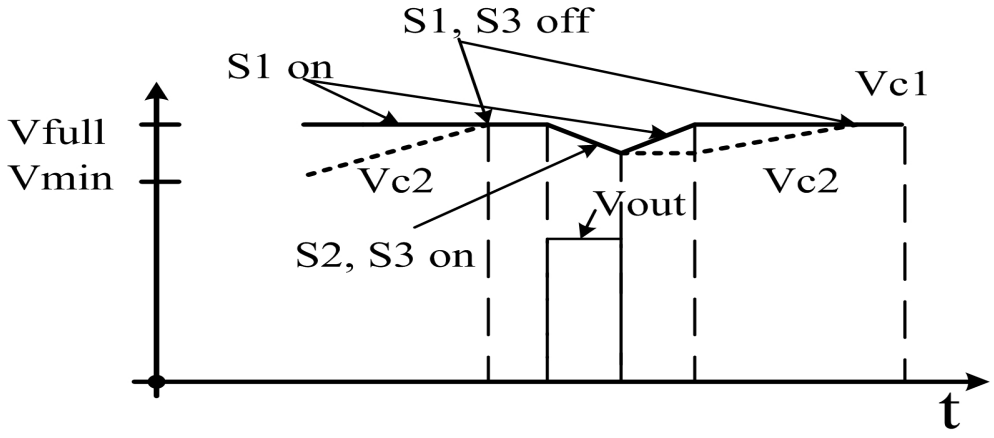
Figure 4.2: 2-stage two-tank circuit.

After that, S3 is slightly turned on to act as a variable resistor in series connection with C2. Then C2 begins to be charged slowly while the voltage Vc1 remains constant. The piezoelectric element now only serves as an energy source. After a trigger signal changes its state from high to low within a predetermined short period to avoid the very long start-up time problem, S1 and S3 are turned off; S2 is turned on and Vout appears immediately. As shown in Fig. 4.3(a) and (b), Vout appears to power on the sensor module without considering the voltage Vc2. So, the operation enters into the transmission phase.

During the transmission phase, the series regulator output Vout appears to power on the sensor module. Only the energy stored in C1 is discharged to the sensor module at first and at the same time the voltages Vc1 and Vc2 are monitored. The



(a) Start-up state.



(b) Fully charged state.

Figure 4.3: Waveforms of 2-stage two-tank circuit.

vibration signal is detected and transferred to the air during this phase. If the voltage Vc2 is larger than the voltage Vc1, S3 is turned on and the energy stored in C2 also discharges to the load together with C1. The piezoelectric element only serves as a signal source. After a predetermined period passed or when the voltage Vc1 falls down to Vmin (2.0 V), S1 is turned on and at the same time S2 and S3 are turned off. Then the operation enters into the scavenging energy phase. Another cycle is repeated in the same way.

In the fully charged state, the charge time of C1 is calculated that

$$T_{c1} = \frac{C1 * \Delta V1}{I_{avg}}, \tag{4.1}$$

where $\Delta V1 = Vfull - Vmin$ is the voltage variation of C1 and I_{avg} is the average input current. For example, C1= 470 μF, $\Delta V1$=3.3-2.0=1.3 V, I_{avg}=0.1 mA, the T_{c1} is about 6 s. The voltage variation of C2 is given by

$$\Delta V2 = \frac{I_{avg} * T_{c2}}{C2}, \tag{4.2}$$

where T_{c2} is the predetermined charge or discharge time of C2.

4.2.2.3 Proposed N-Stage Two-Tank Circuit

Based on the 2-stage two-tank circuit, two types of N-stage two-tank circuits are proposed. The parallel N-stage two-tank circuit, so named because all the capacitors are connected in parallel, is proposed in Fig. 4.4. The series N-stage two-tank circuit, so named because all the capacitors are connected in series, is shown in Fig. 4.5. VR1, VR2, ..., and VRN refer to the voltage controlled resistances, respectively. Vc1, Vc21, Vc22, ..., and Vc2N refer to the voltages across C1, C21, C22, ..., and C2N, respectively. The value of C1 is the smallest one among all the capacitors.

For the parallel N-stage two-tank circuit, the operations are similar to the operations of the 2-stage two-tank circuit.

During the scavenging energy phase, S1 is turned on and S2 is turned off initially. The capacitor C1 is quickly charged to Vfull to avoid the long start-up time problem, meanwhile, the resistances VR1, VR2, ..., and VRN are turned off to prevent C21, C22, ..., and C2N from being charged. Only after the voltage Vc1 reaches Vfull, the value of VR1 is slightly decreased by the control circuit. The voltage Vc1 is held constant at Vfull and the surplus energy is stored into the large capacitor C21. In the same way, after Vc2(I-1) (I=2, 3, ..., N) reaches Vfull, the value of VRI is slightly decreased by the control circuit. The voltage Vc1, Vc21, ..., and Vc2(I-1) are held at

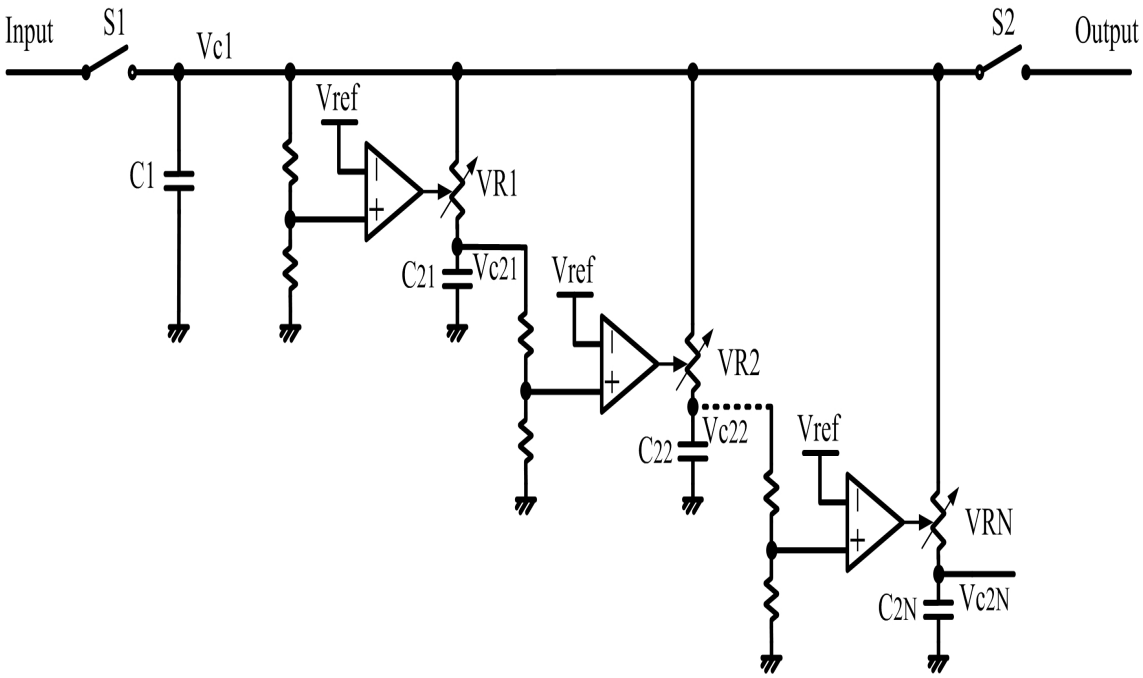


Figure 4.4: Parallel N-stage two-tank circuit.

Vfull and the surplus energy is stored into the larger capacitor C2I. After a trigger signal changes its state from high to low, the operation enters into the transmission phase.

During the transmission phase, S1 is turned off and S2 is turned on initially. The resistances VR1, VR2, ..., and VRN are turned off. The scavenged energy in C1 is discharged to the load. When the control circuit detects that the voltage Vc1 is equal to Vc21, VR1 is set to zero and the energies stored in C1 and C21 are discharged to the load together. In the same way, when the control circuit detects that the voltage Vc2(I-1) is equal to Vc2I, VRI is set to zero and the energies stored in Vc2I and C1, C2, ..., and C2(I-1) are discharged to the load together. After a predetermined discharge period passed or when the voltage Vc1 falls down to Vmin (2.0 V), S1 is turned on and S2 is turned off. Then the operation enters into the scavenging energy phase. Another cycle is repeated again and again. If the input energy is large enough,

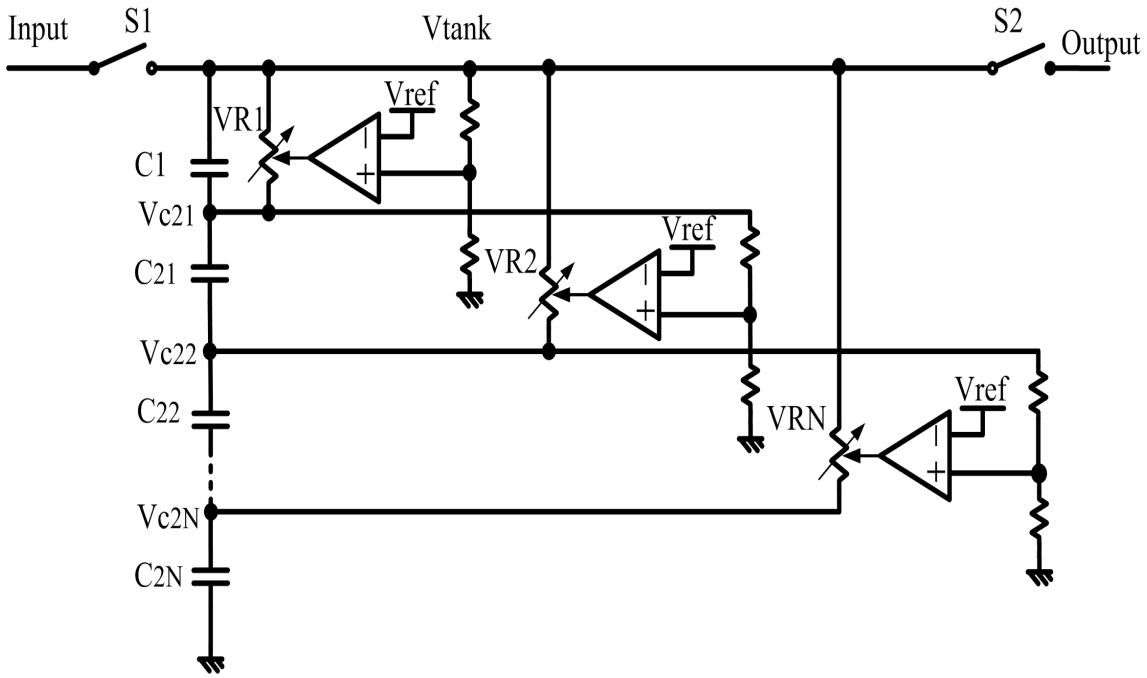


Figure 4.5: Series N-stage two-tank circuit.

the capacitors C21, C22, ..., and C2N will be fully charged to Vfull one by one. How many stages are used depends on the load condition and the input average power density.

The equivalent capacitor during scavenging energy phase is given by

$$C_{equ} = \begin{cases} C1, & \text{for Vc1} < \text{Vfull} \quad (4.3) \\ C1 + \sum_{I=1}^{N} C2I. & \text{for Vc1} = \text{Vfull} \quad (4.4) \end{cases}$$

In the fully charged state, the equivalent capacitor during transmission phase is given by

$$C_{equ} = C1 + \sum_{I=1}^{N} C2I. \quad (4.5)$$

For the series N-stage two-tank circuit, the operations are as follows. During the scavenging energy phase, S1 is turned on and S2 is turned off. The C1 in series connection with C21, C22, ..., and C2N is quickly charged at start-up period due to

the smallest C1 while the resistances VR1, VR2, ..., and VRN are turned off to prevent C21, C22, ..., and C2N from being charged. After the tank voltage Vtank reaches Vfull, the value of VR1 is slightly decreased. The tank voltage is held constant at Vfull and the surplus energy is stored into the larger capacitor C21 in series connection with C22, C23, ..., and C2N. In the same way, after the voltage Vc2(I-1) also reaches Vfull, the value of VRI is slightly decreased. The tank voltage is held at constant and the surplus energy is stored into the larger capacitor C2I in series connection with C2(I+1), C2(I+2), ..., and C2N. After a trigger signal changes its state from high level to low level, the operation enters into the transmission phase.

During the transmission phase, S1 is turned off and S2 is turned on. The resistances VR1, VR2, ..., and VRN are turned off. The scavenged energies in C1 in series connection with C21, C22, ..., and C2N are discharged to the load. When the control circuit detects that the voltage Vtank is equal to Vc21, the VR1 is set to zero and the energies stored in C21 in series connection with C22, C23, ..., and C2N are discharged to the load together. In the same way, when the control circuit detects the voltage Vtank is equal to Vc2I, VRI is set to zero and the energies stored in C2I, C2(I+1), ..., and C2N are discharged to the load together. After the predetermined discharge period passed, S1 is turned on and S2 is turned off. Then the operation enters into the scavenging energy phase. Another cycle is repeated again and again, until the voltages Vc21, Vc22, ..., and Vc2N reach fully charged voltage Vfull one by one.

In summary, the merits of the N-stage two-tank circuit are: (1) A smallest C1 is used to avoid long start-up time problem. Only after Vc1 reaches Vfull and C2 is charged at a predetermined period, Vout appears, rather than C21, C22, ..., C2N are also charged to Vfull. (2) The capacitors C21, C22, ..., C2N are used as batteries to store the surplus energy when input energy is abundant enough and the stored surplus energy can be discharged to the sensor module when input energy is insufficient. (3) It is possible to power on different loads by using an appropriate N-stage architecture.

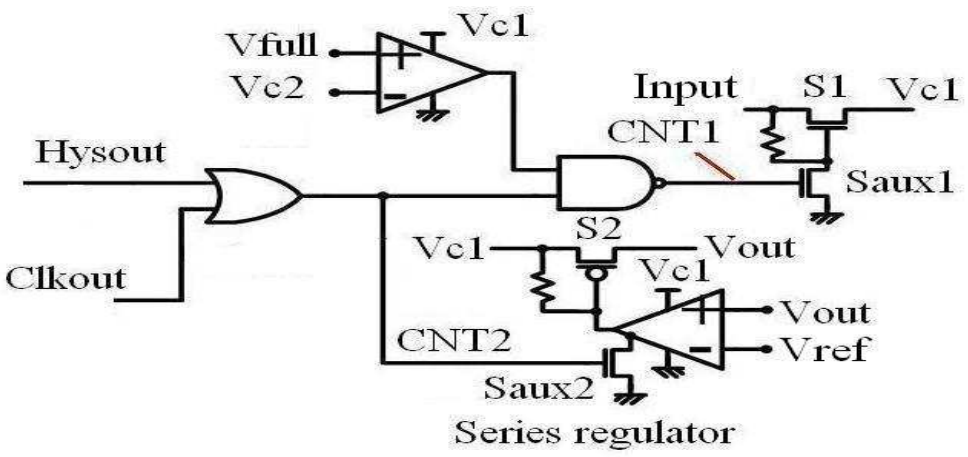


Figure 4.6: Control circuit for S1 and S2.

4.2.3 Control Circuits

In this paper, a parallel 2-stage two-tank is used to verify the principle of the proposed two-tank circuit. Therefore, a control circuit composed of two sections is proposed to determine the timing sequence of the proposed energy management circuit.

Figure 4.6 shows the control circuit for S1 and S2. The signal Hysout is the output of a hysteresis comparator and is used to monitor the voltage Vc1 [16]. The signal Clkout, which could be a clock signal or an output of a micro MCU, is a trigger signal. In this paper, a clock generator is used to generate Clkout signal. Hysout, Clkout, a NOR gate, an NMOS transistor and a series regulator determine the operations to C2. The series regulator composed of an amplifier and S2 with a resistor generates a stabilized DC voltage as a supply voltage of sensor module. The drain terminal of Saux2 is connected to the internal node of the amplifier. CNT2 is used to act as an enable signal to turn on or turn off the amplifier of series regulator. When CNT2 is high, S2 will be turned off. When CNT2 is low, S2 acts as the pass device of the series regulator.

The operations are as follows. When Vc1 reaches Vfull, Hysout signal changes

its state from high to low. This allows Clkout signal to change its state from low to high, and the on state of Clkout signal determines the charge period of C2. During this period, when Vc2 also reaches Vfull, S1 will be turned off to prevent C2 from being over-charged. When Clkout signal changes its state from high to low, S1 is turned off and S2 is turned on. The sensor module enters into transmission phase. The energies stored in C1 and C2 are discharged to the sensor module. While Vc1 is down to Vmin, Hysout signal changes its state from low to high, S1 is turned on and S2 is turned off. Meanwhile, Clkout signal still low, S3 is turned off and the input energy is charged to C1 only. After Vc1 reaches Vfull again, S3 is turned on and C2 will be charged again.

In Fig. 4.6, the upper part circuit determines the operation of S1 and the lower part circuit determines the operation of S2.

Figure 4.7 shows the control circuit for S3 to determine the operation to C2. During scavenging energy phase, when Vc1 is equal to Vfull and Vc2 is less than Vfull, S3 is turned on to charge C2. During this phase, the output of the lower Op-Amp is always zero. Therefore, the upper Op-Amp, the NOR gate and S3 form a negative feedback system. It is used to stabilize Vc1 to Vfull and to charge C2 by the input scavenged energy. During transmission phase, when Vc2 is larger than Vc1, S3 is turned on again to discharge C2 to the sensor module together with C1. In Fig. 4.7, the upper Op-Amp compares the voltage Vc1 with Vfull to determine the moment when the C2 begins to be charged. The lower Op-Amp compares the Vc1 with Vc2 to determine the moment that C2 begins to be discharged.

As shown in Fig. 4.6 and Fig. 4.7[1], the supply voltage of the control circuit is also the varying voltage Vc1 rather than a stabilized DC voltage. Because the whole circuit is a self-powered circuit, therefore, an extra voltage regulator will consume

[1]In the actual circuits, Vfull, Vc1 and Vc2 are reduced by the same factor and then introduced to the input terminals of the Op-Amp. Vfull denotes a reference voltage.

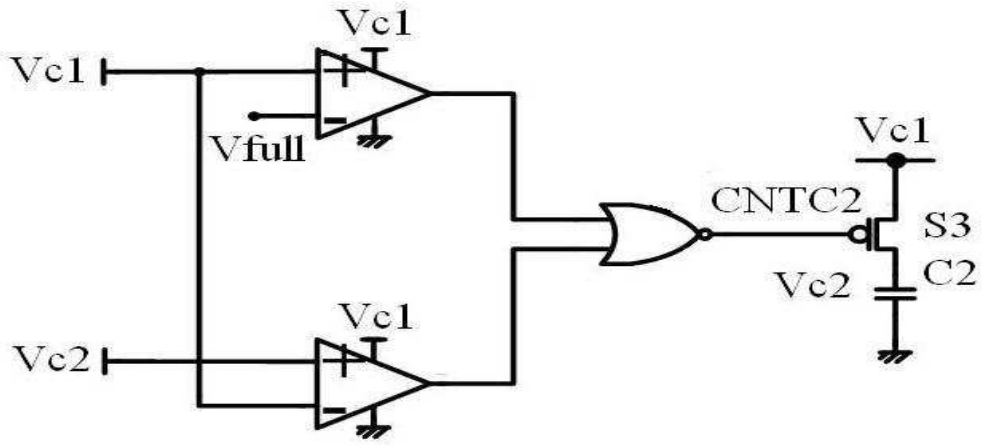


Figure 4.7: Control circuit for S3.

some energies. The self-powering is realized with the NMOS transistors Saux1 and S1 with a resistor in Fig. 4.6. CNT1 is zero and Saux1 is off initially. S1 is turned on because it is tied like a diode. Hence, C1 is charged by the scavenged energy from zero to Vfull. As Vc1 increasing, the control circuits begin to work and then take over the whole circuit operations.

During the start-up state, only the energy stored in C1 is utilized as the supply voltage both of control circuits and sensor module through a series regulator. Therefore, the value of C1 is determined by

$$C1 = \frac{I_{load} * T_{load} * V_{full}}{\Delta V1 * V_{out}}. \tag{4.6}$$

where I_{load} is the average supply current of sensor module and T_{load} is the operating time of sensor module. Given the assumption that I_{load}=2 mA, T_{load}=100 ms, V_{full}=3.3 V, $\triangle V1$= 3.3-2.0= 1.3 V and V_{out}=1.5 V, therefore, the minimum C1 is 340 μF. In practice, a 470 μF C1 is mandated.

In summary, the control circuits are used to determine the timing sequence of switches S1, S2 and S3. The timing sequence determines that the scavenged energy can charge C1 and C2 one by one. The timing sequence determines the operating time of sensor module at a predetermined period 100 ms also.

4.2.4 Simulation Results

In order to verify the principle of the proposed architecture, an Hspice simulation was carried out with a standard 0.35 μm CMOS process. C1 is 470 μF from Eq. (4.6). To simplify the simulation, the small values of C2 = 4700 μF is used. The simulation results of timing waveforms during start-up state are shown in Fig. 4.8. The horizontal axis is the time and the unit is second. The vertical axis is voltage and the unit is volt. The curves are Vc1, Hysout, Clkout, CNTC2, Vc2, CNT1, CNT2 and Vout, respectively. CNT1, CNT2 and CNTC2 are used to control the operation of S1, S2 and S3, respectively. It is shown that the C1 is quickly charged to Vfull with several seconds (about 4.7 s) then C2 is slowly charged. When a predetermined charging period of C2 passed and Clkout signal changed its state from high to low, Vout appears to power on the sensor module during the start-up state, then the sensor module begins to work. However, in the conventional architecture, the sensor module have to wait until a big capacitor is charged to Vfull for a very long period. So, the long start-up time problem can be solved by the proposed two-tank circuit. During the start-up state, the energy consumption of the sensor module is only provided by C1.

The simulation results of timing waveforms during fully charged state are shown in Fig. 4.9. After a long period, C2 is also charged to Vfull. It is shown that when Clkout signal is high, the CNTC2 signal controls S3 slightly on to charge C2. When Vc2 reaches Vfull also, the CNT1 signal turns off S1. However, due to a slight power dissipation of the control circuit, Vc1 slightly decreases and S1 is needed to be slightly turned on to charge C1 and C2. Thus, there are some variations in CNT1 signal during scavenging energy phase. CNT2 signal turns on S2 only after Vc1 reaches Vfull and the Clkout signal falls from high to low. During the fully charged state, the energy to power on the sensor module is provided by C1 and C2.

The input power energy is on the order of several hundred microwatts (For our

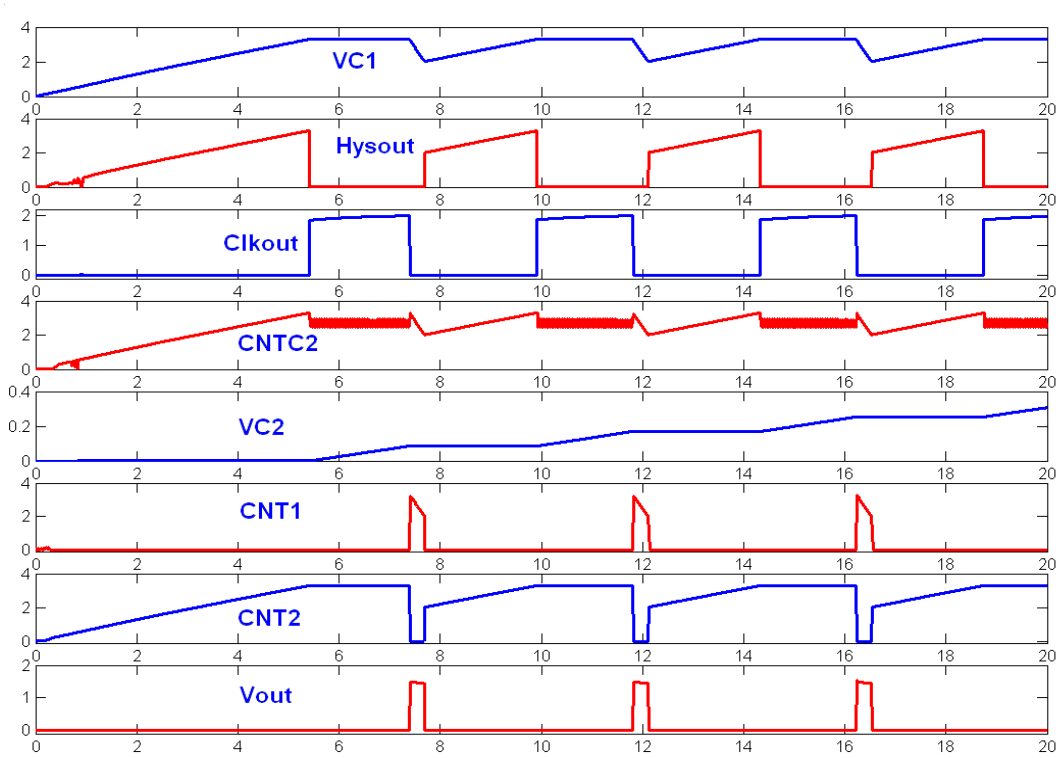


Figure 4.8: Simulation results during start-up state.

application, when the duty cycle is 0.1 , at least three PZT pieces are required in parallel operation). The two-tank circuit with its control circuit consumes about 50 μW in total in this example. The sensor module dissipates about 3 mW from a 1.5 V DC supply. The scavenging energy phase is about 550 ms and the transmission phase is about 100 ms in fully charged state.

4.3 Silicon Verification

To validate the proposed circuit, the 2-stage parallel two-tank circuit has been fabricated in a standard 0.35 μm CMOS process. The die photograph is presented in Fig. 4.10. The proposed energy management circuit occupies a chip area of $80\times360\mu m^2$ without PADs.

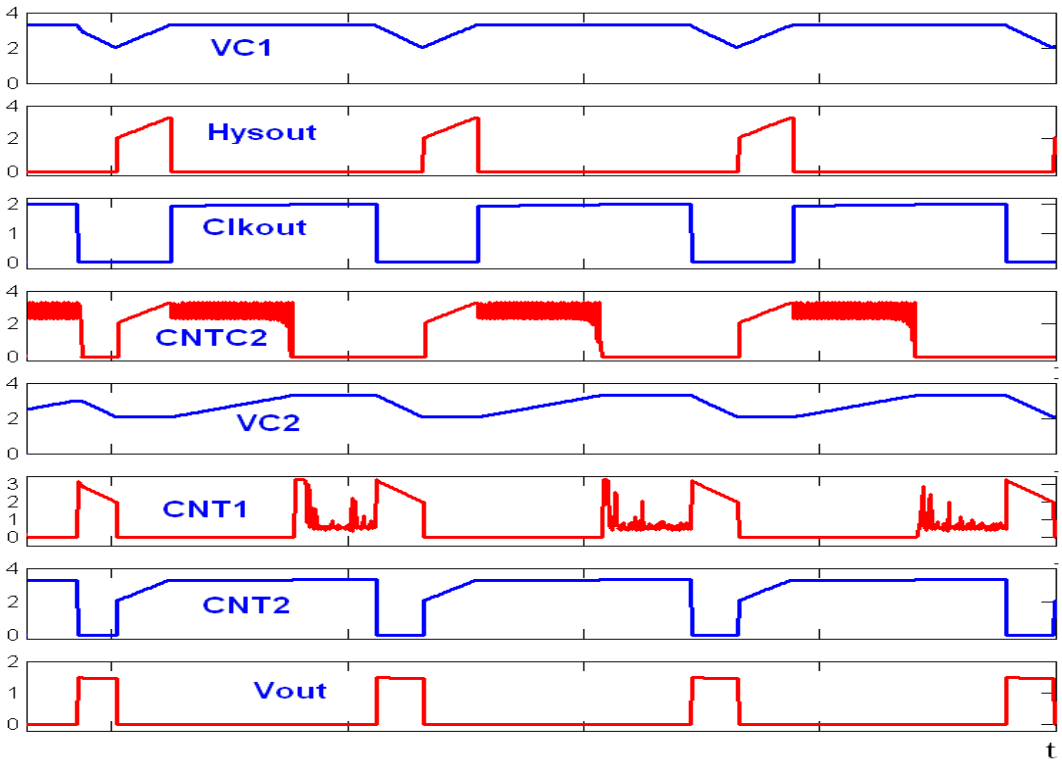


Figure 4.9: Simulation results during fully charged state.

The test conditions are: C1 = 470 μF, and C2 = 4700 μF. In practice, even a larger super capacitor on the order of 1 Farad (size: ϕ21.5×8mm [14]) could be used, however the small C2 capacitor is convenient for the test because it is easier to see the charge/discharge cycles on the C1 and C2. The power consumption of loads is about 2.3 mW. The start-up time is 4.7 s, which is much shorter compared with the several hours start-up time of conventional architecture.

The waveforms of Vc1 and Vc2 are shown in Fig. 4.11. It is shown that when Vc1 reaches 3.3 V, C2 begins to be charged. After a predetermined period, the energy stored in C1 is discharged to the load during the transmission phase. While the Vc1 decreases to Vc2, the energies stored in C1 and C2 are discharged to the load together.

The waveforms of Vc1 and Vout are shown in Fig. 4.12. It is shown that during the

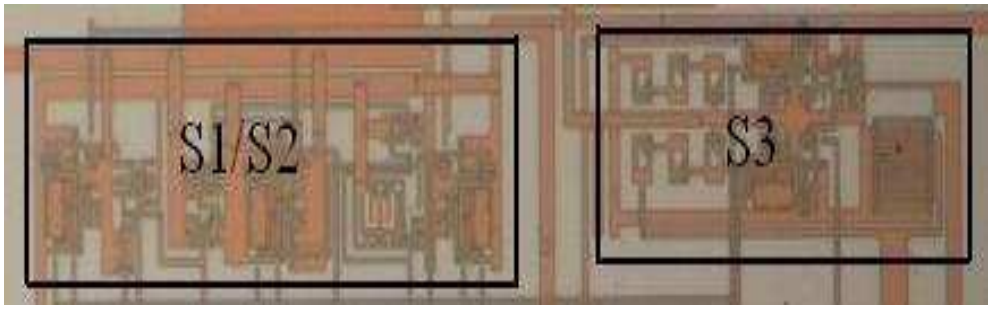


Figure 4.10: Chip die photograph.

transmission phase, Vout appears and the energies stored in C1 and C2 are discharged to the load.

The waveforms of Vc1 and clock signal are shown in Fig. 4.13. It is shown that the low level state of clock signal Clkout is used to determine the transmission period.

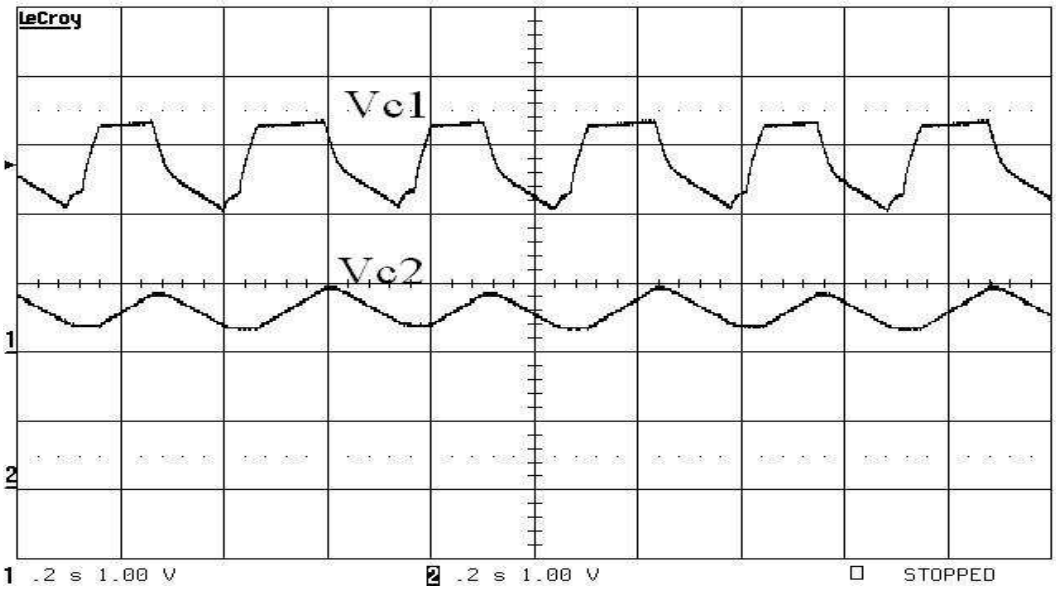
The waveforms of CNT1 and CNT2 are shown in Fig. 4.14. When the CNT1 signal is low, S1 is turned on. When CNT2 is high, S2 is turned off[1].

In summary, the two-tank circuit operates like a battery whose capability is adjustable. In practice, the problem that how many stages are used depends on the load condition and the input average power density. Besides, the input energy of the two-tank could be the vibration-based energy or any other ambient energies.

4.4 Conclusions

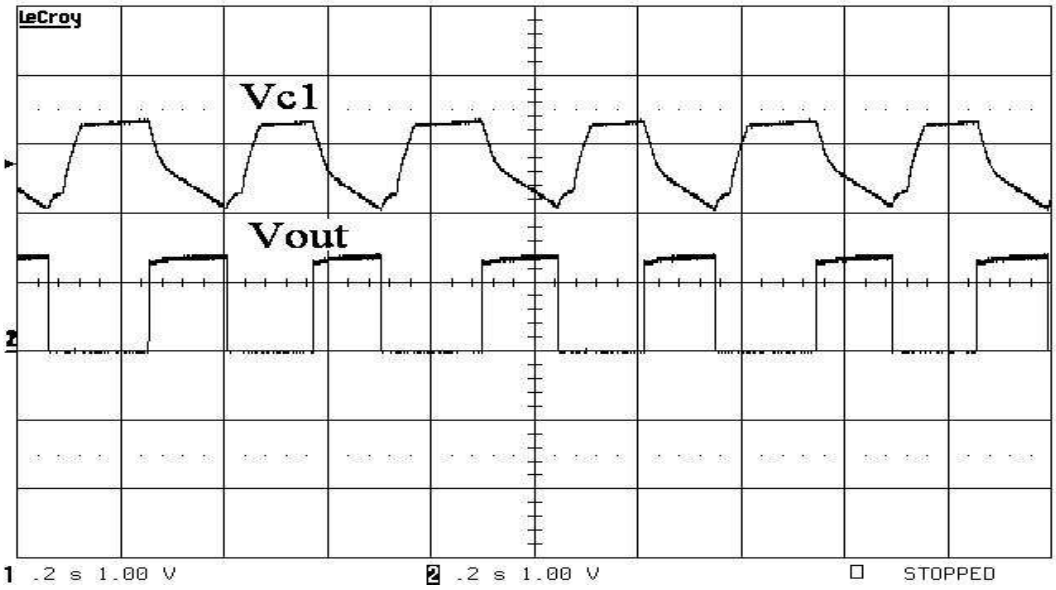
An energy management circuit for efficiently managing the scavenged ambient energy has been proposed for ubiquitous sensor modules using vibration-based energy generation. The implementation of the proposed circuit with a standard CMOS process is presented and further validated by experimental results.

[1]Vc2 is not charged to Vfull in the experimental result. Therefore, CNT1 signal has no variations as shown in Fig. 4.9



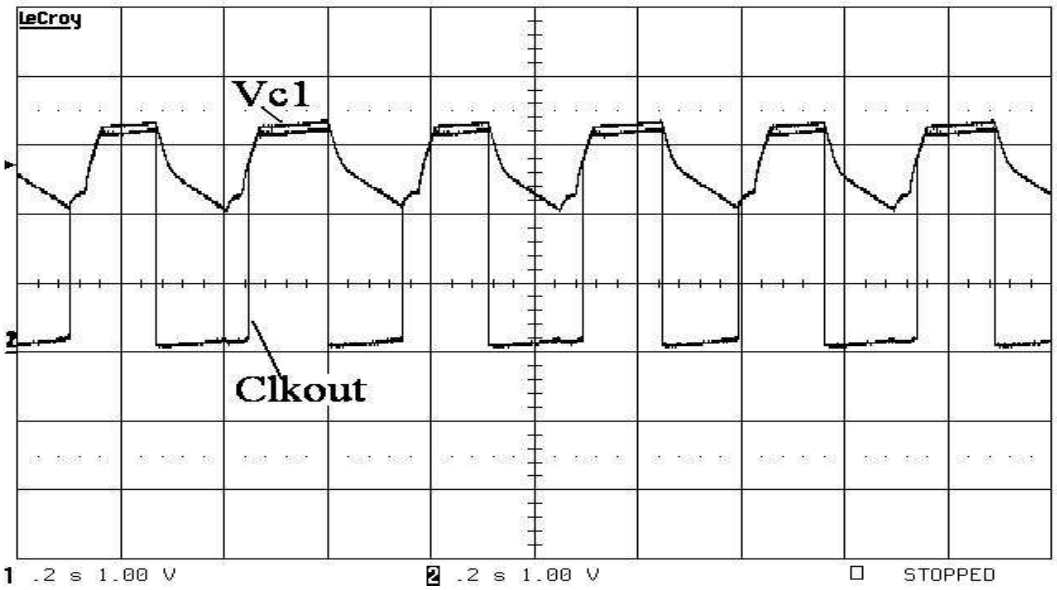
Range H: 0.2 s/div, V: 1.0 V/div

Figure 4.11: Measured Vc1 and Vc2 signals.



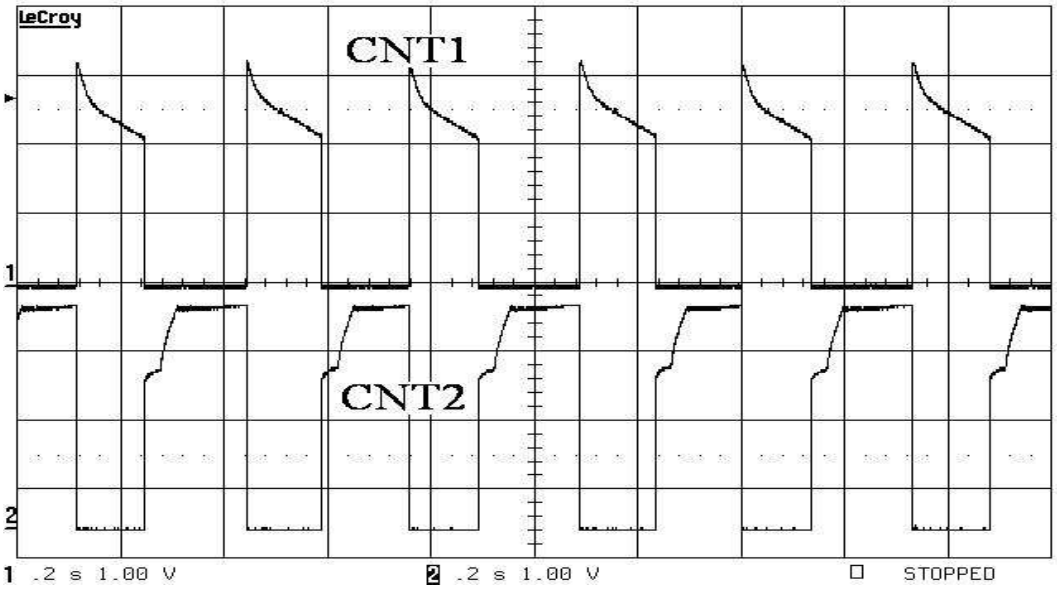
Range H: 0.2 s/div, V: 1.0 V/div

Figure 4.12: Measured Vc1 and Vout signals.



Range H: 0.2 s/div, V: 1.0 V/div

Figure 4.13: Measured Vc1 and Clkout signals.



Range H: 0.2 s/div, V: 1.0 V/div

Figure 4.14: Measured CNT1 and CNT2 signals.

The energy management circuit can avoid the long start-up time problem and can improve the level of integration. Based on our experimental results, the proposed energy management circuit can be used as a battery for any ubiquitous sensor modules using different ambient energies. The proposed energy management circuit is effective in managing the scavenged ambient energy and maximizing the potential applicability of the sensor module.

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Chapter 5

A CHARGE PUMP CIRCUIT WITHOUT OVERSTRESS IN LOW-VOLTAGE SINGLE-WELL CMOS PROCESS

In this chapter, a high efficiency charge pump power management circuit is proposed. Charge pump circuits are frequently used in semiconductor integrated circuits to provide a voltage that is higher than the voltage of a power supply. In case that the scavenged voltage of energy source is small, then the high efficiency charge pump circuit is one of good solutions to convert it to a higher voltage for ubiquitous device. In addition, the proposed circuit is particularly useful in flash and EEPROM non-volatile memories because that programming or erasing the Flash memory cells needs very high positive and negative voltages. Besides, the charge pump circuit has become an important circuit technique in low-supply-voltage system in order to increase dynamic range and simplify circuit design.

The proposed circuit not only completely switch on or switch off the charge-transfer transistors but also can reduce the equivalent on-resistance of these transistors compared with conventional circuits. In addition, the body effect is eliminated due to the proposed two pumping branches architecture. Therefore, its voltage pumping efficiency is much higher than that of the conventional designs. Moreover, the maximum gate-source, gate-drain and drain-source voltages of all transistors in the proposed charge pump circuit do not exceed the power supply voltage Vdd. The proposed charge pump circuit has been realized in a standard CMOS N-Well 0.35 μm technology. The measured results demonstrate that the proposed charge pump circuit has very high voltage pumping efficiency without overstress. Hence, the proposed circuit is suitable for implementation in low-voltage single-well CMOS process.

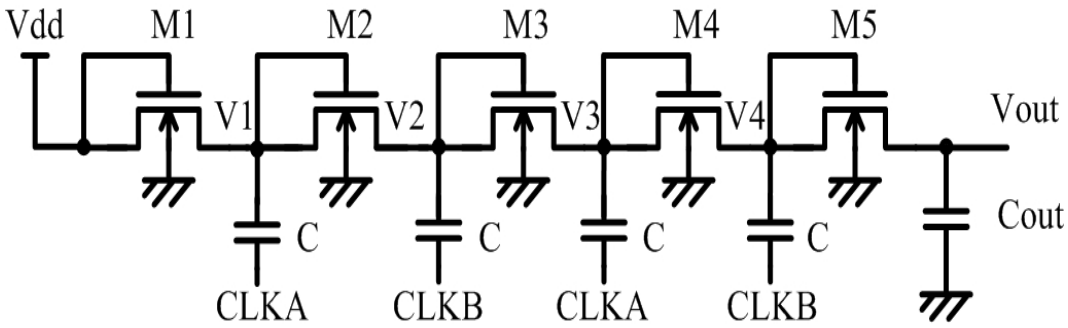


Figure 5.1: Dickson charge pump circuit.

5.1 Introduction

Charge pump circuits play a key role in semiconductor integrated circuits where a voltage that is higher than the voltage of a power supply.

The most popular architectures are based on Dickson [1] topology as shown in Fig. 5.1. However, the traditional Dickson structure has poor pumping efficiency because that the threshold voltage becomes larger due to the body effect as the voltage of each pumping node is pumped higher. In addition, all MOSFETs suffer from high-voltage overstress on their gate oxides because that the maximum voltage difference of each stage is $2Vdd$.

Many improvements based on Dickson structure have been proposed. The schemes proposed in [2–4] still suffer from high-voltage overstress. In addition, they also suffer from body effect issue and their voltage pumping efficiencies are degraded due to a diode-connected MOSFET in the last stage as shown in Fig. 5.2 [2]. A charge pump circuit composed of PMOS and NMOS devices on a triple well technology is presented in [5–7]. Triple well process requires additional masking and process steps compared to the standard CMOS process [8]. The propose charge pump circuit in [8] has to satisfy a condition to achieve a correct functionality. However, the condition depends on parasitic capacitance which always varies with different process and layout designs.

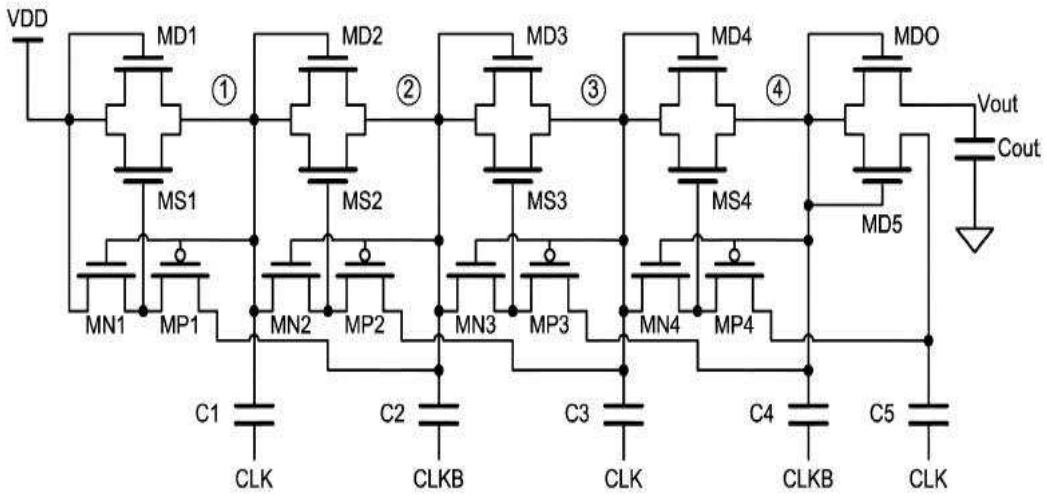


Figure 5.2: Proposed charge pump circuit in [2].

In addition, the minimum supply voltage is limited by this condition which makes it impracticable for low-voltage applications. The use of low-voltage MOSFETs can overcome the poor voltage pumping efficiency problem due to the higher threshold voltage of high-voltage MOSFETs [3]. In addition, the gate-oxide reliability issue must also be considered in the design of charge pump circuit, especially in the low-voltage single-well CMOS process with the technology advanced [5]. In this paper, a high pumping efficiency all PMOS charge pump circuit without high-voltage overstress is proposed in a low-voltage CMOS process. With the proposed architecture, the charge pump circuit achieves high voltage pumping efficiency without high-voltage overstress.

This chapter is organized as follows. Section 2 introduces the proposed architecture. Experimental results are given in section 3, followed by conclusions in section 4.

5.2 Proposed Architecture

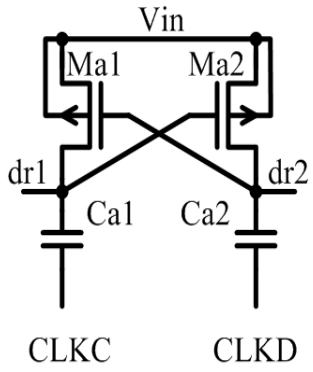
In this section, a novel driver circuit with a proposed level shifter is introduced to fully switch on charge-transfer transistors and to prevent the charges back to the previous stage. To avoid body effect, a symmetrical architecture is introduced in the proposed circuit.

5.2.1 Proposed Level Shifter

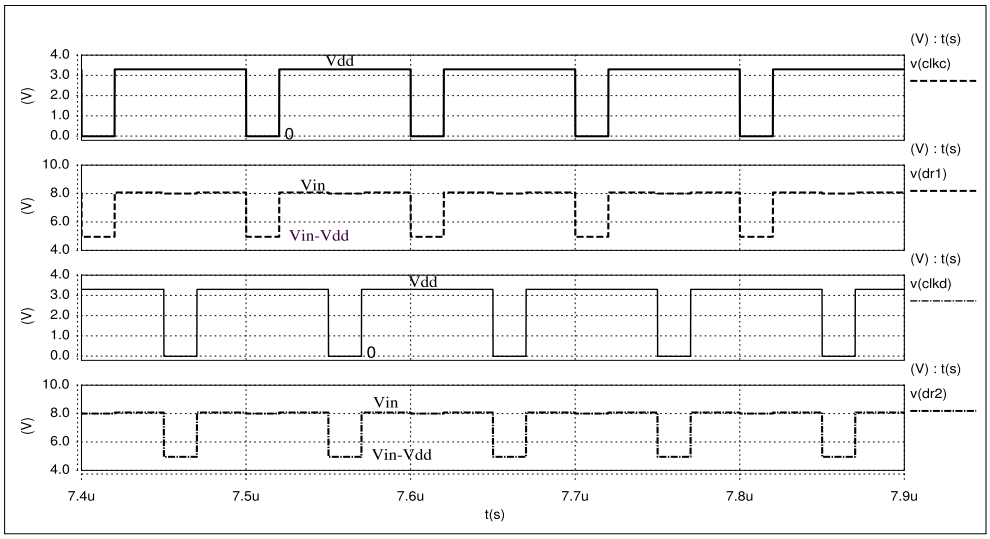
A proposed level shifter with its transient responses are presented in Fig. 5.3. The level shifter is a part of the proposed driver circuit for charge-transfer transistors. It is composed of two PMOS transistors Ma1-Ma2 and two small capacitors Ca1-Ca2. Ca1 and Ca2 are driven with two out-of-phase clock signals CLKC and CLKD, respectively. The outputs are derived from dr1 and dr2 nodes. If the input is Vin and the amplitude of clock signals is Vdd, as illustrated in Fig. 5.3(b), the output voltage of dr1 is between Vin and Vin-Vdd and the output voltage of dr2 is between Vin-Vdd and Vin. Note that the maximum gate-source, gate-drain and drain-source voltages of all transistors in the proposed lever shifter are Vdd.

5.2.2 One Stage of the Proposed Charge Pump Circuit

One stage of the proposed charge pump circuit is shown in Fig. 5.4. Note that several stages can be cascaded. To avoid body effect, only PMOS transistors are used and the bulks of the PMOS transistors are connected in the way as shown in Fig. 5.4. In is the input terminator and out is the output terminator. This is a symmetrical structure including four charge-transfer transistors Mp1-Mp4, a driver circuit including level shifter and two driving transistors Ma3-Ma4, two small driving capacitors Cd1-Cd2 and two pumping capacitors C1-C2. The driver circuit is used to fully switch on Mp1 and Mp2 and to prevent the charges back to the previous stage. A six-phase clock including CLKA, CLKB, CLKC, CLKD, CLKE and CLKF has been designed using



(a) Proposed level shifter.



(b) Transient responses of proposed level shifter.

Figure 5.3: Proposed level shifter with its transient responses.

a single clock as reference. The clock signals are shown in Fig. 5.5. As shown in this figure, each signal varies from 0 to Vdd. Clock signals CLKA and CLKB are two non-overlapped signals with a preset dead time. CLKE and CLKF are also out-of-phase. CLKC and CLKD are the signals which change their values from Vdd to 0 only during the dead time period between CLKA and CLKB.

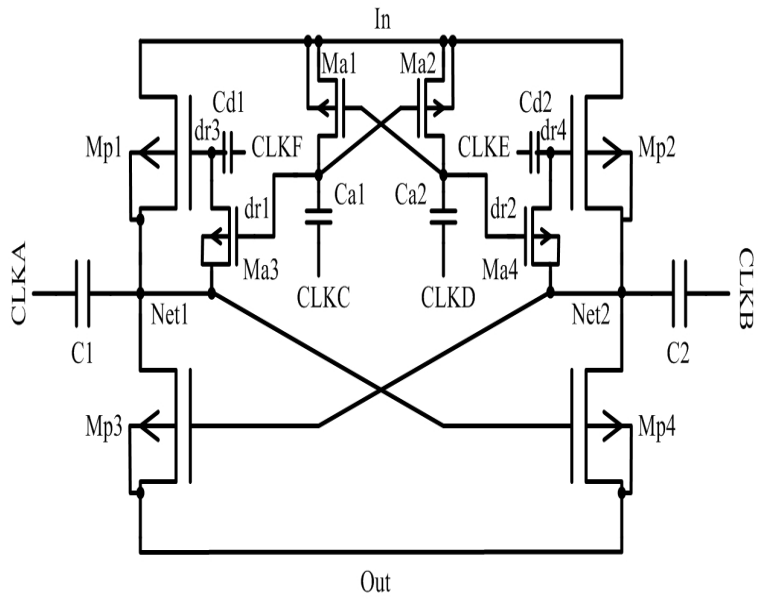


Figure 5.4: One stage of the proposed charge pump circuit.

5.2.3 Operation

The operation of proposed charge pump circuit can be divided into four time intervals. The states of six clock signals with voltage values of each nodes in the proposed one stage charge pump circuit are tabulated in Table 5.1. The states of each transistor during each interval are shown in this table also. According to the table, the maximum voltage of each transistors is Vdd. Therefore, the overstress is avoided. Actually, T1, T3 and T2, T4 intervals are opposite of each other. The detailed operations are as follows.

During the interval T1, as shown in Table 5.1, the source-gate voltage of Mp3 is Vdd. Therefore, it is fully switched on, the energy stored in C1 is discharged to the next stage while Mp4 is off. During this interval, Mp2 is on only when CLKE changed its state to 0. Then, the energy stored in the previous stage is charge to C2 while Mp1 is off. At the same time, Ma3 is also on, the voltage of dr3 is the same as the voltage of Net1. Therefore, PMOS Mp1 is fully switched off to prevent charge stored

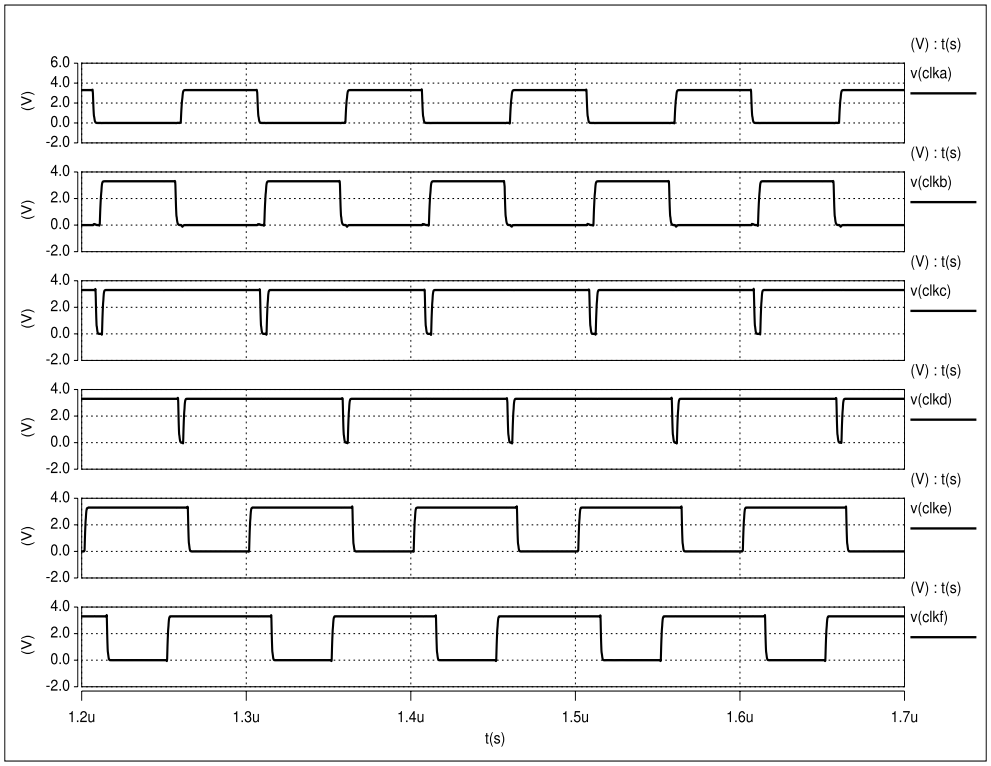


Figure 5.5: Clock signals.

in C1 back to the previous stage. On the contrary, during the interval T3, Mp2 and Mp3 will be switched on.

During the interval T2, CLKC is 0. Therefore, Ma2 and Ma3 are switched on. Then, nodes Net1 and dr3 have the same voltage Vin. Hence, during the next interval, when CLKF changed its state to 0, Mp1 can be switched on. On the contrary, during the interval T4, Ma1 and Ma4 will be switched on.

5.3 Experimental Results

5.3.1 Simulation Results

A four-stage charge pump circuit is presented in Fig. 5.6 as an example to verify the proposed principle. For the proposed charge pump circuit, there is no limitation on

Table 5.1: Time intervals.

Items	Intervals			
	T1 Interval	T2 Interval	T3 Interval	T4 Interval
CLKA	Vdd	0	0	0
CLKB	0	0	Vdd	0
CLKC	Vdd	0	Vdd	Vdd
CLKD	Vdd	Vdd	Vdd	0
CLKE	Vdd→ 0→Vdd	Vdd	Vdd	Vdd
CLKF	Vdd	Vdd	Vdd→ 0→Vdd	Vdd
Net1	Vin+Vdd	Vin	Vin	Vin
dr1	Vin	Vin-Vdd	Vin	Vin
dr3	Vin+Vdd	Vin	Vin→Vin-Vdd →Vin	Vin
Net2	Vin	Vin	Vin+Vdd	Vin
dr2	Vin	Vin	Vin	Vin-Vdd
dr4	Vin→Vin-Vdd →Vin	Vin	Vin+Vdd	Vin
ON Trs.	Mp2, Mp3, Ma3	Ma2, Ma3	Mp1, Mp4, Ma4	Ma1, Ma4
OFF Trs.	Mp1, Mp4, Ma1, Ma2, Ma4	Mp1, Mp2, Mp3, Mp4, Ma1, Ma4	Mp2, Mp3, Ma1, Ma2, Ma3	Mp1, Mp2, Mp3, Mp4, Ma2, Ma3

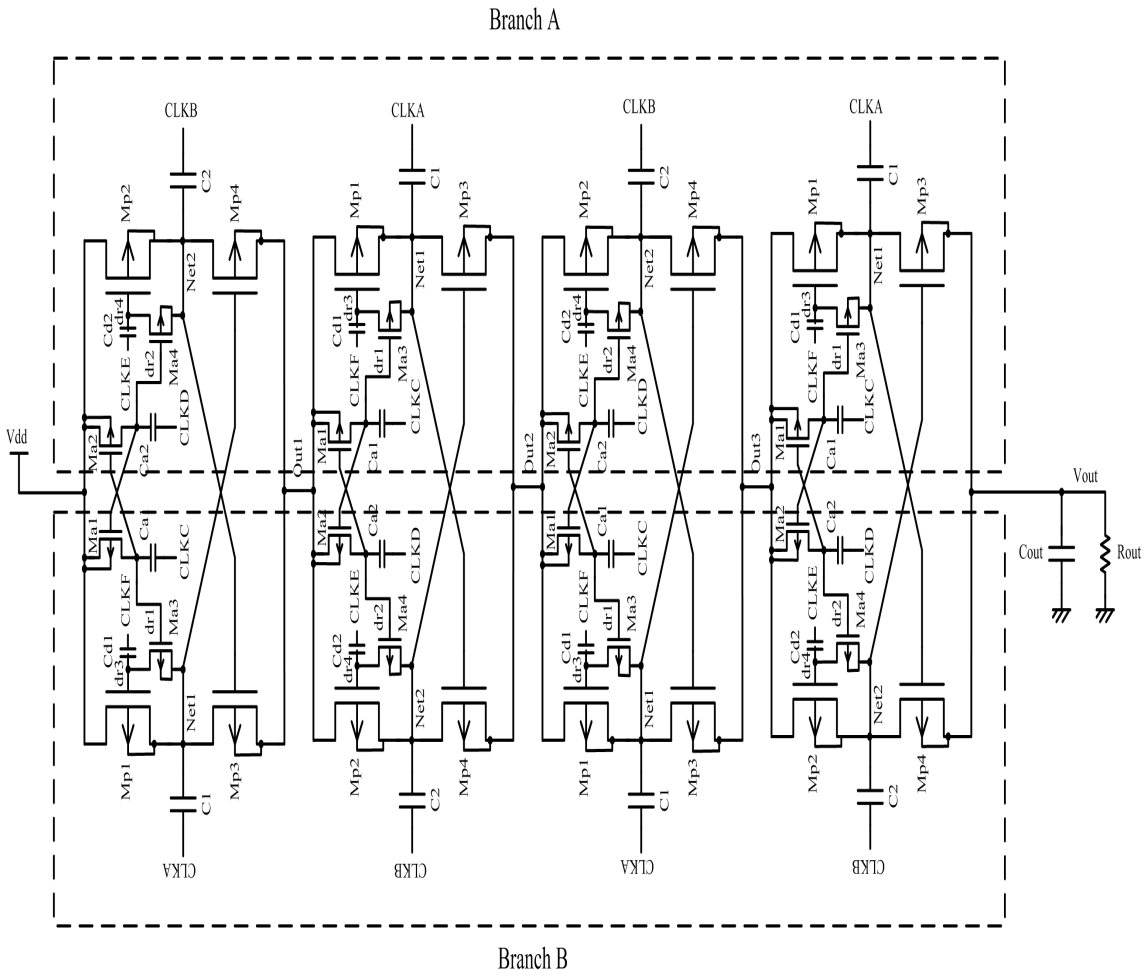


Figure 5.6: Proposed charge pump circuit by cascading stages.

the number of the cascaded stages. While, for the Dickson architecture, the number of cascaded stages is limited due to the body effect. As shown in Fig. 5.6, there are two charge transfer branches, branch A and branch B. The clock signals of these two branches are intertwined. In addition, clock signals of branches A and B are out-of-phase. Therefore, branch A and branch B can pump the output voltage to high, alternately. The N-stage output voltage of the proposed charge pump circuit with

current load is given by [9]

$$V_{out} = (1 + N)Vdd - R_{out}I_{out}, \tag{5.1}$$

where N is the number of the stages, R_{out} is the charge pump output resistance and I_{out} is the current delivered to the output. R_{out} is given by

$$R_{out} = \frac{N}{fC_{ST}} coth\left(\frac{T_{on}}{\gamma_{on}C_p}\right), \tag{5.2}$$

where f and C_{ST} are the operating frequency and the total capacitance in each charge pump stage, respectively. T_{on} is the on time of charge transfer switch, γ_{on} is the on-resistance of charge transfer switch and C_p is the pumping capacitor of each stage. γ_{on} can be expressed as

$$\gamma_{on} = \frac{1}{\mu C_{ox}(W/L)V_{ov}}, \tag{5.3}$$

where symbols W, L, μ and C_{ox} have their usual meanings, and V_{ov} is the overdrive voltage of charge-transfer transistor.

The V_{ov} of the proposed charge pump circuit is

$$V_{ov} = Vdd - |Vthp| - \frac{I_{out}}{fC_{ST}}, \tag{5.4}$$

where $Vthp$ is the threshold voltage of PMOS.

The V_{ov} of the Racape's circuit [8] is

$$V_{ov} = Vdd - 2|Vthp| - \frac{I_{out}}{fC_{ST}}. \tag{5.5}$$

As shown in Eqs. (5.4) and (5.5), the V_{ov} of Racape's circuit is smaller than that of the proposed circuit. Therefore, the equivalent on-resistance of the proposed circuit is smaller than that of Racape's circuit and the V_{out} of the proposed circuit is larger than that of Racape's circuit.

The proposed charge pump circuit in Fig. 5.6 and the Racape's circuit [8] are designed in a standard 0.35 μm CMOS N-well process for comparison. The operating frequency is preset to 1 MHz. The total pumping capacitor of each stage is 20 pF.

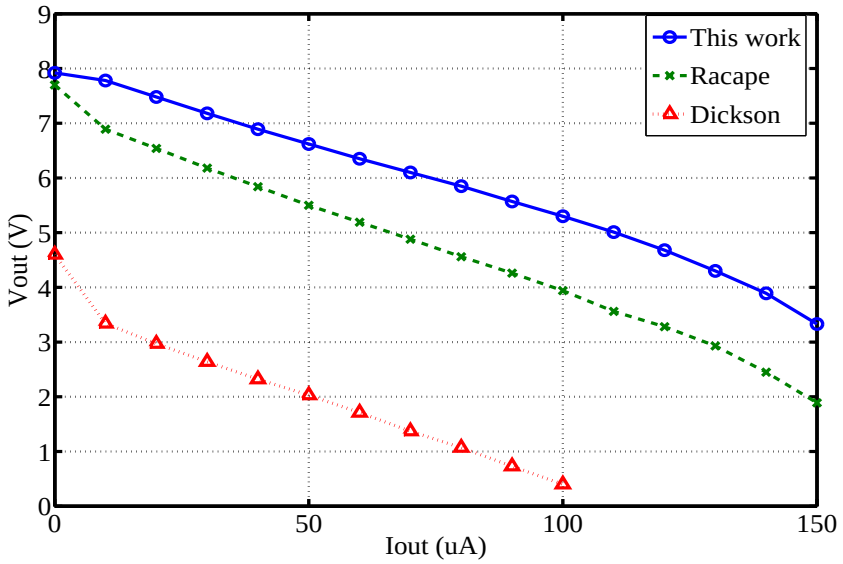


Figure 5.7: Simulated Vout of the proposed circuit, Racape's circuit [8] and Dickson circuit with Vdd=1.65 V and different load in an ideal case.

The simulated output voltages of the proposed charge pump circuit, Racape's circuit [8] and Dickson charge pump circuit with different output currents are shown in Fig. 5.7. Vdd is 1.65 V. All the simulations are in an ideal case that parasitic capacitors are not included. For fair comparison, the pumping capacitors and charge-transfer transistors in Dickson circuit are designed two times larger than the devices in the proposed circuit and Racape's circuit. As shown in Fig. 5.7, the output voltages of the proposed charge pump circuit with different output currents are much higher that those of Racape's circuit and Dickson charge pump circuit. Especially, with a higher output current of 150 μA, the proposed charge pump circuit still has the best pumping performance because that the MOSFETs in the proposed charge pump circuit are fully switched on or switched off. Since the proposed charge pump circuit has two pumping branches, the degradation of the output voltage is smaller while the output current increases. The output voltages of the proposed circuit are larger than

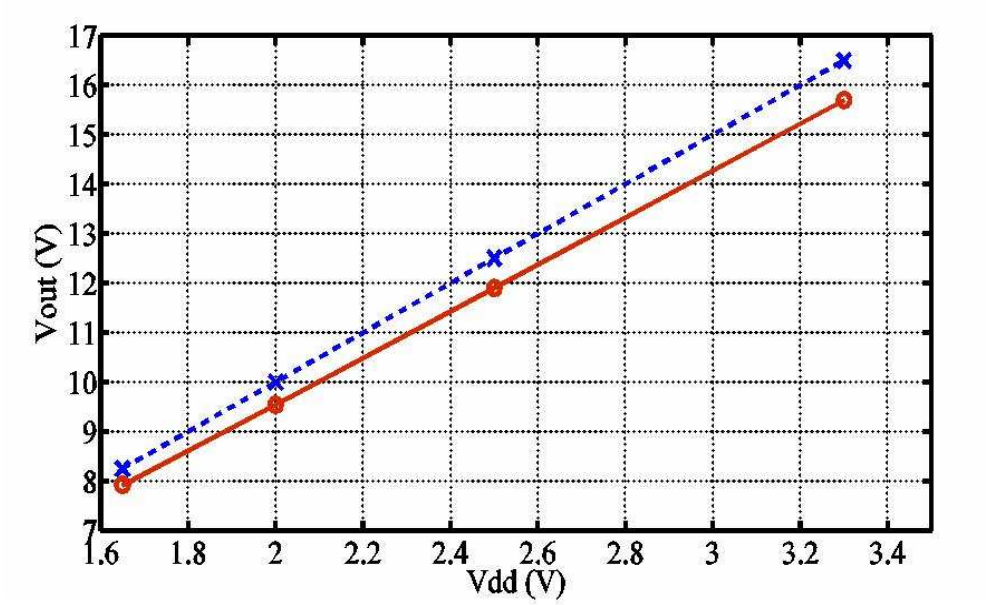


Figure 5.8: Simulated Vout of the proposed circuit with different Vdd.

those of the Racape's circuit especially when the load current increases due to the smaller on-resistance.

The simulated output voltage of the proposed charge pump circuit with different Vdd are compared in Fig. 5.8. The ideal results are shown in the upper curve and the simulation results are shown in the lower curve. All the simulations are in the ideal case. As shown in Fig. 5.8, the voltage pumping efficiency can reach as high as 95% with different Vdd.

5.3.2 Comparison with Reported Charge Pump Circuits

The summary of comparison with Dickson's charge pump circuit and Racape's circuit is tabulated in Table 5.2. According to the table, the maximum Vdd of the proposed charge pump circuit is twice of that in Dickson's circuit. The pumping efficiency of the proposed circuit in ideal case is 96% compared with 55.8% of Dickson's circuit and 93% of Racape's circuit. The pumping efficiency of the proposed circuit in ideal

Table 5.2: Comparison with reported charge pump circuits.

	This work	Dickson [1]	Racape [8]
Technology	0.35 μm CMOS		
V_{th}	V_{thp}= -0.65 V V_{thn}= +0.50 V		
Max. Vdd	3.3 V	1.65 V	3.3 V
Min. Vdd	$\lvert V_{thp}\rvert(1+\frac{C_{par}\dagger}{C_{d1}})$	-	$2\lvert V_{thp}\rvert(1+\frac{C_{par}}{C_{d1}})$
Eff. @ 0 μA	96%	55.8%	93%
Eff. @ 50 μA	80.6%	24.6%	66.7%

†Note: Total parasitic capacitance at nodes dr3 or dr4.

case with 50 μA load is 80.6% compared with 24.6% of Dickson's circuit and 66.7% of Racape's circuit. The minimum Vdd of the proposed circuit is the half of that in Racape's circuit. The proposed circuit has very high voltage pumping because that the charge-transfer transistors can be fully switched on and switched off. The difference of efficiency increased when the same load is added due to the two branches architecture of the proposed charge pump circuit.

5.3.3 Silicon Verification

To validate the proposed circuit, the 4-stage circuit has been fabricated in a standard 0.35 μm CMOS process. The die photograph is presented in Fig. 5.9. The proposed energy management circuit occupies a chip area of $500\times1200\mu m^2$ without PADs.

The measured output voltages of the proposed charge pump circuit without load and with different Vdd are shown in Fig. 5.10. From this figure, the calculated voltage pumping efficiency reachs as high as 84% with 2 V Vdd. The output voltages are limited by the breakdown voltages of the parasitic pn-junctions when the input voltage is larger than 2.5 V [5].

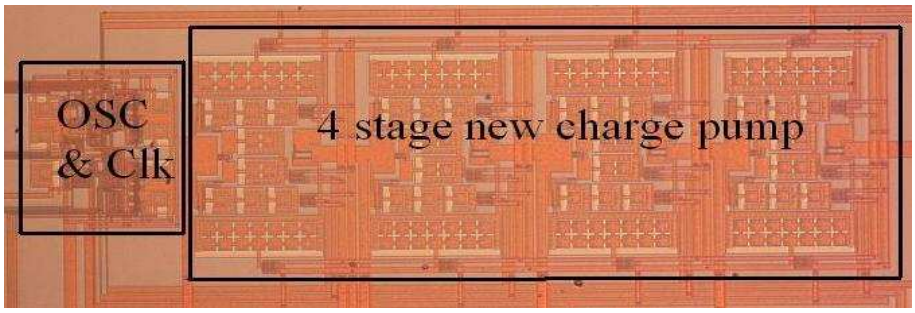


Figure 5.9: Chip die photograph.

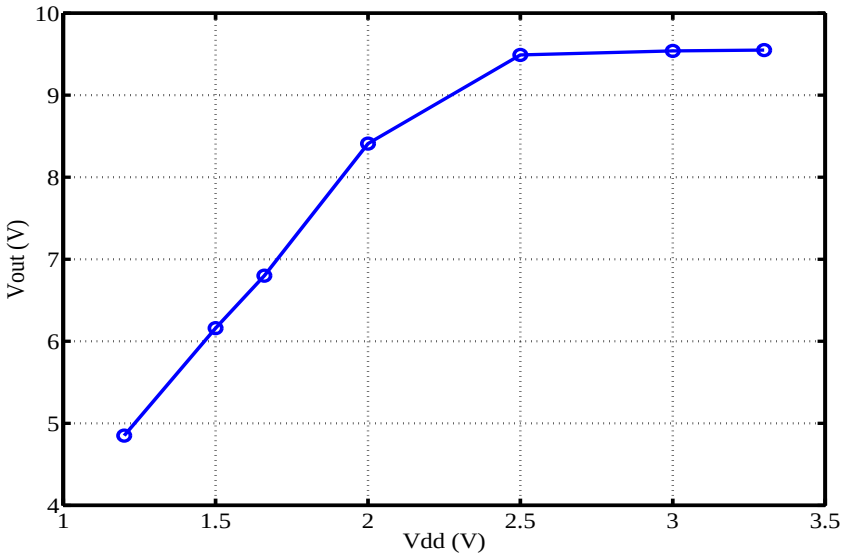


Figure 5.10: Measured Vout of the proposed circuit without load and with different Vdd.

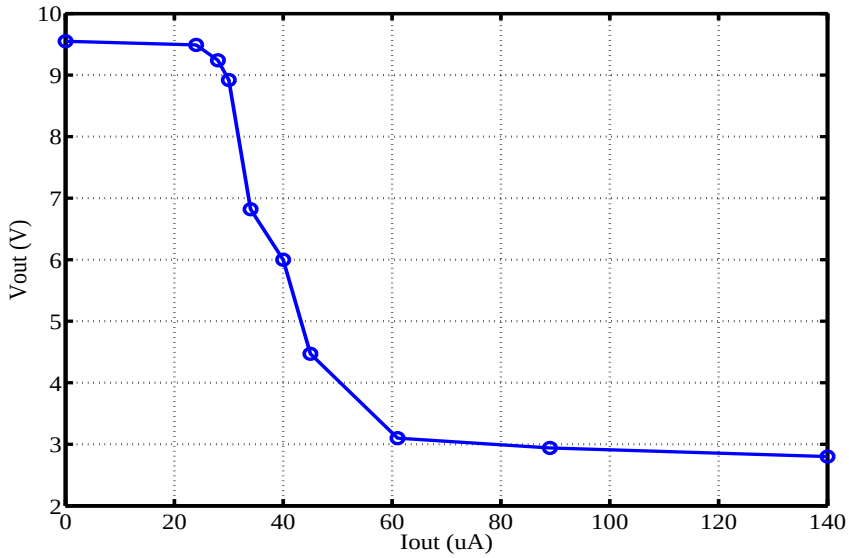


Figure 5.11: Measured Vout of the proposed circuit with Vdd=3.3 V and different loads.

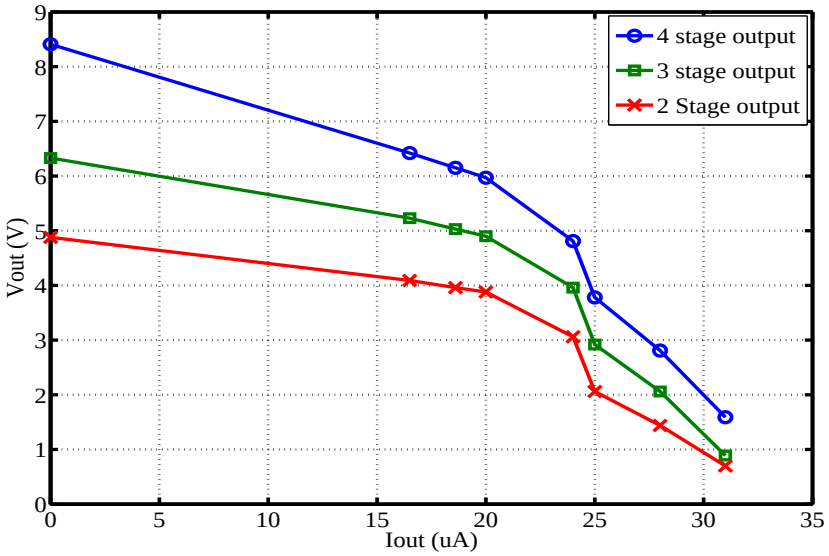


Figure 5.12: Measured Vout of the proposed two-stage, three-stage, and four-stage circuit with Vdd=2.0 V and different loads.

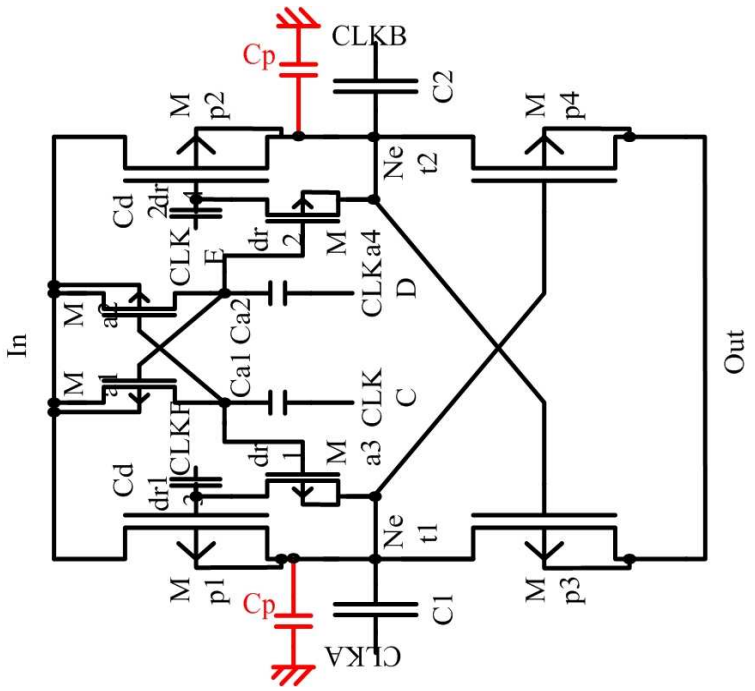


Figure 5.13: Parasitic capacitors in the proposed charge pump circuit.

The measured output voltages of the proposed charge pump circuit with Vdd=3.3 V and different loads are shown in Fig. 5.11. The measured output voltages of the proposed two-stage, three-stage, and four-stage charge pump circuit with Vdd=2.0 V and different loads are presented in Fig. 5.12.

5.3.4 Discussions

As shown in the simulation results and measurement results, the measured output voltages are little lower than the simulation output voltages because of the parasitic capacitor of each stages as shown in Fig. 5.13. In real circuit, the parasitic capacitor Cp is taken into account by reducing the clock signals because a voltage divider is formed by C1 and Cp. In the ideal case, the voltage step of each stage between input terminal and output terminal is Vdd. However, in the real circuit the voltage step of each stage becomes $Vdd\frac{C}{C+Cp}$ due to the voltage divider. Therefore, the measure

output voltages are little lower than the simulation results. The parasitic capacitance is caused by process, bonding wires and the package. Besides, as shown in Fig. 5.10 and Fig. 5.11, the maximum output voltage of the proposed circuit is limited by the breakdown voltage between N-well and P-substrate [5].

5.4 Conclusions

A high efficiency all PMOS charge pump circuit without high-voltage overstress is proposed in this chapter. The proposed driver circuit with six-phase clock generator can reduce the equivalent on-resistance of charge-transfer transistors. Moreover, the driver circuit can completely switch on the charge-transfer transistors and can prevent charge back to the previous stage. In addition, the body effect is eliminated due to the proposed two pumping branches architecture. Therefore, its voltage pumping efficiency is much higher than that of the conventional charge pump circuits.

The measured results confirmed that the proposed charge pump circuit has a high pumping efficiency without overstress and the proposed charge pump circuit can be realized in any low-voltage single-well standard CMOS technologies.

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Chapter 6

CONCLUSIONS AND FUTURE WORKS

In this dissertation, several low-power design techniques and power management circuits for ubiquitous device are proposed, which are summarized as follows.

6.1 Summary of Low-Power Design Techniques

Threshold voltage of a MOSFET can be reduced electrically by using forward biased body-effect which helps in reducing the supply voltage and power dissipation. In addition, the temperature characteristic can be modified by body-effect. The proposed reference can operate at a supply voltage down to 0.95 V in a standard CMOS 0.35 μm technology with threshold voltages of about 0.5 V and -0.65 V for n-channel and p-channel MOSFETs, respectively. The minimum power dissipation is 1.1 μW and the supply voltage dependence is -0.36 mV/V (Vdd=0.95$\sim$3.3 V). No particular analog process options are required. This circuit with a simple architecture is suitable for low-voltage micro-power electronic applications.

A continuous-time phase frequency detector (PFD) based on conventional tri-state PFD is proposed for fast lock charge pump phase-locked loops (CPPLLs). When the PLL is in out of lock state and the phase difference is large, the continuous-time circuit is activated. More current will be injected into the loop filter, therefore, the locking time is reduced. When the PLL is in near locking state, only the conventional PFD exists to realize the fine tuning. Therefore, the proposed architecture can achieve fast lock without extra power dissipation. Any conventional tri-state PFDs can be improved with the proposed continuous-time architecture. The simulation results demonstrate that the proposed continuous-time PFD is effective to reduce the locking

time without extra power dissipation.

6.2 Summary of Power Management Circuits

An energy management circuit for efficiently managing the scavenged ambient energy has been proposed for ubiquitous sensor modules using vibration-based energy generation. The implementation of the proposed circuit with a standard CMOS process is presented and further validated by experimental results. The energy management circuit can avoid the long start-up time problem and can improve the level of integration. Based on our experimental results, the proposed energy management circuit can be used as a battery for any ubiquitous sensor modules using different ambient energies. The proposed energy management circuit is effective in managing the scavenged ambient energy and maximizing the potential applicability of the sensor module.

A high efficiency all PMOS charge pump circuit without high-voltage overstress is proposed in this paper. The proposed driver circuit with six-phase clock generator can reduce the equivalent on-resistance of charge-transfer transistors. Moreover, the driver circuit can completely switch on the charge-transfer transistors and can prevent charge back to the previous stage. In addition, the body effect is eliminated due to the proposed two pumping branches architecture. Therefore, its voltage pumping efficiency is much higher than that of the conventional charge pump circuits. The measured results confirmed that the proposed charge pump circuit has a high pumping efficiency without overstress and the proposed charge pump circuit can be realized in any low-voltage single-well standard CMOS technologies.

6.3 Future Research Works

For the low-power voltage reference design, the future works should focus on how to improve the output initial accuracy performance of reference voltage due to the large deviation of threshold voltage of MOSFET, the MOSFET layout mismatching, the absolute value deviation of resistor, and the offset voltage of amplifier. At the same

time the noise of the voltage reference should be considered especially for implantable medical device application.

For the PLL design, the future works may focus on the jitter and power reduction of voltage control oscillator (VCO) because the VCO is the key cell cell in PLL design and the noise performance of VCO determines the overall PLL noise performance.

For the power manager circuit design, the future works may focus on how to increase efficiency of the whole system.

For the charge pump circuit design, the future works may focus on how to reduce the complexity of drive circuit and chip size.

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