Waseda University Doctoral Dissertation

SiGe-Based Broadband and High Suppression Frequency Doubler ICs for Wireless Communications

SUN, Jiangtao

Graduate School of Information, Production and Systems

Waseda University

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Contents

Chapter 1 Introduction

1.1 Background

Our world has been greatly affected by the silicon-based integrated circuits made for all kinds of wireless systems at RF and microwave frequencies. Such systems cover from short range radio frequency identification (RFID), wireless body area network (WBAN), electronic toll collection system (ETC) and wireless fidelity (WiFi) to long range wireless microwave access (WiMax) and long term evolution (LTE) [1]-[6].

Although the wireless systems at microwave band have flooded the markets, the systems of quasi-millimeter-wave or millimeter-wave are attractive and on the markets. Several emerging 60GHz standards, including wireless HD, IEEE 802.15.3c, and European computer manufacturers association (ECMA) 387, are targeted toward short-range wireless personal area networking (WPAN) such as high definition streamed multimedia and high-speed data transfers [7]-[9]. Another millimeter-wave application is the vehicular intelligent safety systems, which allow the vehicle to perceive the surrounding environment and avoid road accidents. The adoptions of both 24/26GHz and 79GHz short-range radar (SRR) and 76-77GHz (hereafter referred to as 77GHz) long-range radar (LRR) sensors have different advantages in comparison with other safety systems (e.g. lidar, video, infrared, acoustic, etc.) [10]-[13].

Automotive radar sensors enable a 360° safety zone around the vehicle. Several short-range sensors are usually mounted around the vehicle to detect objects at close range (0-40m), which enable advanced driver-assistance and security functions including collision avoidance, precise

airbag activation, parking assistance, improved road handling, lane change support and short-range adaptive cruise control (ACC) stop-and-go capability (Fig.1-1) [14]. On the other hand, a single forward-looking sensor may be sufficient for long-range detection (≈150m), primarily used for ACC [15].

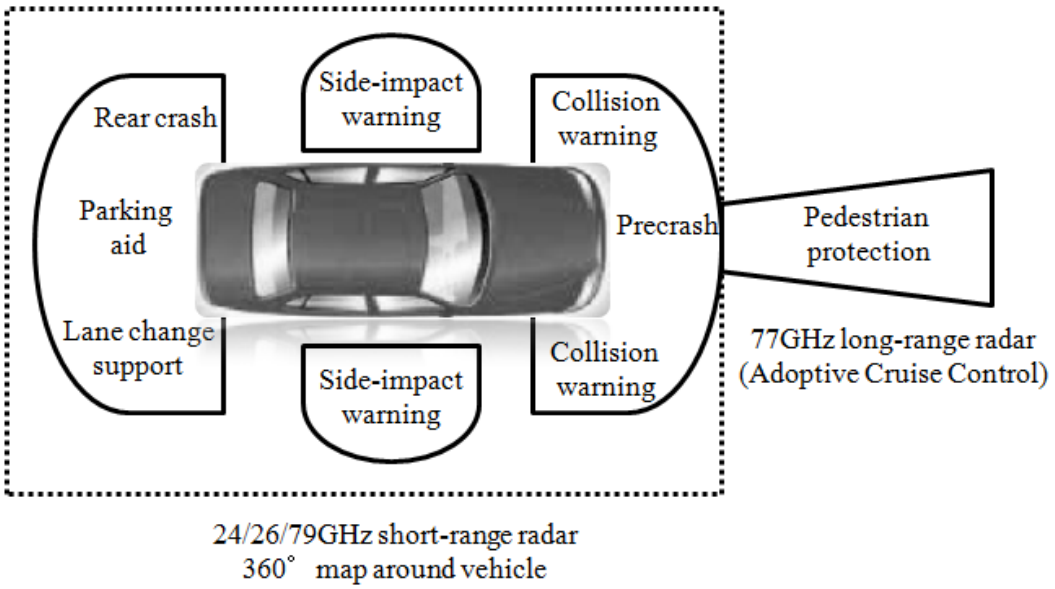


Fig.1-1 Image of radar sensor applications in an automotive environment.

Developing vehicular radar sensor systems in quasi-millimeter-wave and millimeter-wave bands, both academic and industrial, have instigated intensive research and development. Long-range radars in III-V technologies enabling ACC operating in the 77GHz band have been around for some time [15]. Since small form-factor and low cost are imperative for automotive applications, silicon-based implementations are attractive and can make radar sensors affordable to the end customer. In the last few years, silicon-based 24GHz short-range automotive radars have been investigated both by industry and academia [16][17]. Recent works have demonstrated the possibility of designing highly-integrated high-frequency circuits in advanced silicon technologies [18][19]. In fact, 24GHz silicon-based short-range radar sensors have already been deployed in the commercial automotive market [14]. Realization of 24GHz short-range radar transceiver circuits has been reported in a Silicon-Germanium (SiGe) process [14][20], but suffers from limited integration, limited bandwidth and high power dissipation.

Intensive research and development is also underway for developing 77GHz long-range and 79GHz short-range radars in silicon technologies [21][22]. Most of the current efforts have focused on chip development in high performance SiGe technologies. A SiGe-based four-channel transceiver (TRX) IC for use in long-range ACC and collision-avoidance systems is in production [19]. Experimental results on a 77GHz transceiver in 65-nm CMOS have recently been reported by the academia [23].

Several radar architectures have been studied and employed during the last century [24]. In the context of automotive radars, only a few architectures are of relevance, and can be classified into two categories: frequency modulation continuous-wave (FMCW) and pulsed. FMCW based architecture is the most popular for automotive radars, and has been employed in short-range/long-range radar implementations [23]. In FMCW radars, the frequency of the radar signal is varied according to a pre-determined pattern. The most widely used patterns is linear frequency modulation (LFM), in which frequency is changed by a step in each time period. An FMCW radar transmits a continuous wave, which is triangularly modulated in frequency, and receives the wave reflected from objects. As can be illustrated in Fig.1-2, for a moving target, the received frequency would be shifted (i.e., Doppler shift), resulting in two different offset frequencies f^+ and f^- for the falling and rising ramps. Denoting the modulation range and period as B and T_m, respectively, we can derive the distance R and the relative velocity V_R as

$$R = \frac{cT_m}{4B} \cdot \frac{(f^+ + f^-)}{2} \tag{1-1}$$

$$V_R = \frac{c}{2f_c} \cdot \frac{(f^+ - f^-)}{2} \tag{1-2}$$

where f_c represents the center frequency and c the speed of light.

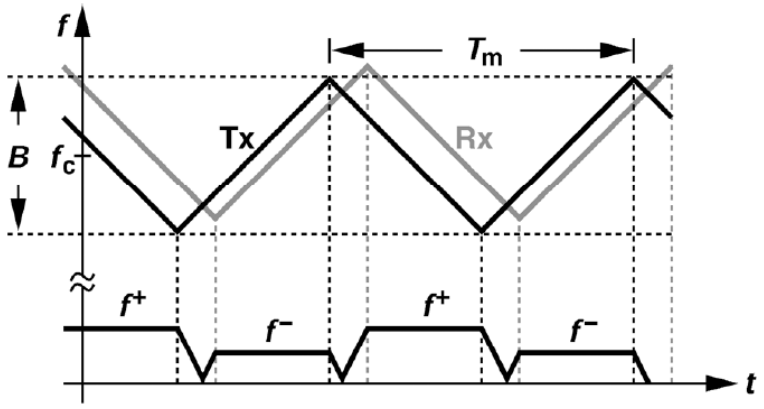
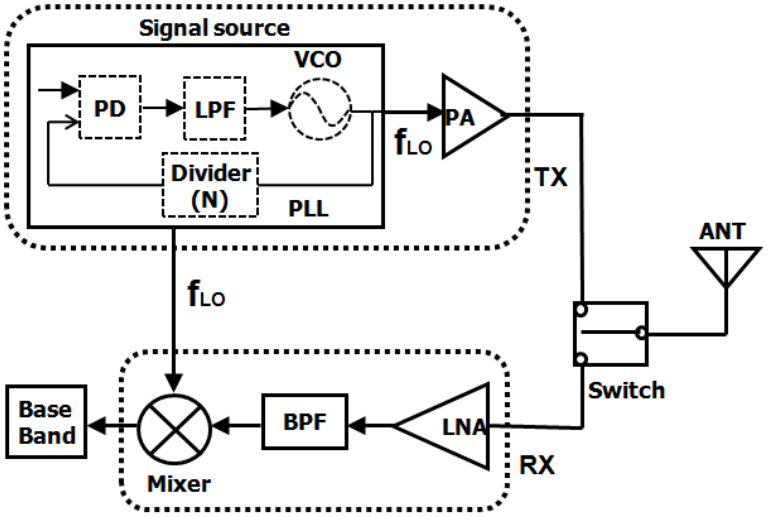


Fig.1-2 FMCW radar operation principle.

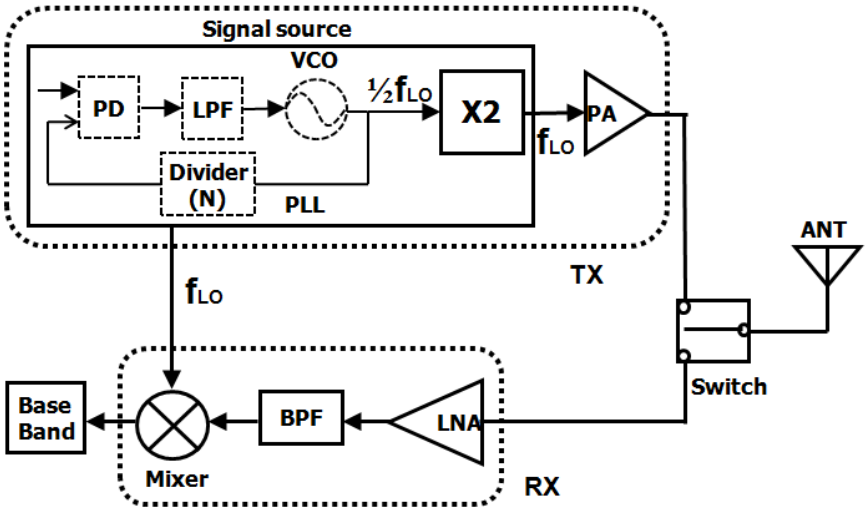
1.2 Frequency doubler in wireless communication systems

Signal sources in quasi-millimeter-wave and millimeter-wave systems for radar and wireless communication applications are applied to generate transmission signals or to provide the local oscillator for mixers. A millimeter-wave oscillator at the desired fundamental carrier frequency often has the disadvantage of high phase noise and, hence, needs to be stabilized e.g. in a phase-locked loop (PLL) architecture shown in Fig.1-3(a). The signal source in Fig,1-3(a) is composed of phase detector (PD), low pass filter (LPF), voltage control oscillator (VCO) and frequency divider.

A major obstacle to low DC power high frequency transceiver implementation is the performance degradation with increasing frequency of key passive components, variable capacitors in particular. This is particularly severe in frequency synthesizers where high frequency VCOs consume large power, display relatively poor spectral purity and have limited tuning range, and PLL's divider requires large input voltage swing and eventually burn more power than the VCO itself [25][26].



(a)



(b)

Fig.1-3 FMCW architecture for wireless communication transceiver : (a) Conventional transceiver (b) Transceiver integrating with frequency doubler

On the other hand, the signal of a high quality VCO at low frequencies can be multiplied up to the desired millimeter-wave frequency, entailing a degradation of the phase noise of 20log$n$, with n being the multiplication factor. The signal source using frequency doubler in which n is 2 is shown in Fig.1-3(b).

There are several reasons to use a lower frequency oscillator with a frequency doubler instead of an oscillator at a higher frequency. The phase noise of the latter is usually higher than that of the former. Furthermore, the use of a frequency doubler is beneficial for a high-frequency PLL. Generally, a VCO oscillates up to f_{max} and a frequency divider operates up to 1/4 and 1/2 of f_t. It is very difficult to increase the operating frequency of a frequency divider up to the output of a high-frequency VCO. A frequency doubler (or multiplier) with a VCO has half the frequency output. Thus, the maximum operating frequency of a frequency divider followed by a VCO in PLL is mitigated by half [27].

Another reasons is the avoidance of VCO pulling which results in VCO eventually lock to the interferer frequency [28]. Various sources can introduce VCO pulling. For example, the power amplifier output may couple to the VCO. Another example of injection pulling arises in the receive path when the desired signal is accompanied by large interferer. If the interferer frequency is close to the LO frequency, coupling through the mixer may pull desired frequency to interferer frequency. Thus, the VCO must be followed by a buffer stage with high reverse isolation, which may increase the phase noise, DC power consumption and design difficulty. Hence, the VCO with frequency doubler may avoid these problem.

1.3 Research subjects of frequency doubler

Frequency doubler which is a key component in the signal source for high frequency applications is faced with several design subjects such as operation bandwidth, fundamental frequency suppression, conversion gain, input drive power and DC power consumption. A frequency design pentagon is shown in Fig.1-4. When designing a high performance frequency doubler, the subjects demonstrated in Fig.1-4 must be tradeoff. In this section, the operation bandwidth, fundamental frequency suppression, conversion gain, input drive power and DC power consumption will be described in detail. Then figure of merit (FOM) are defined to verify the performance of the frequency doubler.

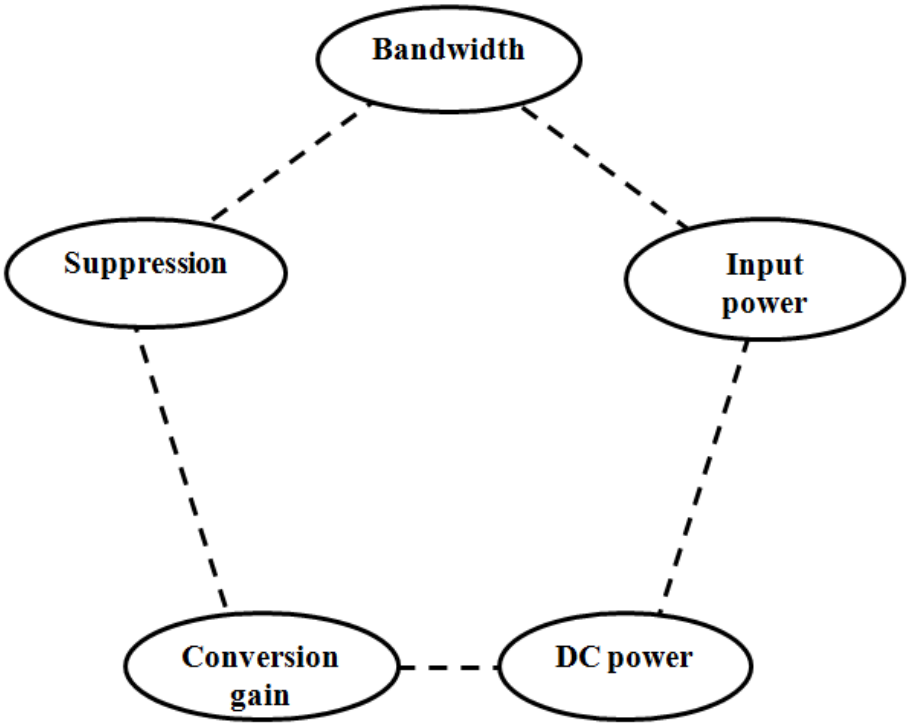


Fig.1-4 Frequency doubler design pentagon

1.3.1 Operation bandwidth

In the signal source, the operation bandwidth of frequency doubler determines the operation band of radar sensor. However, in the world, organizations which draws up regulation has announced various available frequency band in different region such as in USA, EU and Japan. In the US, there are two regulations. In 2002 the Federal Communication Committee (FCC) adopted the 24GHz radar sensor approach for the operation of vehicular radar in the ultra wide band (UWB) of 22-29GHz [29]. From 2004, the frequency is shift to 23.12-29GHz and this allocation is without any restriction in time or in quantity. From 2003, EU adopted 24GHz band and 79GHz band for SRR applications [30]. However, the 24GHz is interim technology until mid of 2013. Now the 26GHz band applications in EU has been proposed. Maybe in the future

26GHz band and 79GHz band SRR will be harmoniously available in EU.

In Japan as a very important region where many technologies are in competition, Ministry Internal Affairs and Communications (MIC) of Japan guided the academic and industrial to investigate the quasi-millimeter-wave radar several years. However an allocation for 24GHz SRR is not yet available in Japan. Since December 2006 a study group works on the boundary condition for the frequency allocation for UWB SRR. Short range automotive radar frequency allocation (SARA) proposes an allocation for 24GHz for a limited time and an allocation around 26GHz analog to the upper part of the US regulation without any restrictions in time or quantity [31].

The global frequency regulations status is shown in TABLE 1-1. From this table, the frequency doubler should cover the band from 22GHz to 29GHz to meet the frequency band in USA, EU and Japan.

TABLE 1-1

Global frequency regulations status of automotive radar sensor frequency bands

	24GHz Narrow band	24GHz UWB for SRR	26GHz UWB for SRR
USA	100/250MHz Available	7GHz Available	4GHz Available
EU	200MHz Available	5GHz Until 2013	4GHz Proposed
Japan	75MHz Available	2.25GHz Study underway	4.25GHz Proposed

1.3.2 Fundamental frequency suppression

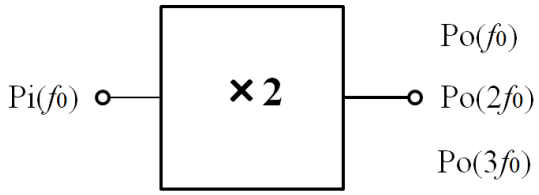


Fig.1-5 Input/output of frequency doubler

The frequency doubler usually adopts nonlinearity of transistors and frequency multiplication. The Fig.1-5 shows the input and output of frequency doubler. From Fig.1-5, the desired output power of frequency doubler is the power of the second harmonic frequency. However, as the desired power being generated, the unwanted powers are also accompanied with the desired power such as fundamental frequency, third harmonic frequency and so on. In the Fig.1-3(b), the unwanted frequency may be injected into power amplifier (PA) and couple to the low noise amplifier (LNA) by the switch. The unwanted powers going into the PA and LNA deteriorate the performance of PA and LNA [32]. Moreover, these unwanted frequencies may result in de-sensitization, cross modulation and inter modulation by the radiation of antenna when the unwanted signals fall in the corresponding bands [33]. In the UWB spectrum mask announced by FCC, the fundamental suppression should be greater than 20dBc. Hence, the output of frequency doubler should reject the unwanted frequencies, fundamental frequency in particular. The fundamental frequency suppression is defined as below:

$$F.S(dBc) = 10\,log_{10}\left(\frac{P_o(2f_0)}{P_o(f_0)}\right) \tag{1-3}$$

where F.S indicates the suppression ratio.

1.3.3 Conversion gain and input power

Frequency doubler cascading with VCO or PLL supplies power to the subsequent stages such as PA in transmitter and down converter in receiver path. Driving PA or down converter needs frequency doubler with a certain conversion gain. Conversion gain is defined in equation 1-4.

$$C.G(dB) = 10\,log_{10}\left(\frac{P_o(2f_0)}{P_i(f_0)}\right) \quad (1\text{-}4)$$

where C.G indicates the conversion gain.

From the equation 1-4, the conversion gain is ratio of output power with respect to input power. The input of frequency doubler is the output of VCO or PLL. Hence, the output power of VCO determines the input power of frequency doubler. As known that, the output power of VCO in high frequency band is not high. The high output power of VCO consumes high DC power including output amplifier. Hence, frequency doubler should exhibit high conversion gain in low input power which releases the design difficulty of VCO.

1.3.4 DC power consumption

The DC power consumption of frequency doubler is not larger compared with the PA. However, obtaining high output power of frequency doubler is at cost of large DC power, the frequency doubler implemented in compounded semiconductor devices such as Indium Phosphite (InP), Gallium Arsenide (GaAs) in particular. Though Si-based frequency doubler can be operated in low supply voltage and consume low DC power, high input power must be provided to drive doubler and the output power is low. The injection locked frequency multiplier is used to in low DC power consumption, however, its performance is determined by injected power and the bandwidth is narrow.

1.3.5 FOM

As mentioned above, many performance indexes are given, such as bandwidth, fundamental suppression, and DC power consumption. Comparing the doubler performance with other works fairly is important. Hence, figure of merit (FOM) to evaluate the performance of doubler is defined in equation 1-5.

$$FOM = 20log_{10}(BW \times 100) + F.S - 10log_{10}\left(\frac{P_{DC}}{1mW}\right) \quad (1\text{-}5)$$

In this equation, BW and P_{DC} are the frequency bandwidth and DC power consumption of the frequency doubler. The BW is a relative bandwidth. F.S denotes fundamental frequency suppression of the frequency doubler.

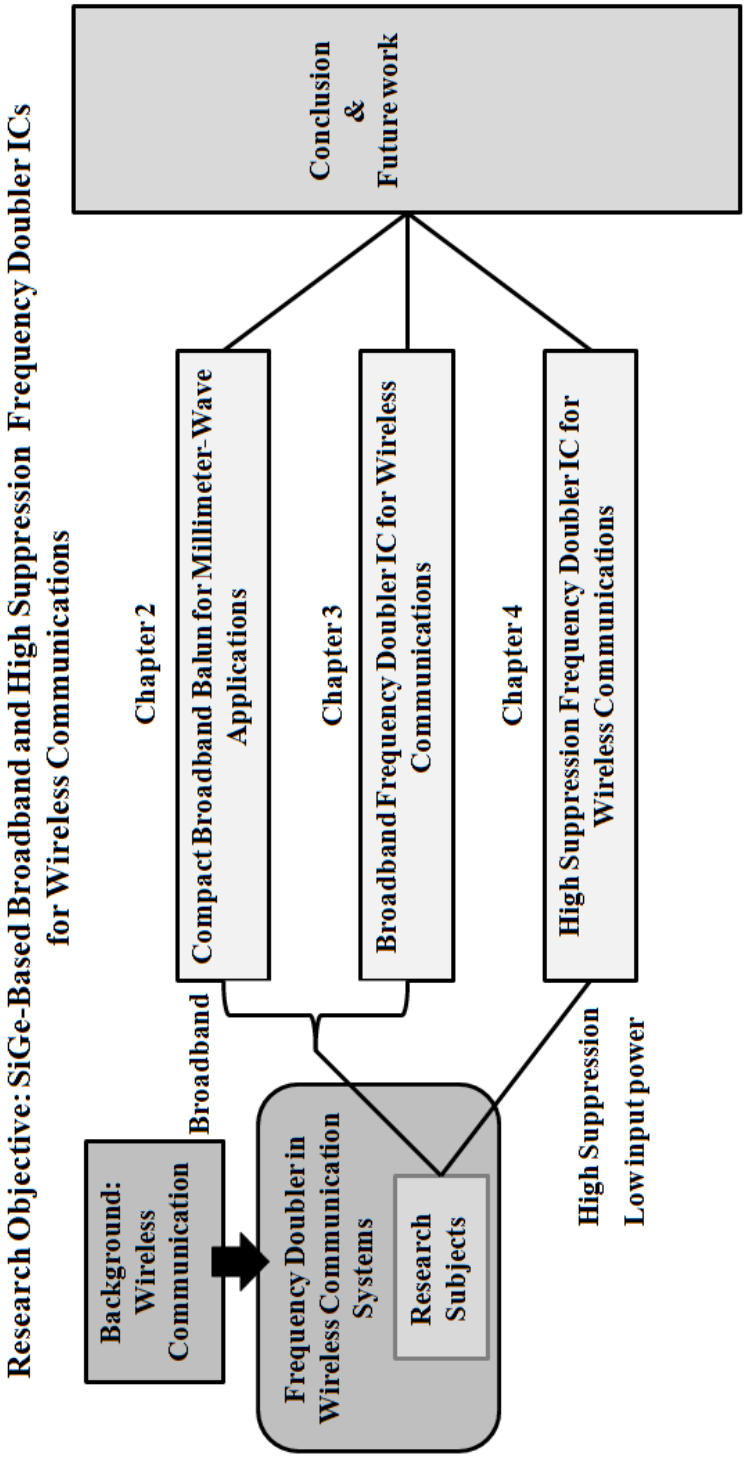


Fig.1-6 Research objective of high performance frequency doubler IC

1.4 Objective and organization of this dissertation

The objective of this dissertation is to achieve high performance of frequency doubler IC used in wireless communication. As mentioned above, several research subjects of frequency doubler are worth studying. In this dissertation, broadband, high suppression and low input power of frequency doubler are focused on. This dissertation consists of five chapters. From Chapter 2 to Chapter 4, these subjects will be researched and demonstrated using the proposed scheme. At last, the conclusion and future work will be given in the Chapter 5. The Fig.1-6 shows the research objective and organization of this dissertation.

In the Chapter 2, a compact broadband Marchand balun based on silicon technology is implemented and valued. Firstly, the passive baluns are reviewed in the section 2.2 in which the Marchand balun is a good candidate to be chosen due to wideband imbalance performance. Then, the cross-section of SiGe BiCMOS which is used to design balun is introduced in section 2.3. The balun design is described in section 2.4 in which a effective slow wave pattern ground structure is proposed. At last, a compact broadband balun is implemented and measured in section 2.5. This work achieves 1dB of amplitude imbalance and 10° of phase imbalance in the band of 20GHz-50GHz. In this band, the minimum insertion loss is 1.5dB. The VSWR which is less than 2 is from 23.4GHz to 39.1GHz. The chip core size is only 0.03mm^2. Compared with the balun using the conventional slot pattern ground structure, the 6-dB cuf-off frequency is extended by 6.6GHz.

In the Chapter 3, a broadband frequency doubler IC based on silicon technology is implemented and valued. Firstly, the broadband frequency doublers are reviewed in section 3.2 in which active doubler is selected due to high conversion gain and low input drive power. Then, the RF performance of SiGe BiCMOS used in this dissertation is introduced in section 3.3. The SiGe BiCMOS technology exhibits excellent radio frequency performance indicating very suitable for millimeter-wave applications. In the section 3.4, an internal low pass filter technique is designed to achieve high suppression, and a pair of matching circuits is effective so that keep the doubler operates in low input drive power with high suppression. At last, the measured results exhibit better than 30dBc in a broad frequency band of 22-30GHz.

In the Chapter 4, a high suppression and low input power frequency doubler IC based on push-push circuit is implemented and valued. Firstly, the frequency suppression techniques are reviewed in the section 4.2. Then, high suppression frequency doubler is proposed and de-

signed. In the frequency doubler, a series LC resonator rejects the fundamental frequency at the output of the doubler core and matches with the input impedance of the output buffer simultaneously. At last, the measured results of the doubler shows fundamental frequency suppression as high as 66dBc and conversion gain of 9.2dB at an output frequency of 26GHz which exhibit comparable performance with the compounded technology.

1.5 Conclusion

In this chapter, the trend of wireless communication applications is introduced in the background, vehicular radar sensor in particular. The frequency doubler in the wireless communications systems is a key component composing of stable signal source which is explained in the section 1.2. There are several research subjects for the frequency doubler such as operation bandwidth, frequency suppression, conversion gain, input drive power and DC power consumption. These subjects are described in detail in section 1.3 and performance evaluating equations are also defined. At last, the objective and organization of this dissertation are given.

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Chapter 2 Compact Broadband Marchand Baluns for Millimeter-Wave Applications

2.1 Introduction

In the Chapter 1, the trend of millimeter-wave communications has been demonstrated. Recently, millimeter-wave communication market has experienced explosive growth, boosting the developments of millimeter-wave circuits based on advanced CMOS and SiGe BiCMOS processes. And many RF transceivers use a combination of single-end and differential device. To interface these different components within a transceiver, a balance to unbalance (or vice versa) component called balun is essential. Hence, broadband baluns are critical components incorporating into circuits such as mixers, power amplifiers and antennas in millimeter-wave band applications shown in Fig.2-1 [1]-[3].

Generally, balun includes active balun and passive balun. In the case of active balun, it is usually implemented based on transistor. There are various types of active baluns such as a common-source/common-gate type, a source/drain type, a push-pull type and a distributed balun type [4]-[7]. An important property of active balun is DC power consumption. Although the active balun generates conversion gain, its bandwidth is narrow.

Another case is passive balun implemented by coupling line [8]. Because the passive balun requires no DC power consumption, has little dependence of performance on the temperature and has no linearity requirement, passive baluns are better candidates compared with active

baluns from the point of view of the DC power consumption and linearity. TABLE 2-1 shows the comparisons between active balun and passive balun.

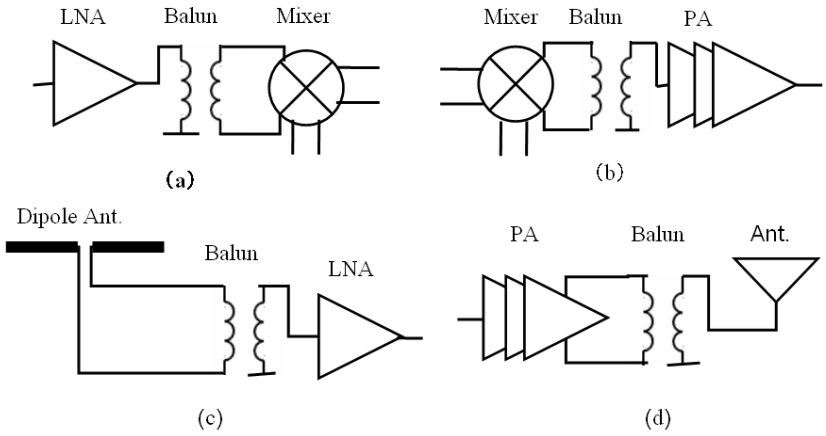

Fig.2-1 Balun applications for differential circuits

TABLE 2-1

Summary of characteristics of active balun and passive balun

	Active balun	Passive balun
Loss/gain	conversion gain	insertion loss
DC power consumption	with	without
Bandwidth	narrow	moderate
Chip size	moderate	large
Balance performance	moderate	good
Performance dependency on temperature	with	without
Linearity requirement	with	without
Directionality	unidirectional	bi-directional

The important figure of merits of balun includes amplitude imbalance, phase imbalance, insertion loss/conversion gain and chip area efficiency. Ideally, the signals at the two differential ports are perfectly equal in amplitude and 180° out of phase for all frequencies, however, in

fact the amplitude of balanced ports are slightly different. The definition of amplitude imbalance is shown in equation 2-1, and similarly, the definition of phase difference between balanced ports is given by equation 2-2.

$$Amplitude\ imbalance/dB = \Delta = 20 * log_{10} \left|\frac{S_{31}}{S_{21}}\right| \tag{2-1}$$

$$Phase\ imbalance/° = \theta = |\angle S_{31} - \angle S_{21} - 180°| \tag{2-2}$$

S_{21} and S_{31} are the transmission S-parameters from unbalanced port to balanced ports, respectively.

When designing a balun, the performance tradeoffs of these figures of merits should be carefully considered to obtain most optimized performance. This chapter is organized as follows. Review of previous passive baluns is followed this part shown in section 2.2, and section 2.3 reviews the metal layer structure of SiGe BiCMOS technology. Then section 2.4 gives the design of proposed balun using modified slot pattern ground, and section 2.5 demonstrates the measured results. Finally, section 2.6 gives a conclusion.

2.2 Passive balun review

Passive balun usually utilizes the transmission lines coupling. There are three kinds of balun that will be introduced in this section.

2.2.1 Transformer-based balun

Transformer is well known applied in RF ICs, i.e. LNA, VCO, mixer, to obtain good impedance matching, low noise figure, wideband operation etc. Due to the symmetrical property from the point of view of physical layout and electrical characteristic, transformer can be easily operated as a balun. [9][10]. However, from the applications of this kind of balun, it is effective operating less than 10GHz and narrow band. Self-resonance frequency limited high frequency application owing to the parasitic capacitance. In addition, this kind of balun usually needs be parallel with capacitors in the input and output to tune the balance performance and insertion loss.

2.2.2 Transmission line balun

Transmission line balun usually is designed in printed circuit board because of occupying large area, for instance, lange coupler, wilkinson coupler, rat-race balun. Lange coupler based balun shows narrow bandwidth of phase imbalance (less than 10°) [11]. In the terms of wilkinson coupler based balun exhibits wideband characteristic of phase imbalance and good phase imbalance performance which is less than 3° in the W-band [12]. However, the chip size is 0.24mm^2. The rat-race balun is another type to achieve broadband operation which drawback also is large chip size [13]. The drawback of large size of transmission line shows limitation in the quasi- and millimeter-wave applications.

2.2.3 Marchand balun

Marchand balun is an important and widely useful kind of passive balun due to wideband property since it has been first proposed by Marchand [14], then simplified by Roberts [15]. Basically, the Marchand balun consists of an unbalanced open end, two short ends and balanced transmission line shown in Fig.2-2. Many researchers are engaging in improving performance of Marchand balun on-chip, i.e. planar spiral Marchand balun [16], stacked spiral Marchand balun [17], spiral Marchand balun with slot pattern [18], asymmetric broadside-coupled Marchand balun [19], meandered multiplier Marchand balun [20] and 3-D Marchand balun [21].

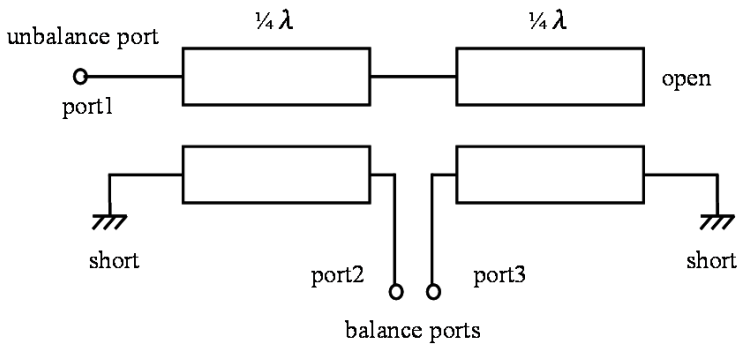

Fig.2-2 Equivalent circuit of Machand balun

TABLE 2-2

Summary of recently published works

Ref.	Type	Size/mm^2	Bandwidth/GHz @AI/PI[a]	Bandwidth of 3dB insertion loss[c] /GHz
[13]	Rat-race	0.35	40-61@1.5dB/15°	44-61
[16]	Planer spiral Marchand	0.16	4-16@2dB/10°	NA
[17]	Stacked spiral Marchand	0.05	22.4-37.3@1dB/10°	NA
[18]	With slot pattern Marchand	0.07	18.4-32.2@1dB/5°	17.8-39
[19]	Asymmetric broad-side-coupled Marchand	0.06	16.5-67@1dB/5°	22-54
[20]	Meandered Marchand	0.058	15.5-40@NA[b]/10°	16-40
[21]	3-D Marchand	0.12	25-50@3dB/6°	NA

a:Amplitude Imbalance/Phase Imbalance.

b:Amplitude imbalance is 1.5 dB at 23.6GHz.

c:The 3dB insertion loss excludes ideal 3dB balun loss.

To have insight into these baluns performances, comparison of performance is depicted in TABLE 2-2. From this table, the rat-race balun has 41.6% of bandwidth, but its balun size is large and its balance performance is not good. The Marchand balun listed in the table illustrates good phase imbalance performance which is less than 10°. Baluns in [17]-[21] use size reduction technique such as staked technique, slot pattern technique, meandered technique and 3-D technique. However, the staked balun and 3-D balun has high insertion loss and the amplitude imbalance of the meandered balun is 1.5dB at 23.6GHz. The balun in [19] using two size reduction techniques simultaneously has good imbalance performance and wide bandwidth of insertion loss, however, its balun size is not small. The slot pattern type balun has a potential to reduce size further, however, the balun in [18] does not show high size efficiency.

Although Marchand baluns mentioned above could reduce balun size, operate in broad bandwidth and have good imbalance performance, to further save chip size, reduce insertion loss with good imbalance performance in broadband is a meaningful challenge work.

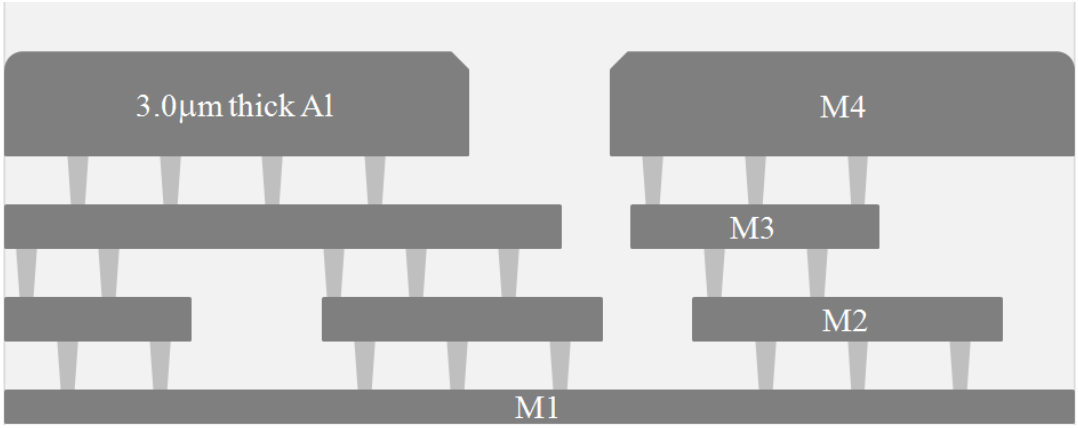

Fig.2-3 The cross-section view of 0.25-μm SiGe BiCMOS technology [22]

2.3 Cross-section introduction of SiGe BiCMOS

The balun is to be designed on the 0.25-μm SiGe BiCMOS technology. Then before designing the balun, it is necessary to introduce the metal layers structure of this technology. Fig.2-3 shows cross-section of the metal layers of 0.25-μm SiGe BiCMOS technology. From Fig.2-3, it is seen that this technology includes four metal layers (M1-M4), and the thickness of the top metal layer (M4) is 3-μm which can result in low loss.

2.4 Compact broadband balun design

From this section, we propose a effective slot pattern ground to reduce the balun size. Considering the band width of the imbalance performance, the high ratio of the even-mode impedance with respect to the odd-mode impedance is needed. The transmission line width and space is optimized to obtain wide bandwidth of imbalance performance.

2.4.1 Design goal

As reviewed in section 2.2, the Marchand balun has better performance than transformer-based balun and transmission line balun. Hence, Marchand balun is a good candidate to be chosen. The balun is to be operated in the quasi-millemter-wave and millimeter-wave applications. The insertion loss is to be less than 3dB in the operation band and the imbalance performance is to be within 1dB/10° in the operation band. The balun size is to be less than $0.04mm^2$. The design goal is listed in the TABLE 2-3.

TABLE 2-3

Design goal of this work

Balun type	Operation band	AI/PI[a]	Insertion loss[b]	Size
Marchand	22-50GHz	1dB/10°	< 3dB	$< 0.04mm^2$

a:Amplitude Imbalance/Phase Imbalance. b:Insertion loss is excluding 3dB balun ideal loss.

2.4.2 Analysis and design of proposed slot pattern ground

Due to the silicon substrate floating, the explicit ground is indispensable, which can supply accurate common ground for signal lines. The solid ground can effectively reduce the loss generated by the silicon substrate because the electric field of signal lines would be terminated before reaching the silicon substrate. However, the critical issue occurs according to the Lenz's law, which can induce the eddy current on the solid ground. The direction of the eddy current is opposite to the one in the signal lines. According to the coupling line theory, the negative mutual coupling between the eddy current and the signal lines current could reduce the magnetic flux, and thus the signal lines inductance. In addition, both the solid ground and the signal lines can also be treated as a non-inverting transformer [23], thus the input resistance of the signal lines will be increased, which can increase the insertion loss and decrease the Q value.

Slot pattern ground structure (also called defected ground structure) is widely used in miniaturization for microstrip antenna [24], microstrip filter [25] and other impedance matching circuits for active devices [26] due to slow wave effect in wave propagation. Generally, the slow wave factor (SWF) is defined by λ_0/λ_{gd} where λ_0 is the free space wavelength and the λ_{gd} is the guide wavelength. Furthermore, the SWF of the microstrip line with slot pattern ground

is defined by $\varepsilon_{eff.d}$ and given as follows [27]:

$$\sqrt{\varepsilon_{eff,d}} = \frac{\lambda_0}{\lambda_{gd}} \tag{2-3}$$

$$SWF(f) = \sqrt{\varepsilon_{eff,d}} = \frac{\lambda_0 \cdot \Delta\theta(f)}{360L} + \sqrt{\varepsilon_{eff}} \tag{2-4}$$

$$\sqrt{\varepsilon_{eff}} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left(1 + 12\frac{h}{w}\right)^{-0.5} \tag{2-5}$$

In the above equations, L is the physical length of microstrip lines, ε_{eff} is the effective permittivity of microstrip without slot pattern ground, and $\Delta\theta(f)$ is the phase difference (in degrees) of S_{21} of microstrip lines between with slot pattern and without slot pattern ground. The dispersion effect caused by slot pattern ground is indicated by $\Delta\theta$.

In [18], a conventional U-type slot pattern for Marchand balun was introduced to reduce balun size and insertion loss shown in Fig.2-4 (a). However, this type slot pattern cannot provide sufficient slow wave effect to further reduce balun size. Hence, a new slot pattern is proposed to achieve size reduction shown in Fig.2-4 (b). In order to compare the proposed slot pattern with conventional one, a spiral transmission line is designed using the conventional slot pattern ground and the proposed one, respectively. The simulated phases of S_{21} of the spiral transmission line with proposed and conventional slot pattern grounds are demonstrated in Fig.2-5. In this figure, the phase difference is also shown, which indicates that the proposed slot pattern ground delay the signal propagation compared with the conventional one. To describe this effect quantitatively, the SWFs of the proposed slot pattern ground and conventional one can be calculated by the equation 2-4, respectively. The calculated results are shown in Fig.2-6. From Fig.2-6, the proposed slot pattern ground has higher SWF than the conventional one, especially in high frequency band. Hence, the proposed slot pattern ground can reduce the balun size. In other word, with the same size of the balun, bandwidth of the balun using proposed slot pattern ground would be wider than the one using conventional slot pattern ground.

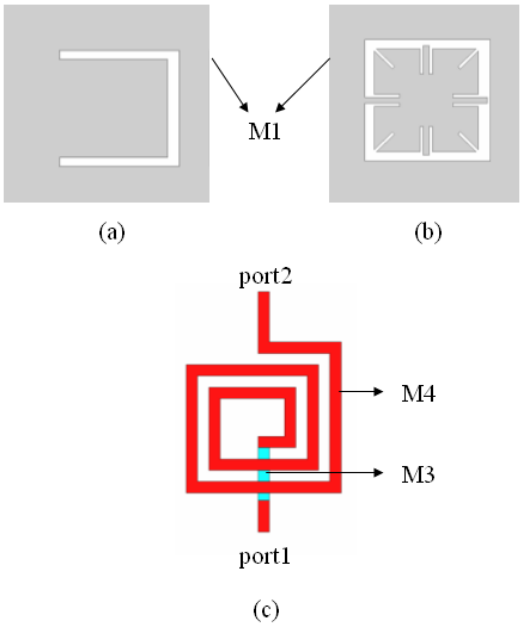

Fig.2-4 Conventional and proposed slot pattern ground (a) Conventional slot pattern ground (b) Proposed slot pattern ground (c) Spiral transmission line

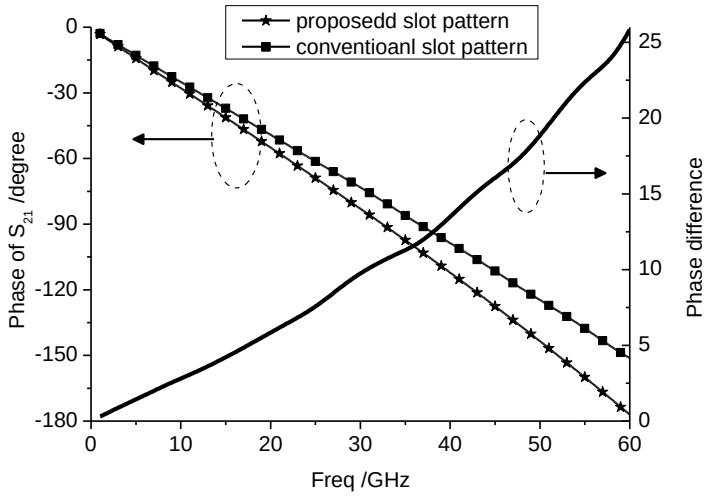

Fig.2-5 Phase of S_{21}

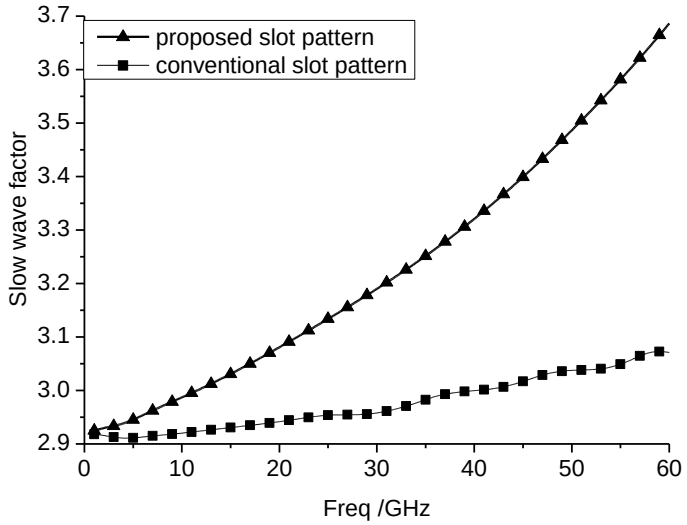

Fig.2-6 Slow wave factor of the conventional and proposed slot pattern ground

2.4.3 Proposed balun design

In the Fig. 2-2, the imbalance performance can be quantified by equation 2-6 [28]. Z_{0e} and Z_{0o} are the even- and odd-mode impedance per unit length of the coupled line, respectively. Equation 2-6 indicates that the imbalance performance of balun is dominated by the ratio of the even- and odd-mode impedance. A large impedance ratio between the even- and odd-mode impedance of the coupled lines is required. Equation 2-7 shows the impedance ratio between the even- and odd-mode impedance of the coupled lines [29]. L_e, L_o, C_e and C_o are the even- and odd-mode inductances or capacitances per unit length of the coupled lines. Hence, the balun performance has a relationship with these four parameters and optimization of these four parameters can obtain high balun imbalance performance.

$$\frac{S_{31}}{S_{21}} = -\frac{Z_{0e}-Z_{0o}}{Z_{0e}+Z_{0o}} \tag{2-6}$$

$$\frac{Z_{0e}}{Z_{0o}} = \sqrt{\frac{L_e \times C_o}{L_o \times C_e}} \tag{2-7}$$

The proposed balun is designed using the top metal of 3-μm thickness and simulated by Ansoft HFSS. The structure of the proposed balun is illustrated in Fig.2-8. From Fig.2-8, the balun consists of a pair of coupled spiral inductors and the proposed slot pattern ground structure under the spiral inductors. The line width of 6-μm is selected for balun size reduction and capacitance decreasing. The line space of the balun is 3-μm for high coupling effect. High coupling effect also increases the capacitance C_o between the coupled lines. The inner dimension is optimized to reduce the insertion loss and amplitude imbalance. The optimized slot in Fig.2-8 delays the even-mode signal and shorts the odd-mode signal from the point view of signal [29]. Therefore, the inductance of even-mode is increased and the one of odd-mode is independent on slot. According to the analysis before, the balun can be expected to obtain good imbalance performance with wide bandwidth owing to high impedance ratio between even- and odd-mode impedance.

Port1 is the unbalanced port and ports 2, 3 are the balanced ports. The length (L) of the balun is 278-μm and the width (W) of the balun is 120-μm shown in Fig.2-8 (c).

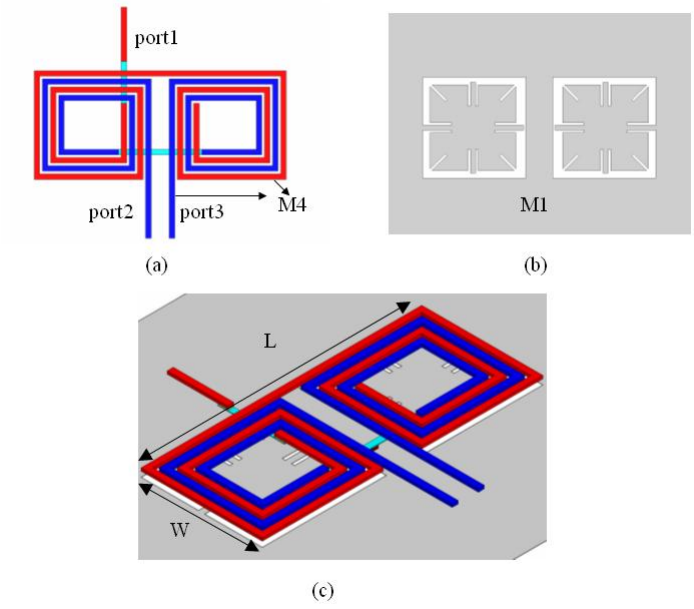

Fig.2-8 Marchand balun using proposed slot pattern ground (a) coupling line of the balun (b) proposed slot pattern ground (c) 3-D view of the balun

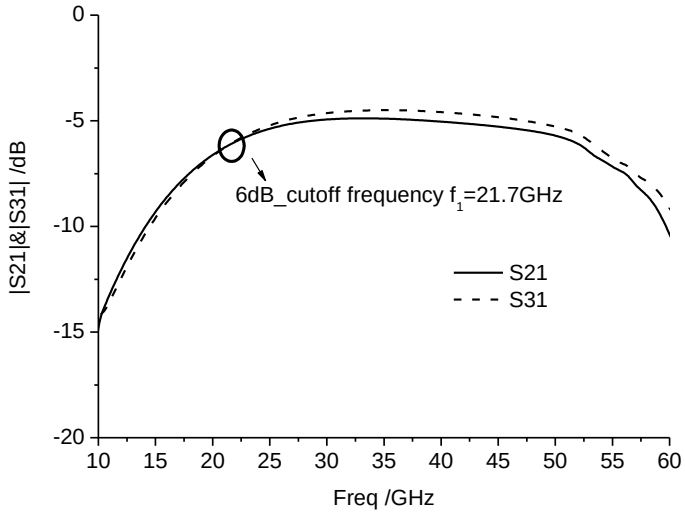

Fig.2-9 Insertion loss of proposed the balun

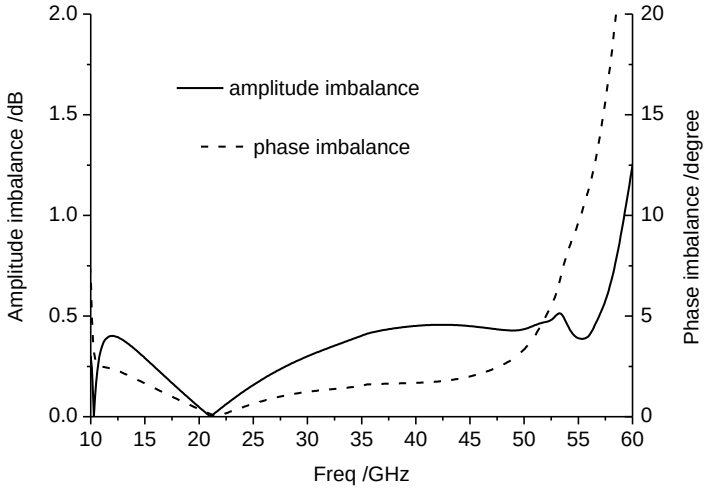

Fig.2-10 Imbalance performance of the proposed balun

The simulated results are shown in Figs.2-9 and 2-10. In the Fig.2-9, the insertion loss of the proposed balun is described where the 6-dB cut-off frequency (f1) is 21.7GHz. In the terms of the imbalance performance shown in Fig.2-10, the amplitude imbalance is less than 1dB from 10 GHz to 59.3GHz. The phase imbalance is less than 10° in the band of 10-55.5GHz.

As mentioned in section 2.4.1, the proposed slot pattern can reduce the balun size. In order to fairly compare with the performance of the proposed balun, the balun using conventional slot pattern ground is also designed shown in Fig.2-11. The length and width of the conventional balun are the same with the proposed balun. The performances of the conventional balun are shown in Figs.2-12 and 2-13. In the Fig.2-12, the insertion loss of the conventional balun is described where the 6-dB cut-off frequency (f1) is 27.1GHz. In the terms of the imbalance performance shown in Fig.2-13, the amplitude imbalance is less than 1dB from 13.5GHz to 60GHz. The phase imbalance is less than 10° in the band of 10-58.8GHz.

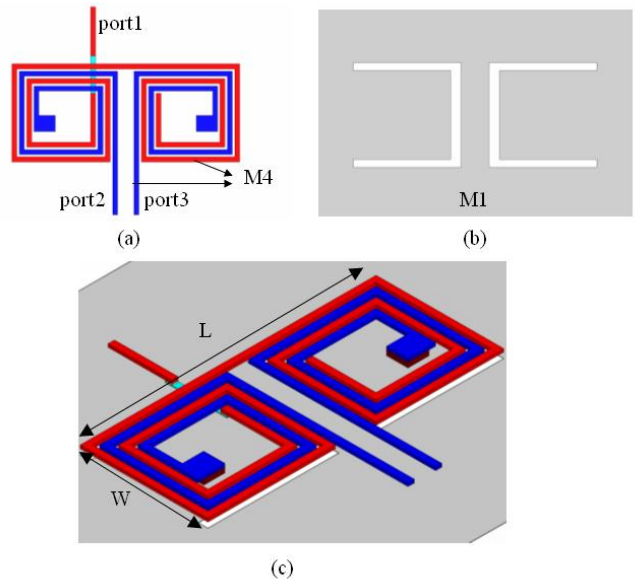

Fig.2-11 Marchand balun using conventional slot pattern ground (a) coupling line of the balun (b) conventional slot pattern ground (c) 3-D view of the balun

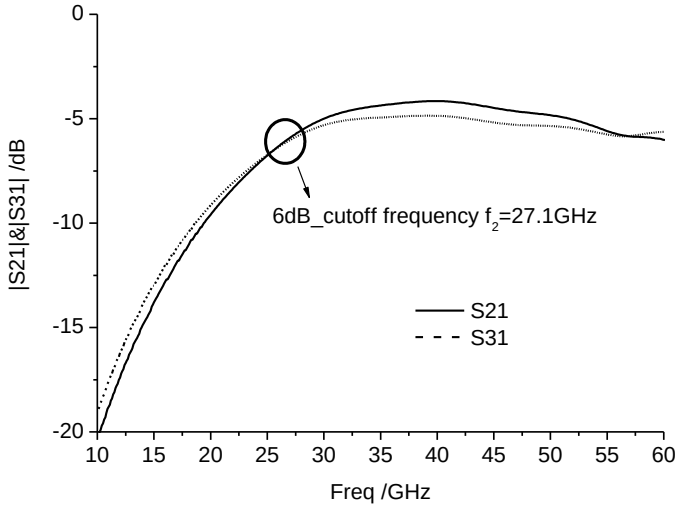

Fig.2-12 Insertion loss of the conventional balun

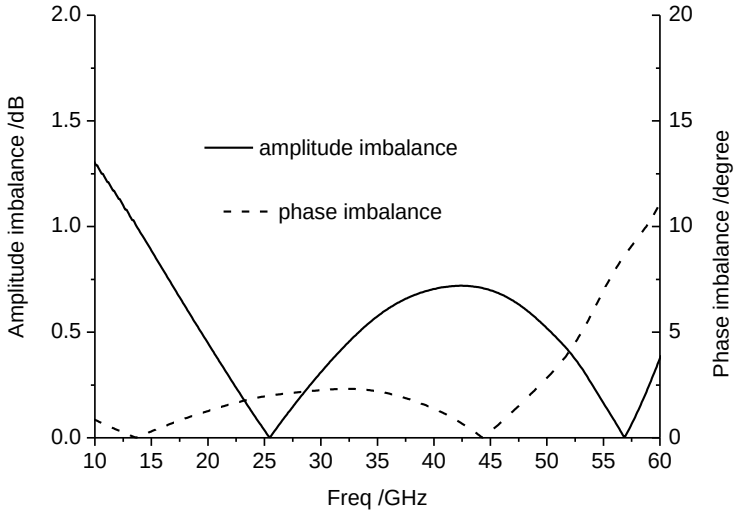

Fig.2-13 Imbalance performance of the conventional balun

The simulated performance comparison of the proposed and conventional balun is listed in TABLE 2-4. From this table, the proposed balun shows the comparable minimum insertion loss and bandwidth of imbalance with the conventional balun. However, the 6-dB cut-off frequency of the proposed balun is extended as expect. This extended frequency achieves 5.4 GHz compared with the conventional balun.

TABLE 2-4

Comparison of simulated results between the proposed and conventional balun

	6-dB cut-off frequency/GHz	Insertion loss/dB[a]	Bandwidth of Imbalance/GHz[b]
Conventional balun	27.1	1.5	13.5-58.8
Proposed balun	21.7	1.6	10-55.5

a: Minimum average insertion loss excluding 3dB balun loss

b: Bandwidth of imbalance at 1dB of amplitude imbalance and 10° of phase imbalance

2.5 Measurements and performance comparison

The proposed and conventional baluns are implemented in 0.25-μm SiGe BiCMOS shown in Figs.2-14 and 2-15. The core sizes of the fabricated baluns are 0.03mm^2. The layout of the center signal pad should be as small as possible (50μm×50μm) with a pitch of 150-μm. The baluns are measured on wafer using 50 Ω system. The ground-signal-ground-signal-ground (GSGSG) RF probe is used to measure the imbalance performance. In the ground of conventional balun, many slits are inserted to meet the requirement of design rule.

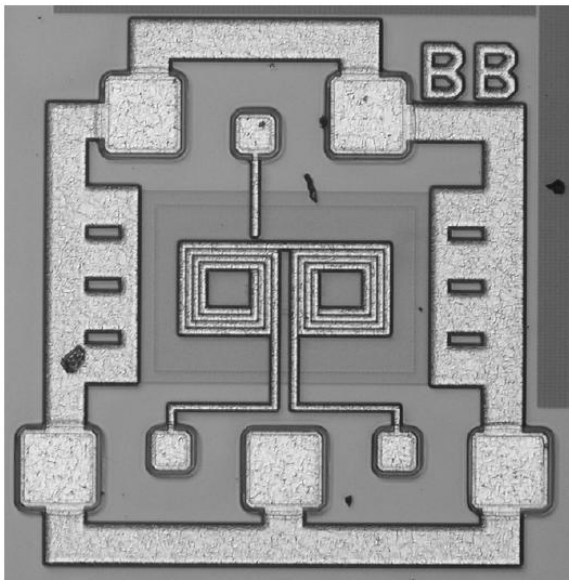

Fig.2-14 Microphotograph of the proposed balun

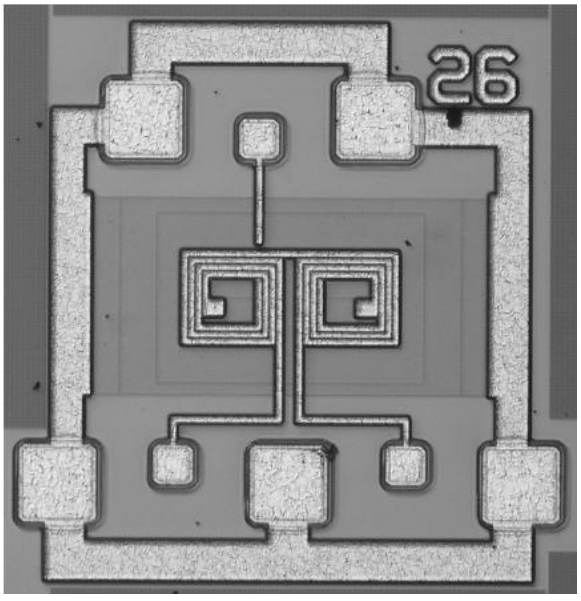

Fig.2-15 Microphotograph of the conventional balun

2.5.1 Measured results

The measured insertion losses are demonstrated in Fig.2-16. From the Fig.2-16, the minimum insertion loss of the proposed balun is 1.5dB. The 6-dB cut-off frequency of the proposed balun is 21.7GHz which agrees with the simulated results. The bandwidth of 6-dB insertion loss (including 3-dB balun loss) in the proposed balun is from 21.7GHz to 50GHz. From 35GHz, the insertion loss of the conventional balun is the same with the proposed one. However, at the low band, the insertion loss of the proposed balun is smaller than the conventional one. The conventional balun shifts the 6-dB cut-off frequency by 1.2GHz because the inserted slits mentioned above under the signal line introduce extra loss. The 6-dB cut-off frequency of the proposed balun is extended by 6.6GHz compared with the conventional one, which indicates the proposed slot pattern ground can improve insertion loss and result in wide band balun operation.

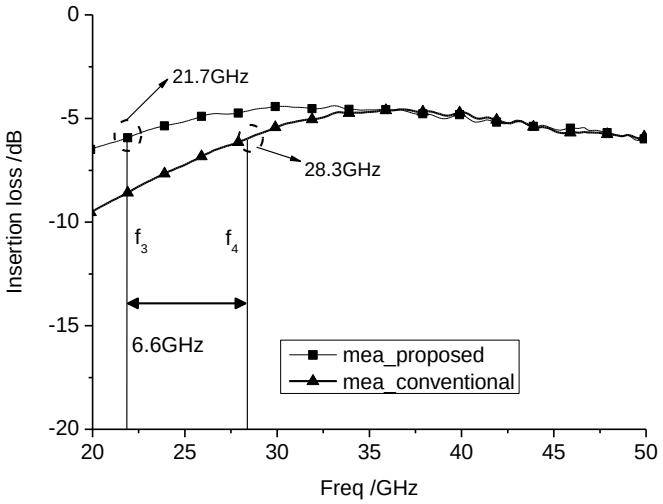

Fig.2-16 Measured insertion loss of the proposed and conventional baluns

The measured imbalance performances are shown in Figs. 2-17 and 2-18. In the Fig.2-17, the proposed balun has less than 1dB of amplitude imbalance from 20GHz to 57GHz. In the terms of the conventional balun, the amplitude imbalance is increased at high band from 47GHz. On

the other hand, the phase imbalance of the proposed balun is less than 10° in the band of 10-50GHz.

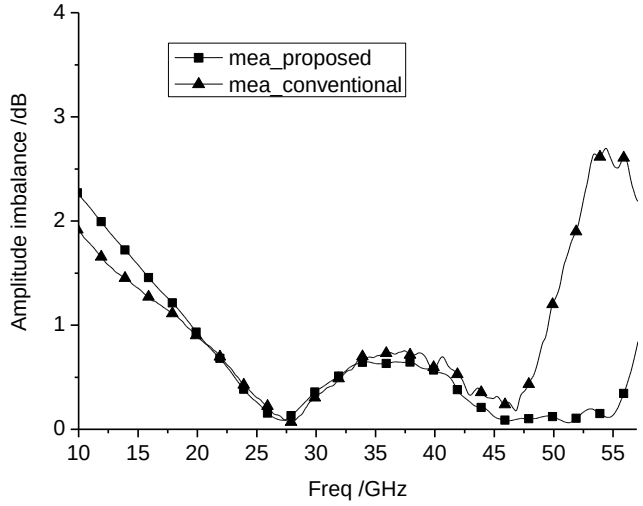

Fig.2-17 Measured amplitude imbalance of the proposed and conventional baluns

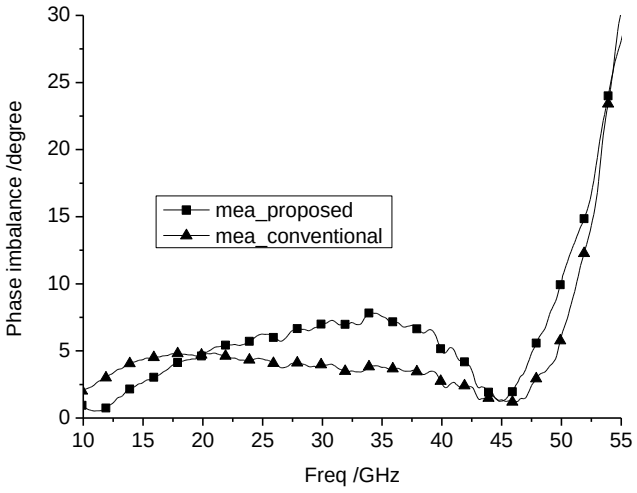

Fig.2-18 Measured phase imbalance of the proposed and conventional baluns

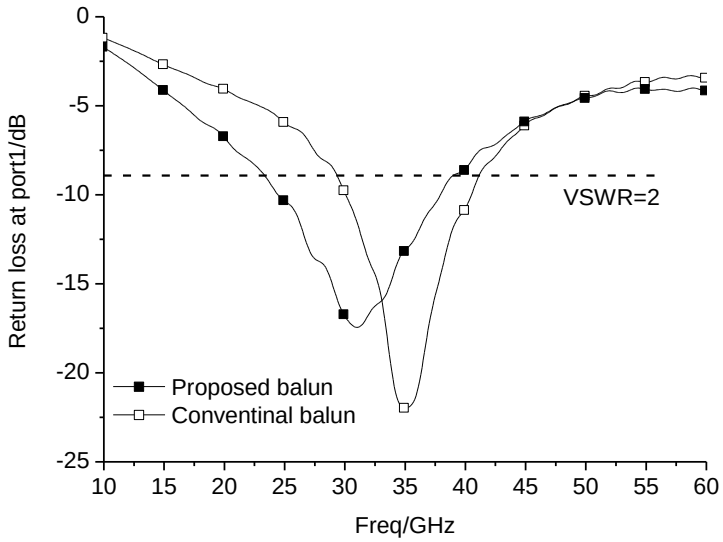

Fig.2-19 Measured return loss of the proposed and conventional baluns

TABLE2-5

Summary of measured results of the proposed balun

	Bandwidth of 3dB insertion loss[a] /GHz	Minimum insertion loss/dB[a]	Bandwidth of Imbalance/GHz[b]	Bandwidth of VSWR<2
Proposed balun	21.7-50	1.5	20-50	23.4-39.1
Conventional balun	28.3-50	1.5	20-50	29.4-41.2

a: Minimum average insertion loss excluding 3dB balun loss

b: Bandwidth of imbalance at 1dB of amplitude imbalance and 10° of phase imbalance

The measured return loss is described in Fig.2-19. From Fig.2-19, although the minimum return loss of the conventional balun is less than the one of the proposed balun, the bandwidth of the proposed balun which VSWR is 2 is wider than the one of the conventional balun.

The summary of the measured proposed and conventional balun is listed in TABLE 2-5. From this table, the performance of the proposed balun satisfies the design goal coving the

quasi-millimeter-wave UWB. Moreover, the band of VSWR less than 2 is available for UWB band. The band of imbalance performance and the band of 3-dB insertion loss are in the same band, which shows the proposed balun can be effectively applied.

2.5.2 Performance comparison

In order to compare the performance of the proposed balun with previous works, TABLE 2-6 gives the performance comparison with other works and Fig.2-20 shows balun size and band-width performance. Compared with the conventional balun, the proposed balun exhibits wider bandwidth with the same size . From this figure, it is can be seen that this work has small size and wide bandwidth. Hence this work could be used in quasi-millimeter-wave and millime-ter-wave applications such as mixers, doublers, low noise amplifiers and power amplifiers.

TABLE2-6

Performance comparison with other works

Reference	Size/mm^2	Operation band[a]
This work	0.03	78.9%
Conventional balun	0.03	55.4%
[13]	0.35	41.6%
[17]	0.05	50%
[21]	0.12	67%

a: Operation band denotes the frequency band of imbalance less than 1dB/10° and insertion loss less than 3dB.

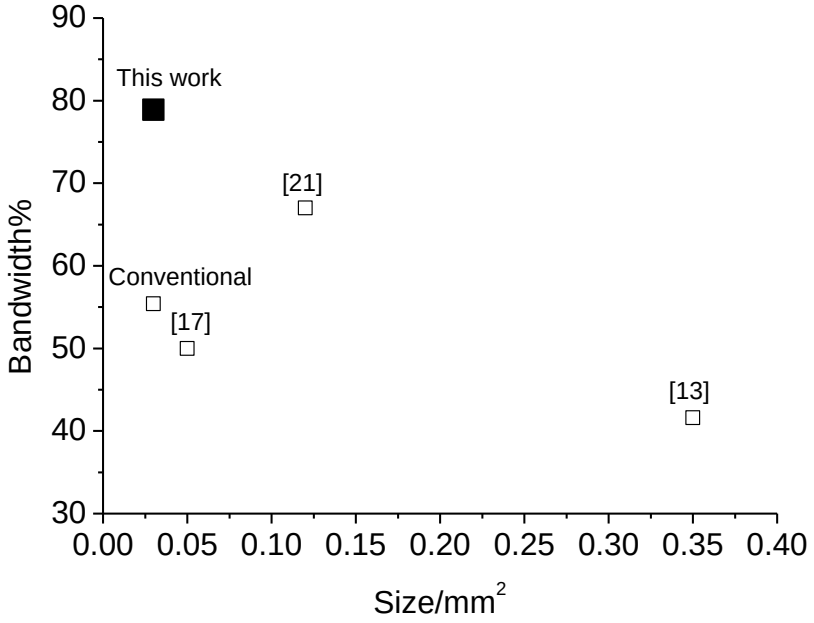

Fig.2-20 Size and bandwidth comparison with previous millimeter-wave band balun

2.6 Conclusion

In this chapter, a compact broadband Marchand balun for millimeter-wave applications is proposed. The proposed balun is implemented in 0.25-μm SiGe BiCMOS and measured on wafer.

In order to design compact broadband balun, a novel slot pattern ground structure is proposed and designed. This novel slot pattern ground structure has high SWF to reduce balun size. To obtain wide bandwidth imbalance performance, even- and odd-mode concept is used to design and optimize the spiral transmission line. The optimized even- and odd-mode impedances result in high ratio of even-mode impedance with respect to odd-mode impedance.

Due to utilization of these techniques, this work achieves 1dB of amplitude imbalance and 10° of phase imbalance in the band of 20GHz-50GHz. In this band, the minimum insertion loss is 1.5dB. The bandwidth of 3dB insertion loss is from 2.7GHz to 50GHz. The VSWR which is less than 2 is from 23.4GHz to 39.1GHz. The chip core size is only 0.03mm^2. Compared with

the balun using the conventional slot pattern ground structure, the 6-dB cuf-off frequency is extended by 6.6GHz. It indicates that the proposed slot pattern ground structure is effective to improve insertion loss of balun in low band.

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Chapter 3 Broadband Frequency Doubler IC for Wireless Communications

3.1 Introduction

In the Chapter 2, broadband compact baluns are implemented and measured on-wafer. The broadband performance was verified according to the measured results. A broadband frequency doubler based on Gilbert cell integrated input and output baluns for wireless communication applications is proposed in this chapter.

In 2002, the Federal Communication Commission announced the allocation of ultra-wideband spectrum in certain frequency bands. The UWB spectrum between 0 and 960MHz is used for ground penetrating radar (GPRs) and through wall imaging systems. The UWB frequency spectrum between 3.1 and 10.6GHz is allocated for the communication systems. The UWB frequency spectrum between 22GHz and 29GHz is used for vehicular short range radar (V-SRR) systems [1]. The advantages of UWB systems include low power consumption, simple receiver architecture, and higher range resolution. UWB can be used for short range vehicular radar systems, which are used for anti-collision sensing, adaptive cruise control (ACC) support, blind spot detection, and parking aid [2][3][4]. So far, about 60 countries allow the V-SRR applications. However, the available frequency band is slightly difference shown in Fig.3-1. In the USA, this configuration has a drawback of necessitating strict control of the output spectrum to avoid emission at the frequency in the forbidden band (23.6-24.0GHz), very

close to the ISM band, which is saved for radio astronomy and for satellite remote sensing. The EU allows the frequency band of 22-26.65GHz for the V-SRR [5]. From 2007, Japan began to investigate and introduce the V-SRR application at the band of 22-29GHz. The band of 22-24.25GHz is conditionally utilized because there are some application in this band such as radio astronomy applications. Hence, the 26-GHz band (24.25-29GHz) is unlicensed and for a long-range use [6].

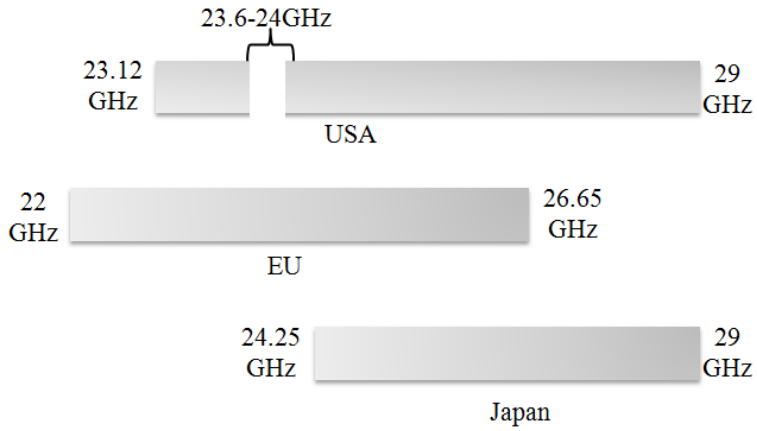

Fig.3-1 Frequency band allocations for V-SRR systems in USA, EU and Japan.

The broadband V-SRR systems is necessary to cover the band of 22-29GHz meeting the frequency band of requirements of the USA, EU and Japan. As mentioned in chapter 1, frequency doubler is key component composing of the V-SRR systems. Hence, the performance of broadband V-SRR systems depends on the broadband frequency doubler.

This chapter is organized as follows. Broadband frequency doubler circuit review followed this part is shown in section 3.2, and section 3.3 presents a 0.25-μm SOI SiGe BiCMOS technology employed in this work. section 3.4 describes frequency doubler design. From section 3.5, measured results and discussions are demonstrated. Finally, section 3.6 gives a conclusion of this chapter.

3.2 Broadband doubler circuit review

As mentioned above, broadband operation of frequency doubler is of importance to meet different requirements. Hence, broadband frequency doublers are reviewed from this section. So far, there are two type broadband frequency doubler adopted by researchers. One is passive frequency doubler which uses diodes [7]. Another is active frequency doubler which is utilization of frequency multiplication and nonlinearity of transistors [8][9].

3.2.1 Passive frequency doubler

Passive frequency doubler usually consists of wideband balun and a pair of antiparallel diodes. The input power are divided into two parts to feed two antiparallel diodes. Due to the diodes being antiparallel, the generated second-harmonic signals are 180° out-of-phase. The second-harmonic signals are combined through the balun at the output. The passive frequency doubler using balun and antiparallel diodes can achieve high bandwidth [10][11]. However, they suffer greatly from the conversion loss (typically from -12 to -15dB) caused by the large series resistance. Larger size diodes can be used to improve the performance, however, at the expense of the parasitic capacitance, which limits the high frequency response. The availability of broadband baluns is also necessary to provide fully differential operation across the bandwidth. Moreover, the passive frequency doubler usually needs high input power as high as 14dBm in [12]. The high input power is difficult to be obtained by the oscillator in low DC power IC solution. Hence, the passive frequency doubler is not applicable for high integration los DC power IC solution.

3.2.2 Active frequency doubler

So far, many researchers use state-of-the-art technology to improve performance of active frequency doubler such as InGaP-based doublers [13][14], GaAs-based doublers [15]-[18], SiGe-based doublers [19][20] and CMOS-based doublers [21][22].

Active differential/single-ended frequency doubler usually adopts the nonlinear characteristics of the transistor which generates second harmonic frequency at the output. The differential doubler usually utilize push-push circuit to cancel fundamental frequency while the single-ended douler use input/output reflector to improve fundamental frequency suppression [23][24]. Frequency doubler achieving broadband operation always needs input/output imped-

ance matching network, The input/output impedance matching networks are composed of several series capacitor and inductors. The fundamental frequency suppression and conversion gain frequently depend on the performance of the inductors. In the high frequency band, Q value of the inductor is difficult to achieve high value using Si-based process [25]. Hence, the inductor performance limits the broadband operation and degrades the fundamental frequency suppression.

Another broadband frequency doubler is based-on Gilbert cell which uses the frequency multiplication. Owing to the differential operation of the Gilbert cell, a balanced broadband matching circuit at the input is necessary such as power splitter cascading Cherry–Hooper topology [26][27] and input doubler emitter followers [28]. The power splitter and input doubler emitter followers result in broadband operation for frequency doublers. However, they are active circuits and the DC power consumption of the frequency doublers is increased.

3.3 0.25-μm SOI SiGe BiCMOS technology

SiGe BiCMOS has become a dominant technology for radio frequency circuit implementation partly due to steep performance gains which have enabled products with lower power consumption, smaller form factors, and higher functional integration [29]. Also contributing to the popularity of SiGe BiCMOS is the fact that common radio architectures are well suited to implementation in a combination of bipolar and CMOS devices, as well as the fact that SiGe BiCMOS is available today from a variety of sources making it easily accessible and affordable.

A 0.25-μm SiGe BiCMOS technology that includes four metal layers (3-μm thickness of the top layer) and four poly (MOS gate, poly resistor, double-poly self-aligned SiGe HBT) is performed on an silicon on insulator (SOI) shown in Fig.2-3. The substrate resistivity is several tens Ω·cm. Metal insulator metal (MIM) capacitor is performed between the first metal layer and the second metal layer. Devices can be completely isolated by the buried SiO_2 layer and shallow/deep trench isolations to realize latch-up free structure. These devices and metallization are fabricated on a 200-mm wafer line.

An typical cross-sectional view of SiGe HBT is shown in Fig.3-2 [30]. The typical specifications of 0.25-μm SiGe HBT used in this thesis is listed in TABLE 3-1. The cutoff frequency (f_t)

and the maximum oscillation frequency (f_{max}) are 137 GHz and 180GHz, respectively. Hence, these results indicate that the SiGe HBTs are very suitable for millimeter-wave applications.

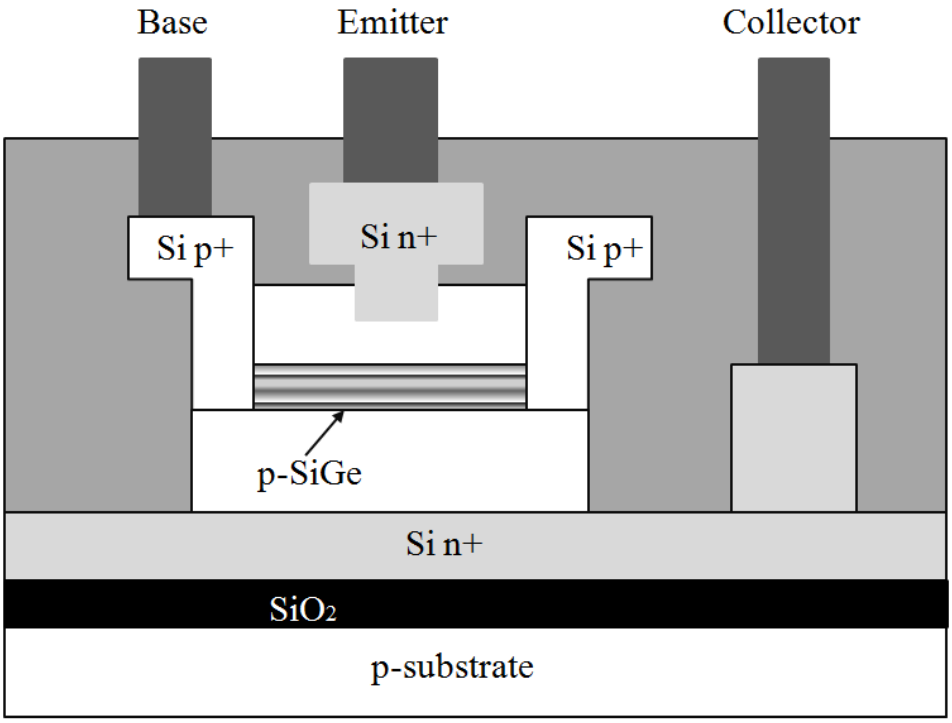

Fig.3-2 An typical cross-sectional view of SiGe HBT [30].

TABLE 3-1

Typical specifications of SiGe HBT(25°)

B_{cbo}	B_{ceo}	f_t	f_{max}	Emitter size
6.5V	2.0V	137GHz	180GHz	$0.2\times1\mu m^2$

3.4 Broadband frequency doubler design

From this section, a Gilbert cell based frequency doubler is to be designed. In this section, designed goal is given firstly, then the components composing of frequency doubler are designed

respectively. At the last, the simulated results of the frequency doubler are given. The block diagram of the proposed frequency doubler is shown in Fig.3-3.

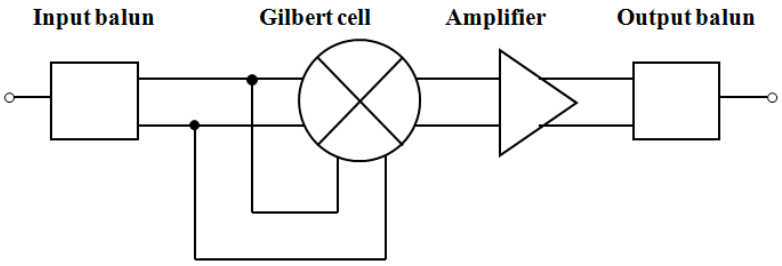

Fig.3-3 The block diagram of frequency doubler

3.4.1 Design goal

As it is well known, specifications of frequency doubler strongly depends on a target application system. Typically, a frequency doubler is applied in a quasi-millimeter-wave UWB radar sensor system. In this application, the equivalent isotropic radiated power (EIRP) in the available band is -41.3dBm/MHz while the one is less than -61.3dBm/MHz out of the available band shown in TABLE 3-2 [31]. Hence, the ratio of EIRP in band with respect to the one out of band is 20dBc.

TABLE 3-2

EIRP for V-SRR in the USA, EU and Japan

	USA	EU	Japan
Available band/GHz	23.12-23.6 and 24-29	22-26.65	24.25-29
EIRP in band	-41.3dBm/MHz	-41.3dBm/MHz	-41.3dBm/MHz
EIRP out of band	-61.3dBm/MHz	-61.3dBm/MHz	-61.3dBm/MHz

TABLE 3-3

Design goal of frequency doubler

Items	Specifications
Bandwidth	22-29GHz
Input power	≤ 0dBm
Output power	≥ -10dBm
Suppression ratio (f_0)	≥ 30dBc
Suppression($3f_0$)	≥ 20dBc
VSWR	≤ 2.5
DC power consumption	< 80mW

The design target of the frequency doubler is listed in TABLE 3-3.

Gilbert cell is adopted for frequency multiplication in the broadband frequency doubler with high fundamental frequency suppression. High fundamental frequency suppression can alleviate the influence of fundamental frequency to subsequent stage of doubler, for example, power amplifier in FMCW radar frontend [32]. Since the frequency doubler is a differential and broadband operation circuit, broadband baluns splitting into differential power in the input and combining differential power in the output are indispensable components. The input and output baluns provide single-ended ports to test the frequency doubler. In order to obtain a certain conversion gain, an output differential amplifier is essential to achieve this goal.

3.4.2 Balun design

As mentioned in chapter 2, a passive Marchand balun is chosen for this design due to better amplitude balance and phase balance than active one. Both input balun and output balun are designed using the top metal of 3-μm thickness and simulated by Ansoft HFSS. Both baluns are the same structure but different turns and different sizes to meet the input and output frequency bands. The structure of the output balun is illustrated in Fig.2-11. The simulated imbalance performances of input balun and output balun are depicted in Figs.3-4 and 3-5, respectively. Fig.3-4 shows that the amplitude imbalance is less than 0.5dB and the phase imbalance is less than 2° from 10GHz to 20GHz. The imbalance performance of the output balun is that the amplitude imbalance is less than 0.5dB and the phase imbalance is less than 2.5° from 20GHz to 30GHz, as shown in Fig.3-5.

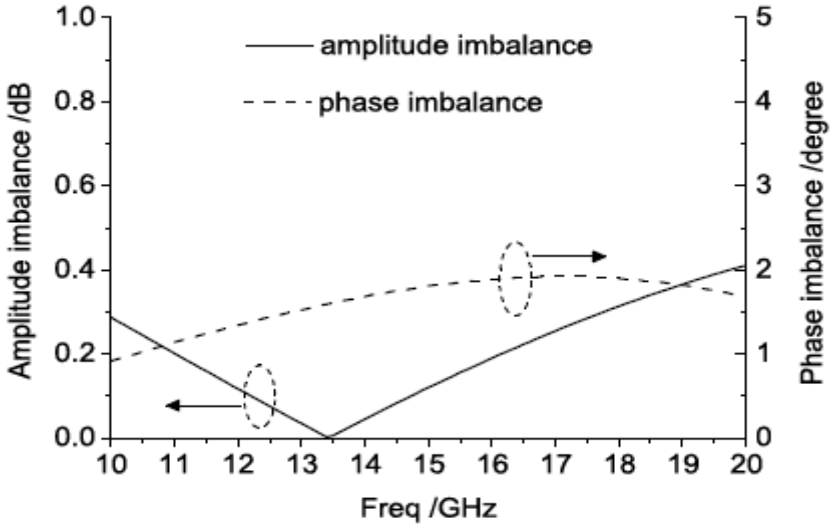

Fig.3-4 Simulated imbalance performance of input balun

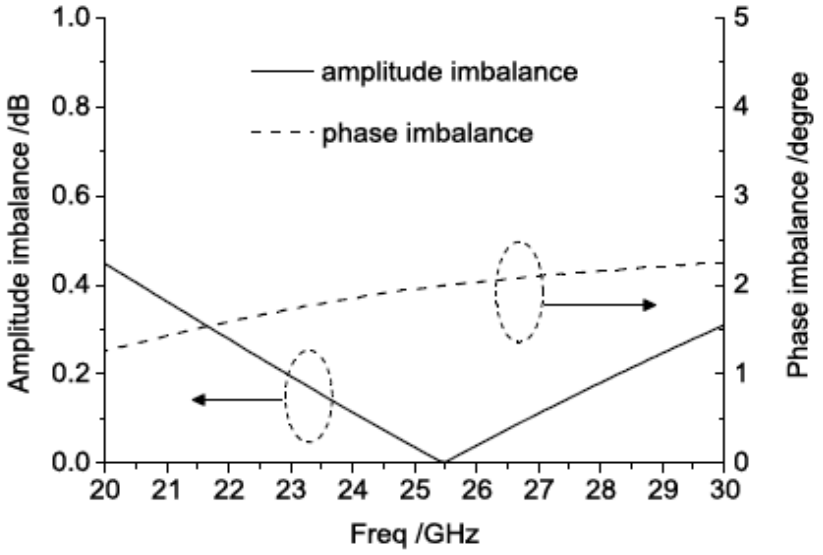

Fig.3-5 Simulated imbalance performance of output balun

3.4.3 Doubler core design concept

The Gilbert cell is widely used to implement frequency mixers and variable gain amplifiers shown in Fig.3-6. The operation principle of the Gilbert cell doubling the fundamental frequency f_0 is explained by the equations 3-1, 3-2 and 3-3 [33]. ΔI_{out} indicates differential output of frequency doubler, I_{EE} is the bias current and V_T is the thermal voltage. The DC term in the equations 3-1, 3-2 and 3-3 is omitted.

$$\Delta I_{out} = I_{EE}\left[tanh\left(\frac{V_{RF}(f_0)}{2V_T}\right)\right]\left[tanh\left(\frac{V_{LO}(f_0)}{2V_T}\right)\right] \approx \frac{I_{EE}}{2V_T^2} \times A^2 \times cos(2\omega_0 t) \quad (3\text{-}1)$$

where

$$V_{LO}(f_0) = V_{RF}(f_0) = 2A\,cos(2\pi f_0 t) = 2Acos(\omega_0 t) \quad (3\text{-}2)$$

$$V_{RF}{}^{+}(f_0) = V_{LO}{}^{+}(f_0) = Acos(2\pi f_0),\ V_{RF}{}^{-}(f_0) = V_{LO}{}^{-}(f_0) = -Acos(2\pi f_0) \quad (3\text{-}3)$$

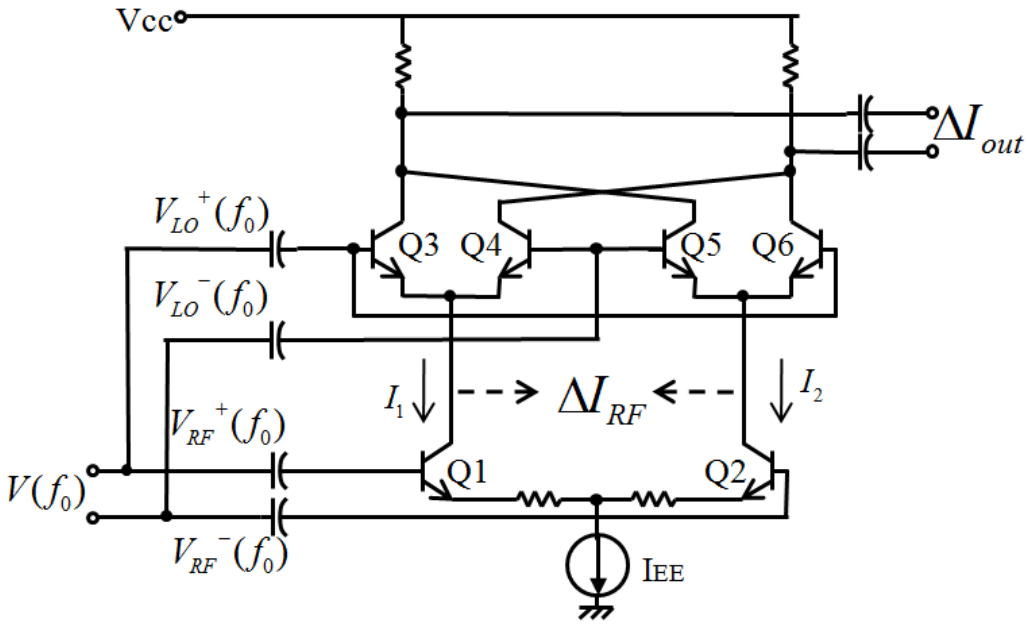

Fig.3-6 Conventional Gilbert cell for the frequency doubler core.

The transistors of Q1-Q2 are biased closed to class A and the transistors of Q3-Q6 are biased near class B. The degeneration resistance R1 (10Ω)and R2 (10Ω) are used to improve the linearity of the transistors of Q1 and Q2. However, the improvement of linearity is limited. Since the transistors of Q1 and Q2 have nonlinear characteristics, the outputs of Q1and Q2 indicate not only fundamental frequency f_0 but also second harmonic frequency $2f_0$ and third harmonic frequency $3f_0$. If the input signal of doubler core has no imbalance and the devices in doubler core are matched well, the output of core is only second harmonic and no fundamental frequency component as shown in Fig.3-7(a).

$$V_{RF}{}^{+}(f_0) = Acos(2\pi f_0) \tag{3-4}$$

$$V_{RF}{}^{-}(f_0) = -Aacos(2\pi f_0 + \varphi) \tag{3-5}$$

$$\begin{aligned}\Delta I_{RF} &= I_1 - I_2 \\ &= g_m A[cos(\omega_0 t) + acos(\omega_0 t + \varphi)] + \frac{g'_m A^2}{2}[cos(2\omega_0 t) - a^2 cos(2\omega_0 t + 2\varphi)]\end{aligned} \tag{3-6}$$

However, the input signal is imbalanced defined in equations 3-4 and 3-5, where a and φ denote the amplitude and phase imbalance, respectively. Assume that all devices are matched well. The current of ΔI_{RF} is given in equation 3-6. From this equation, the output current of Q1 and Q2 , ΔI_{RF} , includes the fundamental component and second harmonic component. Hence, the ΔI_{out} of the Gilbert cell is obtained in equation 3-7. The fundamental and third harmonic components is generated as expected.

$$\begin{aligned}\Delta I_{out} &= I_{EE} \times \Delta I_{RF} \times \left[tanh\left(\frac{V_{LO}(f_0)}{2V_T}\right)\right] = \frac{1}{2} g_m A^2 cos(2\omega_0 t) + \frac{1}{2} g_m A^2 a^2 cos(2\omega_0 t + 2\varphi) + \\ & g_m A^2 a\, cos(2\omega_0 t + \varphi) + \frac{1}{4} g'_m A^3 cos(\omega_0 t) + \frac{1}{4} g'_m A^3 acos(\omega_0 t - \varphi) - \\ & \frac{1}{4} g'_m A^3 a^2 cos(\omega_0 t + 2\varphi) - \frac{1}{4} g'_m A^3 a^3 cos(\omega_0 t + \varphi) + \\ & \frac{1}{4} g'_m A^3 cos(3\omega_0 t) + \frac{1}{4} g'_m A^3 a\, cos(3\omega_0 t + \varphi) - \frac{1}{4} g'_m A^3 a^2 cos(3\omega_0 t + 2\varphi) - \\ & \frac{1}{4} g'_m A^3 a^3 cos(3\omega_0 t + 3\varphi)\end{aligned} \tag{3-7}$$

According to the principle of the Gilbert cell doubling f_0, much attention should be paid to the

second harmonic frequency $2f_0$ of Q1 and Q2, because $2f_0$ of Q1 and Q2 can be mixed with f_0 of Q3-Q6, and then down-converted to f_0 and up-converted to $3f_0$ Hence, fundamental frequency and third harmonic frequency components appear in the output of the doubler core which is demonstrated in Fig.3-7(b). Therefore, to reduce the fundamental frequency and the third fundamental frequency at the output of Gilbert cell, the second harmonic frequency in the output of Q1 and Q2 should be as small as possible.

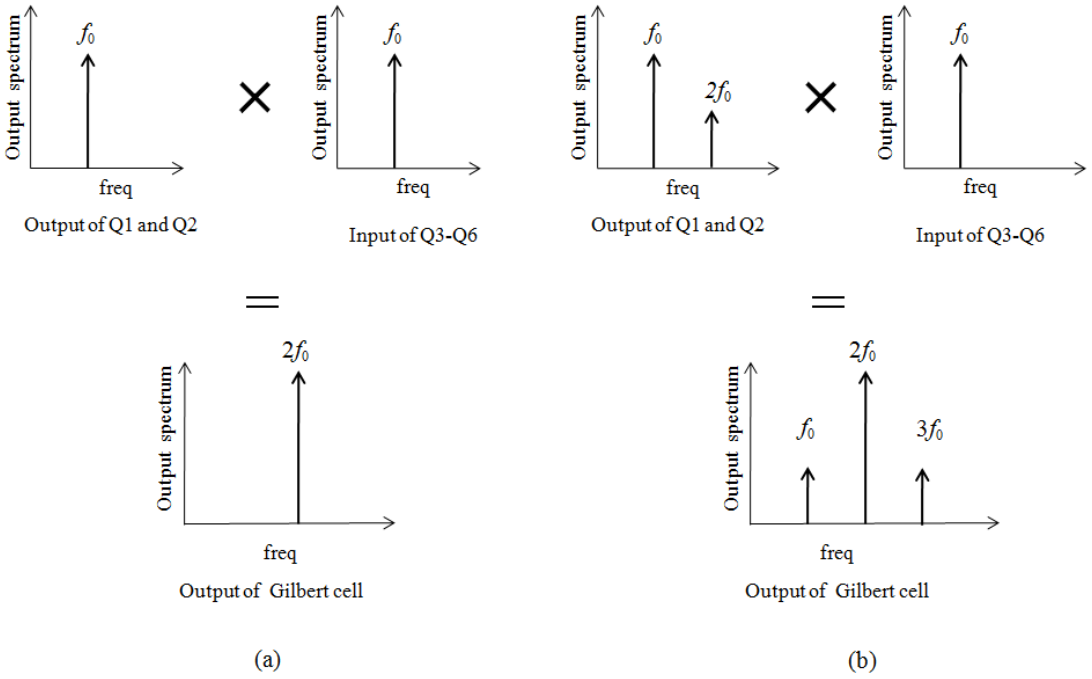

Fig.3-7 The frequency conversion in the Gilbert cell: (a) the ideal case , (b) the case with imbalance input signal and mismatched devices..

The design concept of this doubler core is to degrade the second harmonic frequency at the output of Q1and Q2 and the fundamental frequency at the output of Q1 and Q2 should not be changed, simultaneously. Hence, an low pass filter (LPF) could reduce the second harmonic frequency and pass the fundamental frequency. This design concept is shown in Fig.3-8 in which an LPF is inserted between the transistor of Q1 and switch quad transistors of Q3 and Q4. On the other hand, the output power from the input balun is divided equally to the transis-

tors of Q1-Q2 and Q3-Q6. However, the transistors of Q3-Q6 acting as transistor commutating switch need high power to switch well. Therefore, matching circuit is necessary to provide high power to the switch quad shown in Fig.3-9.

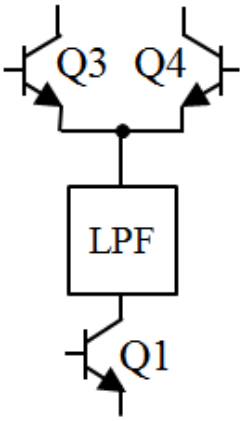

Fig.3-8 Design concept of suppress second harmonic frequency for the Q1.

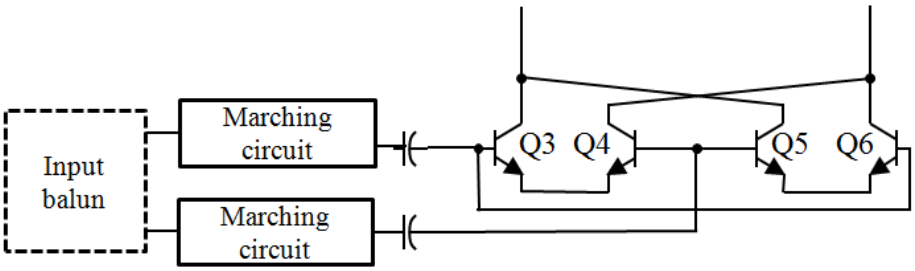

Fig.3-9 Design concept of impedance matching between the input balun and switch quad.

3.4.4 Gilbert cell design

As described before, $2f_0$ mainly comes from Q1 and Q2, therefore, a pair of novel internal low pass LC filters inserted in the outputs of Q1 and Q2 and emitters of switch quad is proposed in this work demonstrated in Fig.3-10. The supply voltage V_{cc} is 2.4V. The specifications of transistors and inductance and capacitance used in Gilbert cell are listed in TABLE 3-4. The cut-off

frequency and maximum oscillation frequency of transistors in Gilbert cell shown in TABLE 3-5 are 81.5 GHz/84.3GHz and 66GHz/79.5GHz for the Q1-Q2 and Q3-Q6, respectively.

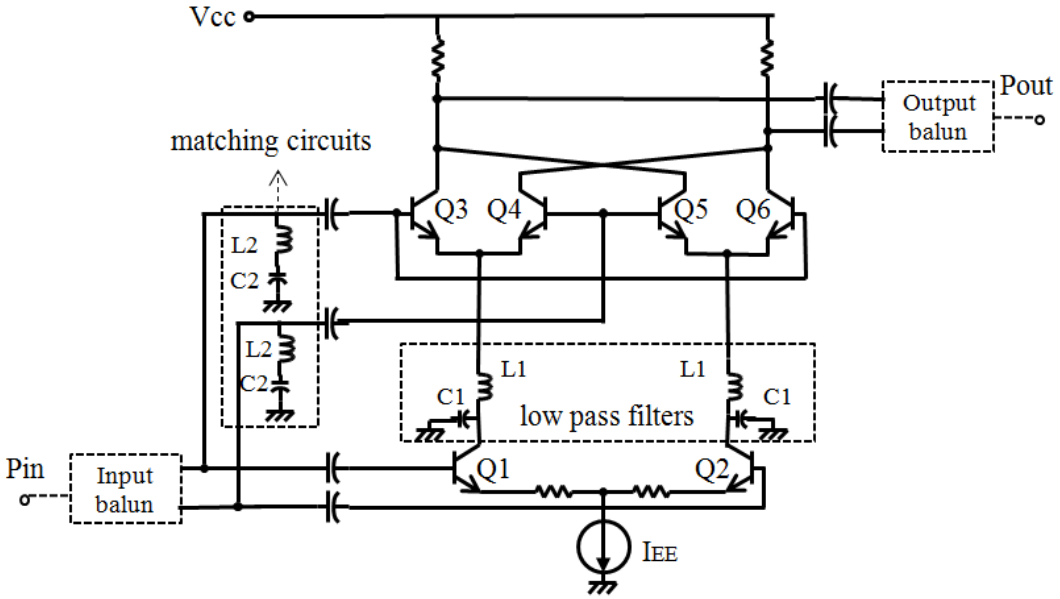

Fig.3-10 The proposed frequency doubler core circuit based on Gilbert cell.

TABLE 3-4

Specifications of transistors and inductance and capacitance in Gilbert cell

	Emitter size		Values
Q1-Q2	0.2μm×4μm	L1/L2	0.5nH/1nH
Q3-Q6	0.2μm×3μm	C1/C2	0.28pF/1pF

TABLE 3-5

Cut-off frequency and Maximum oscillation frequency of transistors in Gilbert cell

	Q1-Q2	Q3-Q6
f_t /f_{max}	81.5 GHz/84.3GHz	66 GHz/79.5GHz

Fig.3-11 shows simulated frequency response of suppression of the proposed Gilbert cell. The Gilbert cell is simulated with the input and output baluns shown in Fig.3-10. The solid line denotes the fundamental frequency suppression ratio of the proposed doubler core while the dashed one denotes the fundamental frequency suppression ratio of doubler core without LPF. From Fig.3-11 it is found that the frequency doubler core with internal low pass LC filter effectively improves the fundamental frequency suppression ratio at an input power of -1dBm.

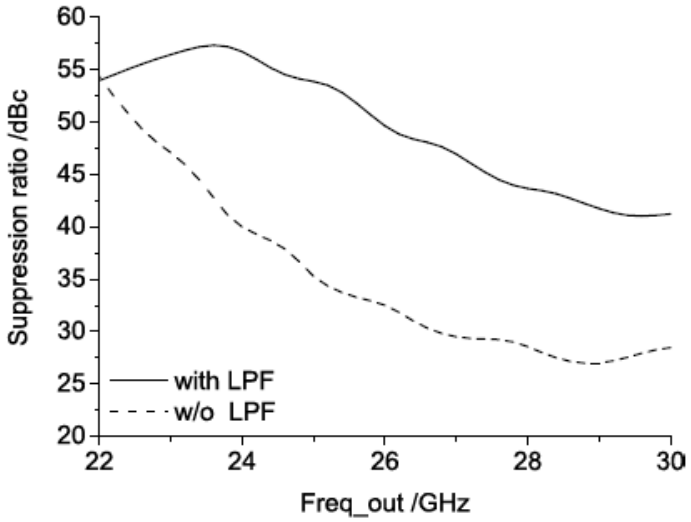

Fig.3-11 Frequency response of suppression of the frequency doubler cores.(solid line denotes the fundamental frequency suppression ratio of the proposed doubler core; dashed line denotes the fundamental frequency suppression ratio of doubler core without LPF)

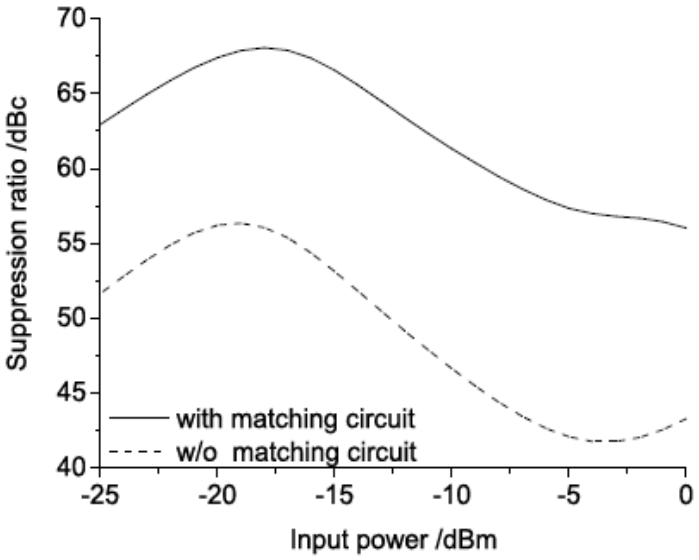

Fig.3-12 The effectiveness of matching circuits in low drive power at input frequency of 11.5GHz.

The power injecting into the switch quad of the Gilbert cell should be sufficient to switch well. As shown in Fig.3-10, a pair of matching circuits in parallel with the LO inputs is designed. In the operating frequency band, the matching circuits work as inductive circuits to match input balun and also boost the power to Q3-Q6 without increasing input power of doubler. Fig.3-12 depicts the suppression improving effectiveness of the matching circuit. In Fig.3-12, it is clearly shown that the doubler core with the matching circuit has much higher suppression in low input drive power from -25dBm to 0dBm at an input frequency of 11.5GHz.

Parasitic feedback of Q3-Q6 through the base-collector parasitic capacitor at the second harmonic frequency can deteriorate fundamental frequency suppression performance. Because the second harmonic frequency coming from the output of the Gilbert cell can be multiplied with fundamental frequency of LO inputs generating f_0 component in the output of doubler core. To alleviate the influence of parasitic feedback, small size transistors of Q3-Q6 are chosen in this design. Nevertheless, the f_t of transistor quad needs to be at least twice the maximum operating frequency to guarantee fast switching. In this design, f_t of transistor quad is 66GHz which is much larger than twice the maximum operating frequency. The emitter size of transistors of

Q3-Q6 describes in TABLE 3-4.

In this doubler core, to compensate the conversion loss of the Gilbert cell, an output amplifier is designed and cascaded with the Gilbert cell. Fig.3-13 shows the circuit schematic of the output amplifier. The supply voltage V_{cc_amp} of this amplifier is 3.3V. The f_t of transistors of Q7-Q10 are 123GHz. The specifications of transistors and inductance and in output amplifier is shown in TABLE 3-6. A cascode topology is adopted to improve the gain and a high-pass type LC circuit is designed to suppress the fundamental frequency signal. Fig.3-14 shows the small signal gain of the output amplifier with input/output baluns. From this figure, the high-pass effect is demonstrated.

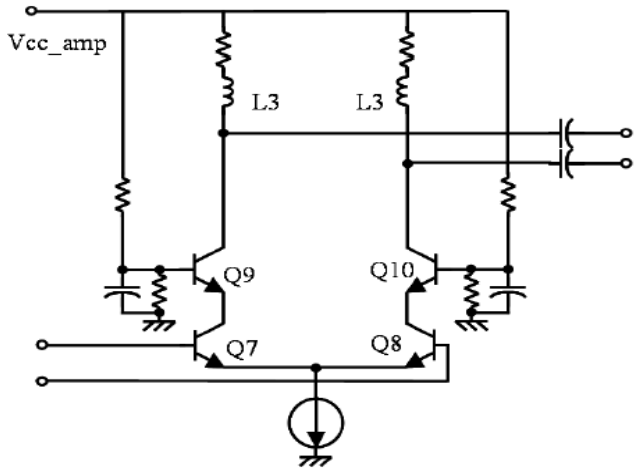

Fig.3-13 The topology of output amplifier.

TABLE 3-6

Specifications of transistors and inductance and in output amplifier

	Emitter size		Values
Q7-Q10	0.2μm×2μm×4figures	L3	1nH

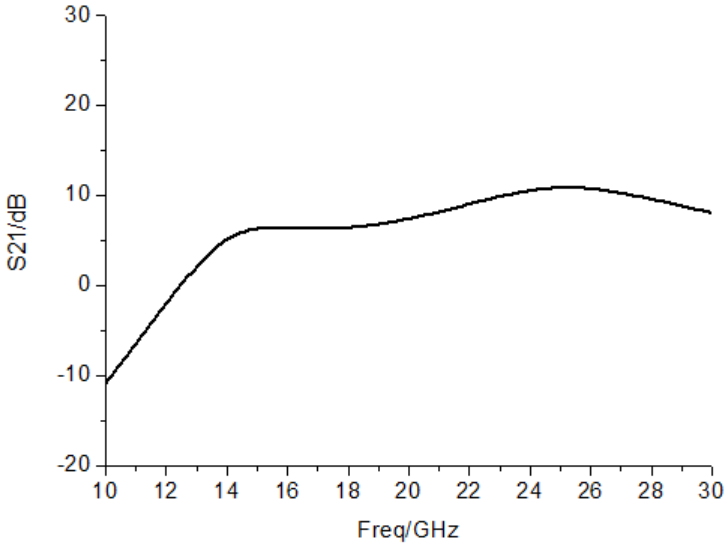

Fig.3-14 The simulated gain of output amplifier.

3.4.5 Simulated results

All components of the frequency doubler described in the previous sections are combined to realize a complete frequency doubler as shown in Fig.3-3. The frequency doubler is simulated by Agilent ADS with harmonic balance method. The output power of frequency doubler at 23 GHz is shown in Fig.3-15. From this figure, the output power of 23GHz from an input power of -6dBm is almost saturated. Fig.3-16 illustrates the suppression of the doubler when an input drive power is -1dBm. The fundamental frequency suppression in the Fig.3-16 has a smaller drop than the one shown in Fig.3-11. The impedances of differential ports of output balun are designed in 100Ω. On the other hand, the input impedance of output amplifier shows impedance of 25Ω. When simulating the suppressions in Figs.3-11 and 3-16, the load impedances of Gilbert cell are changed from 100Ω to 25Ω. Thus, simulated suppression ratio in Fig.3-16 is slightly degraded comparing with one in Fig.3-11. The conversion gain was also calculated and described in Fig. 3-16, showing better than -7.5dB.

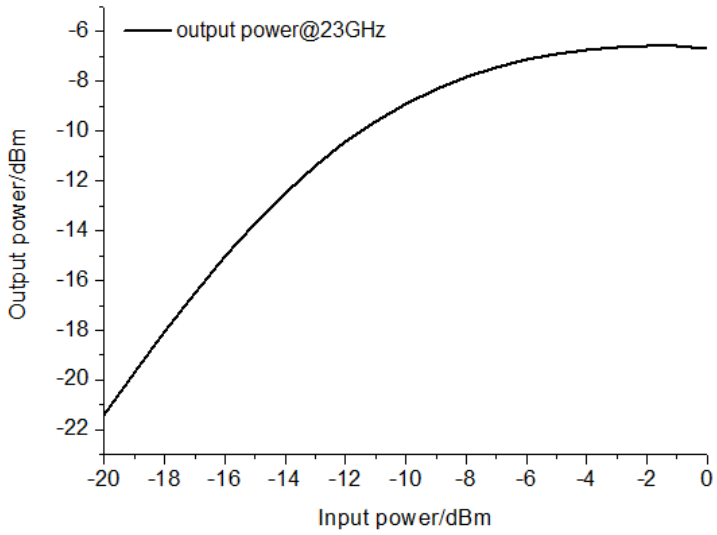

Fig.3-15 The simulated input-output performance of the proposed frequency doubler at an output frequency of 23GHz.

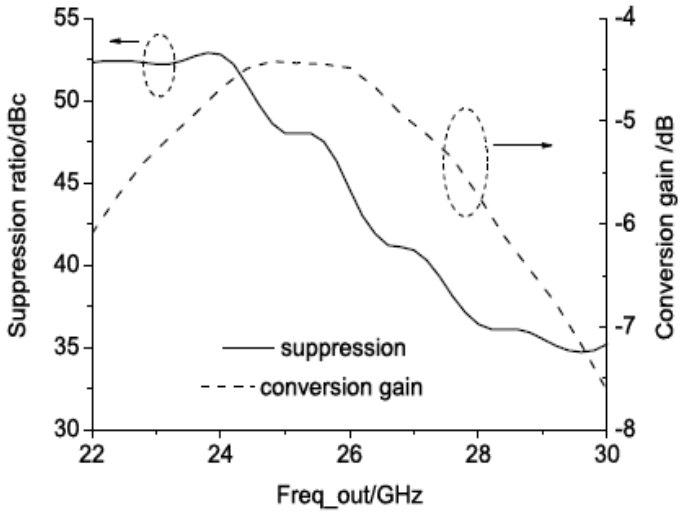

Fig.3-16 Simulated suppression and gain of proposed frequency doubler.

3.5 Measured results and performance comparison

The proposed broadband frequency doubler is fabricated in 0.25-μm SOI SiGe BiCMOS technology. The chip photograph is shown in Fig.3-17. The chip size is 1340×750μm^2 excluding pad area. The layout of the center signal pad should be as small as possible (50μm×50μm) with a pitch of 150-μm. The chip is fully measured on-wafer. At the input, the single-ended signal from power signal generator (Agilent E8267D) while the output is connected with power spectrum analyzer (Agilent E4448A). The bias condition is shown in TABLE 3-7.

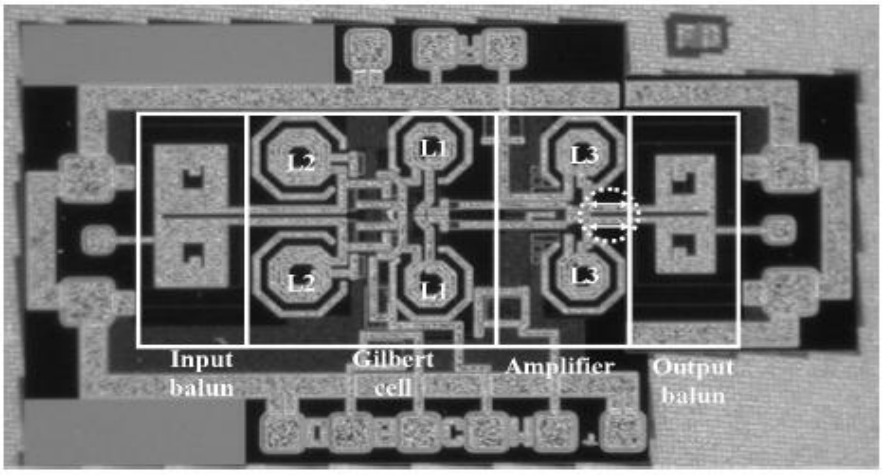

Fig.3-17 The micrograph of the proposed frequency doubler.

TABLE 3-7

Bias condition of the frequency doubler

V_{cc} ,V_{cm}[a]	I_{cc} +I_{cm}[a]	V_{cc_amp} ,$V_{cc\_amp\_cm}$[b]	I_{cc_amp} +$I_{cc\_amp\_cm}$[b]	Total DC Power
2.4V	5.7mA+0.9mA	3.3V	13.4mA+1.8mA	66mW

a: V_{cm}, I_{cm} are the bias voltage and current of current mirror in the Gilbert cell.

b: $V_{cc\_amp\_cm}$, $I_{cc\_amp\_cm}$ are the bias voltage and current of current mirror in the output amplifier.

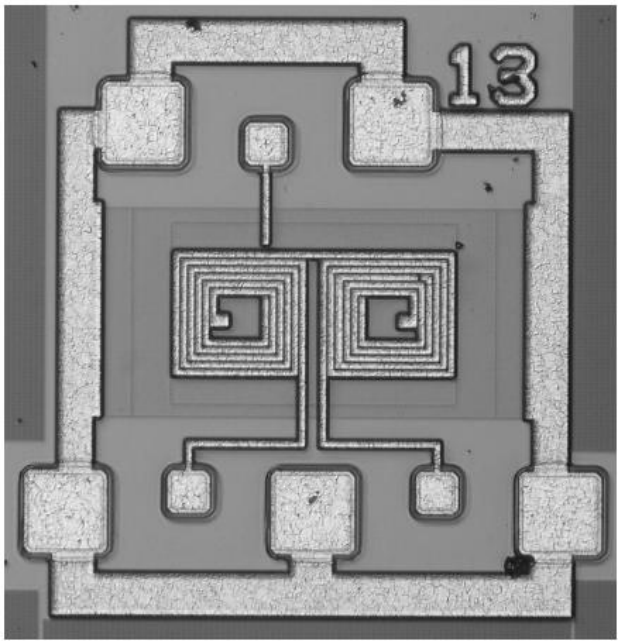

Fig.3-18 The micrograph of the input balun.

The micrograph of the input balun is shown in Fig.3-18 and the micrograph of output balun is mentioned in Fig. 2-15.

3.5.1 Measured results

The core sizes of the input and output baluns are 340×150μm^2 and 280×120μm^2, respectively. The input balun exhibits an amplitude imbalance of less than 0.5dB and a phase imbalance of less than 3° in the frequency band of 10-20GHz, as shown in Fig.3-19. Fig.3-20 depicts measured imbalance performance of the output balun at from 20 to 30GHz. The output balun has an amplitude imbalance of less than 0.9dB and a phase imbalance of less than 5°. From Figs.3-19 and 3-20, it is expected that the input and output baluns effectively convert from (to) single-ended signal to (from) balanced signal. These measured results well agree with the simulated ones. In addition, the measured insertion loss of the input balun is from -5.2dB to -2.6dB in the band of 11-15GHz, and the measured insertion loss of the output balun is -13.5~-9.6dB and -5.5~-2.4dB in the band of 11-15GHz and 22-30GHz, respectively.

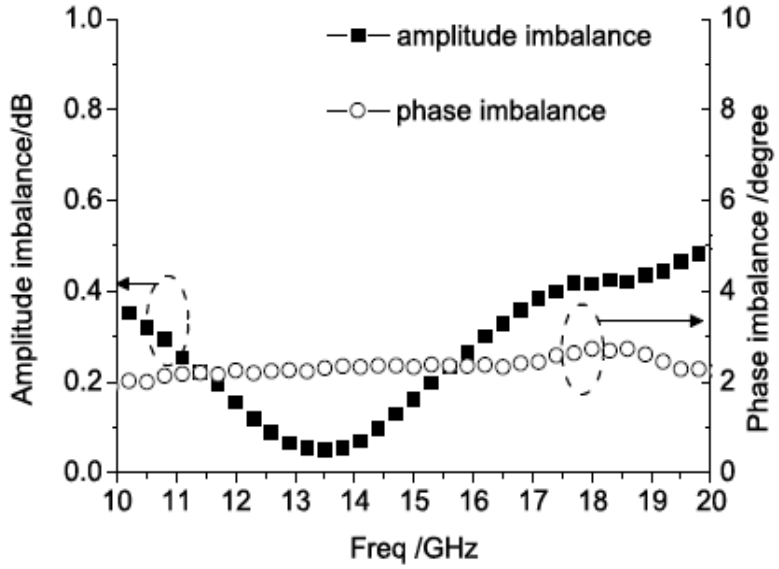

Fig.3-19 Measured imbalance performance of input balun

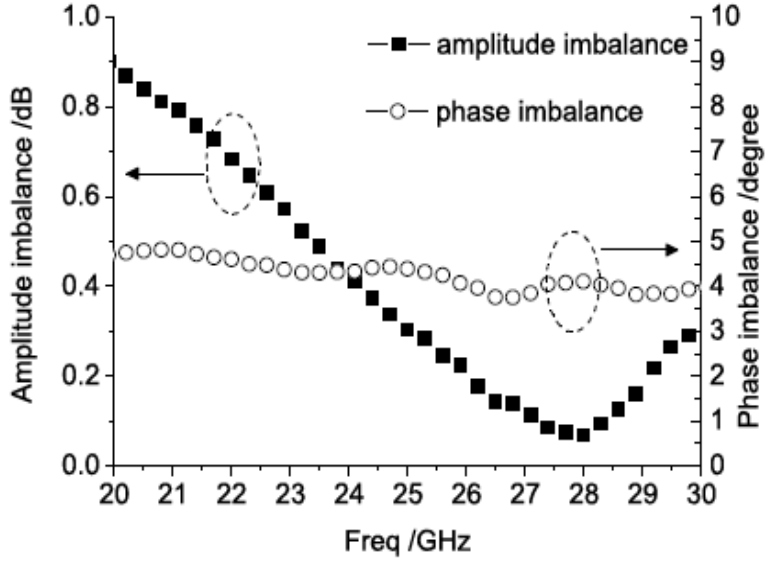

Fig. 3-20 Measured imbalance performance of output balun.

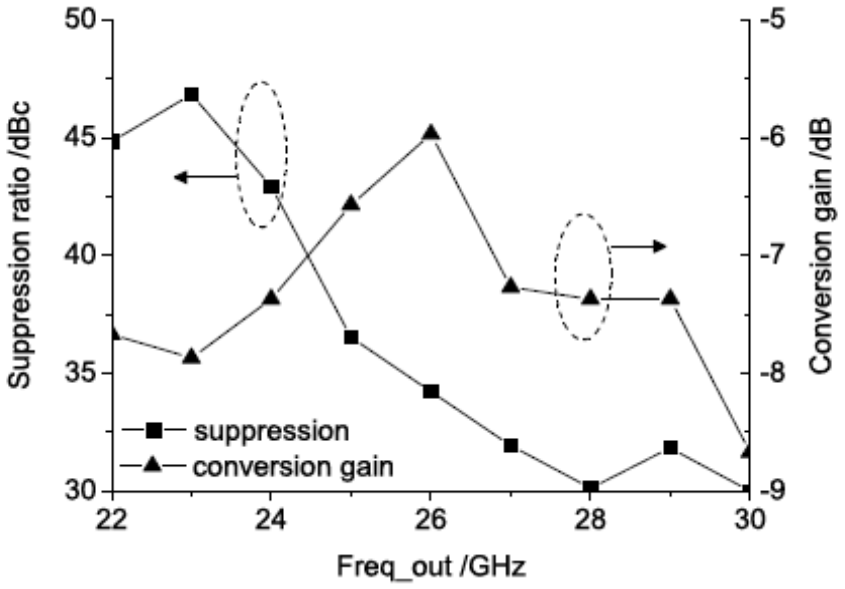

Fig. 3-21 Measured fundamental frequency suppression and conversion gain of the proposed frequency doubler.

Fig.3-21 shows measured fundamental frequency suppression and conversion gain of the frequency doubler, where the horizontal axis is the frequency at the output. The input power to the doubler is -1dBm. The proposed frequency doubler achieves a fundamental frequency suppression greater than 30dBc. The maximum suppression is 47dBc at 23GHz. In addition, from Fig.3-21, the conversion gain of the frequency doubler is higher than -9dB in the whole frequency band and the maximum conversion gain is -6dB. The measured conversion gain compared with the simulated one in Fig.3-16 is decreased by 2.5dB at 23GHz. The conversion gain is related to the output buffer amplifier and the output balun. The signal lines between the output amplifier and output balun are circled by dotted line shown in Fig.3-17. The physical parameters of the signal line are that the length is 82-μm, the width is 9-μm and the space between the lines is 20-μm. The measured inductance of single line is 0.15nH.

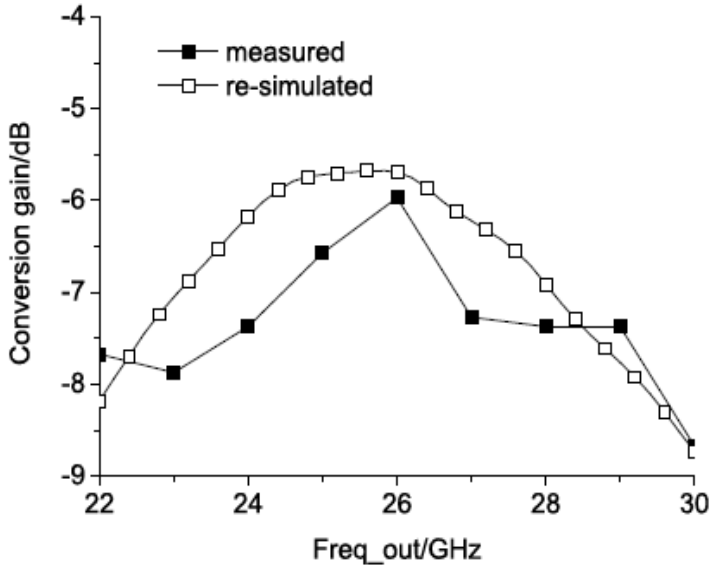

Fig.3-22 Measured re-simulated conversion gain of the proposed frequency doubler.

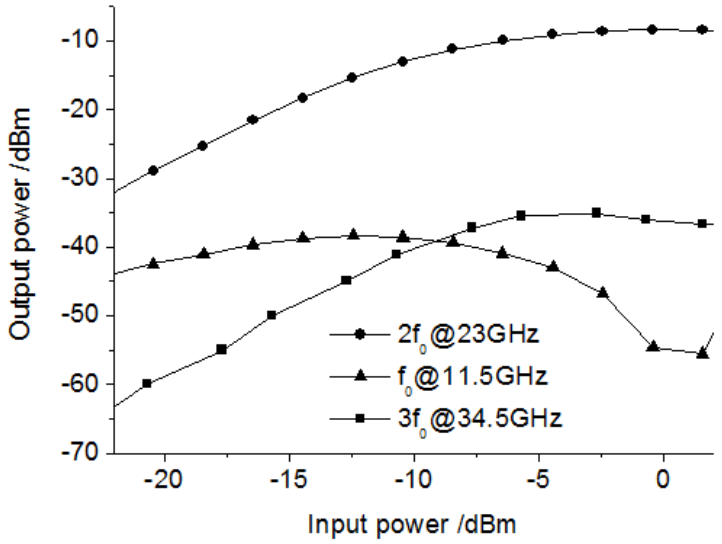

Fig.3-23 Measured input and output characteristic at an input frequency of 11.5GHz.

Hence, the parasitic effects of signal lines in the output of amplifier and output balun should be considered. The coupling line model is used to simulate. The re-simulated conversion gain including parasitic effects is demonstrated in Fig.3-22. The re-simulated gain is closed to the measured one. Fig.3-23 shows the measured input-output characteristic at an input frequency of 11.5GHz. The output power gradually saturates with increasing the input power and is almost constant at the input power from -5dBm to 0dBm. The suppression is larger than 32dBc at the same input power level and the maximum fundamental frequency suppression is 47dBc at the input power of -1dBm. Furthermore, Fig.3-23 also shows the output power of the third harmonic frequency. It is seen that the third harmonic frequency suppression is 30dBc at the input power of -1dBm. In addition, the measured third harmonic frequency suppression is better than 20dBc in the output band of 22-30GHz.

The measured return losses are shown in Fig.3-24. The measured input return loss and output return loss are less than -8.7dB and -6.5dB in the input frequency band of 11-15GHz and output frequency band of 22-30GHz, respectively. In the low band of output frequency, the output return loss is a little higher than the design target by 0.8dB because the frequency band of impedance matching of the output balun shifts toward to high frequency slightly. In addition, the measured fundamental frequency leakage of S_{21} is also depicted in Fig.3-24 and the leakage is less than -20dB when the input frequency is 11-15GHz.

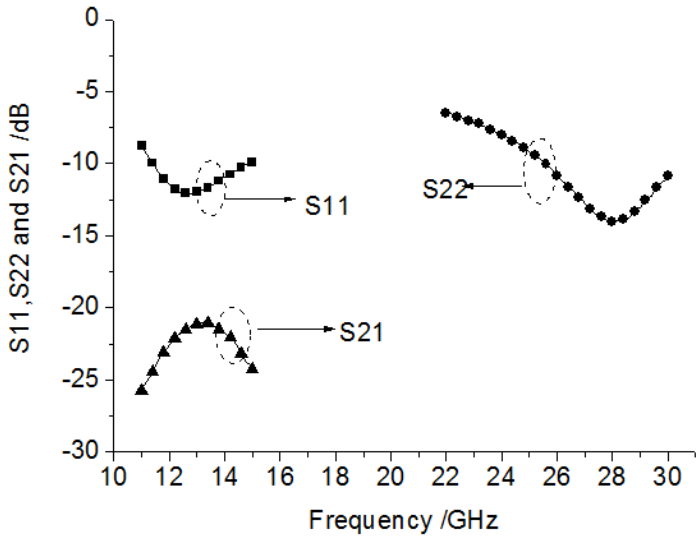

Fig.3-24 Measured return loss and leakage.

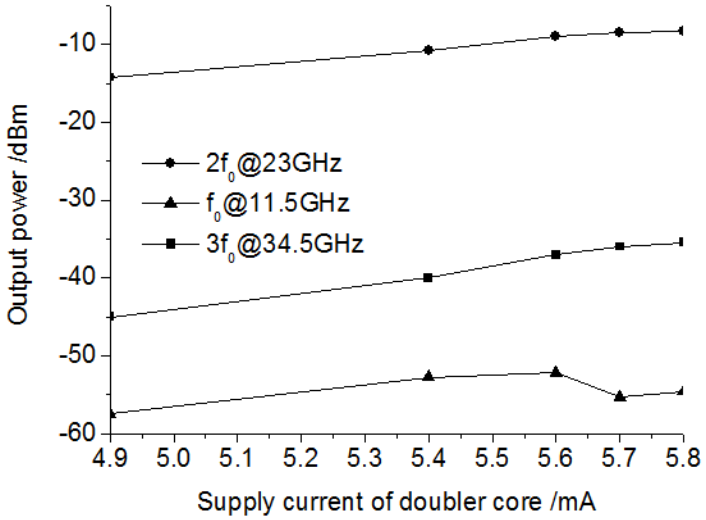

Fig.3-25 Measured dependence of output power on supply current of doubler core.

To gain more insight into the dependence of performance on supply current and voltage of doubler core, the output power of frequency doubler is shown in Fig.3-25 and the fundamental frequency suppression and conversion gain is demonstrated in Fig.3-26. In the Fig.3-25, the input power is -1dBm at an input frequency of 11.5GHz. The output power of 23GHz saturates from 5.6mA and decreases with the reduction of supply current. The output powers of 11.5GHz and 34.5GHz are less than -52dBm and -35dBm, respectively.

On the other hand, from Fig.3-26, it is found that the best suppression and gain can be obtained at 2.4 V with supply voltage of doubler core simultaneously. As the supply voltage decreased, the voltage drop of current source and the Q1-Q2 of the doubler core are also decreased. When the supply voltage is 2.1V, the current source only provide small current. Because the current source has entered the saturation region of transistor. The bias condition of Q1-Q2 and Q3-Q6 are all changed. Hence, the conversion gain at a supply voltage of 2.1V is sharply reduced.

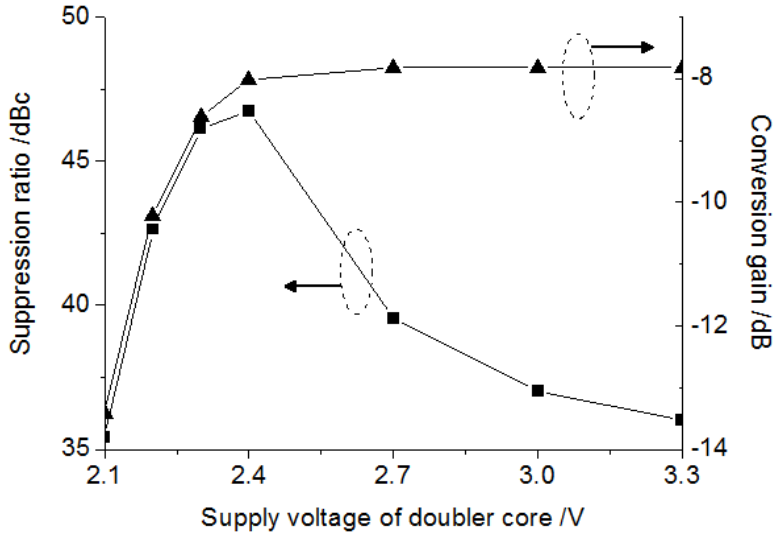

Fig.3-26 Measured dependence of fundamental suppression and conversion gain on supply voltage of doubler core

TABLE 3-8

Measured results summary and comparison with design goal

Items	Specifications	Measured results
Bandwidth	22-29GHz	22-30GHz
Input power	≤ 0dBm	-1dBm
Output power	≥ -10dBm	≥ -9.7dBm
Suppression ratio (f_0)	≥ 30dBc	≥ 30dBc
Suppression($3f_0$)	≥ 20dBc	≥ 20dBc
VSWR	≤ 2.5	≤ 2.5[a]
DC power consumption	< 80mW	66mW

a: In the low band of output frequency, the output return loss is a little higher than the design target by 0.8dB.

At last, a summary of measured results and comparison with the design goal is given in the TABLE 3-8. From this table, the measured results meets the requirements of the design goal. Hence, this frequency doubler can effective to be used in UWB sensor systems as expect.

3.5.2 Performance comparison

Based on the measured results, the broadband performance with high suppression which is greater than 30dBc has been verified. Using the FOM shown in equation 3-3, the performance comparison with other works can be obtained.

$$FOM = 20log_{10}(BW \times 100) + F.S - 10log_{10}\left(\frac{P_{DC}}{1mW}\right) \quad (3\text{-}3)$$

In this equation, BW is the frequency bandwidth of the doubler. P_{DC} is DC power consumption of the frequency doubler. F.S denotes fundamental frequency suppression of the frequency doubler.

The compared frequency doublers are the ones operated from K band to Ka band. The used devices are SiGe, GaAs and CMOS devices. The comparison conclusion is shown in TABLE 3-9 and the FOM with respect to input power is demonstrated in Fig. 3-27. Although the doubler in [19] used in SiGe HBT technology has high operation frequency, the bandwidth is narrower than this work and it show low FOM. Compared the doubler in [16] implemented in GaAs technology, both works have 8GHz bandwidth, however, the work in[16] consumes high DC power. Compared with the doubler in [35] implemented in 90-nm CMOS, the proposed work has higher suppression and wider bandwidth. Hence, the frequency doubler proposed in this chapter shows higher FOM and superior performance compared with doublers based-on GaAs technology and CMOS technology.

TABLE 3-9

Perfromance comparison with other works

Reference	Technology	Output frequency/GHz	Pin/dBm	FOM
This work	SiGe BiCMOS	22-30	-1	60
[19]	SiGe HBT	34.6-37.6	6	32
[16]	GaAs	26-34	3	48
[34]	GaAs	30-32	5	20
[35]	90nm CMOS	37.5-39	0	38

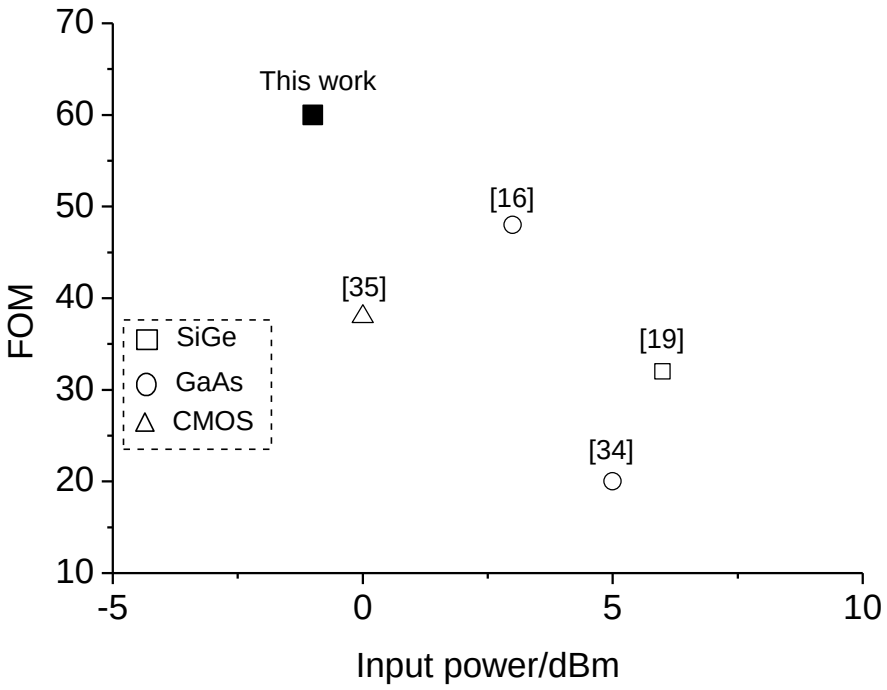

Fig.3-27 Broadband frequency doubler comparison with other works.

3.6 Conclusion

In this chapter, a broadband frequency doubler based on Gilbert cell is proposed. The proposed frequency doubler is implemented in 0.25-μm SOI SiGe BiCMOS technology and measured on wafer.

In the Gilbert cell, the input signal shows amplitude and phase imbalance, which results in the imbalance signal of second harmonic at the output of the RF stage of Gilbert cell. The imbalance signal of second harmonic multiplied by the fundamental input signal generates the fundamental signal in the output of the frequency doubler. In order to reduce the imbalance signal of second harmonic at the output of RF stage, an internal low pass filter technique is designed to suppress the second harmonic imbalance signal. And a pair of matching circuits parallel with the input of switch quad show impedance match between Gilbert cell and input balun. The matching circuits is effective to provide high input power into switch quad so that keep the doubler operates in low input drive power with high suppression, relaxing the design of VCO.

To verify the effectiveness of these techniques, a balanced frequency doubler has been fabricated in 0.25-μm SOI SiGe BiCMOS technology and measured on-wafer. A high fundamental frequency suppression of 47dBc has been achieved at 23GHz, and better than 30dBc in a broad frequency band of 22-30GHz. The proposed frequency doubler achieves a maximum conversion gain of -6dB at an input power as low as -1dBm. frequency doubler proposed in this chapter shows superior performance compared with doublers based-on GaAs technology and CMOS technology.

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Chapter 4 High Suppression Frequency Doubler IC for Wireless Communications

4.1 Introduction

In the Chapter 3, a broadband frequency doubler based on Gilbert cell has been proposed, implemented and measured on-wafer. The broadband performance was verified according to the measured results. A high fundamental frequency suppression frequency doubler for 26GHz band wireless communication is proposed in this chapter.

As mentioned in Chapter 1, 26GHz band vehicular radar sensor can avoid the band of 23.6-24GHz. The band 23.6-24GHz is allocated to passive services including the radio astronomy and earth exploration satellite services on a primary basis in the radio regulations which prohibit all emissions into the band. The 26GHz band has been introduced from 2004 in USA. In Japan, the 24GHz band will been unavailable until December 2016. On the other hand, the penetration of 26GHz band radar sensor is expected to 7% in 2022 [1]. EU also has proposed the 26GHz band short range radar sensor scheme for e-Safety conception [2].

The desired output power of frequency doubler is the power of the second harmonic frequency. However, as the desired power being generated, the unwanted powers are also accompanied with the desired power such as fundamental frequency, third harmonic frequency and so on. The unwanted frequency may be injected into power amplifier and couple to the low noise amplifier by the switch. The unwanted powers going into the PA and LNA deteriorate the per-

formance of PA and LNA [3]. Moreover, these unwanted frequencies may result in desensitization, cross modulation and inter modulation by the radiation of antenna when the unwanted signals fall in the corresponding bands [4]. In the UWB spectrum mask announced by FCC, the fundamental suppression should be greater than 20dBc [5]. Hence, the output of frequency doubler should reject the unwanted frequencies, fundamental frequency in particular.

This chapter is organized as follows. Frequency suppression technique review followed this part is shown in section 4.2, and section 4.3 describes high suppression frequency doubler design. From section 4.4, measured results and performance comparison is demonstrated. Finally, section4.5 gives a conclusion of this chapter.

4.2 Frequency suppression technique review

One of the most important motivation of designing frequency multiplier is to reject the undesired frequency component at the output. So far, many researchers devoted themselves to proposing effective solutions such as half-wave length bias circuit [6], band pass filter technique [7]-[8], resistive feedback circuit [9] and balanced topology [10]-[12].

A solution for frequency doubler utilizes the fact that a transmission line with an electrical length of $\lambda/2$ at the output frequency ($2f_0$) has a length of $\lambda/4$ for the fundamental frequency (f_0). Therefore the line in the base bias transforms the RF short of the DC supply to an open for fundamental frequency, but to a short for $2f_0$. This single element at the same time provides an RF choke at f_0 and prevents energy at $2f_0$ from leaking out through the input. At the transistor output, similar constructions are used. However, these lines are quite demanding in terms of chip area, especially in coplanar technologies. Band pass filter technique can used in the output of multiplier to pass the desired frequency and reject the undesired frequency. Yomaguchi, in [7], implemented a x-band frequency quadrupler utilizing a 2-band elimination band pass filter. The band pass filter solution also has low area efficiency.

A degeneration resistive feedback technique using frequency doubler can improve the frequency suppression duo to the change the dynamic load line of transistor in core circuit. The suppression improvement is only 7dBc compared with the conventional doubler which is without degeneration resistor.

Balanced topology usually uses the nonlinearity of transistor to generate second harmonic

frequency and cancel out the fundamental frequency at output. A push-push circuit is the famous one in balanced topology. Most of works using push-push topology are differential inputs, single-ended output and the improvement of suppression depends on the better imbalance performance of input balun. In [10], Lee proposed a fully differential doubler based on push-push circuit, however, the suppression performance also depends on the input balun.

4.3 High suppression frequency doubler design

In this section, the frequency doubler will be designed which generates the desired frequency using push-push circuit core. Firstly, the design goal is described. Then the design concept of frequency doubler core is demonstrated. The doubler core design and simulated results of frequency doubler are given at the last of this section.

4.3.1 Design goal

As mentioned in Chapter 1, a simple block of FMCW frontend was introduced in [13], where a VCO cascades a frequency doubler with input and output buffers to realize a stable signal source. Doublers with input and output buffers can improve conversion gain of whole circuit and operate in low input drive power. Fig.4-1 shows the block diagram of the proposed frequency doubler includes doubler core, input and output buffers and input and output on-chip baluns owing to balanced operation.

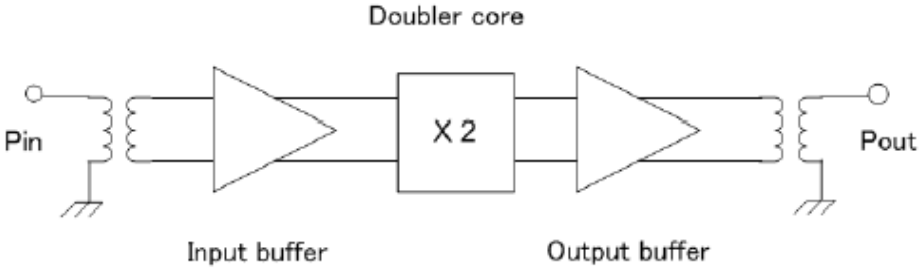


Fig.4-1 The block diagram of the proposed frequency doubler.

Due to the differential operation of the proposed frequency doubler, the input and output baluns are essential components as depicted in Fig.4-1. Both baluns are used to split and combine the differential signal in the input and output of the doubler. A passive Marchand balun is chosen due to better amplitude balance and phase balance than active one. In addition, there is little dependence of temperature on the performance of passive balun and no DC power consumption. The performance of input and output baluns have been demonstrated in Chapter 3.
Since the input power of frequency doubler is the output power of VCO or PLL, the output powers of oscillators operating from 11 GHz to 14.5GHz were investigated and are illustrated in Fig.4-2 [14]-[19]. In Fig.4-2, the output powers are almost from -10dBm to 0dBm. To release implementation difficulty of VCOs, the target input power of this work is determined to be -10dBm. The design targets are listed in TABLE 4-1.

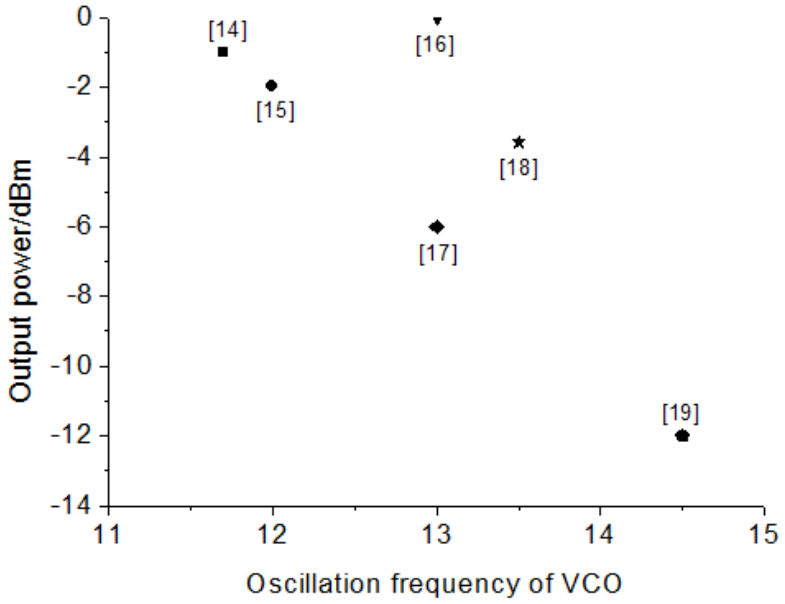


Fig.4-2 Output powers of oscillators operating at 11-14.5GHz.

TABLE 4-1

Design goal of frequency doubler

Items	Specifications
Output frequency	26GHz
Pin	-10dBm
Fundamental suppression	≥ 40dBc
Conversion gain	≥ 0dB
P_{dc_core}	< 10mW
P_{dc}	< 150mW
Supply voltage	3.3V

4.3.2 Doubler core design concept

Frequency doublers based on push-push circuit exploit steep nonlinear I-V characteristic to generate output second harmonics. Fundamental frequency signals are canceled out at the nodes of emitters and collectors when the doubler core is driven by differential input signals [20]-[23]. A fully differential push-push circuit core is shown in Fig.4.3.

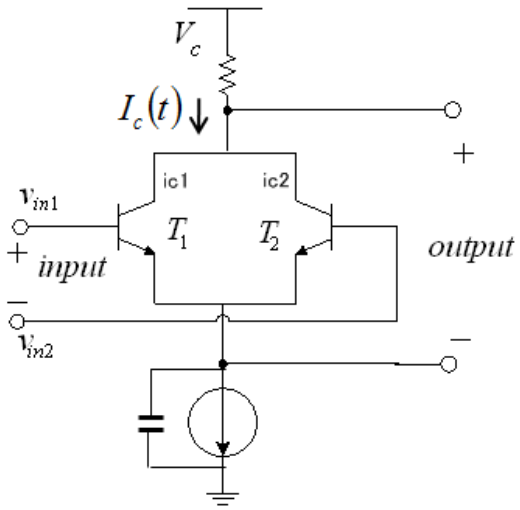


Fig.4-3 The conventional fully differential frequency doubler core.

Its harmonic component of collector current (I_c) is a function of conduction angle, which can be controlled by the input driving power and base bias point. If the collector current is modeled as a train of rectified cosine pulses (Fig.4-4), using a Fourier series expansion, it can be represented as [24] and I_{max} is the maximum current, t_0 is the length of the pulse, and T is the period of the fundamental frequency. The collector current can be described using equations from 4-1 to 4-4. In the case of second harmonic current, by equation 4-4, a relationship between second harmonic current and conduction duty cycle of each transistor is drawn in Fig.4-5. To maximize the second harmonic current (I_2), the conduction duty cycle of each transistor t_0/T is 0.32, which indicates the transistor is bias in Class C. As known that, Class C amplifier is driven large signal, namely high input power. However, as mentioned above, the design goal of the frequency doubler is low input power operation. Hence, the Class C is not a good candidate although it can save DC power.

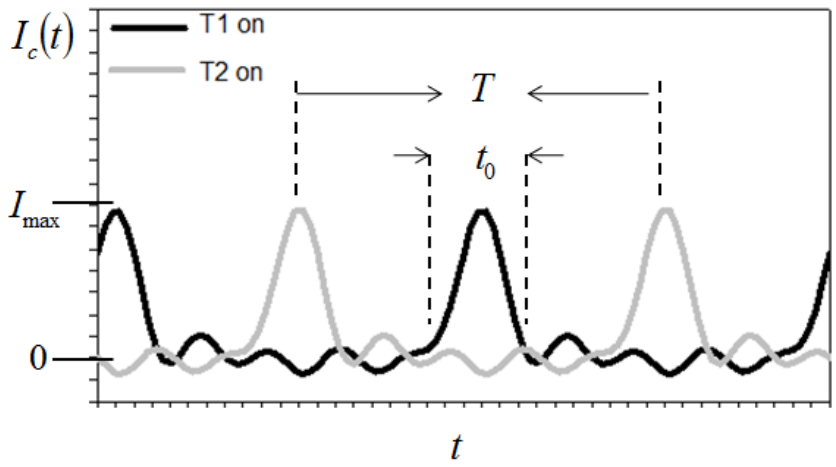


Fig.4-4 Corrector current modeled as a train of rectified cosine pulses.

$$I_c(t) = I_0 + I_1 cos(\omega_1 t) + I_2 cos(\omega_2 t) + \cdots \quad (4\text{-}1)$$

where I_n is *n* th harmonic current component

$$I_0 = I_{max} \frac{2t_0}{\pi T} \quad (4\text{-}2)$$

$$I_n = 0, \quad n\ odd \quad (4\text{-}3)$$

$$I_n = I_{max}\,\frac{8t_0}{\pi T}\left|\frac{cos\left(\frac{n\pi\, t_0}{T}\right)}{1-\left(\frac{2n t_0}{T}\right)^2}\right|, \quad n\ even \tag{4-4}$$

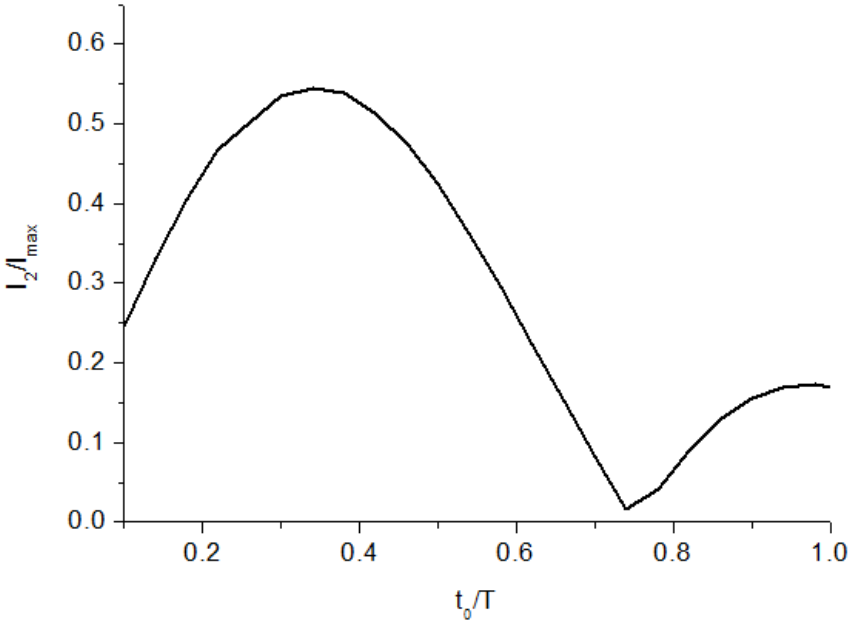


Fig.4-5 Second harmonic collector current components as a function of t_0/T.

A push-push conventional fully differential frequency doubler core circuit biased on near class B shown in Fig.4-3 generates differential second harmonic frequency at the output and ideally cancels fundamental frequency owing to perfect input differential signal and well-matched transistors T_1 and T_2.

Practically, the differential input signals are imbalance signals with amplitude and phase imbalance, coming from the differential input buffer amplifier. Piernas,et.al analyzed the influence of imbalance input signal on fundamental frequency rejection [25]. In addition, both transistors in push-push circuit should be well-matched. The input differential signals of doubler core from the input buffer amplifier shown in Fig.4-3, as mentioned above, are imbalance signals due to amplitude unbalance and phase unbalance. Hence the input signals are explicitly given by

$$v_{in1} = V_0 + a_0\, cos(\omega_0 t + \theta) \tag{4-5}$$

$$v_{in2} = V_0 - a_0 K(\omega_0)\, cos[\omega_0 t + \theta + \varphi(\omega_0)] \tag{4-6}$$

where $K(\omega_0)$ and $\varphi(\omega_0)$ are the amplitude unbalance and phase unbalance.

The total output currents of the circuit given in Fig.4-3 are the sum of currents flowing in the T_1 and T_2, given by equations from 4-7 to 4-10.

$$i_{c1}(t) + i_{c2}(t) \rightarrow i_o(\omega_0) + i_0(2\omega_0) \tag{4-7}$$

where

$$\begin{aligned} i_0(\omega_0) = {} & (g_{m1} A a_0 + 2g'_{m1} A^2 V_0 a_0) \times \pi \times \left[\delta(\omega + \omega_0) \times e^{j\theta} + \delta(\omega - \omega_0) \times e^{-j\theta}\right] \\ & - \left(g_{m2} B a_0 K(\omega_0) + 2g'_{m2} B^2 V_0 a_0 K(\omega_0)\right) \times \pi \\ & \times \left[\delta(\omega + \omega_0) \times e^{j(\theta+\varphi)} + \delta(\omega - \omega_0) \times e^{-j(\theta+\varphi)}\right] \end{aligned} \tag{4-8}$$

$$\begin{aligned} & i_0(2\omega_0) = \\ & \left(\frac{1}{2} g'_{m1} A^2 a_0^2\right) \times \pi \times \left[\delta(\omega + 2\omega_0) \times e^{j2\theta} + \delta(\omega - \omega_0) \times e^{-j2\theta}\right] - \left(\frac{1}{2} g'_{m2} B^2 a_0^2 K^2(\omega_0)\right) \times \\ & \pi \times \left[\delta(\omega + 2\omega_0) \times e^{j2(\theta+\varphi)} + \delta(\omega - 2\omega_0) \times e^{-j2(\theta+\varphi)}\right] \end{aligned} \tag{4-9}$$

$$A = \frac{\beta}{\beta + r_{b1} g_{m1}} \qquad B = \frac{\beta}{\beta + r_{b2} g_{m2}} \tag{4-10}$$

From equation 4-7, the output of the frequency doubling circuit not only has desired component but also fundamental frequency component, which decreases the fundamental frequency F.S (Frequency Suppression) defined by equation 4-11.

$$F.S(dBc) = 10log\left(\frac{P(2\omega_0)}{P(\omega_0)}\right) \quad (4\text{-}11)$$

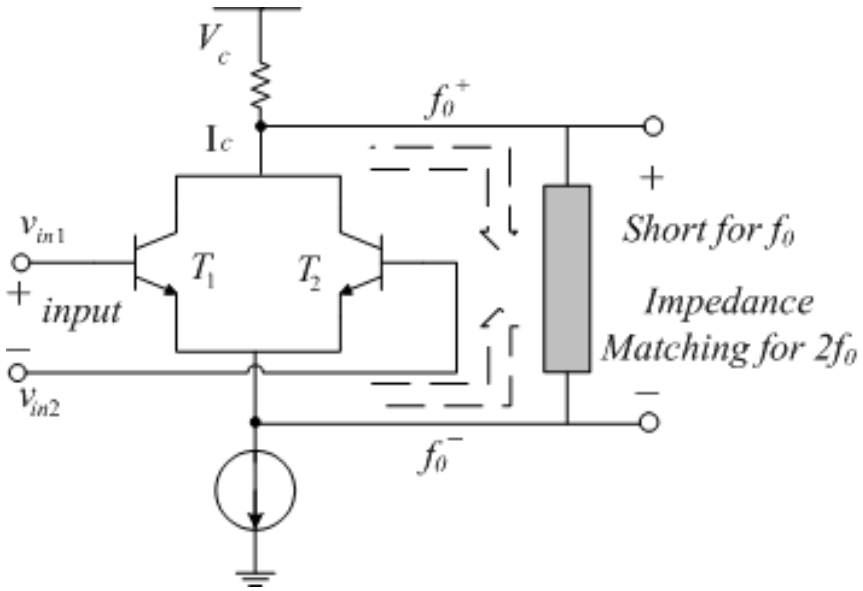


Fig.4-6 Design concept to reject fundamental frequency and match impedance for $2f_0$.

High fundamental frequency suppression will be achieved if the fundamental frequency component is rejected at the output of doubler core. Owing to the differential outputs of the push-push circuit, a short circuit can cancel the fundamental frequency at the differential outputs shown in Fig.4-6. Moreover, the output power of frequency doubler should be as large as possible. Hence, the circuit canceling the fundamental frequency components also has impedance matching with the output buffer at the second harmonic frequency. As known that, a ideal series LC resonator can exhibit short circuit effect at low frequency and high inductance at high frequency. Hence, a series LC resonator is good candidate to cancel the fundamental frequency and matches the output impedance of core with input impedance with output buffer.

4.3.3 Push-push core design

According to the aforementioned analysis, a series LC resonator circuit is proposed to improve the suppression of fundamental frequency at the output of the double core, as shown in Fig.4-8. Before designing the doubler core, the input impedance of output buffer at 26GHz is simulated

and shown in Fig.4.9, the performance of output buffer has been introduced in Chapter 3. The size and performance of transistor T_1 and T_2 are listed in the TABLE 4-2. The size of transistors and inductance in the output buffer are described in Chapter 3. The bias circuits of Fig. 4-8 are not shown. Another feature of this LC resonator is to improve matching condition between the input of the output buffer (Z_{o_in}) and the output of the doubler core (Z_{c_out}) at the second harmonic frequency. The calculation equations of LC resonator are defined in equations 4-12 and 4-13, respectively.

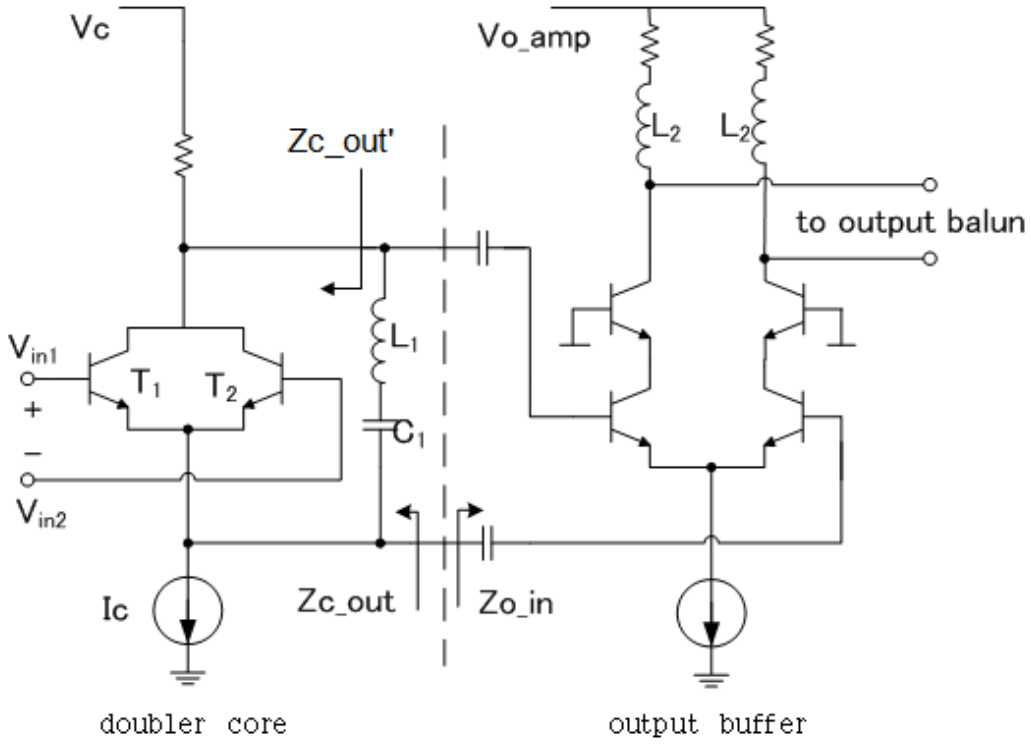


Fig.4-8 The proposed suppression and conversion gain improving technique using LC resonator.

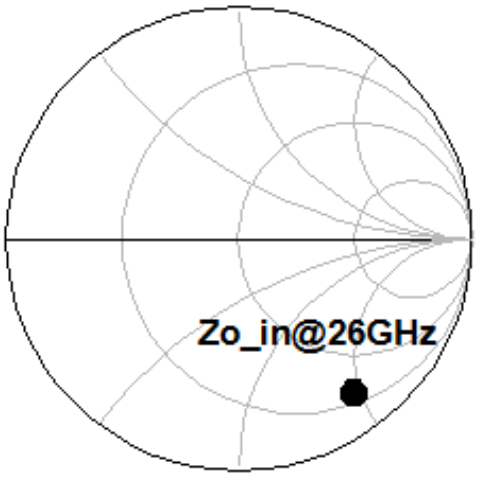


Fig.4-9 Input impedance of output buffer at 26GHz.

TABLE 4-2

Size and performance of transistors in the doubler core

	Size	f_t/f_{max}
T_1-T_2	0.2μm×4μm	46.2GHz/66.5GHz

$$\omega_0 = \frac{1}{\sqrt{L_1 C_1}} \tag{4-12}$$

$$\left(j2\omega_0 L_1 + \frac{1}{j2\omega_0 C_1}\right) // Z_{c\_out}{}' = \left(Z_{0\_in}\right)^* \tag{4-13}$$

Thus, the inductance (L_1) and capacitance (C_1) are determined so that (1) the resonant frequency is 13GHz (equation 4-12) and (2) the output impedance of the doubler core is complex conjugate of the input impedance of the output buffer amplifier at 26GHz (equation 4-13). Consequently, the optimum inductance and capacitance are 0.5nH and 0.3pF, respectively. The frequency response of the output impedance of the doubler core from 13GHz to 26GHz and the input impedance of the output buffer amplifier at 26GHz are shown in Fig.4-10. This inductor is designed using top metal of 3-μm thickness. This inductor has a Q of 16 at 13GHz.

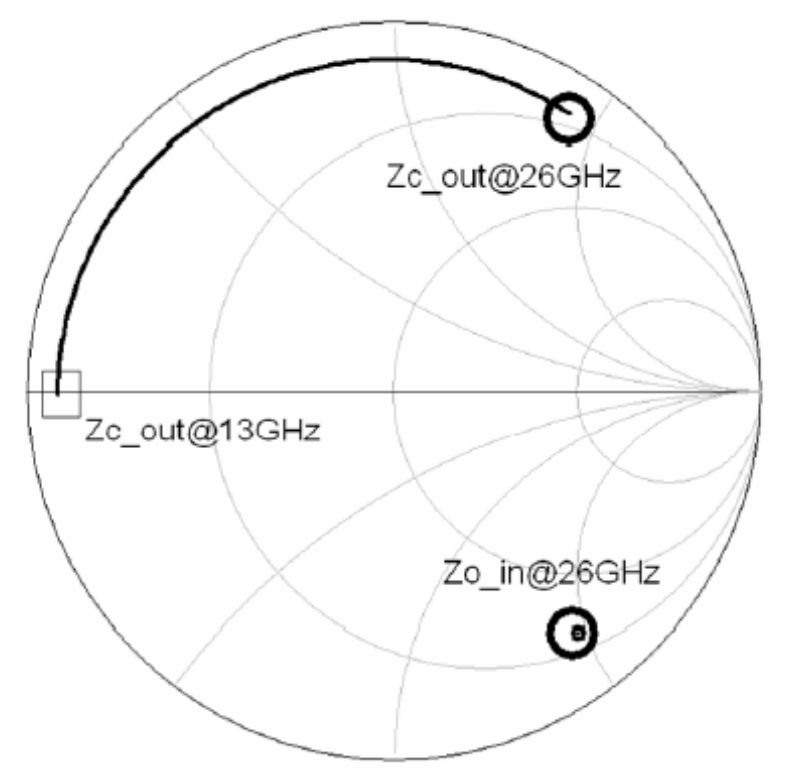


Fig.4-10 Frequency response of the output impedance of doubler core.

4.3.4 Circuit design and simulated results

Fig.4-11 shows the schematic of the input buffer amplifier consisting of a common base amplifier and a differential amplifier. The bias circuit is not shown. The size of Q_1-Q_2 are 0.2μm×1μm. The size of Q3-Q6 are 0.2μm×4μm and the fingers are 3. The g_m of Q_1-Q_2 are optimized to match with the impedance at the differential ports of input balun. The simulated gain of input buffer with input and output baluns is shown in Fig.4-12. From 10GHz to 15GHz, the gain is from 7.5dB to 9.5dB and the gain flatness is within 2dB. At 13GHz, the gain is 8.7dB. Hence, the input power injected in to doubler core is enough to drive the core operating as a switch.

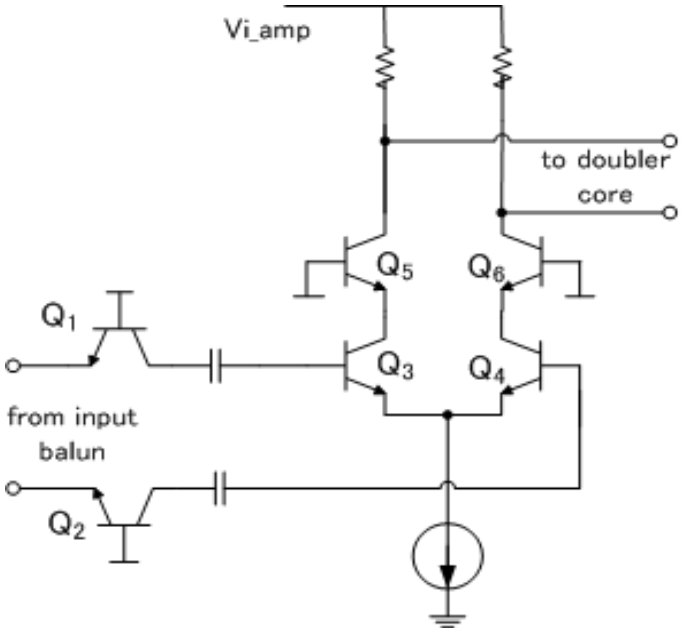


Fig.4-11 The schematic of input buffer amplifier.

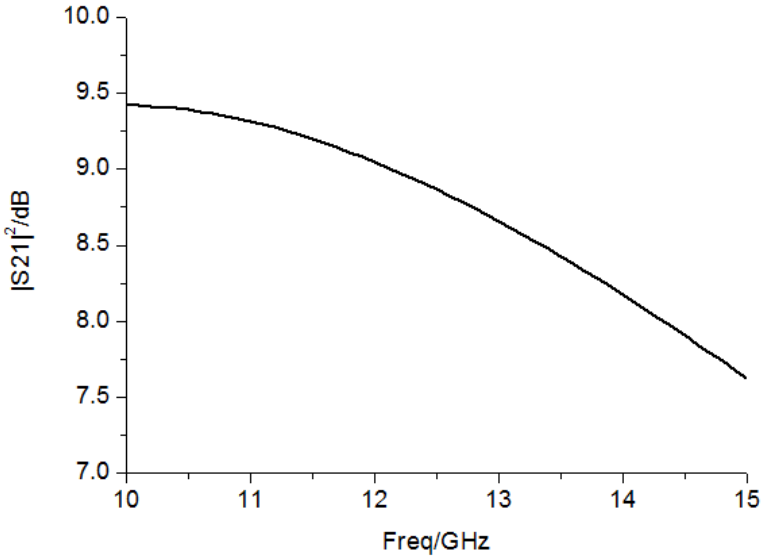
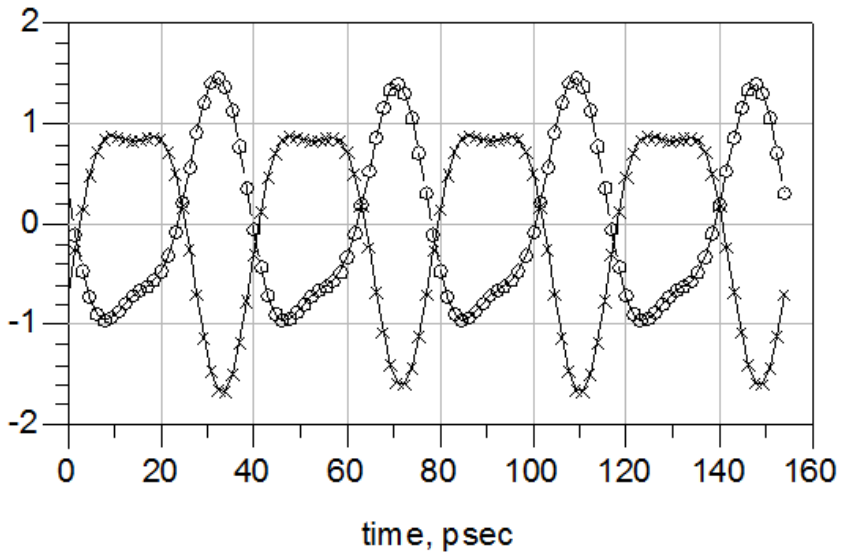
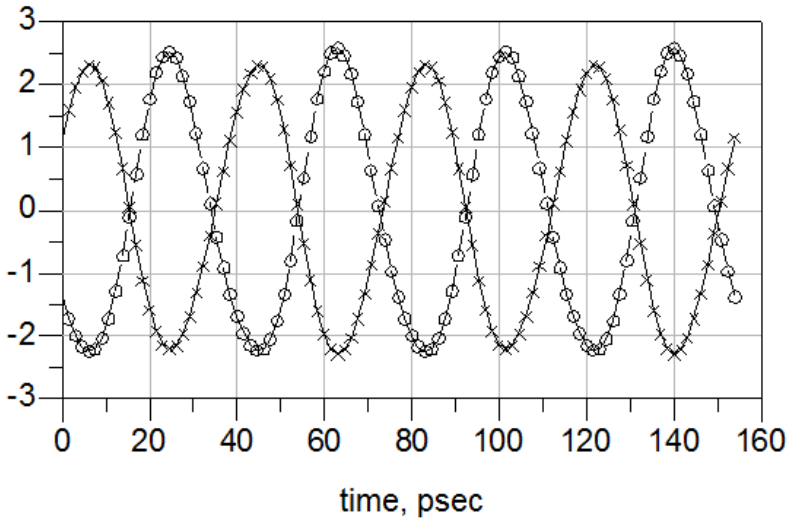


Fig.4-12 The simulated gain of input buffer amplifier.

Due to the differential operation of the output buffer, the input signal should be balance signal which determines the output buffer performance. Fig.4-13 describes the simulated current waveforms of doubler core without LC and with LC, respectively. The output of doubler core with LC is more symmetrical and larger than the one without LC shown in Fig.4-13. As discussed above, the LC resonator changes the output impedance of doubler core. Therefore the load lines of transistors T1 and T2 are sloped further as expected resulting in the switch-off operation of transistors more complete. Owing to the conjugated matching between core and output buffer, more power injecting into the output buffer, the current amplitude of waveform (b) is larger than the one of waveform (a).



(a)



(b)

Fig.4-13 The simulated current waveform of doubler core at output frequency of 26GHz: (a) waveform w/o LC,(b) waveform with LC

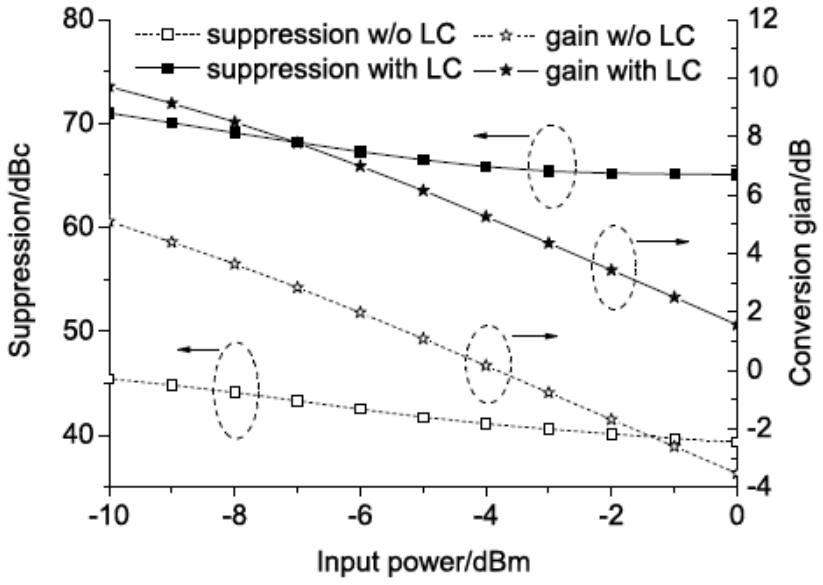


Fig.4-14 The simulated suppression and conversion gain of the whole circuit with the optimized LC resonators an without LC resonator at an input frequency of 13GHz

Simulated fundamental frequency suppression and conversion gain of the whole circuit with optimized LC resonator and without LC resonator at an input frequency of 13GHz are illustrated in Fig.4-14. The fundamental frequency suppression of the proposed frequency doubler is improved by 25dB compared with the one without LC resonator. In addition, the conversion gain of proposed frequency doubler is improved by 4dB. Therefore, the LC resonator is effective to improve the suppression and conversion gain.

4.4 Measured results and performance comparison

The proposed frequency doubler is implemented in 0.25-μm SOI SiGe BiCMOS technology. The die photograph of the implemented frequency doubler IC is shown in Fig.4-15. The layout of the center signal pad should be as small as possible (50μm×50μm) with a pitch of 150-μm. The chip size is 1.4×0.65 mm^2 excluding pad area. The bias condition of the frequency doubler are listed in TABLE 4-3. The performance of the whole circuit of the frequency doubler are measured on-wafer.

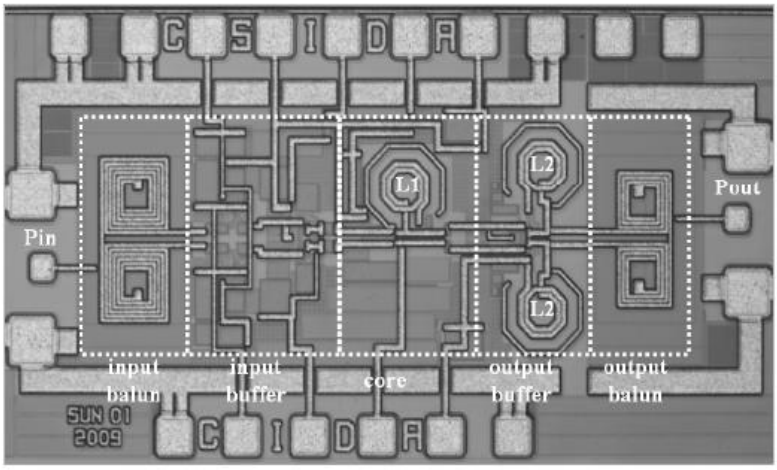


Fig.4-15 The micrograph of the proposed frequency doubler.

TABLE 4-3

Bias condition of the frequency doubler

$V_c = V_{i\_amp}$ $= V_{o\_amp}$	I_{i_amp} + $I_{i\_amp\_cm}$[a]	I_c + I_{cm}[a]	I_{o_amp} + $I_{o\_amp\_cm}$[a]
3.3V	20.3mA+5mA	1.9mA+0.5mA	12.2mA+1.6mA

a: $I_{i\_amp\_cm}$, I_{cm} and $I_{o\_amp\_cm}$ are the bias current of current mirror of input amplifier, doubler core and output amplifier, respectively.

4.4.1 Measured results

Fig.4-16 shows the measured and simulated input/output characteristic at an input frequency of 13GHz.

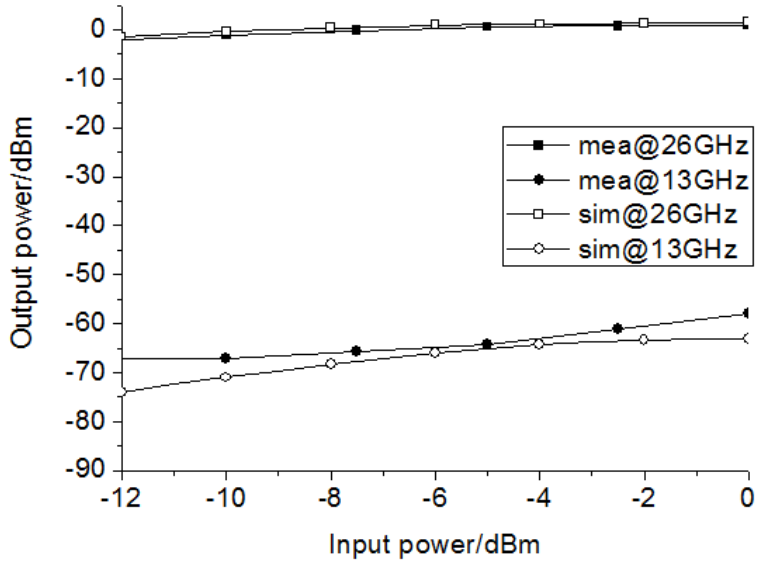


Fig.4-16 Measured and simulated input-output performance at an input frequency of 13 GHz.

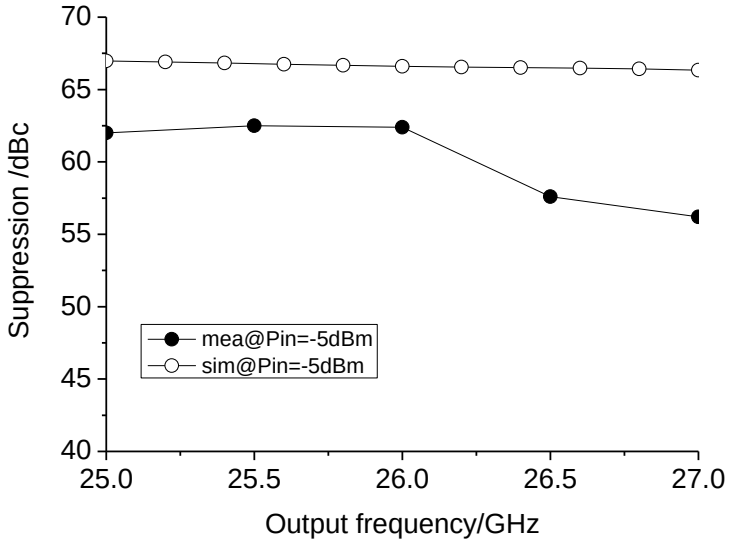


Fig.4-17 Measured and simulated frequency response of fundamental frequency suppression

The measured output power at 26GHz is saturated and is almost constant from -10dBm to 0dBm. The measured output power at 26GHz is closed to 0dBm. The measured fundamental frequency output power is less than -58dBm at an input power of from -10dBm to 0dBm. At the input powers from -10dBm to 0dBm, the difference between the measured fundamental frequency output power and the simulated one are less than 5dB. The measured maximum suppression is 66dBc at an input power of -10dBm.The measured output power at 13GHz is almost constant at an input power lower than -10dBm. This phenomenon results from the limitation of dynamic range of the spectrum analyzer.

The frequency response of the fundamental frequency suppression at an input power of -5dBm is given in Fig.4-17. The measured fundamental frequency suppression achieves greater than 55dBc at an input power of -5dBm in the broadband of 25-27GHz. However, there is significant difference between the simulated results and measured results over 26GHz. The reason will be discussed later.

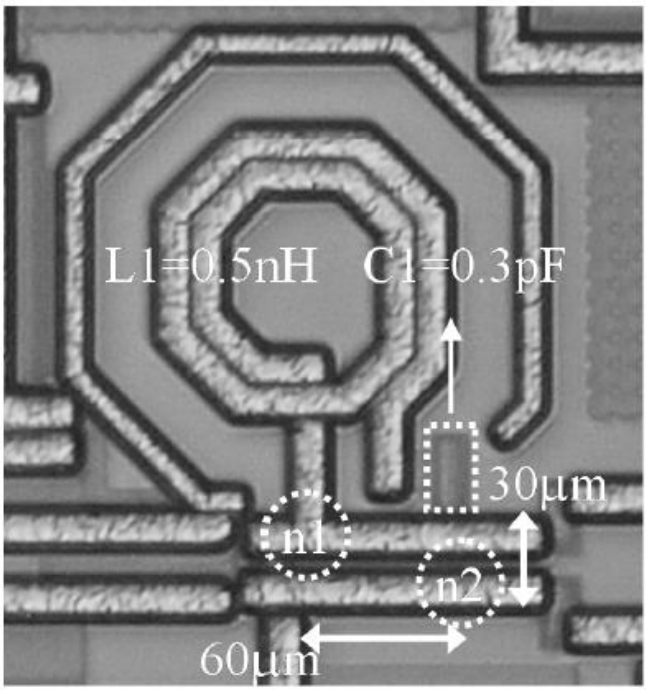


Fig.4-18 layout of LC resonator in Fig.4-15.

The LC resonator is connected in parallel with the output notes (n1,n2) of the doubler core circuit shown in Fig.4-18. It is found that the connecting lines including 60-μm length, 9-μm width connecting line using top metal (M4) and 30-μm length, 9-μm width connecting line using metal 1 (M1) introduce parasitic effects. To investigate the influence on resonant frequency and suppression of the frequency doubler, LC resonator with the connecting lines is measured.

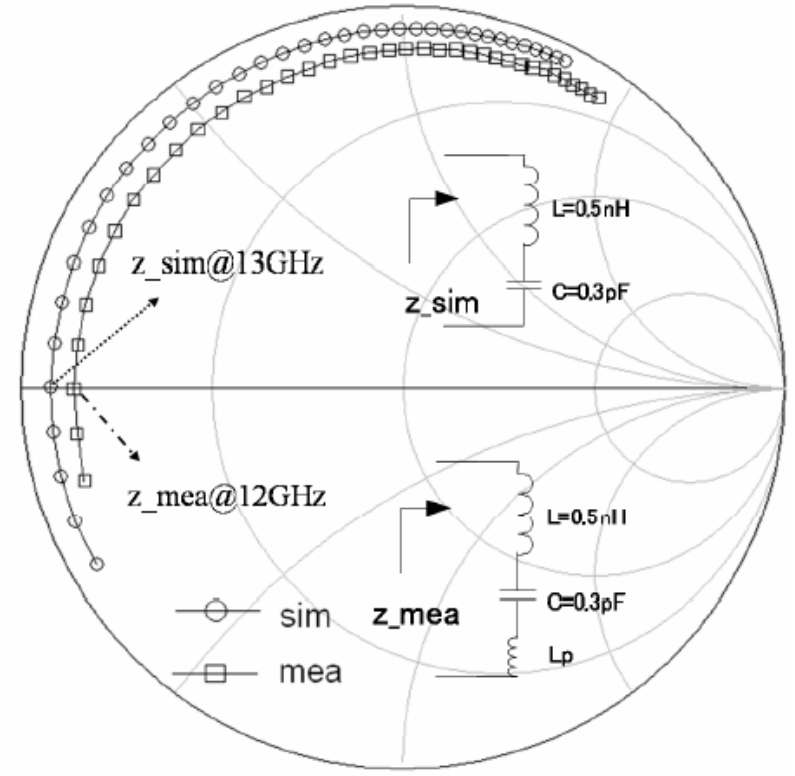


Fig.4-19 Measured and simulated impedance of LC resonator (From 11GHz to 29GHz, step by 500MHz).

Fig.4-19 shows the measured impedance of LC resonator with the connecting lines and the simulated impedance of LC resonator, respectively. The measured resonant frequency is 12GHz deviating the designed frequency of 13GHz. Thus, the measured performance of the suppression over 26GHz are degraded compared with the simulated one. From revised simulation using the measured results in Fig.4-19, it is expected that the suppression at an input frequency of 13.5GHz is 60dBc, which agrees with the measured one.

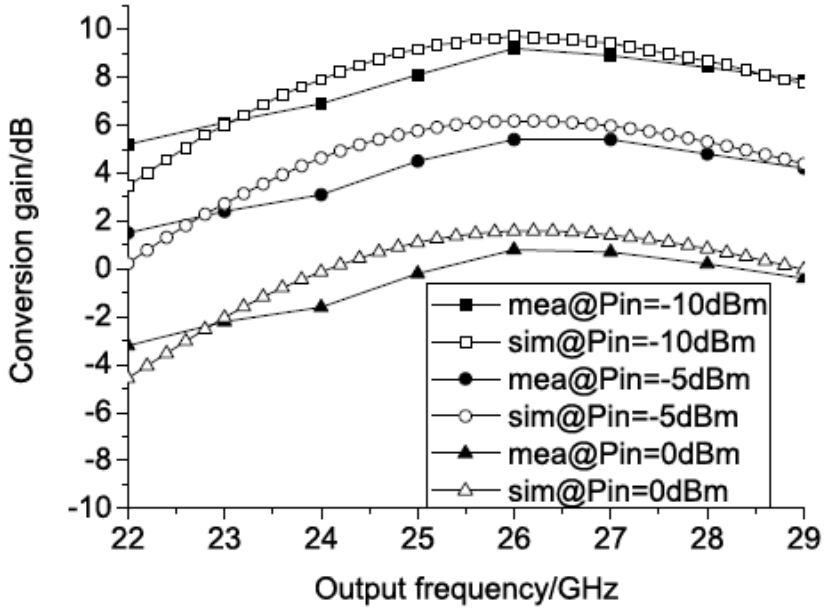


Fig.4-20 Measured and simulated frequency response of conversion gain.

Fig.4-20 illustrates the frequency response of conversion gain with different input power. From Fig.4-20, it can be seen that the measured conversion gain of frequency doubler is larger than 5dB over the frequency band of 22-29GHz at an input power of -10dBm. Furthermore, the measured maximum gain is 9.2dB at an output frequency of 26GHz. The output powers of frequency doubler are greater than -5dBm over the output frequency of 22-29GHz when the input power is -10dBm.

The proposed doubler core is biased on near Class B. To gain more insight on dependence of performance on the bias conditions, the measured fundamental frequency suppression and conversion gain with varying supply voltage and current for doubler core are shown in Figs.4-21 and 4-22. The input frequency is 13GHz and the input power is -10dBm. The designed supply voltage and current are 3.3V and 1.9mA, respectively. As shown in Fig.4-21, the suppressions at 2.4V and 3.6V show differences from input power of -10dBm to 0dBm, however, these differences are less than 2dB. In the case of conversion gain, the differences are much smaller and only 1dB. In Fig.4-22, the same trend appears to suppression and conversion gain variation with the supply current of doubler core circuit. The conversion gains are more

sensitive to supply current than to supply voltage seen from Figs.4-21 and 4-22. In addition, the performance of fundamental frequency suppressions has a little fluctuation with supply voltage and current.

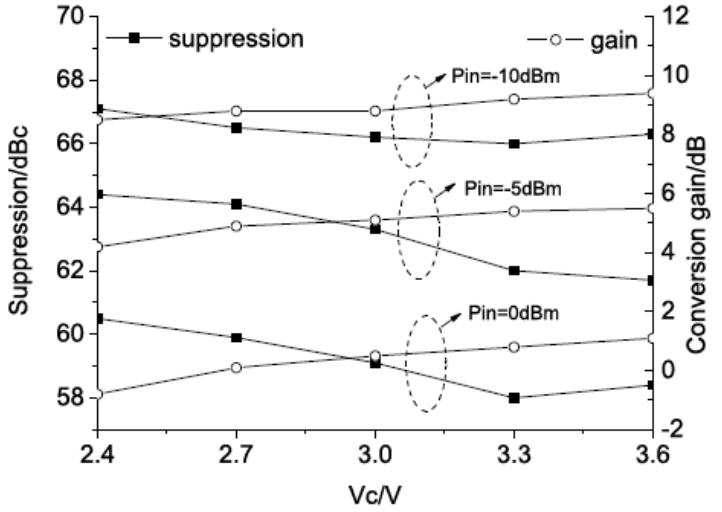


Fig.4-21 The dependence of fundamental suppression and conversion gain on supply voltage of doubler core.

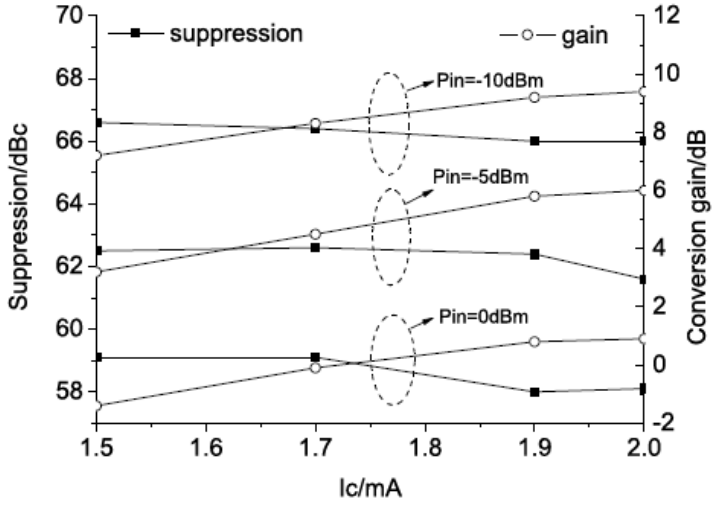


Fig.4-22 The dependence of fundamental suppression and conversion gain on supply current of doubler core.

TABLE 4-5

Design goal of frequency doubler

Items	Specifications	Measured results
Output frequency	26GHz	26GHz
Pin	-10dBm	-10dBm
Fundamental suppression	≥ 40dBc	66dBc
Conversion gain	≥ 0dB	9.2dB
P_{dc_core}	< 10mW	6.3mW
P_{dc}	< 150mW	137mW
Supply voltage	3.3V	3.3V

At last, a summary of measured results and comparison with the design goal is given in the TABLE 4-5. From this table, the measured results meets the requirements of the design goal. Hence, this frequency doubler can effective to be used in 26GHz sensor systems as expect.

4.4.2 Performance comparison

Based on the measured results, the high fundamental suppression performance operated in low input power has been verified. Using the FOM defined in equation 4-14, the performance comparison with other works can be obtained.

$$FOM = 20log_{10}(BW \times 100) + F.S - 10log_{10}\left(\frac{P_{DC}}{1mW}\right) \quad (4\text{-}14)$$

In this equation, BW is the frequency bandwidth. P_{DC} is DC power consumption of the frequency doubler. F.S denotes fundamental frequency suppression of the frequency doubler.

The used devices of compared frequency doublers are SiGe, GaAs and CMOS devices, respectively. The comparison conclusion is shown in TABLE 4-6 and the FOM with respect to input power is demonstrated in Fig. 4-23. The work in Chapter 3 and this work used the same technology but different topology, the former work focused on the broadband performance and latter one was designed to obtain high suppression. Compared with the work in Chapter 3, this work has a comparable FOM. Because the work in Chapter 3 has wide bandwidth and low power consumption although the suppression is less than this work. From this comparison, this

work has 31dB higher FOM compared with the one in [26] implemented in SiGe HBT. Although the doubler in [29] implemented in CMOS shows low input power and low DC power, the proposed work has higher FOM than the one in [29] due to the low suppression in [29]. Compared with the work in [27] and [28], this work exhibits high FOM and low input power. Hence, the frequency doubler proposed in this chapter shows higher FOM and low input power compared with doublers based-on GaAs technology and CMOS technology.

TABLE 4-6

Performance comparison with previous works

Ref.	Technology	Output frequency/GHz	Pin/dBm	FOM
This work	SiGe BiCMOS	25-27	-10	63
[26]	SiGe HBT	34.6-37.6	6	32
[27]	GaAs	30-32	5	20
[28]	GaAs	26-34	3	48
[29]	90nm CMOS	37.5-39	0	38

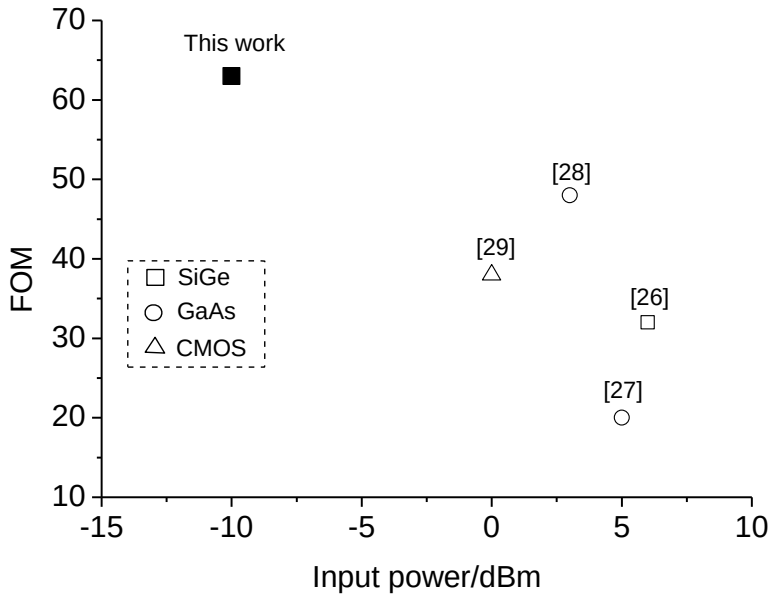


Fig. 4-23 High suppression frequency doubler comparison with other works.

4.5 Conclusion

In this chapter, a high fundamental suppression frequency doubler based on push-push circuit is proposed. The proposed frequency doubler is implemented in 0.25-μm SOI SiGe BiCMOS technology and measured on wafer.

In the fully differential push-push circuit, the input signal shows amplitude and phase imbalance, which results in the imbalance signal of fundamental frequency at the output of push-push circuit. According to the definition of the fundamental frequency suppression, the appearance of the fundamental frequency reduces the frequency suppression. In order to suppress the fundamental frequency at the output of push-push circuit, a LC series resonant circuit parallel with the differential output of push-push circuit shows low resistance at fundamental frequency. At the same time, the LC circuit has impedance matching between the push-push circuit and output buffer amplifier.

To verify the effectiveness of these techniques, a balanced frequency doubler has been fabricated in 0.25-μm SOI SiGe BiCMOS technology and measured on-wafer. A high fundamental frequency suppression of 66dBc has been achieved at 26GHz at an input power of -10dBm. The measured maximum conversion gain achieves 9.2dB at the input power of -10dBm. Hence, the frequency doubler proposed in this chapter shows higher FOM and low input power performance compared with doublers based-on GaAs technology and CMOS technology.

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Chapter 5 Conclusion and Future Work

5.1 Introduction

In this dissertation, high performance frequency doublers which are key component in the vehicular radar sensor have been researched and implemented. The subjects of broadband, high fundamental frequency suppression and high gain are devoted to in this dissertation. The conclusion of this dissertation will be described in the next sub-section.

5.2 Conclusions of this dissertation

In the Chapter 2, a compact broadband Marchand balun based on silicon technology is implemented and valued. Firstly, the passive baluns are reviewed in the section 2-2 in which the Marchan balun is a good candidate to be chosen due to wideband imbalance performance. Then, the cross-section of SiGe BiCMOS which is used to design balun is introduced in section 2-3. The balun design is described in section 2-4 in which a effective slow wave pattern ground structure is proposed. At last, a compact broadband balun is implemented and measured in section 2-5. this work achieves 1dB of amplitude imbalance and 10° of phase imbalance in the band of 20GHz-50GHz. In this band, the minimum insertion loss is 1.5dB. The VSWR which is less than 2 is from 23.4GHz to 39.1GHz. The chip core size is only 0.03mm^2. Compared with the balun using the conventional slot pattern ground structure, the 6-dB cuf-off frequency is extended by 6.6GHz. In this work, a compact size with broadband balun is implemented.

In the Chapter 3, a broadband frequency doubler IC based on silicon technology is imple-

mented and valued. Firstly, the broadband frequency doublers are reviewed in section 3-2 in which active doubler is selected due to high conversion gain and low input drive power. Then, the RF performance of SiGe BiCMOS used in this dissertation is introduced in section 3-3. The SiGe BiCMOS technology exhibits excellent RF performance indicating very suitable for millimeter-wave applications. In the section 3-4, an internal low pass filter technique is designed to achieve high suppression, and a pair of matching circuits is effective so that keep the doubler operates in low input drive power with high suppression. At last, the measured results exhibit better than 30dBc in a broad frequency band of 22-30GHz. In this work, the high FOM and wide bandwidth is achieved.

In the Chapter 4, a high suppression and high conversion gain frequency doubler IC based on push-push circuit is implemented and valued. Firstly, the frequency suppression techniques are reviewed in the section 4-2. Then, high suppression frequency doubler is proposed and designed. In the frequency doubler, a series LC resonator rejects the fundamental frequency at the output of the doubler core and matches with the input impedance of the output buffer simultaneously. At last, the measured results of the doubler shows fundamental frequency suppression as high as 66dBc and conversion gain of 9.2dB at an output frequency of 26GHz which exhibit comparable performance with the compounded technology. In this work, high FOM performance operating in low input power is obtained.

5.3 Future work

Now the utilization of frequency band for the vehicular radar sensor application includes 24GHz band, 26GHz band, 77GHz band and 79GHz band. The 26GH band SSR now is prepared to be in production and will be expected to be available in 2-3 years in Japan [1]. As the f_t of device increasing, the future frequency band for the automotive radar sensor maybe higher than 100GHz [2]. A clear trend in vehicular radar sensor applications has been the push towards higher integration and multi-band (or broadband) operation, in order to enable low-cost high-functionality consumer devices [3][4][5]. The broadband millimeter-wave frequency doubler will be researched based on the work of Chapter 2 in the future.

Applications at microwaves, millimeter-waves and even in the THz gap are flourishing due to the ever increasing speed of CMOS devices in ultra-scaled nodes, such as 45-nm [6] and

65-nm [7]. When designing frequency multipliers in CMOS, operating in millimeter-wave in particular, they are suffered from low-conversion gain, or even loss, large input capacitance, and single-ended output. For these reasons the principle of frequency multiplication did not find extensive application to date. The adoption of injection locking mechanism in the frequency multiplier designs provides several advantages over conventional structure, especially within the millimeter wave range where inductors and transformers have higher Q and smaller sizes [8][9]. Specifically, the output power of an injection-locked frequency multiplier is mainly determined by the bias current instead of the input power in a traditional frequency multiplier, therefore large output power can be obtained with low input power level. Furthermore, the injection-locking structure can achieve low phase noise and high harmonic rejection. The low DC power, high output power and high suppression frequency multiplier based on injection locking mechanism using state-of-the-art RF CMOS technology (such as 65-nm) for millimeter-wave applications will be researched in the future.

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