Study on Wideband Voltage Controlled Oscillator and High Efficiency Power Amplifier ICs for Wireless Communications

LIU,Qing

Graduate School of Information, Production and Systems
Waseda University

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Abstract

As the growth in the wireless communication systems, the need of the high speed, high transmission data rate becomes critical issue to satisfy the wireless communication application for daily life. And the necessary of high integration of the baseband circuit and radio frequency analog transceiver in one chip makes the CMOS the most important process for Integrated Circuit (IC) design. However, it is a challenge work to design a high quality high speed Radio Frequency Integrated Circuit (RFIC) by CMOS process because of its low quality factor on-chip inductor, large parasitic capacitance and large substrate noise. Recent years, many researches were carried out and many techniques were reported to deal with these defects in design high performance RFIC in CMOS process. Among all of the components constituting the RFIC, Power Amplifier (PA) and Voltage Controlled Oscillator (VCO) are the most critical parts and it is quite significant to promote their performance.

VCO is the heart of the frequency synthesizer, the performance of the VCO has large effect on phase lock loop (PLL) and the quality of transceiver. For system with high dynamic range requirements, the VCO must achieve a corresponding spectral purity. Thus, the VCO should have a low harmonic frequency, especially, a low phase noise, which has important effect on Signal to Noise Ratio (SNR). VCO in a high speed communication system is far more challenge because of the requirement of wideband oscillation frequency. In this thesis, an ultra-wideband VCO is designed. A novel tunable switching inductor is proposed to enlarge the oscillation frequency, and switching AMOS varactor bank is used to decrease the VCO gain and improve the phase noise. The chip was fabricated in 0.13 μm CMOS process and the experimental results demonstrate a wideband of 92.6% from 1.20 GHz to 3.27 GHz with a phase noise of -120 dBc/Hz at 1 MHz offset from the 3.1 GHz carrier is obtained.

PA is the key component in the transceiver and it consumes above 60% dc power

of the whole communication systems. Thus, the efficiency of the CMOS PA also affects the efficiency of the transceiver. However, in the modern wireless communication systems, the linear modulation is usually adopted for the high data rate and high speed communication systems, such as complex vector modulations. In this kind of modulations, the signal has a very high Peak to Average Ratio (PAR) and usually the PA should be backed off from output 1 dB Compression Point (P1dB) to get the desired specifications, which cause the efficiency of PA is much lower than the maximum efficiency near the output P1dB. Therefore, the linearization technique is developed for PA and it can decrease the back-off dBs from P1dB with the desired specifications, thus, increase the efficiency of the PA. In this thesis, a novel multi-cascode linearized CMOS PA is presented with post-linearization technique for 5.8 GHz Dedicated Short Range Communication (DSRC) applications. It was fabricated in 0.13 μm CMOS process to verify the effectiveness of the proposed technique. Experimental results show a Third-order Intermodulation Distortion(IMD) improvement of 5.5 dB over large output power range and the maximum improvement of 10 dB with a high Power Added Efficiency (PAE) of 32% at the output 1 dB gain compression point (P1dB).

A CMOS Class-G supply modulation for polar PA with high average efficiency and low ripple noise is also proposed. In the proposed Class-G supply modulation, the parallel supply modulations which are controlled by switch signals are utilized for low power and high power supplies to increase the average efficiency. A low dropout (LDO) is utilized to suppress the delta-modulated noise and provide a low ripple noise power supply. The proposed supply modulation was designed with 0.13 μm CMOS process. The simulation results show that the proposed supply modulation achieves a maximum efficiency of 85.1%. It achieves an average efficiency of 29.3% and a 7.1% improvement compared with the conventional supply modulations with Class-E power amplifier. The proposed supply modulation also shows an excellent spurious free dynamic range (SFDR) of -73 dBc for output envelope signal.

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Dedicated to my father Zhi-Ping Liu,
my mother Wen-Xiu He.

Chapter 1

Introduction

1.1 Background

With the fast development of the wireless communications, wireless communications has been used in every field of daily life. Explosive growth in the wireless market makes wireless communications the center of the industrial development in the 21^{th} century.

In February 1980, a family of IEEE (Institute of Electrical and Electronic Engineers) 802 standards dealing with local area networks and metropolitan area networks was established [1]. These standards is maintained by the IEEE 802 LAN/MAN Standards Committee (LMSC) and an individual Working Group provides the focus for each area [2].

In the 1980s, cellular phones were first introduced. And the early systems became known as first generation (1G) mobile phones, such as Advanced Mobile Phone Service (AMPS), Nordic Mobile Telephone (NMT), and Radio Telefono Mobile Integrato (RTMI). In the 1990s, second generation (2G) mobile phone systems such as Global System for Mobile Communication (GSM) and IS-95 (CDMA) began to widely be used. And in Japan, the Personal Digital Cellular telecommunication system (PDC) is standardized as the digital mobile communication system. NTT DoCoMo has commercially operated the PDC system to provide voice, data, and facsimile communication service sine March 1993 [3]- [4]. Before the widely spread of the third generation (3G) mobile phone systems, 2.5G systems such

as General Packet Radio Service (GPRS), Code Division Multiple Access (CDMA) and Enhanced Data rates for GSM Evolution (EDGE) were developed as a transition from the second generation to third generation. In 2.5G, it provide a high speed of data and it can provide some benefits of third generation systems and also it is compatible with the second generation network.

The availability of low-cost digital circuits paved the way to adopting advanced digital modulation schemes. Due to the increased level of usage, service providers started to add more base stations which led to higher density and smaller size of cellular sites. From 2G systems, International Telecommunication Union (ITU) specifies the International Mobile Telecommunications-2000 (IMT-2000) as a generation of standards for mobile phones and mobile telecommunications services. Application services include wide-area wireless voice telephone, mobile Internet access, video calls and mobile TV, all in a mobile environment. Compared to the older 2G and 2.5G standards, a 3G system must provide peak data rates of at least 200 kbit/s according to the IMT-2000 specification. Recent 3G releases, often denoted 3.5G and 3.75G, also provide mobile broadband access of several Mbit/s to laptop computers and smartphones [2], [5],[6] and [7]. Universal Mobile Telecommunications System (UMTS) and Code Division Multiple Access 2000 (CDMA2000) are the representation of the 3G mobile telecommunications technologies. UMTS, which also being developed into a 4G technology, is specified by 3GPP and is part of the global ITU IMT-2000 standard. The most common form of UMTS uses Wideband Code Division Multiple Access (WCDMA) as the underlying air interface but the system also covers Time Division CDMA (TD-CDMA) and Time Division-Synchronous Code Division Multiple Access (TD-SCDMA) with a peak data rate of 2 Mbps [8].

In less than twenty years, mobile phones have gone from rare and expensive consumption to now every people has their own mobile phones as every family has their own land-line telephones. By the end of 2005, the global mobile phone market grew to 2 billion subscribers. Yet this market is still growing.

Concurrent with the developments of mobile phones, the other wireless commu-

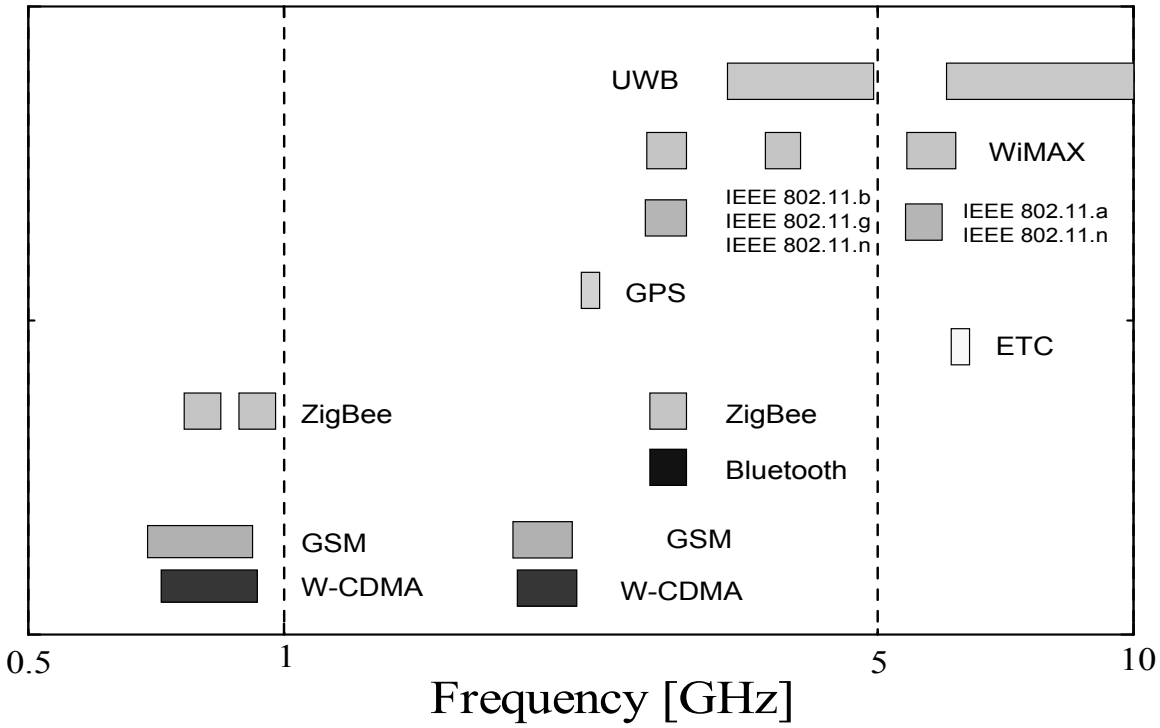


Figure 1.1: The main wireless communication systems.

nications such as ZigBee, Bluetooth, Global Positioning System (GPS), Worldwide Interoperability for Wireless Access (WiMAX), Ultra Wide Band (UWB) and Wireless Local Area Network (WLAN) are also growing explosively. The main wireless communications is shown in Figure 1.1. ZigBee is focused on control and automation, While Bluetooth is focused on connectivity between laptops, PDAs, and the like, as well as more general cable replacement [9]. The frequency range of UWB is from 3.1 GHz to 10.6 GHz and it supports short distance communication with a data rate above 100 Mbps. And the UWB is widely used in wireless Universal Serial Bus (USB) [10]. The most well-known systems are probably applications related to Wireless Local Area Network (WLAN). The WLAN worldwide service revenues are projected to reach 9.5 Billion dollar by 2007 (source: Alexander Resources). WLAN links two or more devices using some wireless distribution method

(typically spread-spectrum or OFDM radio), and usually providing a connection through an access point to the wider internet. This gives users the mobility to move around within a local coverage area and still be connected to the network [2], [11]. Wireless LAN is promoted by Wi-Fi Alliance which is a trade association technology and certifies products if they conform to certain standards of interoperability [12]. The original 802.11 standard allowed a maximum channel bit rate of only 2 megabits per second, while the current 802.11b standardcommonly known as Wi-Fi supports an 11 Mbps maximum rate. However, the widespread deployment of 802.11a and 802.11g standards, which allow a bit rate of up to 54 Mbps, pave the way for new types of mobile applications, including mobile commerce transactions and location-based services [13]. And the latest IEEE802.11n system offers enhanced 114 Mbps data rates, greater spectral efficiency, and better quality and robustness compared with the existing IEEE802.11a/b/g systems and it will create a demand for seamless connectivity between a growing array of multimedia and entertainment platforms [14].

The development trends of the mobile telecommunications systems and the other wireless communication systems all show the fast growth in high speed and high data rate communication ability. This need makes the system design more difficult and challenge.

With the developments in the wireless communication industry, there are several tremendous advantages in semiconductor technologies. Among them, GaAs HBT, GeSi HBT and Si CMOS is quite prevalent and the most significant progress made is CMOS technologies. The remarkable characteristic of CMOS transistors is that their speed increase, while the consume less power per function in digital circuits, and low cost duo to the decreased size and its Si materials. The digital circuit is nearly not impossible to be integrated by GaAs HBT or GeSi HBT with the merit of CMOS process. In addition, the integration of the RFIC in CMOS process make it the most widely used semiconductor technologies which can fulfill the integration of the whole system on one chip [15] to [17].

1.2 Motivation and Research Objective

A typical wireless transceiver architecture is shown in Figure 1.2. The position of the VCO is as shown in this figure. The VCO is a key part with the most challenging aspects in PLL and it is controlled by the signal from the filter to provide an appropriate frequency reference to operate.

Commonly, in the cellular phone and WLAN, the bandwidth is quite narrow and design a VCO with low phase noise is not so difficult. With the development of the wireless communications, current trends clearly indicate a growing customer demand for multi-band multi-standard transceivers [18] and faster data rates [19] to [21]. The high data rate is achieved by using a wideband channel bandwidth. Applications such as the 3.1 to 10.6 GHz frequency range UWB system, the wideband VCO is necessary to cover a wideband range from 3.1 to 10.6 GHz [22] to [23]. Furthermore, the future cognizant radios which can sense unused or less crowded portions of the spectrum and reconfigure itself to operate there. These systems have a wideband in order to raise the utilization of the spectrum, therefore, requiring a wideband frequency synthesizer as well. Hence, wideband VCOs are becoming important in those applications.

Design wideband VCO is quite challenge in CMOS process because of the large parasitic capacitance. These parasitic capacitance exists in crossing couple NMOS or PMOS transistors and switches in a capacitor bank, which is commonly used for a wide turning ratio of capacitance. Between these two kinds of parasitic capacitors, the parasitic capacitor of switches in capacitor bank seriously detriments the turning ratio of the capacitance, thus, limited the turning range of the oscillation range. To enlarge the turning range, the new technique should be proposed to overcome the drawbacks in a conventional VCO.

The PA is the last active building block in the transmitter chain as shown in Figure 1.2. The most important function of a PA is to amplify the signal to a level high enough that it can travel through the air to the receiver and the signal can be correctly demodulated in the receiver. Nowadays, there is a trend of integrating all the components in

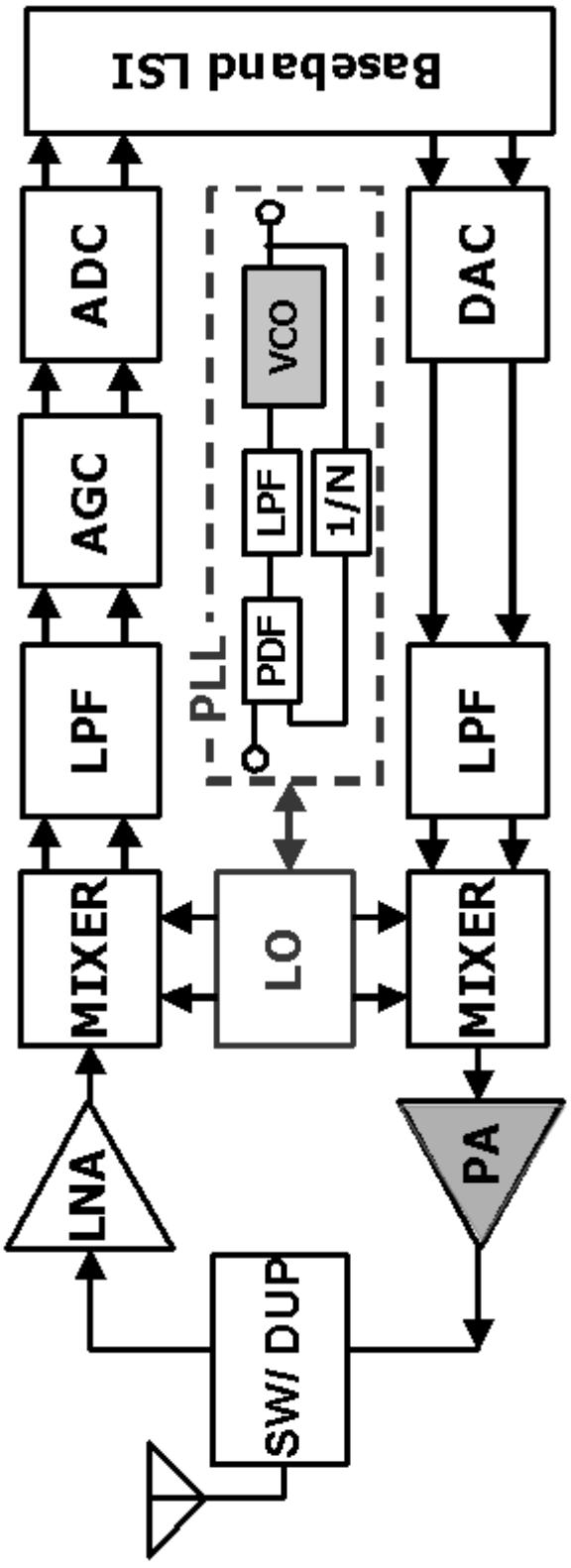


Figure 1.2: A typical wireless transceiver architecture.

a wireless communication system on a single chip [24] and [25] in CMOS process. However, there is still one component PA that is hard to integrated with other system in CMOS process because the drawback of the CMOS process. Today, almost all PAs in market are manufactured with III-V compound semiconductors. This is necessary because high output power and high power efficiency are required PA specifications in various applications. The III-V compound semiconductors offers a much better efficiency and linearity, and it also offers a higher output power compared with CMOS semiconductors because of the merit of the III-V compound process. This is very difficult to satisfy those requirements with CMOS technologies. In CMOS technologies, the poor quality value of the inductors cause large loss in the output matching network, which decrease the efficiency of PA. Further more, the lossy substrate of CMOS process also cause power loss in route and between the connection of MOS transistors, which also impairs the efficiency of PA. And up to now, almost all of the PA reported in CMOS has a low efficiency about 25% at P1dB when the operating frequency is above 5 GHz. The large variation of the parasitic capacitance in CMOS process also detriments the linearity of PA and the low breakdown drain to source voltage limited the output power capacity below 1 W. Because of all these drawbacks, the usage of the CMOS PA is largely limited in commercial product. However, due to the high manufacturing cost of the III-V technologies, and the impossible of integration of the whole system to realize system-on-chip (SoC) by III-V technologies, there is a growing interests of research on CMOS PA.

The first CMOS RF PA that could deliver hundreds mW power was reported in 1997, implemented in a single-ended configuration with a 0.8 μm CMOS technology [26]. And the first CMOS RF differential amplifier that could deliver over 1W at GHz range was reported in 1998, implemented with a 0.35 μm CMOS technology [27]. After that, there have been quite a few publications on CMOS RF PAs [28] to [32]. They all rely on off-chip components to implement low-loss impedance transformation network. After several years research of the CMOS PA, the fully integration of CMOS PA was reported in [33] and [34].

In the modern wireless communication systems, in order to get a high speed and

high data rate, the linear modulation with high PAR is used. The CMOS PA has to work in a back off state to get the desired specification. With a back-off state, the PA works with a poor efficiency. Commonly, the PA dominates the power consumption of the entire transceiver. Therefore, improving the PA power efficiency also improves the efficiency of the whole wireless communication systems. And this is especially important in portable devices such as cell phones, PDAs demanding low power systems for a longer battery life.

In light of the above trends, the main goals of this thesis are to design high performance wideband VCO and high linearity and high efficiency PA to satisfy the growth in the high speed and high data rate modern wireless communication. With new design techniques, the VCO and PA show an improved performance in CMOS process compared with the conventional prototypes.

1.3 Contribution of the Thesis and Its Structure

The main objective of this research is to promote the performance the key component VCO and PA in the wireless communications. The research work can be divided into two significant parts, the first part focus on the design of a wideband VCO with a tunable switching inductors. This technique is further described in Chapter 2. To demonstrate the design techniques, an experimental prototype wideband VCO was designed. The prototype wideband VCO can cover a wide frequency band, in which many popular wireless communications are located. The second part focus on the design of a high linearity and high efficiency PA. A post-linearization is proposed dedicated for cascode architecture which usually used in CMOS PA to boost the output power capacity. To demonstrate the design techniques, an experimental prototype was designed for 5.8 GHz Dedicated Short Range Communication (DSRC) applications. This technique is further described in Chapter 3. A Class-G supply modulation PA is also design for high efficiency, the simulation is carried out to verify the effectiveness of the proposed Class-G supply modulation PA. This technique is further described in Chapter 4.

The primary contributions of this research are:

♦ A new technique was proposed with tunable switching inductors, the VCO with this technique can get a much more wideband turning range. The proposed tunable switching inductors are implemented based on transformers. By changing the equivalent inductance in the secondary, the effective inductance of the transformer is changed. The equivalent circuit of the transformer based tunable inductor is derived from the transformer equivalent T-model and the principle analysis is also given in this research. And many practical implementation issues are discussed.

♦ To verify the proposed technique, firstly, this wideband VCO was designed and optimized in ADS. Then, the wideband VCO was fabricated by 0.13 μm CMOS process and the prototype was measured fully on-chip. The proposed wideband VCO exhibits a frequency tuning range as high as 92.6% from 1.20 GHz to 3.27 GHz at an operation voltage of 1.5 V. The measured phase noise of -120 dBc/Hz and -123 dBc/Hz at 1 MHz offset from the 3.1 GHz and 1.2 GHz, respectively, carrier is obtained.

♦ A multi-cascode post-linearization technique for CMOS cascode PA is proposed in this work and this architecture can minimize the transconductance distortion in the cascode stage, thus, linearize the cascode PA. The transconductance distortion is also analyzed in this work in order to search this effective technique and this analysis shows the transconductance distortion canceling can be achieved with only an additional common-gate transistor as a linearizer. It also can be concluded that this linearizer does not sacrifice efficiency because of its closed to Class-C operation condition.

♦ To verify the proposed technique, firstly, this high linearity and high efficiency PA was designed and optimized in ADS. Then, the prototype PA was fabricated by 0.13 μm CMOS process and measured fully on-chip. With a low supply voltage of 2.0 V, the

prototype PA produces an output power of 1 dB compression point (P1dB) of 17.3 dBm and Power Added Efficiency (PAE) of 32 % at the P1dB. The improvement in IM3 of 6 dB over large output power range and the maximum improvement of 12 dB are achieved. The measured Output Third Order Intercept Point (OIP3) is as high as 27.3 dBm.

♦ In order to increase the efficiency of the PA, a new architecture of Class-G supply modulation PA is proposed. In this architecture, hybrid amplifier is used for high power supply and LDO is used for the low power supply. This architecture has a high efficiency at high output current and low output current. It also has good SFDR at low output current comparing with the conventional supply modulation.

♦ In order to suppress the noise from the switching PA, a twice noise filtering technique is proposed to suppress the noise of switching PA. The first noise filter is implemented by the low output impedance of the Class-AB amplifier as in conventional supply modulation. The second noise filter consists of the LDO with a novel bias technique for a fixed dropout voltage to make the LDO with high PSRR. With this twice noise filtering technique, the noise is largely suppressed.

♦In order to track the current accurately for the switching PA, an accurate current detector is proposed. The proposed current detector overcomes the inaccuracy introduced by the channel length modulation in conventional current detector. It can accurately copy the current from Class-AB amplifier output stage with rail-to-rail output range within 0.4% error.

♦ To verify the proposed technique, the proposed Class-G supply modulation PA and conventional supply modulation PA are simulated. the simulation results confirms that it achieves an average efficiency of 29.3% and a 7.1% improvement compared with the conventional supply modulations with Class-E PA. The proposed supply modulation also shows

an excellent spurious free dynamic range (SFDR) of -73 dBc for output envelope signal.

This dissertation is organized into four relatively independent parts, including

Chapter 2: A Wideband LC VCO IC

Chapter 3: A High Linearity and High Efficiency PA IC

Chapter 4: A CMOS Class-G Supply Modulation for Polar PAs with High Average Efficiency and Low Ripple Noise

Chapter 5: Conclusions and Future Work

Chapter 2 focus on the wideband VCO design. A wideband VCO design with variable inductors are introduced in this paper. The prototype of the wideband VCO is also fabricated and measured. The measured result and the result analysis are also given in this chapter.

Chapter 3 focus on the high linearity and high efficiency PA design. To overcome the drawbacks of CMOS PA, a new post-linearization technique is introduced in this chapter. The prototype of the PA is also fabricated and measured. The measured result and the result analysis is also given in this chapter.

Chapter 4 focus on the high efficiency Class-G Supply Modulation PA design. To increase the average efficiency, a new Class-G Supply Modulation PA is introduced in this chapter. The prototype of the PA is simulated to demonstrate the improvement in average efficiency.

Chapter 5 provides the conclusion and future work of this thesis.

Chapter 2

Novel Wideband LC VCO IC

2.1 Overview

VCO is the key part in PLL, and the performance of VCO in terms of phase noise, tuning range and turning range also determines the performance of PLL, and hence, determines many of the basic performance characteristics of a transceiver. There is a trend towards wideband higher data transfer rates in wireless communication system as shown in Figure 2.1. And this trend demands very wide tuning range and low phase noise performance of VCO [35]-[39]. This trend also generates an interest of wideband VCO design. Whereas relaxation oscillators easily achieve very wide tuning range (i.e. 100% or more), their poor phase noise performance limited them in most of todays wireless communication applications. Because the LC VCO has a high qualify factor of LC tank, the performance of the LC VCO is much better compared with the relaxation oscillators. Because of this merit, the LC VCO has been used for many narrowband wireless transceivers. Compared with the relaxation oscillators, the LC VCO promises a broad application in wideband VCO design and there is a growing interest in extending tuning range of LC VCO. Recently, several wideband CMOS LC VCOs have been demonstrated using a variety of techniques [36]-[39]. Though, the accumulation-type MOS varactors support a very wide tuning range and their Q is sufficiently high that good phase noise performance can be maintained [37], the overall

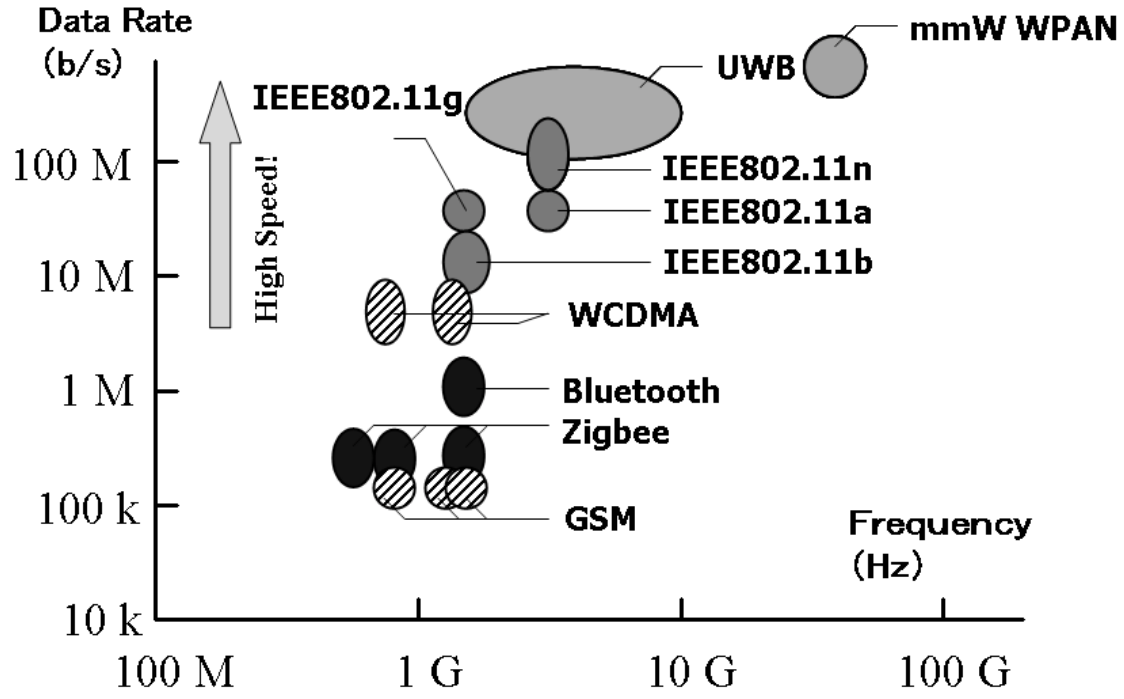


Figure 2.1: The trend of the wireless communication systems.

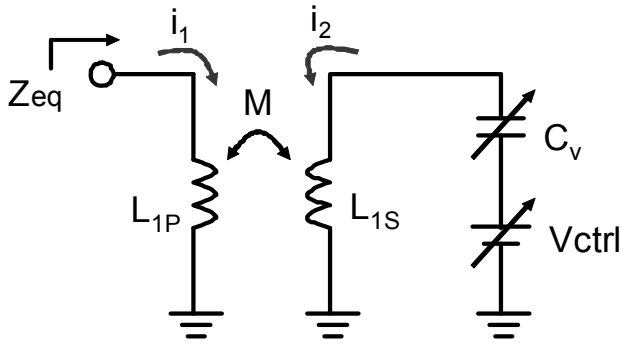
phase noise performance is also highly dependent on the tuning sensitivity of the VCO, since noise from preceding stages of the frequency synthesizer is inevitably injected onto the VCO control input. Thus, on the other hand, decrease the tuning sensitivity of the VCO is critical to improve the phase noise performance. And there are also some reports about decreasing the tuning sensitivity and increasing the bandwidth of the VCO [40] - [42].

2.2 Wideband LC VCO Design

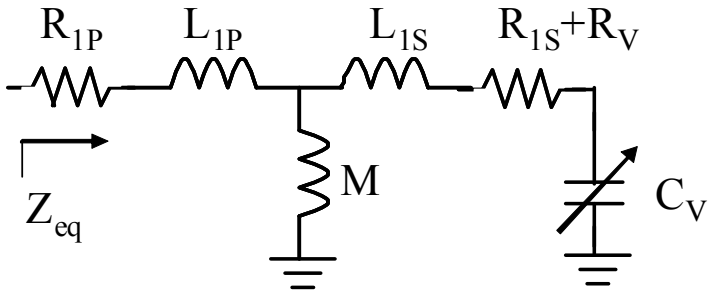
This wideband VCO is designed by 0.13 μm CMOS process, the target of the wideband VCO is shown in Table 2.1.

Table 2.1: Wideband VCO Target

Frequency Bandwidth	1.2 GHz – 3.2 GHz
Voltage	1.5 V
Turning Range	$\geq$ 90 %
Phase Noise @ 1 MHz	$\leq$-115 dBc@ 3.1 GHz and -120 dBc@ 1.2 GHz



(a).



(b).

Figure 2.2: (a) Schematic of the transformer-based variable inductor. (b) The equivalent circuit of the variable inductor.

2.2.1 Transformer-based Switched Variable Inductors Design

The proposed transformer-based switched variable inductors and its equivalent circuit is shown in Figure 2.2. In the Figure 2.2 (a) L_{1P} and L_{1S} are the primary and

secondary inductances, respectively. M is the mutual inductance, and i_1 and i_2 are the current through primary and secondary windings, respectively. C_V is the AMOS varactor for changing the capacitance and consequently changes the effective inductance L_{eq}, which is the inductance looking into the primary inductor of the transformer. C_V is controlled by the control voltage V_{ctrl} . The equivalent circuit is shown in Figure 2.2 (b). R_{1P} and R_{1S} are the primary and secondary parasitic resistance, respectively, and R_V is the parasitic resistance of the varactor. The equivalent impedance Z_{eq} from the circuit is derived to be:

$$Z_{eq} = R_{1P} + j\omega L_{1P} + j\omega L_{1P} \| (R_{1S} + R_V + j\omega L_{1S} - j(\omega C_V)^{-1}) \tag{2.1}$$

where ω is the angular frequency. After arranging the Equation 2.1, the equivalent impedance Z_{eq} is expressed as:

$$Z_{eq} = R_{1P} + j\omega L_{1P} + \frac{\omega^2 M^2}{R_{1S} + R_V + j\omega L_{1S} - j(\omega C_V)^{-1}} \tag{2.2}$$

The equivalent L_{eq} is derived from Equation 2.2 to be:

$$L_{eq} = L_{1P} - \frac{\omega M^2 [\omega L_{1S} - (\omega C_V)^{-1}]}{(R_{1S} + R_V)^2 + [\omega L_{1S} - (\omega C_V)^{-1}]^2} \tag{2.3}$$

if $R_V + R_{1S}$ is small enough and Equation 2.2 can be approximated as:

$$L_{eq} \approx L_{1P} + \frac{\omega M^2}{(\omega C_V)^{-1} - \omega L_{1S}} \tag{2.4}$$

then equation Equation 2.4 can be rearranged to be:

$$L_{eq} \approx L_{1P} + \frac{\omega^2 M^2 C_V}{1 - \omega^2 L_{1S} C_V} \tag{2.5}$$

the angular frequency ω is decided by oscillation frequency of the VCO and it can be expressed by:

$$\omega = \sqrt{\frac{1}{L_{eq} C_{tal}}} \tag{2.6}$$

where C_{tal} is the total capacitance of the LC-tank and MOS transistors. Replace ω in Equation 2.5 with Equation 2.6, the Equation 2.6 can be rewritten by:

$$L_{eq} \approx L_{1P} + \frac{\omega^2 M^2 C_V}{1 - L_{1S} C_V / L_{eq} C_{tal}} \tag{2.7}$$

In Equation 2.7, the second part can be either positive or negative. This is a double-tuned transformer with only one driving port [43]. The resonator exhibits a two resonance-points characteristic with different signal levels. For the sake of simplicity, assume that the transformer is fully balanced, which means $L_{1S} = L_{1P} = L$, $R_{1S} = R_{1P} = R$ and $C_{tal} = C_V = C$. The two resonance frequencies as a function of the tank parameters is described as:

$$\varpi_{1,2} = \frac{1}{\sqrt{LC(1 \pm k)}} \tag{2.8}$$

The quality factor at each resonance point is given by:

$$Q_{1,2} \cong \frac{1}{R}\sqrt{\frac{L}{C}(1 \pm k)} \tag{2.9}$$

The amplitude at the two resonance-points is described as:

$$V_{1,2} = \frac{i_1(1 \pm k)L}{2RC} \tag{2.10}$$

In order to avoid the unintentional occurrence of this upper resonate mode in the VCO, in the design, C_{tal} is much larger than C_V and $L_{eq}C_{tal}$ is much larger than $L_{1S}C_V$. Thus, Equation 2.6 can be approximated as:

$$L_{eq} \approx L_{1P} + \omega^2 M^2 C_V \tag{2.11}$$

However, it shows the property of inductance only when the capacitance C_V is small. When the capacitance C_V becomes large, oscillation of the secondary transformer starts up. The image part becomes infinite and if the capacitance C_V continue to become large, the transformer shows a property of capacitance. And near the oscillation point, the Q-value also deteriorates. Thus, commonly, the small C_V is used as shown in the shadow in Figure 2.3.

Equation 2.11 reveals the principle of the proposed transformer-based variable inductor. The effective inductance is nearly linear with C_V and it can be changed by tuning C_V of the varactor. Thus, a continuous inductance can be obtained by turning the

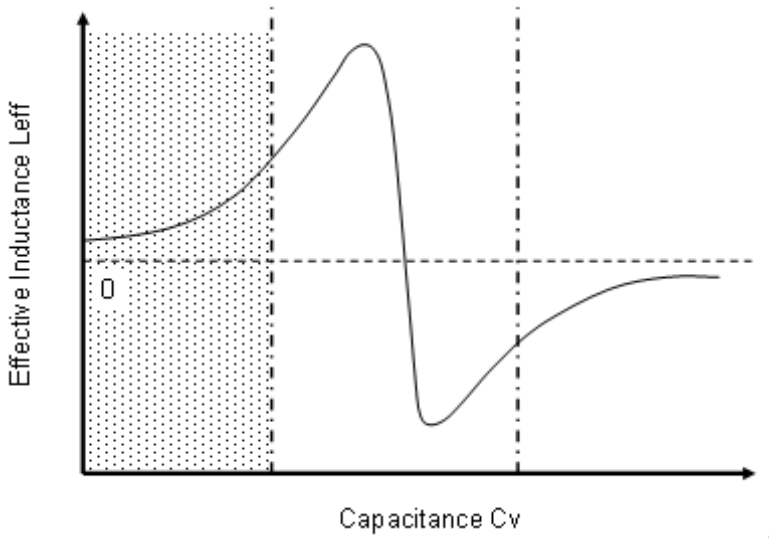


Figure 2.3: The operational region of the transformer.

capacitance of the varactor C_V . In addition, the range of the tuning voltage is the same with the control voltage of the AMOS varactor bank. Therefore, the same control voltage can be used for the varactor in the AMOS varactor bank and in the variable inductors. And in the PLL system, they can share the same control voltage from the output of the PLL filter.

The equivalent resistance R_{eq} can also be obtained from Equation 2.2 as:

$$R_{eq} = R_{1P} + \frac{\omega^2 M^2 (R_{1S} + R_V)}{(R_{1S} + R_V)^2 + [\omega L_{1S} - (\omega C_V)^{-1}]^2} \tag{2.12}$$

If $R_V + R_{1S}$ is negligible, this expression can be approximated as:

$$R_{eq} = R_{1P} + \frac{\omega^2 M^2 (R_{1S} + R_V)}{[\omega L_{1S} - (\omega C_V)^{-1}]^2} \tag{2.13}$$

In the same way as Equation 2.7 to Equation 2.11, the Equation 2.13 can be approximated as:

$$R_{eq} = R_{1P} + \omega^4 M^2 C_V^2 (R_{1S} + R_V) \tag{2.14}$$

From Equations 2.3 and 2.14, the quality factor of the equivalent inductor can be obtained as:

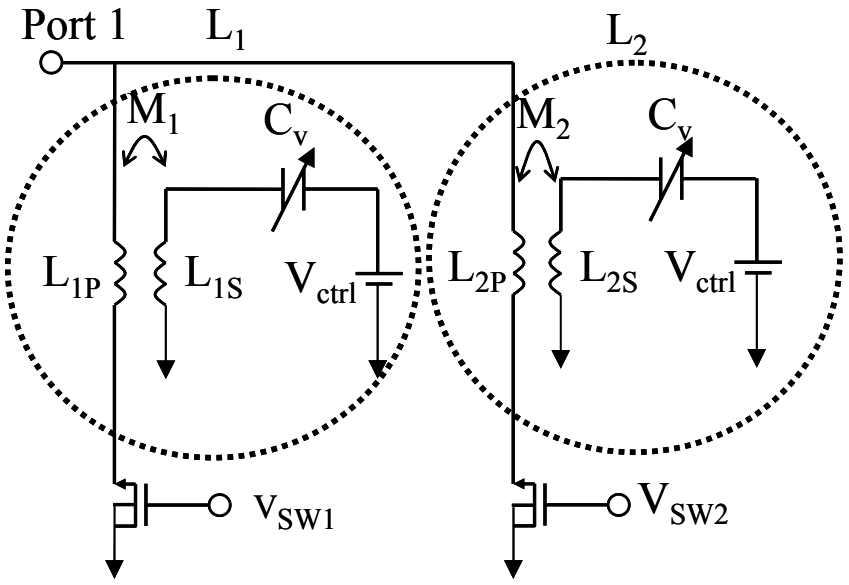


Figure 2.4: Schematic of the proposed transformer-based switched variable inductor set.

$$
\begin{aligned}
Q &= \frac{\omega L_{eq}}{R_{eq}} \\
&= \omega \left\{ L_{1P} - \frac{\omega M^2 [\omega L_{1S} - (\omega C_V)^{-1}]}{(R_{1S}+R_V)^2 + [\omega L_{1S} - (\omega C_V)^{-1}]^2} \right\} \\
&\div \left\{ R_{1P} + \frac{\omega^2 M^2 (R_{1S}+R_V)}{(R_{1S}+R_V)^2 + [\omega L_{1S} - (\omega C_V)^{-1}]^2} \right\} \\
&\approx \frac{\omega L_{1P} + \omega^3 M^2 C_V}{R_{1P} + \omega^4 M^2 C_V^2 (R_{1S}+R_V)}
\end{aligned} \tag{2.15}
$$

In this work, two transformer-based variable inductors (L_1 and L_2) are connected in parallel with two NMOS for switching the inductors. The schematic of the proposed transformer-based switched variable inductor set is shown in Figure 2.4. The two variable inductors have different effective inductance (L_{eq}). Thus, coarse tuning of inductance can be realized by switching the two variable inductors and the fine turning of the inductance is by turning the varactor. To avoid the oscillation region as shown in Figure 2.3, the small size of the varactor is chosen for turning the inductance.

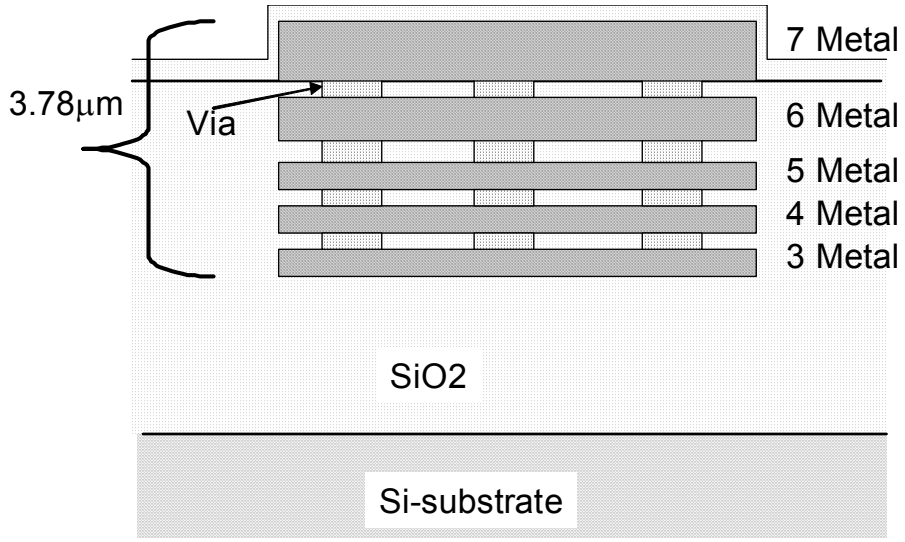
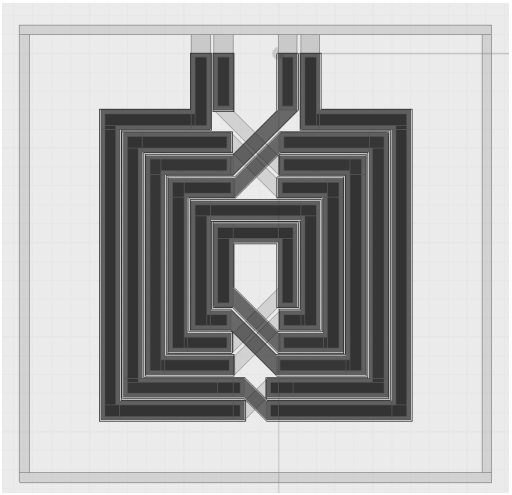


Figure 2.5: The metal layers in the CMOS process.

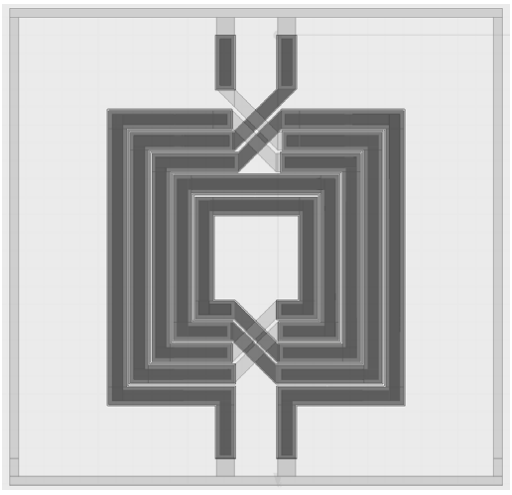
To decrease both the parasitic on-resistance and off-capacitance of the switching circuit, the NMOS switching connecting series with the inductors have the minimal gate length of 0.11 μm and a total gate width of 600 μm, which provide a good compromise between parasitic on-resistance and off-capacitance.

There are 7 metal layers in this 0.13 μm CMOS process, and the top metal are quite think. The loss is very large if only use the top metal. Thus considering the loss in the metal and parasitic capacitance between the substrate, the top five metals are used for the transformer as shown in Figure 2.5. Composed by the top five layers, the metal thickness for the transformer is 3.78 μm.

The transformers are designed with 3D Electronic Magnetic software Ansoft HFSS. The models of the two transformers are shown in Figure 2.6 (a) and Figure 2.6 (b). To enhance the effective coupling factor k, multiple circles coupling are used to decreasing the area of the transformers. The primary inductor of L_1 is a double-turn 10-μm-wide coil with a radius of 140 μm. The secondary inductor of L_1 is a triple-turn 10-μm-wide coil with a radius of 164 μm. The primary inductor of L_2 is a double-turn 10-μm-wide coil with a



(a).



(b).

Figure 2.6: (a) The layout of the transformer D116N2W10. (b) The layout of the transformer D140N2W10.

radius of 116 μm. The secondary inductor of L_2 is a quadruple-turn 10-μm-wide coil with a radius of 164 μm. The width of 10 μm chosen for the metal layers also provide a good compromise between the metal loss and parasitic capacitance between the substrate. The S-parameter is also obtained in HFSS. The effective coupling factor is got by Z-parameter. The inductance value, quality factor and Z-parameter are calculated from the S-parameter.

Then calculate the inductance of the primary stage of transformer, the secondary stage of transformer is open. And the primary stage of transformer is open, when calculate the inductance of the secondary stage of transformer. Then, the inductance is obtained by the following expression:

$$L_p = \frac{Im(Z_{11})}{Re(Z_{11})} \tag{2.16}$$

The inductance is variable with the frequency as shown in Figure 2.7. The inductance of the primary stage of transformer D116N2W10 is from 0.45 nH to 0.6 nH and the inductance of the secondary stage of it is from 1.6 nH to 2.5 nH. The inductance of the primary stage of transformer D140N2W10 is from 0.57 nH to 0.68 nH and the inductance of the secondary stage of it is from 1.15 nH to 1.3 nH.

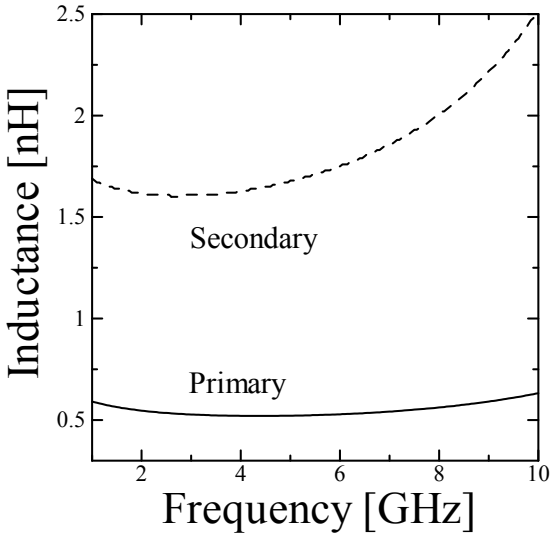
The Q-factors from the primary stage inductor of transformer is very important like that of the inductors in the LC-tank in a conventional VCO. When test the Q-factors from the primary stage inductor, the secondary of the transformer is open. The Q-factors values is calculated as that in a inductor:

$$Q_p = \frac{Im(Z_{11})}{\varpi} \tag{2.17}$$

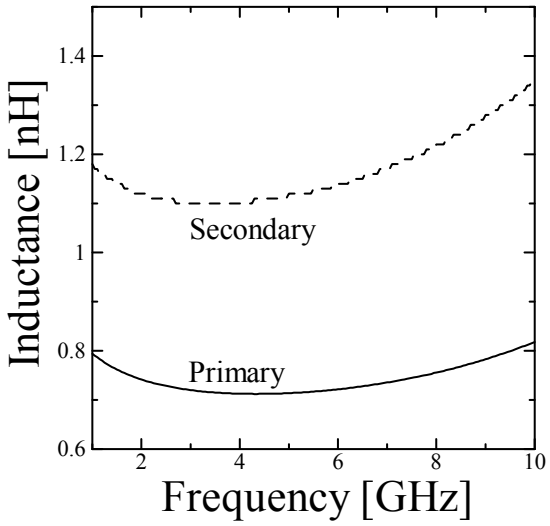
The simulation Q-factors from the primary stage inductor L_1 of D116N2W10 and L_2 of D140N2W10 are shown in Figure 2.8. Q-factors of L_1 and L_2 are expected to be from 4.2 to 6.2 over the same frequency range. These relatively low Q-factors comparing with general spiral inductors result from mutual coupling between the primary and secondary inductors.

The simulated effective coupling factor k results are shown in Figure 2.9. The L_1 has a large area compared with the L_2 and thus the inductance L_1 is larger than inductance L_2. The coupling length of L_1 is also longer than the length of L_2, thus the effective coupling factor k in L_1 is large than L_2 as shown in Figure 2.9. The effective coupling factor k of L_1 is from 0.57 to 0.68, and that of L_2 is from 0.45 to 0.56.

The combination of the transformer based inductors are shown in Figure 2.4. There are three kinds of inductance can be connected in the LC tank when switch on or off the



(a).



(b).

Figure 2.7: (a) The inductance in transformer D116N2W10. (b) The inductance in transformer D140N2W10.

NMOS. The biggest inductance connected in the LC tank is obtained when the L_1 is on and L_2 is off. And the lowest inductance connected in the LC tank is obtained when the L_1 is on and L_2 is on.

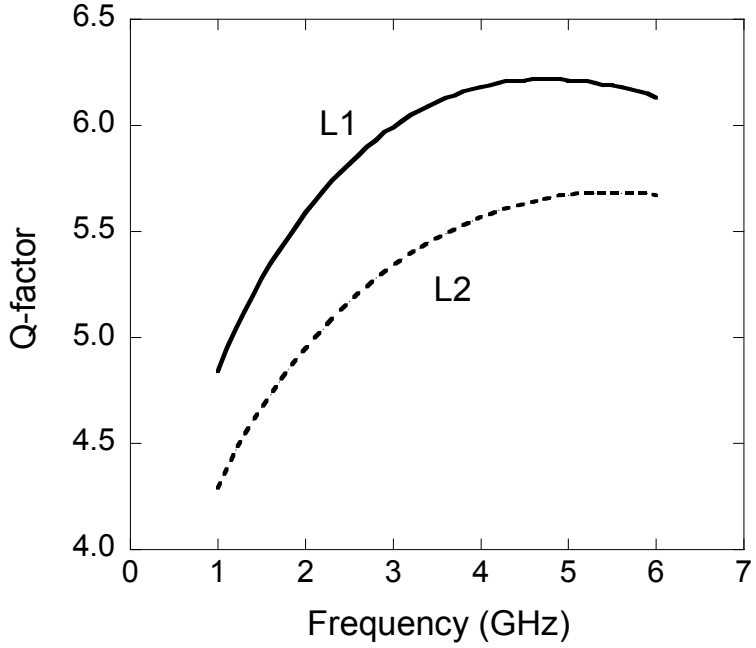


Figure 2.8: The Q-factor of the inductor L1 and L2.

The detail circuit of the transformer based inductors are shown in Figure 2.10. There are two sets of transformer based inductors which are denoted as [S], and there two NMOS switching and two AMOS varactors for one set. The simulation of the inductance with the control voltage from 0 V to 2.5 V is shown in Figure 2.11. It is clear that the inductance is changed with the turning voltage. Each L1 and L2 are simultaneously turned on or off, and there are three kinds of inductance is obtained. The inductance of L1 varies from 0.82 nH to 0.94 nH and that of L2 varies from 0.71 nH to 0.94 nH by the control voltage (Vctrl). The inductance variation is not so high so as to gradually change the oscillation frequency and to avoid the degradation of the phase noise. Thus, by switching the three different kinds of inductance, the coarse turning of the VCO is carried out. The fine turning of the VCO is carried out by turning the varactor in the transformer based inductance and varactors in the capacitor bank.

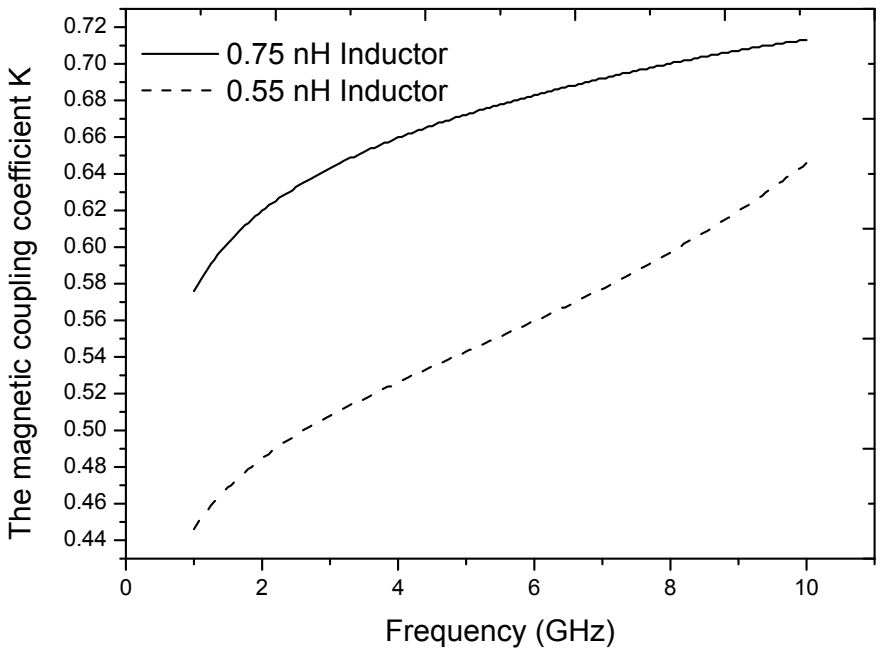


Figure 2.9: The coupling factor k of inductor L1 and L2.

2.2.2 Switched AMOS Varactors Design

MOS Varactors are based on MOS transistor structures (metal-oxide-semiconductor) and widely used in RF applications [44]. With PN-junction varactors, MOS varactors have a large capacitance per area, tuning range and the ratio of the C_{max}/C_{min}. The two most important types of MOS varactors are the NMOS and PMOS varactors. The NMOS varactor is the most commonly used varactor in CMOS technology. By varying the voltage between the two terminals (G and D/S), the capacitance of the device changes in accordance with the operating voltage by which it is biased. This device makes use of the gate oxide as dielectric so that the device capacitance is dependent on the capacitance of the charge zone (C_{Si}) and the capacitance of the oxide (C_{ox}). The total capacitance C of the device is given by [45]:

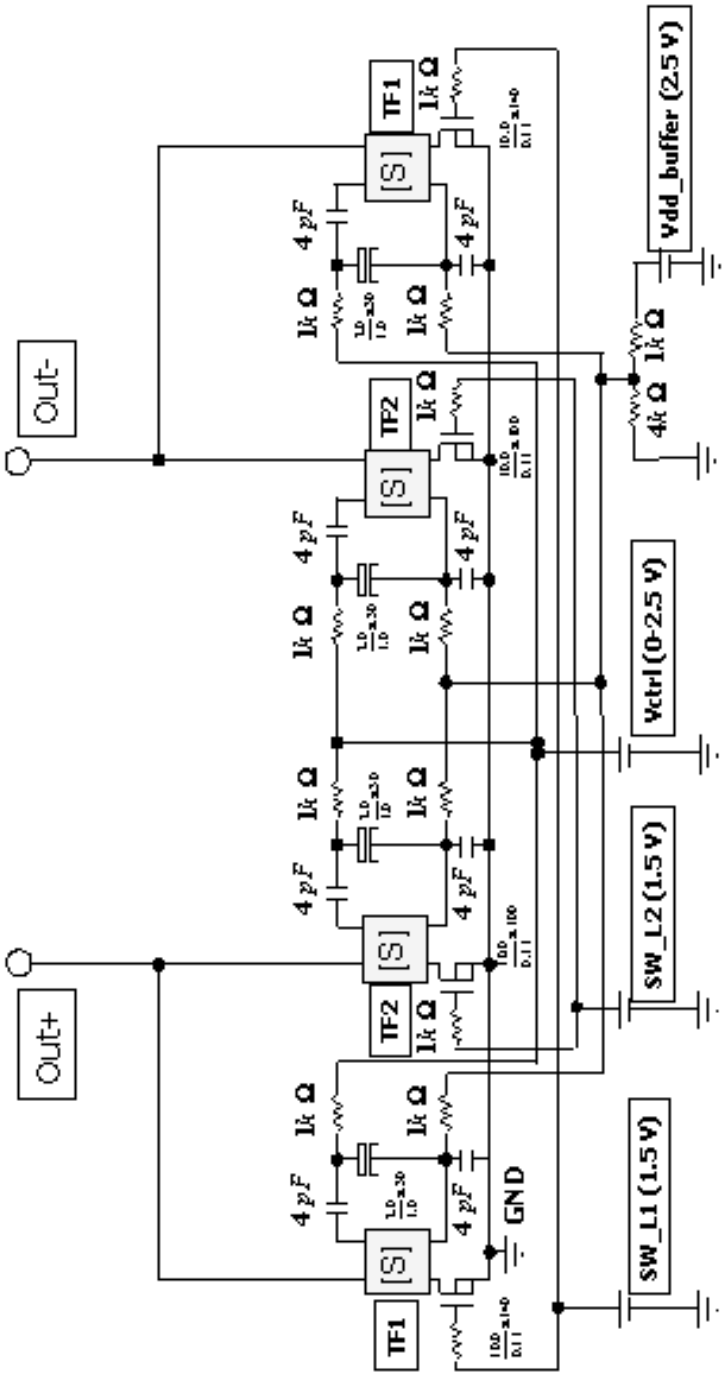


Figure 2.10: The detail circuit of the transformer based inductors.

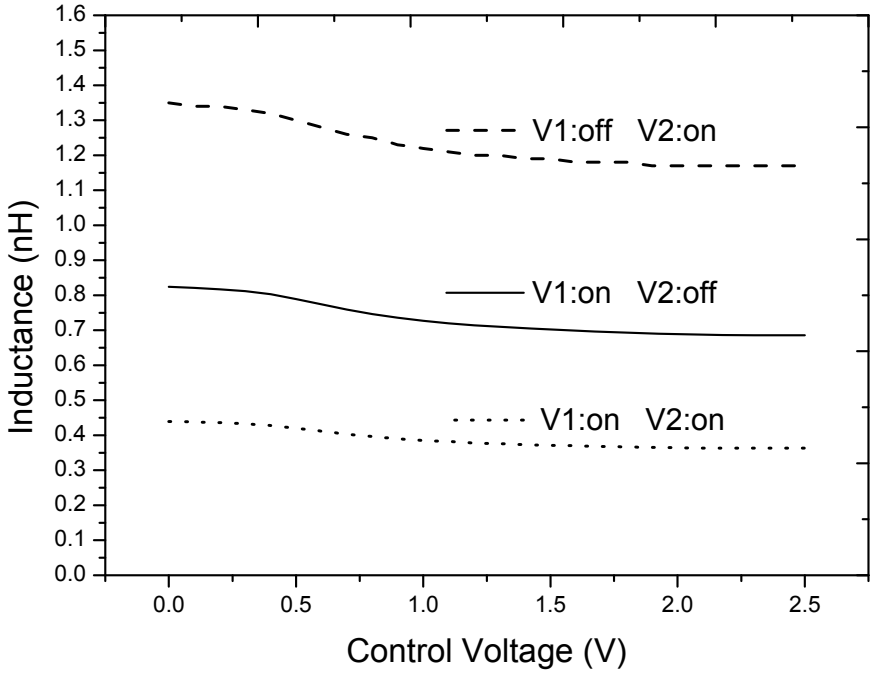


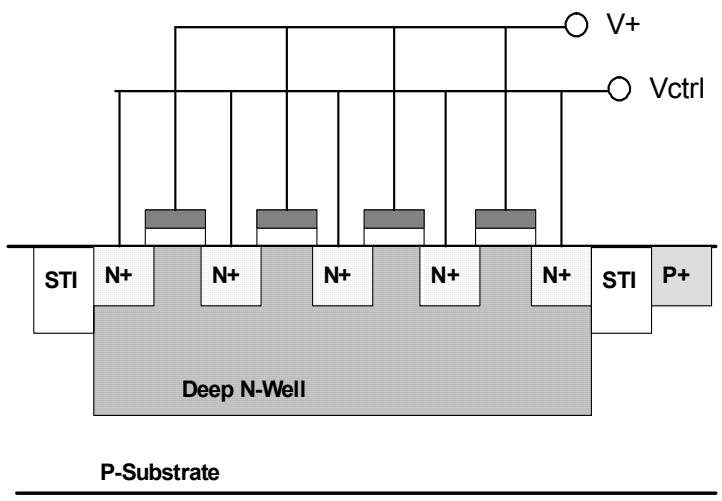
Figure 2.11: The three kinds of inductance of the transformer based inductors.

$$C = C_0 W L \tag{2.18}$$

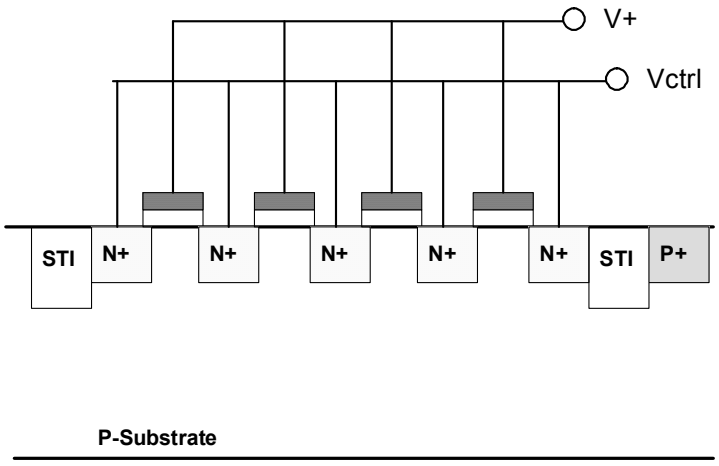
where C_0 is the capacitance per unit of area, which is equal to [46]:

$$C_0 = (\frac{1}{C_{ox}} + \frac{1}{C_{Si}})^{-1} \tag{2.19}$$

The effective capacitance from MOS Varactors almost three times higher than that of a PN-junction varactor per area [47]. The C_{max}/C_{min} ratio improves in comparison with that obtained with PN-junction varactors. NMOS varactors have a special operations modes, the accumulation mode which also called AMOS varactor. The difference between the AMOS varactor and the common NMOS varactors lies in the existence of an N well in the channel between the drain and the source in accumulation varactors, the difference of a cross section of an NMOS varactor and AMOS varactor is as shown in Figure 2.12.



(a).



(b).

Figure 2.12: (a)A cross section of an AMOS varactor. (b) A cross section of an NMOS varactor.

When a positive voltage (Vgs) is applied to the gate of an AMOS varactor, the total capacitance is mainly given by the oxide capacitance C_{ox}. When this voltage is decreased to negative values, the free electrons are repelled out the channel, generating an empty zone to which a capacitance C_{Si} is associated. In other words, when positive bias voltages are applied to the gate, the AMOS varactor C is the only capacitance of the varactor is C_{ox}.

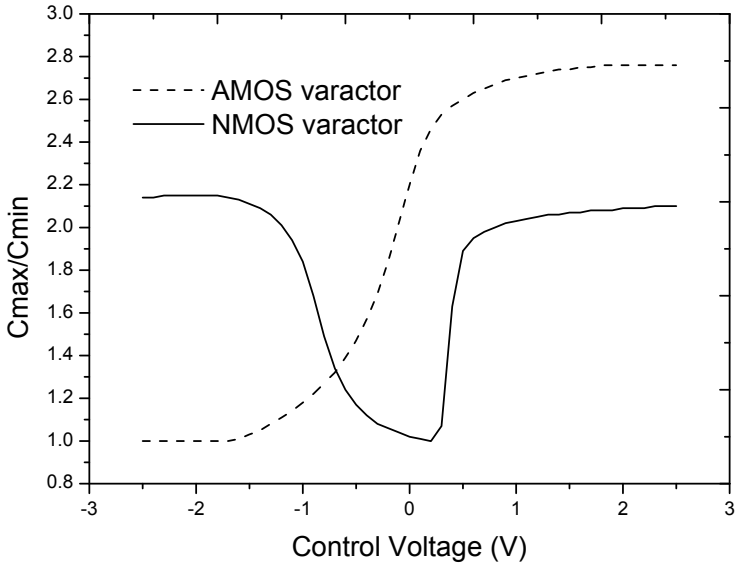


Figure 2.13: The Cmax/Cmin of AMOS varactor and NMOS varactor.

However, when this bias is reduced, it becomes the series of of C_{ox} and C_{Si} [47]:

$$C = \frac{C_{ox}C_{Si}}{C_{ox} + C_{Si}} \tag{2.20}$$

Thus, the total capacitance decreased. Commonly, the C_{Si} is smaller than C_{ox}, and the variation of the capacitance is large. To compared with the NMOS varactor, the simulation capacitance of both NMOS varactor and AMOS varactor are shown in Figure 2.13. The C_{max}/C_{min} ratio of NMOS varactor is from 1 to 2.1, while the C_{max}/C_{min} ratio of AMOS varactor is from 1 to 2.75.

The Q-factors simulation results of the NMOS varactor and AMOS varactor are shown in Figure 2.14. To obtain a improvement in the performance of the two type of varactor, there must be a compromise between capacitance and the quality factor. When Q reaches its maximum point, the capacitance is at its minimum level and vice versa. Compared with the NMOS varactor, AMOS varactor has a high Q-factors. The Q-factors of the NMOS varactor is between 10 and 30, while the Q-factors of the NMOS varactor is between 30 and 70. It is very clear that AMOS varactor has a better performance than

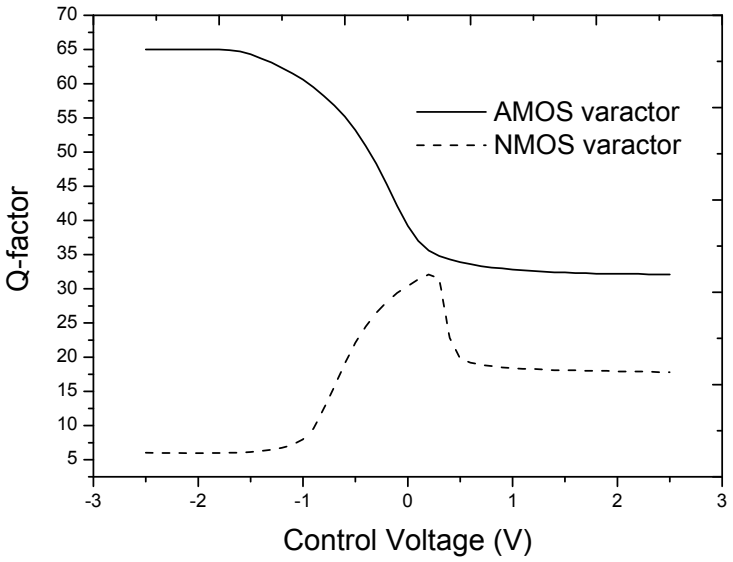


Figure 2.14: The Quality factor of AMOS varactor and NMOS varactor.

NMOS varactor .

To get a broader turning range, the switched AMOS varactor is used in this design. The schematic of the AMOS varactor bank is shown in Figure 2.15. There are five varactor branches. The gate length and finger width of the unit switching NMOS is 0.11 μm and 1000 μm, respectively. The AMOS varactor of the first branch has a 30 unite cells, and the AMOS varactor of the other branches has a unite cell of 50. There are five varactor branches: the first branch is always turned on and other branches are selectively turned on using NMOS switches (SW_C1 to SW_C4). The control voltage (V_{ctrl}) is the same as that for controlling transformer-based variable inductors. Hence, the variable inductors and varactors are simultaneously controlled by V_{ctrl}.

The simulation of the Figure 2.15 is shown in Figure 2.16. To compared with a conventional varactor, a single varactor is also simulated. In a single varactor, the turning range is about 1 to 1.6, however, the varactor bank has a turning range of 1 to 4.2. The varactor bank has a 2.5 times wider turning range than a single varactor.

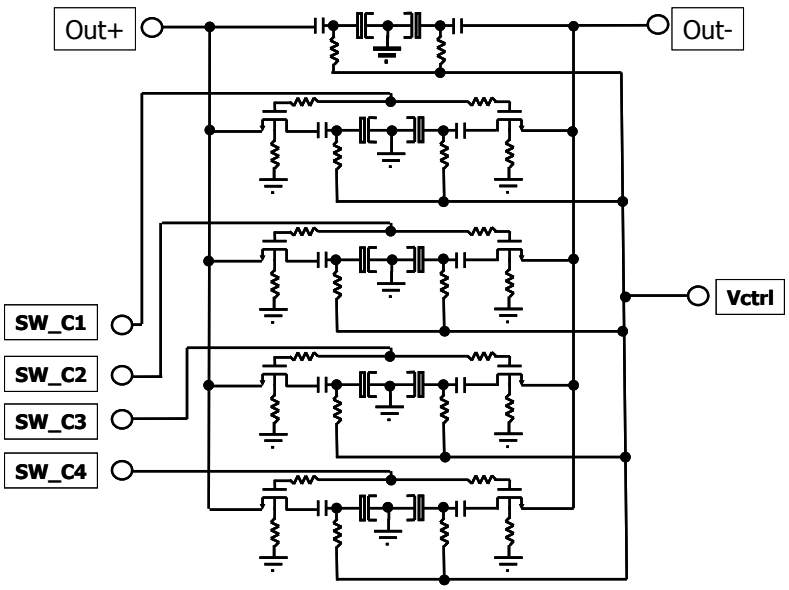


Figure 2.15: Switched AMOS varactor bank.

2.2.3 Cross-coupled PMOS Design

The merit of the PMOS transistor compared with the NMOS transistor is the low Flicker noise. A characteristic of the PMOS transistor is shown in the Table 2.2, where fmax is the frequency where the power gain becomes 1 and ft is the frequency where the current gain becomes 1. The fmax is 36.5 GHz and ft is 40.4 GHz. The fmax and ft are large enough for the 1 GHz to 3 GHz VCO design.

The basic PMOS crossing coupling transistor VCO is shown in Figure 2.17. The length of the PMOS transistor is 0.13 μm and the width of the PMOS transistor is 10 μm *60 figures.

To guarantee oscillation start-up at all operating temperatures and under worst case process variations, the PMOS transistor should provide enough negative resistance. If Rf is the resistance looking into the differential cross-couple pair of active devices, Ra is the equivalent differential resistance of the frequency selective network (comprised of LC

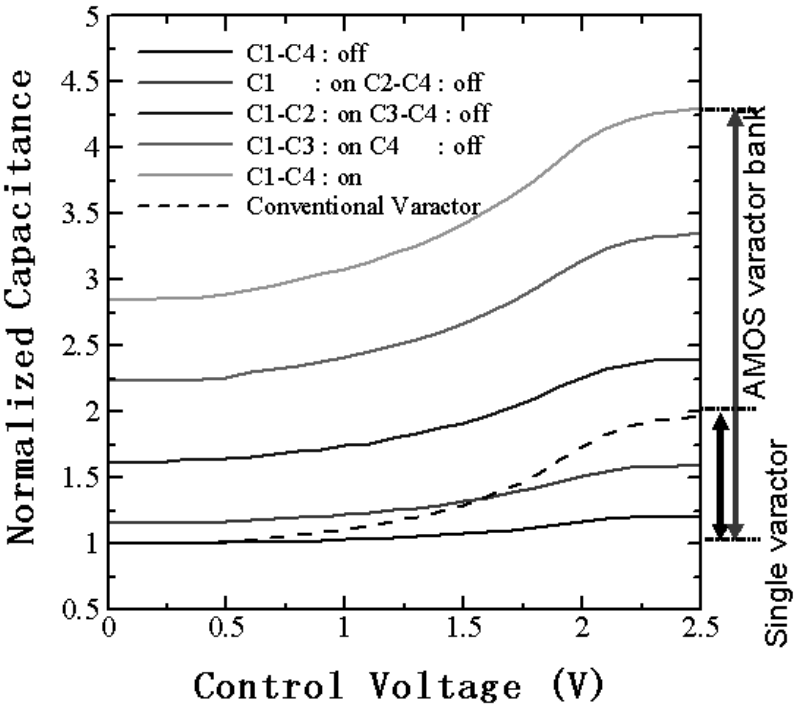


Figure 2.16: Capacitance turning range comparison.

tank), and gm is the small-signal transconductance of two PMOS transistors. In order to maintain the oscillation:

$$\frac{1}{Rf} + \frac{1}{Ra} < 0 \tag{2.21}$$

and

$$Rf = \frac{2}{gm} \tag{2.22}$$

To get enough negative resistance, the bias current is 40 mA for the PMOS crossing coupling transistor and the power supply is 1.5 V. The simulation of the negative resistance is shown in Figure 2.18.

From 0 Hz to 10 GHz, the negative resistance is from -30 to -13 Ω and the negative resistance is enough for the VCO to start up oscillation in the required bandwidth.

Table 2.2: Wideband VCO Target

$W(\mu m)/L(\mu m)$	276/ 0.13
fmax [GHz]	36.5
ft [GHz]	40.4
Ids[uA/um]	75.7

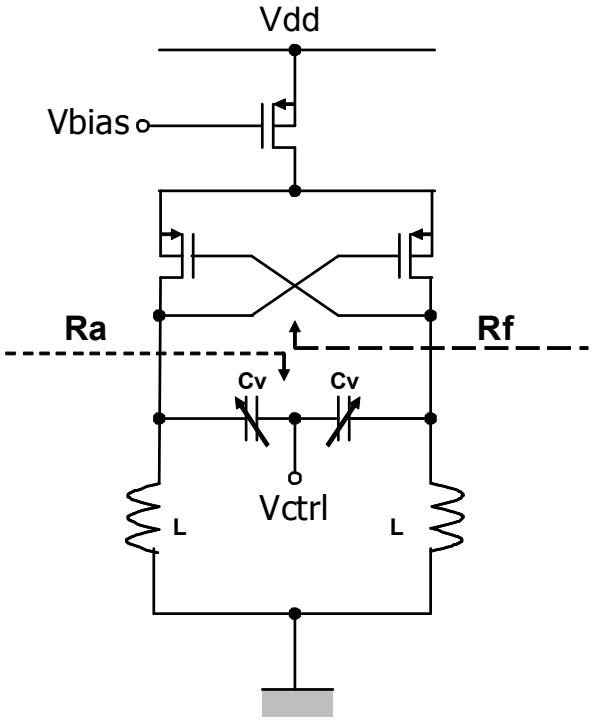


Figure 2.17: Basic PMOS crossing coupling transistor VCO.

2.2.4 VCO Circuit Design

The equivalent circuit of the Proposed VCO is shown in Figure 2.19. In the proposed wideband VCO, the varactor bank is used for the capacitance turning and the transformer based switched variable inductors are used for the inductance turning. The turning voltage of both the varactor bank and the transformer based switched variable

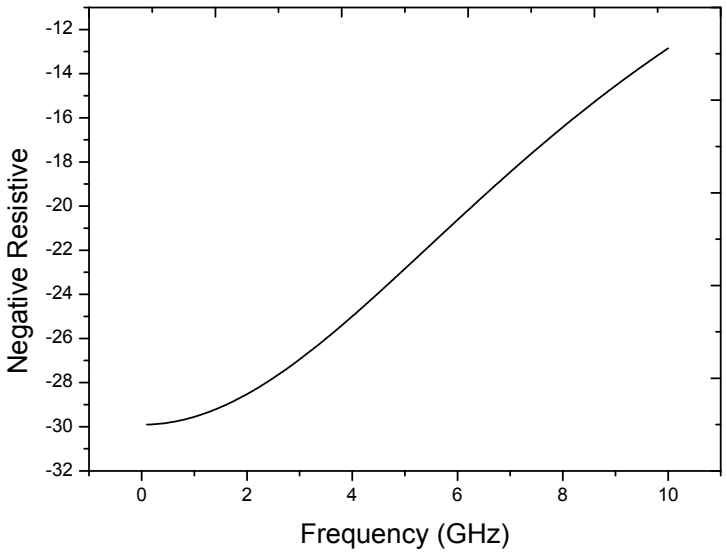


Figure 2.18: The simulation of the negative resistance provides by PMOS crossing coupling transistor .

inductors are the same voltage from the PLL loop after the filter.

The buffer amplifier is shown in Figure 2.20. The buffer amplifier works as a source follower. The buffer amplifier separates the 50 Ω load from the LC tank. If the 50 Ω load is directly connected with the LC tank, the Q-value becomes too low and it affects the phase noise of the VCO. The transistors for the amplifier have a gate length size of 0.3 μm and a gate width of 5.2 μm by 40 figures. The power supply is 2.5 V and the bias current is 16 mA for each amplifier.

The simulation of the LC tank is carried out at 2.47 GHz and 3.1 GHz, respectively. The impendence and the reactance of the LC tank are showing in Figure 2.21. The impendence is 43 Ω at the oscillation of 2.47 GHz and 55 Ω at the oscillation of 3.1 GHz. Compared with the negative resistance as showing in Figure 2.18, the impendence is about -28.4 Ω at the oscillation of 2.47 GHz and -26.7 Ω at the oscillation of 3.1 GHz. These conditions satisfy the oscillation start-up criterion as in Equation 2.21. And there is still some margin to deal with the variation of the temperature, process and other factors. The

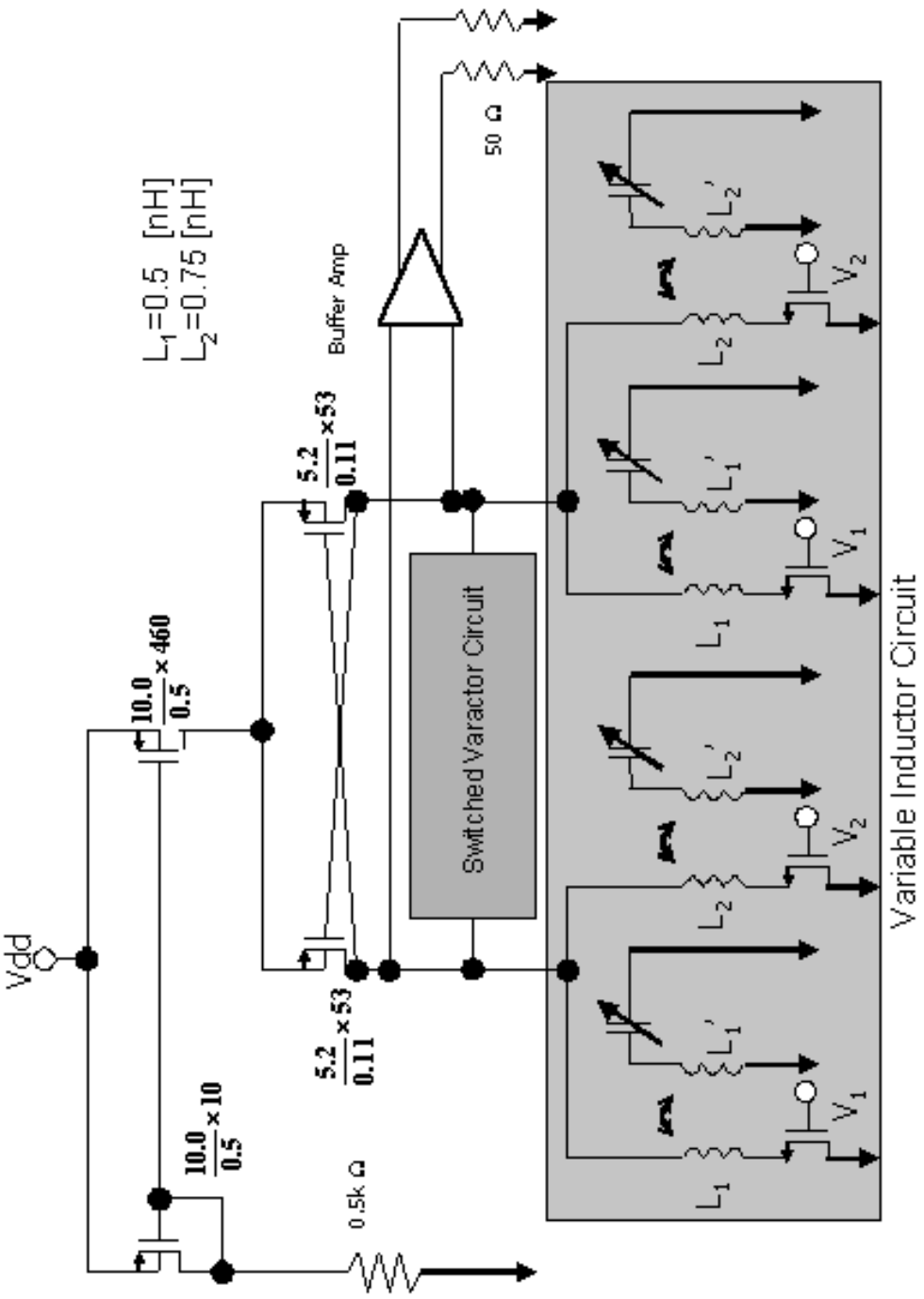


Figure 2.19: The equivalent circuit of the Proposed VCO.

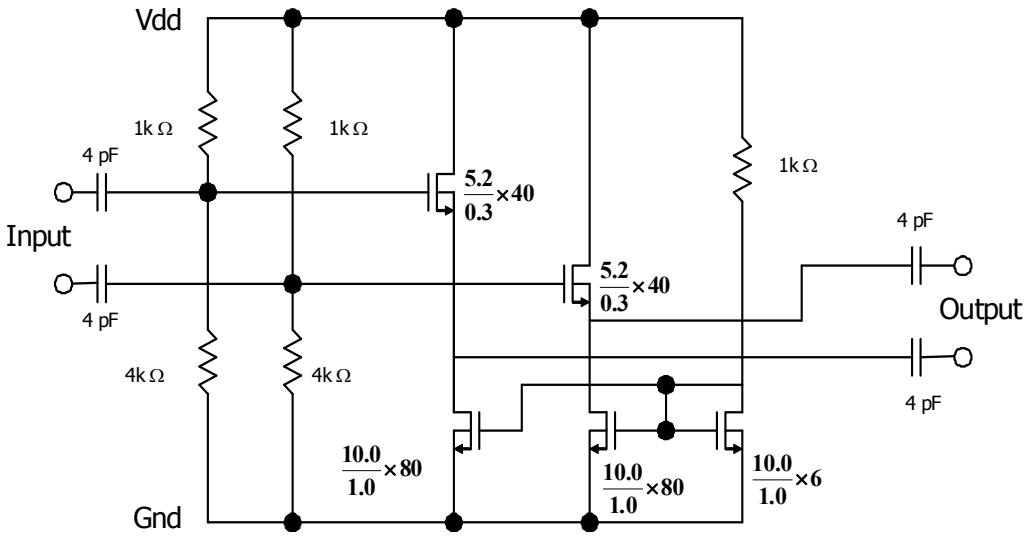
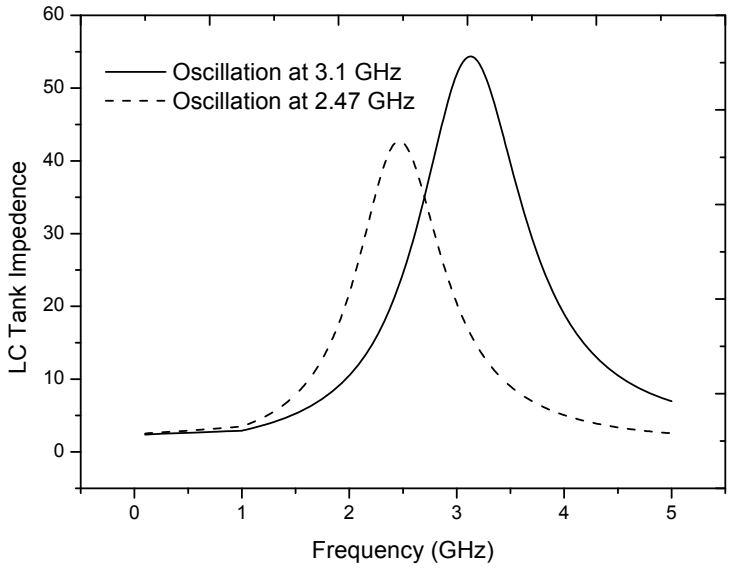


Figure 2.20: Schematic of the buffer amplifier.

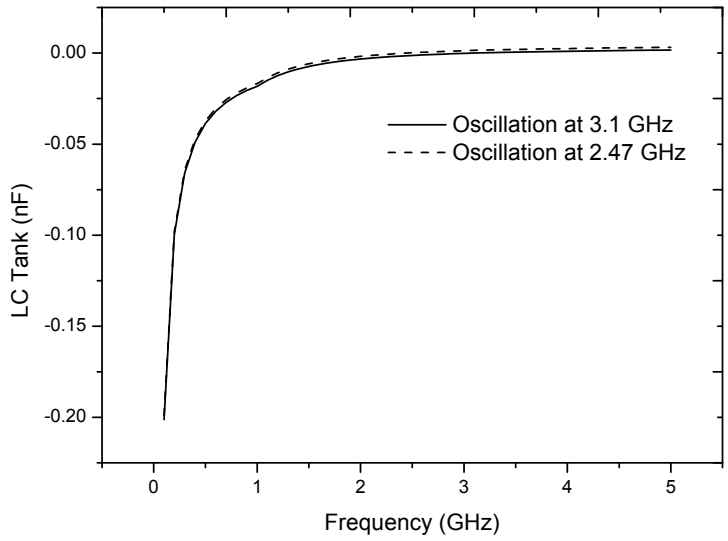
reactance of the LC tank is 0 at the oscillation frequency as showing in Figure 2.21.

The load line of the PMOS crossing coupling transistors are drawn as showing in Figure 2.22. The loadline is drawn at a control voltage of 1.5 V and the oscillation frequency of 3.1 GHz. As shown in the figure, part of the loadline enters into the negative axis of current. The maximum current is near 53 mA and the minimal current is near -8 mA. It implies the PMOS crossing coupling transistors work in the Class-AB state and there is no waste of the quiescent bias current.

To show the coarse turning of the transformer based inductor, the simulation is carried out in Figure 2.23. The solid line shows the calculated oscillation frequencies when both L1 and L2 are turned on and the first AMOS branch is only turned on. This condition is for obtaining highest oscillation frequency. The broken line shows the frequencies when L1 is turned off and L2 are turned on and the first AMOS branch is only turned on. The dotted line shows frequencies when L1 is turned on and L2 is turned off with all AMOS varactor branches are turned on. This condition gives the lowest oscillation frequency. By selectively turning the AMOS varactor branches on, it is expected that the VCO generates



(a).



(b).

Figure 2.21: (a) The impedance of the LC tank at the oscillation frequency. (b) The reactance of the LC tank at the oscillation frequency.

continuous oscillation frequencies.

In Figure 2.24 illustrates the detail simulated oscillation frequencies of the VCO

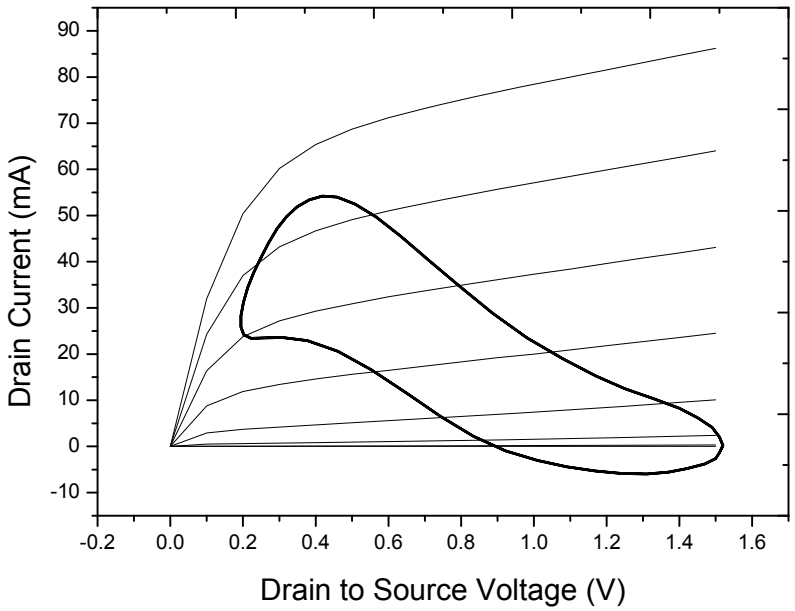


Figure 2.22: The loadline of the PMOS crossing coupling transistors

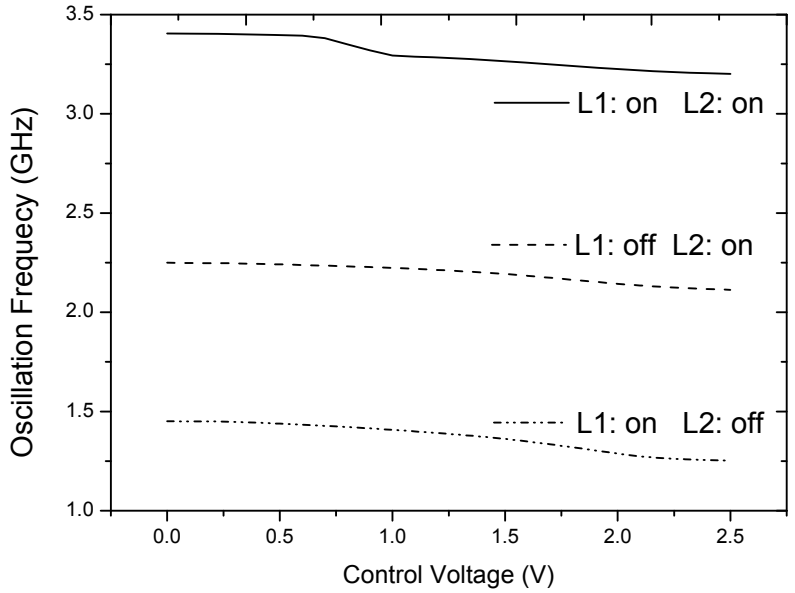


Figure 2.23: The coarse turning of the transformer based inductor.

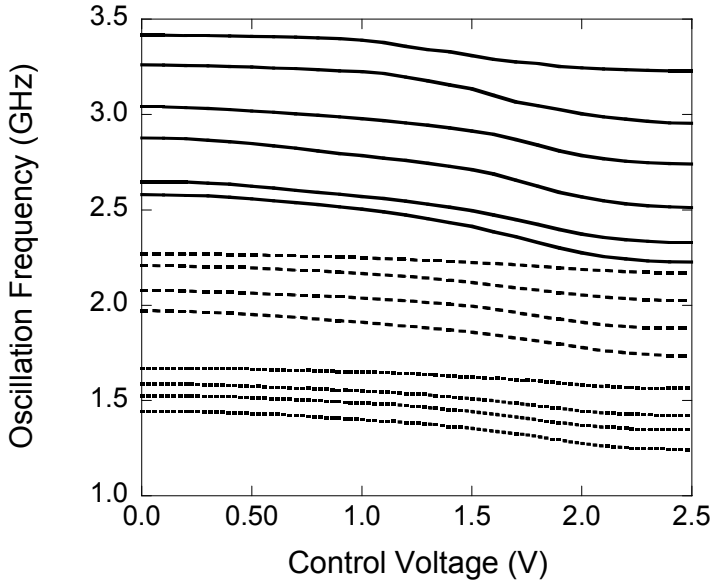


Figure 2.24: Simulated oscillation frequency tuning range.

IC. The oscillation frequency is expected to be from 1.25 GHz to 3.45 GHz. For the four AMOS varactor banks C1-C4, they can be expressed by a four bit binary code, where "1" indicates the bank is on and "0" indicates the bank is off. The solid lines show the simulated oscillation frequencies when both L_1 and L_2 are turned on while the AMOS varactors are selectively turned on as "1000", "0100", "0010", "1100", "1110", "1111". The broken lines show the oscillation frequencies when only L_2 is turned on while the AMOS varactors are selectively turned on as "1000", "1100", "1110", "1111". The dotted lines show oscillation frequencies when only L_1 is turned on while the AMOS varactors are selectively turned on as "1000", "1100", "1110", "1111". By selectively turning on the variable inductors and AMOS varactor branches, the VCO is expected to generate continuous oscillation frequencies from 1.25 GHz to 3.45 GHz.

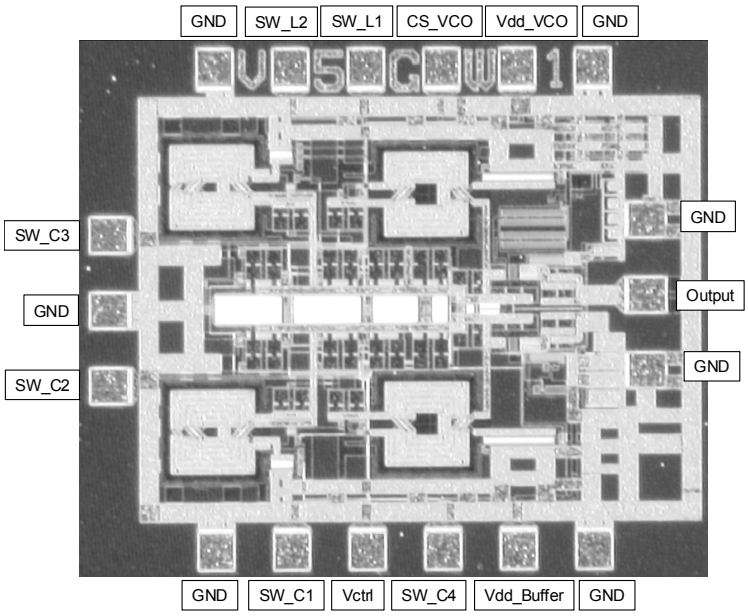


Figure 2.25: Photograph of the fabricated VCO IC.

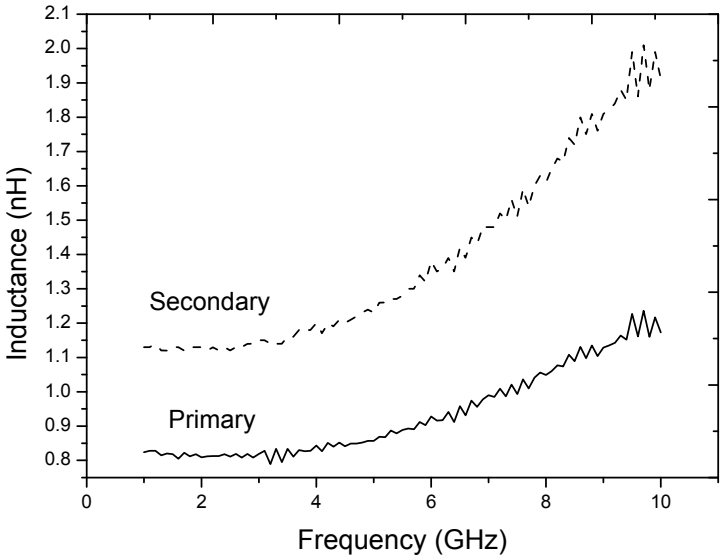


Figure 2.26: The measured inductance of the transformer D116N2W10.

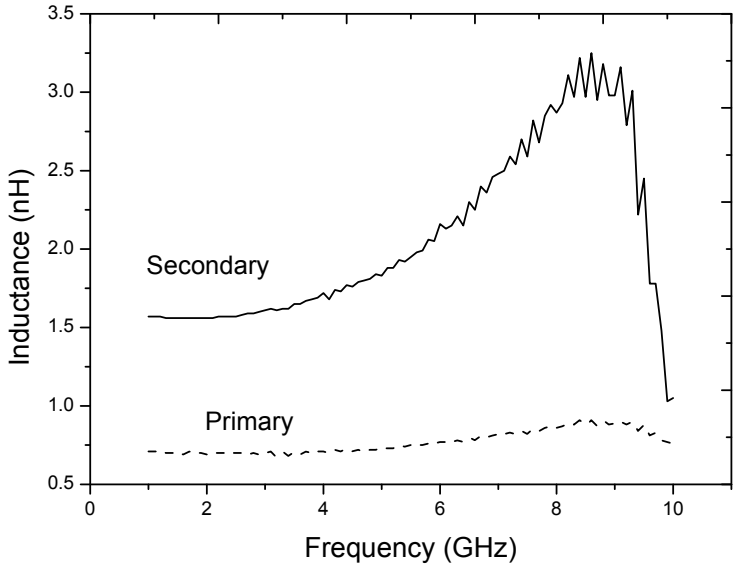


Figure 2.27: The measured inductance of the transformer D140N2W10.

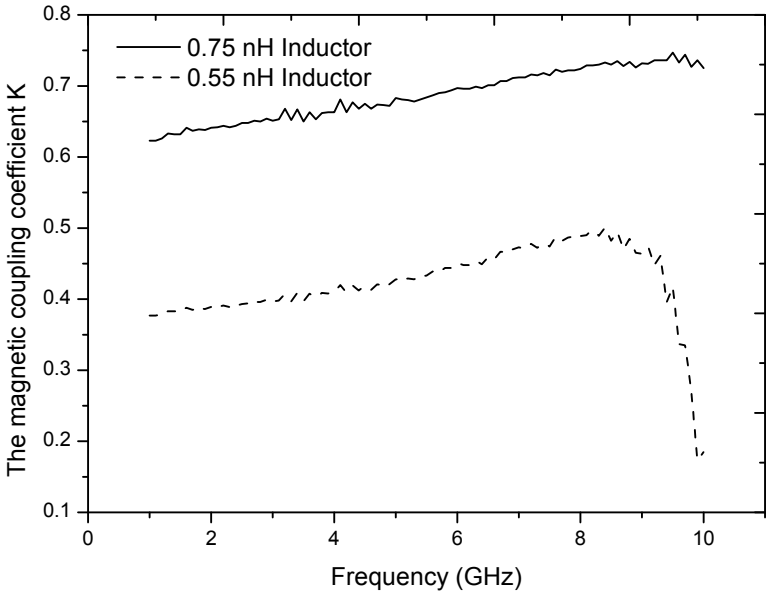


Figure 2.28: The measured coupling coefficient.

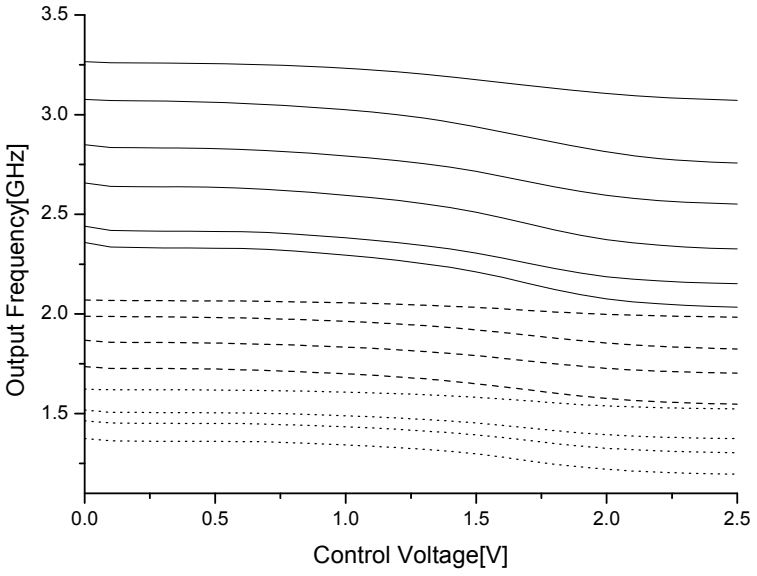


Figure 2.29: Measured oscillation frequency tuning range.

2.3 Experiment Results

The proposed VCO IC is implemented in the 0.11 μm CMOS process. Figure 2.25 shows a photograph of the fabricated VCO IC. The VCO IC size is 0.65 mm by 0.9 mm.

The VCO IC measurement is carried out with on-wafer probes. The measured inductance value is show in Figure 2.26 and 2.27. The inductance of the primary stage of transformer D116N2W10 is from 0.72 nH to 0.9 nH and the inductance of the secondary stage of it is from 1.6 nH to 2.5 nH. The inductance of the primary stage of transformer D140N2W10 is from 0.82 nH to 0.68 nH and the inductance of the secondary stage of it is from 1.15 nH to 1.3 nH. The measured effective coupling factor k results are shown in 2.28.

The dependence of the measured frequency tuning range on the control voltage is illustrated in Figure 2.29. Continuous oscillation frequency from 1.20 GHz to 3.27 GHz is obtained. Thus, a frequency tuning range as high as 92.6 % has been realized with a center frequency of 2.23 GHz. The measured oscillation frequencies agree well with the expected

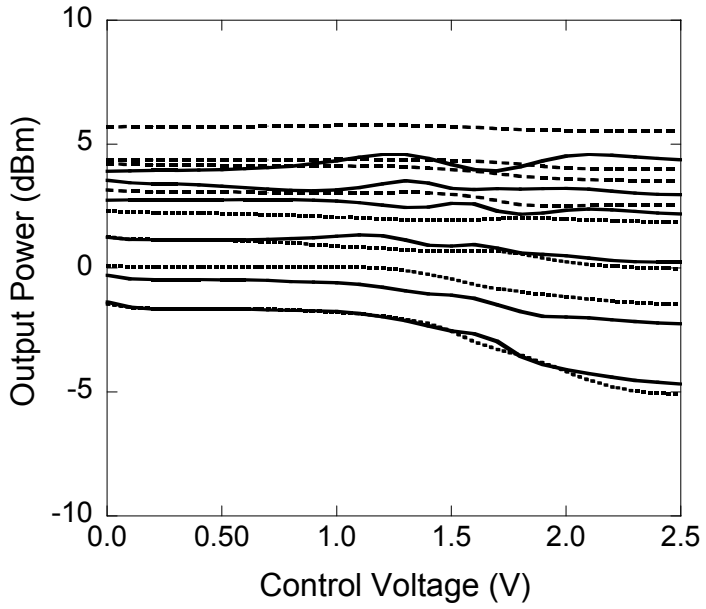


Figure 2.30: Measured output power of the proposed VCO IC.

ones. The measured output power is from -5.1 dBm to +5.7 dBm over the frequency range from 1.20 GHz to 3.27 GHz, as shown in Figure 2.30. For each switched inductor, the output powers reduce as the output frequency decreases because the Q-factors decrease as the number of switch-on varactor banks increases.

In Figure 2.29 and Figure 2.30, the solid lines show measured results when both L_1 and L_2 are turned on and AMOS varactors are selectively turned on. The broken lines show those when only L_2 is turned on, and dotted lines shows those when L_1 is turned on. As shown in Figure 2.29, course tuning is realized by switching inductors and AMOS varactors, and fine tuning is achieved by changing bias voltage (control voltage) to the AMOS varactors and variable inductors (C_V in Figure 2.4) . It is estimated that a VCO with no C_V in Fig.2 has a tuning range of around 85%. Thus, a contribution of changing inductance to the tuning range is around 8%. The phase noise measurements are performed on Agilent signal source analyzer E5052B. Figure 2.31 illustrates measured phase noise curves of the VCO at oscillation frequencies of 1.2 GHz (solid line) at a control

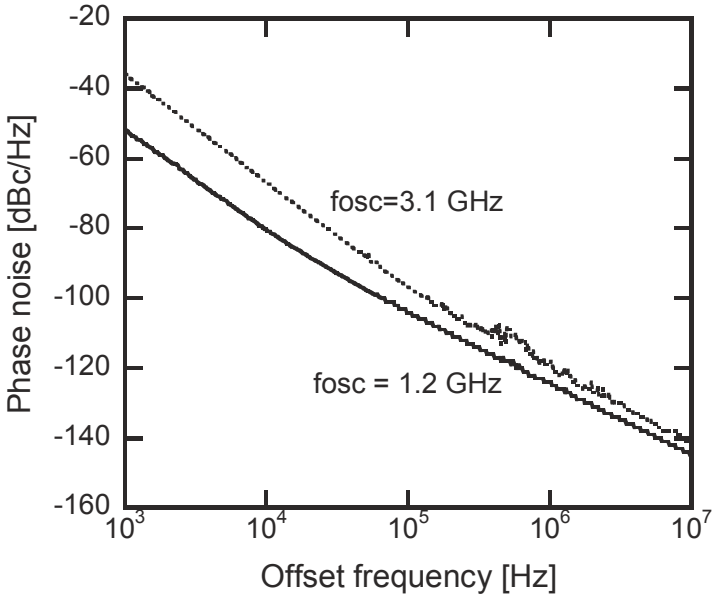


Figure 2.31: Measured phase noise performance of the proposed VCO IC at 1.2 GHz (solid line) and 3.1 GHz (dotted line).

voltage of 2.5V and 3.1 GHz (dotted line) at a control voltage of 1.5V, respectively. The measured phase noises at 1 MHz offset from the carriers are -120 dBc/Hz at 3.1 GHz and -123 dBc/Hz at 1.2 GHz, respectively. The measured phase noises at offset frequencies from 1 KHz to 100 KHz at 3.1 GHz carrier (dotted line) is around 10 dBc/Hz higher than those at 1.2 GHz carrier (solid line). This phenomenon is mainly caused by low quality factor of the switched variable inductors, because this oscillation condition is obtained by turning on two transformer-based inductors (L_1 and L_2 in Fig.2) simultaneously. At the oscillation condition of 1.2 GHz, only L_1 is turned on, and the quality factor of L_1 is higher than that of the parallel connection of L_1 and L_2.

Table 2.3 summarizes the performance of the proposed VCO IC and recently reported wideband VCOs using CMOS technologies. The VCO IC proposed in this paper exhibits an ultra-wideband tuning range with excellent phase noise.

Table 2.3: Summary of the proposed VCO IC and comparison with recently reported wideband VCOs

Reference	This work	[50]	[51]	[52]	[53]
Technology CMOS	0.13 μm	0.13 μm	0.13 μm	0.13 μm	0.18 μm
Supply voltage	1.5 V	1.2 V	1.0 V	1.0 V	1.8 V
Center frequency	2.2 GHz	4.15 GHz	5.2 GHz	4.3 GHz	1.39 GHz
Tuning range	92.6 %	50.6 %	69%	58.7 %	66.6 %
Phase noise @1 MHz	-120 dBc @ 3.1 GHz	-118 dBc @ 4 GHz	-118 dBc @ 4.6 GHz	-120 dBc @ 3 GHz	-127 dBc @ 1.7 GHz

2.4 Summary

In this chapter, the limitation of the wideband VCO design is analyzed, firstly, Because of the limitation of the capacitor bank, the switched transformer-based switched variable inductors are proposed. The proposed novel ultra-wideband VCO IC has been demonstrated using 0.11 μm CMOS technology. By simultaneously controlling transformer-based switched variable inductors and switched AMOS varactors, a continuous frequency oscillation from 1.20 GHz to 3.27 GHz was realized. The frequency tuning range is as high as 92.6 % with a center frequency of 2.23 GHz. The measured phase noises at 1 MHz offset from the carriers are -120 dBc/Hz at 3.1 GHz and -123 dBc/Hz at 1.2 GHz, respectively.

Chapter 3

High Linearity and High Efficiency PA IC

3.1 Overview

In some wireless standards, such as GSM, where the modulated signal has constant envelope, a nonlinear PA can be used. A nonlinear PA generally has higher efficiency than a linear PA. However, with their higher efficiency, the data that these transceivers can transmit within a given bandwidth are quite low. In order to increase the data rate and get the high speed without increasing the bandwidth, a more spectrally efficient linear modulation scheme must be used as in Table 3.1. The use of the linear modulation makes the signal envelop has a much higher Peak to Average Ratio (PAR) and the PA has to back off several dBs from P1dB to satisfy the demanding specifications of Adjacent-channel Power Ratio (ACPR) and Error Vector Magnitude (EVM). However, in this case, the PA works in an ultra low efficiency state, and a large of the power consumption is wasted. To deal with this problems, the linearization technique is used for PA. The linearization technique can improve the linearity of the PA and operating with a less back-off from P1dB. Thus, the PA can work near the P1dB with a higher efficiency and more effective. Designing an effective linearization technique is quite important for PA in linear modulation system.

Table 3.1: Summary of wireless communication system with PAR

System	Bandwidth(MHz)	Modulation	PAR(dB)	Antenna Power(dBm)
EDGE	0.20	8PSK	3.2	27
UMTS	3.84	HPSK	3.5-7	24
cdma2000	1.23	HPSK	4-9	24
802.11b	11	QPSK	3	20
802.11a/g	18	OFDM	6-17	20
DSRC	2	QPSK	4	12

The research of the linearization technique is very attractive in these years. Many CMOS linear PAs were reported to realize high linearity in [54]-[62]. The linearization technique by suppressing the harmonic generated from the nonlinear source of transconductance g_m and gate-source capacitance c_{gs} is reported in [54]. The c_{gs} compensation is reported in [55],[56] and g_{m3} (the 3rd-order derivative of the dc transfer characteristic) canceling by multigated transistor (MGTR) is reported in [57] for linearization of the CMOS PA. Besides the above transistor level linearization, there are many system level linearizations, such as envelope elimination and restoration (EER) [58], digital predistortion [59], Doherty [59] and envelope tracking [62].

Dedicated Short Range Communication (DSRC) is being seriously considered as a promising wireless technology for enhancing transportation safety and highway efficiency. It also promises a proposed solution for the automatic debiting of vehicles in an electronic toll collection (ETC) system with a carrier frequency of 5.8 GHz, which makes a revolution in traffic charging without disturbing the traffic flow. The modulation of the DSRC-based ETC system is Amplitude Shift Keying (ASK) or Quadrature Phase Shift Keying (QPSK) with a peak-to-average power ratio (PAR) of 2 dB to 4 dB. Therefore, high linearity PA design is necessary for DSRC application. However, many linearization techniques sacrifice the power efficiency to obtain some improvement in linearity. The PAEs of the linearized

PAs operating during 5 GHz to 6 GHz are always below 25% at P1dB. Thus, a linearization technique with high linearity improvement and high efficiency is considered quite critical for modern linearity PA design.

In this paper, a novel multi-cascode CMOS PA with post-linearization technique is proposed for the 5.8 GHz DSRC application. The post-linearization technique is dedicated for CMOS cascode PA, which is usually used to boost output power to overcome the poor device reliability and ruggedness problems [63]. Post-linearization is used to linearize LNA in [64]-[65]. However, it is only limited in LNA application and no application in PA is invested. In this paper, the principle analysis of the proposed novel multi-cascode PA with post-linearization is described with Volterra Series. To verify the effectiveness of proposed post-linearization technique, the novel CMOS PA is designed and fabricated. The measurement results demonstrate the proposed idea.

3.2 Multicascode PA Design

3.2.1 Transconductance Nonlinearity in Conventional Cascode PA

Figure.3.1 shows a conventional cascode PA and its simplified small signal AC equivalent circuit. The distortion of the cascode PA is the total distortion from the common source stage and common gate stage. The analysis is simplified and the result is also simplified in order to demonstrate the principle of the post-linearization technique.

In the cascode PA, the drain current can be expressed in terms of the gate-source voltage around the bias point by the power series expansion in limited third degree as [66]:

$$i_{outa} = g_{a1}v_{ga} + g_{a2}v_{ga}^2 + g_{a3}v_{ga}^3 \tag{3.1}$$

$$i_{out} = g_{b1}v_{gb} + g_{b2}v_{gb}^2 + g_{b3}v_{gb}^3 \tag{3.2}$$

where g_{ai} and g_{bi} are the ith-order derivative of the dc transfer characteristic of common source and common gate stage, respectively.

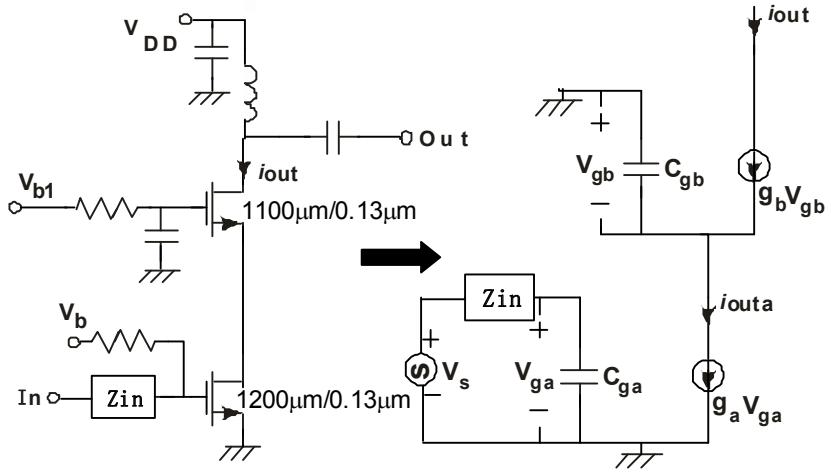


Figure 3.1: A conventional cascode PA and its simplified small signal AC equivalent circuit.

Let the excitation is:

$$v_s = \frac{1}{2}\sum_{q=-Q}^{Q} exp(j\omega_q t) \tag{3.3}$$

where Q implies the excitation frequency and it is not equal to zero.

The v_{gb} can be expressed in a limited third order as:

$$v_{gb} = v_{gb1} + v_{gb2} + v_{gb3} \tag{3.4}$$

where v_{gb1}, v_{gb2} and v_{gb3} are the first, second and third orders of the response to the common source current. i_{out} can also be expressed in limited third order as:

$$i_{out} = i_{out1} + i_{out2} + i_{out3} \tag{3.5}$$

where i_{out1} , i_{out2} and i_{out3} are the first, second and third orders of the corresponding response to v_{gb}.

Using Kirchhoff's Voltage Law for the input loop analysis, v_{ga} can be obtained as:

$$v_{ga} = \frac{1}{2}\sum_{q=-Q}^{Q} \frac{1}{j\omega_q c_{ga} z_{in} + 1} exp(j\omega_q t) \tag{3.6}$$

Let

$$v_{ga} = \frac{1}{2}\sum_{q=-Q}^{Q} H_0(\omega_q)exp(j\omega_q t) \tag{3.7}$$

where

$$H_0(\omega) = \frac{1}{j\omega_q c_{ga} z_{in} + 1} \tag{3.8}$$

The current excitations from the common source stage are discussed according to the orders. For the first order current $g_{a1}v_{ga}$ from the common source stage: by using Kirchhoff's Current Law for the source node of cascode stage, v_{gb1} can be written as:

$$v_{gb1} = \frac{1}{2}\sum_{q=-Q}^{Q} H_1(\omega_q)exp(j\omega_q t) \tag{3.9}$$

where

$$H_1(\omega) = \frac{g_a}{j\omega c_{gb} + g_{b1}} \cdot \frac{1}{j\omega c_{ga} z_{in} + 1} \tag{3.10}$$

Thus, the first order current $i_{out1,1st}$ from excitation of $g_{a1}v_{ga}$ can be obtained as:

$$i_{out1,1st} = \frac{g_a}{2}\sum_{q=-Q}^{Q} H_1(\omega_q)exp(j\omega_q t) \tag{3.11}$$

By using nonlinear current analysis, $i_{out2,1st}$ and $i_{out3,1st}$ can be expressed as:

$$\begin{aligned} &i_{out2,1st} \\ &= \frac{g_a}{4}\sum_{q1=-Q}^{Q}\sum_{q2=-Q}^{Q}(\{\frac{j(\omega_{q1}+\omega_{q2})c_{gb}g_{b2}}{j(\omega_{q1}+\omega_{q2})c_{gb}+g_{b1}}H_1(\omega_{q1}) \\ &H_1(\omega_{q2})exp[j(\omega_{q1}+\omega_{q1})t]\}) \end{aligned} \tag{3.12}$$

and

$$\begin{aligned} &i_{out3,1st} = \\ &\frac{1}{8}\sum_{q1=-Q}^{Q}\sum_{q2=-Q}^{Q}\sum_{q3=-Q}^{Q}\{(\frac{-2g_{b2}^2}{j(\omega_{q1}+\omega_{q2}+\omega_{q3})c_{gb}+g_{b1}}+g_{b3}) \\ &H_1(\omega_{q1})H_1(\omega_{q2})H_1(\omega_{q3})exp[j\sum_{j=1}^{3}\omega_{qj}t]\} \end{aligned} \tag{3.13}$$

Usually, g_{b1} is much larger than c_{gb} to get a desired voltage gain. Therefore, c_{gb} is negligible compared with g_{b1}.

Thus, for two excitation frequencies, where Q=2, the terms of $\omega = 2\omega_1 - \omega_2$ can be obtained as:

$$i_{out3,1st}(2\omega_1 - \omega_2) = \frac{3}{8}(g_{b3} - \frac{2g_{b2}^2}{g_{b1}})H_1(\omega_1)H_1(\omega_1) \cdot H_1(-\omega_2)exp[j(2\omega_1 - \omega_2)t] \tag{3.14}$$

For the second order current $g_{a2}v_{ga}^2$ from the common source stage, v_{gb1} can be obtained by using Kirchhoff's Current Law for the source node of cascode stage, and it can be written as:

$$v_{gb1} = \frac{1}{4}\sum_{q1=-Q}^{Q}\sum_{q2=-Q}^{Q}(\{\frac{g_{a2}}{j(\omega_{q1}+\omega_{q2})c_{gb}+g_{b1}}H_0(\omega_{q1}) H_0(\omega_{q2})exp[j(\omega_{q1}+\omega_{q1})t]\}) \tag{3.15}$$

and the corresponding current is

$$i_{out1,2st} = \frac{g_{b1}}{4}\sum_{q1=-Q}^{Q}\sum_{q2=-Q}^{Q}(\{\frac{g_{a2}}{j(\omega_{q1}+\omega_{q2})c_{gb}+g_{b1}}H_0(\omega_{q1}) H_0(\omega_{q2})exp[j(\omega_{q1}+\omega_{q1})t]\}) \tag{3.16}$$

This part only generates even order current and the higher orders for the excitation of the second order current $g_{a2}v_{ga}^2$ generate fourth and sixth orders signal. Thus, they have no effect on the third order distortion.

For the third order current $g_{a3}v_{ga}^3$ from the common source stage, v_{gb1} can be obtained as:

$$v_{gb1} = \frac{1}{8}\sum_{q1=-Q}^{Q}\sum_{q2=-Q}^{Q}\sum_{q3=-Q}^{Q}\{(\frac{g_{a3}}{j(\omega_{q1}+\omega_{q2}+\omega_{q3})c_{gb}+g_{b1}}) H_0(\omega_{q1})H_0(\omega_{q2})H_0(\omega_{q3})exp[j\sum_{j=1}^{3}\omega_{qj}t]\} \tag{3.17}$$

Thus, the corresponding current is

$$i_{out3,3th} = \frac{1}{8}\sum_{q1=-Q}^{Q}\sum_{q2=-Q}^{Q}\sum_{q3=-Q}^{Q}\{(\frac{g_{a3}g_{b1}}{j(\omega_{q1}+\omega_{q2}+\omega_{q3})c_{gb}+g_{b1}}) H_0(\omega_{q1})H_0(\omega_{q2})H_0(\omega_{q3})exp[j\sum_{j=1}^{3}\omega_{qj}t]\} \quad (3.18)$$

The other high orders generated from third order current $g_{a3}v_{ga}^3$ are above six orders and they are neglected.

For two excitation frequencies, where Q=2, the terms of $\omega = 2\omega_1 - \omega_2$ can be obtained as:

$$i_{out3,3th}(2\omega_1-\omega_2) = \frac{3}{8}\frac{g_{a3}g_{b1}}{(2\omega_1-\omega_2)c_{gb}+g_{b1}} H_0(\omega_1)H_0(\omega_1)H_0(-\omega_2)\cdot exp[j(2\omega_1-\omega_2)t] \quad (3.19)$$

Thus, the nonlinearity in the total cascode PA is the total third order distortion from Equation.3.14 and Equation.3.19.

3.2.2 Principle Analysis of the Proposed Technique

The nonlinearity in the total cascode PA is the total third order distortion from Equation.3.14 and Equation.3.19. The Equation.3.14 expresses the nonlinearity from common gate stage and Equation.3.19 expresses the nonlinearity from common source stage. In the cascode PA, g_{a1} is very large to get a large gain in the common source stage, and g_{b1} is small because the gate of the common gate stage isn't shorted to ground by a large bypass capacitor. Thus, $H_1(\omega)$ is much larger than $H_0(\omega)$, and the nonlinearity generated in the common gate stage is much larger than that in common source gate. In this paper, the proposed technique is focused on the distortion canceling, which is mainly generated in common gate stage as shown in Equation.3.14.

There are two parts contributing the nonlinear current from Equation.3.14, and

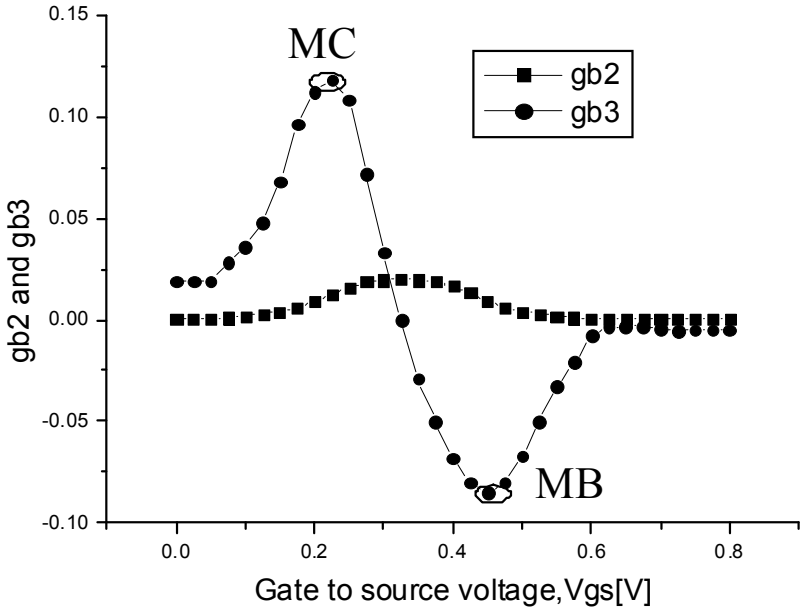


Figure 3.2: g_{b2} and g_{b3} in a NMOS transistor.

the first part of nonlinear current is:

$$i_{out3}(2\omega_1 - \omega_2) = \frac{3}{8} g_{b3} H_1(\omega_1) H_1(\omega_1) H_1(-\omega_2) \cdot exp[j(2\omega_1 - \omega_2)t] \tag{3.20}$$

This part is directly contributed by the nonlinearity of g_{m3}. The second part of nonlinear current is:

$$i_{out3}(2\omega_1 - \omega_2) = -\frac{3}{4} \frac{g_{b2}^2}{g_{b1}} H_1(\omega_1) H_1(\omega_1) H_1(-\omega_2) \cdot exp[j(2\omega_1 - \omega_2)t] \tag{3.21}$$

This part is generated by mixing the current of the fundamental frequency and the second harmonic frequency. The second part is normally small compared with the first part because of the small g_{b2} compared with g_{b3} as shown in Figure.3.2. The transconductance of common gate transistor is obtained by fixing the gate voltage and sweeping the voltage

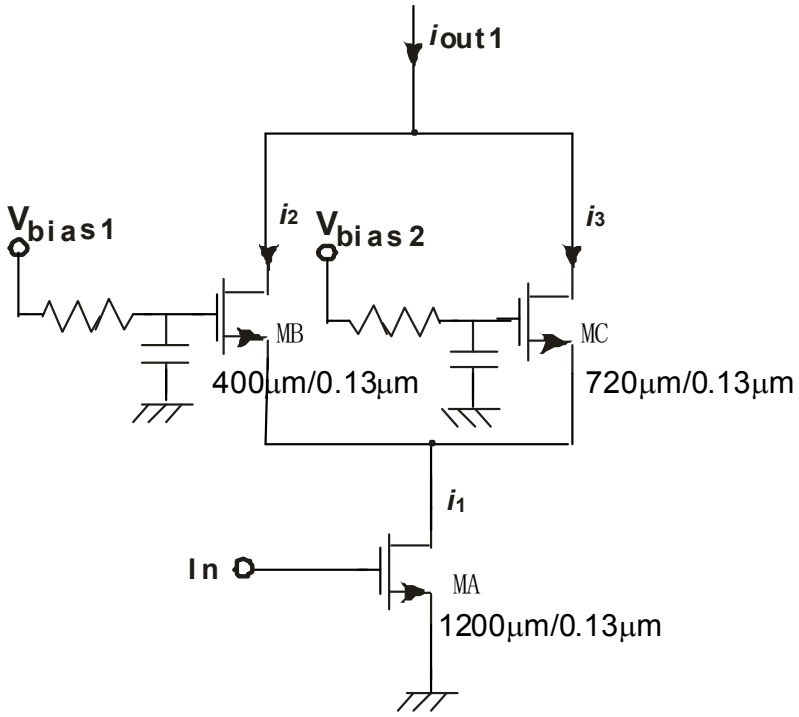


Figure 3.3: Proposed multi-cascode transistor with post-linearization technique.

in the source. The g_{b2} is the differential of transconductance and g_{b3} is the differential of g_{b2}. It is assumed that the $\omega = 2\omega_1 - \omega_2$ nonlinear current is only contributed by the first part. If the $\omega = 2\omega_1 - \omega_2$ nonlinear current becomes zero, the IMD generated by the cascode stage is also zero and eliminated. Therefore, in this paper, a novel multi-cascode post-linearization technique is proposed to cancel the nonlinearity current at $\omega = 2\omega_1 - \omega_2$. The simplicity of the proposed circuit is shown in Figure.3.3.

The 3rd-order derivative of the dc transfer characteristic is g_{m3b} of transistor MB and g_{m3c} of transistor MC. The bias condition of transistor MB is in class-AB and that of transistor MC is closed to class-B. The total g_{b3} of the common gate stage is equal to the addition of g_{m3b} and g_{m3c}. It can be concluded from Figure.3.2 that the positive g_{m3c} compensates the negative g_{m3b} and there is a range of Vgs that the total g_{b3} is very small.

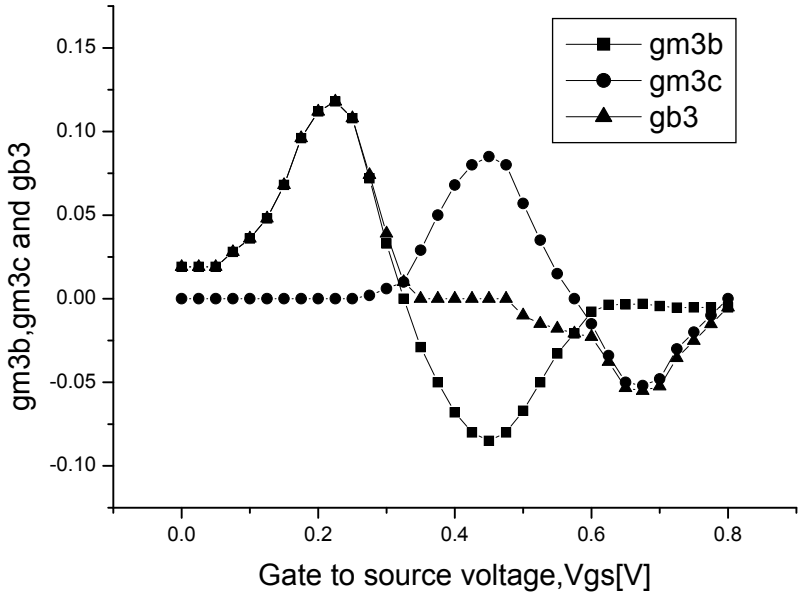


Figure 3.4: g_{m3} of proposed multi-cascode PA.

During this input range, large signal g_{b3} and small signal g_{b3} are very small. Thus, the bias voltage should be selected to enlarge this range. By optimizing the size and bias voltage of the transistor MC and transistor MB, the Vgs=0.20 V of the transistor MC and Vgs=0.44 V of the transistor MB are obtained. The NMOS transistor Vth is 0.15 V and bias voltage of transistor MC is very near Vth. The total g_{b3} is kept small for a large input range as shown in Figure.3.4, where the curve of g_{m3c} has been moved along the positive X-axis by 0.24 V to show the effective range of the g_{b3} compensation in the proposed technique. As shown in Equation.3.14, the IMD directly generated by g_{b3} is canceled.

When the second nonlinear current part is considered with the first nonlinear current part, the principle is analyzed as following: the g_{b2} and g_{b1} are positive, the second nonlinear current part always generates negative nonlinear current. In a conventional cascode PA, this part is added to negative nonlinear current generated by the first part. Thus, the whole linearity is deteriorated. In the proposed post-linearization technique, the transistor MC contributes positive nonlinear current. By increasing the size of transistor MC,

g_{m3c} and the positive nonlinearity current are also increased. Thus, the increased positive nonlinearity current can compensate the negative nonlinear current generated by the second part caused by transistor MB and transistor MC.

If the combination of transistor MA and transistor MB is regarded as a conventional cascode amplifier, the transistor MC is a linearizer with a positive g_{m3c}. The transistor MC generates a nonlinear current with opposite phase to cancel the nonlinear current generated in the conventional amplifier.

3.2.3 Matching Network Design

The load impendence is very important for PA, because the output power and efficiency is decided by the load impendence. In order to decide the load impedance, load pull technique is used in Agilent ADS [67]. The contours for constant 1-dB compressed output power and efficiency contours are plotted on a Smith chart as show in Figure 3.5. An optimized impedance of 8.25+j12.95 is chosen for the PA considering the efficiency and output power.

The main function of an output matching network is to transform the antenna impedance to an appropriate level at the output of the amplifier. All the discussions that follow pertain not only to a linear amplifier design but also to nonlinear amplifier design. In this work, it focuses only on the lumped-element matching network. As the impedance transformation ratio increases, a single L-match stage may not be optimal in terms of insertion loss. Multistage L-match may have lower insertion loss if the reactive component or components have low Q, even though the impedance transformation ratio is not high. Thus, in this design, the second order π type high pass matching circuit is used for output match. It consists of two inductors and one capacitor as shown in Figure 3.6.

The output matching network is fully integrated on a chip. The on-chip CMOS inductors have quite poor performance. In this process, there are seven metal layers as shown in Figure 3.7. The metal of the top layer is aluminum and the metal of the lower six layers is copper. The top two layers are very thick and they are far away from the substrate.

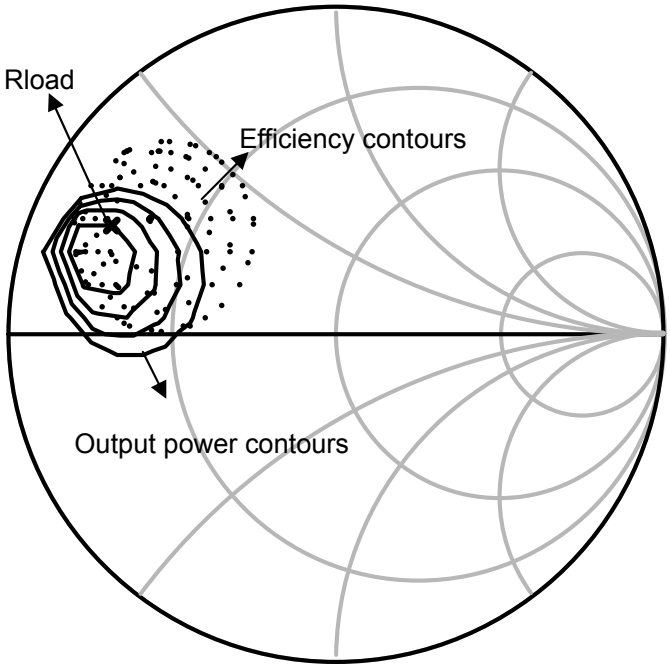


Figure 3.5: Efficiency and output power contours of the PA.

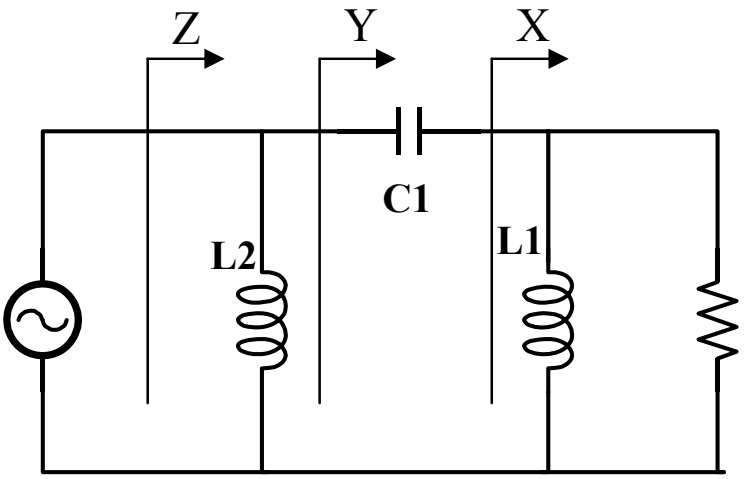


Figure 3.6: The π type high pass matching circuit.

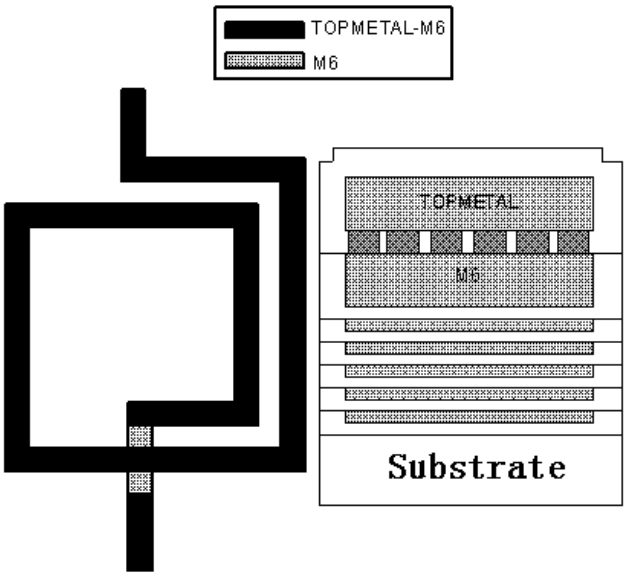


Figure 3.7: The metal layers in the CMOS process.

Thus, by using these two layers, it is capability to design a inductor with a small parasitic resistance and capacitance between the loss substrate and the quality factors are improved. The metal width of 10 μm for inductors is chosen considering the DC parasitic resistance of metals and parasitic capacitance between inductors and Si substrate.

In the π type high pass matching circuit, the two inductances 0.75 nH and 1.1 nH are optimized from Agilent ADS. The inductor simulations were carried out in Ansoft HFSS. The parameters such as inductance and quality factors of these two inductors were extract from the Z-parameters obtained from HFSS as follows:

$$L_p = \frac{Im(Z_{11})}{Re(Z_{11})} \tag{3.22}$$

$$Q_p = \frac{Im(Z_{11})}{\varpi} \tag{3.23}$$

The extracted inductance and quality factors of the two inductors are show in Figure 3.8 and Figure 3.9. The 0.75 nH inductor varies from 0.75 nH to 0.8 nH at 1 GHz and 10 GHz, respectively. The 1.1 nH inductor varies from 1.1 nH to 1.25 nH at 1 GHz and 10 GHz,

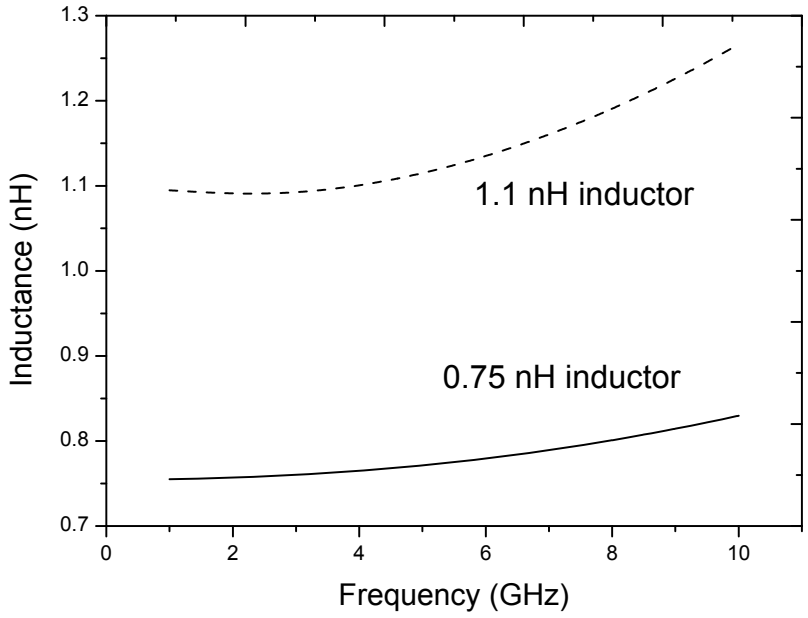


Figure 3.8: The simulated inductance of the inductors.

respectively. The quality factor for 0.75 nH inductor is 11 at 5.8 GHz and that of 1.1 nH inductor is 14 at 5.8 GHz.

The metal-insulator-metal (MIM) capacitors are used for input and output matching. The transformation of the impendence is shown in Figure 3.10. Firstly, the the 50 Ω load is transformed to the normalized impendence of 0.41+j*0.45 by the parallel inductor. Secondly, the normalized impendence of 0.41+j*0.45 is transformed to normalized impendence of 0.45+j*0.27 by a series capacitor, usually, this series capacitor is very large to pass the output power. At last, the impendence is transformed to normalized impendence of 0.17+j*0.26 by a parallel inductor. This inductor also connect to the power supply and provide the power for the PA.

The input matching circuit is designed for a complex conjugate match for large gain. However, if the input matching network has a high gain, there is a probability of oscillation of the PA. Thus, additional care needs to prevent any instability.

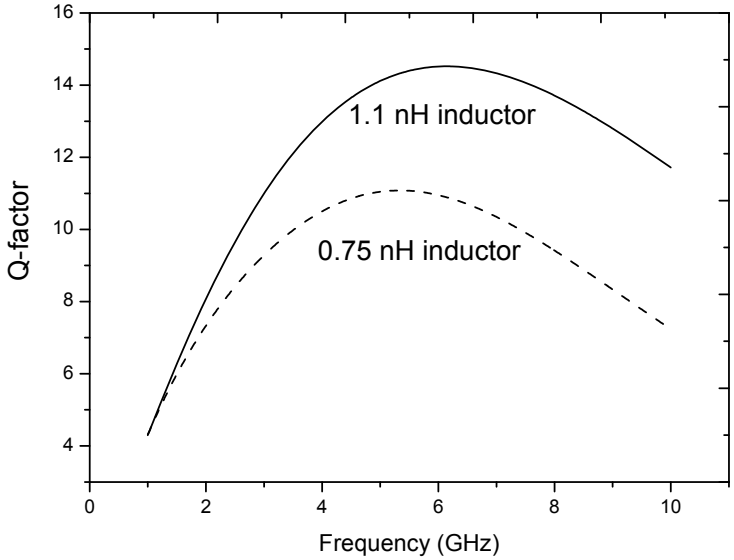


Figure 3.9: The simulated Q-factors of the inductors.

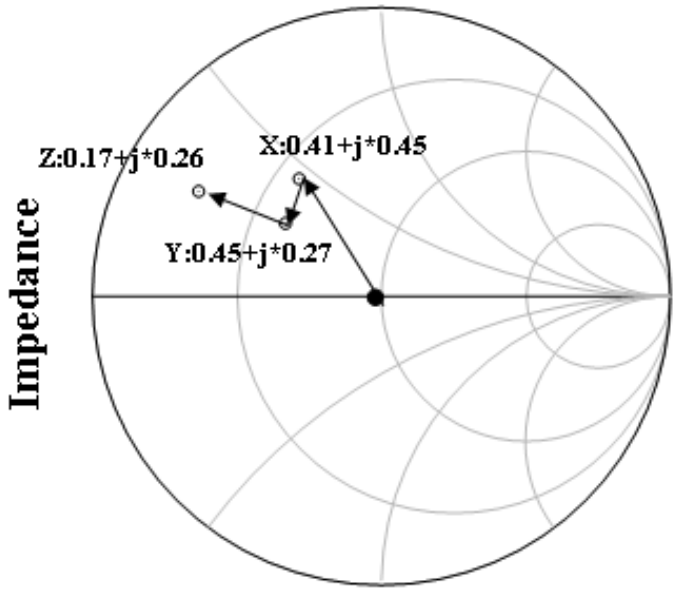


Figure 3.10: The impendence conversion of the matching circuit.

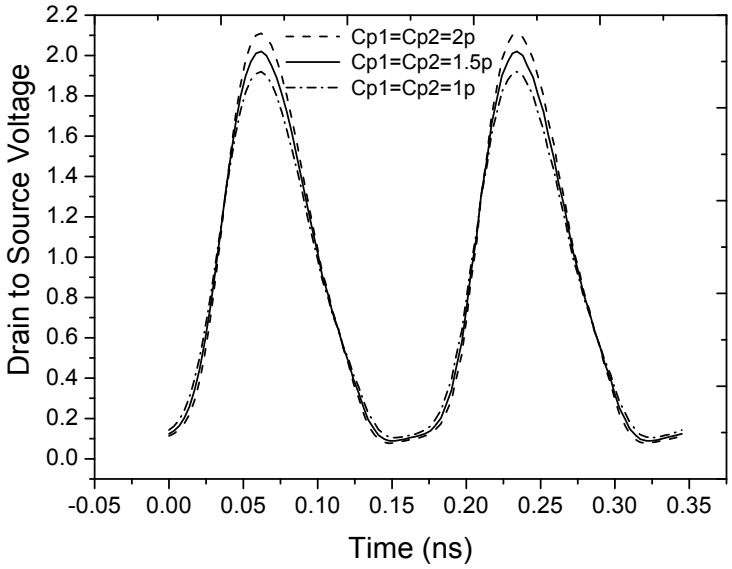


Figure 3.11: The simulated drain to source voltage with different bypass capacitance.

3.2.4 Stability Design

Normally, the bypass capacitors of Cp1 and Cp2 are large and the gate potential of the cascode is AC ground. However, in this design, the capacitance of Cp1 and Cp2 are optimized for two goals:

1) To increase the stability of the PA.

2) To limit source-drain voltage swing across cascode stage within the breakdown voltage.

If bypass the gate potential of the cascode to AC ground, a quite large capacitance is necessary, which costs a large area. By not completely bypassing the cascode gate, Cgd of the cascode transistor and the bypass capacitor (Cp1 and Cp2) form a capacitive divider, which allows the voltage swing at cascode gate to be in phase with the output node. This reduces the maximum voltage across the oxide region of the cascode transistor, as shown in Figure 3.11. The simulation is carried with Cp1=Cp2=1.5 pF and Cp1=Cp2=2 pF. With the Cp1=Cp2=2 pF, the drain to source voltage exceeds the breakdown voltage of 2 V.

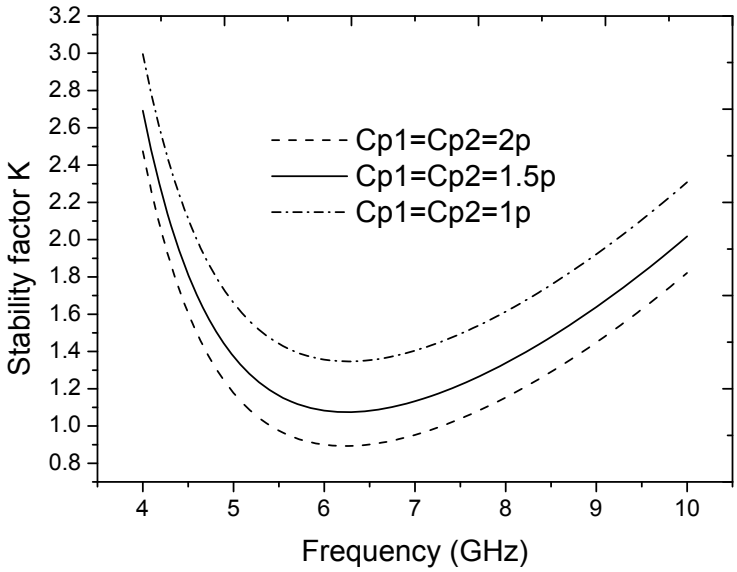


Figure 3.12: The simulated stability with different bypass capacitance.

With a limited bypass capacitance, the gain of the transistor decreased and the stability increased. The stability factor K is a convenient way of expressing the necessary and sufficient conditions for unconditional stability [68]. To guarantee the stable operation of the amplifier, the stability factor K should be bigger than one. However, with large stability factor K, the gain is too low and it affects the efficiency of the PA. The simulation was carried out with Cp1=Cp2=1 pF, Cp1=Cp2=1.5 pF and Cp1=Cp2=2 pF. As shown in Figure 3.12, With a Cp1=Cp2=1.5 pF, the stability factor K is about 1.1 and this is an optimization capacitance used for both Cp1 and Cp2 in this design.

3.3 Overall Simulation Results

The bias current of the PA has strong relation with the output P1dB and PAE. Thus, the bias current is carefully selected in the simulation. As a result, the bias current of 24.0 mA is chosen for this PA design.

The output average power for DSRC applications using QPSK modulation method

is 10 dBm. Since the PAR is about 2 dB, it is considered that 4 dB back-off from P1dB is sufficient to meet the specifications of the linearity. Thus, considering the power loss of 3 dB between the PA and antenna, the required output P1dB is 17 dBm. Schematic of the proposed novel linear PA is shown in Figure 3.13. Compared with a conventional cascode PA, two transistors are used for the common gate stage. The sizes of the transistors are optimized in Agilent ADS. The transistors MA, MB and MC MC have a gate length of 0.11 μm and a gate Figure width of 10 μm. The transistors MA consists of 120 The transistor MB consists of 40 fingers and MC consists of 72 fingers. The bias circuits for the transistors MB and MC are made up of resistors as shown in Figure 3.13. The values of these resistors decide the bias voltages of the transistors MB and MC. The load line of the PA changes with output power, thus after optimizing the output IMD, the Vgs=0.48 V of transistor MB and Vgs=0.18 V of transistor MC are decided. The quiescent current of the linearizer transistor MC is only 0.2 mA and it is biased near Class B, thus the efficiency of transistor MC is very high. The whole efficiency of the PA is not deteriorated by the linearizer.

The simulation was carried out with a quiescent current of 24.0 mA and a supply voltage of 2.0 V. The S-parameter simulated results is shown in Figure 3.14.

This single stage has a small gain of 12 dB, the input return loss is -18 dB and the output return loss is -4.5 dB at 5.8 GHz. Thus, the small signal output return loss is not very good. However, there is a interesting thing to look at the large signal output return loss as shown in Figure 3.15. As the input power increases, the output return loss becomes better. And when near the input P1dB of 5.6 dBm, the output return loss becomes -17. Thus, it can be concluded that the inset loss in the output match decreases with the large output power. The reason for this change is that the linearizer transistor MC works in a near Class-C state, and the output impendence of the linearizer transistor MC largely changes with the output power. The parallel impedance of the transistor MC and transistor MB become small and the output return loss becomes better.

The simulated input-output response at 5.8 GHz is shown in Figure 3.16. As shown in the Figure, the gain is very flat and output P1dB is 17.5 dBm. The simulated

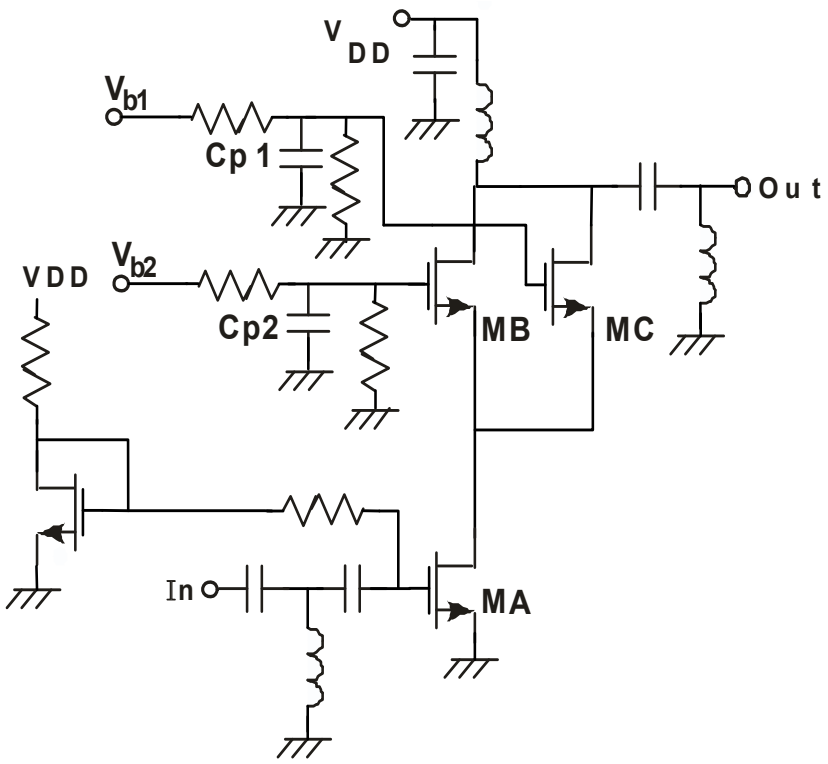


Figure 3.13: Schematic of the novel PA.

PAE at 5.8 GHz is shown in Figure 3.17. The PAE at the P1dB is 37%.

The operational condition of the common source transistor and common gate transistor are very important. And the operational condition of the transistor can be seen from the load line because we can see clearly the voltage, current and the load impedance directly. The load line of the transistor MA and transistor MB (transistor MC) are shown in Figure 3.18 and Figure 3.20. Five circles are drawn in the Figure and the largest circle shows operational condition of P1dB. As shown in Figure 3.18 and Figure 3.20, the maximum current is 180 mA. In order not to exceed the breakdown voltage, the drain to source voltage is limited in 2V for both transistor MA and transistor MB (transistor MC). The slop of the circles indicates the load impedance of the transistors.

To show the effectiveness of the linearity improvement of the proposed circuit, the simulation is carried out with different sets of Vgs and the same total drain to source

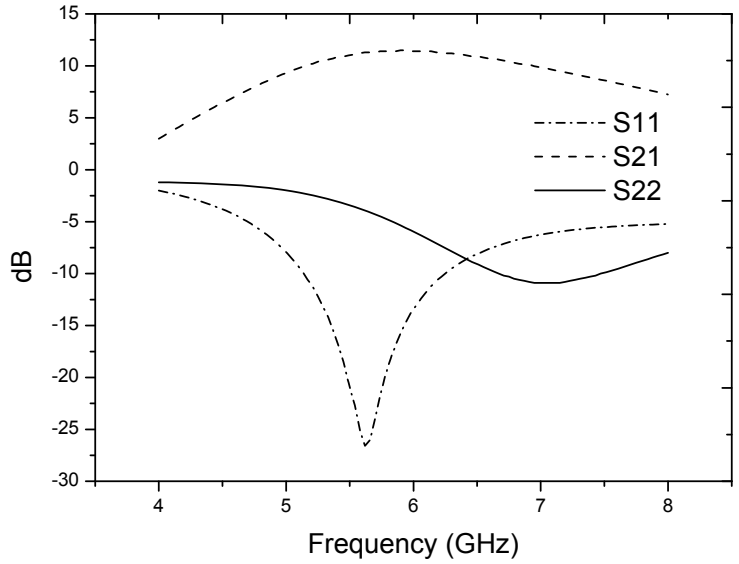


Figure 3.14: Simulated S-parameter performance.

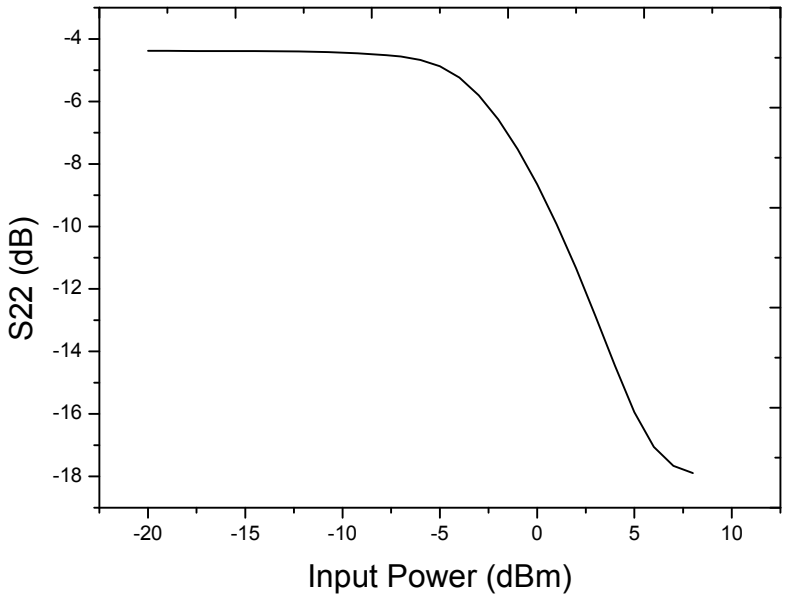


Figure 3.15: Simulated large signal S22 at 5.8 GHz.

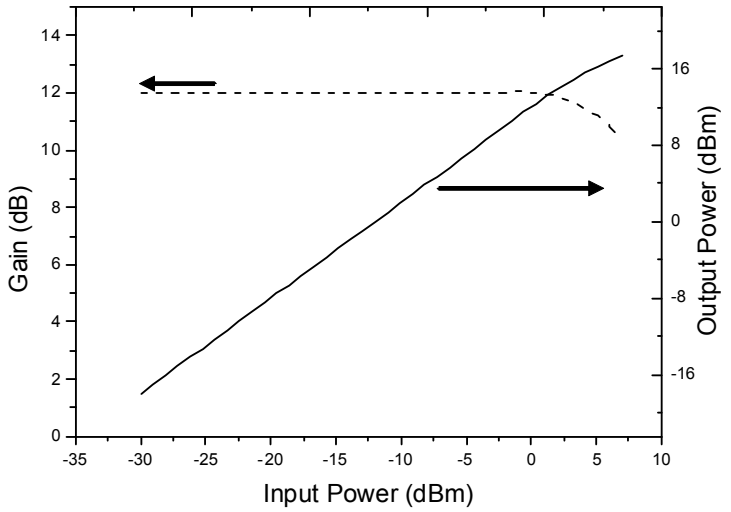


Figure 3.16: Simulated input-output response at 5.8 GHz.

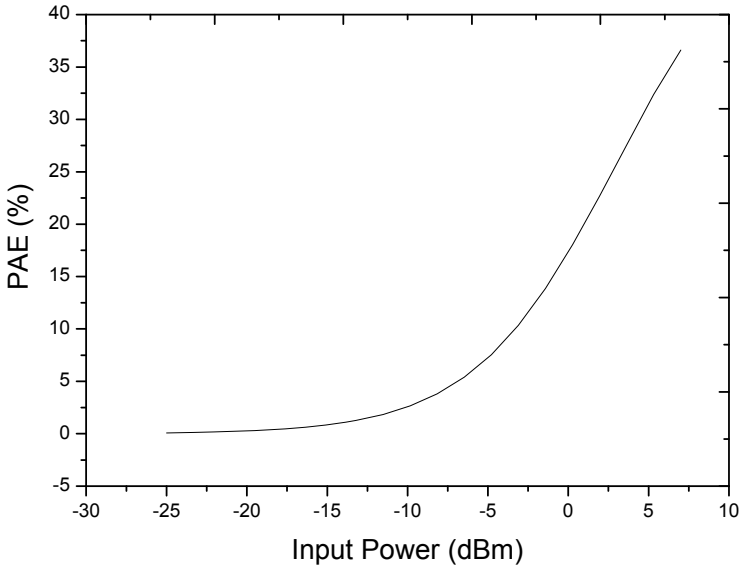


Figure 3.17: Simulated PAE at 5.8 GHz.

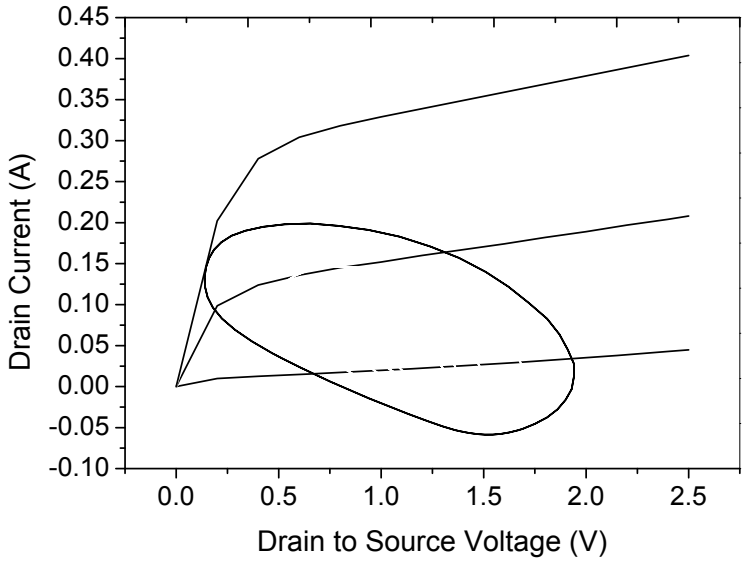


Figure 3.18: Simulated loadline of the common-gate transistor.

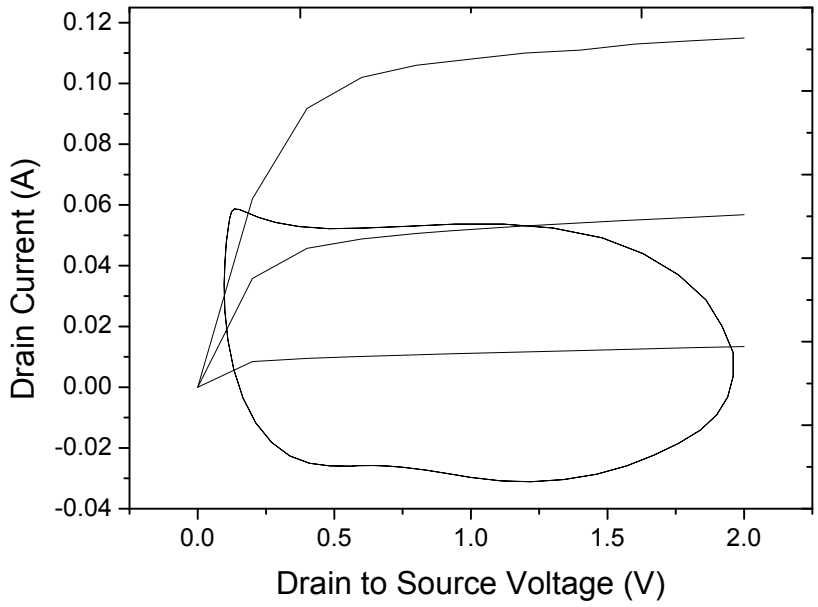


Figure 3.19: Simulated loadline of the common-source transistor MB.

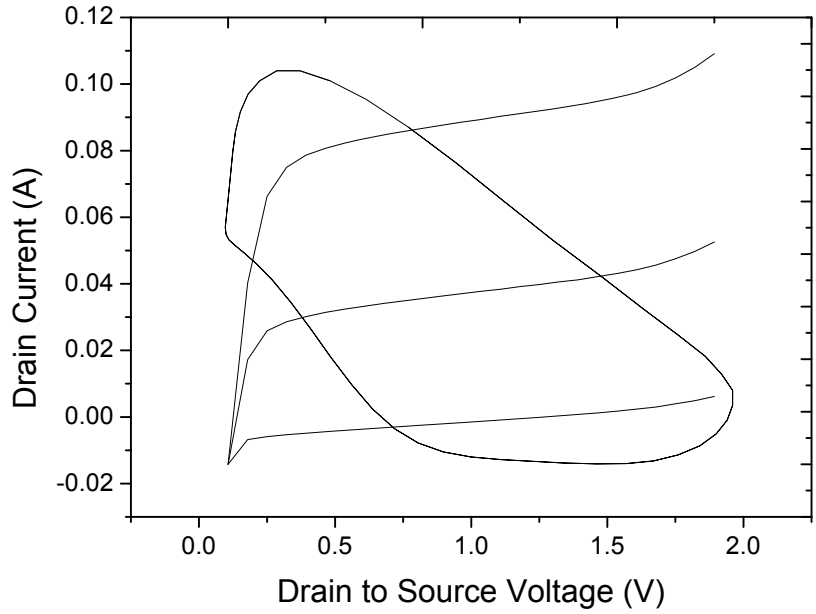


Figure 3.20: Simulated loadline of the common-source transistor MC.

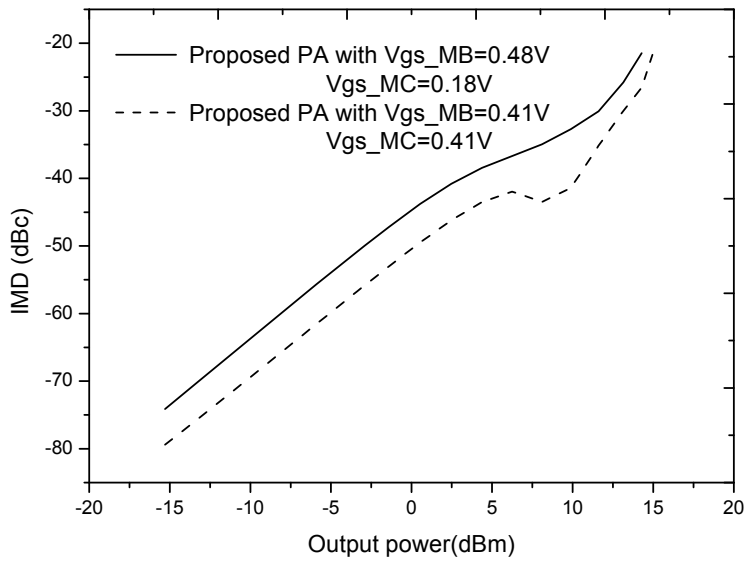


Figure 3.21: The simulation comparisons of the IMD with different Vgs in common gate stage.

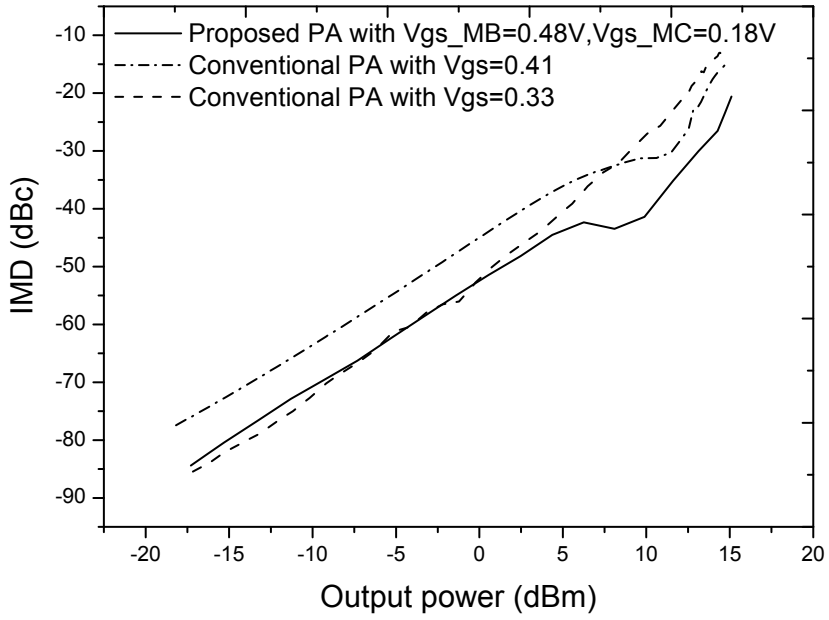


Figure 3.22: The IMD simulation of the conventional PA with different Vgs in common gate stage.

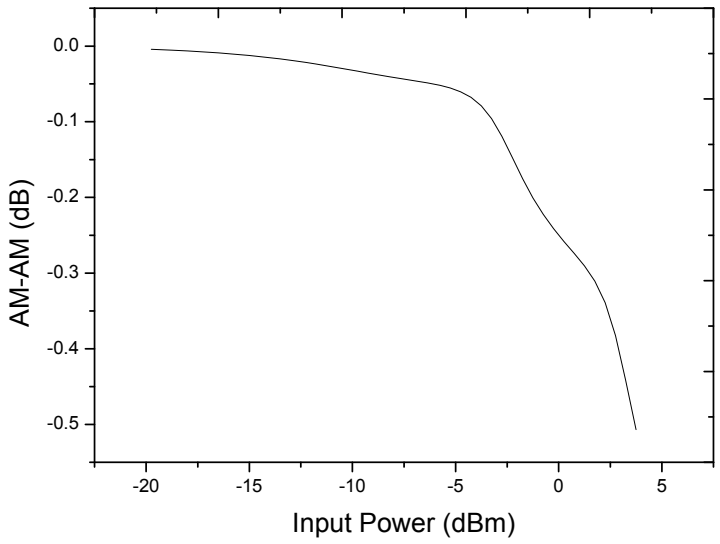


Figure 3.23: Simulated AM-AM conservation.

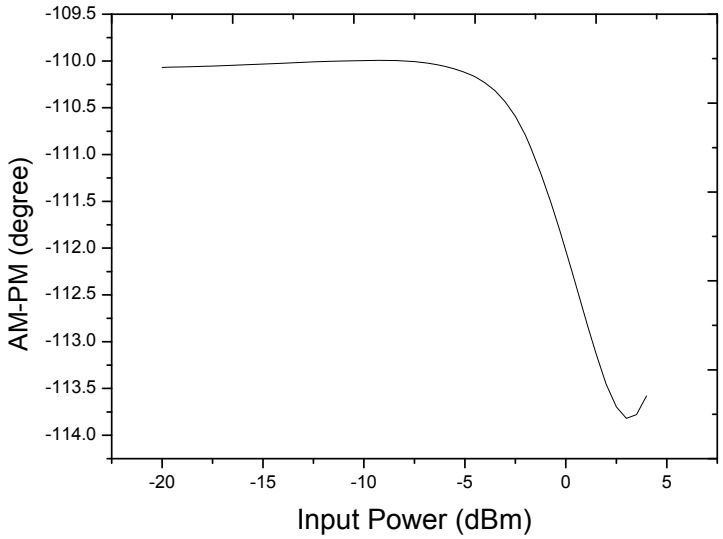


Figure 3.24: Simulated AM-PM conservation.

quiescent current. One bias set is with Vgs=0.48 V of transistor MB and Vgs=0.18 V of transistor MC, and the other set is with Vgs=0.41 V of transistor MB and transistor MC. In the first case, it has the effect of g_{m3} canceling. In the second case, there is no effect of g_{m3} canceling as a conventional PA because of the same Vgs. As shown in Figure.3.21, the proposed PA with Vgs=0.48 V of transistor MB and Vgs=0.18 V of transistor MC shows an IMD improvement of 6 dB.

The simulation is also carried out with different sets of Vgs of common-gate transistor by changing the width of the common-gate transistor in the conventional cascode PA. The conventional cascode PA has the same input and output matching networks as shown in Figure.3.13, however, there is no transistor MC in the common-gate stage. In the conventional cascode PA, the common-source transistor and common-gate transistor have a gate length of 0.11 μm and a gate finger width of 10 μm. The common-source transistor consists of 120 fingers and common-gate transistor consists of 110 fingers. It has the same bias current as the proposed circuit with a Vgs=0.41 in the common-gate stage, and the simulation result shows a similar performance compared with the proposed circuit at

Vgs=0.41 of transistor MB and transistor MC. Then, the size of the common-gate stage is optimized to set the Vgs=0.33 where the g_{m3} gets across the zero. This shows the conventional method to improve the linearity in cascode PA. The simulation shows that the IMD improves in small signal region as shown in Figure.3.22. Compared with the conventional method, proposed circuit also improves the IMD in large signal region.

AM-AM conversion and AM-PM conversion are shown in Figure 3.23 and Figure 3.24. The AM-AM conversation is only 0.5 dB difference up to P1dB output. The phase of the AM-PM is from 110 degree to 113.7 degree, and there are only 3.7 degree difference.

3.4 PA Layout

The PA has a large output power, thus the transistor size is also large. The layout should be carefully designed to avoid the parasitic resistance, parasitic inductance and parasitic capacitance. There are many ways to layout one structure. Trade-offs have to be made based on different considerations of each individual case.

The power transistor has a very large size, for example, the common source transistor has a gate length of 0.11 μm and width length of 1.2 mm. If only one transistor with one figure is used, the metal interconnect of the length of 1.2 mm maybe contains several ohm resistance. And this resistance is comparable with the load impendence. Thus, a large of voltage drop on the parasitic resistance and the output power also wastes on this parasitic resistance. It deteriorates the efficiency of the PA. Commonly, a large power transistor can be obtained by connecting unit cells in parallel. The dimension of the unit cell is determined by the frequency and parasitic resistance. The distance between unit cells is another factor under consideration by the designer during layout. Decreasing of this distance is of course the advantage from integration density perspective. However, this results in higher chip temperature due to heat flow degradation. If the distance is too large, parasitic elements will degrade the RF performance. In order to minimize the source resistance, which degrades the gain, output power and efficiency, the source electrode is contacted on both sides

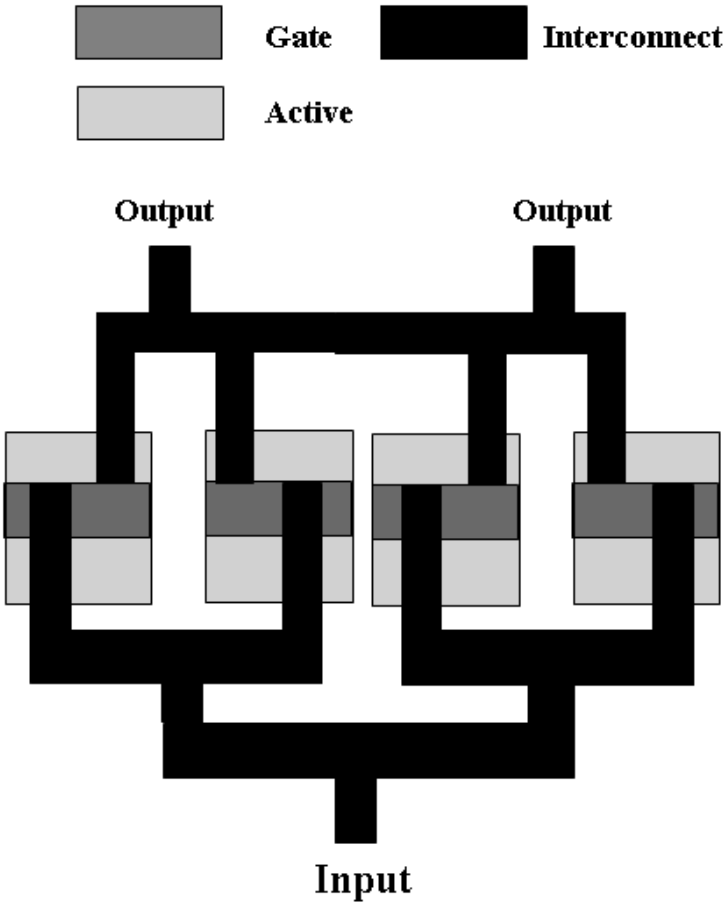


Figure 3.25: The common-source transistor layout.

of the transistor.

Assembling smaller unit transistors into a much larger power transistor entails a trade-off between the chip size and the delay equalization. If the delay for each transistor is different, it will degrade the performance greatly, since signals from each unit transistor will not sum up in phase. Furthermore, some unit transistors experience excessive voltage drops comparing to others, and current is not evenly distributed in the device. To avoid these problems, the common source transistor are layout as shown in Figure 3.25. It is called tree layout. The common source transistor is divided into four unit transistors and the signal

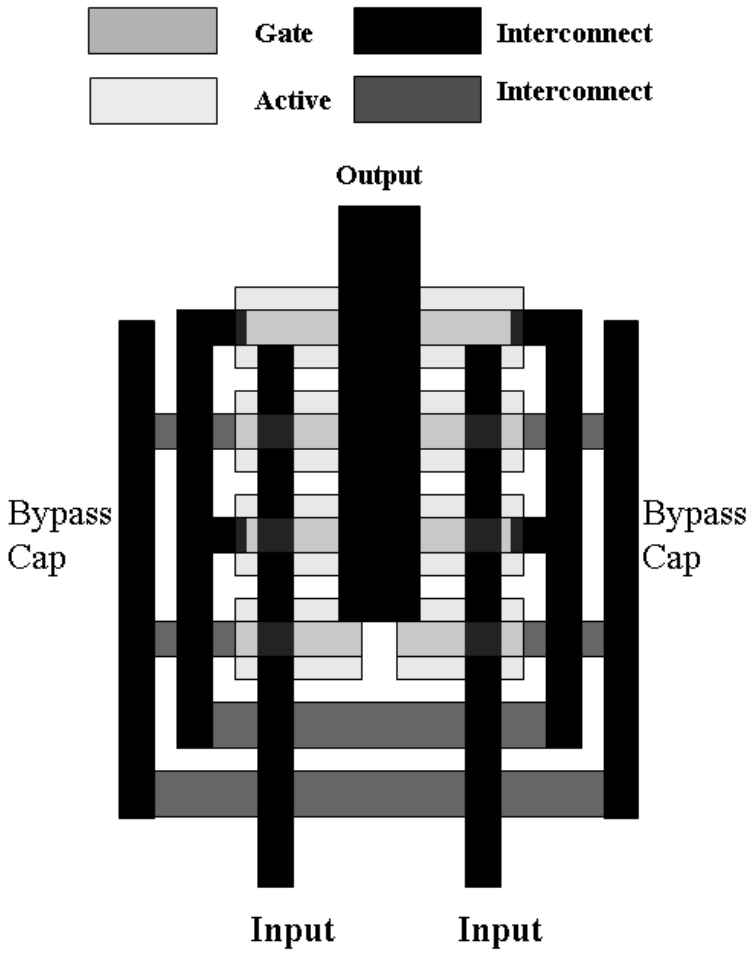


Figure 3.26: The common-gate transistors layout.

will reach each unit transistor simultaneously, and the output from each unit transistor will arrive at the summing point simultaneously.

The common gate power transistor layout is much more difficulty than the common source power transistor because of the proposed multi-cascode architecture. There are two transistors in the common source stage with the common source input and drain output, however, the gate is not connected as in a conventional transistor. The matching of the two transistors are very important because if these two transistors mismatch, the performance of the gm3 compensation also get worse. The common gate power transistors layout are shown

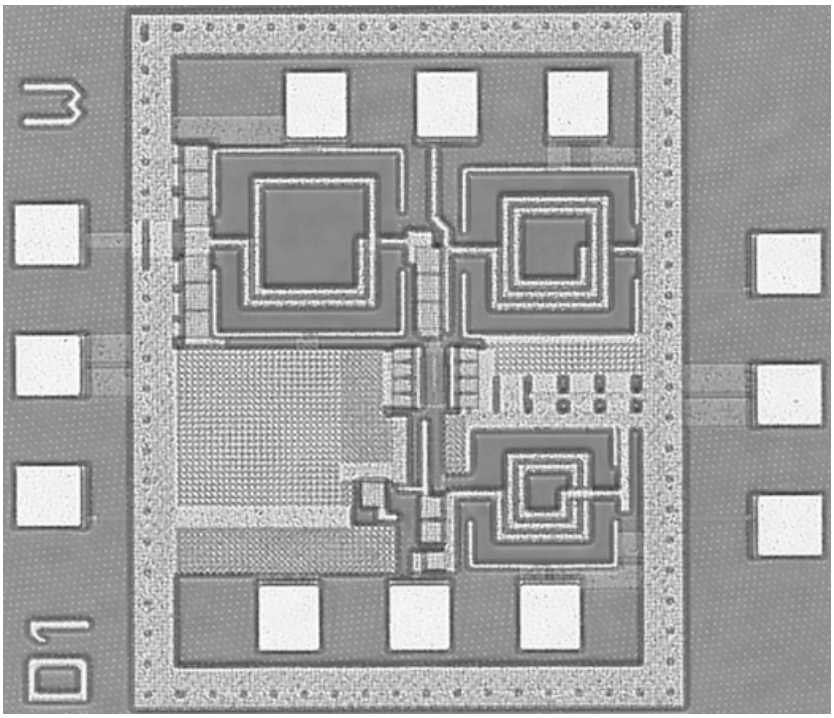


Figure 3.27: Photograph of the fabricated PA (800 μm by 870 μm).

in Figure 3.26. Each transistor are divided into four unit transistors. And these four unit transistors are crossing interconnects with each other. Thus, this crossing interconnects cancels the effect caused by the non-ideal process. And in this case, the two transistors match well from each other.

3.5 Experiment Results

The PA was fabricated by 0.13 μm CMOS process. The photograph of the fabricated PA is shown in Figure 3.27. The PA occupies an area of 800 μm by 870 μm including all pads.

The measurements were carried out on wafer. No off-chip matching elements are needed. The amplifier is tested with a low supply voltage of 2.0 V at quiescent drain current of 24.0 mA. Firstly, the small signal performance measurements were performed on network

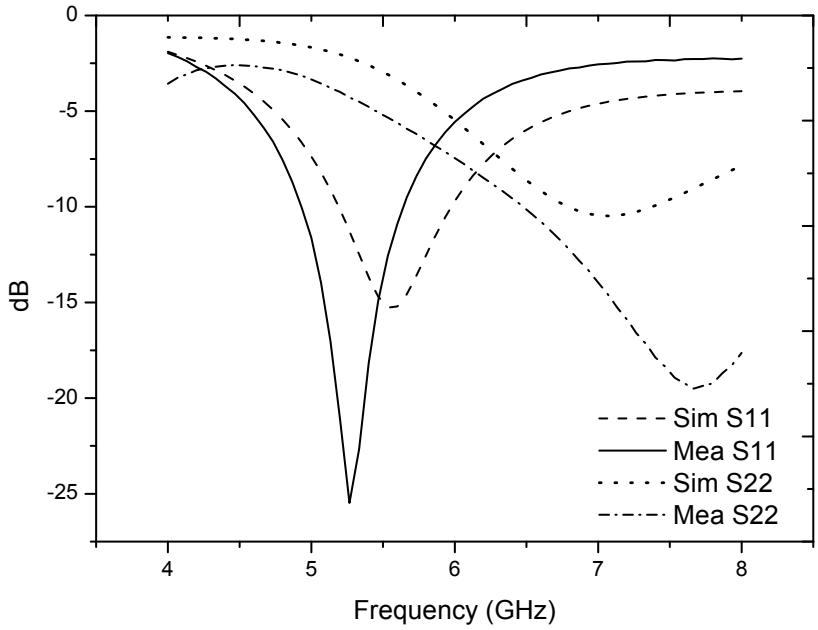


Figure 3.28: Measured and simulated small-signal performance of S11 and S22 of the PA.

analyzer of Agilent E8361A. Figure 3.28 and Figure 3.29 show the small signal measured results with simulated results. The small signal gain is 11.5 dB, the input return loss is -7.5 dB and the output return loss is -6.5 dB at 5.8 GHz.

Next, the single-tone signal is used to test the large signal performance. Measured input-output response at 5.8 GHz is shown in Figure 3.30. The measured output P1dB is 17.3 dBm and the measured saturated output power is 18.6 dBm. The measured efficiency of the PA at 5.8 GHz is shown in Figure 3.31. The measured PAE at the P1dB is 32% and the peak PAE is 33.8%. The maximum drain efficiency (DE) of the PA is 43%. The measured DC current consumption increases at the P1dB compared with the simulated results and the output P1dB is well agreed with the simulated one. Thus, the load line slope of the PA rises compared with simulated result because of the difference between simulated between simulated and measured output matching circuit as shown in Figure 3.28. In addition, the gain decreases because of the increased input return loss compared with simulation one, thus, the PAE of the PA decreases by 5% at the P1dB compared with simulation result.

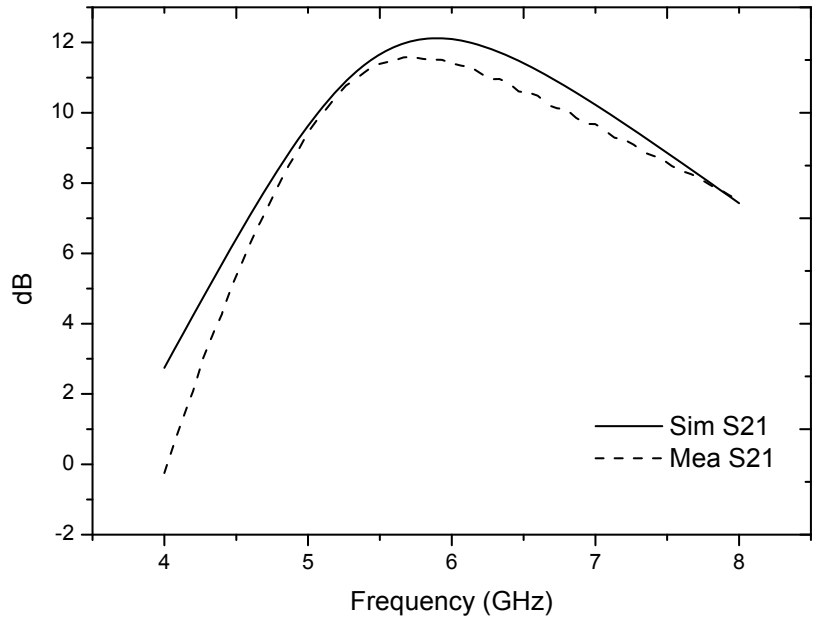


Figure 3.29: Measured and simulated small-signal performance of S21 of the PA.

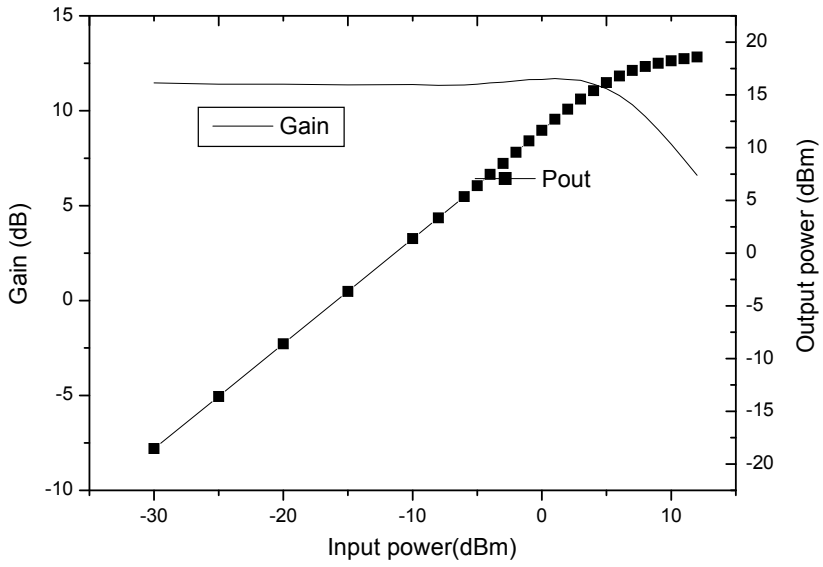


Figure 3.30: Measured input-output response at 5.8 GHz.

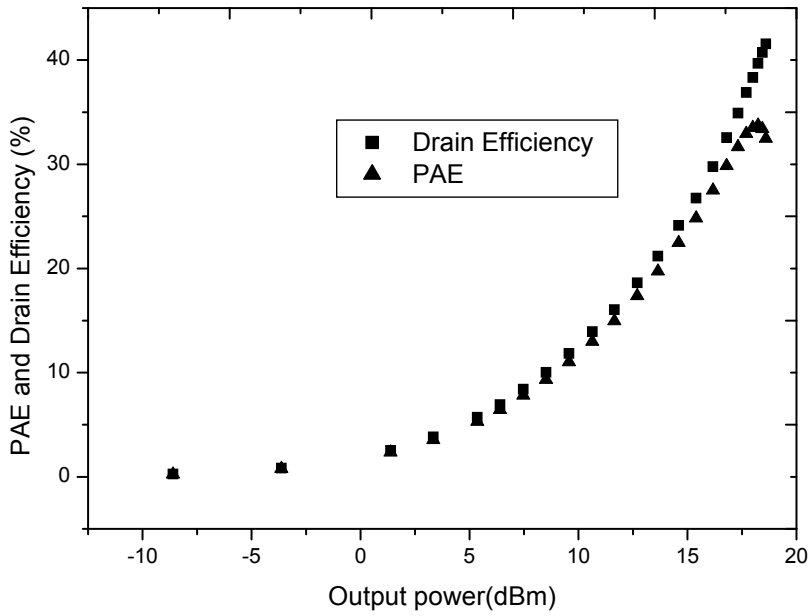


Figure 3.31: Measured PAE and Drain efficiency at 5.8 GHz.

A two-tone test was performed at the center frequency of 5.8 GHz with a space of 1 MHz. To verify the effectiveness of the novel linearization technique, a conventional cascode PA with the same process was fabricated and measured with the same operating current. The conventional cascode PA has the same input and output matching networks as shown in Figure 3.13, however, there is no transistor MC in the common gate stage. Figure 3.32 the measured IMD of the proposed and conventional PA. The proposed PA exhibits an improved IMD of 6 dB over large output power range and the maximum improvement of 12 dB. The measured OIP3 is as high as 27.3 dBm. With the proposed novel multi-cascode technique, the PA shows a considerable improvement in linearity.

Table 3.2 summarizes the performance of the proposed PA and recently reported PAs. The other works are all operate during 5 GHz – 5.8 GHz, and the PAE or drain efficiency (DE) are below 30%. The proposed novel PA exhibits excellent PAE compared to another works with similar P1dB.

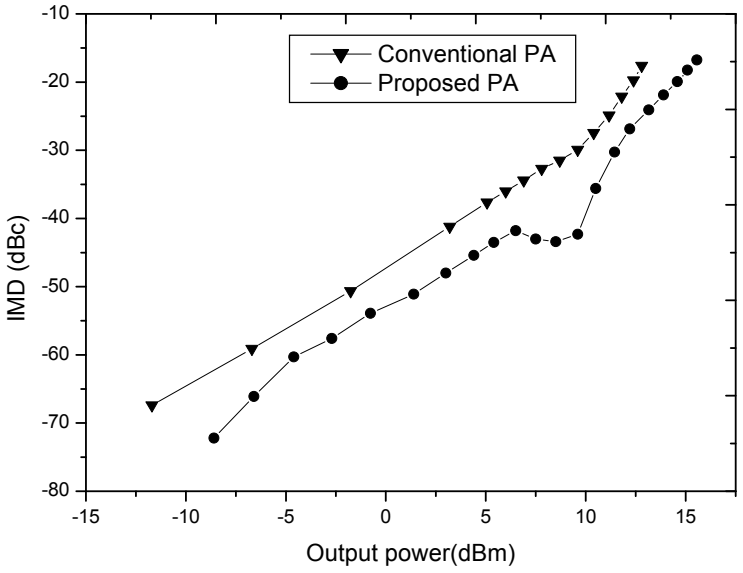


Figure 3.32: The comparisons of the IMD between the proposed and conventional PA.

Table 3.2: COMPARISON OF THE PROPOSED PA WITH RECENTLY REPORTED PA

Reference	Frequency (GHz)	P1dB (dBm)	PAE	Chip area (mm^2)	Process CMOS (μm)	Voltage (V)
This work	5.8	17.3	32%@P1dB	0.7	0.13	2.0
[69]	5.2	17.1	23%@P1dB	1.26	0.18	2.5
[70]	5.25	16.5	20%@MAX	1.36	0.18	2.4
[71]	5.8	20.5	27%@MAX	0.81	0.09	1.0
[72]	5	15.4	27.1%@MAX	0.84	0.18	1.8
[73]	5.2	16	23%@P1dB	N/A	0.18	3.3

3.6 Summary

In the chapter 3, the deign of high linearization and high efficiency PA are introduced for high speed wireless communications with linear modulation. First, the transistor

level linearizations and system level linearizations technique are researched in this chapter. Especially, the drawbacks of post linearization technique which widely used in small signal amplifier is researched. And based on these technology, the multi-cascode post linearization technique is proposed. In the theory, this chapter explains the principle of the proposed multi-cascode post linearization technique.

The novel linearized PA has been demonstrated using 0.13 μm CMOS technology for 5.8 GHz DSRC applications. The PA has exhibited an output P1dB of 17.3 dBm with a PAE of 32% and obtained an maximum IMD improvement of 12 dB with an OIP3 as high as 27.3 dBm.

Chapter 4

CMOS Class-G Supply Modulation for Polar PAs with High Average Efficiency and Low Ripple Noise

4.1 Overview

PAs usually consume a significant power in wireless communication systems. Therefore, increasing the average efficiency of the PAs is quite critical for long run-time portable wireless communication systems and the research on high average efficiency PAs design is very popular in these years. Recently, the supply modulation gains popularity in modern wireless transceiver systems for polar transmitter and the applications of the supply modulation cover many high performance, high data rate linear modulation transmitters (i.e., EDGE, CDMA, WCDMA, 802.11g WLAN) [100]-[108].

As shown in Figure 4.1, in the polar modulation transmitter architecture, the phase modulated signal with constant envelope is amplified by a non-linear PA (Class-E or Class-F) and the amplitude information is restored via its power supply modulation, conventionally, which usually consists of a hybrid amplifier (a switching PA and a linear amplifier). Therefore, this kind of supply modulation can achieve a relative high aver-

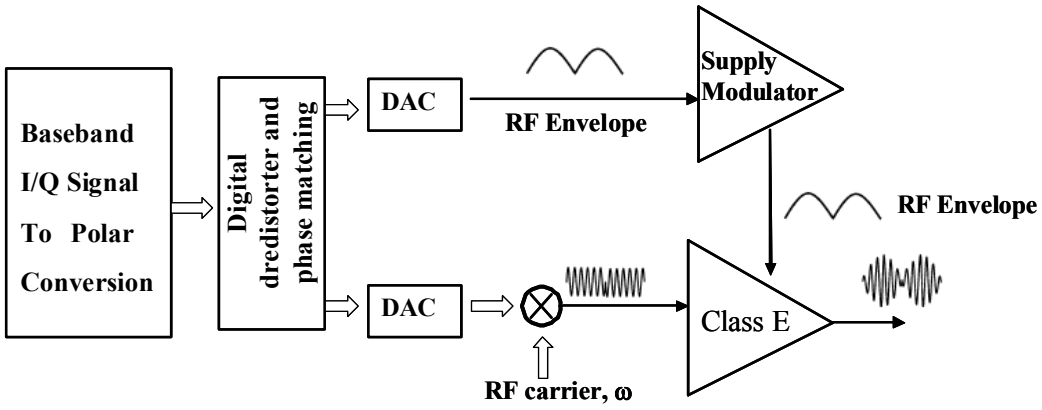


Figure 4.1: Polar modulated transmitter architecture.

age efficiency compared with conventional Class-AB PA. However, in many popular linear modulation transmitters [103], [109] (i.e., CDMA, 802.11g WLAN), the peak output power distribution probability is several dBm and far away from the saturate output power. As the output power decreases, the output current also decreases and so as the supply modulation efficiency. Especially, when the ripple current amplitude provided by the linear amplifier is close to the current amplitude provided by the switching PA, the efficiency of the supply modulation even drops below 30% near peak output power distribution probability of envelope signal. Thus, the average power efficiency of the conventional supply modulation becomes worse.

Another disadvantage of the conventional supply modulation is that the switching noise increases as the output power decreases. The switching noise in the conventional supply modulation is suppressed by the low output impedance of the Class-AB amplifier [105]. As the output power decreases, the Class-AB amplifier output stage works near the linear region, and the gain bandwidth (GBW) decreases as well. The output impedance of the Class-AB amplifier rapidly increases [58]. Thus, the switch noise becomes worse [105]. It severely deteriorates the signal to noise ratio (SNR) of the envelope signal at low input voltage.

In this paper, a CMOS Class-G supply modulation is proposed to solve these two problems. In the high power supply modulation, it consists of a wideband Class-AB linear amplifier and rectangular wave delta modulation (RWDM) switch-mode PA to achieve both high efficiency and high speed. A low dropout (LDO) is utilized to suppress the delta-modulated noise and provide a low ripple noise power supply. In low power supply, only an LDO which is controlled by a switch signal is used. To verify the effectiveness of the proposed supply modulation, the proposed supply modulation was designed with 0.13 μm CMOS process. The conventional supply modulation was also designed for comparison. The simulation result comparisons confirm the effectiveness of the proposed Class-G supply modulation. Without Class-E PA, it shows an average efficiency improvement of 16.6% compared with the conventional supply modulations. With Class-E PA, it shows an average efficiency improvement of 7.1% compared with the conventional supply modulations and an average efficiency improvement of 13.4% compared with a conventional Class-B PA. It also shows an excellent SFDR of -73 dBc with the LDO for noise suppression. The Class-G supply modulation amplifiers were also reported in [110]-[112] to improve the average efficiency of PAs. In this paper, the originality of the proposed Class-G supply modulation, principle analysis and efficiency analysis are described in Section II. And the circuits implementation are introduced in Section III. To verify the effectiveness of the proposed Class-G supply modulation, the simulations were carried out and simulation results comparison and discussions are shown in Section IV and finally Section V summarizes the conclusions.

4.2 The Proposed Class-G Supply Modulation

4.2.1 The Originality of the Proposed Class-G Supply Modulation

There are three originalities in this paper. Firstly, in order to increase the efficiency of the PA, a new architecture of Class-G supply modulation is proposed. In this architecture, hybrid amplifier is used for high power supply and LDO is used for the low power supply. Compared with the other Class-G supply modulation [111], the proposed

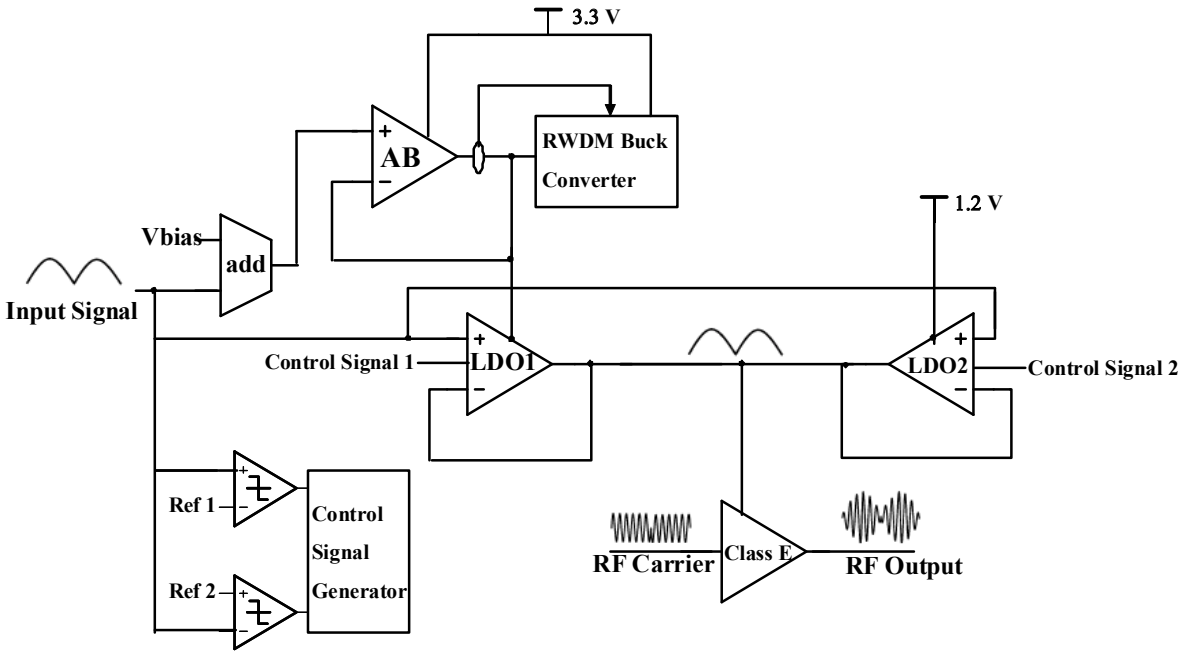


Figure 4.2: The proposed supply modulation with Class-E PA.

architecture has high efficiency in the high power supply. Compared with the conventional supply modulation, the proposed architecture has high efficiency with low output current. Secondly, in order to suppress the noise from the switching PA, a twice noise filtering technique is proposed to suppress the noise of switching PA. The first noise filter is implemented by the low output impedance of the Class-AB amplifier as in conventional supply modulation. The second noise filter consists of the LDO with a novel bias technique for a fixed dropout voltage to make the LDO with high PSRR. With this twice noise filtering technique, the noise is largely suppressed. Thirdly, in order to track the current accurately for the switching PA, an accurate current detector is proposed. The proposed current detector overcomes the inaccuracy introduced by the channel length modulation in conventional current detector [107].

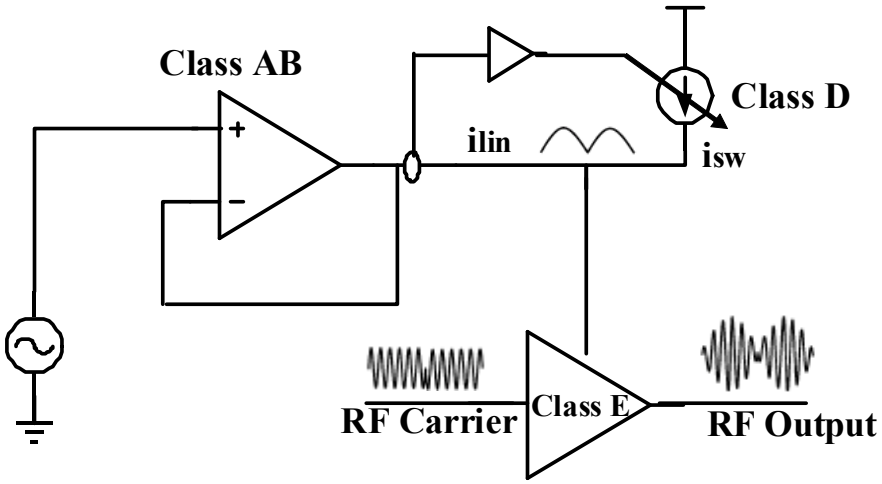


Figure 4.3: Schematic of the conventional supply modulation.

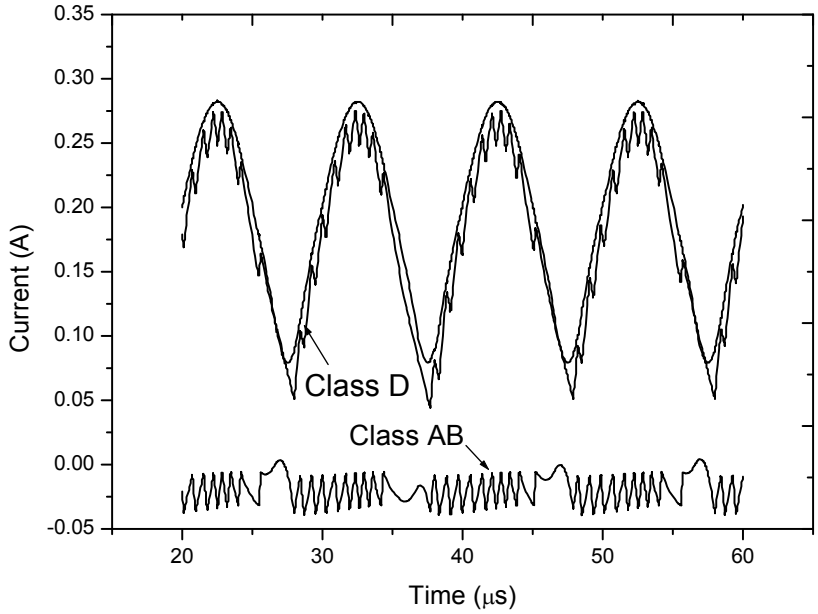


Figure 4.4: Current supplied by Class-AB and Class-D amplifier.

4.2.2 The Principle Analysis

The proposed CMOS Class-G supply modulation with Class-E PA is shown in Figure 4.2. The high power supply is 3.3 V and the low power supply is 1.2 V, which are

commonly used in a chip. In the high power supply part, it consists of a hybrid amplifier and an LDO. The hybrid amplifier comprising of a self-oscillating parallel linear and a switching Class-D PA that is widely used for conventional supply modulation [100]-[108] as shown in Figure 4.3. The linear Class-AB amplifier provides high speed, and it can track the fast variation of the envelope. The switching Class-D PA provides a highly efficiency current serving to supply most of the load current by sensing the current from the linear amplifier. A typical current contributed by Class-AB and switching Class-D PA for an envelope signal is shown in Figure 4.4. It is obviously that the linear amplifier only provides some ripple current, and large current is provided by the switching Class-D PA. Thus, the efficiency of the high power supply is mainly dominated by the efficiency of the Class-D PA. It can achieve a high efficiency up to 89% [108] with a large output current. Traditionally, the pulse width modulation (PWM) [107], [108] is used for the modulation of the switching PAs. However, the PWM modulator has the unstable possibility. Considering the stability of the modulator, in this work, the RWDM is used for modulation of switching PA and it has been used in audio amplifier applications, where it was originally proposed to improve the fidelity of the class-D audio amplifier [113], [114].

To suppress the switching noise, the LDO1 connected as a buffer amplifier is used as shown in Figure 4.2. The output voltage of the hybrid amplifier is used as a power supply for the LDO. The LDO has a high power supply rejection ratio (PSRR). It can effectively suppress the switching noise. To protect the LDO from being driven into linear region, thus, deteriorating the PSRR, an adder is used. With this adder, there is a constant voltage difference which is at least the minimum dropout voltage setting by Vbias between the output and power supply of the LDO. This voltage keep the LDO always in the saturate region with high PSRR.

In the low power supply part, it consists of the LDO2 connected as a buffer amplifier. The two LDOs in this design are controlled by control signals generated from comparators. They are switched on or off dependent on the amplitude of the envelope. For small envelope signal with low output current, the low power supply is on and high power

supply is off. For large envelope signal with high output current, the low power supply is off and high power supply is on. Thus, the proposed supply Class-G modulation can obtain a very high average efficiency.

4.2.3 The Efficiency Analysis

Conventionally, for constant envelope communications, the efficiency of the PA at the saturate output power is very important. However, in modern communication systems, the average efficiency of the supply modulation is quite important because the modern communication systems with the multicarrier modulation standards such as orthogonal frequency-division multiplexing (OFDM), where the PA rarely operates at peak output power. Thus, the PAs with a high average efficiency is much more important than that with a high efficiency at saturate output power.

For an envelope signal with an output peak probability density function (PDF) of p_v, the average efficiency of the PA can be written as:

$$\eta_{avg} = \frac{P_{out,avg}}{P_{DC,avg}} = \frac{\int P_{out} p_v d(V)}{\int P_{DC} p_v d(V)} = \int \eta_{DE} p_v d(V) \tag{4.1}$$

where $P_{out,avg}$ and P_{out} are the average output power and output power of PAs, $P_{DC,avg}$ and P_{DC} are the average DC power consumption and DC power consumption, and η_{DE} is the drain efficiency of PAs. For the proposed supply modulation, the efficiency in high power supply is decided by the hybrid amplifier efficiency and that in low power supply is decided by the LDO efficiency.

In high power supply, the loss is from the Class-AB amplifier and switching PA. If the envelope signal is a DC signal, the Class-AB amplifier only provides some ripple current i_{sw}. The loss of the Class-AB can be expressed as:

$$P_{AB} = \frac{1}{2} i_{sw} V_{dd} \tag{4.2}$$

Output stage of the Class-D PA usually consists of a common-source PMOS and NMOS. The loss in the Class-D PA is mainly from the conduction loss, switching loss and

commutation loss. The conduction loss is from the on-resistance when the PMOS or NMOS is turned on. This loss can be expressed as:

$$P_{con} \approx I^2 R_{eq} = D I_{sw}^2 R_{PMOS} + (1-D) I_{sw}^2 R_{NMOS} \tag{4.3}$$

where D is the duty cycle, I_{sw} is the current provided by Class-D PA and R_{PMOS}, R_{NMOS} are the on-resistance of the PMOS and NMOS transistor, respectively.

The switching loss is introduced from driver for switching the C_{gs} of the PMOS and NMOS transistor, it can be expressed as:

$$P_{switch} = C_{eq} f V_{dd}^2 \tag{4.4}$$

where the C_{eq} is the total C_{gs} capacitance of the PMOS and NMOS transistor.

The last loss is the commutation loss from the PMOS and NMOS nonzero turn-on and turn-off time. This part of loss can be expressed as [104]:

$$P_{com} = I_{on} \cdot V_{off} (t_{on} + t_{off}) \cdot f_{sw,avg} / \alpha \tag{4.5}$$

where t_{on} and t_{off} are the switch turn-on and turn-off time, $f_{sw,avg}$ is the average switching frequency and α is the commutation parameter. In this design, the predictive deadtime driver circuit as shown in [115] is used to eliminate the commutation loss. Thus, according to Equation 4.2, 4.3 and 4.4, the efficiency of the hybrid amplifier can be expressed as:

$$\eta_{hybrid,amp} \approx \frac{I_{sw}^2 \cdot R_{load}}{I_{sw}^2 \cdot R_{load} + P_{AB} + P_{con} + P_{switch}} \tag{4.6}$$

The LDO is used for suppressing the switching ripple noise for the high power supply. An minimum dropout voltage is necessary to maintain the high PSRR. Thus, the efficiency of the LDO is defined as:

$$\eta_{LDO} \approx \frac{Vout}{Vout + Vbias} \tag{4.7}$$

where Vout is the output voltage and it equals the envelope voltage when the LDO is connected as a follower amplifier. From Equation 4.7, designing the LDO with a low dropout

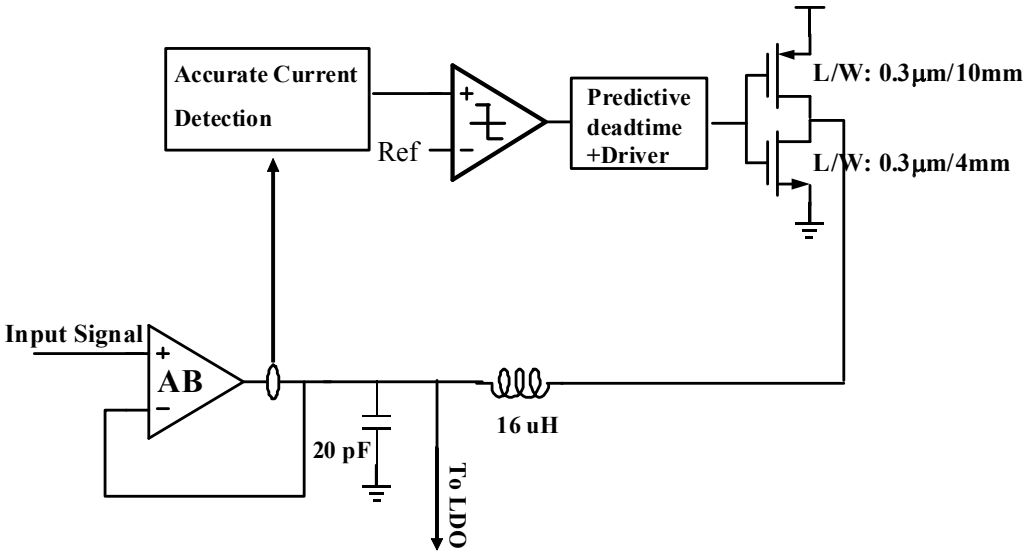


Figure 4.5: The circuit implementation of the RWDM.

voltage is very necessary to increase the efficiency. According to Equation 4.6 and 4.7, the efficiency of the supply modulation for high power supply is:

$$\eta_{high,supply} \approx \eta_{LDO} \cdot \frac{I_{sw}^2 \cdot R_{load}}{I_{sw}^2 \cdot R_{load} + P_{AB} + P_{con} + P_{switch}} \tag{4.8}$$

For low power supply, the efficiency is decided by LDO and it is simply defined as:

$$\eta_{low,supply} \approx \frac{Vout}{Vdd} \tag{4.9}$$

4.3 Circuit Implementation

4.3.1 Two-Stage Class-AB Amplifier

The implementation of the hybrid amplifier is shown in Figure 4.5. The linear Class-AB amplifier is a two stage with a common-source output stage and Miller compensation as shown in Figure 4.6. The input stage is rail-to-rail input in order to enable arbitrary feedback configurations, including unite gain follower. The GBW of the amplifier

should be large and provide a low output impendence to suppress the switching noise. Thus, it is very challenge to design the Class-AB amplifier because of high GBW. The GBW can be expressed as:

$$GBW = \frac{g_{m1}}{C_m} \tag{4.10}$$

where the C_m is the total Miller compensation capacitance and gm_1 is the transconductance of the first stage. Thus, increasing the transconductance and decreasing the Miller capacitance are quite necessary to increase the GBW.

The output stage M1 and M2 are optimized for efficiency. They have a size of 0.3 μm/3 mm and 0.3 μm/1 mm, respectively. The capacitance C1 and C2 are used for frequency compensation. This compensation technique shifts the output pole to a frequency of

$$w_{out} = \frac{C_m}{C_{gs}} \frac{g_m}{C_L} \tag{4.11}$$

where C_{gs} is the total gate to source capacitance of the output transistor and g_m is the tranconductance of the output transistor. The quiescence bias of the output stage is 3.5 mA to get a large tranconductance and pull the output pole far from the 2*GBW. C_L is 20 pF to ensure stability. The output pole is set at above 400 MHz and the GBW of the Class-AB amplifier is 150 MHz. The phase margin is 60 degree at 150 MHz.

4.3.2 RWDM Switch-Mode Regulator

The implementation of RWDM is shown in Figure 4.5. The RWDM technique generating the output signal in a class-D amplifier makes use of a delta modulation scheme for providing a sinusoidal output voltage with a low harmonic content. A modulated rectangular wave is produced whose average value tracks that of the input signal as well. The input control signal of the RWDM is from the current detection of the Class-AB amplifier.

The accurate current detection circuit includes a accurate current sensing circuit, a current to voltage converter and a voltage adder as shown in Figure 4.7. It will be introduced

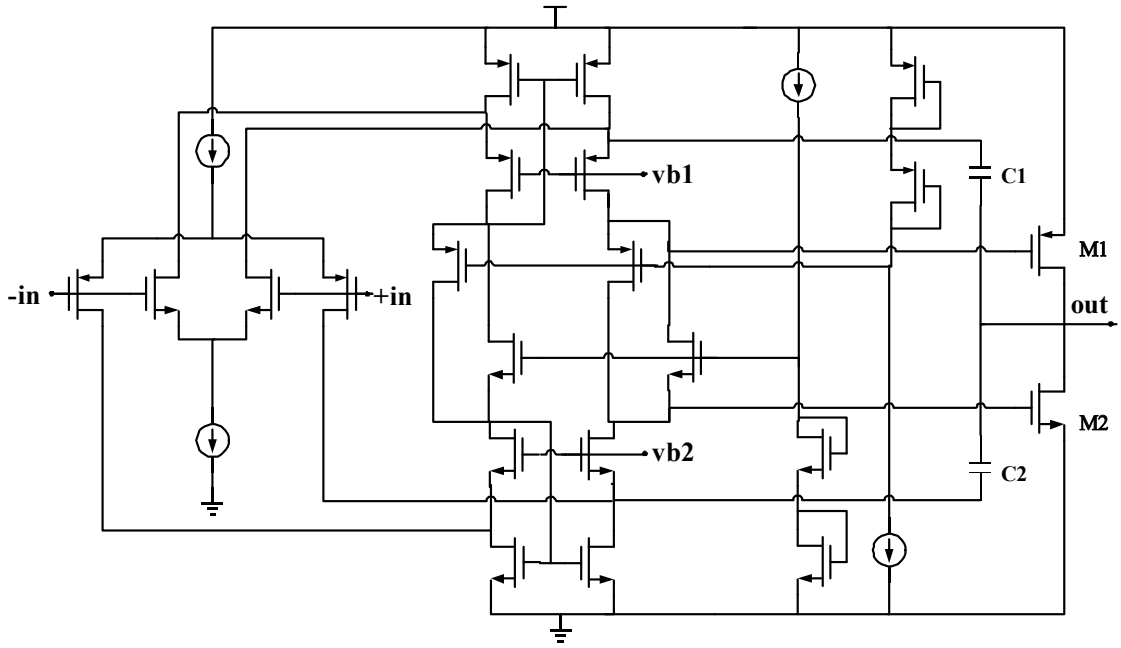


Figure 4.6: Two-stage Class-AB amplifier.

in the following section for details. The output signal from this part is compared with a hysteresis comparators. The hysteresis voltage of the comparators is about 8 mV considering the switching frequency and the bandwidth of the RWDM.

The hysteresis comparator output controls the Class-D PA. The predictive dead-time and driven circuit as shown in [115] is used to generate a delay to guarantee the conduction of power NMOS and PMOS will not be overlapping. The delay of 10 ns is selected for the dead time control in this design. The switching power NMOS and PMOS are optimized for efficiency with a size of 4 mm and 10 mm, respectively.

The low-passing output filter of the RWDM has an inductor of 16 uH and a capacitor of 20 pF, respectively, for optimizing ripple noise and bandwidth. The low-passing filter has an effective bandwidth of 140 kHz.

The worst ripple noise of the hybrid amplifier is about 8 mV and the worst SFDR is about -55 dBc. The GBW of the hybrid amplifier is 150 MHz.

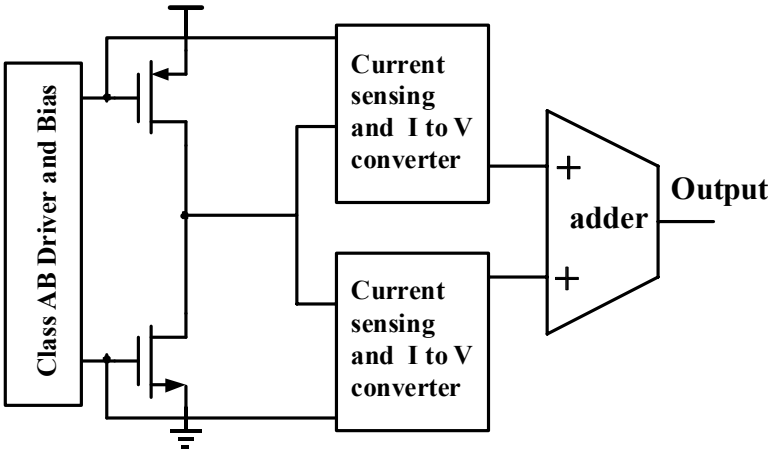


Figure 4.7: Accurate PMOS and NMOS Current detection circuit.

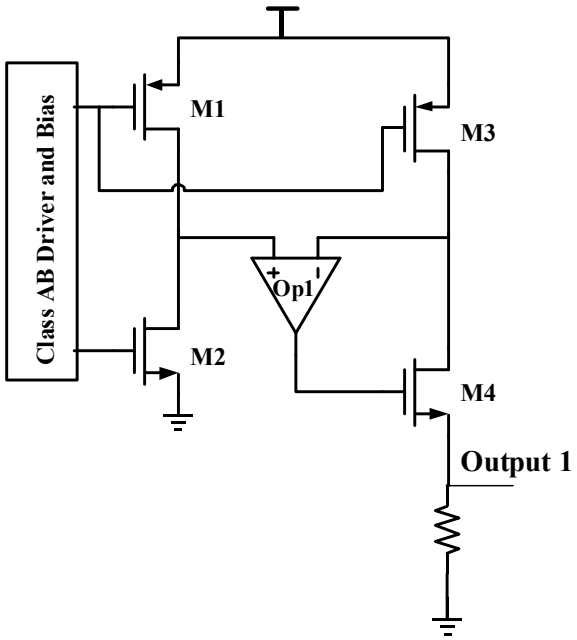


Figure 4.8: PMOS transistor current sensing circuit.

4.3.3 Accurate Current Detection Circuit

Typical current sensing techniques utilize a small series resistor and measure the voltage drop across it [107]. Though the output voltage varies with the current in the last stage, the difference drain voltage between the MOS transistor in the output stage of Class-AB amplifier and MOS copy transistor introduces some inaccuracy because of the channel-length modulation. In order to track the current accurately, in this paper, an accurate current detection circuit is proposed as shown in Figure 4.7.

The currents of the NMOS and PMOS transistors are accurately copied and converted to voltage by a small resistor, respectively. The addition of the two voltage is the total output voltage of the accurate current detection circuits.

The detail PMOS transistor current sensing circuit is shown in Figure 4.8. The current is accurately copied by transistor M3 and M4 with an operational amplifier. The gate of the M3 is connected with M1 and the drain voltage of the M3 follows with the drain voltage of M1 by the operational amplifier Op1. The gate of the M1 and M3 is 0.3 μm and the width are 3 mm and 18 μm, respectively. Thus, the currents in M1 and M3 are always with a constant ration of 3000/18. The current in M1 is accurately copied to M3 and it is converted to voltage by a resistor as shown in Figure 4.8.

The detail NMOS transistor current sensing circuit is shown in Figure 4.9. The principle of this circuit is the same with PMOS transistor current sensing circuit. However, there are twice accurate current copies in this circuit. The gate of the M2 and M4 is 0.3 μm and the width are 1 mm and 6 μm, respectively. M3 and M5 have the same gate length and width. The currents copy ration is the same with PMOS transistor current sensing circuit with a constant ration of 1000/6.

The detail two inputs adder circuit is shown in Figure 4.10. The adder circuit firstly convert the input2 voltage to current and added to the input1 in the output by resistor RES2. The resistors Res1 and Res2 should have the same value to guarantee the input2 voltage is not changed in the current copy.

The simulation shows the proposed accurate current detection circuit can accurately copy the current from Class-AB amplifier output stage with rail-to-rail output range

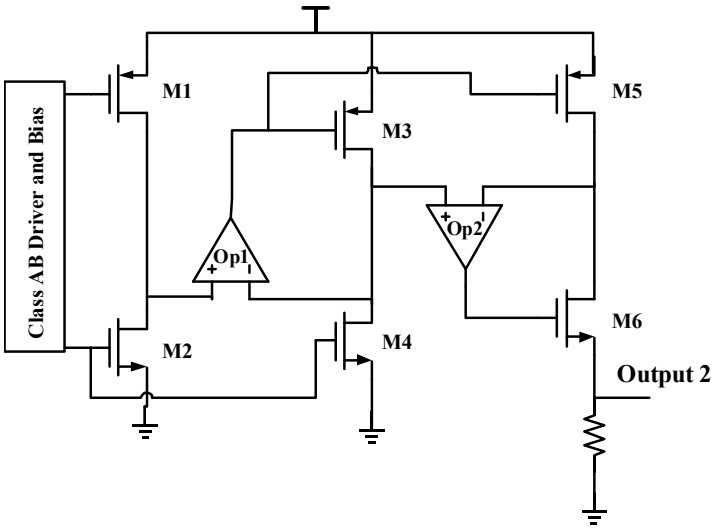


Figure 4.9: NMOS transistor current sensing circuit.

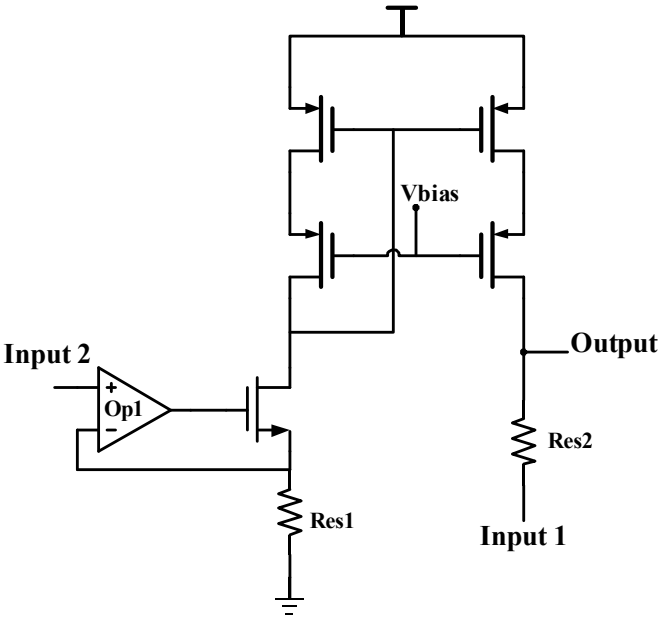


Figure 4.10: The two inputs adder circuit.

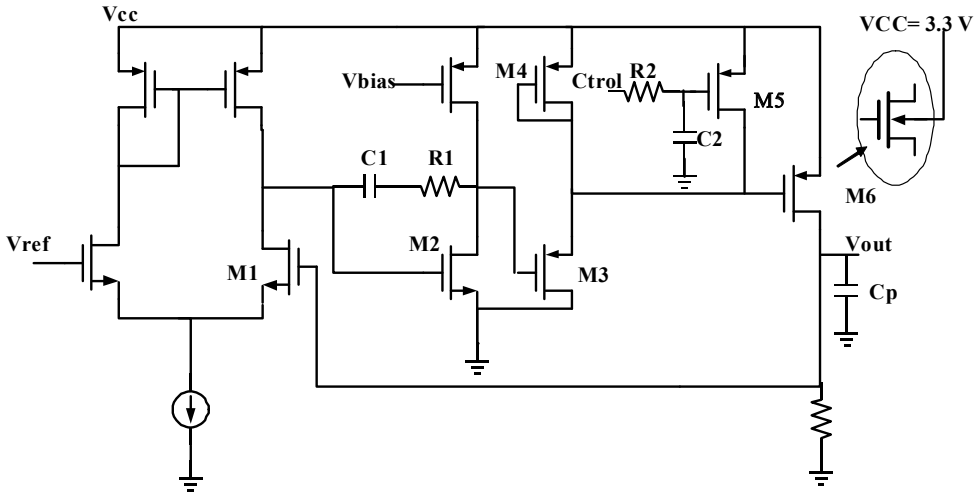


Figure 4.11: The LDO circuit implementation.

within 0.4% error.

4.3.4 LDO Circuit Implementation

The LDO is used in this proposed supply modulation and there are some requirements on the bandwidth, PSRR, phase margin and dropout voltage in this system. Firstly, because the LDO is fast switched on or off in this system, a phase margin of near 60 degree is quite necessary. At this phase margin, the transient response for a square waveform has the best compromise performance of ringing in time domain and peaking in the frequency domain. It has the fast rise time and settling time. Then, the LDO should also have a high PSRR to high frequency to suppress the switching noise ripple. And at last, a low dropout voltage is necessary for high efficiency according to Equation 4.7.

The LDO circuit used in this system is shown in Figure 4.11. This LDO consists of four stage: the first stage is a differential to single ended amplifier and the other three stage is a single ended amplifier. One stage is a common source amplifier with Miller compensation, one stage with a subtractor to increase PSRR and the last stage is output by-pass stage.

The output of the LDO due to total power supply noise at the low frequency can be shown as [116]:

$$V_{out} = [\frac{1 - A_{p1}}{A_1\beta} + \frac{1}{A_1\beta g_m r_d}]V_{dd} \tag{4.12}$$

where the A_{p1} is the power gain, A_1 is the gain of the error amplifier, β is the feedback coefficient and g_m and r_d are the transconductance and output impedance of the by-pass PMOS transistor, respectively. The first part can be eliminated by a subtractor M4 as shown in Figure 4.11 [117]. The second part of the Equation 4.12 can be minimized by a large gain of the error amplifier at high frequency. Thus, by optimizing the circuit, the total power supply noise at the output of the LDO is decreased, and the PSRR is improved.

For this LDO, the GBW is decided by:

$$GBW = \frac{gm_1}{C_1} \tag{4.13}$$

where the C_1 is the Miller compensation capacitance and gm_1 is the transconductance of the first stage. Thus, to design a wideband LDO, increasing the transconductance of the first stage and minimizing the Miller compensation capacitance are very necessary. The dominant pole is at the output of the first stage and this dominant pole P_1 can be written as:

$$P_1 = \frac{gm_2}{R_o C_1} \tag{4.14}$$

where the gm_2 is the transconductance of the second stage and R_o is the output stage of the first stage. The second pole is at the output of the second stage. This pole P_2 can be written as:

$$P_2 = \frac{gm_2}{C_1 + C_{gs3}} \tag{4.15}$$

where C_{gs3} is the source to drain capacitance of M3. This pole should be set above the 2*GBW to get a phase margin near 60 degree. The resistor R_1 is added here to compensate the zero introduced by feedforward path of the Miller capacitor C_1.

The third stage is a source follower and the output impedance is quite low. The pole in this stage has nearly no effect on the phase margin. In this design, the impedance

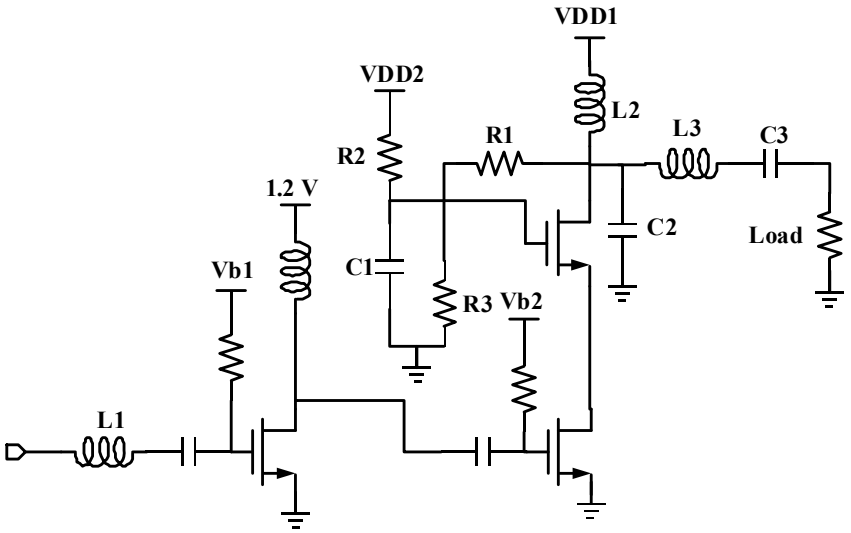


Figure 4.12: The self-biased Class-E PA.

looking from the drain of the Class-E PA is between 10 Ω to 28 Ω. The value of C_p is 10 pF. Thus, the pole at the output of the by-pass stage is also very low, and no phase compensation is needed here. In the LDO for 1.2V supply part, the N-well of the PMOS transistor should be connected to 3.3V to prevent the current flowing from drain to source when the high power supply is on as shown in Figure 4.11.

The switching signal is delayed by the resistor R2 and the capacitor C2. This delay circuit decreases the control signal rise slop. This is very important in a Class-G amplifier to suppress the switching glitch in output current. The optimized value of R2 is 5 KΩ and that of C2 is 0.2 pF.

4.3.5 Class-E PA Design

A Class-E PA with an output power of 23 dBm at 2.4 GHz for 802.11g WLAN applications is also designed to verify the effectiveness of this proposed supply modulation. This is a two stage Class-E PA with the first stage for driven. The cascode Class-E PA

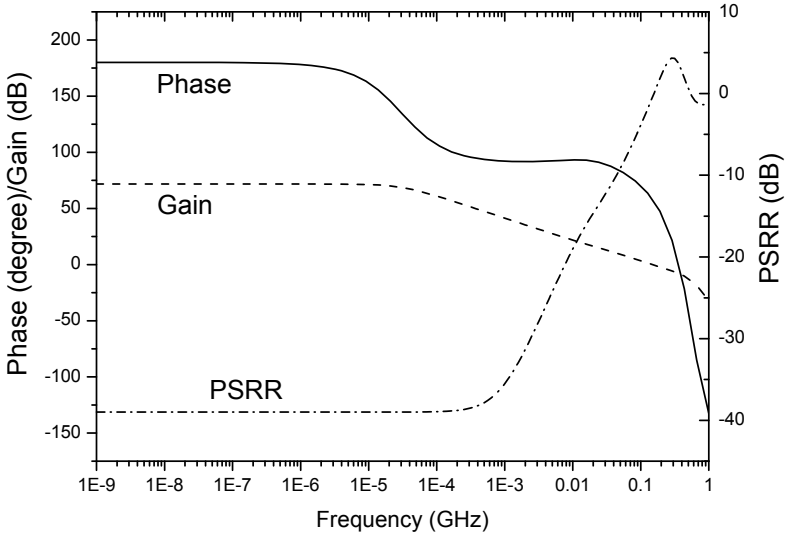


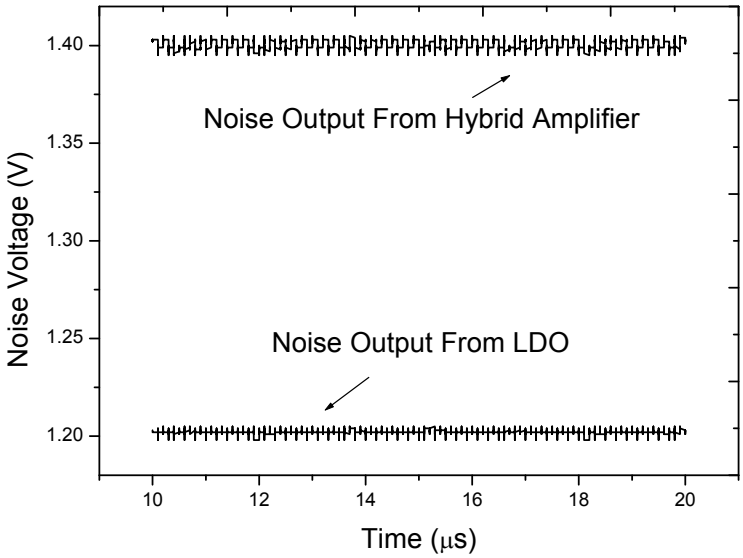
Figure 4.13: The AC characteristic of the LDO.

is used for large output power. The self-biasing technique [118] for dynamic supply is used in this PA because the drain voltage is varied with envelope signal. The self-biasing circuit consists of R_1, R_2 and R_3. The output matching network is optimized to have a the minimum overlap of the drain current and drain voltage for high efficiency. This Class-E PA can work at a low voltage of 0.1 V, and it has a saturate output power of 23 dBm with the peak efficiency of 57%.

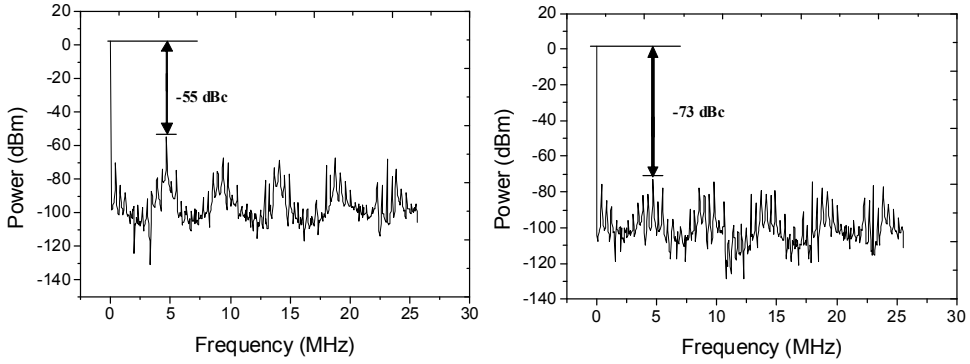
4.4 Simulation Results and Discussion

The simulation is carried out in Cadence by Spectre tools. To make the simulation and comparisons accurate, all of the components used in the simulation are on-chip devices except for the inductor used in RWDM. The inductor used in RWDM has an ESR of 0.1 Ω. The on-chip inductors used for Class-E PA have a qualify value of near 14 at 2.4 GHz.

The LDO is simulated with a minimum dropout voltage of 0.2 V. The AC characteristic of the LDO is shown in Figure 4.13. From the figure, the GBW of the LDO is



(a).



(b).

Figure 4.14: (a) The noise suppression of the LDO. (b) The output signal spectrums from the hybrid amplifier and LDO.

147 MHz. It is wide enough to process a WLAN signal with a bandwidth of 20 MHz. The phase margin at 147 MHz is 57.4 degree, which is very close to 60 degree to get a fast settle time and rise time. The PSRR of the LDO is also shown in this figure, it gets a PSRR up to 40 MHz and the PSRR is 19 dB at 10 MHz.

The switching noise from the output of hybrid amplifier and from the output of LDO is shown in Figure 4.14. The peak to peak value of the switching noise from the

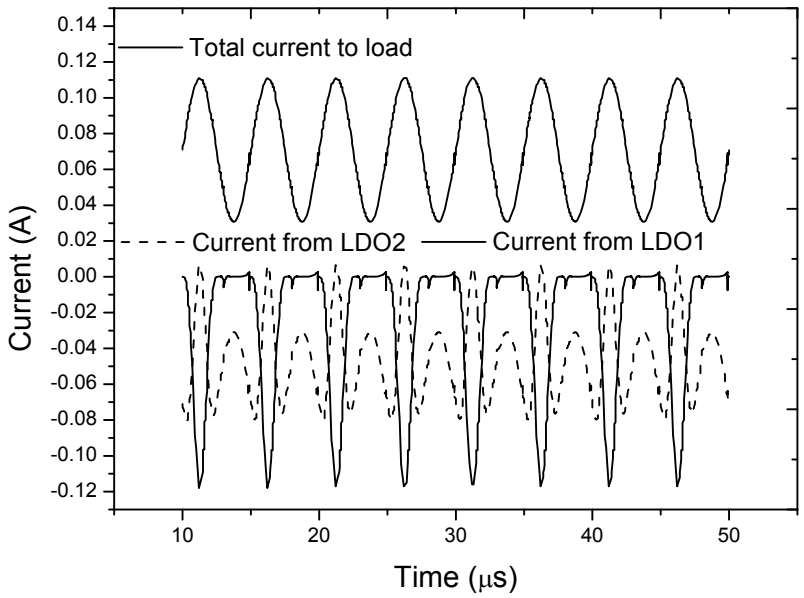


Figure 4.15: The current contributed by two LDOs.

output of LDO is smaller than that from hybrid amplifier. As shown in Figure 4.14(a), there are many low frequency components in the switching noise from output of hybrid amplifier, which is the switching noise at 5.6 MHz. However, in the output of LDO, the low frequency components is suppressed leaving high frequency components as shown in Figure 4.14(b). In the simulation, the SFDR is -55 dBc from the output of hybrid amplifier while it is -73 dBc from the LDO with noise suppression. The suppression is 18 dB at 5.6 MHz. The suppression is 5 dB smaller than that in the small signal simulation because of the difference of LDO power supply between the hybrid amplifier and the ideal supply in the simulation. The spike in Figure 4.14(a) consists of large high order switching noise. From the Figure 4.14(b), the high order switching noise is all below -75 dBc and it nearly contains no energy. Thus, the spike does not have effect on SNR of the envelop signal.

To verify the effectiveness of the proposed Class-G supply modulation, a sine envelope signal with peak-to-peak voltage from 0.7 V to 1.5 V is used as an excitation to

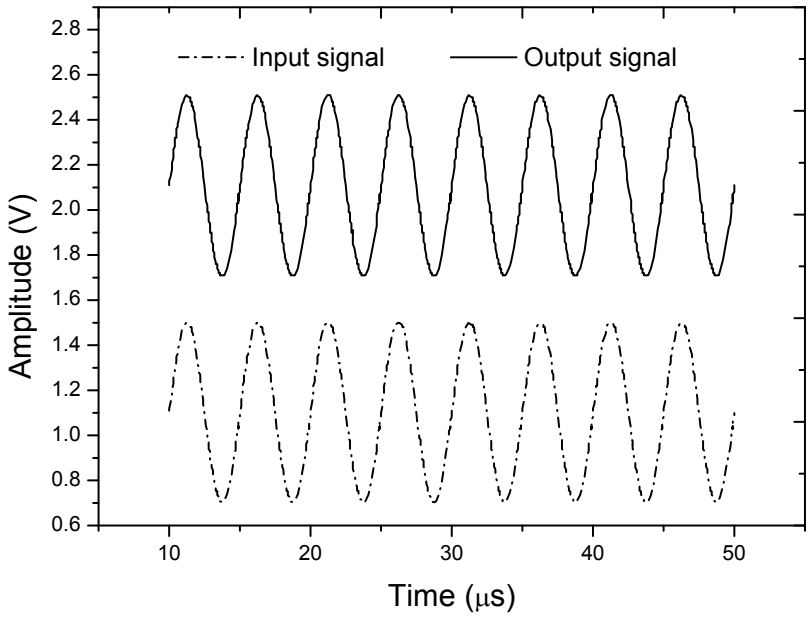


Figure 4.16: The input envelope and output waveform.

the supply modulation. The current from LDO1 and LDO2 is plotted in Figure 4.15. The output voltage and input envelope are plotted in Figure 4.16, respectively, for comparison. In the Figure 4.15, the current on the top is the total current to load and it is an addition of the current from LDO1 and LDO2. The current from LDO1 and LDO2 are plotted in the below in Figure 4.15. In the Figure 4.16, the top figure is output signal and the below is the input envelope signal. From the figure, the output signal is the same with the input envelope signal. Compared the voltage waveform with current waveform, it can be seen that, when the input envelope is low voltage part, the current is from LDO2 with low power supply. When the input envelope is high power part, the current is from LDO1 with high voltage supply. Thus, by switching the power supplies, the average efficiency of the PA largely increases. By optimizing the slop of the switching control signals and phase margin of LDO, there is no obvious glitch in the total current waveform and in the output voltage waveform when switching the supplies. The simulation indicates that the spurious is only

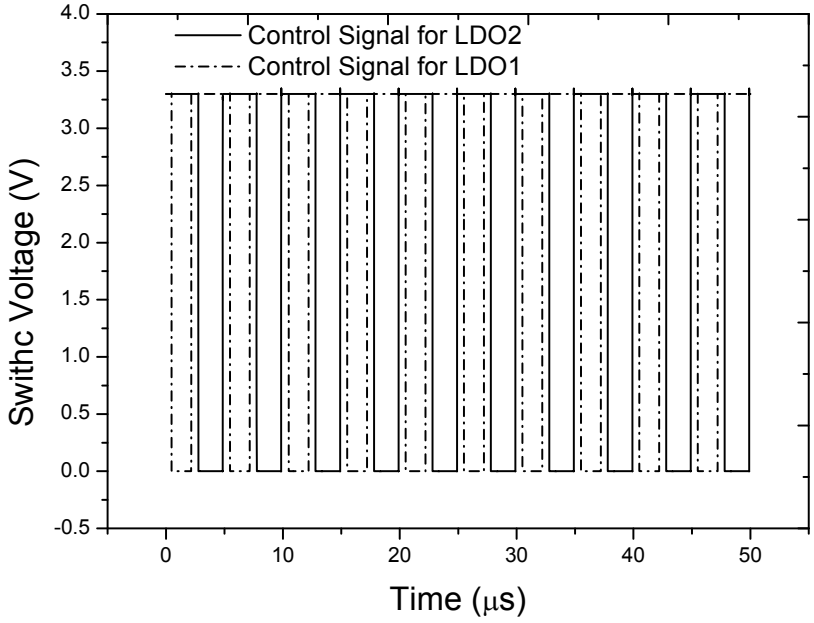


Figure 4.17: The control signal waveform.

-58 dBc with a phase margin of 45 degree and without the R2, C2 for optimizing the slop of switching control signals.

The switching control signal is shown in Figure 4.17. The high voltage enable the corresponding LDO and low voltage disable the corresponding LDO. As shown in the figure, the enable signal of one control signal is firstly on before the disable signal of the other control signal is on. The enable signal of the control signal is off later than the disable signal of the other control signal is off. This is quite important to eliminate the glitch and keep the integration of the envelope signal. The simulation indicates that the spurious is -34 dBc when the enable signals do not completely overlap with a gap time of 1% signal period.

The efficiency simulation of the proposed supply modulation is shown in Figure 4.18. Above the 1.2 V, the efficiency is the same with the hybrid amplifier and below 1.2 V, the efficiency is the same with LDO. The first peak efficiency in the figure is 85.1 % of the hybrid amplifier. To calculate the average efficiency, a PDF of a 64 QAM OFDM

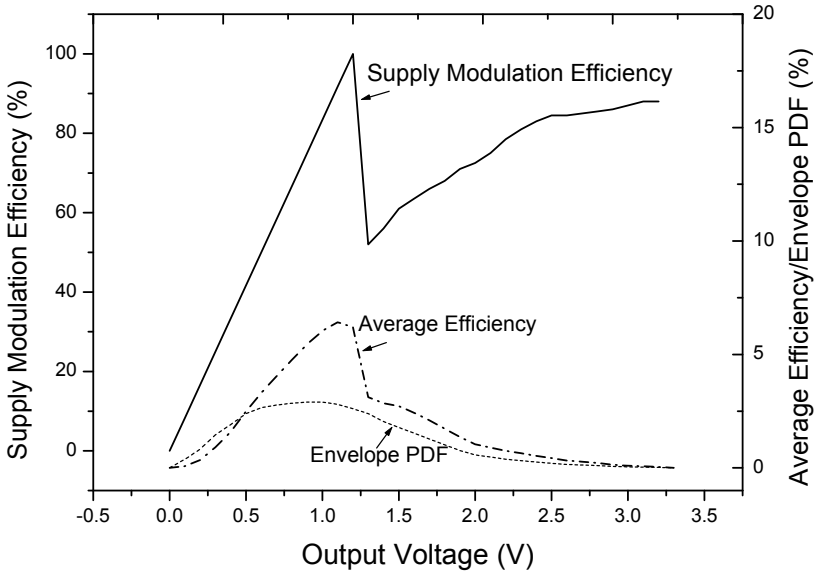


Figure 4.18: The efficiency of the proposed supply modulation.

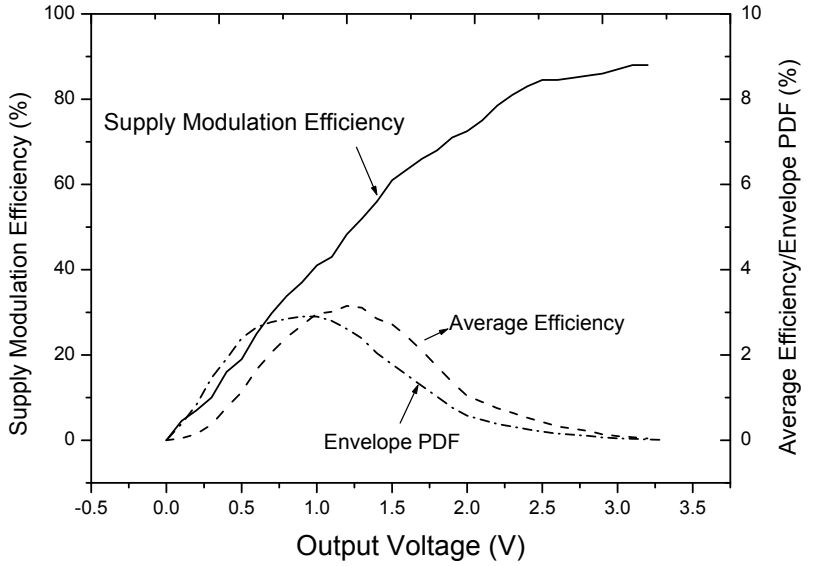


Figure 4.19: The efficiency of the conventional supply modulation.

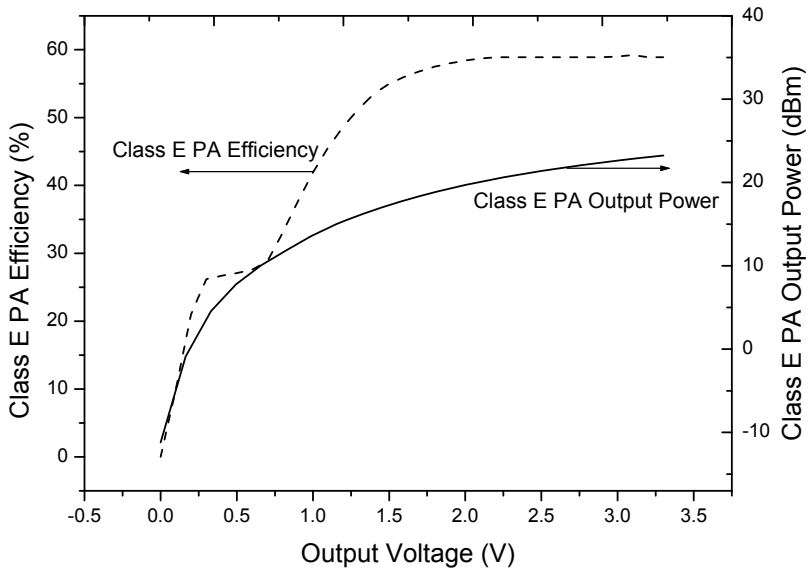


Figure 4.20: The efficiency and output power of the Class-E PA.

envelope is plotted in Figure 4.18 versus output voltage scaling. The average efficiency of the supply modulation is calculated according to this PDF. The calculated result is also plotted in Figure 4.18. Integrating the calculated efficiency, the average efficiency of the proposed supply efficiency is 62.5%.

To compared with the proposed supply modulation, the conventional supply modulation is also designed and simulated as shown in Figure 4.19. Integrating the calculated efficiency of the conventional supply modulation, the average efficiency is 45.7%. Therefore, the proposed supply modulation has a 16.6% improvement in average efficiency compared with a conventional supply modulation.

The efficiency and output power of Class-E PA are shown in Figure 4.20. The Class-E PA has a maximum efficiency of 57% with an saturate output power of 23 dBm. The average efficiency of the proposed supply modulation and the conventional supply modulation with the Class-E PA is calculated as shown in Figure 4.21. Above the 1.2 V voltage, the efficiency of the two supply modulation is nearly the same. Below the 1.2 V voltage,

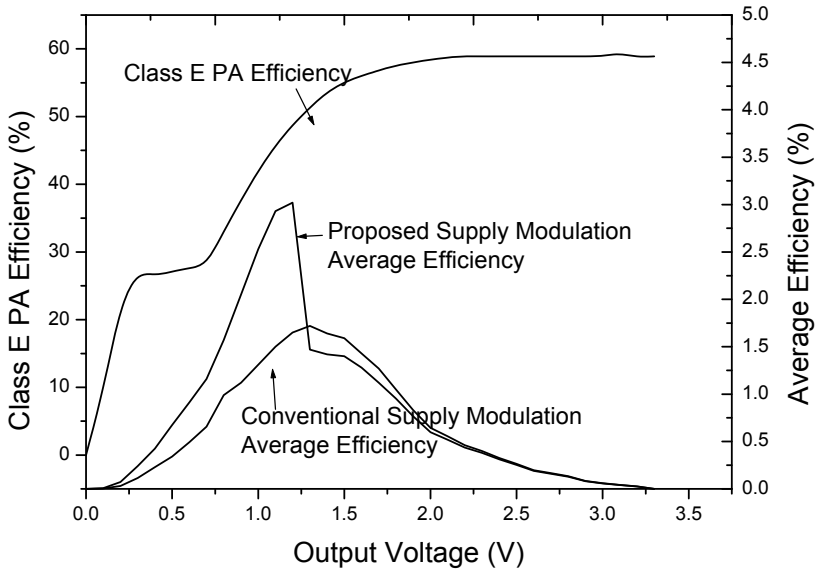


Figure 4.21: The efficiency of the Class-G supply modulation with the Class-E PA.

the proposed supply modulation has a much higher efficiency. The calculated average efficiency of the proposed supply modulation is 29.3% and 22.2% of the conventional supply modulation. A conventional Class-B PA is also designed and the calculated average efficiency is only 15.9%. This proposed supply modulation improves the average efficiency 7.1% compared with the conventional supply modulation and it improves the average efficiency 13.4% compared with a conventional Class-B PA. The comparison with other Class-G supply modulation is also carried out in Table 1. The proposed Class-G supply modulation also shows an improved performance compared with other design.

4.5 Summary

A Class-G supply modulation has been demonstrated using 0.13 μm CMOS technology for modern wireless communication systems to improve the average efficiency of PAs. In the RWDM switch-mode regulator, an accurate PMOS and NMOS current detection circuit is used for accurately detecting the current from the Class-AB amplifier. For

Table 4.1: COMPARISON OF THE PROPOSED CLASS-G SUPPLY MODULATION WITH OTHER WORK

Reference	Supply Modulation	Supply Modulation Efficiency with PA	Modulation PDF Efficiency	CMOS Process (μm)
This work	62.5%(Simulation)	29.3%(Simulation)	64 QAM OFDM	0.13
[111]	52.0%(Simulation)	24.5%(Simulation) 22.6%(Measurement)	64 QAM OFDM	0.13

suppressing the switching noise, an LDO with a bandwidth of 147 MHz and a PSRR of 19 dB at 10 MHz is designed. It can effectively suppress the switching noise at a low dropout voltage of 0.2 V in the system. The proposed Class-G supply modulation shows an average efficiency of 62.5% and a 16.6% improvement compared with the conventional supply modulations. With the Class-E PA, its average efficiency is 29.3% and a 7.1% improvement compared with the conventional supply modulations. The proposed supply modulation also shows a worst SFDR of -73 dBc. The simulation results verified that the proposed supply modulation is very effective to achieve a high average efficiency and it also shows an excellent SFDR performance.

Chapter 5

Conclusions and Future Work

This research is focus on design the wideband VCO and high efficiency PA for the growth in the high speed high performance wireless communications. Based on the reported circuit in other papers, the new techniques are proposed for the wideband VCO and high efficiency PA to overcome the disadvantages of current techniques. The conclusions and future work are shown in the following.

5.1 Conclusions

In chapter 2, the limitation of the conventional wideband VCO is analyzed. To overcome the limitation of the conventional wideband VCO, a novel ultra-wideband VCO IC has been demonstrated using 0.11 μm CMOS technology. By simultaneously controlling transformer-based switched variable inductors and switched AMOS varactors, a continuous frequency oscillation from 1.20 GHz to 3.27 GHz was realized. The frequency tuning range is as high as 92.6% with a center frequency of 2.23 GHz.

In chapter 3, a novel linearized PA has been demonstrated using 0.11 μm CMOS technology for 5.8 GHz DSRC applications. The PA has exhibited an output P1dB of 17.3 dBm with a PAE of 32% and obtained an maximum IMD improvement of 10 dB with an OIP3 as high as 27.3 dBm. The proposed novel PA exhibits excellent PAE compared

to another works with similar P1dB. The measurement results confirm that the proposed post-linearization technique has excellent improvement in linearity with high efficiency.

In chapter 4, a CMOS Class-G supply modulation for polar PAs with high average efficiency and low ripple noise is proposed. In the proposed Class-G supply modulation, the parallel supply modulations which are controlled by switch signals are utilized for low power and high power supplies to increase the average efficiency. A low dropout is utilized to suppress the delta-modulated noise and provide a low ripple noise power supply. The proposed supply modulation has high efficiency at large output current as the conventional supply modulation, and it also has high efficiency and low ripple noise at the low output current. To verify the effectiveness of the proposed supply modulation, the proposed supply modulation was designed with 0.13 μm CMOS process. The simulation results show that the proposed supply modulation achieves a maximum efficiency of 85.1%. It achieves an average efficiency of 29.3% and a 7.1% improvement compared with the conventional supply modulations with Class-E PA. The proposed supply modulation also shows an excellent SFDR of -73 dBc for output envelope signal.

5.2 Future Work

Recently, as the development of the UWB system, the maximum speed can reach 480 Mbps. The transceivers at 60 GHz and beyond are reported in [119]-[120]. The VCO operating up to 192 GHz is reported in [121] by 0.13 μm CMOS process. By increasing the carrier frequency, the data rate can reach several Gbps.

To increase the PA performance in the linear modulation for high speed and high data rate in modern wireless communications, the supply modulation gains popularity in modern wireless transceiver systems for polar transmitter and the applications of the supply modulation cover many high performance, high data rate linear modulation transmitters (i.e., EDGE, CDMA, WCDMA, 802.11g WLAN) [100]-[108]. To improve the linearity and efficiency are still an important research. By using high efficiency and high linearity

technique, it predicts a good solutions for high performance PA for high speed and high data rate in modern wireless communications.

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