Significant Performance Enhancement of Very Thin InGaZnO Thin-Film Transistors by a Self-Assembled Monolayer Treatment

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Significant Performance Improvement of Oxide Thin-Film Transistors by a Self-Assembled Monolayer Treatment

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Abstract: Despite being a standard process in fabrication of organic thin-film transistors (TFTs) to reduce interface trap density and decrease surface energy, self-assembled monolayer (SAM) treatment of gate dielectrics is rarely used in oxide-semiconductor-based TFTs due to possible damage to the SAM during semiconductor deposition. Here, by studying the dependence of plasma damage to SAM on the IGZO sputtering power, the feasibility of

improving the characteristics of InGaZnO (IGZO) TFTs using octadecyltrichlorosilane (OTS)-treated, ultra-thin Al_xO_y gate dielectrics is tested. It is discovered that under optimized conditions, device performance is significantly improved, showing a reduction of interface trap density by 50% and an increase of carrier mobility and current on/off ratio by a factor of 2.3 and 76, respectively. The effects on bias stress stability are also studied, showing significant improvement after the SAM interface treatment, including a reduced threshold voltage shift and a diminished degradation of carrier mobility. Finally, such an optimized condition is found also to work for IGZO TFTs gated with OTS-treated HfO_x, showing excellent electrical properties, including a low operating voltage of 1 V, a high mobility of 16 $cm^2 V^{-1} s^{-1}$ and a low subthreshold swing of 69 mV dec^{-1}, which is very close to the theoretical limit. As a result, this simple and yet effective interface treatment method and the resulting devices may have potential applications in future low-cost, low-power electronics.

1. Introduction

Thin-film transistors (TFTs) have been investigated for many years and have shown great potential in applications such as large-area circuits, biochemical sensors, active-matrix flat panel displays and radio-frequency identification tags.[1-3] It is generally accepted that the properties of the dielectric/transistor channel interface play a critical role in the electrical performance of TFTs.[4, 5] An entirely common method to improve the interface properties and electrical performance of organic TFTs is to apply a self-assembled monolayer (SAM), such as octadecyltrichlorosilane (OTS) and hexamethyldisilazane (HMDS), onto the gate dielectric surface, which enables tuning of the surface energy and reduction of the interface trap density.[6, 7] A very large number of reports show that the carrier mobility and current on/off ratio of SAM-treated organic TFTs can be increased by orders of magnitude. SAM treatment has therefore become a standard process in organic TFT fabrication.[7-9] Despite such an

effective treatment, to date it is still challenging for organic TFTs to obtain a carrier mobility comparable to that of oxide TFTs.

Similar to organic semiconductors, oxide semiconductors can also be deposited using solution processes. However, to obtain reasonable electrical properties, such a method requires high-temperature treatment,[10] which may damage SAMs. A more common method of depositing oxide semiconductors is sputtering. However, SAMs are typically less than 3 nm thick and their organic nature makes them less robust than inorganic films.[6, 8] As a result, sputtering has hardly been used together with SAM treatment owing to the potential damage caused by the high energy ions in the plasma.[11] Although a previous paper showed that SAMs somewhat survived the sputtering of InGaZnO (IGZO), the resulting TFTs displayed a mobility less than 2 $cm^2 V^{-1} s^{-1}$,[12] which is much lower than the typical carrier mobility (~ 10 $cm^2 V^{-1} s^{-1}$) in IGZO TFTs reported in the literature. Furthermore, the mobility in the devices without the SAM treatment was not reported, making it impossible to determine whether the carrier mobility had been improved and if so, by how much.

We have recently demonstrated that by gating with solution-processed ultra-thin gate dielectrics (Al_xO_y and HfO_x), IGZO TFTs are capable of operating under an ultra-low voltage of 1 V.[13-15] In this work, we explore the possibility of improving the performance of oxide TFTs by using a SAM treatment on the gate dielectric prior to the sputtering of oxide semiconductor. In order to study the possible plasma damage to the SAM during the sputtering, several sputtering powers have been tested. The electrical characteristics in terms of the leakage current density, capacitance density, interface trap density, and carrier mobility have been systematically studied to analyze the survival of OTS layer after the sputtering. Under the optimized sputtering conditions, we are able to show that the OTS treatment on the Al_xO_y dielectric enabled IGZO TFTs to show a significant performance enhancement, including a decrease of trap density by 50%, as well as an increase of current on/off ratio and carrier

mobility by a factor of 76 and 2.3, respectively. Such dramatically improved dielectric/channel interface properties also enabled a better stability under the bias stress. The optimized condition has also been used with OTS-treated thin HfO_x gate dielectrics and the obtained IGZO TFTs show a mobility as high as 16 $cm^2 V^{-1} s^{-1}$, which is increased by a factor of 2.1 compared with the untreated ones. The reported inexpensive and yet effective method might well be applicable to other sputtered oxide semiconductors, and it is possible that it may become a standard process in industry applications, such as manufacturing of display back plane drivers.

2. Results and Discussions

Figure 1(a) shows the schematic diagram of IGZO TFT with an OTS treatment performed on anodized Al_xO_y. The chemical structure of OTS is shown in **Figure 1(b)**. As shown in **Figure 1(c)**, the contact angles before and after the deposition of OTS SAM were found to be 53˚ and 92˚, respectively, clearly showing that the surface of the film has been changed from hydrophilic to hydrophobic.

First, the properties of the ultra-thin Al_xO_y gate insulator with and without OTS treatment were studied. Capacitance measurements were carried out using the structure shown in **Figure 1(d)**. At 100 kHz, a capacitance density of about 1000 nF cm^{-2} was found in the $Al/Al_xO_y/Al$ structure (**Figures S1(a) and (b)**). After the application of OTS, the capacitance density was reduced to about 490 nF cm^{-2} ((**Figures S1(a) and (b)**). The current density of the capacitors using bare Al_xO_y and OTS-modified Al_xO_y as the insulator is shown in **Figure 1(e)**. After the addition of the OTS layer, the current density decreased by roughly 3 times and was less than 3.5 nA cm^{-2} throughout the whole test. This confirms the formation of a monolayer and improved insulating properties.

The robustness of the films was tested by studying the breakdown voltage of the capacitors with bare and OTS-modified Al_xO_y. It has been found that the breakdown voltage was 3.4 V for bare Al_xO_y and 8.8 V for OTS-modified Al_xO_y, as shown in **Figure S1(c)**. For deep analysis of the vertical carrier transport mechanism of both types of insulators, the measured current was fitted with different modes, as shown in **Figures. S1(d) and (e)**. The electron transport of bare Al_xO_y was found to be dominated by Fowler-Nordheim (F-N) tunneling, suggesting that carriers can obtain enough energy and tunnel through the barrier. However, in the case of OTS-modified Al_xO_y, most carriers get through the films via shallow traps and hence the dominant conduction mechanism was Poole-Frenkel (P-F) emission.

During the sputtering of IGZO on top of organic materials, plasma-induced damage may occur. A higher sputtering power does not only mean more energetic ion bombardments, but also higher deposition rate and thereby quicker coverage of the SAM. In order to study the dependence of possible damage to SAM on the sputtering power, transistors gated with bare Al_xO_y (devices A, B and C) and OTS-modified Al_xO_y (devices D, E and F) have been fabricated using 25 W (devices A and D), 40 W (devices B and E) and 50 W (devices C and F) sputtered IGZO as the channel layer. **Figure 2(a) to (f)** show the transfer and output characteristics of the fabricated IGZO TFTs gated with bare Al_xO_y and OTS-modified Al_xO_y. The obtained electrical characteristics of these devices are summarized in **Table S1**.

The comparisons between devices A and D, B and E, and C and F clearly show that the gate leakage current, I_G, of the TFTs gated with OTS-modified Al_xO_y is much smaller than that of the TFTs gated with bare Al_xO_y, indicating superior insulating properties of the OTS-modified Al_xO_y dielectric. Such a decrease of I_G also results in a decrease of off-current and hence an increase of current on/off ratio by more than one order of magnitude. In addition, a significant decrease in hysteresis is clearly seen after the OTS modification, which is critical to many circuit applications. The water contact angles in **Figure 1(c)** show that the surface of the gate

dielectric has been changed from hydrophilic to hydrophobic after the OTS treatment, indicating a decreased surface energy. Hence, a possible reason for the decreased hysteresis would be the application of OTS forming a less polar surface and thus reducing influence of surface hydroxyl groups and water vapor.[16, 17] The subthreshold swing, *SS*, is found to be about 70 mV dec^{-1} in all six devices, which is very close to the theoretical limit of SS at 300 K.[18] This demonstrates a large insulator capacitance and a low interface trap density.

To confirm this, the capacitance of every device was measured by positively biasing the gate at +1 V so that the TFT was turned on and the semiconductor film did not contribute to the gate capacitance. At 100 Hz, the obtained capacitances in devices A, B, C, D, E and F are 1090, 1130, 1080, 730, 560 and 580 nF cm^{-2}, respectively. A lower capacitance density is obtained in devices gated with OTS-treated Al_xO_y, suggesting that the OTS is not completely removed by the plasma and remains effective. The trap density, D_{it}, was then calculated using the following equation:

$$D_{it} = \left[\frac{SS\,log(e)}{KT/q} - 1\right]\frac{C}{q^2}, \quad (1)$$

where k is the Boltzmann constant, T is the temperature, q is the electron charge and C is the capacitance per unit area. D_{it} is found to be 1.2×10^{12}, 1.2×10^{12}, 1.1×10^{12}, 7.7×10^{11}, 4.8×10^{11} and 8.6×10^{11} cm^{-2} eV^{-1} in devices A, B, C, D, E and F, respectively. Since all the devices have a same IGZO thickness, the trap densities induced by the bulk and top surface are similar. Hence, the change of D_{it} here is mainly related to the change of interface states. As indicated in **Figure 2(g)**, a lower D_{it} is found for devices D, E and F, suggesting a suppressed level of trap states at the dielectric/transistor channel interface owing to the OTS treatment.

As shown in **Figure 2(h)**, the threshold voltage, V_{TH}, is found to be left-shifted after the OTS modification of the dielectric layer. Since anodization is a solution-based deposition

method, as-deposited Al_xO_y layers may contain some –OH groups on the surface, which act as traps at the Al_xO_y/IGZO interface. The formation of a SAM would cap the –OH groups, and passivate the traps at dielectric/channel interface, resulting in a decreased turn-on voltage and a left shift of V_{TH}.[19] Also, because the C-H bond is not strong, it may be easily broken during the sputtering of IGZO, resulting in hydrogen incorporation into the IGZO channel and/or at the dielectric/channel interface. While the hydrogen inclusion in the channel could lead to an increased carrier concentration near the semiconductor/dielectric interface, the hydrogen incorporation at the dielectric/channel interface could also passivate the defects at the interface, both resulting in a negative shift of the threshold voltage.[20, 21]

The mobility, μ, in the saturation regime can be derived from

$$I_D = \frac{W}{2L}\mu C(V_G - V_{TH})^2, \quad (2)$$

where *W/L* is the channel width to length ratio and V_G is the gate voltage. As a result, the calculated μ for devices A, B, C, D, E and F are 4.9, 5, 8.2, 7.8, 13 and 9.6 $cm^2\ V^{-1}\ s^{-1}$, respectively. A clear increase of mobility after the OTS modification is shown in **Figure 2(i)**, and for the best devices the mobility is increased by a factor of 2.6 (comparison between devices B and E). This also confirms an improvement of the gate dielectric/semiconductor channel interface quality and a decreased number of trap states by the SAM treatment.[4, 22]

The corresponding output characteristics of the devices A, B, C, D, E and F (**Figures 2(d) to (f)**) indicate that all TFTs work in *n-type* mode with linear, pinch-off and on-state regimes clearly shown. It is found that even though the gate capacitance is decreased after the OTS treatment, an increased on-current is achieved in all sputtering cases. This suggests improved interface properties owing to the OTS modification and is in agreement with the decrease of D_{it}. The combination of the highest μ, the lowest *SS* and the lowest D_{it} is clearly seen in device E, which demonstrates that the use of 40 W for the sputtering of IGZO is the optimum deposition condition resulting in the minimum damage to the OTS layer.

Due to the difficulties in analyzing the chemical variation of the OTS surface as a function of IGZO sputtering powers after the formation of channel layers, we here measure the damage to the OTS layer by using electrical performance of IGZO TFTs. As shown in **Figure 2(g)**, unlike devices A, B and C, D_{it} of devices D, E and F changes with the IGZO sputtering power. A slightly higher D_{it} is obtained in device D than in device E, which might be due to a slightly more damaged OTS layer (much more disordered insulator/semiconductor interface) in device D. As the plasma damage occurs before the OTS layer is covered by the IGZO layer, the more severe damage to the OTS layer at a lower power may be attributed to the longer time required for IGZO to effectively cover the OTS. However, the comparison of D_{it} in devices E and F indicates that the worse interface quality was also obtained in the highest power case. This is likely due to the higher sputtering power resulting in Ar ions with higher energy, causing more damage to the OTS.

The comparison in terms of mobility of the devices also agrees well with this conclusion. While devices A, B and C show an increase of mobility with sputtering power owing to the increase of indium composition and carrier concentration,[23, 24] the highest mobility among OTS-treated Al_xO_y/IGZO TFTs is achieved in device E instead of device F. This suggests that the worse dielectric/channel interface quality is present in device F and could be due to more severe damage to the OTS layer caused by the strong plasma.

To investigate the damage to OTS layer due to sputtering further, parallel plate structures using Al/Al_xO_y/OTS/IGZO/Al (**Figure S2(a)**), Al/Al_xO_y/OTS/Al (**Figure S2(b)**) and Al/Al_xO_y/IGZO/Al (**Figure S2(c)**) have been fabricated. Regardless of the IGZO deposition power, devices with OTS-modified Al_xO_y show lower current densities than the devices without OTS modification (**Figure S2(d)**). This indicates that the OTS SAM is at least not completely destroyed during the sputtering process. At an applied voltage of 1 V, the current density in devices using 25 and 50 W sputtered IGZO is double that of the devices without

IGZO, which may be caused by a greater level of damage to OTS layers at these two sputtering powers. Similar current density is observed in the device without IGZO and the device using 40 W sputtered IGZO, indicating less damage to the OTS layer when using 40 W to sputter IGZO, in agreement with the results shown in **Figure 2**. For devices using 40 W sputtered IGZO, 8 devices that were fabricated in different batches have been randomly chosen from 40 devices to test the current density. Similar current densities are found for all devices, demonstrating good uniformity and reproducibility (**Figure S2(e)**).

The study of the uniformity and reproducibility of the IGZO TFTs was performed on ten OTS-modified Al_xO_y/IGZO TFTs that were fabricated in different batches (**Figure S3**). The devices show similar behaviors including a current on/off ratio of $(2.7 \pm 1.5) \times 10^7$, a mobility of 11.7 ± 1.3 cm^2 V^{-1} s^{-1}, a subthreshold swing of 68 ± 3 mV dec^{-1} and a threshold voltage of 0.3 ± 0.09 V.

The device performance was then compared with previously reported oxide TFTs gated with solution-processed, ultra-thin dielectric layers (**Table S2**). The comparison in terms of mobility, current on/off ratio, subthreshold swing and operating voltage clearly show that our devices are ones of the best reported to date (**Table S2**).[13,14, 25-27]

To study the role of the OTS interlayer on the device operational stability further, both types of devices (i.e. without and with OTS treatment) were positively biased at $V_G = +1$ V for 3000 s and the obtained results are shown in **Figure 3**. The devices gated with OTS-modified Al_xO_y maintain a current on/off ratio of about 10^7 and a maximum leakage current less than 0.1 nA throughout the whole test. This is much better than the devices gated with bare Al_xO_y and suggests that a stable OTS layer is formed at the dielectric/channel interface. After a bias stress of 3000 s, the threshold voltage for the device gated with bare Al_xO_y shifts by approximately 0.17 V from 0.46 to 0.63 V, which is 0.06 V more than the threshold voltage shift of the device using OTS-modified Al_xO_y. Both types of devices show a little change of

mobility after bias stress, but the mobility degradation in the device gated with OTS-modified Al_xO_y is 20 times smaller than that of the device using a bare Al_xO_y insulator. The results clearly demonstrate improved dielectric/channel interface properties owing to the effective OTS modification.

To investigate whether such a treatment also works with other gate dielectrics in improving transistor performance, IGZO TFTs gated with 2.5 V anodized HfO_x (with and without OTS treatment) were fabricated. The obtained electrical properties of both types of transistors are shown in **Figure 4**.

Owing to the improved insulating properties, TFTs gated with OTS-treated HfO_x show a decreased leakage current and hence a decreased off-current. The on-current of the device improved after the OTS treatment, even though the gate capacitance is decreased from 1300 to 700 nF cm^{-2} (measured in TFT structure at 100 Hz by biasing the gate at +1 V), suggesting an improved interface quality. To verify this, we calculate the D_{it} of both devices. With the use of the subthreshold swing values (73 mV dec^{-1} for TFTs gated with bare HfO_x and 69 mV dec^{-1} for TFTs gated with OTS-treated HfO_x), D_{it} is found to be 1.8×10^{12} and 6.7×10^{11} cm^{-2} eV^{-1} for devices gated with bare HfO_x and OTS-treated HfO_x, respectively. A clear improvement in the dielectric/channel interface quality is found here after the OTS treatment, with a reduction of D_{it} by more than 60% because of the effective OTS modification. Similar to the case of Al_xO_y, the anodized HfO_x films may contain some defects (i.e. –OH groups) at the surface. With the OTS treatment, the traps have been passivated, resulting in a decreased interface trap density, and hence an increase of on-current and a left shift of the threshold voltage. The mobility is found to be increased by a factor of 2.1 from 7.8 to 16 cm^2 V^{-1} s^{-1} after the OTS treatment. Such a carrier mobility is comparable to or better than that of low-voltage IGZO TFTs reported previously.[14, 25, 28, 29]

Both types of the devices were then tested under bias stress conditions, as shown in **Figure 5**. The untreated devices (gated with bare HfO_x) show an increase of subthreshold swing after the bias stress, which might be due to the stress-induced traps at the dielectric/channel interface. However, the OTS-treated devices show negligible change of subthreshold swing throughout the whole test, suggesting the creation of trap states at the dielectric/channel interface induced by the gate bias stress is negligible.[30] Also, the untreated devices show a large threshold voltage shift of +0.21 V after the bias stress, while only +0.06 V of threshold voltage shift is found in the case of using OTS-treated HfO_x. Furthermore, OTS-treated devices show small mobility degradation and maintain a high mobility of 15 cm^2/Vs even after being stressed for 3000 s, which nearly triples the mobility of the untreated devices (5.2 cm^2/Vs after the bias stress). The huge improvements under the bias stress are considered mainly due to the effective OTS treatment, which improve the dielectric/channel interface properties.

3. Conclusion

In this work, the effectiveness of a SAM treatment on gate dielectrics (Al_xO_y and HfO_x) has been studied in TFTs with sputtered oxide semiconductor channel layers. The results show that depending on the IGZO sputtering power the damage to the OTS SAM can be minimized and effectively controlled. Under the optimal conditions, a significant increase in electrical performance of TFTs has been achieved. This includes a more than two-fold increase of carrier mobility, an increase of current on/off ratio by approximately two orders of magnitude and a reduction of trap density by more than 50%. Such a hugely reduced trap density also dramatically improves bias stress stability. This work demonstrates a convenient and yet effective method to substantially improve the performance of IGZO TFTs which may have potential applications in oxide-semiconductor-based electronics.

4. Experimental Section

Gate/Dielectric: To fabricate Al/Al_xO_y, first a 200 nm thick Al layer was thermally evaporated onto a glass substrate as the gate electrode. Next, approximately 3 nm thick Al_xO_y was grown by anodizing the Al gate lines in 1 mM citric acid using the process conditions reported previously.[13] For Hf/HfO_x, first a 100 nm thick layer of Hf was sputtered as the gate electrode using radio frequency (RF) magnetron sputtering at 45 W in pure argon atmosphere. Then, the Hf gate lines were anodized applying 2.5 V in 1 mM citric acid. The thickness of the formed HfO_x layer was found to be approximately 11 nm.

OTS treatment: The anodized gate dielectrics were then treated by spin coating of 0.1 wt% *n*-octadecyltrichlorosilane (OTS) in trichloroethylene (TCE) in ambient conditions.

IGZO TFTs: A 25 nm thick IGZO (In:Ga:Zn = 1:1:1) channel layer was deposited on top of the formed gate/dielectric layers by RF magnetron sputtering in pure argon ambient at room temperature. Three different IGZO sputtering powers were used, which were 25, 40 and 50 W. Finally, 150 nm thick Al source/drain electrodes were thermally evaporated through a shadow mask. The channel length and width of all the devices were 60 μm and 2 mm, respectively.

Measurement: The electrical characteristics of the devices were measured using an Agilent E5270B semiconductor analyzer and an Agilent E4980A LCR meter at room temperature.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.
C-V, C-f and *J-V* characteristics, and linear fitting of leakage current (**Figure S1**), electrical properties obtained for IGZO TFTs gated with bare Al_xO_y and OTS-modified Al_xO_y (**Table S1**), current density (**Figure S2**), statistical information (**Figure S3**), and comparison of oxide-semiconductor-based TFTs gated with solution-processed, ultra-thin dielectric layer (**Table S2**).

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References

[1] J. H. Lee, D. H. Kim, D. J. Yang, S. Y. Hong, K. S. Yoon, P. S. Hong, C. O. Jeong, H. S. Park, S. Y. Kim, and S. K. Lim, in *SID Symposium Digest of Technical Papers*, **2008**.

[2] B. D. Yang, J. M. Oh, H. J. Kang, S. H. Park, C. S. Hwang, M. K. Ryu, and J. E. Pi, *Etri J.,* **2013**, 35.

[3] X. Du, Y. Li, J. R. Motley, W. F. Stickle, and G. S. Herman, *ACS Appl. Mater. Interfaces,* **2016**, 8.

[4] D. Knipp, R. Street, A. Völkel, and J. Ho, *J. Appl. Phys.,***2003**, 93.

[5] S. Steudel, S. De Vusser, S. De Jonge, D. Janssen, S. Verlaak, J. Genoe, and P. Heremans, *Appl. Phys. Lett.,* **2004**, 85.

[6] S. Kobayashi, T. Nishikawa, T. Takenobu, S. Mori, T. Shimoda, T. Mitani, H. Shimotani, N. Yoshimoto, S. Ogawa, and Y. Iwasa, *Nat. Mater.,* **2004**, 3.

[7] S. C. Lim, S. H. Kim, J. H. Lee, M. K. Kim, and T. Zyung, *Synth. Met.,* **2005**, 148.

[8] L. Majewski, R. Schroeder, M. Voigt, and M. Grell, *J. Phys. D: Appl. Phys.,* **2004**, 37.

[9] A. Salleo, M. Chabinyc, M. Yang, and R. Street, *Appl. Phys. Lett.,* **2002**, 81.

[10] S. J. Kim, S. Yoon, and H. J. Kim, *J. J. Appl. Phys.,* **2014**, 53.

[11] D.-H. Kim, D.-W. Kim, K.-S. Kim, H.-J. Kim, J.-S. Moon, M.-P. Hong, B.-S. Kim, J.-H. Shin, Y.-M. Kim, and K.-K. Song, *J. J. Appl. Phys.,* **2008**, 47.

[12] M. Park, J. Jang, S. Park, J. Kim, J. Seong, J. Hwang, and C. Eon Park, *Appl. Phys. Lett.,* **2012**, 100.

[13] W. Cai, S. Park, J. Zhang, J. Wilson, Y. Li, Q. Xin, L. Majewski, and A. Song, *IEEE Electron Device Lett.,* **2018**, 39.

[14] W. Cai, J. Wilson, J. Zhang, S. Park, L. Majewski, and A. Song, *IEEE Electron Device Lett.,* **2019**, 40.

[15] W. Cai, J. Brownless, J. Zhang, H. Li, E. Tillotson, D. G. Hopkinson, S. J. Haigh, and A. Song, *ACS Appl. Electron. Mater,* **2019**.

[16] W. Kim, A. Javey, O. Vermesh, Q. Wang, Y. Li, and H. Dai, *Nano Lett,* **2003**, 3.

[17] L. Fumagalli, D. Natali, M. Sampietro, E. Peron, F. Perissinotti, G. Tallarida, and S. Ferrari, *Org. Electron.,* **2008**, 9.

[18] L.-Y. Su, H.-Y. Lin, H.-K. Lin, S.-L. Wang, L.-H. Peng, and J. Huang, *IEEE Electron Device Lett.,* **2011**, 32.

[19] L.-L. Chua, J. Zaumseil, J.-F. Chang, E. C.-W. Ou, P. K.-H. Ho, H. Sirringhaus, and R. H. Friend, *nature,* **2005**, 434.

[20] K. Remashan, D.-K. Hwang, S.-J. Park, and J.-H. Jang, *IEEE Trans. Electron Devices,* **2008**, 55.

[21] T. Kim, K. Jang, C. P. T. Nguyen, J. Raja, S. Kang, S. Lee, T. T. Trinh, J. Jung, Y.-J. Lee, and J. Yi, *Adv. Mater.,* **2017**, 9.

[22] A. Valletta, L. Mariucci, G. Fortunato, and S. Brotherton, *Appl. Phys. Lett.,* **2003**, 82.

[23] J.-X. Wang, S. J. Kwon, and E. S. Cho, *Microelectron. Eng.,* **2012**, 95.

[24] J. K. Jeong, J. H. Jeong, H. W. Yang, J.-S. Park, Y.-G. Mo, and H. D. Kim, *Appl. Phys. Lett.,* **2007**, 91.

[25] E. Carlos, R. Branquinho, A. Kiazadeh, P. Barquinha, R. Martins, and E. Fortunato, *ACS Appl. Mater. Interfaces,* **2016**, 8.

[26] A. Liu, G. Liu, H. Zhu, Y. Meng, H. Song, B. Shin, E. Fortunato, R. Martins, and F. Shan, *Curr. Appl. Phys.,* **2015**, 15.

[27] X. Xu, Q. Cui, Y. Jin, and X. Guo, *Appl. Phys. Lett.,* **2012**, 101.

[28] P. Ma, J. Sun, G. Liang, Y. Li, Q. Xin, Y. Li, and A. Song, *Appl. Phys. Lett.,* **2018**, 113.

[29] Y. Shao, X. Xiao, X. He, W. Deng, and S. Zhang, *IEEE Electron Device Lett.,* **2015**, 36.

[30] A. Suresh and J. Muth, *Appl. Phys. Lett.*, **2008**, 92.

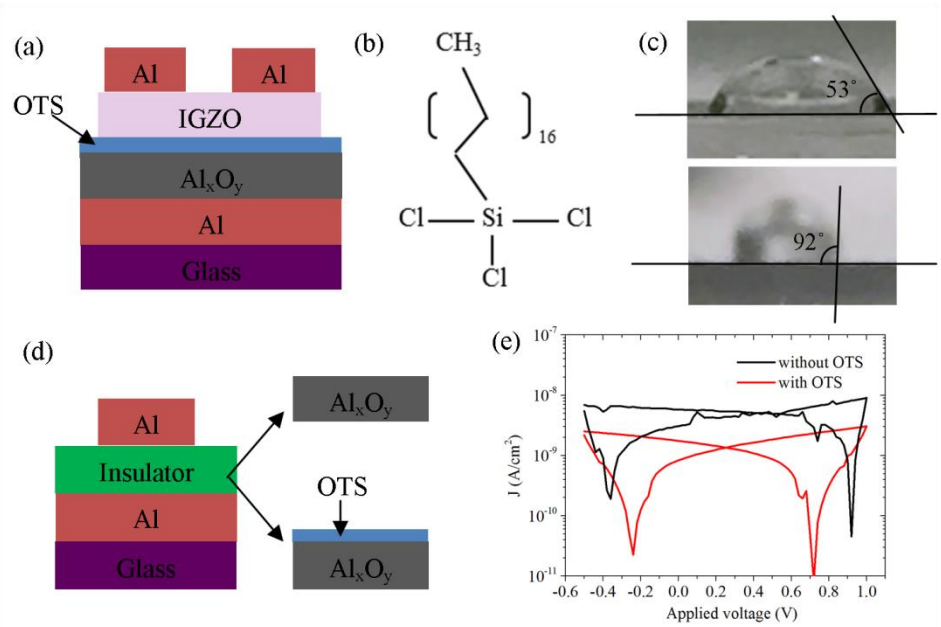


Figure 1. (a) Chemical structure of OTS (*n*-octadecyltrichlorosilane). (b) A drop of 1 µL DI water on Al_xO_y (top) and OTS-treated Al_xO_y (bottom) films showing the contact angles of water. (c) A schematic diagram of IGZO transistors. (d) A schematic diagram of capacitors with and without OTS treatment. (e) *J-V* characteristics of the studied capacitors.

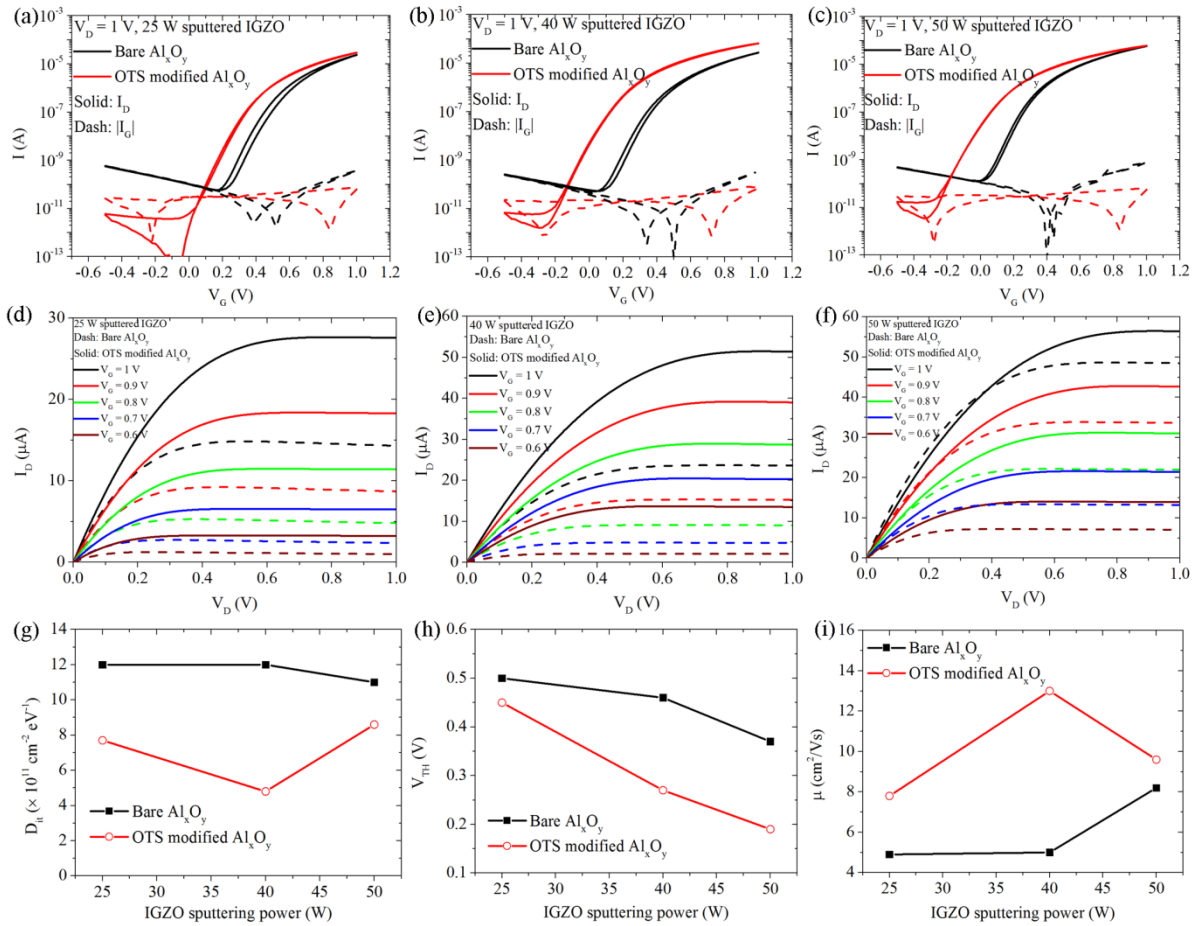


Figure 2. Transfer characteristics of the TFTs fabricated using (a) 25 W (devices A and D), (b) 40 W (devices B and E) and (c) 50 W (devices C and F) sputtered IGZO as the channel layer. Corresponding output characteristics of (d) devices A and D, (e) devices B and E, and (f) devices C and F. (g) D_{it}, (h) V_{TH} and (i) μ of the TFTs gated with bare Al_xO_y (black) and OTS-modified Al_xO_y (red) at different IGZO sputtering powers.

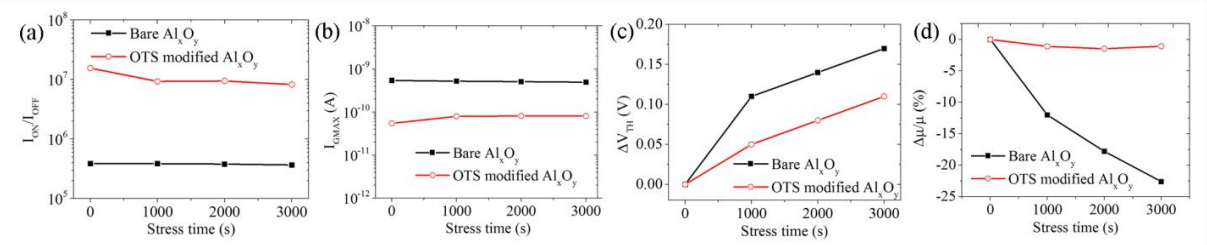


Figure 3. (a) Current on/off ratio, (b) maximum leakage current, (c) threshold voltage change and (d) mobility change of IGZO TFTs gated with OTS-modified Al_xO_y (red) and bare Al_xO_y (black) under a positive gate bias stress of V_G = +1 V for up to 3000 s. The sputtering power for the IGZO layer is 40 W.

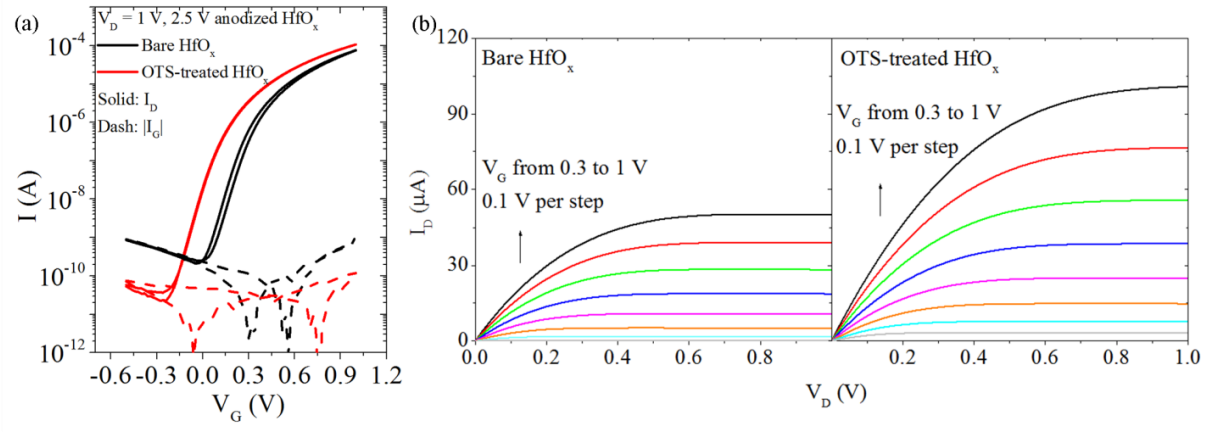


Figure 4. Electrical properties of IGZO TFTs gated with bare HfO_x and OTS-treated HfO_x. (a) Transfer characteristics. (b) Output characteristics.

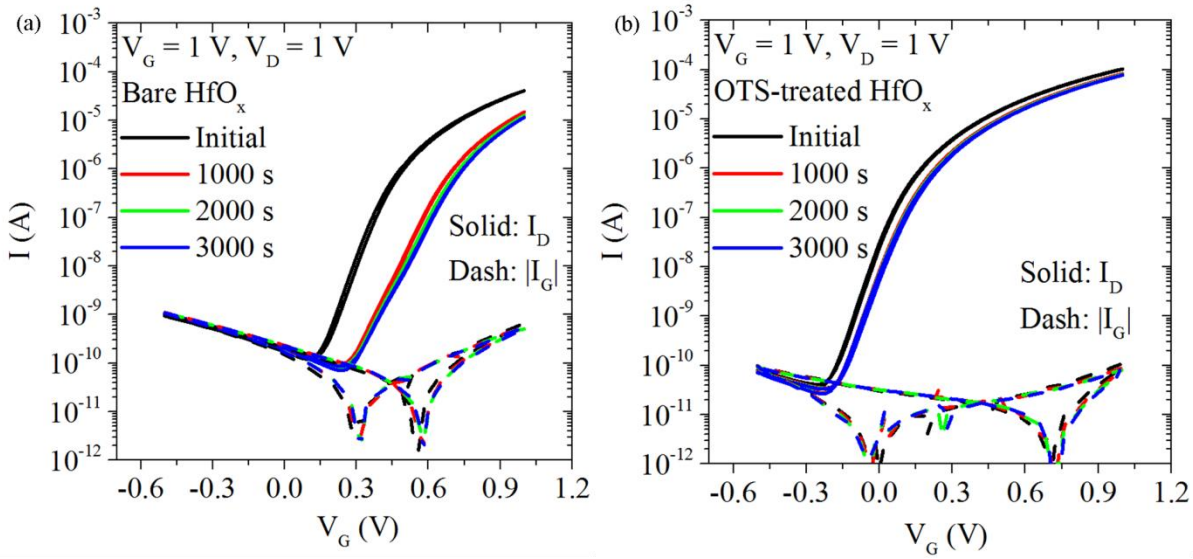


Figure 5. Transfer characteristics of IGZO TFTs gated with (a) bare HfO_x and (b) OTS-treated HfO_x under a positive gate bias stress of V_G = +1 V for up to 3000 s.

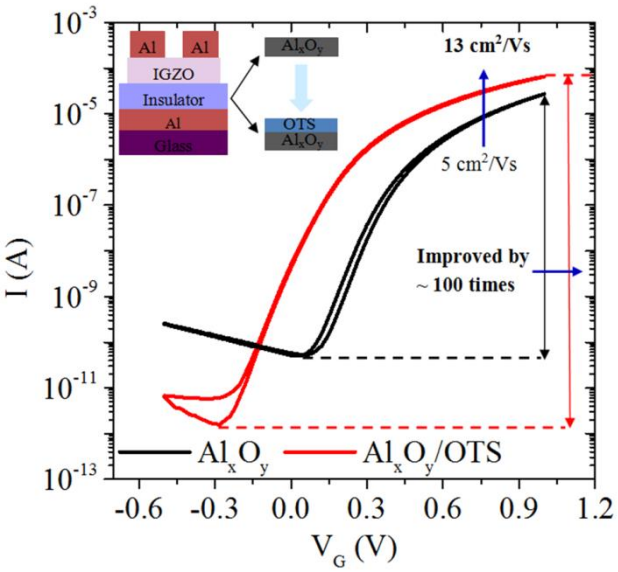
Significant performance enhancement of InGaZnO thin-film transistors is achieved by a self-assembled monolayer treatment at the dielectric/channel interface. The treated devices show a more than two-fold increase of carrier mobility, an increase of current on/off ratio by approximately two orders of magnitude and improved bias stress stability mainly due to the reduction of interface trap density by more than 50%.

Keyword: thin-film transistors

Wensi Cai, Jiawei Zhang, Joshua Wilson, Joseph Brownless, Seonghyun Park, Leszek Majewski and Aimin Song*

Title: **Significant Performance Improvement of Oxide Thin-Film Transistors by a Self-Assembled Monolayer Treatment**

TOC figure:



Supporting Information

Title: **Significant Performance Improvement of Oxide Thin-Film Transistors by a Self-Assembled Monolayer Treatment**

*Wensi Cai, Jiawei Zhang, Joshua Wilson, Joseph Brownless, Seonghyun Park, Leszek Majewski and Aimin Song**

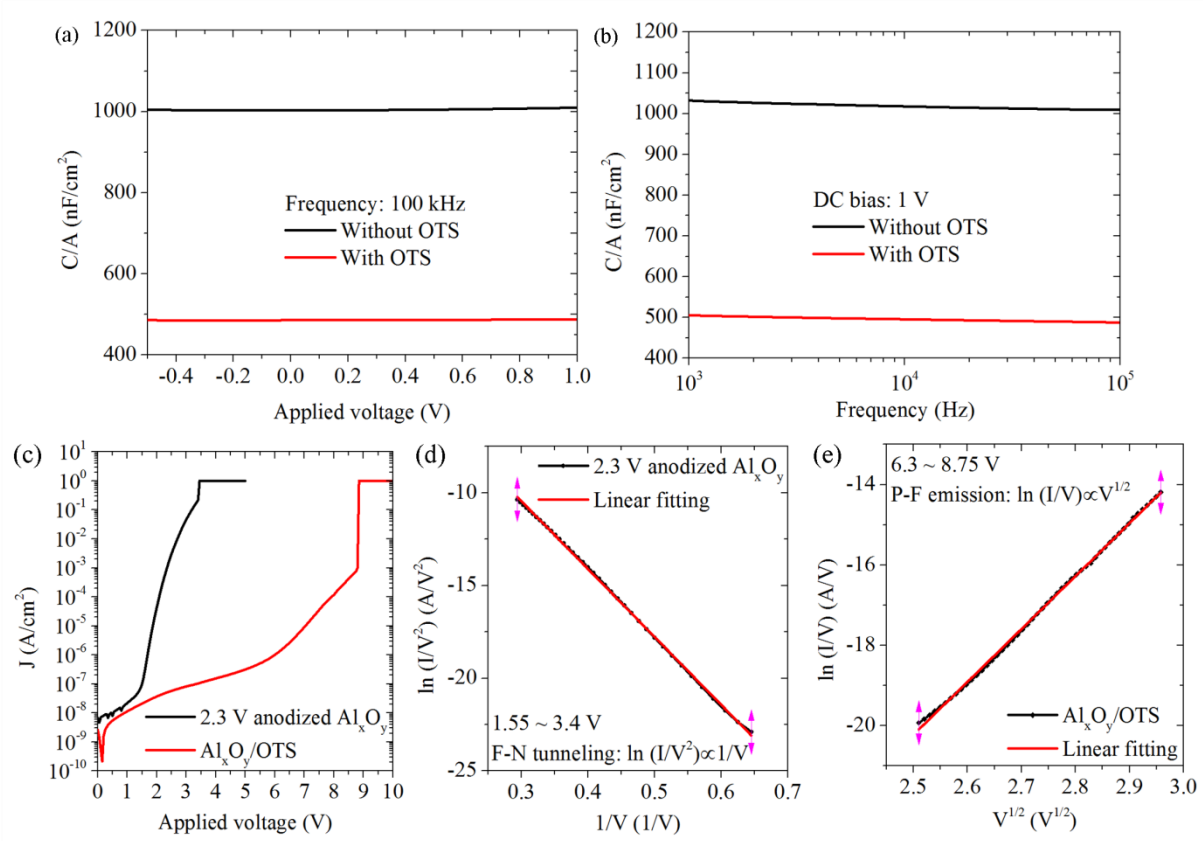


Figure S1. (a) *C-V* characteristics of devices using Al/Al_xO_y/Al (black) and Al/Al_xO_y/OTS/Al (red) structures that were measured at 100 kHz. (b) *C-f* characteristics of devices using Al/Al_xO_y/Al (black) and Al/Al_xO_y/OTS/Al (red) structures that were measured at a bias voltage of 1 V. (c) Breakdown voltage of devices using Al/Al_xO_y/Al (black) and Al/Al_xO_y/OTS/Al (red) structures. (d) The linear fitting of leakage current by F-N tunneling for devices using Al/Al_xO_y/Al structure. (e) The linear fitting of leakage current by P-F emission for devices using Al/Al_xO_y/OTS/Al structure.

Table S1. Electrical characteristics obtained for the devices shown in Figure 2.

Gate dielectric	Sputtering power (W)	Current on/off ratio	*SS* (mV dec^{-1})	*C/A* (nF cm^{-2})	D_{it} (cm^{-2} eV^{-1})	V_{TH} (V)	μ (cm^2 V^{-1} s^{-1})
OTS-modified Al_xO_y	25	2.9×10^7	69	730	7.7×10^{11}	0.45	7.8
	40	4.1×10^7	68	560	4.8×10^{11}	0.27	13
	50	1.7×10^7	74	580	8.6×10^{11}	0.19	9.6
Bare Al_xO_y	25	4.1×10^5	70	1090	1.2×10^{12}	0.5	4.9
	40	5.4×10^5	70	1130	1.2×10^{12}	0.46	5
	50	4.7×10^5	70	1080	1.1×10^{12}	0.3	8.2

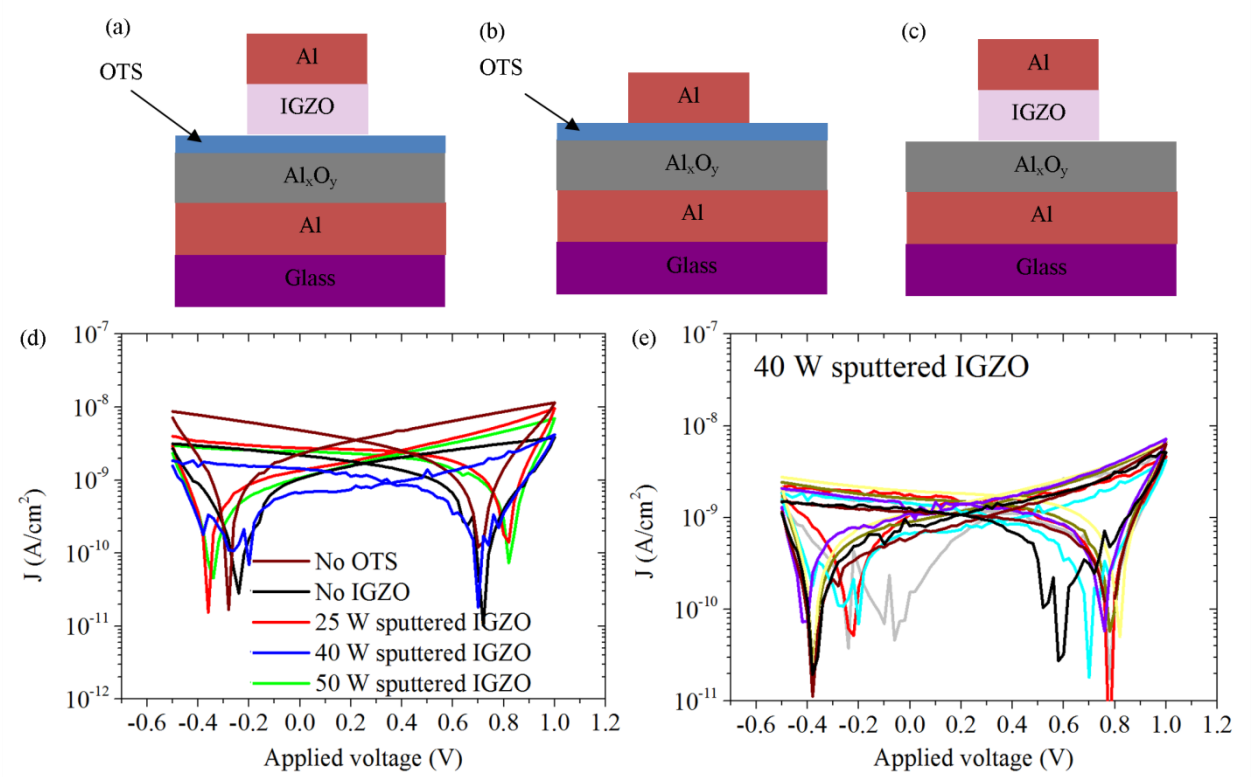


Figure S2. (a), (b) and (c) Schematic diagrams of device structures for testing the sputtering damage to the OTS layer. (d) Current density for devices using structures shown in (a), (b) and (c). (e) Current density for 8 devices using the structure shown in (a) with a 40 W sputtered IGZO layer.

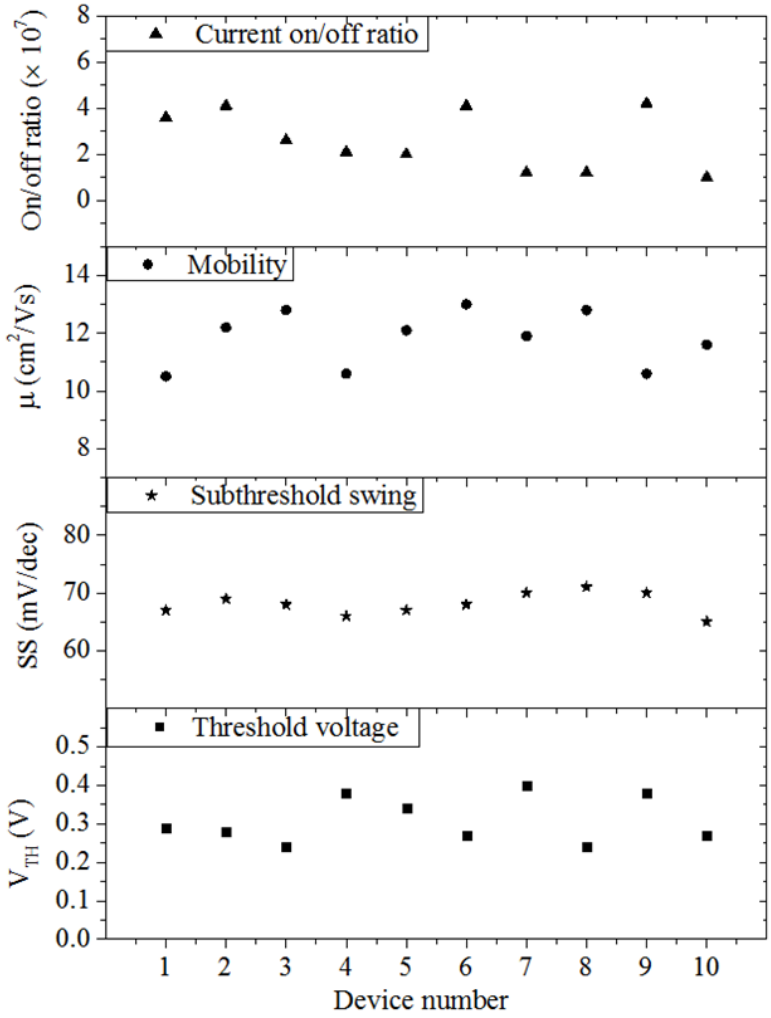


Figure S3: Statistical information. Reproducibility and uniformity test of current on/off ratio, mobility, subthreshold swing and threshold voltage of ten IGZO TFTs gated with OTS-modified Al_xO_y. The IGZO sputtering power is 40 W. The devices show similar behaviours including a current on/off ratio of $(2.7 \pm 1.5) \times 10^7$, a mobility of 11.7 ± 1.3 cm^2 V^{-1} s^{-1}, a subthreshold swing of 68 ± 3 mV dec^{-1} and a threshold voltage of 0.3 ± 0.09 V.

Table S2. Comparison of oxide-semiconductor-based TFTs gated with solution-processed, ultra-thin dielectric layers

TFT (dielectric/ channel)	Dielectric thickness (nm)	Operating voltage (V)	I_{ON}/I_{OFF}	*SS* (mV dec^{-1})	D_{it} (cm^{-2} eV^{-1})	μ (cm^2 V^{-1} s^{-1})	Ref.
(Al_xO_y|OTS) /IGZO	**~ 6**	**1**	**4.1×10^7**	**68**	**4.8×10^{11}**	**13**	**This work**
Al_xO_y/IGZO	3	1	1.6×10^6	68	8.5×10^{11}	5.4	[1]
Al_xO_y/IGZO	3	1	$> 10^5$	83	/	9	[2]
Al_xO_y/IGZO	12	2	5.9×10^4	110	/	6.3	[3]
YO_x/In_2O_3	17	1.5	6×10^6	75	7×10^{11}	15.98	[4]
ZrO_x/ZnO	5	3	10^5	250	/	0.45	[5]

References:

[1] W. Cai, S. Park, J. Zhang, J. Wilson, Y. Li, Q. Xin, L. Majewski and A. Song, *IEEE Electron Device Lett.*, **2018**, 3.

[2] W. Cai, J. Wilson, J. Zhang, S. Park, L. Majewski and A. Song, *IEEE Electron Device Lett.*, **2019**, 40.

[3] E. Carlos, R. Branquinho, A. Kiazadeh, P. Barquinha, R. Martins and E. Fortunato, *ACS Appl. Mater. Interfaces*, **2016**, 8.

[4] A. Liu, G. Liu, H. Zhu, Y. Meng, H. Song, B. Shin, E. Fortunato, R. Martins and F. Shan, *Curr. Appl. Phys.* **2015**, 15.

[5] X. Xu, Q. Cui, Y. Jin and X. Guo, *Appl. Phys. Lett.* **2012**.