Study of the Influence of the Dielectric Composition of Al/Ti/ZrO_2:Al_2O_3/TiN/Si/Al Structures on the Resistive Switching Behavior for Memory Applications

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The memory behavior of Al/Ti/ZrO_2:Al_2O_3/TiN/Si/Al devices is investigated in this work. They are adequate to be used as resistive switching memories, with two clearly different states. Besides, intermediate states are also accessible in a controllable manner. The electrical characterization in terms of admittance parameters provides relevant complementary information. The cation ratio influences the memory maps and can be changed to obtain specifically sized shape of the maps.

Introduction

Nowadays both volatile and non-volatile memories are under a high development pressure in the industrial context. Besides the dominant solid-state memory technologies, such as DRAM and flash, non-volatile random access resistive memories (RRAM) are considered adequate candidates to complement the memory landscape [1, 2]. In spite of the interest, no consensus has been reached yet about the selection of appropriate materials for fabrication [3, 4]. The aim of this work is to deepen the knowledge on the usefulness of transition metal oxides in this field, and specifically to explore the improvements on the memory behavior of metal/ZrO_2/metal structures by stabilizing metastable phases of ZrO_2 by doping or nanolaminating the dielectric films with small and controlled amounts of Al_2O_3. The effects of materials structure and composition on memory window, stability and robustness, as well as comparative small-signal response are reported in this study.

Experimental

ZrO_2:Al_2O_3 films were grown on highly-doped conductive Si <100> substrates covered by 10 nm thick TiN films by means of atomic layer deposition (ALD) at 350 ºC. The reactor was a flow-type hot-wall F120 (ASM Microchemistry Ltd.). The precursors were $AlCl_3$ (99%, Acros Organics), $ZrCl_4$ (99.9%, Aldrich), and O_3. For electrical measurements, Al/Ti/ZrO_2:Al_2O_3/TiN/Si/Al capacitor stacks were fabricated. Double-layer 110 nm-Al / 50 nm-Ti top electrodes were electron-beam evaporated. The electrode area used in the measurements was 0.204 mm^2. The bottom electrode was provided by evaporating 100-120 nm thick Al layer on HF-etched Si. A similar sample based on HfO_2:Al_2O_3 was also deposited for comparison, deposited at 350 ºC and by using $HfCl_4$ (99.9%, Strem) as precursor. All samples are listed in Table I.

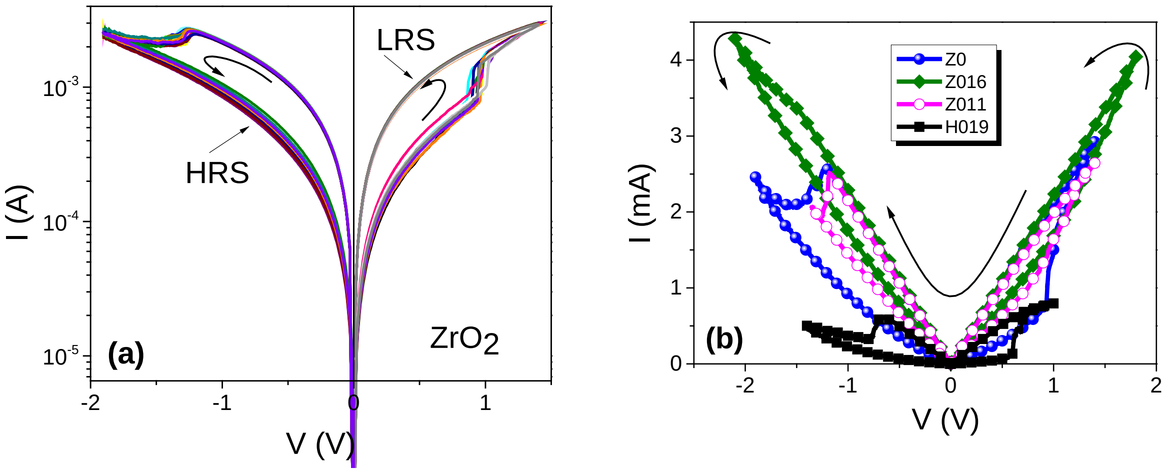

Figure 1. Current loops showing the low (LRS) and high (HRS) resistance states of the ZrO_2-based sample (a). Comparison of the resistive switching loops of the whole set of samples (b).

The electrical characterization consisted on recording the d.c. and small-signal parameters by using a Keithley 4200 semiconductor analyzer. The bias voltage was applied to the top electrode, while the bottom electrode was grounded. To record the admittance parameters, a small signal of 30 mV r.m.s. was superimposed with the d.c. bias voltage. The experimental frequency did not affect the resistive switching behavior in the range of 20 kHz - 1 MHz.

TABLE I. List of the dielectric films studied in this work. Composition is expressed in the form of cation ratios, while t denotes the oxide thickness, measured by energy dispersive X-ray (EDX) spectrometry. Deposition sequences express the amounts of successive and alternating ALD cycles for ZrO_2 and Al_2O_3. A single constituent metal oxide ALD cycle consisted of time sequence 0.5-0.5-0.5-0.5 s for metal precursor pulse – purge – water pulse – purge durations.

Sample	Deposition sequence	Composition	t, nm
Z0	700 x ZrO_2	Al:Zr = 0	45
Z016	5 x [5 x ZrO_2 + 6 x Al_2O_3] + 120 x ZrO_2	Al:Zr = 0.16	38
Z011	100 x [200 x ZrO_2 + 10 x Al_2O_3] + 200 x ZrO_2	Al:Zr = 0.11	276
H019	3 x [200 x HfO_2 + 10 x Al_2O_3] + 200 x HfO_2	Al:Hf = 0.19	48

Results and Discussion

Pristine samples showed insulating behavior, but after a forming step they behaved as memory elements, with two clearly distinct states: high-resistance state (HRS) and low-resistance state (LRS). The forming voltage is an initial electrical stress necessary to activate the switching property, and the forming step consisted of a bias ramp from 0 to ≈ 3-4 V, with a current compliance of 10 mA. In Fig. 1(a) 20 consecutive I-V cycles are depicted for the bare ZrO_2 sample, showing good repetitiveness. A set transition drives the device from the HRS to LRS. To do this, a high enough positive voltage of around 1.1 V

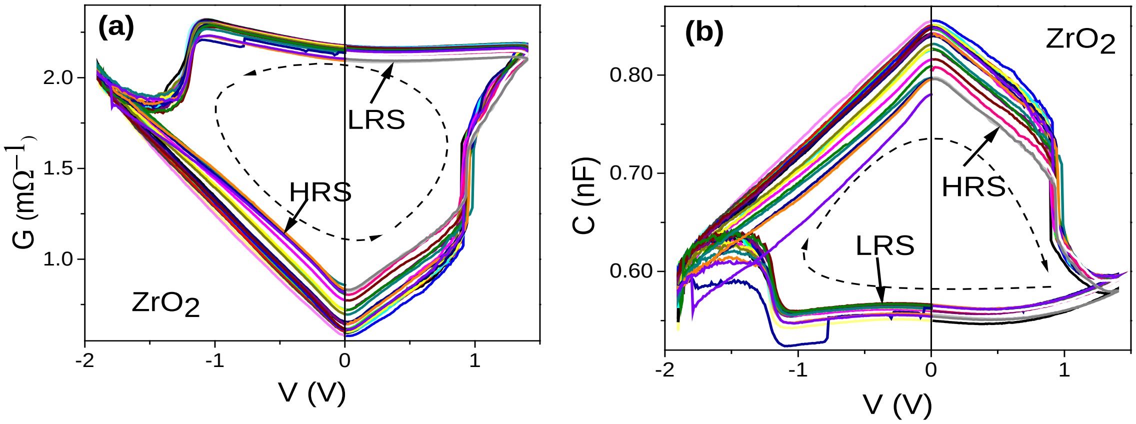

Figure 2. Admittance loops showing the low (LRS) and high (HRS) resistance states of the ZrO$_2$-based sample: in-phase (a) and in-quadrature (b) components.

must be applied. In a similar fashion, a reset transition which takes the sample from the LRS to the HRS is produced by applying a bias voltage of around -1.6 V. To establish the influence of the dielectric composition on the resistive switching performance, a comparison of the I-V loops is shown in Fig. 1(b). The incorporation of certain amounts of Al_2O_3 to ZrO_2 increases the current values, slightly extends the voltage range in which the loops appear, and at the same time provides narrower current windows, as it is seen for the Z016 sample (Al:Zr = 0.16). Thicker dielectrics lead to narrower voltage ranges and lower current levels (Z011 sample), with current window widths intermediate between those of Z0 and Z016. Finally, the resistive switching characteristics of samples based on HfO_2 instead of ZrO_2 have much lower current values with relatively wide windows and narrow voltage ranges.

After the forming, admittance (small-signal) parameters were recorded as well. Similarly to the current, both conductance, G (in-phase) and capacitance, C (in-quadrature) components exhibit set and reset loops [5], as it can be seen in Fig. 2. In LRS, G and C are practically constant (ohmic behavior), whereas in the HRS the linear voltage dependencies

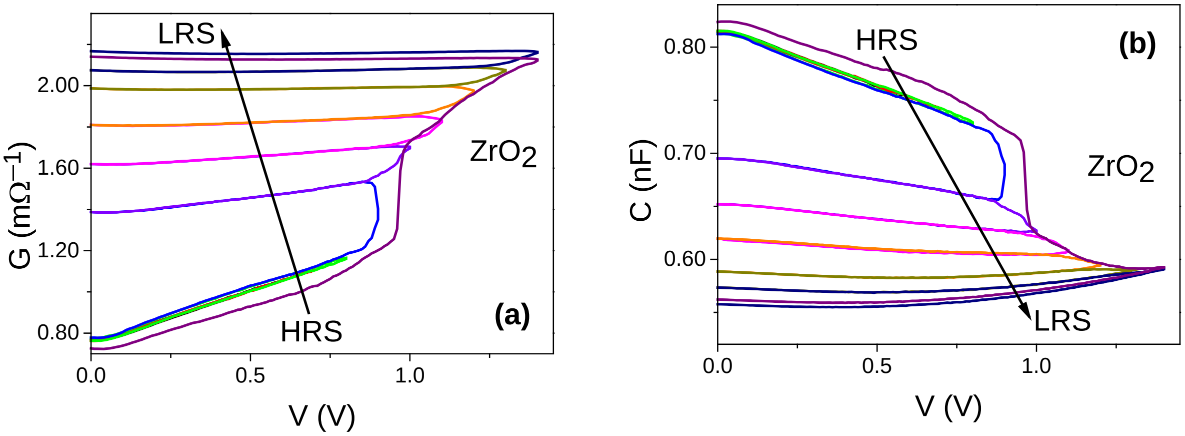

Figure 3. Internal loops of the admittance signal in terms of the in-phase (a) and in-quadrature (b) components during a progressive set process in ZrO_2 film without Al_2O_3 additives.

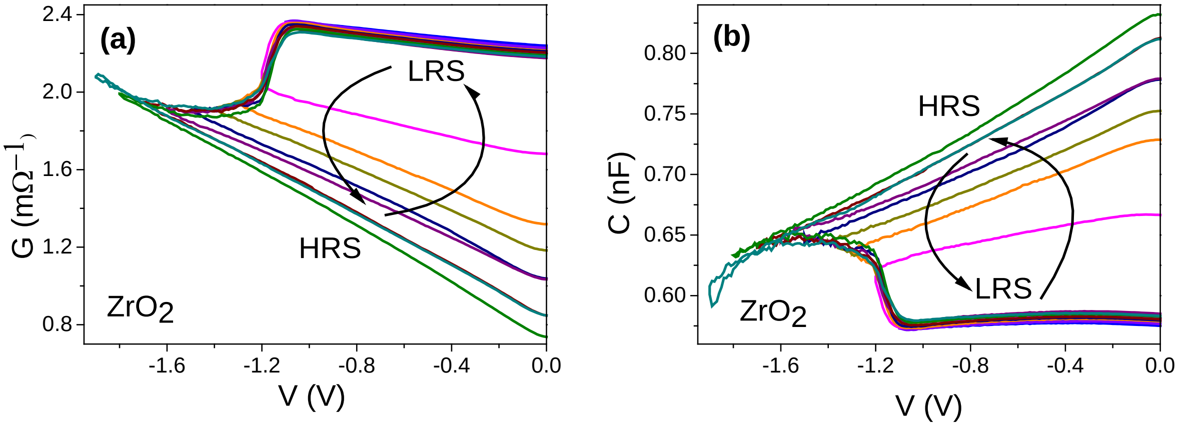

Figure 4. Admittance signal showing intermediate reset loops. Both in-phase (a) and in-quadrature (b) components are plotted.

of G and C indicate that the conduction is dominated by the space charge limited conduction (SCLC) mechanism.

Admittance parameter recording allowed us to access intermediate states between HRS and LRS in a controlled way. For example, progressive writing process (see Fig. 3 for the Z0 sample) was carried out by driving the device to the HRS and, after that, applying triangularly shaped bias voltages from 0 V to positive voltages and then returning to 0 V, with the positive voltage increasing in successive cycles. In this way, each loop started at the same conductance/capacitance value at which the previous one ended. When the applied positive voltage reached the set value (1.2 V), the memory device was switched to the LRS. Similarly, progressive erasing process could be accomplished.

On the other hand, as can be seen in Fig. 4, partial transitions between LRS and HRS were performed by means of full set loops departing from different initial reset states. To do this, different negative bias voltages were applied just before driving the device to the LRS. In this way, all conductance/capacitance loops had the same returning path. In a similar fashion, partial transitions between HRS and LRS could be obtained driving the device to the HRS from different initial set states.

It has been established earlier, that by using pulsed voltages instead of ramped bias, memory mapping can be performed [6]. Conductance memory maps clearly show the two different states, as well as the influence of the dielectric composition (Fig. 5a). These maps represent the conductance values measured at 0 V as a function of the programming voltage applied prior to recording the conductance signal. The memory map aspect ratio is modulated when the dielectric composition is changed, both in terms of height (difference of the conductance values at the HRS and LRS) and width (voltage span). In addition, some information about the set and reset processes is obtained from the left (fall) and right (rise) edge shapes. Namely, the Z016 sample shows much more gradual transitions than Z011, which in turn needs less voltage span to perform both transition. On the other hand, H019 is the most asymmetrical in terms of set and reset transitions, having the set abrupt and the reset much more gradual.

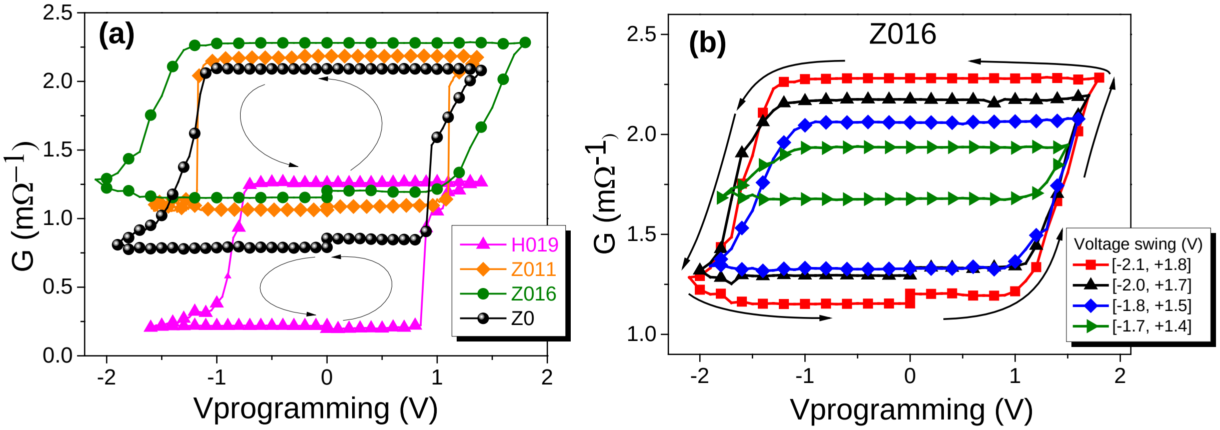

Figure 5. Comparison of the conductance memory maps of the whole set of samples (a). Conductance memory maps showing intermediate states of the ZrO_2:Al_2O_3-based sample, with Al:Zr = 0.16.

Intermediate states are also displayed in the conductance memory maps, as it is illustrated in Fig. 5(b) for the Z016 sample. To realize this, positive and negative bias voltage pulses of different height must be applied. This way, concentric loops are obtained. Therefore, by properly choosing the bias voltage pulses the sample can be driven to a particular intermediate state.

Conclusions

Repetitive resistive switching behavior in Al/Ti/ZrO_2:Al_2O_3/TiN/Si/Al devices was demonstrated. The composition of dielectrics has influence on the HRS-LRS window as well as on the range of switching voltage values. Study on small-signal parameters carried out, both in terms of conductance and capacitance in a wide frequency range, demonstrated the possibility to control intermediate states between low and high resistance. The Al:Zr ratio also played certain role in the set and reset shape transitions. By comparison, HfO_2:Al_2O_3 based sample could show similar behavior, though with lower currents and slightly narrower voltage ranges switching the material, compared to that achieved in ZrO_2 based films.

Acknowledgments

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