Radiation Induced Variable Retention Time in Dynamic Random Access Memories

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***Abstract*—The effect of gamma-ray and neutron radiations on the Variable Retention Time (VRT) phenomenon occurring in Dynamic Random Access Memory (DRAM) is studied. It is shown that both ionizing radiation and non-ionizing radiation induce VRT behaviors in DRAM cells. It demonstrates that both Si/SiO2 interface states and silicon bulk defects can be a source of VRT. It is also highlighted that radiation induced VRT in DRAMs is very similar to radiation induced Dark Current Random Telegraph Signal (DC-RTS) in image sensors. Both phenomena probably share the same origin but high magnitude electric fields seem to play an important role in VRT only. Defect structural fluctuations (without change of charge state) seem to be the root cause of the observed VRT whereas processes involving trapping and emission of charge carriers are unlikely to be a source of VRT. VRT also appears to be the most probable cause of intermittent stuck bits in irradiated DRAMs.**

***Index Terms*—Dynamic Random Access Memory, DRAM, Variable Retention Time, VRT, Variable Junction Leakage, VJL, Random Telegraph Signal, RTS, DC-RTS, Oxide Defects, Interface States, Bulk Defects, Gamma-ray, Gamma Irradiation, Total Ionizing Dose, TID, Neutron, Displacement Damage Dose, Leakage Current, Intermittent Stuck Bits, ISB, DDR3, DDR3L, Metastable Defects, Defect Structural Fluctuation.**

I. Introduction

VARIABLE Retention Time (VRT) [1], [2] is a well-studied phenomenon (see [3] and references therein) that represents a major issue for Dynamic Random Access Memory (DRAM) manufacturers and users. It is well admitted that VRT is caused, in unirradiated DRAMs, by Variable Junction Leakages (VJL) due to meta-stable generation centers located at the Si/SiO_2 interface. In particular, the V_2O_x complex defect has been proposed as a possible source of VJL [4], [5]. It has also been clearly demonstrated that Electric Field Enhancement (EFE), especially Trap Assisted Tunneling (TAT), plays an important role in DRAM VRT. However, it appears necessary to clarifying further the physical origin of the meta-stable behaviors to possibly develop effective mitigation techniques.

Radiation effects on DRAM retention time is also an active field of study. It is well-known that Total Ionizing Dose (TID) decreases the retention time of DRAM cells by enhancing their leakage current [6]–[9]. Displacement damage, likewise, is known to increase the leakage current of DRAM cells and so, to reduce their retention time [10], [11]. Several workers also reported the creation of Intermittent Stuck Bits (ISB) in proton or neutron exposed DRAMs [12]–[14]. This behavior has been attributed by these authors to a displacement damage induced variable leakage phenomenon analogous to the dark current random telegraph signal (DC-RTS) [15] studied in charge-coupled-devices (CCD). Displacement damage induced defect clusters are mentioned in these studies as the most probable cause of ISB.

However, to our knowledge, a clear link between ISB in irradiated DRAMs and the well-known VRT phenomenon observed in unirradiated DRAM has never been proposed. Moreover, the fact that TID could induce VRT or ISB in DRAMs has not been reported before and it is generally concluded that TID cannot be the cause of ISB. Finally, clear retention time evolutions with time exhibiting a clear RTS behavior in an irradiated DRAM cannot be found in literature[1].

The purpose of this work is to demonstrate that displacement damage as well as ionizing radiation lead to the generation of VRT DRAM cells and that the responsible meta-stable generation centers can exist both at the Si/SiO_2 interface and in the silicon bulk. The cause of this original TID effect on DRAMs is most likely the same phenomenon as the TID induced DC-RTS observed in CMOS image sensors (CIS) [16]. This additional similarity to DC-RTS in solid-state image sensors [15], [17] strongly suggests that VRT, VJL, ISB and DC-RTS are in fact the exact same phenomenon and that there are many more possible defects than the V_2O_x complex or bulk defect clusters to explain the existence of this exotic mechanism.

II. Variable Retention Time

In DRAM cells, the maximum duration during which the written data can be kept is called the retention time. This time is limited by the cell capacitor leakage current (Fig. 1) which is mainly given by the leakage of the PN junction to which the storage plate is connected. In a healthy DRAM cell, the leakage current is very low, the retention time is high and the stored bit is kept until the end of the refresh period as illustrated in Fig. 2. On the contrary, some weak cells can exhibit a very high leakage current (i.e. a low retention time) leading to the loss of the stored bit before the next refresh

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[1]It is worth mentioning that in [13], a few extrapolated DRAM cell leakage current traces exhibiting an RTS behavior are presented.

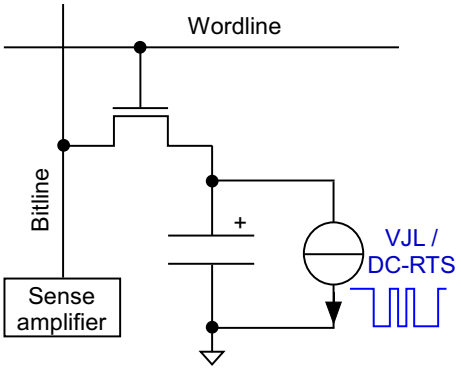

Figure 1. Schematic representation of a DRAM cell with the cause of Variable Retention Time (VRT): a leakage current source switching between several discrete current levels. Such current Random Telegraph Signal (RTS) phenomenon is called Variable Junction Leakage (VJL) in MOSFETs drain/source and Dark Current Random Telegraph Signal (DC-RTS) in solid-state image sensors.

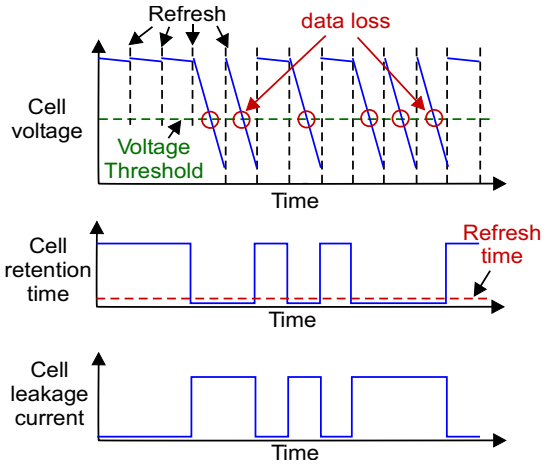

Figure 2. Illustration of the variable retention time phenomenon. The top drawing shows that a bit error (data loss) occurs when the cell voltage drops below the threshold within a refresh period. The middle diagram illustrates that data loss occurs when the cell retention time is shorter than the refresh time. The bottom one shows that a low retention time corresponds to a high leakage current and vice versa.

operation. The VRT phenomenon describes the behavior of the cells that randomly alternate between high and low retention times because of a leakage current RTS phenomenon as shown in Fig. 2. Such leakage current fluctuation is called VJL in MOSFETs source and drains and DC-RTS in image sensor photodiodes. As mentioned in the introduction, VRT is well known in the DRAM manufacturing community but there is no study in the literature dedicated to the effects of radiation on VRT in DRAMs.

VRT is a serious issue since it cannot be detected during a single classical retention time measurement and it is nearly impossible to detect without time consuming experiments. Many VRT cells are then generally seen as healthy cells until they fail during the operation of the DRAM. As mentioned in the next section, only a sub-part of a DRAM memory is studied here, but in the case of a full size modern DRAM, the number of VRT cells can be large enough to be an important source of bit errors. For these reasons, detecting

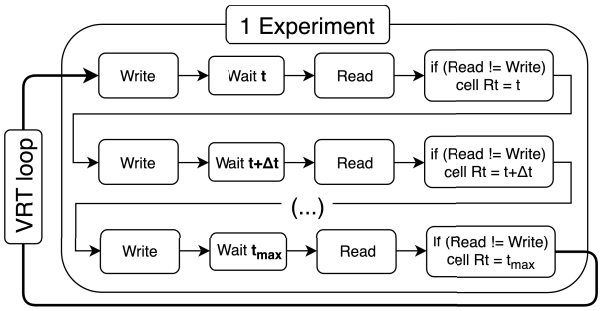

Figure 3. Test procedure to measure the VRT phenomenon. One experiment represents the steps to follow to obtain one mapping of the DRAM cells retention time at a given time. This experiment is repeated in the VRT loop every 5 minutes during 22.5 h to detect and measure VRT traces. The whole procedure presented here represents what needs to be done to perform a complete VRT measurement. Rt stands for retention time.

and understanding the origin of VRT cells is of primary importance, especially when DRAM are used in radiation environments.

III. Experimental Details

The VRT behavior of two Double Data Rate 3 Low voltage Synchronous Dynamic Random Access Memories (DDR3L SDRAMs), one 2 GB and one 4 GB, coming respectively from two different major manufacturers were studied using a Xilinx KC705 evaluation kit similarly to the approach proposed by Liu *et al.* [18]. Both DDR3L SDRAMs use a 1.35 V nominal supply voltage and the technology node of the studied 4 GB memory is 30 nm (the technology node of the 2 GB one is not known).

To first measure the retention time of each cell, one loop of the procedure presented in Fig. 3 is performed. It mainly consists in writing a given data pattern in the memory, put on hold the refresh cycle for a given amount of time and read back the memory to look for cells that have lost the stored information. The hold time is progressively stepped from 200 ms to 10 s leading to 50 steps in a VRT loop of Fig. 3.

If a cell fails during any VRT loop of the whole VRT measurement, it is counted as a weak cell for the whole VRT measurement and the lowest hold time value at which the cell loses its data gives its retention time for the current VRT loop. At the end of the VRT measurement, if in some VRT loops an identified weak cell does not fail, its retention time is artificially set to 10 s for those VRT loops. In other words, a retention time of 10 s in a figure of this manuscript means that the weak cell exhibited a real retention time of 10 s or more during this particular VRT loop. To keep the duration of retention time mapping (i.e. a VRT loop in Fig. 3) reasonable we focused on a 1 Mbit region for each studied memory module. Since 32 bit words are used to read and write the memory modules and since one elementary DRAM component has an 8 bit data bus, the 1 million studied cells are distributed evenly between 4 physical DRAM devices. It should be noted that the physical-to-logical mapping is not known for the studied devices and so that the precise location of the studied memory cells is unknown.

In these conditions, about 5 min are necessary to obtain a retention mapping (i.e. a VRT loop lasts ≈ 5 min). This VRT loop is repeated (see Fig. 3) 270 times to reach a total experiment duration of 22.5 h to detect, measure and store VRT traces.

If not stated otherwise, all the measurements presented in this article were performed at $60 \pm 0.3°\mathrm{C}$ by placing the test setup in a climate chamber with regulated temperature. This realistic operating temperature for a DRAM appears to be a good trade-off between the high temperature ($85°\mathrm{C}$) generally used in VRT studies (as mentioned in [18] and used in [9]) and the lower temperatures generally used in DRAM Single Event Effects (SEE) testing. It allows a significant activation of the leakage mechanisms to observe a large population of weak cells in the chosen time window while limiting the high temperature annealing effects expected at the maximum recommended operating temperature of $85°\mathrm{C}$.

DRAM manufacturers optimize the physical mapping of their memory to reduce as much as possible the bit errors by implementing strategies that limit leakages and bit errors due to electrical coupling from cell to cell or between the bit/word lines. Hence, a logic 1 does not necessary mean that the memory cell capacitor is set to VDD and the physical mapping of the memory cells does not corresponds to the logic mapping [18]. Because of that, the used data pattern is known to have a large influence on the number of detected weak cells (as discussed in [18]). In this work it has been chosen to use a basic static data pattern with a single write and read operation per hold time. This approach is less efficient than the ones proposed in [18] at detecting the exact total number of weak cells in the memory but it is much faster and it thus allows to obtain more retention time data points over the experiment duration (and so better defined VRT traces).

A few basic static data patterns (all 1, all 0 and checkerboard patterns) were tested on each memory and at each dose. It appeared that the most efficient data pattern was always the same on a given technology (all 1 for the 2 GB memory and all 0 for the 4 GB memory), whatever the dose or the type of particle. Hence, the same static data pattern, the most efficient one, was used for all the DRAMs from the same vendor.

Finally, several DRAMs (one per dose) from each vendor were exposed at room temperature to $^{60}\mathrm{Co}$ $\gamma-$rays (from 10 to 200 krad(SiO_2)) at TRAD, Toulouse, France, to generate Si/SiO_2 interface defects and to a neutron spectrum with a mean energy of 20.4 MeV (with fluences ranging from 10^{12} cm^{-2} to 10^{13} cm^{-2}, 1 MeV neutron equivalent fluences ranging from about 2×10^{12} cm^{-2} to 2×10^{13} cm^{-2} and displacement damage dose from about 380 $\mathrm{TeV/g}$ to 38 $\mathrm{PeV/g}$) from the NIF CRC facility of the Université Catholique de Louvain, Louvain la Neuve, Belgium, to create silicon bulk defects. At the maximum neutron fluence used in this work (i.e. 10^{13} cm^{-2}) the total TID absorbed by the exposed devices is 15 krad(SiO_2). For each device, all the measurements have been performed within a month after exposure.

For TID tests, the reverse bias voltage does not have a proven effect on the radiation induced degradation of PN junctions whereas it is well known that applying non-zero voltages on MOSFETs enhances the radiation induced I-V characteristics degradations [19]. For this reason, grounded irradiation condition was preferred in order to reduce the degradation of the sensitive electronic functions, such as the sense amplifiers, while keeping a comparable level of degradation in the memory cell storage junction. Here again this choice means that at a given TID the number of weak or VRT cells might be underestimated, but the purpose of this study is not to determine the exact number of weak/VRT cells at a given dose in a given technology but to determine whether or not radiation can induce VRT behaviors and to investigate the underlying physics. Neutron irradiations were performed grounded as well as it is usually recommended for displacement damage testing.

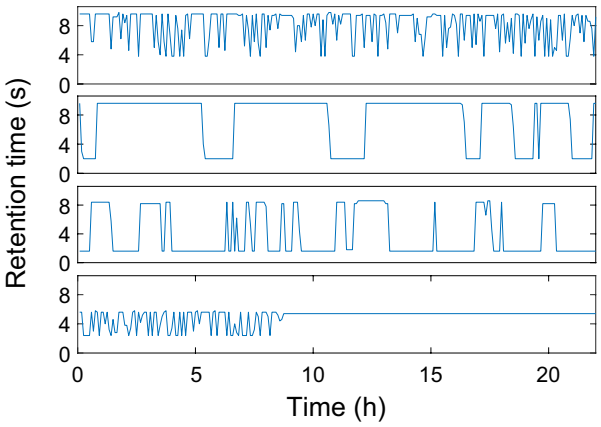

Figure 4. Selected temporal evolutions of the retention time of four DRAM cells exhibiting the VRT phenomenon before irradiation (from the 2 GB memory).

IV. Results and Discussion

A. Before Irradiation

Fig. 4 presents four temporal evolutions of selected DRAM cells that exhibit the VRT phenomenon. The typical RTS behavior that is often reported in irradiated solid-state image sensors can clearly be recognized in this figure showing that VRT already exists before irradiation in the studied DRAMs (as expected). Fig. 5 displays the distribution of the minimum and maximum retention times measured on the two DRAM technologies before irradiation during a whole VRT measurement. This representation proposed in [18] allows detecting VRT on the whole population of scanned memory cells. Indeed, non VRT cells have the same minimum and maximum retention time and are thus distributed along the diagonal. Therefore, the VRT cells can be identified as all the memory cells that depart from the diagonal. The further one memory cell is from the diagonal, the larger is its VRT amplitude (the vertical distance to the diagonal gives the VRT amplitude). This figure confirms that VRT is present in a significant number of cells before irradiation on both studied technologies.

The typical refresh period for DDR3 DRAM cells is 64 ms at $85°\mathrm{C}$ [18]. It is worth noting here that, on this small number of cells and in these operating conditions, several cells of

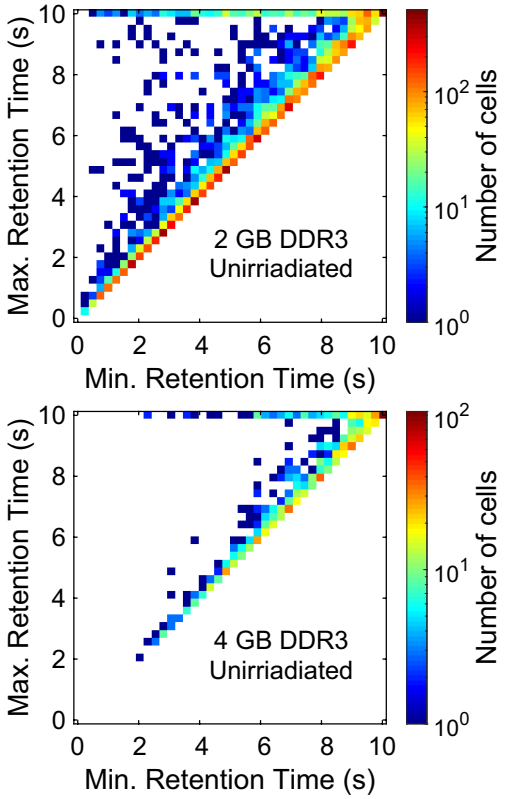

Figure 5. Minimum and maximum retention time distributions of the studied unirradiated DRAMs. Only about one million cells (1 Mbit) are scanned. All the memory cells located above the diagonal of this diagram can be considered as VRT cells since their minimum and maximum retention time are different. The 2 GB memory exhibits many more VRT cells (especially with lower retention times) than the 4 GB one.

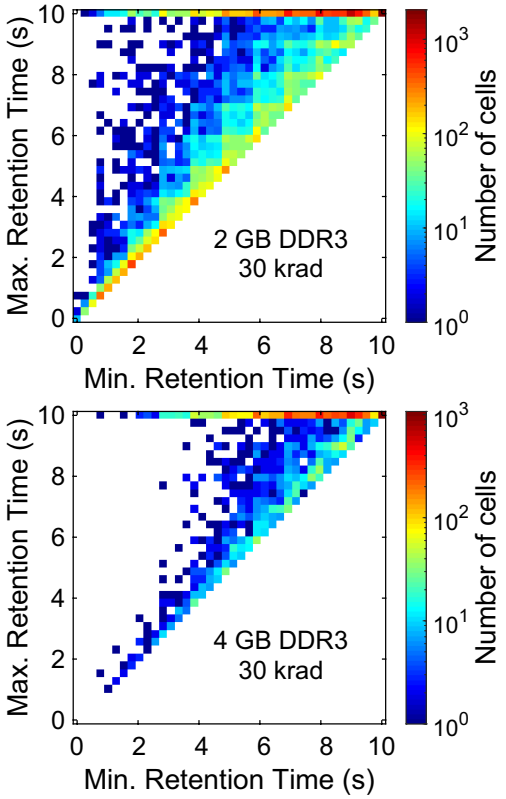

Figure 6. Minimum and maximum retention time distributions of the two types of DRAMs exposed to 30 krad(SiO_2) with the ^{60}Co source. Only about one million cells (1 Mbit) are scanned. The TID induced generation of VRT cells appears clearly when compared to Fig. 5. The 2 GB memory exhibits memory cells with very low retention times (below 200 ms) that can be seen as Intermittent Stuck Bits (ISB).

the 2 GB DRAM, including a few VRT cells, approach the range of retention times where retention failures are expected whereas the VRT cells of the 4 GB have a safe margin of more than 2 s before entering the 64 ms range. It means that VRT induced ISB would probably not be observed in those unirradiated DRAMs even if some VRT cells of the 2 GB device might cross the failure threshold if the temperature rises up to the maximum recommended operating temperature of 85°C. This is most likely the reason why no ISB was observed in unirradiated DRAM in [12] whereas probably many cells exhibited VRT as in the DRAM studied here.

The important discrepancy between the two studied DDR3L SDRAMs illustrated in Fig. 5 is most likely due to technological and design differences between the two vendors such as the cell design itself (size/shape of the storage PN junction) and the doping concentrations.

B. Gamma-ray irradiations

As mentioned previously, ^{60}Co gamma rays were used to deposit TID in the studied DRAMs. The main effect of TID in CMOS circuits is to generate oxide defects near or at the Si/SiO_2 interface and so to increase the density of interface states and oxide positive trapped charge [19].

After exposure to TID, Fig. 6, Fig. 7 and Fig. 8 demonstrate that a large number of new VRT cells are created (some of them are illustrated in Fig. 9) and that their number increases with the radiation dose. This TID effect has not been observed before in ISB studies and in TID effect studies on DRAM retention time in general. The reason why previous ISB studies have not reported any TID induced ISB is most likely due to the fact that the technology studied in previous work behaves like the 4 GB DRAM studied here: the minimum retention times of the VRT cells generated at 200 krad are still above the 64 ms limit.

On the contrary, in the 2 GB memory, many of these TID induced VRT cells reach a minimum retention time in the range of the typical refresh period (especially at 200 krad). Since they alternate between a stuck bit configuration (below the refresh period as depicted in the middle diagram of Fig. 2) and a healthy configuration (above the refresh period), those VRT cells would be qualified as ISB cells in a DRAM single event effect (SEE) test. It can then be inferred that TID can lead, not only to VRT but also to ISB and this particular 2 GB DRAM technology apparently suffers from such effect.

One can also notice in Fig. 8 that the increase in VRT with TID of the 2 GB DRAM is larger than the one of the 4 GB DRAM. It suggests that the storage PN junction of the 2 GB cell has a larger sensitive depletion volume or more intense electric fields than its 4 GB counterpart.

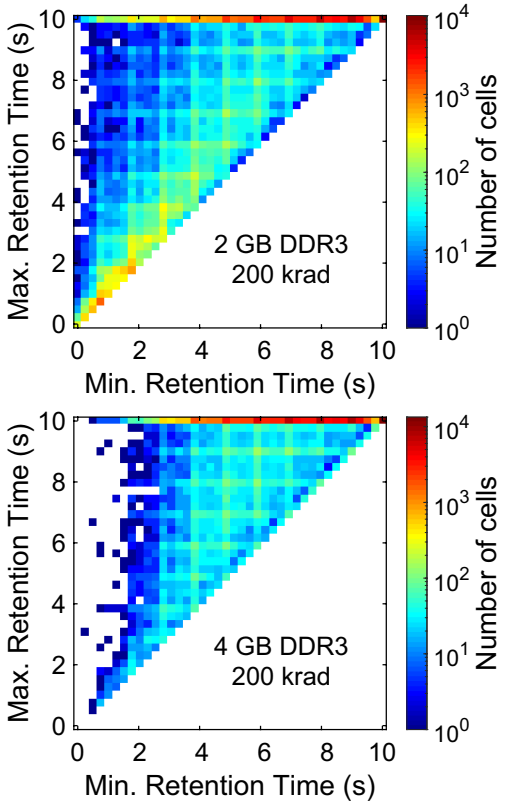

Figure 7. Minimum and maximum retention time distributions of the two types of DRAMs exposed to 200 krad(SiO_2) with the ^{60}Co source. Only about one million cells (1 Mbit) are scanned. Compared to Fig. 6, the number of VRT cells increases further, on both DRAM technologies, when the absorbed TID increases. However, only the 2 GB memory exhibits VRT cells with short enough minimum retention time to act as Intermittent Stuck Bits (ISB).

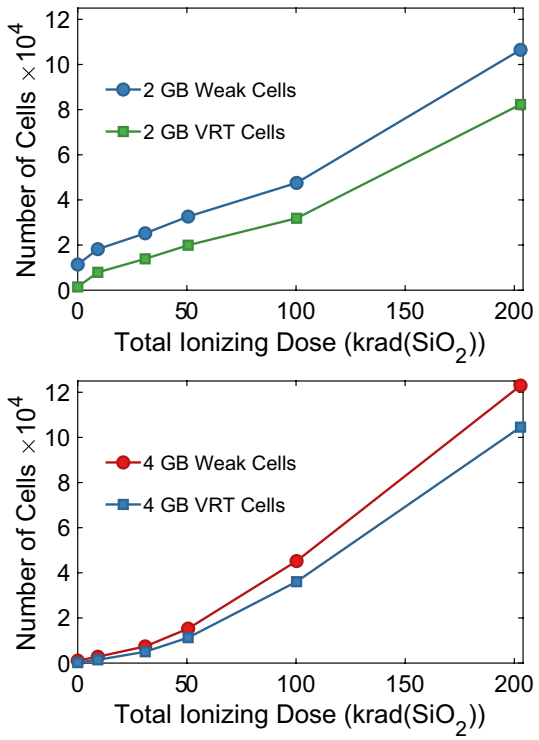

Figure 8. Number of detected weak and VRT cells as a function of TID for the two studied DRAM technologies (^{60}Co irradiations). TID clearly creates both types of defective memory cells (weak and VRT).

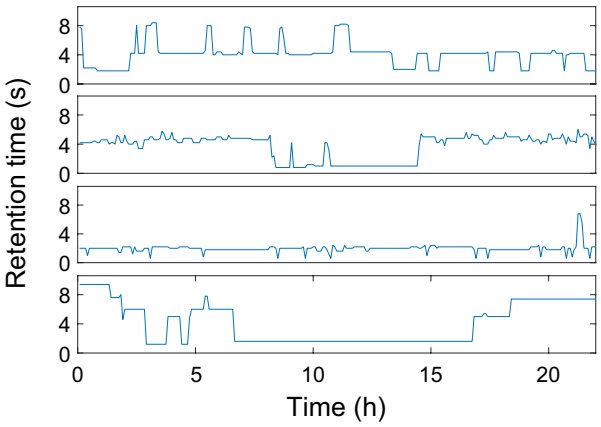

Figure 9. Selected temporal evolutions of the retention time of four DRAM cells exhibiting the VRT phenomenon after exposure to ^{60}Co $\gamma-$rays (from the 2 GB memory).

Overall, the fact that TID generates VRT cells is in very good agreement with the behavior of DC-RTS centers in image sensors where it has been clearly demonstrated that ionizing radiation generates a large number of metastable generation centers at the various CMOS Si/SiO2 interfaces [16], [20].

C. Neutron irradiations

The main effects of 20 MeV neutrons on silicon devices are displacement damage effects that can be summarized as the creation of silicon bulk defects [21]. However, at the fluence used in this work, the indirect TID contribution cannot be neglected.

As mentioned in the introduction, displacement damage is known to be a source of ISB [12]–[14]. Since ISB is most likely due to VRT cells with a minimum retention time that is lower than the refresh period, one can expect to see a clear increase of VRT cells with neutron fluence. This is what is presented in Fig. 10, Fig. 11 and Fig. 12.

Fig. 12 illustrates that the number of VRT cells increases almost linearly with the neutron fluence. However, the number of detected VRT cells (in the 10^3-10^4 range) is close to what is observed in Fig. 8 in the corresponding TID range (between 0 and 15 krad). It strongly suggests that most of the VRT cells created during neutron irradiations are due to TID effects and not to displacement damage.

To estimate further the influence of displacement damage on VRT, Fig. 11 to Fig. 6 can be used to compare the min/max retention time distributions after exposure to ^{60}Co and neutrons for the same order of magnitude of TID. In the 4 GB memory case, it appears clearly that there are many more VRT cells with low minimum retention time in neutron irradiated devices when compared to ^{60}Co irradiations, even if the TID is twice higher in the ^{60}Co case (30 krad vs 15 krad). The same conclusion can be drawn on the 2 GB memory by focusing on the bottom-left corner of the min/max

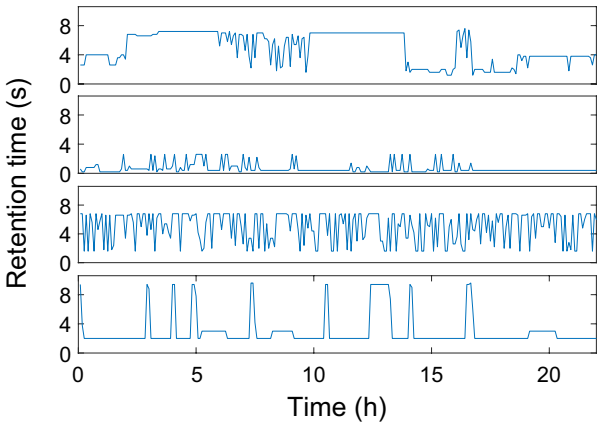

Figure 10. Selected temporal evolutions of the retention time of four DRAM cells exhibiting the VRT phenomenon after exposure to 20 MeV neutrons (from the 2 GB memory).

retention time distribution. In this part of the figures, the neutron irradiated 2 GB memory exhibits much more low retention time VRT cells than the ^{60}Co irradiated one.

To confirm this observation, the evolution with TID of the number of VRT cells with minimum retention times lower or equal to 400 ms is displayed in Fig. 13 for both neutron and gamma irradiations. When exposed to ^{60}Co, the 4 GB memory does not exhibit any VRT cell with retention time below 400 ms and the 2 GB has only a few up to 15 krad. On the contrary, when exposed to neutrons, an important number of VRT cells with low retention time are created when compared to the ^{60}Co case at a comparable TID. This figure clearly shows that neutron induced displacement damage creates VRT cells in DRAMs and that an important number of displacement damage induced VRT cells exhibit a minimum retention time in the failure range in both technologies. This confirms that ISB can be caused by displacement damage induced VRT.

It is interesting to notice in Fig. 10 that clear multilevel VRT are observed after neutron irradiation as well as non-stationary behavior as it is often reported for displacement damage induced DC-RTS [22]

All these observations perfectly agree with the behavior of displacement damage induced DC-RTS in solid-state image sensors and they demonstrate that bulk defects can induce VRT in DRAM cells (as well as ISB).

D. Time Constant Distribution

Since many observed VRT cells exhibit a complex multi-level and often non-stationary behavior, extracting a time constant per RTS/VRT level is not straightforward. A first step in studying the time constants of such complex RTSs can consist in counting the number of RTS or VRT transitions during a complete VRT measurement and for each VRT cells. The average time constant of the studied VRT phenomenon is then given by the overall VRT measurement duration (22.5 h) divided by the number of VRT transitions. Even if this time constant is not as accurate as a per level time constant, it gives a first idea of the timescale at which the phenomenon occurs.

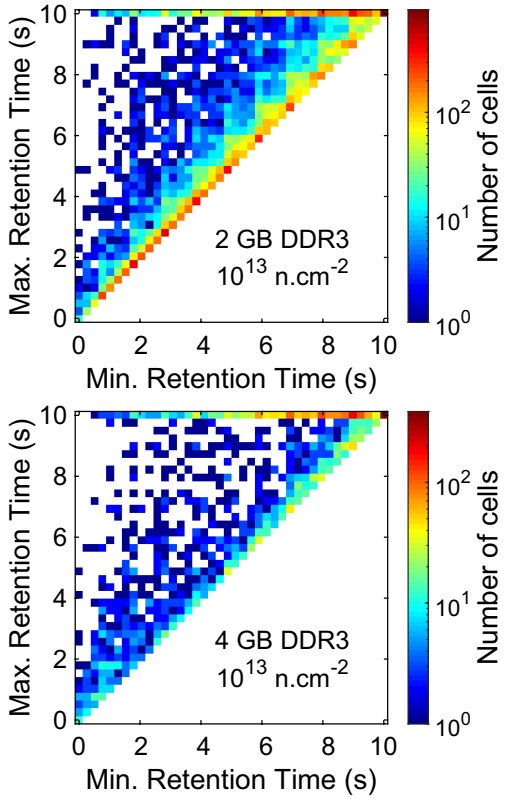

Figure 11. Minimum and maximum retention time distributions of the DRAMs exposed to 10^{13} cm^{-2} 20 MeV neutrons (corresponding TID $\approx$ 15 krad). Only about one million cells (1 Mbit) are scanned. Compared to the devices exposed to ^{60}Co gamma-rays at 30 krad(SiO_2) (Fig. 6), many more low minimum retention time VRT cells (extreme left part of the diagrams) are created whereas the absorbed TID is twice lower. Is shows that neutron induced displacement damage leads to the creation of VRT cells and that those cells can exhibit much lower retention times (i.e. much higher leakage currents) than TID induced ones.

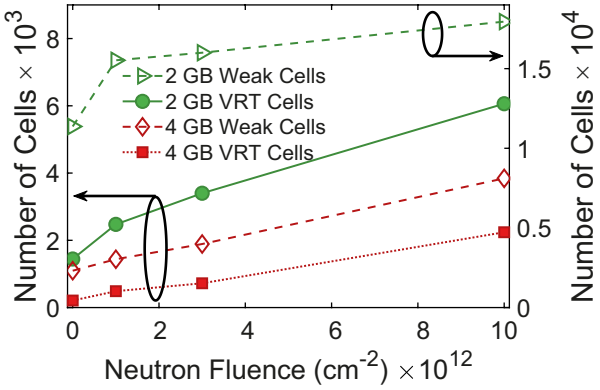

Figure 12. Evolution of the number of detected weak and VRT cells as a function of the neutron fluence for the two DRAM technologies. Both populations grow but the it cannot be concluded from this graph if this increase is only due to TID or if the displacement damage dose plays a role.

Fig. 14 presents the distribution of the number of transitions detected for each detected VRT cells of the 4 GB DRAM exposed to 100 krad of TID. It clearly shows that, as usually observed for DC-RTS, the random switching mechanism is not restricted to a given time range and that all the time constants

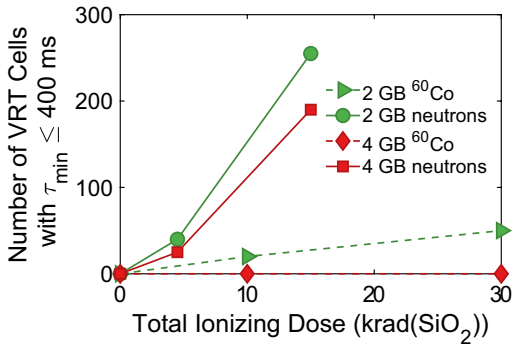

Figure 13. Evolution of the number VRT cells with minimum retention time lower than 400 ms as a function TID for the two DRAM technologies and the two irradiation sources. This figure clearly reveals that displacement damage increases the number of low minimum retention time VRT cells in both DRAM technologies.

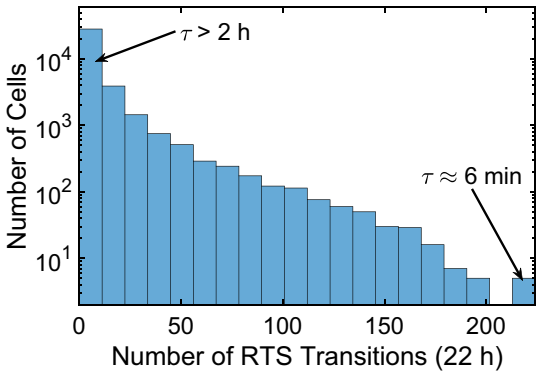

Figure 14. Distribution of the number of RTS transitions per VRT cells over 22.5 h measured at 60°C on the 4 GB DDR3 DRAM exposed to 100 krad. Time constants are well distributed over the studied time range, as usually reported for leakage current RTS mechanisms.

DRAM Cell Id	Irradiation	Eact Amplitude (eV)	Eact Max (eV)	Eact Min (eV)	Eact Ntrans (eV)
a	neutron	-0.64	-0.56	-0.40	0.28
b	neutron	-0.51	-0.54	-0.58	0.50
c	neutron	-0.33	-0.38	-0.54	0.29
d	neutron	-0.44	-0.38	-0.26	0.32
e	gamma	-0.20	-0.29	-0.38	-0.16
f	gamma	-0.07	-0.13	-0.17	-0.20
g	gamma	-0.04	-0.17	-0.30	0.33
h	gamma	-0.29	-0.36	-0.40	0.20

Table I
EXTRACTED ACTIVATION ENERGIES ON THE VRT AMPLITUDE (EACT AMPLITUDE), THE MINIMUM VRT LEVEL (EACT MIN), THE MAXIMUM VRT LEVEL (EACT MAX) AND THE NUMBER OF RTS TRANSITION PER 22 H (EACT NTRANS) OF THE VRT TRACES ILLUSTRATED IN FIG. 15.

that can possibly be observed in this test are effectively seen. The same result (same distribution shape) has been obtained on all the tested DRAM and the same conclusion can be drawn on all the studied devices and irradiation conditions.

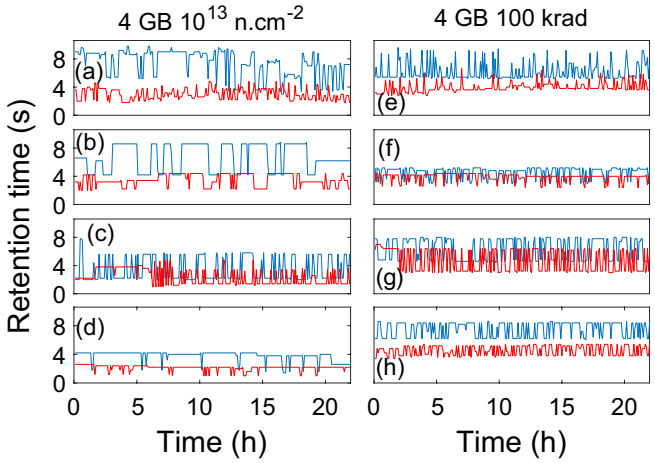

Figure 15. VRT traces selected for the activation energy estimation on the 4 GB DRAM. Blue traces have been measured at 50°C and red traces at 60°C. Rising the temperature enhances the leakages current and so decreases the retention times. The specific evolution with temperature of the VRT parameters is discussed in the text.

E. Evolution With Temperature

RTS behaviors in semiconductor devices are always temperature activated and most of their characteristics follow an Arrhenius law characterized by an activation energy E_{act}.

To perform an activation energy estimation and to ensure that the VRT traces to follow stay in the very limited dynamic range of the VRT measurement (retention times from 200 ms to 10 s), only two close temperatures were used: 50°C and 60°C. Selected traces that fit inside the retention time measurement windows at both temperature and with an almost stationary behavior over the 22.5 h measurement duration (at both temperatures) are displayed in Fig. 15 and the resulting activation energies (extracted in the stationary part of the traces when clear change of behavior is observed during the 22.5 h measurement) are presented in Tab. I.

The observed reduction of minimum, maximum and amplitude of the retention time variations in Fig. 15 when the temperature increases corresponds to the fact that the leakage current is activated by the temperature and that the retention time is inversely proportional to the leakage current. Some of the amplitude activation energies for the neutron irradiated DRAM cells correspond well to the typical $\approx$ 0.55 eV generally measured on DC-RTS in the absence of electric field enhancement, i.e. in a state-of-the-art photodiode [23]. However, most of the leakage current related (i.e. retention time related) activation energy are below the classical mid-gap value strongly suggesting an important role of high magnitude electric fields [24], [25]. This effect is much more pronounced in the gamma-ray irradiated DRAM, showing that oxide/silicon interface VRT centers are more exposed to intense electric fields than bulk defects. Overall, the leakage current activation energies observed here correspond very well to the distribution obtained for DC-RTS centers placed artificially in high magnitude electric field (see for example Fig. 17 in [20]).

Regarding the number of RTS transitions per VRT measurement (which is inversely proportional to the overall time constant), their activation energies are lower than the usually reported value in unirradiated DRAM (0.7 to 1.5 eV [2], [4], [26], [27]). Compared to the radiation induced DC-RTS literature, those time constant activation energies are also lower than the range reported in [15] and [28] (i.e. between 0.55 and 0.9 eV) but they are in good agreement with the time constant distribution shown in [29] and with the range reported in [30] (0.36-0.54 eV).

Finally, the negative Eact Ntrans values in Tab. I (corresponding to VRT traces that slow down when temperature increases) are probably due to the fact that at 60°C the VRT is too fast to allow the detection of all their RTS transitions leading to an apparent increase of the time constant with temperature. This effect may also contribute to the fact that all the time constant activation energies reported here seem in the lower part of the reported range.

V. Discussion

It is well admitted in literature that VRT is due to the Variable Junction Leakage (VJL) phenomenon [3]. The root cause of VJL is generally attributed to generation-recombination (G-R) centers that switch randomly between several generation rates [3]. Similar meta-stable generation centers are also believed to be at the origin of DC-RTS in CIS [21], [31]. In both cases (VRT and DC-RTS), the RTS phenomenon originates from the depletion region of a reverse biased PN junction. Hence, it is then assumed in the following that the defect at the origin of the VRT, or the DC-RTS, is located inside a reverse biased PN junction under non-equilibrium condition with $pn << n_i^2$ and with both the electron and hole concentrations much lower than their equilibrium concentrations (conditions described in details in [32]). In these conditions, the dominant Shockley-Read-Hall (SRH) process is the generation, i.e. the continuous emission of an electron and a hole from the defect state.

This hypothesis means that classical interface states and border traps (at the origin of low frequency noise and MOSFET channel RTS [3], [33]) cannot explain alone VRT and DC-RTS since they would act as stable SRH generation centers in such conditions, not as meta-stable generation centers[2]. Such trapping/emission centers could however play the role of the modulator in the trap modulator case discussed in the following section.

The generation rate of the G-R center can be significantly increased by the electric field through EFE effects [24] such as barrier lowering (Poole-Frenkel effect) or tunneling. Whether or not the generation rate of the G-R center is enhanced by a high magnitude electric field does not change the nature of the responsible defect: it is only the physical mechanism through which the defect emits electron and holes that is modulated by the electric field.

[2]Indeed, the well-known RTS behavior of the MOSFET channel current is well explained by the trapping and emission of a channel carrier by a classical interface state/border trap whereas the studied VRT phenomenon requires a meta-stable defect that switches between several generation rates. The fundamental difference between MOSFET channel RTS and leakage current RTS such as VRT, VJL and DC-RTS is discussed in details in [3], [31]

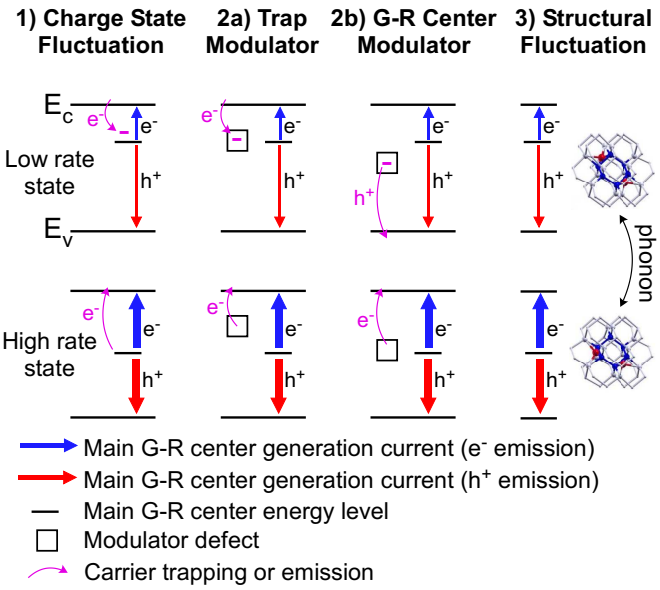

Figure 16. Illustration of the possible VRT origins. For the charge state fluctuation (1) and the modulator cases (2a and 2b), only a few possibilities are represented but all the combinations of electron and hole capture and emission can be considered to justify the change of charge state [26], [35].

A. Known Sources of VRT in Unirradiated DRAMs

VRT and VJL in DRAM are generally attributed to Gate-Induced-Drain-Leakage (GIDL) [34] with TAT as the main underlying mechanism [3], [27]. The defect at the origin of VRT is thought to be located at the Si/SiO_2 interface and silicon bulk defects are not mentioned as a possible source of VRT.

There are three main causes considered to explain the meta-stability of the G-R current at the origin of VRT and VJL [3], [26], [27] (see Fig. 16):

1) The charge state fluctuation of a G-R center (involving the emission or capture of an electron or a hole)
2) The modulation of a G-R center current due to the fluctuation of charge state of a nearby trap (also involving the emission or capture of an electron or a hole)
3) The structural fluctuation of a complex defect between two or more configurations

Since this defect state is emitting thousands of electrons (and holes) per seconds, it is unlikely that one of those electrons (or holes) stay sometimes trapped in the same defect state for hours to change its charge state and thus its generation rate. Hence, the first mechanism (case (1) in Fig. 16) does not seem applicable to the studied situation.

The second mechanism is based on a first defect (the modulator) whose charge states can fluctuate by capturing or emitting electrons or holes and a second nearby defect that acts as the main G-R center [35], [36] (see (2a) and (2b) in Fig. 16). The main G-R center is a source of an important generation current that is modulated by the charge state of the first defect through the interaction of the two defects (such

as the local stress induced by the different charge states of the modulator). The charge state of the modulator can either change by interacting with a single band (through capture and emission of the same type of carrier, case (2a)), or by interacting with the two bands (e.g. by generation electron-hole pairs, case (2b)). For instance, the modulator could be located inside an oxide and the main G-R center could be a classical interface state. In the silicon bulk the modulator could be buried inside a defect cluster.

In the considered case (reverse biased PN junction under non-equilibrium conditions), it is very unlikely that the modulator (case (2a)) manages to trap a carrier since it is very close to the main G-R center, and so in the close proximity of the depleted region where the electron and hole concentrations are much lower than their equilibrium concentrations.

Even if the trap modulator could rarely capture a carrier after a very long time (explaining the long time constants), the emission time constant which does not depend on the carrier concentration would be very short compared to the capture time constant and VRT/RTS up and down time constants would be extremely different (which is not the case). Indeed, as demonstrated by the ratio of the electron emission and capture time constants [35]:

$$\frac{\tau_e}{\tau_c} = \exp\left\{\left(E_{Fn} - E_t\right)/kT\right\}, \qquad (1)$$

the electron quasi-Fermi level E_{Fn} has to be nearly equal to the trap energy level E_{Fn} to obtain emission and capture time constants in the same order of magnitude. Such condition can only be met at the very edge of the depletion region (where E_{Fn} is still within the band-gap) where the defect generation rate is known to be very low, which is not in good agreement with the fact that VRT/VJL current usually corresponds to very high generation rates. So, to explain the usual reported VRT behaviors, the modulator and the main G-R center would have to be in different parts of the depletion region while being close enough to each other to let the modulator influence the G-R center.

The modulator could also act as a slow G-R center (case (2b)) with a very weak generation current (see the G-R center modulator case in Fig. 16). In this case the charge state fluctuation of the modulator G-R center between the emission of a hole and an electron would explain the generation current discrete fluctuations of the nearby fast G-R center. Such mechanism seems possible but disagrees with some experimental observations such as the fact that increasing the electric field magnitude enhances the RTS center generation rate but not its time constant (which depends on the modulator generation rate that should also be enhanced by the electric field) as can be seen in [29](Fig. 15), in [37](Fig. 13 and 14) and in [38](Fig. 19). Time constant activation energies higher than 0.63 eV as well as multilevel and non-stationary VRTs are also difficult to justify with this G-R center modulator model.

Finally, the last proposed mechanism (case (3) in Fig. 16) is the structural fluctuation model proposed in [26] as a possible cause of VJL but also proposed before to explain dark current fluctuations in avalanche photodiode in [39] and DC-RTS in CCDs [15], [40]. As discussed in the next section, this model

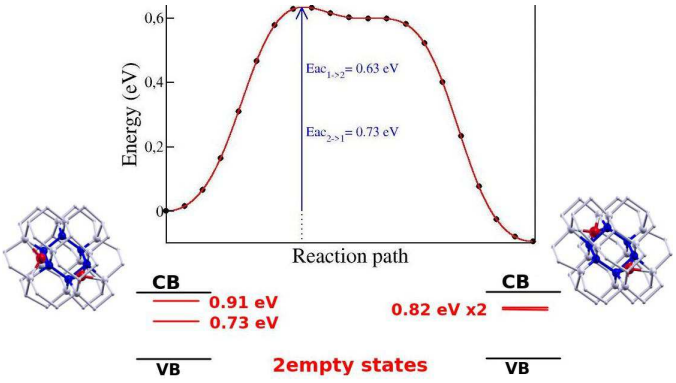

Figure 17. Reaction path separating two configurations of the quadrivacancy, one of the many radiation induced defects that exhibits a spontaneous change of configuration. This particular example exhibits a potential barrier in very good agreement to the ones observed on DC-RTS. The details of the atomic scale simulation of displacement damage in silicon that led to this figure can be found in [44].

is in good agreement with all the reported behavior of VRT. The V_2O_x complex has been identified as possible source of VRT that can undergo spontaneous structural fluctuations [4], [5].

B. Known Sources of DC-RTS

DC-RTS in solid state image sensor is caused by generation centers in the depletion region of reverse biased photodiodes that exhibit meta-stable generation current levels [31]. Even if electric field enhancement has been proposed in the past to justify the large DC-RTS amplitudes in early work on CCDs [15] and active pixel sensor technologies [28], recent results on state-of-the-art CIS technologies tend to indicate that the electric field does not play a significant role in the generation rate of DC-RTS centers [17], [23], [37], [41] except if an electric field hot spot is created by design [42] or if DC-RTS is studied in non-optimized PN junction with much higher electric fields than the photodiode [37]. Hence, the physical generation mechanism behind photodiode DC-RTS current in mature silicon image sensor technologies is considered to be a classical SRH generation current without EFE.

Regarding the location of those DC-RTS centers, it has been clearly established that they can originate from any Si/SiO_2 interfaces (gate oxide, pre-metal-dielectric interface, gate oxide...) in unirradiated sensors [42] and that bulk DC-RTS centers are nonexistent (or extremely rare) in unirradiated sensors [43]. In CIS exposed to TID, all Si/SiO_2 interfaces surrounding the photodiode have been identified as possible source of DC-RTS centers [16], [29]. Finally, after a displacement damage irradiation, it is well known that DC-RTS is caused by bulk defects in CCDs [15] as well as in CISs [17] and in any kind of silicon device.

The most widely accepted concept to explain the metastability of the generation current in image sensors is the structural fluctuation of a complex defect between several configurations [21] as proposed by Hopkins and Hopkinson [15], [40]. Trapping and emission of charge carriers is still sometimes

mentioned as a possible cause of the structural fluctuation [21] but, as discussed in sec. V-A, this is unlikely.

Since the structural fluctuation theory does not involve a change of charge state, it is fully compatible with the validated idea that DC-RTS are located in the photodiode depletion region where no free carrier lays to be trapped. As it has been done for VRT in DRAMs with the V_2O_x complex [4], [5], several authors tried to identify a particular defect that could exhibit such structural fluctuations and so that could explain DC-RTS. The Phosphorous-Vacancy (P-V) center has been proposed in early work [40] and is frequently mentioned [38], [45]. However, the broad distribution of the DC-RTS characteristics (amplitudes, time constants, number of levels, activation energies...) strongly suggests that DC-RTS is not due to a single well identified defect but to a wide variety of complex defects, such as the ones that can be found in a defect cluster. Moreover, a recent study [46] has demonstrated that the phosphorous concentration in the photodiode does influence the DC-RTS behavior and so that the P-V center is not a significant source of DC-RTS. This conclusion agrees well with the fact that the typical annealing behavior of DC-RTS corresponds well to what is known about defect cluster annealing [47].

Recent atomic scale simulations [44], [48] of displacement damage induced defects in silicon and their relaxation with time and temperature have demonstrated that many flickering defects are created by non-ionizing interaction and that many of them continue to oscillate between several configurations even after a long relaxation time corresponding to the time scale at witch DC-RTS measurements are performed. One of the many "flickers" generated by such simulations is presented in Fig. 17. The wide variety of complex defects with structural fluctuation that are generated by this simulation approach exhibit a range of fluctuation time constants and multi-state behaviors in good agreement with the broad dispersion of DC-RTS characteristics mentioned previously. Those observations strongly support the idea mentioned previously that defect clusters (with structural fluctuation) are the root cause of DC-RTS in image sensors exposed to displacement damage.

It is well known that interface states are more than a single well identified point defect and that the wide variety of possible defect structures at or near the interface lead to a continuum of energy states in the bandgap. This description seems very similar to the wide variety of defect structures that can be found in a silicon bulk defect cluster. Therefore, it can be inferred that the spontaneous flickering behavior exhibited by many complex silicon bulk defects, without a change of charge state, is most likely also exhibited by many interface state defect structures (such as the identified V_2O_x complex but probably not only). Such interface state flickers could explain interface state induced DC-RTS (before and after exposure to ionizing radiation).

C. Comparison to Reported Results on Irradiated DRAMs

It is clear that the defects at the origin of DC-RTS in image sensor photodiodes are present in any CMOS circuit PN junction. The only reason why they are only reported in image sensors is the extreme sensitivity to leakages of modern image sensors (as it is the case for modern DRAM cells). Hence, those defects most likely play an important role in DRAM VRT.

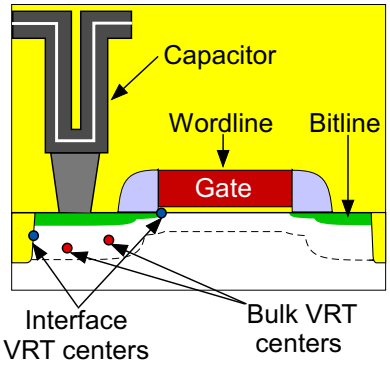

Figure 18. Cross sectional illustration of a DRAM cell (not to scale) showing the identified sources of radiation induced VRT.

All the results reported here agree very well with the idea that VRT centers in DRAMs are the same defects as the ones responsible for DC-RTS in image sensors before irradiation and after exposure to ionizing or non-ionizing radiation. Indeed, both technologies exhibit leakage current RTS behavior coming from oxide interfaces before irradiation. Radiation induced RTS centers are created the same way in both types of device with the same particularity and the same type of RTS traces. The few estimated activation energies are in fairly good agreement if it is considered that VRT center generation rates are enhanced by high electric fields whereas DC-RTS centers in modern CIS photodiodes are not (as expected from DRAM and image sensor literature).

The lowest amplitude activation energies found on gamma irradiated devices compared to neutron irradiated DRAM confirm that the most intense electric fields are located at the Si/SiO_2 interface, probably in the vicinity of the polysilicon gate (since GIDL is recognized as the main generation mechanism involved in DRAM VRT). The fact that neutron induced VRT also exhibit activation energies lower than 0.55 eV suggests as well that the electric field can still be significant far from the polysilicon gate or the interface and so that active VRT centers are probably distributed in several regions on the PN junction.

VI. Conclusion

In this work, it is demonstrated that both ionizing radiation and non-ionizing radiation induce variable retention time in DRAMs cells. In the case of a full size modern DRAM, the number of VRT cells can be large enough to be a critical source of bit errors by inducing intermittent stuck bits. For this reason, detecting and understanding the origin of VRT cells is of primary importance, especially for DRAM operation in radiation environments.

It is concluded that the defects at the origin of DC-RTS in irradiated and unirradiated silicon image sensors (CCDs, CISs, SPADs, APSs...) are likely to be the same as the ones causing VRT in pristine and irradiated DRAMs. Two types of

VRT centers have been highlighted as illustrated in Fig. 18: Si/SiO_2 interface VRT centers and bulk VRT centers. The first ones exist before irradiation and their density is increased by the absorption of ionizing radiation dose, as in image sensors. The bulk VRT defects are probably very rare in non-irradiated devices and their number increases with the displacement damage dose.

The reported activation energies suggest that interface and bulk VRT center generation rates are enhanced by high magnitude electric fields whereas this is usually not the case in CMOS image sensor photodiodes. This conclusion is in good agreement with the widely accepted principle that trap assisted tunneling plays an important role in the generation rate of VRT cells in unirradiated DRAM.

The spontaneous structural fluctuation of complex defects, without capture or emission of a charge carrier, seems to be the most appropriate explanation to justify the generation current metastability for both interface defects and bulk defects. Charge state fluctuation through the capture or emission of charge carriers could also be a possible cause but this explanation seems less compatible with the observed behaviors.

Finally, this study strongly suggests that radiation induced VRT is the main cause of intermittent stuck bits in irradiated DRAMs.

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