NOVEL SINGLE PHASE DC-AC INVERTER TOPOLOGY WITH ENHANCED POWER QUALITY

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2014

NOVEL SINGLE PHASE DC-AC INVERTER TOPOLOGY WITH ENHANCED POWER QUALITY

by

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Thesis submitted in fulfillment of the requirement for the degree of Master of Science

February 2014

ACKNOWLEDGEMENTS

I would like to gratefully acknowledge the contributions of several people who have helped me to complete my course, entitled Novel Single Phase DC-AC Inverter Topology with Enhanced Power Quality. In particular, I would like to convey my grateful thanks to my supervisor, Dr. Shahid Iqbal for giving me valuable assistance to overcome most of my problems in my work. He has given me a lot of valuable advices, comments and guidelines throughout the completion of this project.

Besides that, I would like to express my appreciation to laboratory tutor, Mr. Mohamad Nazir Bin Abdullah and fellow technicians, Mr. Jamaludddin Bin Che Amat, Mr. Ahmad Shaukhi Bin Noor, Mr. Hairul Nizam Bin Abdul Rahman, Mr. Elias Bin Zainuddin for their willingness to help and share some knowledge during the project making. In addition, I also would like to express my gratitude to my fellow course mates whom gave me encouragement, support and advice. They have helped me a lot to overcome several problems that I face during completion of this course.

Last but not least, I would like to dedicate this report to my parents that giving me long way support and encouragement to my studies. They are the one who is above all for giving me strength, motivation and guidance to successfully complete this project.

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LIST OF ABBREVIATIONS

AC	Alternating current
ADC	Analog to digital converter
A/D	Analog/digital
BPWM	Bipolar pulse width modulation
CSI	Current source inverter
DC	Direct current
DC-AC	Direct current to alternating current
EMI	Electromagnetic interference
HPWM	Hybrid pulse width modulation
IGBT	Insulated gate bipolar transistor
I/O	Input/output
LC	Inductor and capacitor
MOSFET	Metal oxide semiconductor field effect transistor
op amp	Operational amplifier
PCB	Printed circuit board
PV	Photovoltaic
PWM	Pulse width modulation
RC	Resistor and capacitor
rms	Root mean square
SPWM	Sinusoidal pulse width modulation
THD	Total harmonic distortion
UPS	Uninterruptable Power Supply
UPWM	Unipolar pulse width modulation

VSI	Voltage source inverter
ZCS	Zero current switching
ZVS	Zero voltage switching

LIST OF SYMBOLS

A_c	Amplitude of reference signal
A_r	Amplitude of carrier signal
C	Capacitor
C_H	Holding capacitor
C_i	Input capacitor
C_S	Snubber capacitor
D	Diode
f_c	Carrier frequency
f_o	Output frequency
f_s	Switching frequency
I_{DS}	Drain to source current
I_{in}	Input current
I_L	Inductor current
I_{out}	Output current
I_p	Peak current
L	Inductor
L_C	Current limiting inductor
L_L	Inductive load
m_a	Amplitude modulation index
m_f	Frequency modulation index
N_1	The number of turn in primary winding of transformer
N_2	The number of turn in secondary winding of transformer
p	The number of pulses per half cycle
P_{on}	Conduction loss
P_{in}	Input power
P_{out}	Output power
P_s	Switching power loss
R	Resistor
R_L	Resistive load
S_1, S_2, S_3, S_4	1^{st}, 2^{nd}, 3^{rd}, 4^{th} power switch

S_c	Control power switch
$t_{c(on)}$	Turn on crossover interval
$t_{c(off)}$	Turn off crossover interval
t_{on}	Turn on time
t_{off}	Turn off time
T_s	Switching time period
V_{DS}	Drain to source voltage
V_{GS}	Gate to source voltage
V_H	Holding voltage
V_{in}	Input voltage
V_{out}	Output voltage
V_{on}	Conduction voltage
V_p	Peak output voltage
V_{sense}	Sensing voltage
V_Z	Breakdown voltage of zener diode
$W_{c(on)}$	Dissipated energy during turn on
$W_{c(off)}$	Dissipated energy during turn off
W_{on}	Dissipated energy during conduction
Z	Impedance
δ	Width per pulse
δ_m	Width of *m*th pulse
ωt	Period in radian
η	Efficiency

PENYONGSANG AT-AU SATU FASA TOPOLOGI NOVEL DENGAN KUALITI KUASA TERTINGKAT

ABSTRAK

Penyongsang digunakan secara meluas dalam banyak aplikasi seperti photovoltaic (PV), bekalan kuasa tanpa gangguan (UPS) dan sebagainya untuk menukarkan kuasa arus terus (AT) kepada kuasa arus ulang alik (AU). Cabaran utama dalam reka bentuk dan pelaksanaan penyongsang adalah merealisasikan kecekapan yang lebih tinggi dan kualiti kuasa keluaran yang baik. Bagi mencapai tujuan tersebut, tesis ini membentangkan penyongsang AT-AU satu fasa topologi novel dengan kualiti kuasa tertingkat. Dalam topologi ini, satu suis disambung pada lengan bawah suis-suis penyongsang tetimbang penuh untuk mengawal voltan keluaran pada penyongsang tersebut. Suis dibawah lengan tetimbang penuh tersebut mengawal keluaran penyongsang tetimbang penuh dengan meningkatkan atau mengurangkan tahap voltan pada lengan bawah tetimbang. Suis dilengan bawah ini dikawal oleh isyarat pensuisan modulasi lebar nadi sinusoidal (SPWM) berfrekuensi tinggi. Manakala suis-suis kuasa penyongsang tetimbang penuh beroperasi dengan isyarat pensuisan gelombang segi empat pada frekuensi 50 Hz. Topologi yang dicadangkan ini menghasilkan gelombang keluaran sinusoidal yang jelas dengan gangguan rendah dan dengan kehilangan pensuisan yang minimum, seterusnya dapat menghasilkan keluaran yang berkualiti tinggi pada kecekapan yang tinggi. Seterusnya, penyongsang pensuisan rawak modulasi lebar nadi hibrid (HPWM) dibangunkan untuk memberi perbandingan antara penyongsang yang dicadangkan dengan penyongsang pensuisan rawak HPWM. Kedua-dua simulasi komputer dan eksperimen telah dijalankan untuk mengesahkan prestasi topologi yang dicadangkan.

Daripada keputusan yang dikemukakan, ia menunjukkan bahawa topologi yang dicadangkan mempunyai prestasi yang lebih unggul berbanding dengan lawannya itu. Didapati bahawa penyongsang yang dicadangkan boleh menghasilkan voltan AU yang mempunyai jumlah herotan harmonik (THD) kurang daripada 5 % pada kecekapan lebih daripada 92 %.

NOVEL SINGLE PHASE DC-AC INVERTER TOPOLOGY WITH ENHANCED POWER QUALITY

ABSTRACT

Inverters are widely employed in many application such as photovoltaic (PV), uninterruptable power supply (UPS) etc for the conversion of direct current (DC) power to alternating current (AC) power. The key challenges in design and implementation of inverters are the realization of higher efficiency and good quality output power. To achieve these, this thesis presents a novel single phase DC-AC inverter topology with enhanced power quality. In this topology, a switch is connected at the lower arm of the full-bridge switches to control the output voltage across the full-bridge inverter. The switch at the lower arm of the full-bridge controls the output of full-bridge inverter by increasing or reducing the voltage level at the lower arm of the bridge. This switch of lower arm is controlled by a high frequency sinusoidal pulse width modulation (SPWM) switching signal. While the power switches of full-bridge inverter operate with square wave switching signal at a frequency of 50 Hz. The proposed topology produces a clean sinusoidal output waveform with low distortion and with minimum switching losses, thus yielding high quality output at high efficiency. Next, a random switching hybrid pulse width modulation (HPWM) inverter is developed in order to give a comparison between the proposed inverter and the random switching HPWM inverter. Both computer simulation and experiment were carried out to verify the performance of proposed topology. From the presented results, it is shown that proposed topology has superior performance compared to its conventional counterpart. It was found that proposed

inverter can produced an AC output voltage with less than 5 % total harmonic distortion (THD) at efficiency of more than 92 %.

CHAPTER 1

INTRODUCTION

1.1 Background

The global electricity consumption has been continuously increasing over the last decade. It was estimated that the consumption of electricity is around 19.09 trillion kWh worldwide and growing each year [1]. It can be said that fossil fuels have been primary source in generating electricity in this present. As the world is concerned with fossil fuels exhaustion and environmental problems caused by conventional power generation, a renewable energy sources, particularly solar energy, have become very popular and demanding. Solar energy has experienced a remarkably rapid growth in the past decade because of its abundant power and pollution free characteristic [2, 3].

The popularity of solar energy has lead the growth in power electronic research particularly inverter as it is the most important interface between solar energy sources and load. Inverter is one of the converter families which are called DC to AC converter. Basically, it converts direct current (DC) to alternating current (AC) as well as DC voltage to AC voltage at the desired magnitude and frequency. A variable output AC voltage can be obtained by either varying the input DC voltage and maintaining the switching gain or maintaining the input DC voltage and varying the switching gain. The switching gain controllable can be achieved by pulse width modulation (PWM) control circuit. The switching gain control is normally accomplished by controlling the modulation index of the PWM where modulation index could be defined as the ratio of reference signal to carrier signal [4].

In general, there are two types of input DC source for inverter which is voltage source and current source. Inverter that is fed by a DC voltage source is referred to as voltage source inverter (VSI), while inverter that is fed by a DC current source is referred to as current source inverter (CSI). Both of these types have their own advantages. However, the VSI is more popular compare to current source inverter in industrial markets, particularly in renewable energy applications [5, 6]. Moreover, the VSI design has proven to be more efficient, have higher reliability and faster dynamic response [7].

Inverter can be classified into two classes which are single-phase inverter and three-phase inverter. Inverter can be divided into four categories depend upon the output waveform namely square wave inverter, modified sine wave inverter, multilevel inverter, and last but not least pure sine wave inverter [8]. Square wave inverter was a pioneer of inverter development and already obsolete design that has a lot of harmonic content. It is not well suited for running motor, transformer and most modern appliances. The modified sine wave is a good approximation of a sine wave. Modified sine wave inverter initially more economical than pure sine wave inverter, and it has the advantages when the load is simple induction load like motor or a resistive load like a light bulb because it typically use DC more efficiently than their pure sine wave inverter counterpart. However, with today's technological advancement and the rapid proliferation of sensitive electronics that requires pure sine wave to operate correctly, the pure sine wave inverter is more preferable because it produce nearly perfect sine wave with less than 3% total harmonic distortion (THD) which is essentially the same as utility grid supply [9]. In addition, with the advance in power inverter research and development, the pure sine wave

inverter is now become more and more economical in cost prices. Meanwhile, multilevel inverter has emerged recently as a very important alternative particularly in high power medium voltage area. It operates by synthesizing a desired voltage from several levels of DC voltage as its input and generates a stepped voltage waveform as its output. This inverter is no better than pure sine wave in term of THD produced, but it actually can reduce power rating in power devices thus giving it advantages to be used in high power conversion [10].

Studies in recent past have introduced various kinds of inverters. Most of the researches works concentrate on reducing power losses, reducing total harmonic distortion, and increasing the efficiency of the inverter. The most important factor in demanding high efficiency is less amounts of losses i.e. heat dissipate in power devices. Inverter which normally consist of a few number of power switches arranged to control the flow of energy in the circuit. In the ideal case, there would be no power loss in the power switch since either the current in the switch is zero during the switch off or the voltage across the switch is zero during the switch on. In real case, there are two mechanisms that create losses which are switching loss and conduction loss [4]. Harmonic distortion is the change in the voltage waveform from the ideal sinusoidal waveform. The most important factor that cause distortion in power inverter are the kind of modulation used, nonlinearities in the output filter, dead times, the direct voltage drop across the power switch (V_{DS}) and modification of the voltage of the DC-link [11]. The standard measure used to characterize the distortion magnitude is the total harmonic distortion (THD) [4].

The typical half-bridge and full-bridge inverters are widely employed and famous in various applications particularly in photovoltaic (PV) system. With

growing PV applications for grid connected as well as standalone application, the demand for higher efficient inverter has become the driving factor toward the development of more efficient, robust and cost effective inverter for the PV system. Another popular and common application of inverter is Uninterruptable Power Supply (UPS) which is used to provide emergency power to a load when the input power source typically mains power fails. UPS is typically used to protect computers, data centers, telecommunication equipment or other sensitive equipment from unexpected power disruption that can cause fatalities to load systems. UPS can be classified as either offline or online. An offline UPS will connect the load to the mains power for most of the time and switch over to the inverter when the mains power fails. On the other hand, an online UPS will always connect the load to the inverter [12, 13].

1.2 Problem statement

Inverter is one of the power conversion systems that convert DC power to AC power. One of the most important performance considerations for inverter is its energy conversion efficiency. The main challenges in DC-AC inverter are the high efficiency and low THD power density.

In order to get low THD output power, studies in pass have introduced sinusoidal pulse width modulation (SPWM). Basically, in SPWM full-bridge switches are commutating at high switching frequency. Unfortunately, the use of high switching technique will result in high switching losses. Moreover, with the large number of power switches that operate in high switching will increase the switching losses in overall inverter system [23-24].

Later, some researchers have introduced techniques that reduce the number of switch in full-bridge that operated at high switching frequency which consequently reduce switching losses. These techniques have efficiently reduced switching losses without degrading the quality of the output power and without increasing the cost of development. However, these techniques have very complex switching generation thus make it a little more difficulty to be implemented [30-32].

Consequently, the need for new design of a single phase inverter that has higher efficiency and lower THD is crucial. In order to fulfill the required factor, a new topology of a single phase DC-AC inverter had been proposed in this thesis. This inverter is proved to have higher efficiency of overall system, low power losses in power devices, low THD, smaller filter size and lower cost of equipment. An experimental prototype was made to test and analyze the performance of the design.

1.3 Objectives

The aim of this research work is to design and develop a novel single phase inverter. The main objectives of this research can be summarized as:

i. To propose a novel topology of a single phase DC-AC inverter.
ii. To design and develop a 100 W prototype of proposed single phase DC-AC inverter.
iii. To evaluate the performance of proposed topology by simulation and experimental result.
iv. To compare the operation and performance of proposed topology with the random switching HPWM inverter.

1.4 Methodology

Methodology adopted to complete this research work can be described as follow. It begins with literature review on the inverter design and topologies and switching technique used in the design. Various topologies were reviewed in order to highlight the advantages and disadvantages of each topology. Next, a novel single phase DC-AC inverter is proposed. Then in the next step, the proposed novel single phase DC-AC inverter is simulated in Pspice. The purpose of the simulation is to verify the working principle of the proposed topology and to estimate the expected result. After verification by simulation result, an experimental prototype was designed, developed and tested. Finally, results are obtained, analyzed and discussed. Figure 1.1 shows the flowchart that indicates the summary of methodology process flow used in this research.

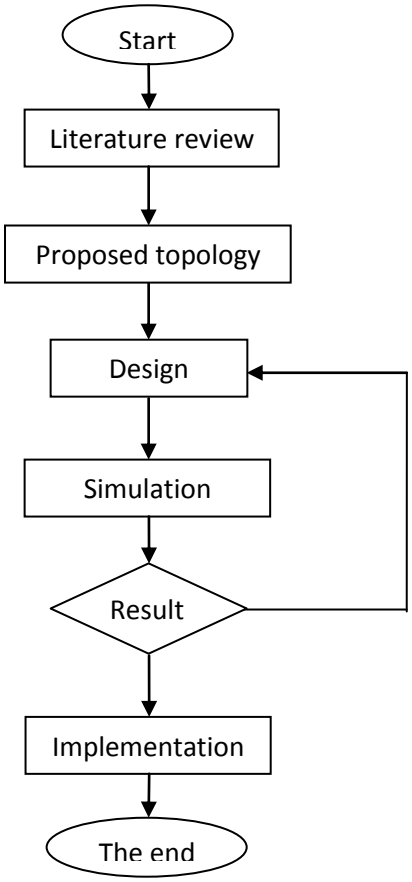


Figure 1.1: Research flowchart

1.5 Thesis outline

This thesis basically discusses and analyzes a novel single phase DC-AC inverter. The thesis consists of a study of a novel topology single phase inverter, the SPWM switching circuit, gate drive circuit, design work and implementation of inverter. The analysis of thesis is focused on the output of the inverter and its measurement such as analysis of the voltage, current and power and also harmonic distortion. This thesis is divided into six main chapters.

Chapter 1 gives general overview of the power inverter. This chapter also outlines the objectives, problem statement. Furthermore, this chapter also states the methodology used during the research.

Chapter 2 is about previous scientific research regarding various single phase inverter topologies, the applied switching technique, some theoretical formulas and calculation. This chapter also highlights some technical mechanism such as switching losses and THD that normally occur in real case scenario.

Chapter 3 basically describes the methodology of the proposed inverter. This chapter discusses two power electronic circuits which are proposed novel single phase DC-AC inverter and random switching hybrid pulse width modulation (HPWM) inverter. The discussion is focused on the topology description and control arrangement of the circuits, as well as their operating principle.

Chapter 4 basically describes the design and implementation of the inverter. It includes the tools and equipments such as control circuit based on analogue control which consist of operational amplifier (op-amps), comparator and control circuit based on microcontroller which consist of PIC microcontroller, related programmer

and some design software. In addition, this topic also covers the procedure and processes that are involved in hardware and software development of the entire project such as the main circuit and related programmer descriptions.

Chapter 5 presents and discusses the results obtained from the simulation as well as results from experimental work. It also discusses the results obtained from each part of the entire project. The results obtained from proposed inverter are compared with random switching HPWM inverter.

Chapter 6 summarizes the entire work done in this thesis. It also makes recommendations for further research on this topic in the future.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

In concept, the inverter operates by turning on and off switches in a specific order and configuration. The objective of inverter is basically to produce a sinusoidal AC output whose magnitude and frequency can both be controlled. Studies in past literature have introduced some basic topologies of single phase inverter which are single phase half-bridge inverter, single phase full-bridge inverter and single phase push-pull inverter. These inverters are the pioneer of inverter topology and each of them have their own advantages. Later, an overview on existing switching techniques is presented. The earlier technique introduced was single pulse width modulation then follow by multiple pulse width modulation, sinusoidal pulse width modulation and modified sinusoidal pulse width modulation. Finally, a review on recent studies is featured. Various topologies and techniques are presented and discussed based on the fundamental concept of the basic operation of each topology and technique. A comparison was made in order to highlight the advantages and deficiencies of each topology discussed.

2.2 Basic single phase inverter topologies

Generally, there are two classifications of inverter which are single phase inverter and three phase inverter. However, the three phase inverter is not discussed and reviewed in this chapter since it was not used in this research work. The single phase inverter can be divided into three basic topologies which are half-bridge inverter, full-bridge inverter and push-pull inverter. These three inverters are

obviously different in configuration and arrangement. Among these topologies, the full-bridge inverter are most widely employed in various industrial applications such as photovoltaic (PV) interface, uninterruptable power supply (UPS), AC motor drive, active filter and etc [14] – [18].

2.2.1 Half-bridge inverter

For the half-bridge inverter two switches and two capacitors are used to form the half-bridge configuration. The half-bridge inverter operates by turning on S_1 and turning off S_2 in the first half cycle and turning off S_1 and turning on S_2 in the second half cycle. Figure 2.1 shows the topology of the half-bridge inverter. The advantages of this topology are it is simple in its configuration because it uses fewer switches to operate and has lower conduction losses compared the full-bridge inverter [19]. Unfortunately, the half-bridge inverter only produces peak output voltage V_P equal to half of its input voltage V_{in}. The peak output voltage V_P is equated as:

$$V_P = \frac{V_{in}}{2} \tag{2.1}$$

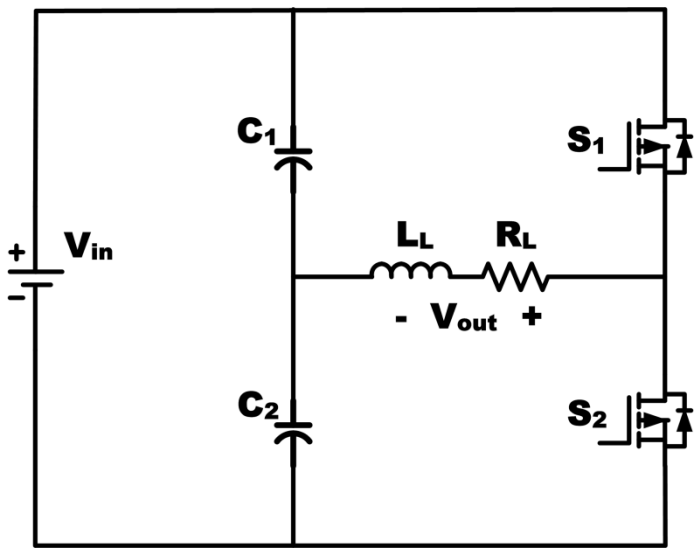


Figure 2.1: Single phase half-bridge inverter

2.2.2 Full-bridge inverter

In full-bridge inverter four switches are used to form the full-bridge inverter. The full-bridge inverter operates by turning on S_1 and S_4 as well as turning off S_2 and S_3 in the first half cycle. For the second half cycle S_1 and S_4 are turned off while S_2 and S_3 are turned on. Figure 2.2 shows the topology of the full-bridge inverter. The advantages of this topology are the peak output voltage V_P is equal to the input voltage V_{in}. This means that it produces twice output voltage and twice output power than the half-bridge inverter [20]. Unfortunately, this topology has slight difficulties in its gate drive circuit because two switches are floating with respect to ground. The peak output voltage V_P is equated as:

$$V_P = V_{in} \tag{2.2}$$

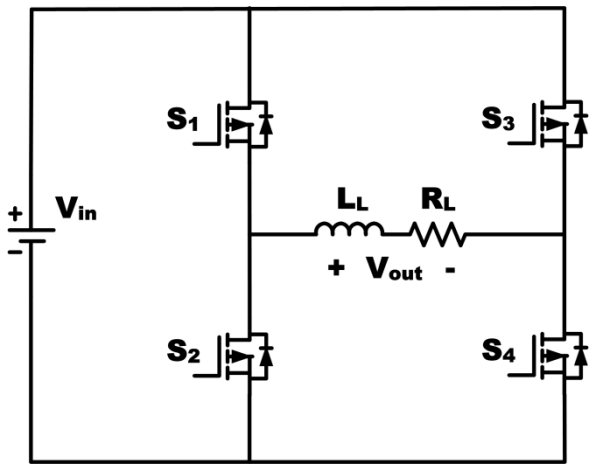


Figure 2.2: Single phase full-bridge inverter

2.2.3 Push-pull inverter

In push-pull inverter, two switches and one center tap transformer are used to form the push-pull configuration. The push-pull inverter operates similarly like the half-bridge inverter where S_1 is turned on and S_2 is turned off in the first half cycle and S_1 is turned off and S_2 is turned on in the second half cycle. Figure 2.3 shows the topology of the push-pull inverter. The advantage of this topology is it has simple

gate drive circuit because both switches are referred to ground. Unfortunately, this inverter has some drawbacks where it may has voltage overshoot during switch is turned off due to leakage inductance of the transformer. Therefore, a snubber circuit is needed in order to remove the drawback [21]. Furthermore, the use of transformer may reduce the efficiency of the inverter system due to transformer losses. The peak output voltage V_P is equated as:

$$V_P = \frac{N_2}{N_1} V_{in} \tag{2.3}$$

where,

N_1 = the number of turn in primary winding

N_2 = the number of turn in secondary winding

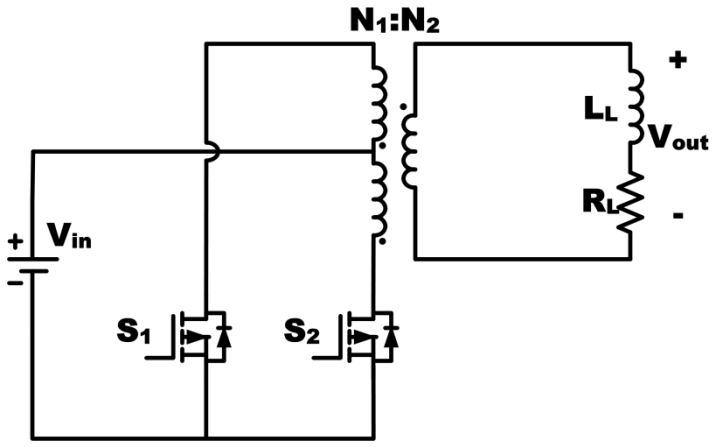


Figure 2.3: Single phase push-pull inverter

2.3 Overview on existing switching technique

In inverter, the most efficient method in order to achieve the requirement for voltage and frequency control is by applying certain switching techniques. In these techniques, a pulse width modulation (PWM) is used. By applying the PWM technique, a switching gain is achieved and hence the ability to control the output voltage is possible by adjusting the switching gain. There are various kind of techniques have been recorded in the past work but the commonly used technique are

single pulse width modulation, multiple pulse width modulation, sinusoidal pulse width modulation (SPWM) and modified sinusoidal pulse width modulation. In this section, all the mentioned technique is discussed where all of them are assumed operated in single phase full-bridge topology.

2.3.1 Single pulse width modulation technique

In single pulse width modulation technique, there is only one pulse per half cycle. The output voltage can be controlled by varying the width of the pulse. Figure 2.4 shows the generation of switching signals and output voltage of the technique. The switching signals are generated by comparing a rectangular waveform (reference signal) with a triangular waveform (carrier signal). The amplitude modulation index m_a is defined as:

$$m_a = \frac{A_r}{A_c} \tag{2.4}$$

where,

A_r = amplitude of reference signal

A_c = amplitude of carrier signal

The rms output voltage is defined as:

$$V_{out\,(rms)} = V_{in}\sqrt{\frac{\delta}{\pi}} \tag{2.5}$$

where,

δ = width per pulse

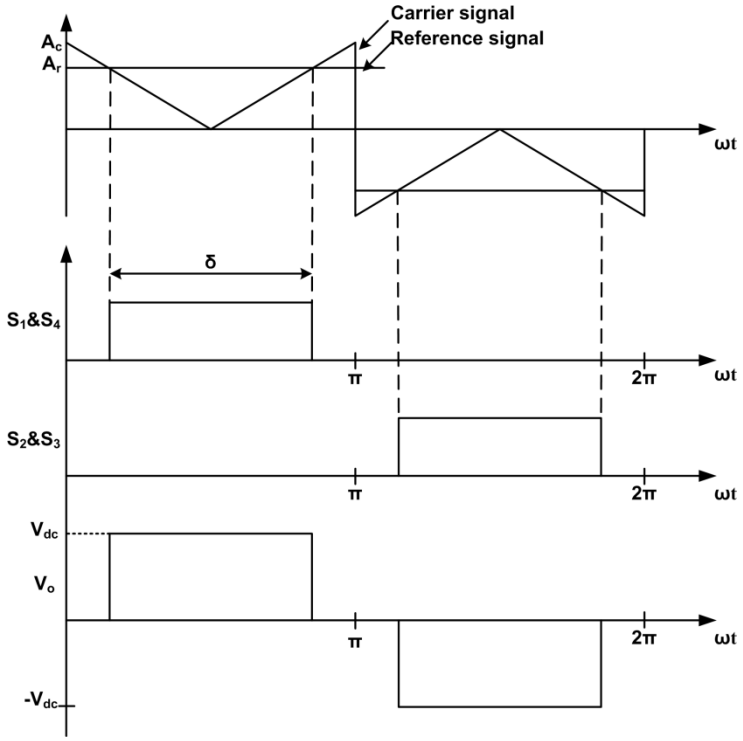


Figure 2.4: Key waveform of single pulse width modulation technique

This technique is allowing the switches to commutate at one time per cycle, thus make the inverter have less switching losses [22]. Unfortunately, the technique produces a lot of harmonic content and has higher magnitude of the 3rd harmonic order. This deficiency makes the technique unsuited for modern appliances which operate by sensitive electronic devices.

2.3.2 Multiple pulse width modulation technique

This technique basically is the extension of the single pulse width modulation technique. In this technique, a several pulses are used in each half cycle of output voltage. Due to this, the harmonic content in the output waveform is reduced [22]. Figure 2.5 shows the generation of switching signals and output voltage of the technique. The switching signals are just like the previous technique where a rectangular waveform (reference signal) is compared with a triangular waveform (carrier signal) but the triangular is in multiple forms.

The frequency of reference signal determines the output frequency f_o and the carrier frequency f_c determines the number of pulses per half cycle p. The amplitude modulation index m_a is similar to the previous technique which is in Equation 2.4. The frequency modulation index m_f is defined as:

$$m_f = \frac{f_c}{f_o} \tag{2.6}$$

The number of pulses per half cycle can be equated as:

$$p = \frac{f_c}{2f_o} \tag{2.7}$$

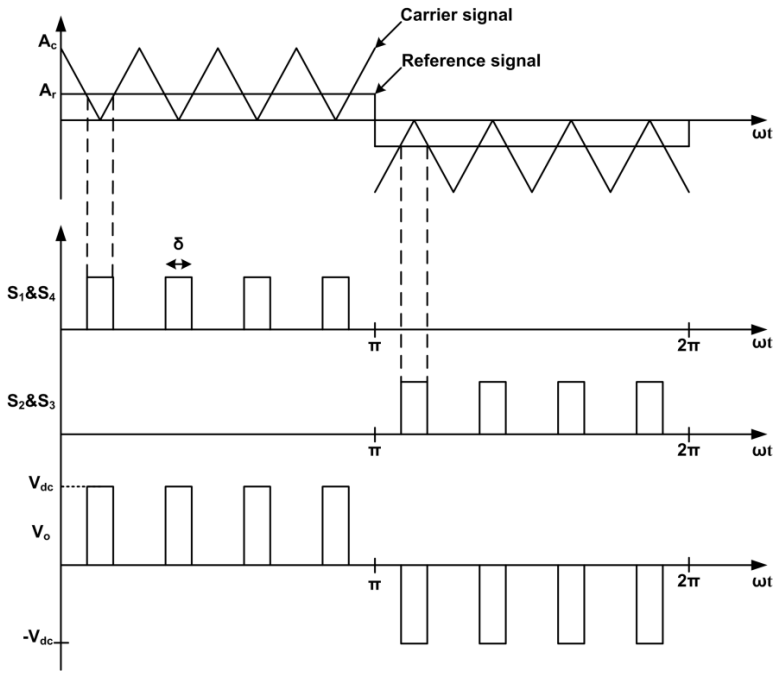


Figure 2.5: Key waveform of multiple pulse width modulation technique

The rms output voltage can defined as follow, where δ is the width of each pulse:

$$V_{out\,(rms)} = V_{in}\sqrt{\frac{p\delta}{\pi}} \tag{2.8}$$

2.3.3 Sinusoidal pulse width modulation (SPWM) technique

SPWM is commonly used in industrial applications. In this technique, the switching signals are generated by comparing a sine waveform (reference signal) with a triangular waveform (carrier signal). The width of the switching pulses is

varied proportionally with the amplitude of the sine wave. SPWM can be generated by either two ways which is bipolar PWM (BPWM) or unipolar PWM (UPWM). The amplitude modulation index m_a and the frequency modulation index m_f can be referred in Equations 2.4 and 2.6 respectively. The rms output voltage is defined as:

$$V_{out\,(rms)} = V_{in}\left(\sum_{m=1}^{2p}\frac{\delta_m}{\pi}\right)^{1/2} \tag{2.9}$$

where,

δ_m = width of *m*th pulse

p = number of pulses per half cycle at the output

In BPWM, a single sine wave is compared with the triangular waveform. Figure 2.6 shows the generation of switching signals and output voltage of the BPWM technique. The amplitude A_r controls the amplitude modulation index m_a and the frequency of reference signal determines the output frequency f_o while the carrier frequency determines the switching frequency f_s.

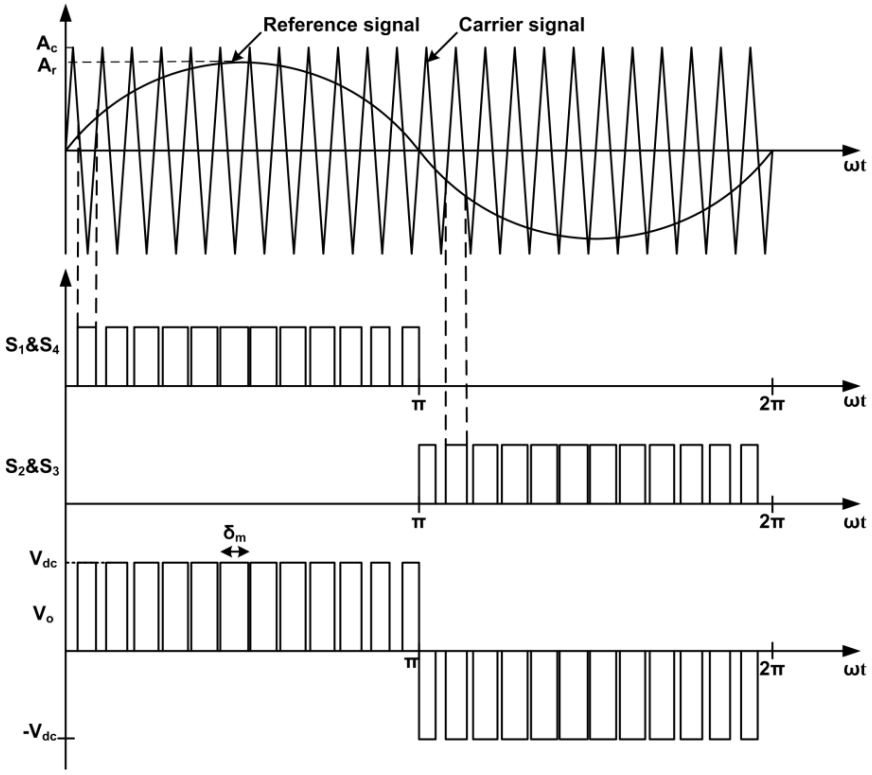


Figure 2.6: Key waveform of BPWM

In UPWM, two sine waves are compared with the triangular waveform. Both sine waves are inversely with each other but have similar amplitude A_r and frequency. Figure 2.7 shows the generation of switching signals and output voltage of the UPWM technique. Similar to the BPWM, the amplitude A_r controls the amplitude modulation index m_a and the frequency of reference signal determines the output frequency f_o while the carrier frequency determines the switching frequency f_s. But, with equal switching frequency to the BPWM, UPWM is able to produce number of pulses per half cycle p at the output twice higher than the BPWM. This means that with equal switching frequency, the performance of UPWM is two times better compared to the BPWM [23 - 24].

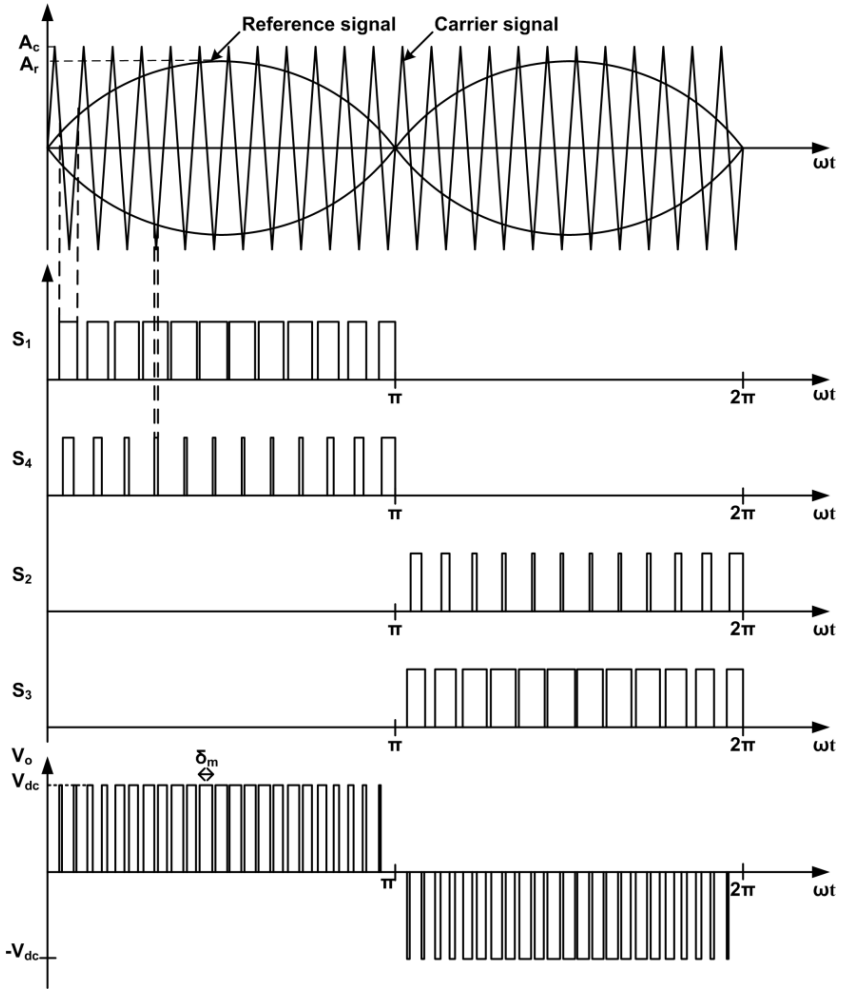


Figure 2.7: Key waveform of UPWM

The advantage of using SPWM is it can produce a high quality output. The high frequency output waveform can be filtered through a filter thus produce an output that has nearly sinusoidal waveform. The generated output also has very low total harmonic distortion (THD). Unfortunately, SPWM technique generates a lot of pulses thus produces higher switching frequency and consequently produces higher switching losses.

2.3.4 Modified sinusoidal pulse width modulation technique

This technique is designed to reduce the switching losses produced by former SPWM technique. It operates by reducing the number of switching pulses nearer to the peak of the sine wave. The technique is achieved by comparing a sine waveform (reference signal) with a modified triangular waveform (carrier signal). Figure 2.8 shows the generation of switching signals and output voltage of the modified SPWM technique.

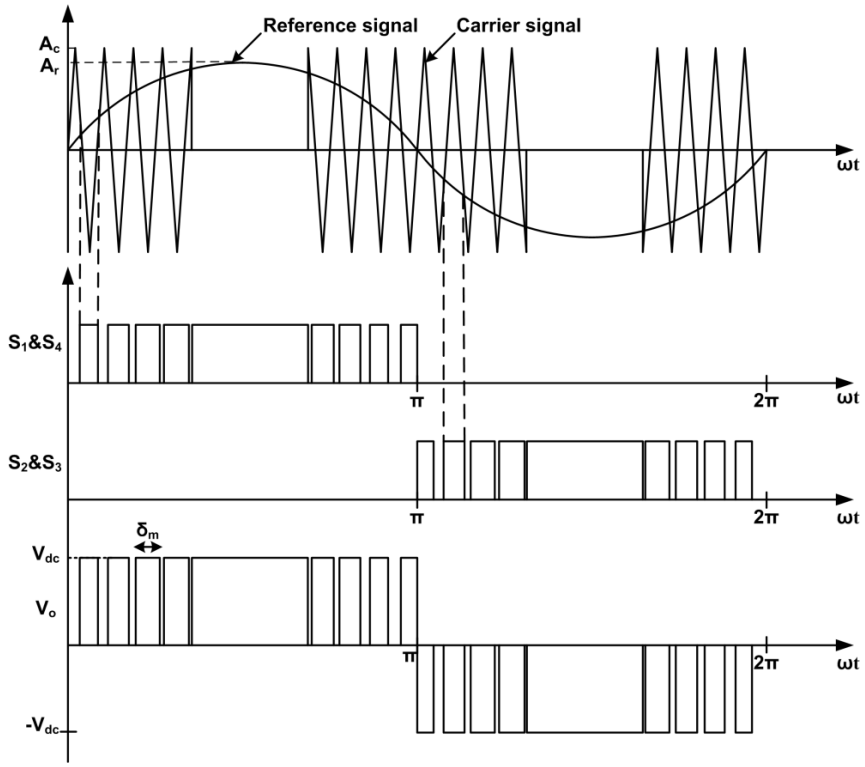


Figure 2.8: Key waveform of modified SPWM technique

Despite being improved in switching losses, this technique does not have lower THD compared to SPWM technique. Thus, this technique does not suitable for applications that require pure sine wave input.

2.4 Power losses in controllable switch

Today, modern power semiconductor devices are very popular in power electronic applications. One of a class of power semiconductor devices which is controllable switches is widely used in power inverter. The controllable switch category includes a number of devices such as metal oxide semiconductor field effect transistors (MOSFETs), and insulated gate bipolar transistors (IGBTs). These devices have major advance in recent years hence increased their power capabilities, ease of control and reduction in cost.

In ideal case, controllable switch has no power losses hence give no effect on operation of overall circuit system. The ideal case for controllable switch will has the characteristics where it can block forward and reverse voltages with zero current flow when turn off, conduct currents with zero voltage drop when turn on, and switch from on to off or vice versa instantly without delay when triggered [4].

Unfortunately, real controllable switch do not has this ideal characteristics and hence dissipate power when operate. There are two mechanisms that create power losses in power inverter which are switching losses and conduction losses [25 - 27]. In order to indicate power dissipation in controllable switch, Figure 2.9 is shown to testify the power dissipation during the operation of the device. Figure 2.9 shows the generation of instantaneous power losses when controllable switch is being operated at switching frequency of $f_s = 1/T_s$, where T_s is the switching time period.

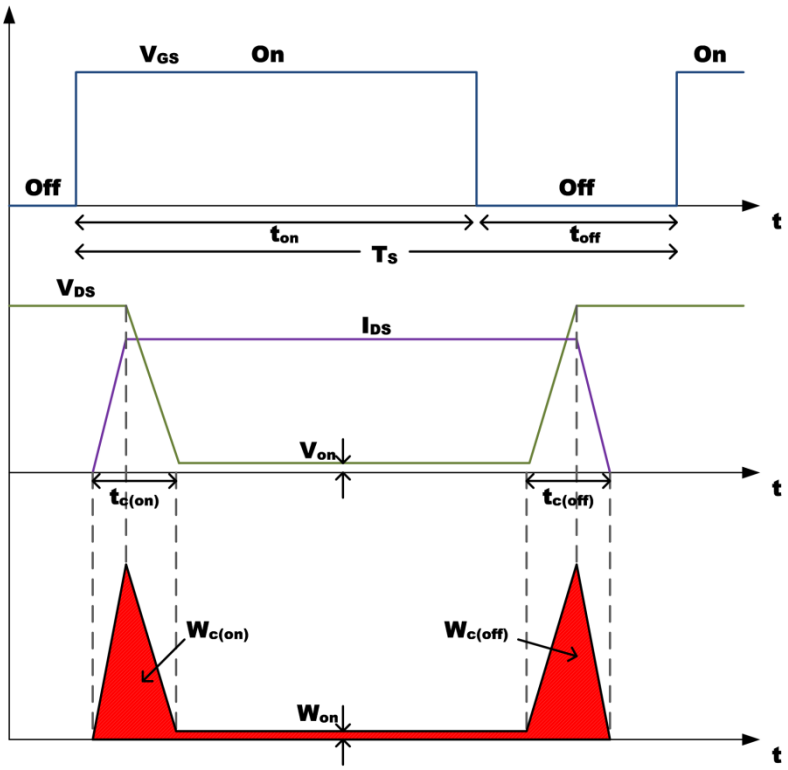


Figure 2.9: Instantaneous power losses

During the turn on transition, the transition of current I_{DS} and voltage V_{DS} consist of short delay time $t_{c(on)}$. During delay time $t_{c(on)}$, large values of voltage and current are present simultaneously hence dissipate energy. The dissipated energy can be approximately equated as:

$$W_{C(on)} = \frac{1}{2} V_{DS} I_{DS} t_{C(on)} \tag{2.10}$$

Similarly during the switch turn off, a short delay occur and large values of voltage and current are present simultaneously during the turn off crossover interval $t_{c(off)}$. The dissipated energy during the turn off crossover interval $t_{c(off)}$ can be approximately equated as:

$$W_{C(off)} = \frac{1}{2} V_{DS} I_{DS} t_{C(off)} \tag{2.11}$$

During the switch is fully turn on, the on-state voltage V_{on} is form in the order of a volt and large amount of current I_{DS} conducted during this time interval. In general, the fully turn on interval is much larger than the turn on and turn off delay transition.

The energy dissipation W_{on} in the switch during this conduction interval can be approximated as:

$$W_{on} = V_{on} I_{DS} t_{on} \tag{2.12}$$

The instantaneous power losses shown in Figure 2.9 make it clear that large instantaneous power dissipation occurs during the turn on and turn off intervals. The switching power loss in the switch varies linearly with the switching frequency. Hence the average switching power loss P_s in the switch can be approximated as:

$$P_s = \frac{1}{2} V_{DS} I_{DS} f_s (t_{C(on)} + t_{C(off)}) \tag{2.13}$$

Another major contribution to the power loss in the switch is the conduction loss which is the average power dissipated during the fully on-state P_{on}, which varies upon the on-state voltage. The conduction loss P_{on} can be equated as:

$$P_{on} = V_{on} I_{DS} \frac{t_{on}}{T_s} \tag{2.14}$$

Since the magnitude of switching loss is greatly depending on the switching frequency, turn on delay and turn off delay, the increment in these variables will result in higher switching loss. Thus, a wide research studies had been done in order to reduce the switching loss by manipulating these variables. Whereas for conduction loss, the voltage drops during turn on is the factor that determines the amount of this loss. The voltage drops characteristic in switch is fixed, thus proper switch with low on-state voltage and low conduction loss is selected in order to reduce this loss.

2.5 Review on recent studies

Studies in recent years have introduced various new topology of the full-bridge inverter in order to reduce the switching losses. It is generally well known that sinusoidal pulse width modulation (SPWM) methods are commonly used in half-bridge and full-bridge inverters to get a high quality output with low total harmonics

distortion (THD). In these techniques, the switches are commutated at high frequency, i.e., the frequency of the carrier signal, but unfortunately, these techniques result in high switching losses [28]. Because of switching losses, the effect of current changes di/dt and voltage changes dv/dt can cause Electromagnetic Interference (EMI) and switching stress on the power devices during the turn on/off operation [29]. In this section, some recent studies is featured and discussed regarding fundamental concept of the basic operation of each topology and technique.

2.5.1 Hybrid pulse width modulation technique

The single phase full-bridge inverter in Figure 2.10 is widely used in various applications. LC filter is used to remove the high frequency characteristic in the output waveform. In conventional full-bridge inverter, all switches are commonly commutated at high switching frequency so that switching harmonic can be filtered more easily. Unfortunately, high switching frequency give rise to high switching losses in power switches thus reduce the efficiency of the inverter.

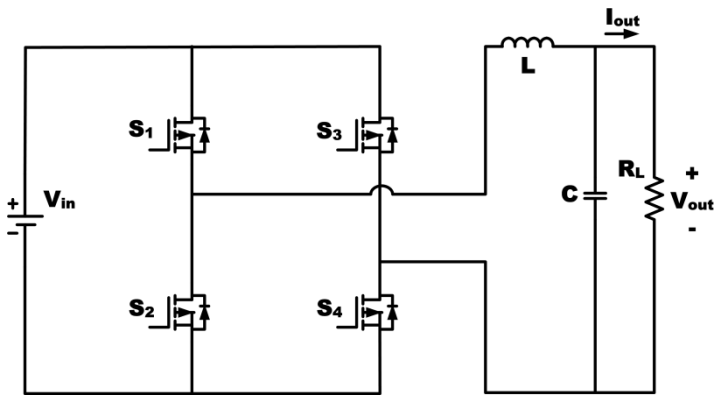


Figure 2.10: Single phase full-bridge inverter with LC filter

Hybrid pulse width modulation (HPWM) technique introduce new switching strategy by commutating only two of the four switches with high switching frequency and leave the other two with low output frequency. Figure 2.11 shows the

gate signal of the proposed HPWM technique. Generally, S_1 and S_2 are assigned to commutate at high switching frequency while S_3 and S_4 are assigned for low switching frequency. Since S_3 and S_4 are commutated at low frequency, their switching losses are greatly reduced. The proposed HPWM technique proved that it can synthesize high quality output waveforms without significant switching losses penalty. It was found out that switching losses of HPWM is similar to unipolar PWM (UPWM), and is approximately half that of bipolar PWM (BPWM) [30]. Unfortunately, it practically suffers from thermal inequality generated in power switches that cause by the switches driven with high switching frequency dissipate more heat in comparison to the switches driven with low switching frequency. Hence, this problem reduces the reliability of the system.

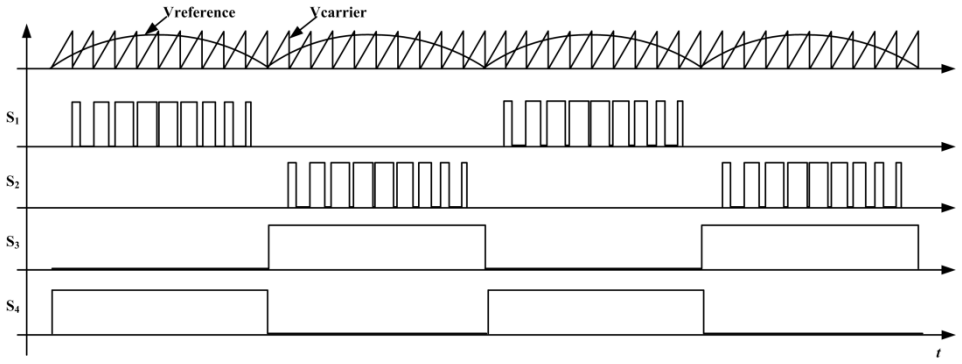


Figure 2.11: Key waveform of HPWM technique

2.5.2 Random switching HPWM technique

In conventional HPWM technique, all the four switches are operated at two different frequencies, S_1 and S_2 commutated at high frequency while the other two, S_3 and S_4 are commutated at low frequency. Typically, the applied switching arrangement reduces switching losses in S_3 and S_4. Unfortunately, this arrangement create new problem, the problem of unequal switching losses and therefore unequal heating among the four switches [31-32]. Thus, a new method is proposed called

random switching HPWM technique designed to overcome the unequal switching losses problem. The proposed random switching HPWM technique commutates all four switches for both high frequency and low frequency randomly. Each switching signals is composed of both high frequency and low frequency. As a result, the averages of switching losses amongst the four switches are equalized. However, this technique requires complicated control circuit in order to generate the switching scheme configuration. Figure 2.12 illustrated the switching scheme of the proposed random switching HPWM technique.

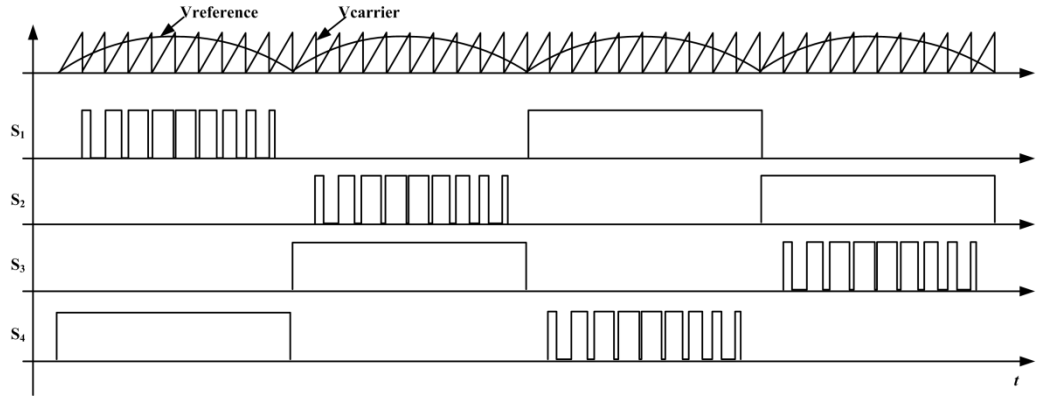


Figure 2.12: Key waveform of random switching HPWM inverter

2.5.3 Zero voltage switching inverter with HPWM technique

This inverter is categorized in a soft switching technique. Soft switching techniques are basically implemented by turn on and turn off switches during the zero current and zero voltage intervals. Soft switching can be achieved by either zero voltage switching (ZVS) and/or zero current switching (ZCS). Various soft switching techniques implementing ZVS and/or ZCS have been proposed recently in order to reduce the switching losses and thus improve the efficiency in inverters. DC-link switches are commonly used in order to achieve ZVS. Authors in [33] have introduced a zero voltage switching single phase inverter using hybrid pulse width modulation technique (ZVS-HPWM). In this topology one switch S_{dc} is connected at

DC-link of the inverter to provide zero voltage switching. The switches $S_1 - S_4$ are the full-bridge inverter and operate in HPWM switching. The efficiency of ZVS-HPWM inverter is improved compared to hard switching HPWM at high switching frequency up to 180 kHz. Unfortunately, it has a complex control arrangement and require additional auxiliary switch with capacitor and inductor that form a resonant circuit in order to achieve ZVS or ZCS. One of the major issues in soft switching technique is the switch voltage stress limitation because it normally requires switch and diode with higher rating than the bridge switches. Figure 2.13 illustrates the topology of the inverter. C_{dc}, C_1, C_2, C_3, and C_4 represent the parasitic capacitors of each switches.

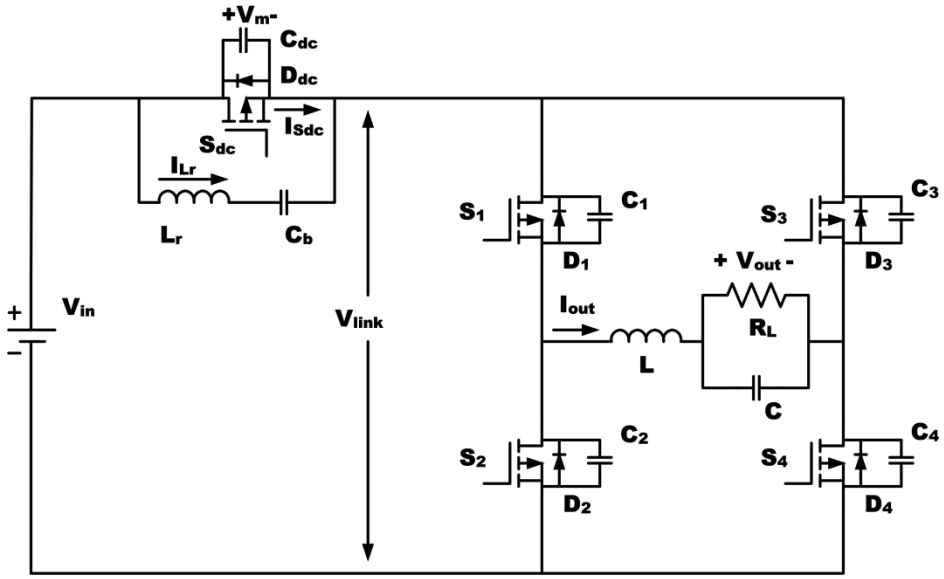


Figure 2.13: ZVS-HPWM inverter

Switch S_1 and S_2 operate in high switching frequency while S_3 and S_4 operate at output frequency. The utilization of high switching frequency in S_1 and S_2 results in high switching losses in both switches. In order to reduce switching losses and improve efficiency of the inverter, zero voltage switching of S_1 and S_2 is introduced

by adding an auxiliary circuit with the additional DC-link switch S_{dc}. The auxiliary circuit consists of switch S_{dc}, inductor L_r, and capacitor C_b.

Figure 2.14 shows the voltage and current waveforms of HPWM inverter operating in ZVS during the positive cycle of the output frequency. During the positive half cycle, switch S_4 is turned on and switch S_3 is turned off all the time, while S_1 is pulse width modulated at high frequency i.e. SPWM signal. During interval t_2, switch S_1 operates in ZVS due to switch S_1 turned on during voltage V_{link} reduces to zero.

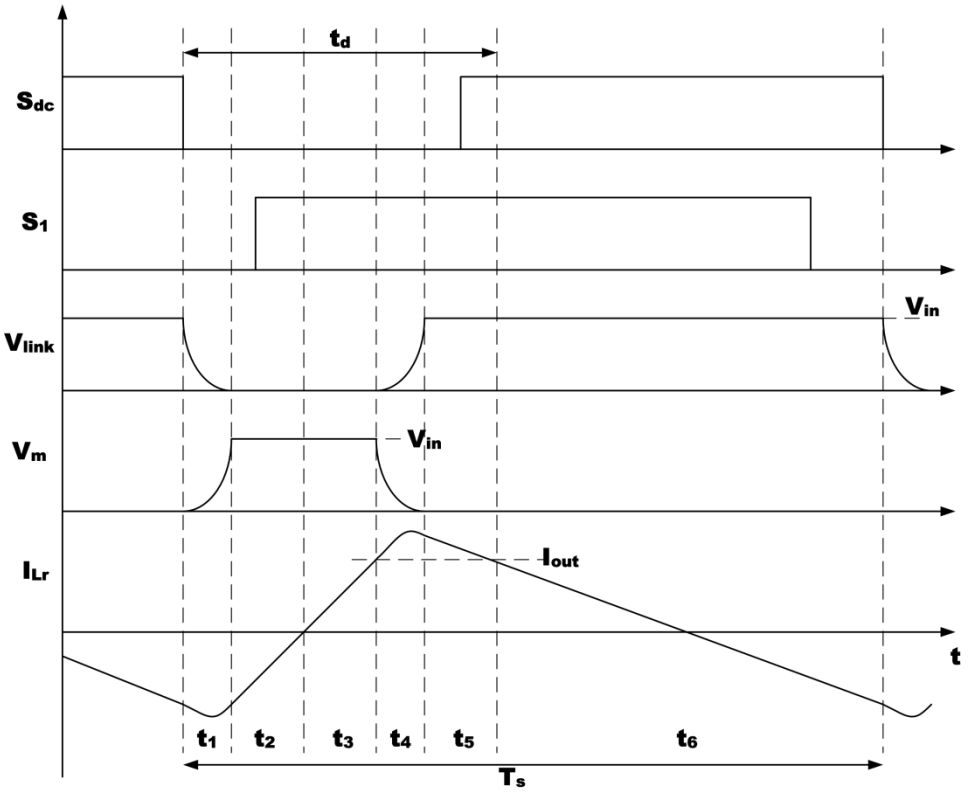


Figure 2.14: Key waveforms during the operation of ZVS for the HPWM inverter

2.5.4 A sine wave inverter with PWM DC-link

In conventional SPWM inverter, a DC-link connects the DC supply to the four switches that form a full-bridge configuration. The four switches are commutated at high frequency with UPWM or BPWM in order to generate sinusoidal output

waveform. Unfortunately, this configuration gives high switching losses because all four switches are conducted at high switching frequency. A sine wave inverter with PWM DC-link proposed a new method where instead of giving SPWM signals to the full-bridge switches the DC-link is replaced by UPWM DC-link [34]. The topology is achieved by connecting a switch at a DC-link of the inverter and commutates the switch with UPWM signal. Figure 2.15 shows the topology of the sine wave inverter with PWM DC-link. Four switches S_1, S_2, S_3, and S_4 form a full-bridge configuration and switch S_5 is connected at DC-link between the DC source and the full-bridge switches.

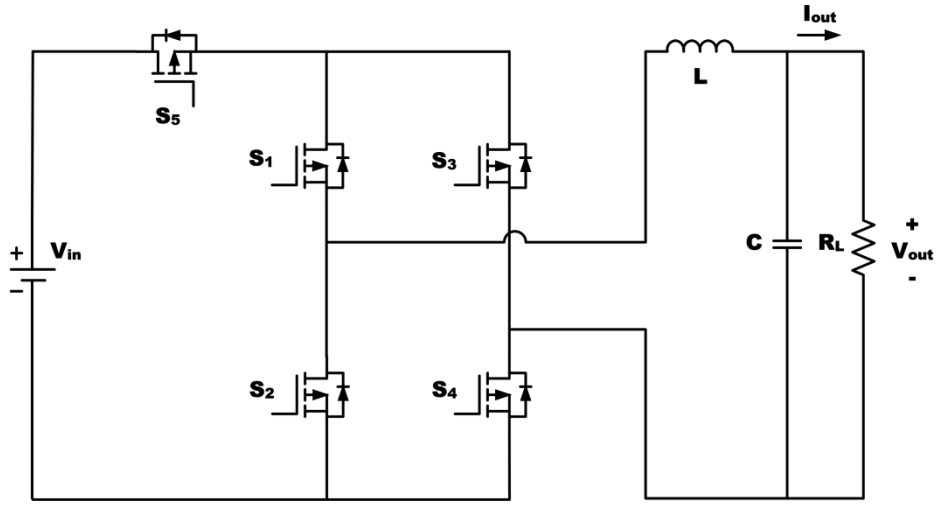


Figure 2.15: Sine wave inverter with PWM DC-link

The full-bridge switches are being commutated with square wave signals at low output frequency where switches S_1 and S_4 are commutated at first half cycle while S_2 and S_3 are commutated at second half cycle. Low frequency commutation of the full-bridge switches reduces the switching losses considerably. Switch S_5 is commutated with high frequency UPWM signal at all time and convert the constant DC flow to the full-bridge switches with SPWM pulses. However, this topology has slight difficulty in implementing the gate drive circuit because one switch is floated

at the DC link. Figure 2.16 illustrated the switching scheme of the proposed sine wave inverter with PWM DC-link.

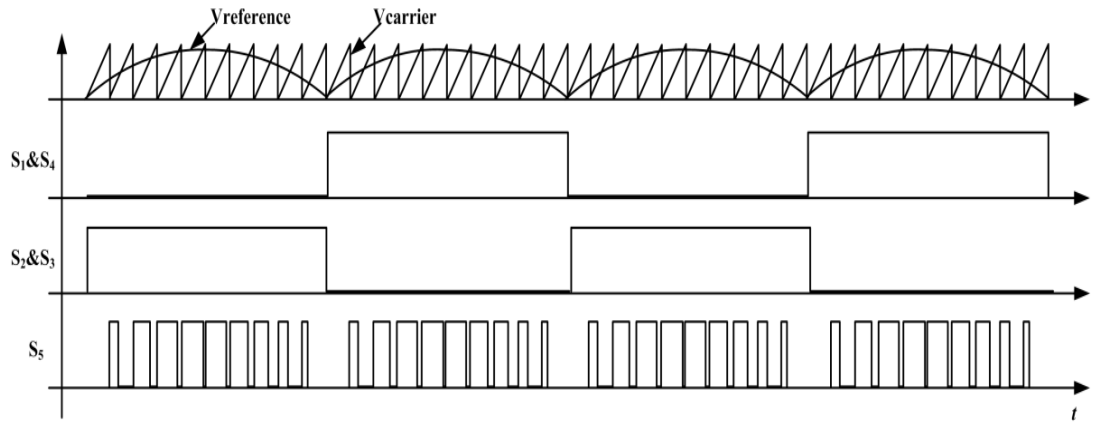


Figure 2.16: Key waveform of sine wave inverter with PWM DC-link

2.5.5 A ZVS-PWM inverter using a voltage clamp ZVS boost DC-link

Authors in [35] proposed A ZVS-PWM inverter using a voltage clamp ZVS boost DC-link. The topology utilize six switches where four switches form a full-bridge and the rest two switches are used for the soft switching. Figure 2.17 shows the topology of the inverter.

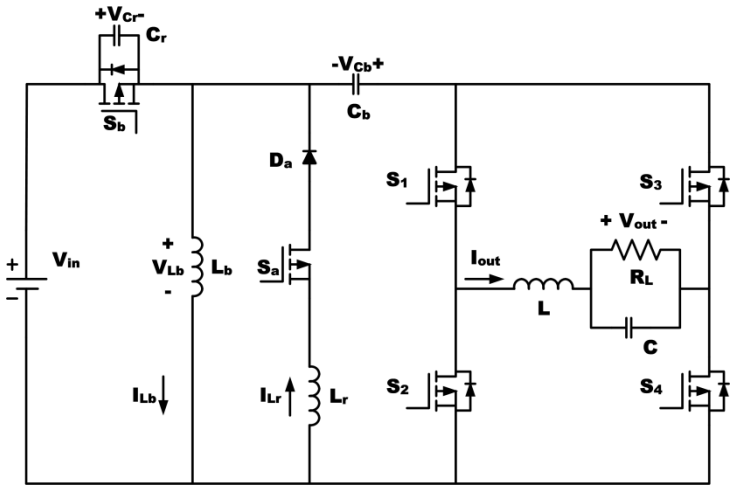


Figure 2.17: ZVS-PWM inverter using a voltage clamp ZVS boost DC-link

The inverter operates by providing unipolar PWM to the full-bridge switches. All four switches are operating under ZVS during turn on and turn off switching thus greatly improves the switching losses. The topology is not only providing soft switching, it also provides boost voltage characteristic. The topology operates in high switching frequency because no switching losses occur thus make the design of output filter smaller. Unfortunately, one switch is floated at the DC link thus make the gate drive circuit of this topology more complex.

2.5.6 A high efficiency inverter for standalone and grid-connected systems

A high efficiency inverter for standalone and grid-connected was proposed by [36] where the topology only adopted five switches and operates in high switching frequency without having high switching losses penalty. The inverter operates in soft switching without having high voltage and current stress. The soft switching characteristic makes the inverter possible to operate in high switching frequency. Moreover, it can operate in both standalone and grid-connected systems. The full-bridge switches of the inverter operate with same frequency of the output voltage thus no switching losses in the full-bridge switches. However, it uses three inductors to operate in resonance. The value for these inductors must be properly selected in order for the inverter to operate in desired output frequency. Furthermore, the topology uses resonance inductor L_o which is huge in value and size. Figure 2.18 shows the topology of the inverter.

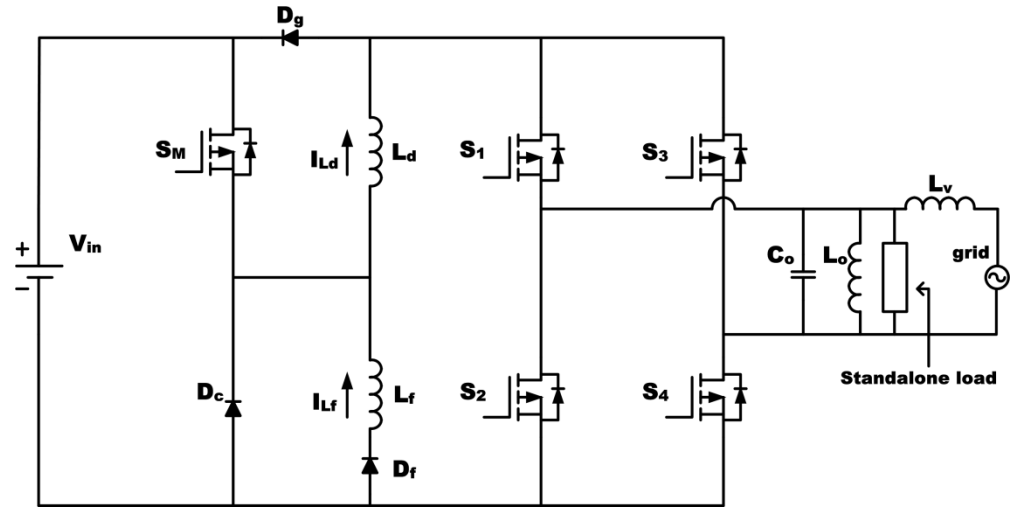


Figure 2.18: High efficiency inverter for standalone and grid-connected systems

2.5.7 A single phase soft switching unipolar PWM inverter

Authors in [37] proposed a single phase soft switching unipolar PWM inverter. In this inverter, four switches are use to form a full-bridge configuration. Two auxiliary switches are added to form ZVS-PWM commutation cell. It has efficiency of 3.4% higher than the hard switching unipolar PWM with equal operating frequency. It operates in ZVS during turn on and ZCS during turn off. It provides the ZVS to all main switches of the full-bridge that operate with high switching unipolar PWM technique. The two auxiliary switches operate at ZCS turn off. In order to achieve low switching losses, switches S_3 and S_4 are commutate at output frequency hence low switching losses occur. Switches S_1 and S_2 are commutate at high switching frequency with SPWM switching technique. Figure 2.19 shows the topology of the single phase soft switching unipolar PWM inverter. Unfortunately, this topology uses two switches that float between DC link and ground thus makes the gate drive circuit difficult to be implemented.

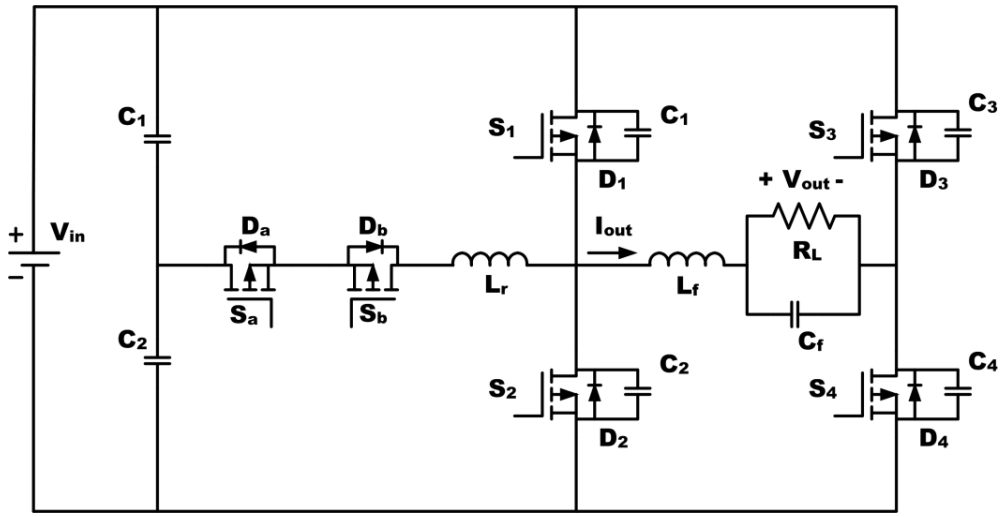


Figure 2.19: Single phase soft switching unipolar PWM inverter

2.5.8 A single phase five-level inverter with coupled inductors

Multilevel topology is very popular in medium and high power applications. This is because multilevel topology has reduced the voltage and current stress problem. In addition, multilevel topology normally operates with low switching frequency which is consequently reducing the switching losses of the system. Nevertheless, multilevel inverter now is having interest and attention by researcher in low power application due to its advantages.

Authors in [38] proposed a single phase five-level inverter with coupled inductors where this topology uses a coupled inductors and the common three arm power module (a,b and c). The inverter only needs one DC source to operate and six power switches with equal voltage rating. Figure 2.20 shows the topology of the single phase five-level inverter with coupled inductors.

The topology is able to generate five voltage levels at its output terminals. Switches S_1 and S_2 are switched at low output frequency while switches S_3 to S_6 are switched with PWM. This mean that the switching losses only occur in switches S_3

to S_6 while switches S_1 and S_2 will have no switching losses. Moreover, this topology requires lower switching frequency in order to get a good quality output. However, the switching scheme of the inverter is complex thus giving a slight difficulty in practical implementation.

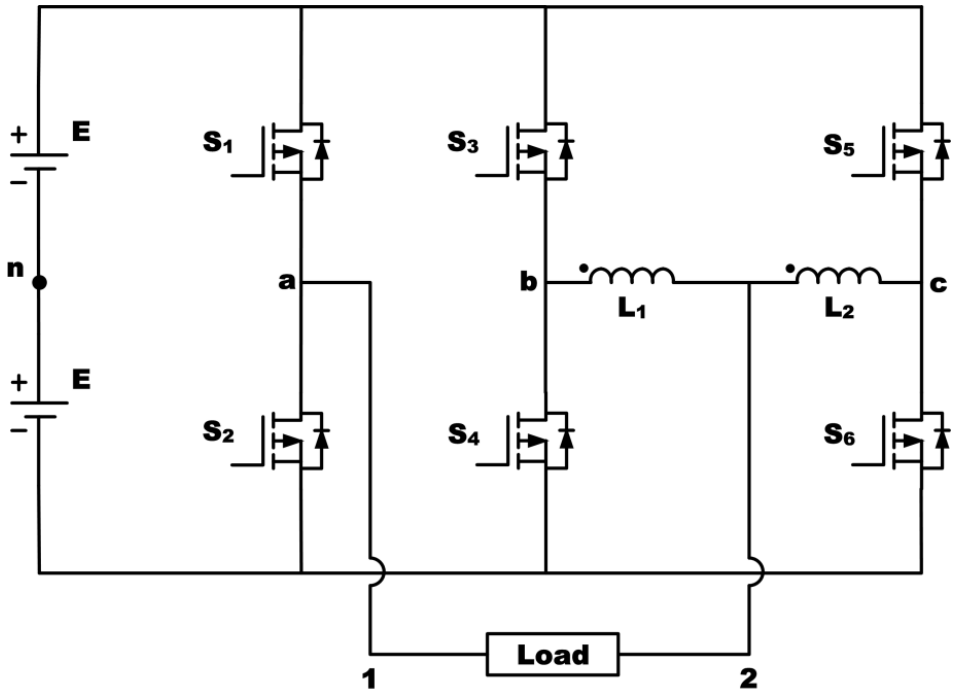


Figure 2.20: Single phase five-level inverter with coupled inductors

2.6 Comparison between the discussed topologies

Review on various inverter topology in literature show that a lot of effort had been made in order to design inverter with better performance and capabilities. Table 2.1 shows a brief summary between the discussed topologies with the key features listed.

Table 2.1: Comparison of various topologies

Topology/ Technique	Switching losses	Switching scheme complexity	Gate drive complexity	No. of switches used	Topology complexity
HPWM	Low	Simple	Simple	4	Simple
Random switching HPWM	Low	Complex	Simple	4	Simple
ZVS-HPWM	Lower	Complex	Complex	5	Complex
Sine wave inverter with PWM DC link	Low	Simple	Complex	5	Simple
ZVS-PWM inverter using a voltage clamp ZVS boost DC link	Lower	Complex	Complex	6	Complex
High efficiency inverter for standalone and grid-connected systems	lower	Simple	Complex	5	Complex
Single phase soft switching unipolar PWM inverter	Lower	Complex	Complex	6	Complex
Single phase five-level inverter with coupled inductors	Lower	Complex	Complex	6	Simple

CHAPTER 3

METHODOLOGY

3.1 Introduction

This chapter presents a novel single phase inverter topology with sinusoidal output voltage and current. The proposed topology is realized by adding auxiliary circuit to the conventional full-bridge inverter. The auxiliary circuit consists of one switch that is connected to the lower arm of the full-bridge. In the proposed novel topology, only switch which is connected to the lower arm of full-bridge is operated at high switching with SPWM and remaining four switches of full-bridge inverter is operated at output frequency (50Hz).

Next, a review on random switching HPWM inverter is included in order to give a comparison between the proposed novel inverter and the random switching HPWM inverter. Random switching HPWM inverter operate with only two switches commutate at a time at high switching frequency while the other two switches with low switching frequency.

3.2 Proposed novel single phase DC-AC inverter

This section describes a novel single phase DC-AC inverter. The discussion covers on the topology description. Next, the operating principle of the inverter is describes. Later, analysis of the circuit is explained step by step.

3.2.1 Topology description

Figure 3.1 shows the circuit diagram of the proposed single phase full-bridge dc-ac inverter. The proposed system consist of an input dc source V_{in}, input capacitor

C_i, full-bridge inverter and auxiliary control circuit connected at the lower arm of the inverter. Basic full-bridge inverter consists of four switches (S_1-S_4), whereas auxiliary control circuit consists of a diode D, holding capacitor C_H, current limiting inductor L_C, control switch S_C and snubber capacitor C_S. The snubber capacitor C_S is the parasitic capacitance exists in switch S_C. A resistor R_L and inductor L_L are connected between leg A and leg B representing the output load of the inverter.

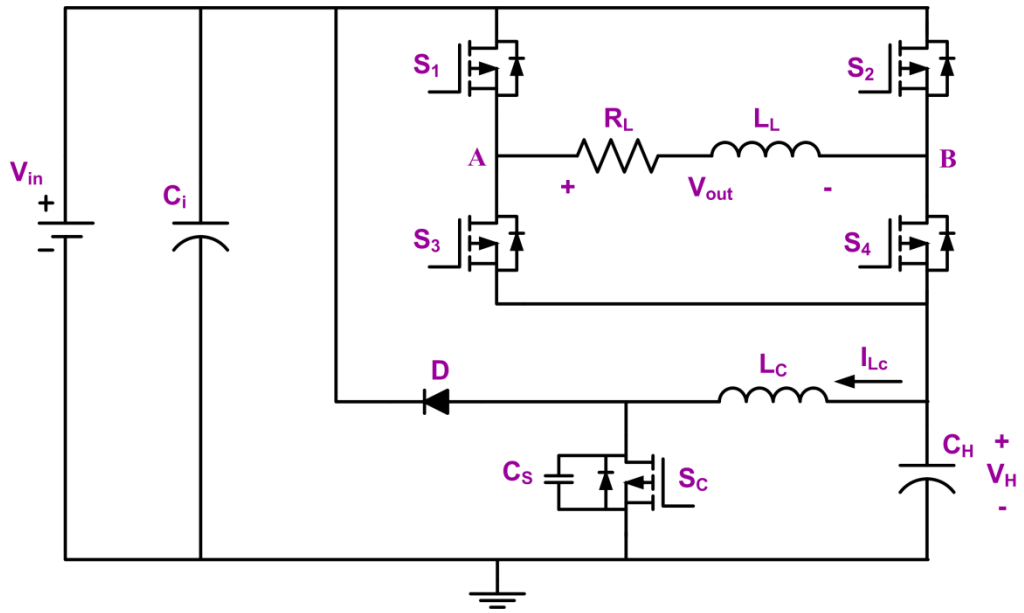


Figure 3.1: Circuit diagram of the proposed novel single phase DC-AC inverter

3.2.2 Principle of operation

The key steady state waveforms of the circuit are shown in Figure 3.2. The power switch S_1 and S_4 are turned on during positive half cycle of the output voltage while S_2 and S_3 are turned on during negative half cycle of output voltage. Meanwhile, control switch S_C is turned on and turned off in high switching frequency along the operation.

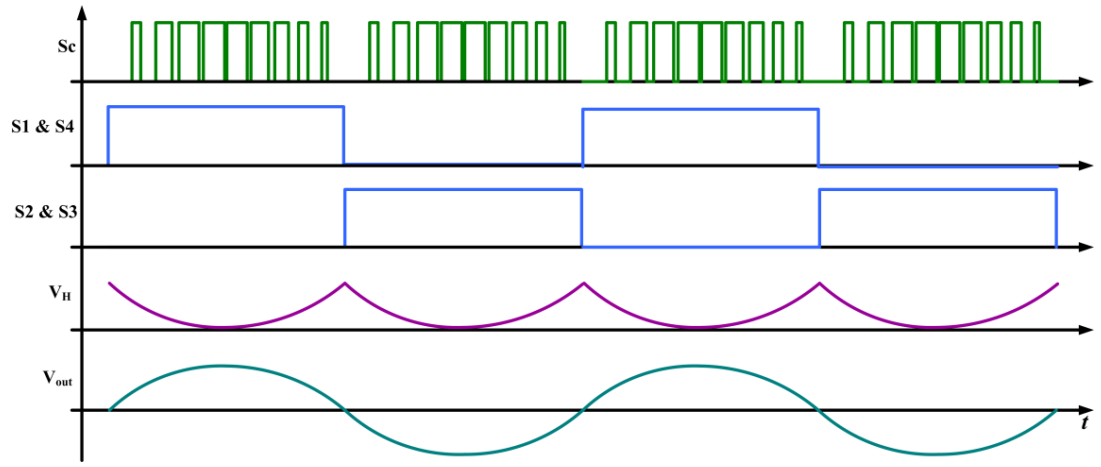


Figure 3.2: Key waveforms of the proposed inverter

In the proposed topology, only control switch S_C which is connected to the lower arm of full-bridge is operated at high switching frequency i.e. SPWM and remaining four switches of full-bridge inverter is operated at output frequency (50Hz). The switch S_C controls the output of full-bridge inverter by increasing or reducing the voltage level at the lower arm of the bridge. Switch S_C is controlled by a high frequency SPWM switching signal. While the power switches of full-bridge inverter operate with square wave switching signal at a frequency of 50 Hz.

3.2.3 Analysis of the circuit

To simplify the analysis of proposed DC-AC inverter, it is assumed that all the components used in the inverter are ideal. The operation of the inverter can be analyzed by studying its modes of operation. As can be seen from Figure 3.3, there are four modes of operation in one output cycle. Mode I and mode II occurs during the first half cycle [0 – π] while mode III and mode IV occurs during the second half cycle [π – 2π]. Basically, mode I and mode II are symmetrical with mode III and mode IV, however they are inverted to each other. These modes are described as:

Operation during positive half cycle

Mode I: When switches S_1 and S_4 are turned on during 0 – π, the input voltage V_{in} is connected directly to the load at point A to B and makes the current flow from A to B. Now, as the switch S_C is turned on instantly, the inductor L_C directly connected to the ground. Hence, current starts flowing through inductor L_C and due to this energy is stored in inductor L_C. The equivalent voltages during this mode can be described as follows:

$$-V_{in} + V_{out} + V_{Lc} = 0 \tag{3.1}$$

$$L_C \frac{di}{dt} = V_{in} - V_{out} \tag{3.2}$$

and

$$-V_{Lc} + V_H = 0 \tag{3.3}$$

$$V_H = L_C \frac{di}{dt} \tag{3.4}$$

Therefore

$$V_{out} = V_{in} - V_H \tag{3.5}$$

Mode II: During this mode, switches S_1 and S_4 remain on, but switch S_C is instantly turned off. As this happen, the current stop flowing through switch S_C. Due to this, inductor L_C starts releasing its stored energy. The equivalent voltage during this mode can be described as follows:

$$V_{out} - V_{Lc} = 0 \tag{3.6}$$

$$L_C \frac{di}{dt} = V_{out} \tag{3.7}$$

and

$$-V_{in} + V_{out} + V_H = 0 \tag{3.8}$$

$$V_{out} = V_{in} - V_H \tag{3.9}$$

Operation during negative half cycle

Mode III: During the time interval π - 2π, switches S_2 and S_3 are turn on. Thus, the input voltage V_{in} is now has oppositely connected to the load from point B to A. Thus the current is now flowing from B to A. As the switch S_C is turned on, the inductor L_C directly connected to the ground. Hence, current start flowing through inductor L_C. Due to this, energy is stored in inductor L_C. The equivalent voltages during this mode can be described as follows:

$$-V_{in} - V_{out} + V_{Lc} = 0 \tag{3.10}$$

$$L_C \frac{di}{dt} = V_{in} + V_{out} \tag{3.11}$$

and

$$-V_{Lc} + V_H = 0 \tag{3.12}$$

$$V_H = L_C \frac{di}{dt} \tag{3.13}$$

Therefore

$$V_{out} = -(V_{in} - V_H) \tag{3.14}$$

Mode IV: In this mode of operation, switches S_2 and S_3 remain on, but switch S_C instantly turns off. Thus, the current stop flowing through switch S_C. Due to this, inductor L_C starts releasing its stored energy. The equivalent voltage during this mode can be described as follows:

$$V_{out} + V_{Lc} = 0 \tag{3.15}$$

$$L_C \frac{di}{dt} = -V_{out} \tag{3.16}$$

and

$$-V_{in} - V_{out} + V_H = 0 \tag{3.17}$$

$$V_{out} = -(V_{in} - V_H) \tag{3.18}$$

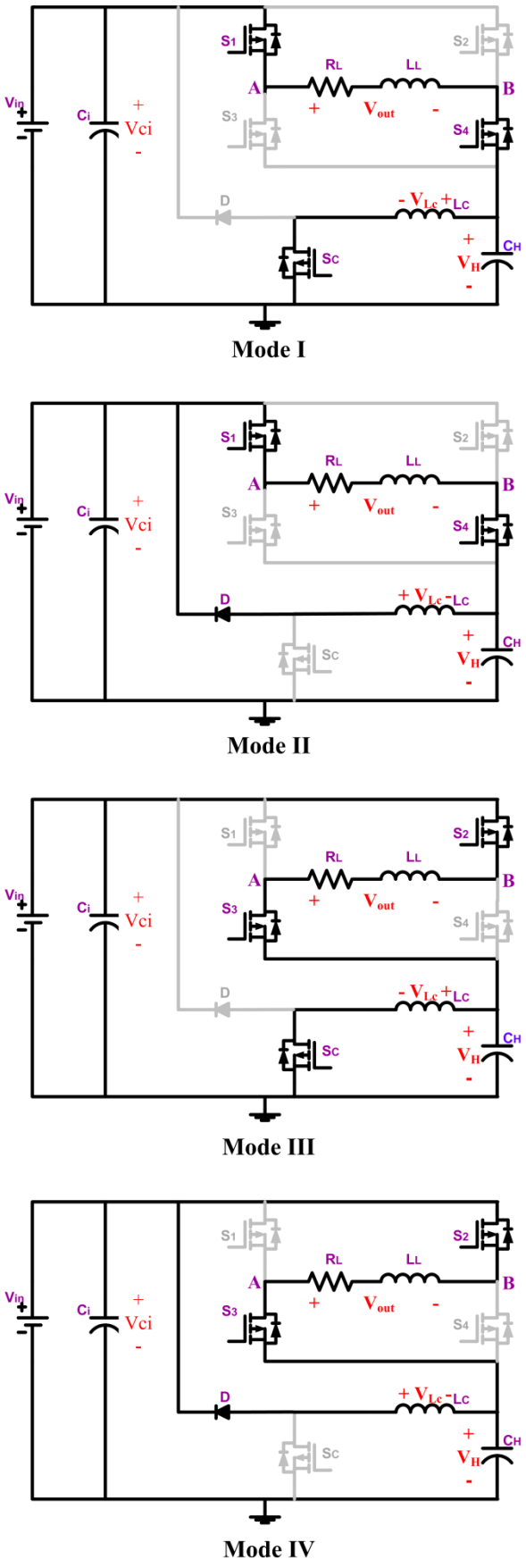


Figure 3.3: The equivalent circuits during various modes of operation

Operation during [0 – π/2] & [π - 3π/2]

During this time interval, the pulse width of switching signal S_C is increasing in sinusoidal way. As this happen, Mode I and Mode III occur longer than Mode II and Mode IV. As a result, energy stored in capacitor C_H starts flowing out and voltage V_H is decreasing in sinusoidal way. This results an increase of voltage across the load V_{out}.

Operation during [π/2 - π] & [3π/2 - 2π]

During this time interval, the pulse width of switching signal S_C is decreasing in sinusoidal way. As this happen, Mode II and Mode IV occur longer than Mode I and Mode III. Hence, energy starts increasingly flowing in into capacitor C_H and voltage V_H is increasing in sinusoidal way. This results a decrease of voltage across the load V_{out}.

3.2.4 Control signal generation circuit

A control signal generation circuit which is used to generate desired signal for the proposed inverter is shown in Figure 3.4. A rectified sinusoidal waveform at output frequency (50 Hz) is compared with a high frequency sawtooth waveform using a comparator. The former is called as reference voltage signal and later is referred as carrier voltage signal. The resulting signal is a SPWM waveform as shown in Figure 3.2. This signal is used to drive the control switch S_C. This generated signal is similar to the classical unipolar PWM switching signal. Since the modulation is symmetric, the reference signal is sampled by the carrier signal once every carrier cycle. Intersection between the sampled reference signal and the carrier signal defines the switching instant of the SPWM pulses. The gating signals for the switches S_1-S_4 are obtained by using a zero crossing detection circuit.

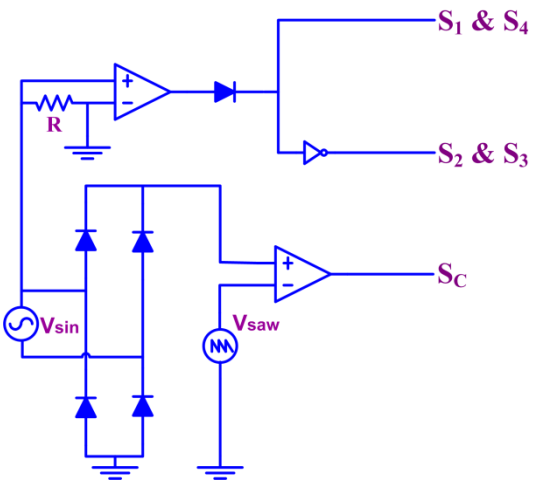


Figure 3.4: Circuit diagram of control signal generation

3.2.5 Overall system analysis

The proposed inverter topology is realized by placing an auxiliary control circuit at the lower arm of the inverter's bridge. The operating principle of auxiliary control circuit is basically operates as voltage reference level at the lower arm of the full-bridge where the effective input voltage across the inverter is the difference between the dc supply voltage V_{in} and voltage drop across the holding capacitor V_H. Meanwhile, the full-bridge switches are operate with low switching frequency square wave so that AC current is achieved by controlling the current flow from A to B and B to A. Figure 3.5 shows the circuit diagram of the overall system of the proposed inverter.

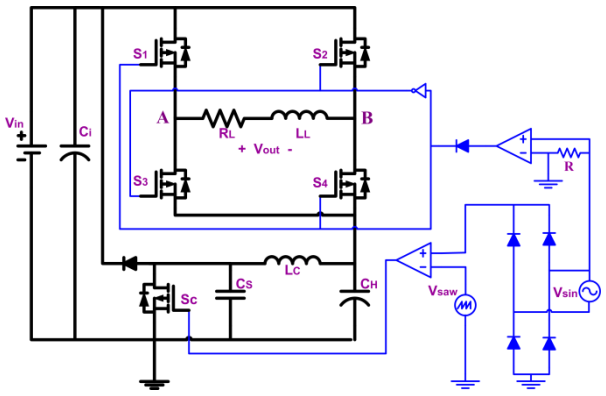


Figure 3.5: Circuit diagram of overall system of the proposed single phase DC-AC inverter

The capacitor C_H continuously charges and discharges during the operation of the control switch S_C by turning it on and off. This operation causes voltage V_H rise and fall due to control sequence of switch S_C. The discharging rate of the capacitor C_H and voltage drop across the holding capacitor V_H is controlled by pulse width of switching signal of the switch S_C. Therefore, the pulse width is properly selected to SPWM so that the voltage V_H can be increased or reduced in sinusoidal way. As a result, output voltage V_{out} also increased and reduced in sinusoidal way. Since the output voltage V_{out} can be varied accordingly by reducing or increasing the voltage V_H, thus the magnitude of the output voltage V_{out} can be controlled by manipulating the modulation index m_a of SPWM pulses of switch S_C.

Figure 3.6 shows the changing of pulse width in SPWM switching signal with respect to amplitude of voltage V_H and output voltage, V_{out}. From Figure 3.6, it shows that as the pulse width increases the amplitude of voltage V_H decreases while output voltage V_{out} increases and when the pulse width decreases, the amplitude of voltage V_H increases while output voltage V_{out} decreases.

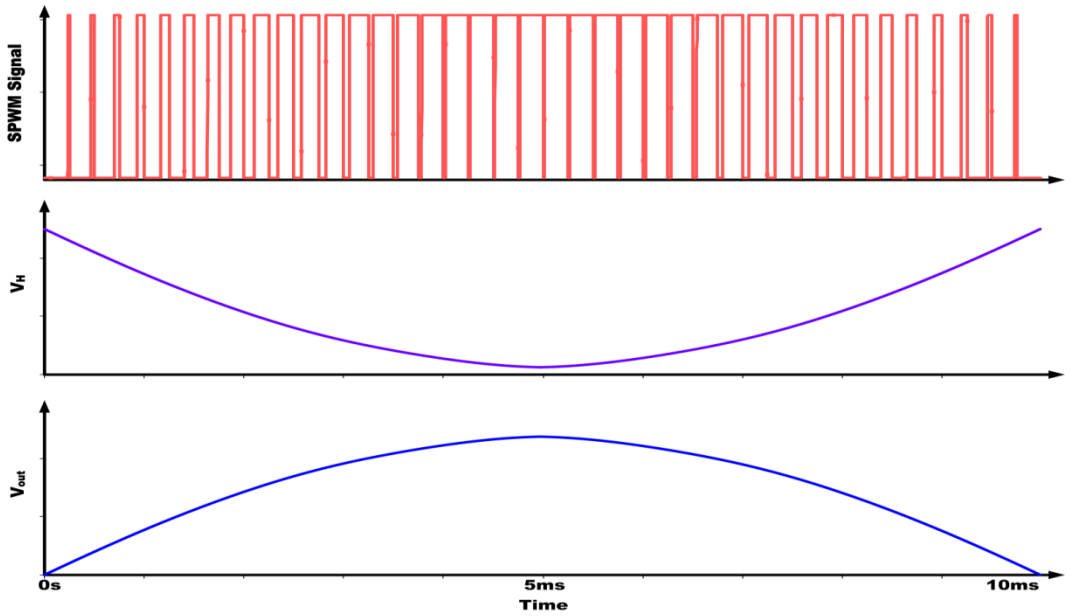


Figure 3.6: SPWM signal with respect to holding voltage, V_H and output voltage, V_{out}

3.3 Development of microcontroller-based inverter with random switching HPWM technique

As explained previously, this technique was first proposed by authors in [31]. In this section, the realization of random switching HPWM using microcontroller-based inverter is presented. The random switching HPWM inverter is explained in more detail in term of topology description as well as operating principle of the topology. The aim is to compare the results of the two techniques (proposed DC-AC inverter and random switching HPWM inverter).

3.3.1 Topology description and principle of operation

The block diagram of the inverter is shown in Figure 3.7. DC source is connected to the input of the inverter and a voltage sensor is connected between the DC source and the inverter. The sensing voltage is then read and processed by a microcontroller. Afterward, the microcontroller produces four switching signal for each switch in the full-bridge inverter. Output of the inverter is connected to a LC filter to remove the high frequency characteristic of the output waveform. At the end of the circuit, a load is connected where the filtered output is diverted to the load.

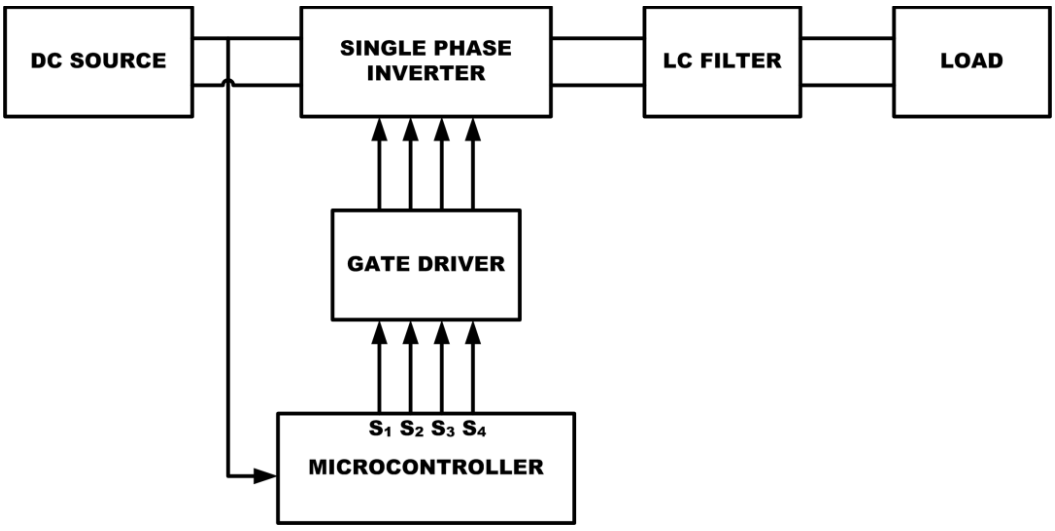


Figure 3.7: Block diagram of the inverter

The circuit diagram of this inverter is based on the conventional single phase full-bridge inverter illustrated in Figure 2.2. The system consists of an input dc source V_{in}, full-bridge switches (S_1-S_4) and LC low past filter.

The key steady state waveforms of the circuit are shown in Figure 3.8. The random switching HPWM method commutates all four switches for both high frequency and low frequency symmetrically. Each switching signals is composed of both high frequency and low frequency. Consequently, the averages switching losses amongst the four switches are equalized.

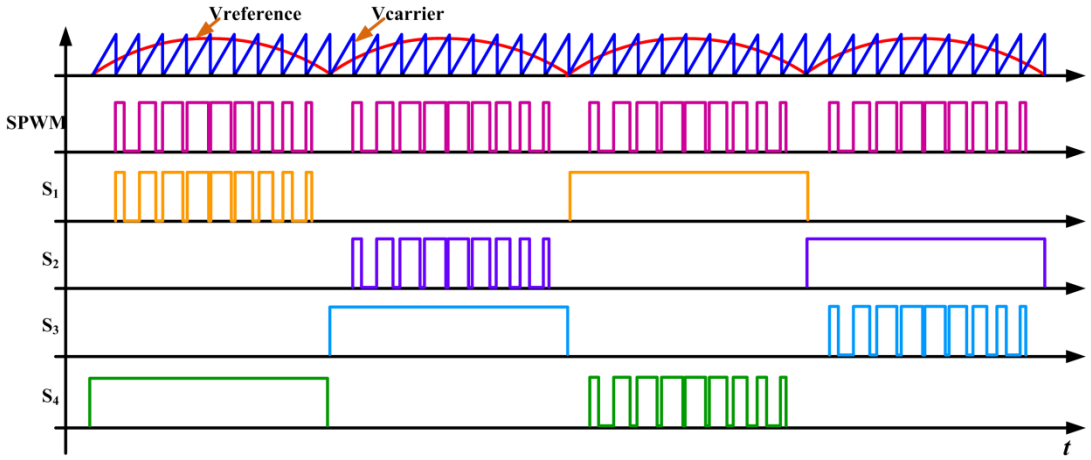


Figure 3.8: Key waveform of the random switching HPWM inverter

Theoretically, the basic principle of generating SPWM is illustrated in Figure 3.9. A rectified sinusoidal waveform at output frequency is compared with a high frequency sawtooth waveform using a comparator.

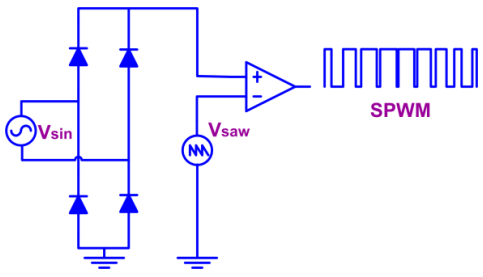


Figure 3.9: The principle of generating SPWM

Generally, the comparator operates by follows the following condition equation where:

$$V_{out} = \begin{cases} HIGH & if \quad V+ > V- \\ LOW & if \quad V+ < V- \\ LOW & if \quad V+ = V- \end{cases} \tag{3.1}$$

The rectified sinusoidal is called as reference voltage signal and the sawtooth is referred as carrier voltage signal. The waveform during the modulation process in generating SPWM waveform is illustrated in Figure 3.8. This generated signal is similar to the classical unipolar PWM switching signal. Since the modulation is symmetrical, the SPWM generated will be a reference to all four switches during commutating in high frequency. The gating signals for the switches S_1-S_4 are interchanging between the high frequency switching to low frequency switching by applying algorithm in the microcontroller. The power switch S_1 and S_4 are turn on during positive half cycle of the output voltage while S_2 and S_3 are turn on during negative half cycle of output voltage.

3.3.2 Analysis of the circuit

In random switching HPWM inverter, any two of the four switches can be commutated at high switching frequency and the other two operated at low frequency for one output cycle. For simplicity in this discussion, S_1 and S_2 are assigned to high frequency switches while S_3 and S_4 are assigned to low frequency switches.

During the course of operation, the random switching HPWM inverter operates as a positive buck converter during the positive half cycle and operates as a negative buck converter during the negative half cycle. During the positive half cycle, S_4 is always turned on thus makes node B is always connected to negative supply and the equivalent circuit is shown in Figure 3.10(b). When S_1 is turned on, node A directly

connected to positive supply and the positive buck converter becomes the circuit in Figure 3.10(c). When S_1 is turned off, the power supply is disconnected from the circuit and the equivalent circuit becomes as shown in Figure 3.10(d).

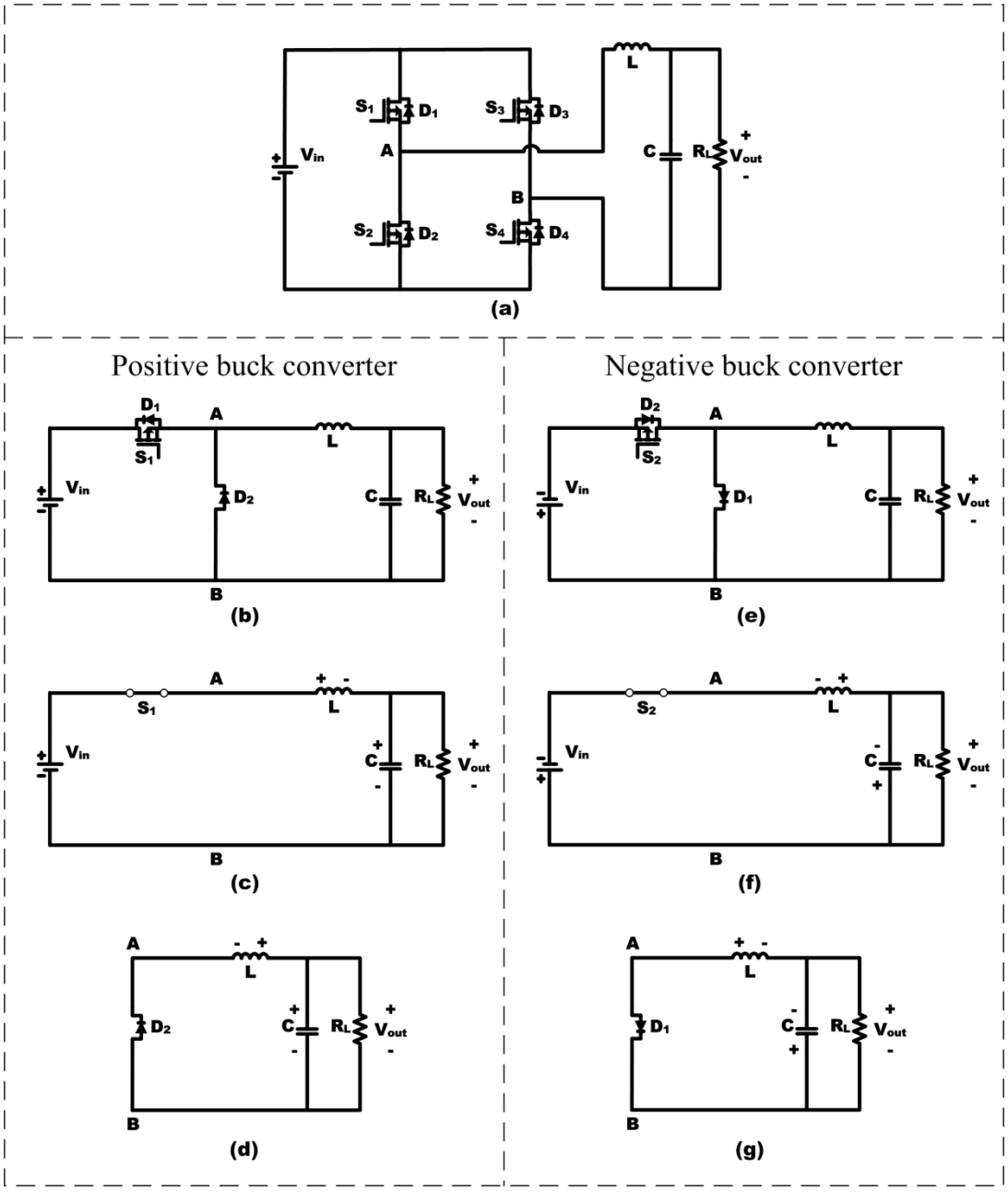


Figure 3.10: The equivalent circuits of random switching HPWM inverter. (a) Conventional full-bridge inverter: (b) - (d) Positive buck converter, and (e) - (g) Negative buck converter

During the negative half cycle, S_3 is always turned on, hence makes node A is always connected to negative supply and the equivalent circuit is shown in Figure

3.10(e). During switch S_2 is turned on, node B is connected to positive supply and the negative buck converter becomes the circuit in Figure 3.10(f). When S_2 is turned off, the power supply is disconnected from the circuit and the negative buck converter becomes the circuit in Figure 3.10(g). Since for the next cycle of the switching signal is switch between the high frequency and low frequency, the operating principle is still remain same.

From the analysis of the circuit, the illustrated currents of each switch of the inverter are shown in Figure 3.11. Each current of the switch are switched at the carrier frequency during the switch commutated at high switching frequency.

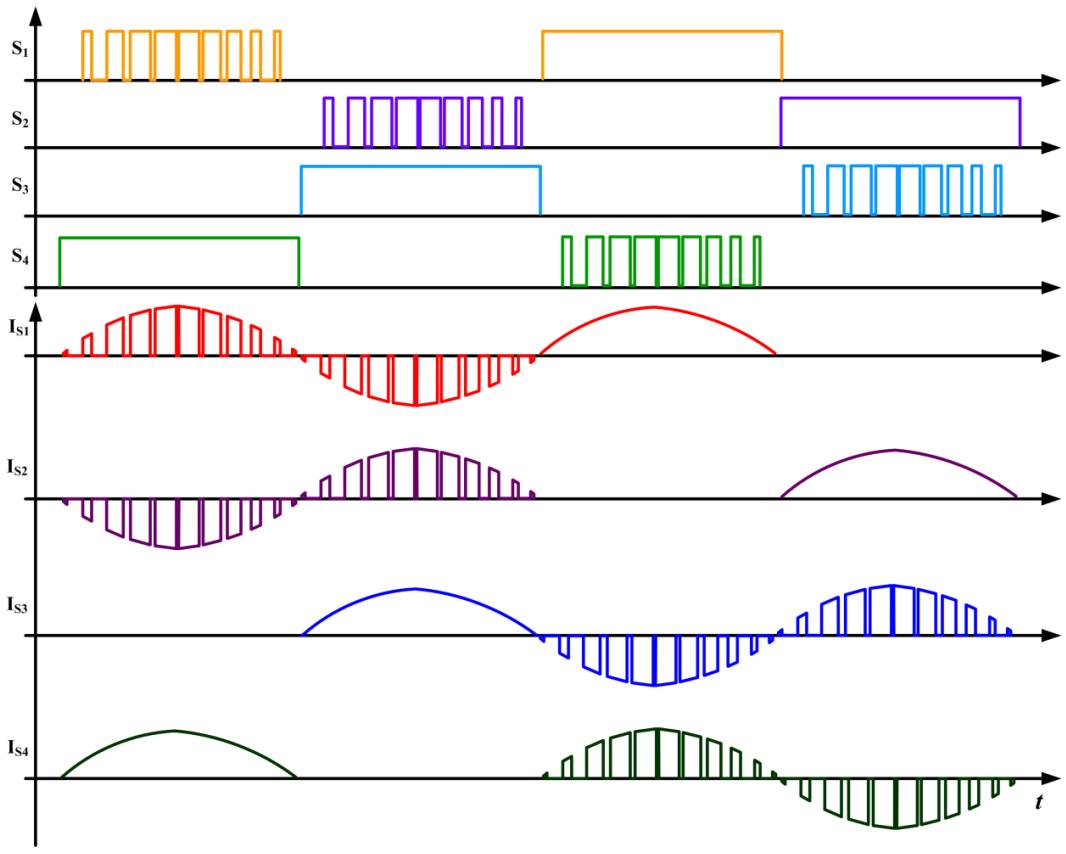


Figure 3.11: Current waveforms of switches

Since the circuit is operated just like buck converter, the freewheeling diode of the switch enable the reverse current flowing through the switch while the inductor is

discharging. When the switch is commutated at low switching frequency, the current flowing through it is also switched at low frequency because of the discharging current from the inductor is still flowing during the DC source cut off interval.

3.3.3 Realization of random switching HPWM technique using microcontroller

In order to generate the random switching HPWM technique, a PIC microcontroller is used. The algorithm of the PIC microcontroller program is described in Figure 3.12. The algorithm flow chart shown in Figure 3.12 gives a representation of a program code created in APPENDIX A. The program code is created by using a PicBasic Pro programming language and compiled in MicroCode Studio.

The algorithm developed in the main program operates by sensing the voltage, V_{sense} from the input of the inverter. The microcontroller obtains the required voltage information from a voltage divider in hardware section and process the voltage information through its built in analog to digital converter (ADC). The built in ADC is able to read the voltage value from 0V to 5V, where the maximum of 5V is equal to 255. X value represent the variable number sensed and stored where the number of the elements range from 0 to 255.

The HPWM lookup tables were calculated and built first before the program is made. The tables contain a sequence of pulse width values of the HPWM and stored in the program subroutine. The HPWM waveforms consist of three different modulation index, m_a values. Once the HPWM finished executed, the program will start over again sensing the voltage V_{sense}. Since the HPWM program take two output cycles to finish execute, the response for the system looping will take approximately about 0.04 seconds.

The lookup tables are based on comparison of two waveforms created in MATLAB. Mathematical functions and formulas are computed in the MATLAB where they represent sinusoidal waveform and sawtooth waveform. Both sinusoidal function and sawtooth function are computed by follow the rules of Equation 3.1. The MATLAB program that generates the lookup tables is shown in APPENDIX B.

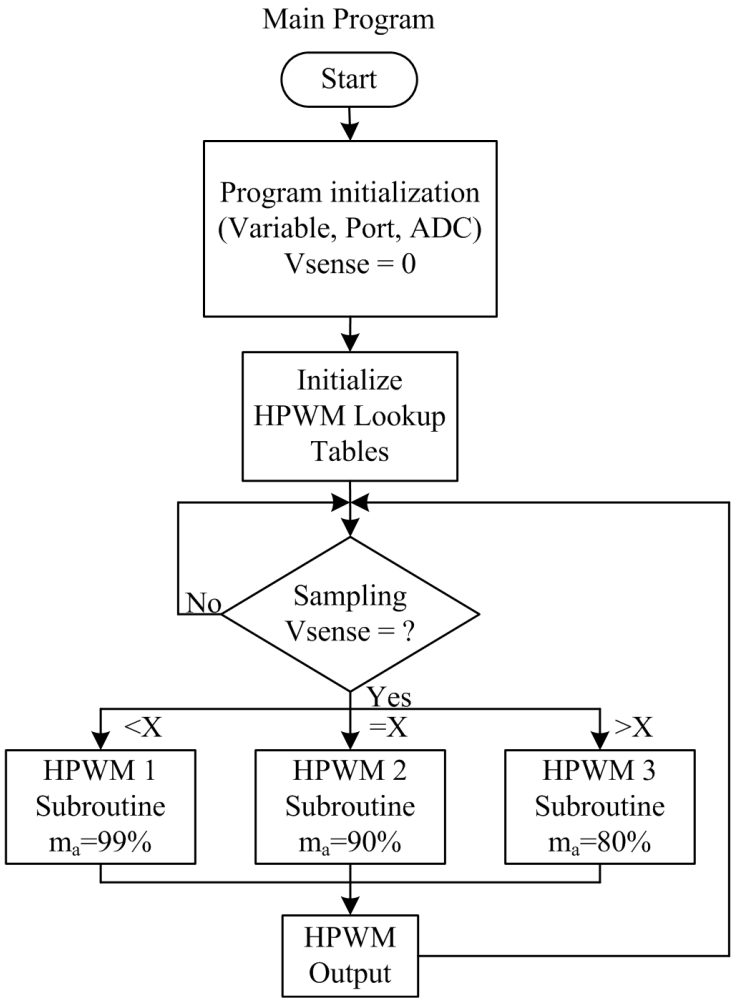


Figure 3.12: Algorithm for the proposed random switching HPWM Inverter

CHAPTER 4

DESIGN AND IMPLEMENTATION

4.1 Introduction

This chapter presents the details of design and implementation process of the proposed inverter systems. This chapter is divided based on two major topic of the proposed design which are novel single phase DC-AC inverter and the random switching HPWM inverter with microcontroller implementation. The discussions covers on design of inverter system, control signal generator, and gate drive circuit.

4.2 Design and implementation of a novel single phase DC-AC inverter

This section describes the design and implementation of the novel single phase inverter. The discussion covers the design of proposed inverter system, design of control signal generator circuit, design of gate drive circuit and implementation of overall system.

4.2.1 Design of inverter system

The first step in designing the inverter system is to determine the maximum voltage and current stress across power switches and other circuit components. This is the important step in order to select proper power switches and component to be used in experiment.

To obtain the maximum voltage and current stress across the power switches and circuit components, the input voltage V_{in} is set to maximum value and it is assume that maximum output power is equal to maximum input power $P_{in} = P_{out}$.

Therefore, voltage stress at each switches of full-bridge is

$$V_{S1} = V_{S2} = V_{S3} = V_{S4} = V_{in} \tag{4.1}$$

For switch S_C, the voltage stress is

$$V_{Sc} = V_{in} - V_{diode} \tag{4.2}$$

where $V_{diode} = 0.7\,V$, therefore

$$V_{Sc} = V_{in} - 0.7 \tag{4.3}$$

$$V_{Sc} \approx V_{in} \tag{4.4}$$

For circuit's capacitors, the voltage stresses are:

$$V_{Ci} = V_{in} \tag{4.5}$$

$$V_{CH} = V_{H\,max} = V_{in} \tag{4.6}$$

For diode D, the voltage stress is:

$$V_D = V_{in} \tag{4.7}$$

In order to find current stress of each component in the circuit, it is assume that the efficiency of the system is equal to 100 % and modulation index m_a equal to 1. Therefore

$$P_{in} = P_{out} = V_{out\ rms} . I_{out\ rms} \tag{4.8}$$

and peak output voltage

$$V_p = \sqrt{2} V_{out\ rms} = V_{in} \tag{4.9}$$

where

$$I_{out\ rms} = \frac{P_{out}}{V_{out\ rms}} \tag{4.10}$$

and peak current is

$$I_p = \sqrt{2} I_{out\ rms} \tag{4.11}$$

$$I_p = \sqrt{2} \frac{P_{out}}{V_{out\ rms}} \tag{4.12}$$

$$I_p = \frac{2P_{out}}{V_{in}} \tag{4.13}$$

Since same current is flowing through all switches, inductor L_C, and diode D, therefore, the maximum current stress of this component can be equated as:

$$I_{switch} = I_{Lc} = I_D = I_p = \frac{2P_{out}}{V_{in}} \tag{4.14}$$

Table 4.1 summarizes the equation of the voltage and current stress across the power switches and other circuit components of the proposed inverter. Since every component in the inverter are having maximum voltage rating equal to maximum input voltage, therefore each component can easily be selected by choosing a proper component with voltage rating slightly higher than maximum input voltage.

Table 4.1: Equation of maximum voltage and current stress across power switches and circuit components of the proposed inverter

Component	Maximum voltage stress	Maximum current stress
Power switches, S_1-S_4	V_{in}	$\frac{2P_{out}}{V_{in}}$
Power switches, S_C	V_{in}	$\frac{2P_{out}}{V_{in}}$
Input capacitor, C_i	V_{in}	-
Holding capacitor, C_H	V_{in}	-
Filter inductor, L_C	-	$\frac{2P_{out}}{V_{in}}$
Diode, D	V_{in}	$\frac{2P_{out}}{V_{in}}$

By solving equation in Table 4.1, the maximum voltage and current stress across the power switches and circuit components can be obtained. Table 4.2 shows the calculated value of maximum voltage and current stress across the power switches and circuit components of the proposed inverter. The input voltage for the experimental prototype is set at 100 V and output power of 100 W. With these values, the power switches and other components can be selected properly.

In this experiment, the power switches selected are SPW47N60C3 which is Cool MOS power transistor produced by Infineon Technologies. This switch has maximum drain to source voltage of 650 V and maximum forward current of 47 A. The design of inductor L_C is similar to the design of filter in random switching HPWM inverter and discussed in that section. The optimum values of inductor L_C and capacitor C_H are determined by repetition of computer simulation. During the simulation, range of value are selected and tested where the value for inductor L_C is selected from (0.1 mH – 5 mH) and capacitor C_H is selected from (1 µF - 10µF). It was found out that the proposed topology are able to operate with optimize

performance with inductor L_C equal to (1 mH – 4 mH) and capacitor C_H is equal to 4.7 µF.

Table 4.2: Maximum voltage and current stress across power switches and circuit components of the proposed inverter

Component	Maximum voltage stress, V	Maximum current stress, A
Power switches, S_1-S_4	100	2
Power switches, S_C	100	2
Input capacitor, C_i	100	-
Holding capacitor, C_H	100	-
Filter inductor, L_C	-	2
Diode, D	100	2

Given V_{in} = 100 V and P_{out} = 100 W

4.2.2 Design of control signal generator

Figure 4.1 shows the block diagram of signal generator circuit for the proposed inverter and Figure 4.2 shows the complete signal generator circuit. The circuit consists of combination of several operational amplifiers (op amp). The circuit is divided into several parts which are phase-shift oscillator, voltage follower, non-inverting and inverting amplifier, zero voltage comparator, sawtooth oscillator and signal comparator. Each of these parts is elaborate in the next succeeding paragraph.

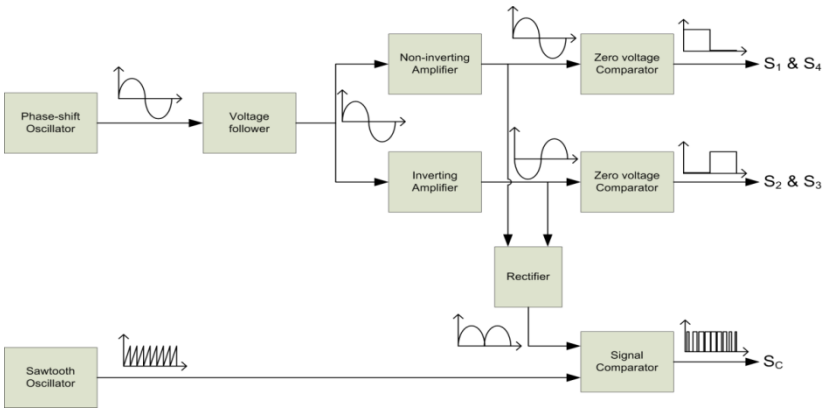


Figure 4.1: Functional block diagram of signal generator circuit for the proposed inverter

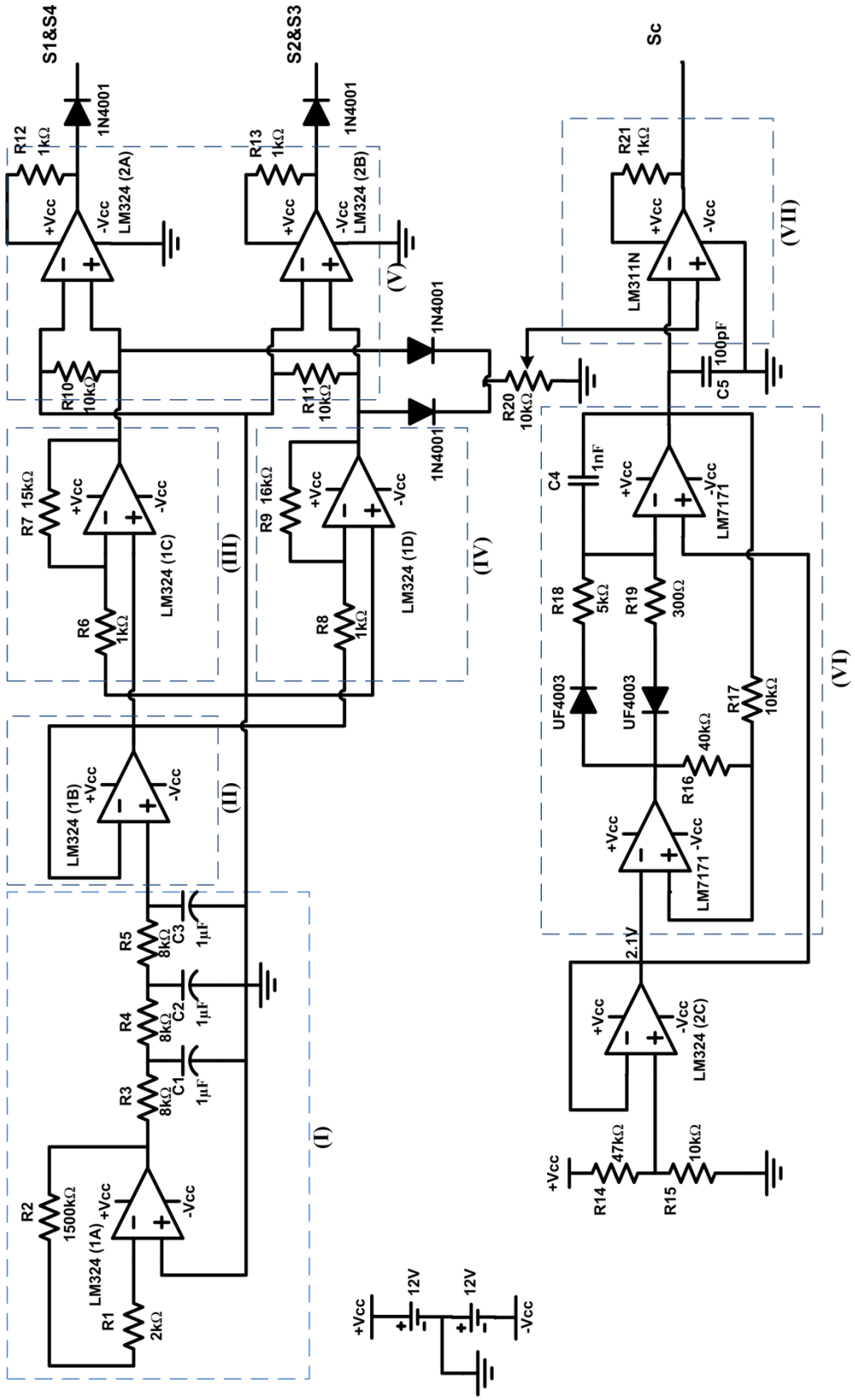


Figure 4.2: Signal generation circuit for proposed inverter: (I) Phase-shift oscillator, (II) Voltage follower, (III) Non-inverting amplifier, (IV) Inverting amplifier, (V) Zero voltage comparator, (VI) Sawtooth oscillator, and (VII) Comparator

A phase-shift oscillator is a linear oscillator circuit that produces a sine wave output. The phase-shift oscillator has less distortion and has good frequency stability. A phase-shift oscillator can be built with one op amp shown in Figure 4.1(I). Three RC sections are cascaded to get the steep slope, dϕ/dω, required for a stable oscillation frequency. The RC sections form a filter that shifts the input by 180 degrees at the oscillation frequency. The related equation for this oscillator is:

$$\omega = 2\pi f = \frac{1.732}{RC} \tag{4.15}$$

Where, tan 60º = 1.732 and 60 degrees is the phase shift of each section of the waveform and R= R3, R4 & R5 and C= C1, C2 & C3.

Voltage follower shown in Figure 4.1(II) is used as a buffer amplifier to eliminate loading effect. Non-inverting amplifier in Figure 4.1(III) is used to amplify the voltage by varying the amplifier gain. For non-inverting amplifier the related equation is:

$$V_{out} = V_{in}(1 + \frac{R7}{R6}) \tag{4.16}$$

Inverting amplifier in Figure 4.1(IV) also amplifies the voltage but it invert the original signal. For inverting amplifier the related equation is:

$$V_{out} = -\frac{R9}{R8}V_{in} \tag{4.17}$$

Two op amps in Figure 4.1(V) are used to convert the sinusoidal waveform into a square wave for S_1, S_4 and S_2, S_3 respectively. These op amps operate as comparators that compare the sinusoidal waveform with zero voltage. The outputs that came out from these op amps are in the form of square waveforms. Diode is connected on each of the op amps output in order to eliminate any negative cycles in the waveform. The benefit of this method is that it automatically gives dead time to each signal generated.

Sawtooth oscillators basically generate a waveform that has resemblance to the teeth of a saw. The convention is that a sawtooth wave ramps upward and then sharply drops. The sawtooth oscillator can be built with two high speed op amps shown in Figure 4.1(VI). A voltage divider and one voltage follower is connected in order to provide 2.1V to the sawtooth oscillator circuit. The voltage 2.1V is needed to lift the minimum level of the sawtooth waveform from negative to zero voltage reference. For the first half cycle, the capacitor charges through R19, and for the other half, it quickly discharges through R18. The slope of the sawtooth can be adjusted by varying R18 and R19 values. The oscillation frequency i.e switching frequency can be calculated by the following formula:

$$f = \frac{1}{2C(R18+R19)}\left(\frac{R16}{R17}\right) \tag{4.18}$$

A comparator in Figure 4.1(VII) is used to compare the sinusoidal and the sawtooth waveform to generate the SPWM signal for S_C. The condition equation is:

$$V_{out} = \begin{cases} High & if \quad V+ > V- \\ Low & if \quad V+ < V- \\ Low & if \quad V+ = V- \end{cases} \tag{4.19}$$

For this topology, the dead time control for switching signal between upper switches (S_1 and S_4) and lower switches (S_2 and S_3) is not implemented. This is because the possibility of upper and lower switches to overlap will not result in short circuit. This is due to the existence of current limiting inductor L_C that prevents the circuit from short circuit during the transition between positive and negative cycles. Therefore, this feature gives additional advantages compared to the conventional full-bridge topology that requires dead time control.

4.2.3 Design of gate drive circuit

A gate driver is a power amplifier that accepts low power input signal from the signal generator and produces high power output signal that can be used for operate an IGBT or power MOSFET. As the power switch requires a particular gate voltage in order to switch on, the gate capacitor must be charged to at least the required gate voltage for the power switch to switch on. Similarly, to switch off the power switch, this charge must be dissipated, i.e. the gate capacitor must be discharged.

The proposed topology of the inverter consists of five switches where each switch have different gate to ground point. The gate drive optocoupler HCPL-3140 has been chosen to be implemented in the proposed system because it provides bootstrappable power supply function and has wide operating voltage range. Furthermore, this optocoupler also provide isolation between the gate drive circuit and signal generator circuit. This gives extra protection to signal generator circuit that is at low voltage level than the main inverter circuit which operates at higher voltage. Figure 4.3 shows the functional diagram of the HCPL-3140.

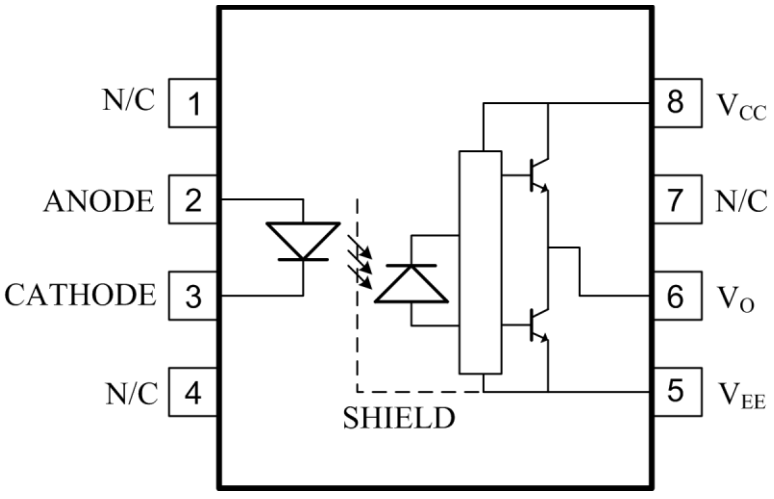


Figure 4.3: Functional diagram of HCPL-3140

For better explanation, Figure 4.4 shows the gate drive circuit for the proposed topology. One optocoupler can only drive one switch and all of them are supplied by a single power supply and connected through a series of diodes. This connection is called a bootstrap. Capacitors are connected from the supply rail of each optocoupler allowing them to store energy to be used to turn on the switch. Capacitors connected to the high side can only charge when the switch that supplied by it is turned off. Bootstrap capacitor selection is important to ensure that the signal reaches the switch's gate terminal do not suffer voltage distortion. The zener diode (with breakdown voltage V_Z) connection is optional where it connected parallel to bootstrap capacitor. This is to ensure that current flow to charge bootstrap capacitor is diverted to the zener diode as soon as voltage at bootstrap capacitor reaches V_Z. The main objective of this is to provide protection to optocoupler.

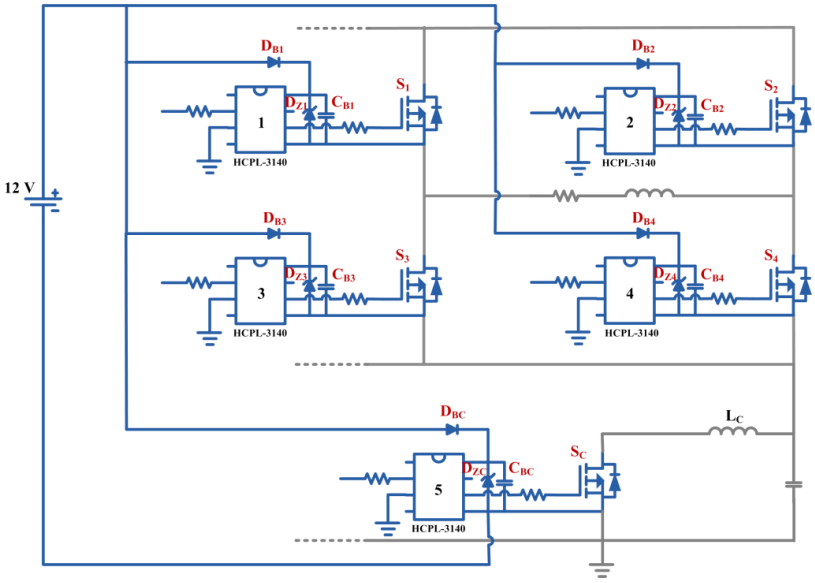


Figure 4.4: Gate drive circuit by using HCPL-3140 of the proposed inverter

Based on gate drive circuit of the proposed inverter shown in Figure 4.3, the bootstrap operation of the gate drive circuit can be discussed as follows:

1. During the first half cycle, switches S_1, S_4 and S_C are turned on while switches S_2 and S_3 are turned off. During this interval, the V_{EE} pin of optocoupler 2 is directly connected to ground through inductor L_C thus forward biased the diode D_{B2} and charging the capacitor C_{B2} with 12 V. Meanwhile, D_{B1} is reverse bias and C_{B1} is supplying voltage to the optocoupler 1 to turn on S_1.
2. In the second half cycle, switches S_2, S_3 and S_C are turned on while switches S_1 and S_4 are turned off. In this interval, the V_{EE} pin of optocoupler 1 is directly connected to ground through inductor L_C thus makes the diode D_{B1} to forward bias and charging the capacitor C_{B1} with 12 V. In the meantime, D_{B2} is reverse bias and C_{B2} is supplying voltage to the optocoupler 2 to turn on S_2.
3. The V_{EE} pin of optocoupler 5 is connected to ground at all times, thus voltage is always supplied to optocoupler 5 to turn on S_C. Meanwhile, capacitor C_{B3} and C_{B4} will charge during S_C is turned on. Since switch S_C is turned on and off rapidly at high speed, so power stored in capacitor C_{B3} and C_{B4} will be enough to turn on S_3 and S_4.

4.2.4 Implementation of overall system

Plate 4.1 shows the photograph of novel single phase DC-AC inverter implemented on the PCB. The three circuits which are proposed inverter, control signal generator and gate drive circuit are implemented on single PCB board. The control signal generator consist of two quad op amps (LM324), two high speed op amps (LM7171) and one comparator (LM311N). The circuit also used 20 resistors, 1 variable resistor, 5 capacitors, 4 diodes (1N4001) and 2 ultra fast recovery diodes (UF4003). For the gate drive circuit, it consists of 5 optocoupler (HCPL-3140), 10 resistors, 5 diodes (1N4001), 5 zener diodes (12 V) and 5 capacitors. Finally, the components for the proposed inverter are 5 power switches (SPW47N60C3), 2

capacitors, 1 inductor and 1 high voltage diode with voltage and current rating higher than calculated in Table 4.2.

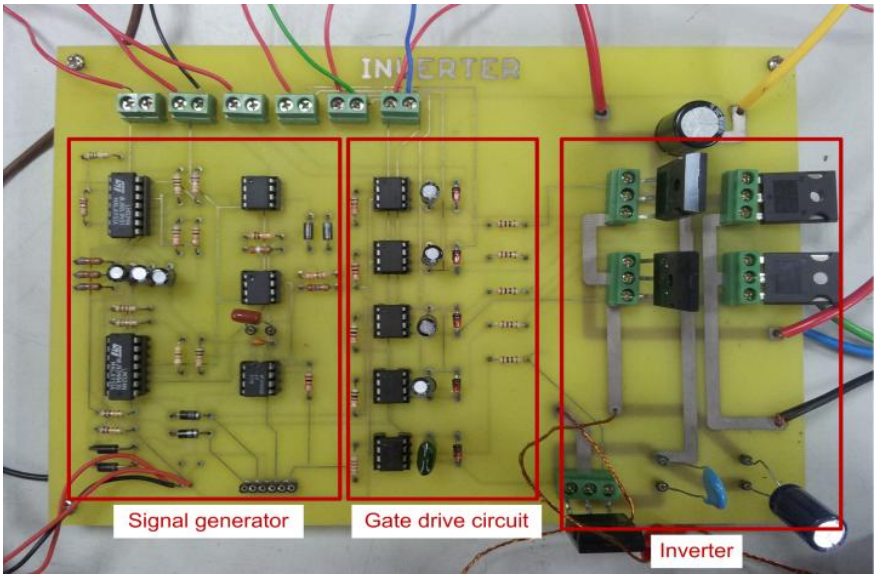


Plate 4.1: The novel single phase DC-AC inverter implemented on the PCB

4.3 Design and implementation of microcontroller-based inverter with random switching HPWM technique

In this section the design and implementation of random switching HPWM inverter based on microcontroller is presented. This section explains the implementation of control signal generator circuit based on microcontroller and the full-bridge inverter. For design of gate drive circuit, the discussion is not included since the method used is similar to the previous method in proposed inverter.

4.3.1 Design of inverter system

Similar to previous design, the first step in designing the inverter system is to determine the maximum voltage and current stress across power switches and other circuit components.

To obtain the maximum voltage and current stress across the power switches and circuit components, the input voltage V_{in} is set to maximum value and it is assume that maximum output power is equal to maximum input power $P_{in} = P_{out}$.

Thus, voltage stress at each switches of full-bridge is

$$V_{S1} = V_{S2} = V_{S3} = V_{S4} = V_{in} \tag{4.20}$$

For circuit's capacitors, the voltage stresses are:

$$V_{Ci} = V_{in} \tag{4.21}$$

$$V_C = V_{in} \tag{4.22}$$

In order to find current stress of each component in the circuit, it is assume that the efficiency of the system is equal to 100 % and modulation index m_a equal to 1. Therefore

$$P_{in} = P_{out} = V_{out\ rms} . I_{out\ rms} \tag{4.23}$$

and peak output voltage

$$V_p = \sqrt{2} V_{out\ rms} = V_{in} \tag{4.24}$$

where

$$I_{out\ rms} = \frac{P_{out}}{V_{out\ rms}} \tag{4.25}$$

and peak current is

$$I_p = \sqrt{2} I_{out\ rms} \tag{4.26}$$

$$I_p = \sqrt{2}\frac{P_{out}}{V_{out\ rms}} \tag{4.27}$$

$$I_p = \frac{2P_{out}}{V_{in}} \tag{4.28}$$

Since same current is flowing through all switches, inductor L_C, and diode D, therefore, the maximum current stress of this component can be equated as:

$$I_{switch} = I_L = I_p = \frac{2P_{out}}{V_{in}} \tag{4.29}$$

Table 4.3 summarizes the equation of the voltage and current stress across the power switches and other circuit components of the proposed inverter.

Table 4.3: Equation of maximum voltage and current stress across power switches and circuit components of the random switching HPWM inverter

Component	Maximum voltage stress	Maximum current stress
Power switches, S_1-S_4	V_{in}	$\frac{2P_{out}}{V_{in}}$
Input capacitor, C_i	V_{in}	-
Filter capacitor, C	V_{in}	-
Filter inductor, L	-	$\frac{2P_{out}}{V_{in}}$

By solving equation in Table 4.3, the maximum voltage and current stress across the power switches and circuit components can be obtained. Table 4.4 shows the calculated value of maximum voltage and current stress across the power switches and circuit components of the random switching HPWM inverter. The input voltage for the experimental prototype is set at 100 V and output power of 100 W. With these values, the power switches and other components can be selected properly. In this experiment, similar power switches were selected which is

SPW47N60C3. This is to ensure that the performance of both inverters can be compared equally.

Table 4.4: Maximum voltage and current stress across power switches and circuit components of the random switching HPWM inverter

Component	Maximum voltage stress, V	Maximum current stress, A
Power switches, S_1-S_4	100	2
Input capacitor, C_i	100	-
Filter capacitor, C	100	-
Filter inductor, L	-	2

Given V_{in} = 100 V and P_{out} = 100 W

4.3.2 Design of LC low pass filter

In order to remove the high frequency characteristic of output waveform of the inverter, a LC low pass filter is design to remove frequencies that are higher than fundamental frequency which is this case 50 Hz. LC filter consists of an inductor L, and a capacitor C.

Design of inductor L is built with a pair of E-cores of ferrite material combined together. The inductor is constructed by winding a copper wire around the inner section of the E-cores. Both E-cores are coupled together and the outer sections of the cores are spaced with air gap on both side. This is to prevent the inductor from saturated during circuit operation. Figure 4.5 shows the design of the inductor L using E-cores.

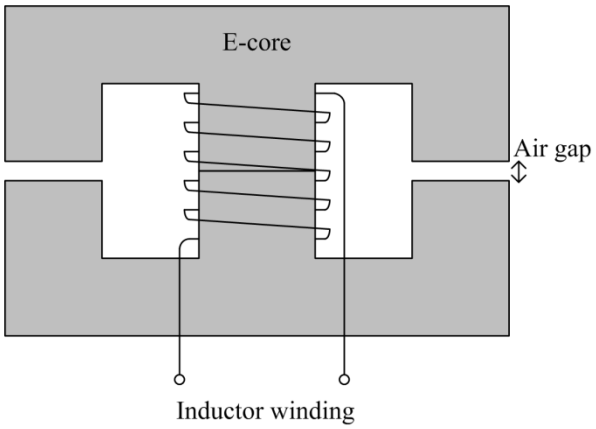


Figure 4.5: Design of inductor L

Plate 4.2 shows the photograph of implemented inductor L constructed with E-core and litz wire. The inductor winding is made by twisting 5 litz wires to increase its current capacity. The outer sections of the cores are spaced with a piece of paper on both sides to provide air gap which is approximately 0.3mm. The inductance value of the inductor L is approximately 1 mH.

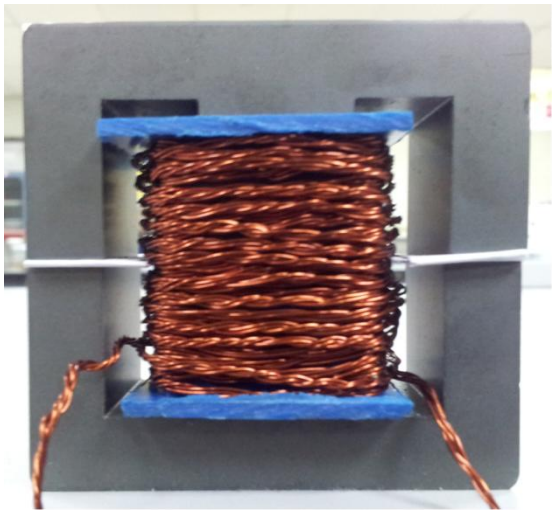


Plate 4.2: Inductor L implemented in experiment

Plate 4.3 shows the photograph of implemented capacitor C. The capacitor C used in the experiment is AC capacitor with capacitance value of approximately 6

µF. In order to get the desired capacitance value, three capacitors with capacitance values of 4.7 µF, 1 µF and 1 µF are connected together in parallel.

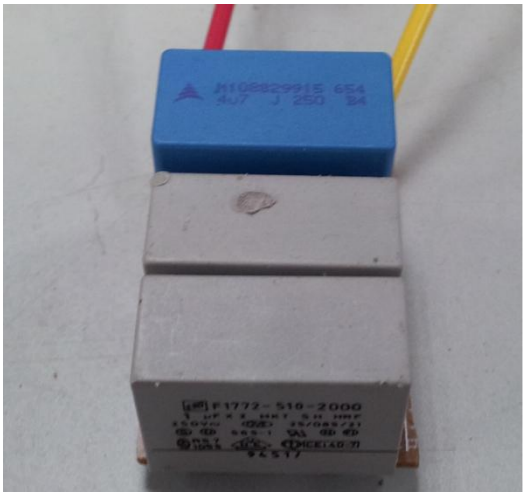


Plate 4.3: Capacitor C implemented in experiment

4.3.3 Design of control signal generator

In order to generate the HPWM technique, a PIC16F877 microcontroller is used. PIC16F877 is considered to be unique as it uses flash memory to work as program memory. Therefore, it can be programmed repeatedly without using ultra-violet to erase its program memory. It is also interesting that PIC16F877 consumes low power supply and voltage which is approximately 5V. It is also fully static or non-volatile where the program memory in PIC16F877 would not be erased and lost when the power supply is switch off from the microcontroller. PIC16F877 has a relatively sufficient memory for storage purposes and industrial applications.

Figure 4.6 shows the pins assignment for PIC16F877 of the random switching HPWM inverter. Generally, PIC16F877 has total of 40 pins where pins 11 & 32 (V_{DD}) are connected to voltage supply 5V while pins 12 & 31 (V_{SS}) are connected to ground. Pin 1 ($\overline{MCLR}$) is an active low reset and connected to 5V supply through a 470Ω resistor R. Pins 13 (OSC1) & 14 (OSC2) are external crystal oscillator pins

and connected to a 20 MHz crystal oscillator (XTAL). The crystal oscillator is grounded through 10 nF capacitor C_1 and C_2. Pi n 2 (RA0) is a bidirectional I/O port assigned as A/D input reference voltage V_{sense}. Pins 37 to 40 (RB4 – RB7) are bidirectional I/O port assigned as switching signal output.

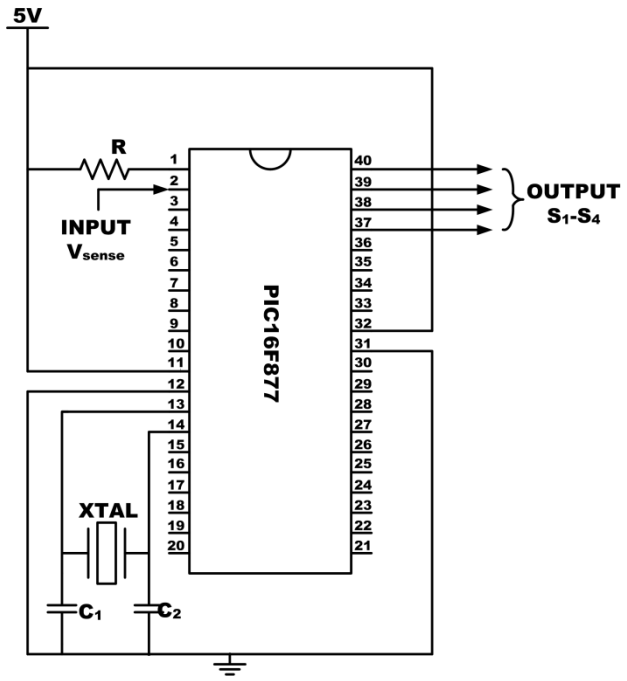


Figure 4.6: The equivalent circuit of signal generator using PIC16F877

4.3.4 Implementation of overall system

Plate 4.4 shows the microcontroller-based random switching HPWM inverter implemented on the PCB. The three circuits which are the full-bridge inverter, control signal generator and gate drive circuit are implemented on single PCB board. The control signal generator consist of one microcontroller (PIC16F877), one 20 MHz crystal oscillator, one resistor and two capacitors. The circuit also used one 5 V voltage regulator (LM7805) and 2 capacitors to be supplied to microcontroller. For the gate drive circuit, it consists of 4 optocoupler (HCPL-3140), 8 resistors, 4 diodes (1N4001), 4 zener diodes (12 V) and 4 capacitors. Finally, the components for the

proposed inverter are 4 power switches (SPW47N60C3), 1 input capacitor, 1 filter inductor and 1 filter capacitor.

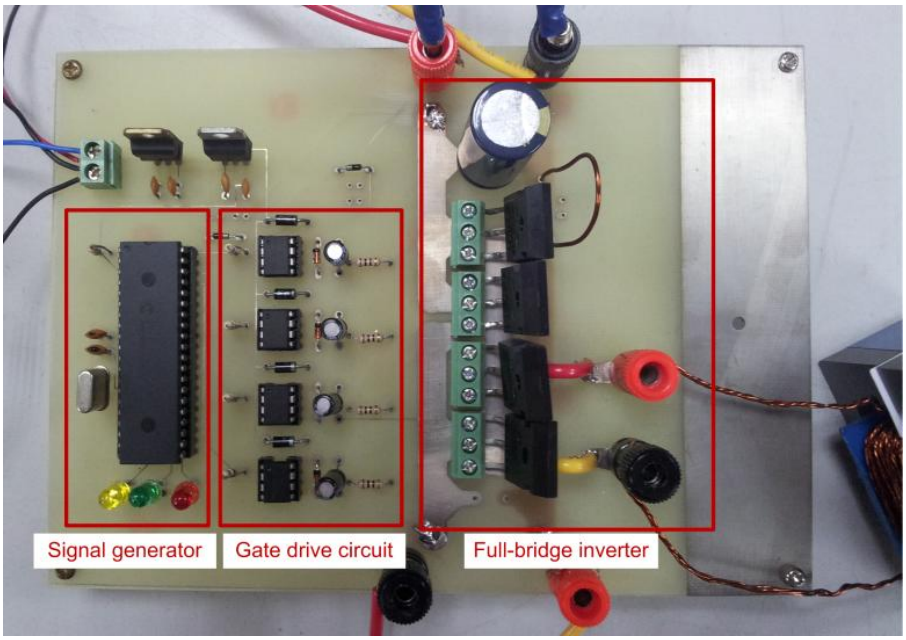


Plate 4.4: The microcontroller-based random switching HPWM inverter

CHAPTER 5

RESULTS AND DISCUSSION

5.1 Introduction

In order to verify the performance of the proposed inverters, simulations were performed and experiments were carried out and the results were collected and analyzed. All the simulations were performed by using the Cadence PSpice AD in order to prove the theoretical concept of the design. Later, the experiments were carried out in order to verify the practical realization. All the results are presented and discussed in the next succeeding sections of this chapter.

5.2 Proposed novel single phase DC-AC inverter

5.2.1 Simulation results

In order to confirm that the proposed topology can be practically implemented, simulation was performed to verify the results. The details of the proposed simulation system are as follow:

Table 5.1: Simulation system parameters for the proposed inverter

Description	Nominal value
DC input voltage, V_{in}	100 V dc
Input capacitor, C_i	100 µF
Snubber capacitor, C_S	1 nF
Holding capacitor, C_H	4.7 µF
Filter inductor, L_C	4 mH
Load resistor, R_L	50 Ω, 75 Ω and 100 Ω
Switching frequency, f_S	10 kHz

Figure 5.1 shows the waveform of gate signal and drain to source voltage of control switch S_C. It also shows the waveform of inductor current. The control switch S_C operates at fixed switching frequency f_S and variable duty cycle D where total period of switching signal $T_S = 1/f_S$ which is equal to $T_S = 0.1$ ms. Figure 5.1 shows the time interval from 2.0 ms to 2.3 ms for 3 cycles of switching pulse for switch S_C. When $V_{GS(Sc)}$ is high, switch S_C is turned on, thus current through inductor L_C starts rising. Due to this, inductor starts storing the energy. When $V_{GS(Sc)}$ is low, switch S_C turned off, energy stored in L_C is released, thus the current through L_C is gradually decreased. Meanwhile, voltage $V_{DS(Sc)}$ during the turned off interval is equal to input dc source V_{in}.

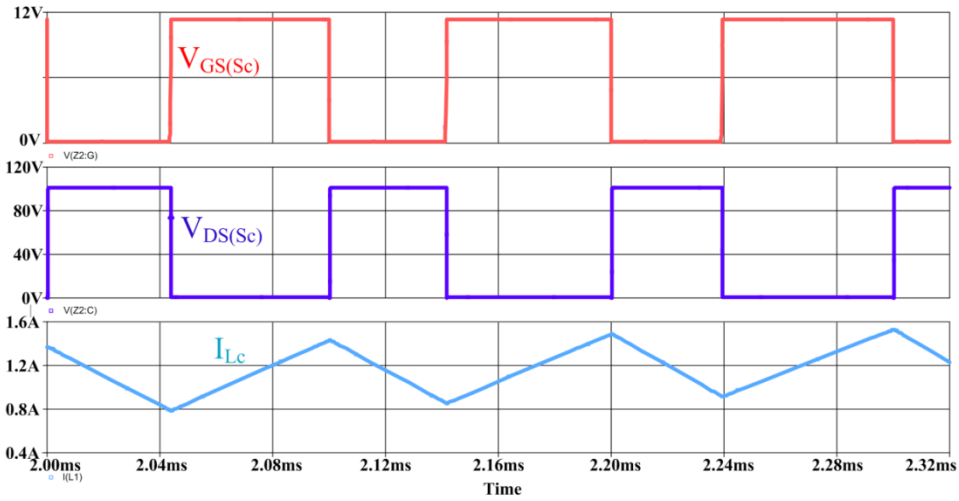


Figure 5.1: Simulation waveforms of the gate signal S_C, voltage at switch S_C and inductor current of the proposed inverter

Figure 5.2 shows the time interval from 2.2 ms to 2.5 ms for 3 cycles of switching pulse for switch S_C. When switch S_C is turned on, current starts flowing through inductor L_C and switch S_C. But when switch S_C is turned off, current stop flowing through switch S_C.

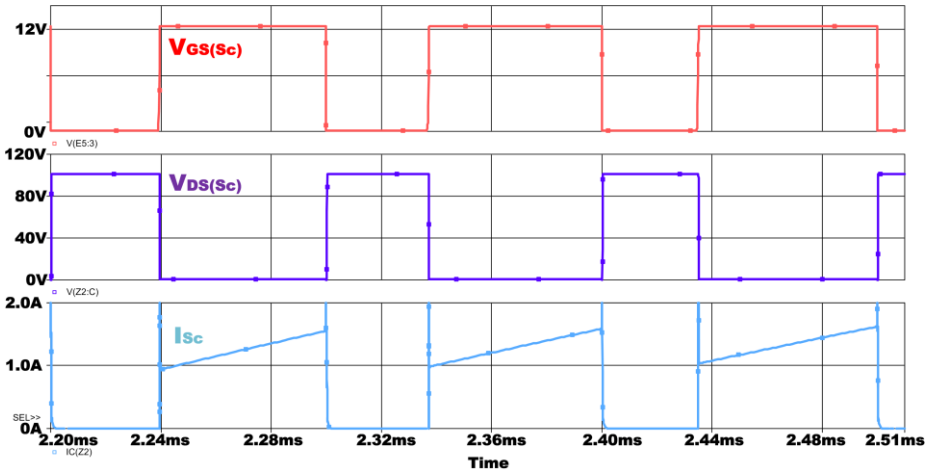


Figure 5.2: Simulation waveforms of the gate signal S_C, voltage at switch S_C and switch current I_{SC} of the proposed inverter

Figure 5.3 show the simulation waveforms of the output voltages, V_{out} and output currents, I_{out} of the proposed inverter for load resistance, R_L = 50 Ω. The waveforms of output voltages and currents show that the proposed topology is able to produce a clean sinusoidal waveform with low distortion and ensure that the proposed topology can obtain less total harmonic distortion, THD. In addition, the amplitude of the output peak voltage V_P produced is almost equal to the input voltage V_{in} which is 100 V. The output current produced is approximately 1.8 A.

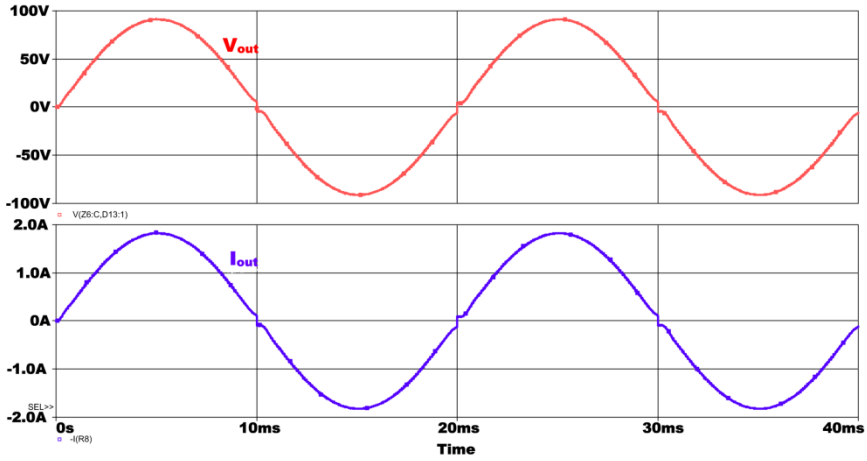


Figure 5.3: Simulation waveforms of the output voltages V_{out} and output currents I_{out} of the proposed inverter for R_L= 50 Ω

Figure 5.4 show the simulation waveforms of the output voltages, V_{out} and output currents, I_{out} of the proposed inverter for load resistance, R_L = 75 Ω. The amplitude of the output voltage V_{out} produced is maintained constant at approximately 90 V, whereas the output current is reduced to approximately 1.2 A due to higher load resistor

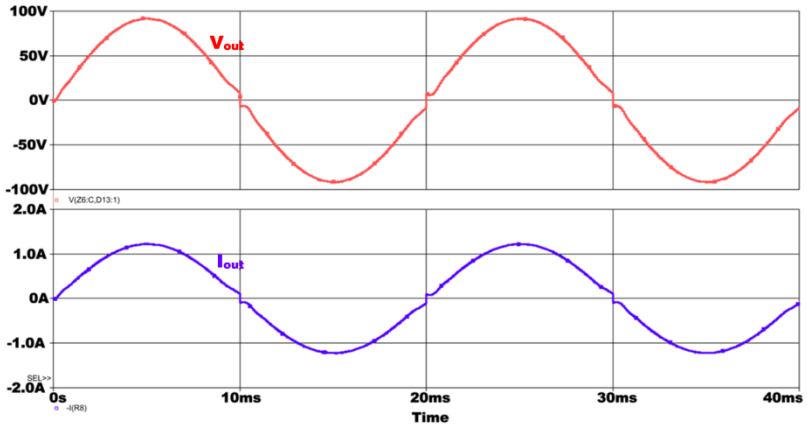


Figure 5.4: Simulation waveforms of the output voltages V_{out} and output currents I_{out} of the proposed inverter for R_L= 75 Ω

Figure 5.5 show the simulation result of the output voltages, V_{out} and output currents, I_{out} of the proposed inverter for load resistance, R_L = 100 Ω. Again the output voltage V_{out} produced is held constant at amplitude of approximately 90 V but the output current is now reduced to approximately 0.9 A.

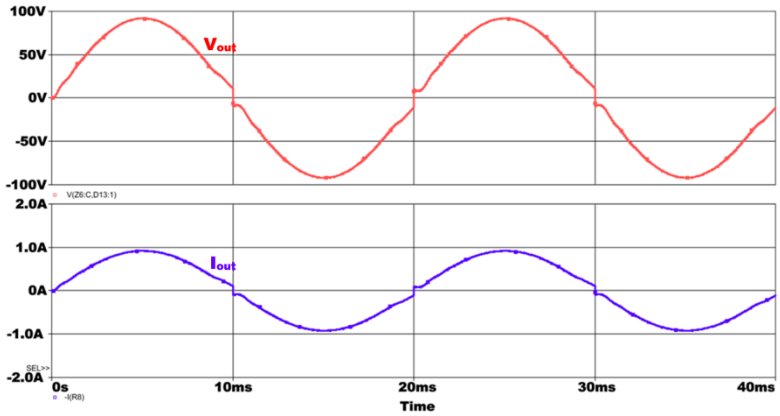


Figure 5.5: Simulation waveforms of the output voltages V_{out} and output currents I_{out} of the proposed inverter for R_L= 100 Ω

From simulation results presented in Figure 5.3 to Figure 5.5, it can be observed that there is distortion during the zero crossing of output voltage and output current waveform. The distortion apparently tends to increase as the load resistance R_L increased. This distortion is caused by phase lag between control switch S_C and the full-bridge switches. Due to this, the circuit is unable to cancel the output voltage to zero during zero crossing intervals. The phase lag causes the holding voltage V_H unable to reach its maximum value during the zero crossing intervals. This problem can be solved by implementing a feedback control into the signal generation circuit of the inverter. A sensor is connected to the circuit to detect the error which is the phase lag during zero crossing. Then, the phase lag will be calculated and the signal generation circuit will correct the error by changing the SPWM signal of switch S_C accordingly with the error calculated.

5.2.2 Experimental results

A 100 W experimental prototype was implemented and tested. The captured experimental results are presented in Figure 5.6 – 5.25. The measured efficiency and THD is given in Table 5.3. The specifications of the experimental system are as follows:

Table 5.2: Experimental system parameters for the proposed inverter

Description	**Nominal value**
DC input voltage, V_{in}	100 V dc
Input capacitor, C_i	100 µF
Snubber capacitor, C_S	1 nF
Holding capacitor, C_H	4.7 µF
Filter inductor, L_C	1.3 mH
Load resistor, R_L	40 Ω - 120 Ω
Switching frequency, f_S	12.5 kHz

The experimental results are very similar to the simulation results presented in previous sections. The output voltage has very less distortion and the result confirm the better performance of proposed system. It was found out that the experimental circuit give better performance for switching frequency, f_S = 12.5 kHz.

Figure 5.6 shows the drain to source voltage of the control switch S_C and inductor current with respect to gate signal voltage waveform of switch S_C respectively. When $V_{GS(Sc)}$ is high, switch S_C is turned on, thus current starts flowing through the inductor L_C. When $V_{GS(Sc)}$ is low, switch S_C is turned off, inductor L_C starts releasing its stored energy. Thus, inductor current I_{Lc} gradually decreases.

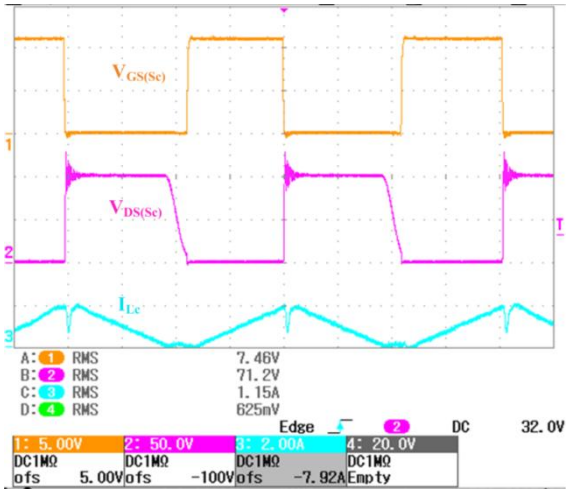
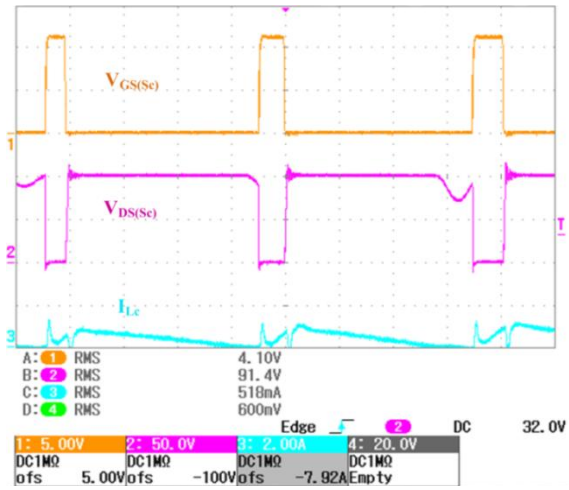
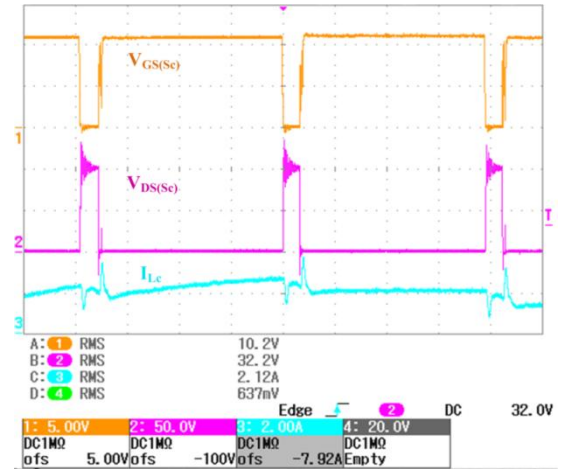


Figure 5.6: Experimental waveforms of the gate signal S_C voltage at switch S_C and inductor current of the proposed inverter for R_L= 50 Ω

Figure 5.7 (a) shows the drain to source voltage of the control switch S_C and inductor current with respect to gate signal voltage waveform of switch S_C at a time interval where duty cycle is smaller. Similarly, Figure 5.7 (b) shows the drain to source voltage of the control switch S_C and current with respect to gate signal voltage of switch S_C at an angle where duty cycle is nearly full. As the duty cycle increased, the inductor current start to increase. Due to this, energy stored in inductor L_C increased.



(a)



(b)

Figure 5.7: Experimental waveforms of the gate signal S_C voltage at switch S_C and inductor current of the proposed inverter at different angle for R_L= 50 Ω: a) short turned on pulses, and b) long turned on pulses

Figure 5.8 shows the experimental waveforms of the output voltage, V_{out} and output load current, I_{out} of the proposed inverter for resistive load, R_L = 40 Ω. As can be seen in Figure 5.8, both the output voltage and output current waveforms are purely sinusoidal.

The obtained result shows that the rms voltage is equal to 61.5 V and the rms current produced is 1.66 A. The power generated for the proposed novel inverter for resistive load, R_L = 40 Ω is equal to 102.09 W. The voltage V_H built up at holding capacitor C_H with a peak value equal to the DC source.

Figure 5.9 shows the THD of the output voltage V_{out}. It can be seen that THD is approximately 3 %. This confirms that proposed inverter produces high quality output voltage. The experimental results presented prove that the proposed topology is capable to produce a clean output power with minimum distortion.

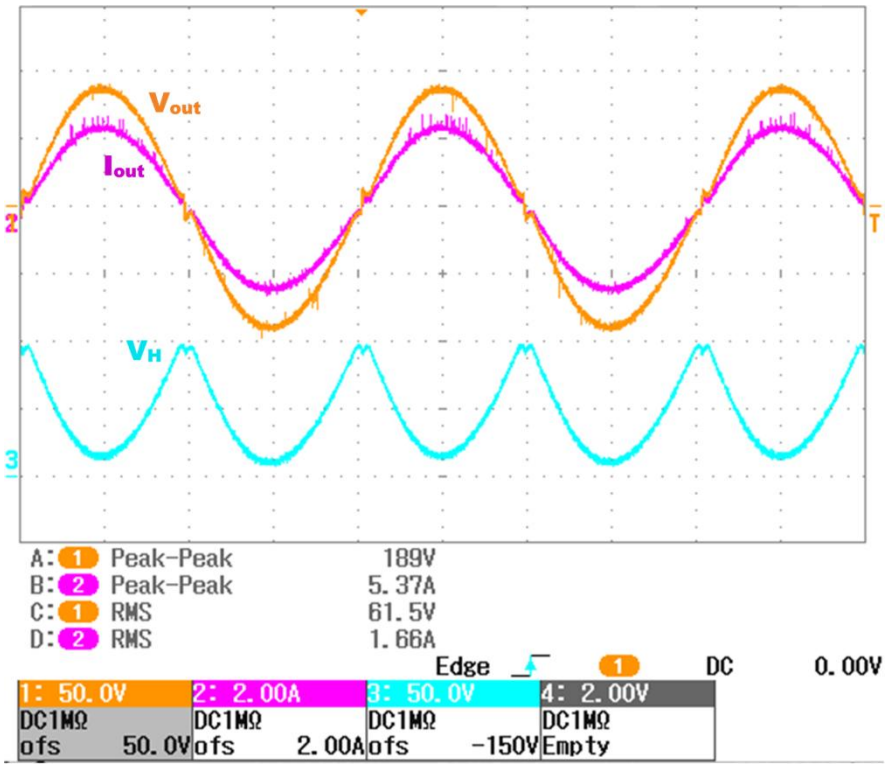


Figure 5.8: Experimental waveforms of the output voltages V_{out} and output currents I_{out} of the proposed inverter for R_L= 40 Ω

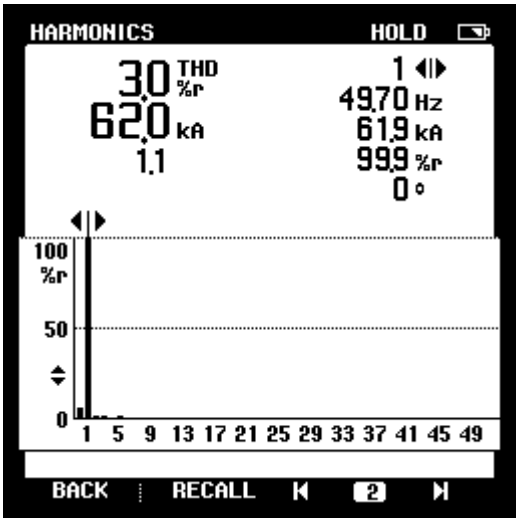


Figure 5.9: Experimental result of voltage harmonic of V_{out} of the proposed inverter for R_L= 40 Ω

Figure 5.10 shows the experimental waveforms of the output voltage, V_{out} and output load current, I_{out} of the proposed inverter for resistive load, R_L = 50 Ω. The obtained result shows that the rms voltage is equal to 62.1 V and the rms current produced is 1.26 A. The power generated for the proposed novel inverter for resistive load, R_L = 50 Ω is equal to 78.25 W. Figure 5.11 shows the THD of the output voltage V_{out} which is approximately 2.9 %.

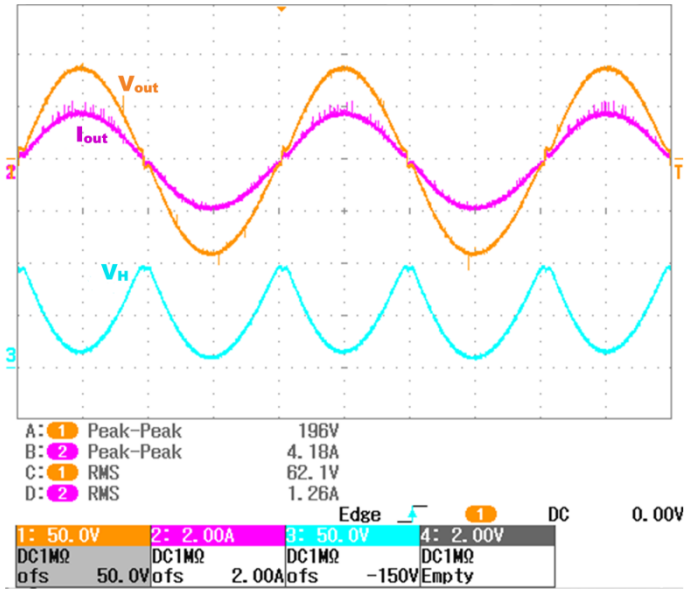


Figure 5.10: Experimental waveforms of the output voltages V_{out} and output currents I_{out} of the proposed inverter for R_L= 50 Ω

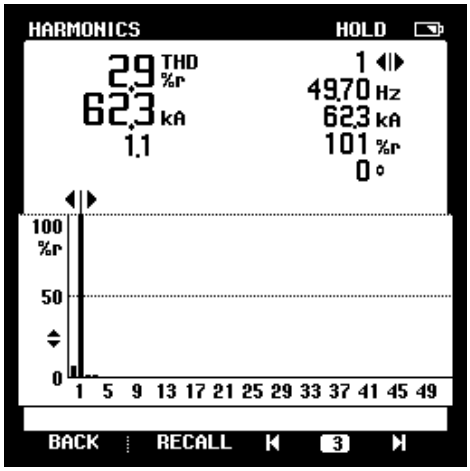


Figure 5.11: Experimental result of voltage harmonic of V_{out} of the proposed inverter for R_L= 50 Ω

Figure 5.12 shows the experimental waveforms of the output voltage, V_{out} and output load current, I_{out} of the proposed inverter for resistive load, R_L = 60 Ω. The obtained result shows that the rms voltage is equal to 62.2 V and the rms load current is 1.07 A. The power generated for the proposed novel inverter for resistive load, R_L = 60 Ω is equal to 66.55 W. Figure 5.13 shows the THD of the output voltage V_{out} produced is approximately 2.8 %.

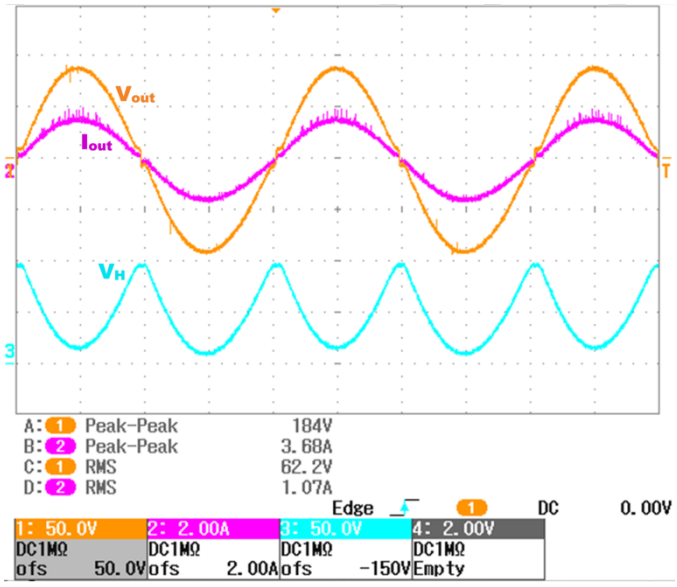


Figure 5.12: Experimental waveforms of the output voltages V_{out} and output currents I_{out} of the proposed inverter for R_L= 60 Ω

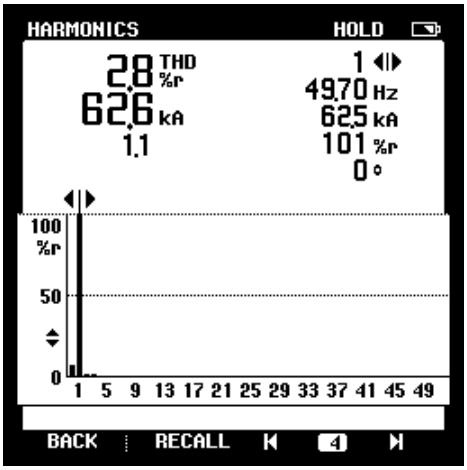


Figure 5.13: Experimental result of voltage harmonic of V_{out} of the proposed inverter for R_L= 60 Ω

Figure 5.14 shows the experimental waveforms of the output voltage, V_{out} and output load current, I_{out} of the proposed inverter for resistive load, R_L = 70 Ω. The obtained result shows that the rms voltage is equal to 62.6 V and the rms current produced is 0.92 A. The power generated for the proposed novel inverter for resistive load of R_L = 70 Ω is equal to 57.59 W. Figure 5.15 shows the THD of the output voltage V_{out} produced that is approximately 2.8 %.

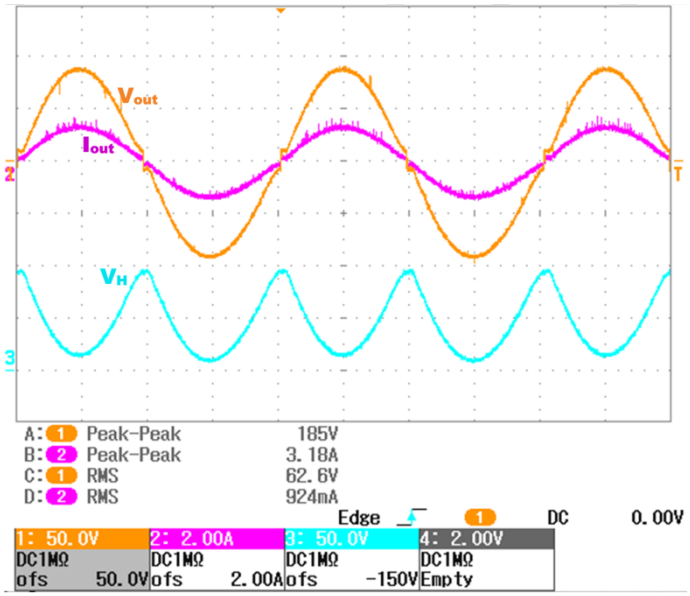


Figure 5.14: Experimental waveforms of the output voltages V_{out} and output currents I_{out} of the proposed inverter for R_L= 70 Ω

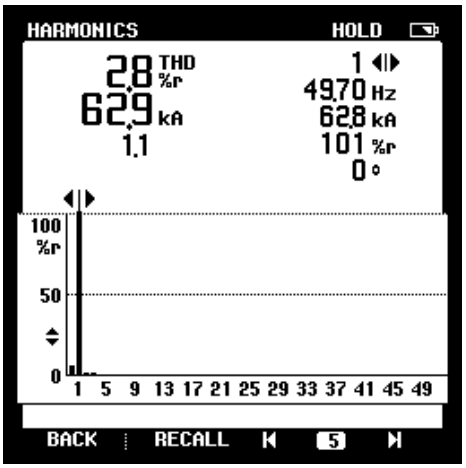


Figure 5.15: Experimental result of voltage harmonic of V_{out} of the proposed inverter for R_L= 70 Ω

Table 5.3 shows the performance of the proposed inverter for output power up to 100 W. Figure 5.16 shows the graph of efficiency for output power range between 30 W – 100 W. The performance data shows that the proposed inverter can operate with efficiency higher than 92% for output power up to 100 W and produce the lowest THD percentage of 2.8%.

Table 5.3: Performance of the novel single phase DC-AC inverter

$R_L(\Omega)$	$V_{in}(V)$	$I_{in}(A)$	$P_{in}(W)$	V_{out} (V)	I_{out} (A)	P_{out} (W)	Η(%)	THD(%)
40	102.2	1.08	110.38	61.5	1.66	102.09	92.50	3
50	102.2	0.81	82.78	62.1	1.26	78.25	94.53	2.9
60	102.2	0.69	70.52	62.2	1.07	66.55	94.37	2.8
70	102.2	0.59	60.30	62.6	0.92	57.59	95.50	2.8
80	102.2	0.51	52.12	63.0	0.80	50.40	96.70	3.2
90	102.2	0.47	48.03	63.0	0.72	45.36	94.44	3.3
100	102.2	0.41	41.90	63.4	0.64	40.58	96.85	3.8
110	102.2	0.38	38.84	63.6	0.59	37.52	96.60	4.2
120	102.2	0.35	35.77	63.8	0.53	33.81	94.52	4.9

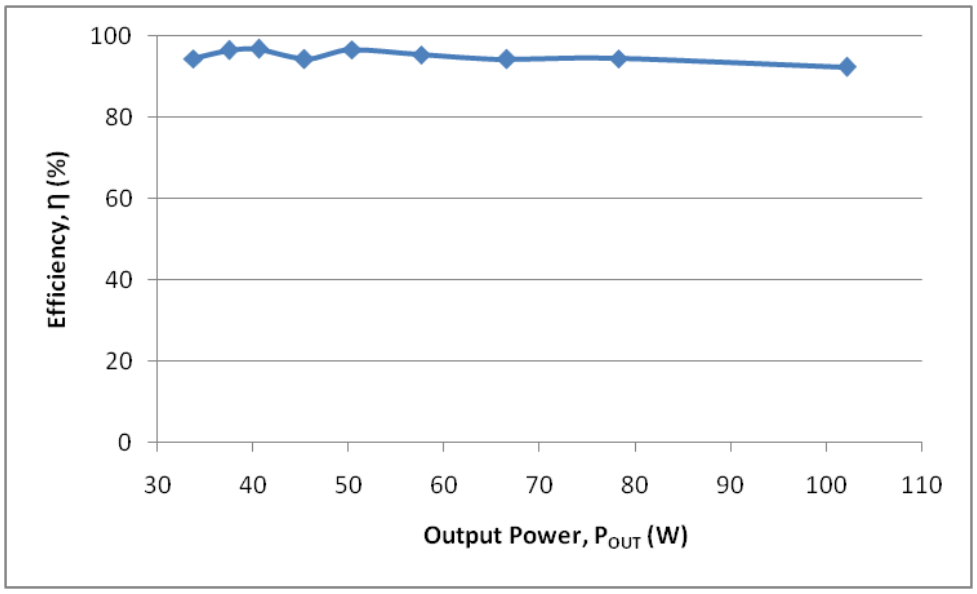


Figure 5.16: Efficiency of the proposed inverter with different output power

5.3 Microcontroller-based inverter with random switching HPWM technique

5.3.1 Experimental results

A 100 W experimental prototype was implemented and tested. The captured experimental results are presented in Figure 5.27 – 5.32. The measured efficiency and THD is given in Table 5.5. The specifications of the experimental system are as follows:

Table 5.4: Experimental system parameters for the microcontroller-based random switching HPWM inverter

Description	Nominal value
DC input voltage, V_{in}	100 V dc
Input capacitor, C_i	100 µF
Filter capacitor, C	6 µF
Filter inductor, L	1 mH
Load resistor, R_L	40 Ω - 120 Ω
Switching frequency, f_S	10 kHz

Figure 5.17 shows the gate signal voltage waveforms of switch S_1- S_4 respectively. In first half cycle, switch S_1 and S_4 is turned on and switch S_2 and S_3 is turned off. Switch S_1 is turned on with high switching frequency while S_4 is turned on with low frequency square wave pulse. In second half cycle, switch S_2 and S_3 is turned on and switch S_1 and S_4 is turned off. Similarly, switch S_2 is turned on with high switching frequency while S_3 is turned on with low frequency square wave pulse. In next first half cycle, the switching operation is reversed where switch S_1 is turned on with low switching frequency while S_4 is turned on with high switching frequency. Similarly in the next second half cycle, the switching is again reversed where S_2 is turned on with low switching frequency and S_3 is turned on with high switching frequency.

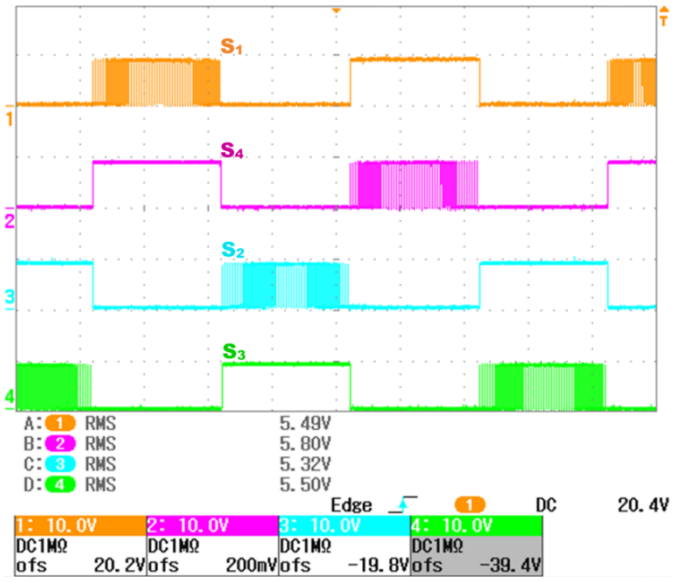


Figure 5.17: Experimental waveforms of the gate signal S_1 – S_4 of the random switching HPWM inverter

Figure 5.18 shows the waveforms of inductor current, I_L and output voltage, V_{out} with respect to gate signal, S_1. The inductor current I_L produced is in form of AC ripple current. The output voltage V_{out} is filtered through the LC filter to produce low frequency (50 Hz) AC voltage.

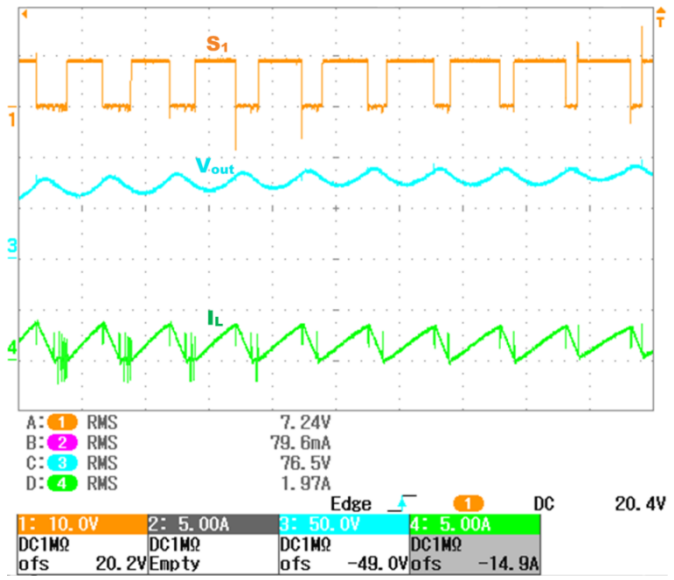


Figure 5.18: Experimental waveforms of inductor current I_L and output voltage V_{out} of the random switching HPWM inverter for R_L= 50 Ω

Figure 5.19 shows the experimental waveforms of the output voltage V_{out}, output load current I_{out} and input current I_{in} with respect to gate signal S_1 of the random switching HPWM inverter. The input current I_{in} is a high frequency pulsating dc current where the frequency of the input current I_{in} is equal to the frequency of the switching signals of the switches.

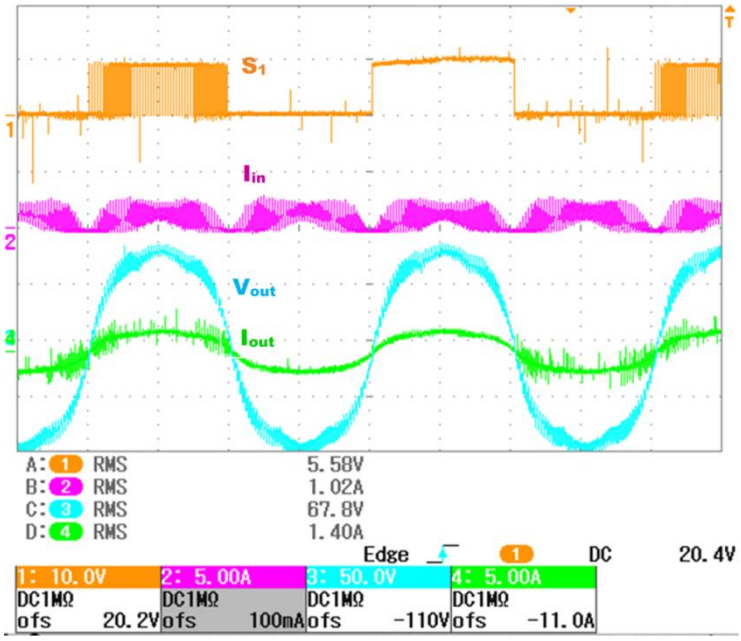


Figure 5.19: Experimental waveforms of output voltage V_{out}, output current I_{out} and input current I_{in} with respect to gate signal S_1 of the random switching HPWM inverter for R_L= 50 Ω

Figure 5.20 shows the experimental waveforms of the output voltage V_{out}, output load current I_{out}, input voltage V_{in}, and gate signal S_1 of the random switching HPWM inverter. The supplied input voltage V_{in} is equal to 100 V. The result in Figure 5.20 shows that the output voltage V_{out} and output current I_{out} are in phase with the gate signal S_1. This is only valid when a small value of LC filter is used. In present case the LC filter value are 1mH and 6µF respectively. Unfortunately, a small value of LC filter will not effectively remove the higher order frequency thus make the output voltage and output current have a higher THD. However, the THD

can be improved by implementing a larger value of LC filter but there will be phase lag between the output waveforms with gate signals. Furthermore, the huge LC filter values come with huge in size and higher in price.

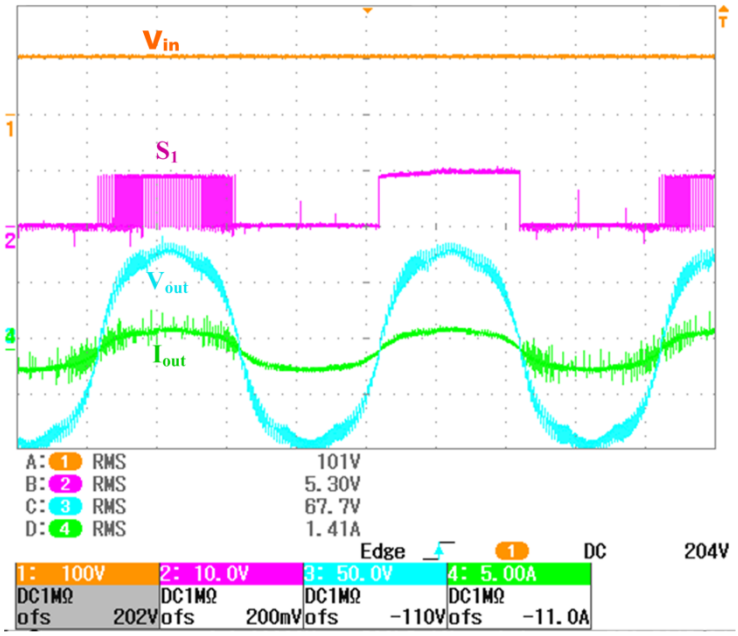


Figure 5.20: Experimental waveforms of input voltage V_{in}, output voltage V_{out}, and output current I_{out} with respect to gate signal S_1 of the random switching HPWM inverter for R_L= 50 Ω

Figure 5.21 shows the output voltage V_{out} and output current I_{out} of the random switching HPWM inverter for resistive load, R = 50 Ω. The obtained result shows that the rms voltage is equal to 66.2 V and the rms current produced is 1.33 A. The power generated for the random switching HPWM inverter for resistive load, R_L = 50 Ω is equal to 88.05 W. Figure 5.22 shows the THD of the output voltage V_{out} produced is 14.7 % for resistive load of R_L = 50 Ω. From the figure, we can observe that the THD produced consist of amount of 3rd and 5th order harmonic compared to the proposed inverter.

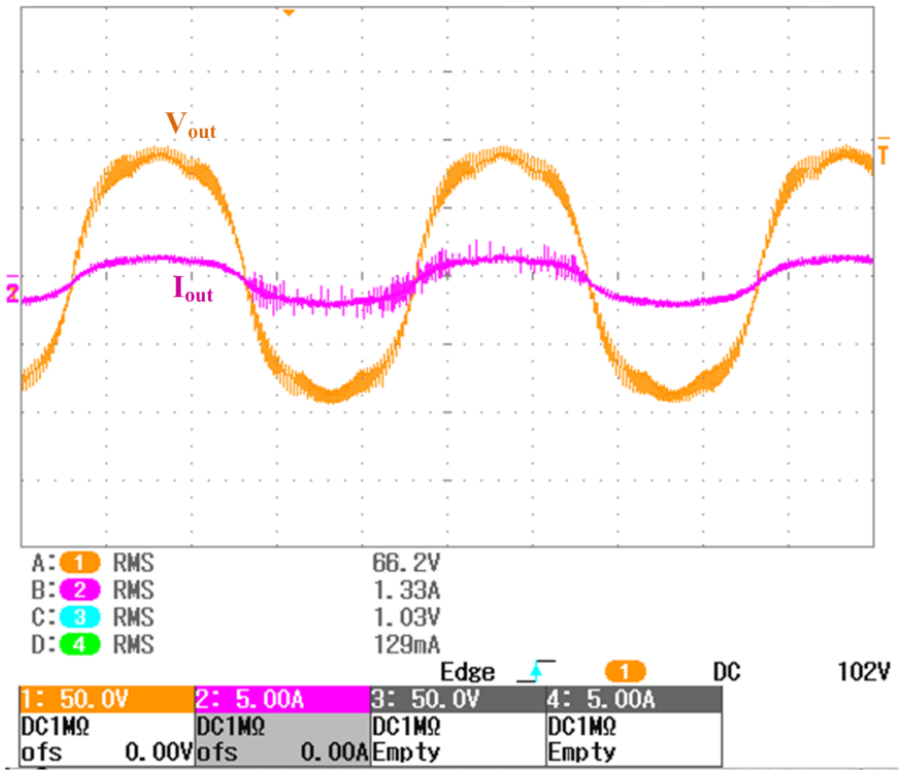


Figure 5.21: Experimental waveforms of output voltage V_{out}, and output current I_{out} of the random switching HPWM inverter for R_L= 50 Ω

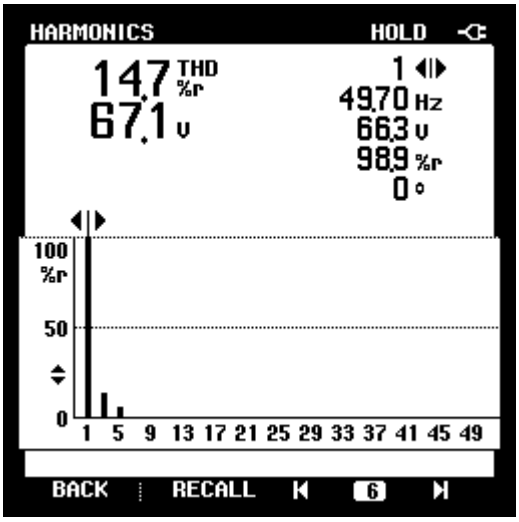


Figure 5.22: Experimental result of voltage harmonic of V_{out} of the random switching HPWM inverter for R_L= 50 Ω

Table 5.5 shows the performance of the random switching HPWM inverter for different output load and the maximum output power produced is equal to 100 W. The output power produced range between 45 – 100 W. The data for output power P_{out} and efficiency Ƞ are arranged and shown graphically in Figure 5.23 in order to show the efficiency performance at different output power levels. The performance data shows that the random switching HPWM inverter operates with efficiencies between 90 % to 92 % for output power up to 100 W and the lowest THD produced is equal to 12 %.

Table 5.5: Performance of the random switching HPWM inverter

$R_L(\Omega)$	$V_{in}(V)$	$I_{in}(A)$	$P_{in}(W)$	$V_{out}(V)$	$I_{out}(A)$	$P_{out}(W)$	Ƞ(%)	THD(%)
40	100	1.12	112	64.5	1.56	100.62	89.8	12.0
50	100	0.95	95	66.3	1.33	88.18	92.8	14.7
60	100	0.83	83	68.0	1.12	76.16	91.7	16.9
70	100	0.73	73	69.5	0.97	67.41	92.3	18.8
80	100	0.66	66	70.5	0.85	59.92	90.8	19.9
90	100	0.61	61	71.6	0.78	55.85	91.5	21.1
100	100	0.57	57	72.3	0.71	51.33	90.0	22.0
110	100	0.53	53	73.2	0.66	48.31	91.1	22.9
120	100	0.49	49	73.9	0.61	45.08	92.0	23.6

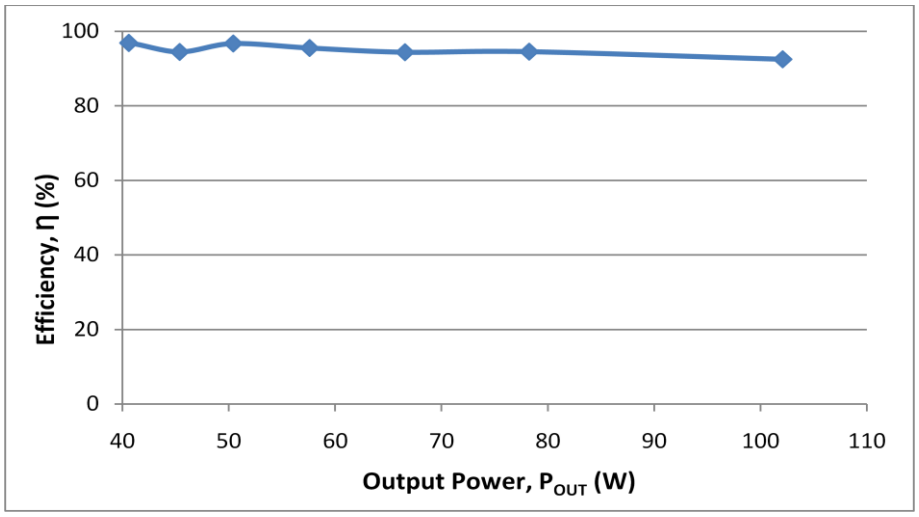


Figure 5.23: Efficiency of the random switching HPWM inverter with different output power

5.4 Comparison between the proposed novel single phase DC-AC inverter and the random switching HPWM inverter

In this section, the performances of the proposed novel single phase inverter and the random switching HPWM inverter is compared. For the proposed novel single phase inverter, the experimental results show good similarity and comparison with the simulation results.

For the proposed inverter, the rms output voltage produced is more stable where rms output voltage is ranged between 61.5 V to 63.8 V for resistive loads between 40 Ω to 120 Ω. Compared to random switching HPWM inverter, it has wider rms output voltage range which is between 64.5 V to 73.9 V for the same resistive loads. This shows that the proposed inverter has smaller voltage regulation compared with the random switching HPWM inverter.

By comparing the output performance of both inverters, it is also proven that the proposed inverter has better output quality. Figure 5.34 shows the comparison of efficiency between the proposed inverter and the random switching HPWM inverter. From the figure, it can be observed that the proposed inverter is operating with higher efficiency than the random switching HPWM inverter.

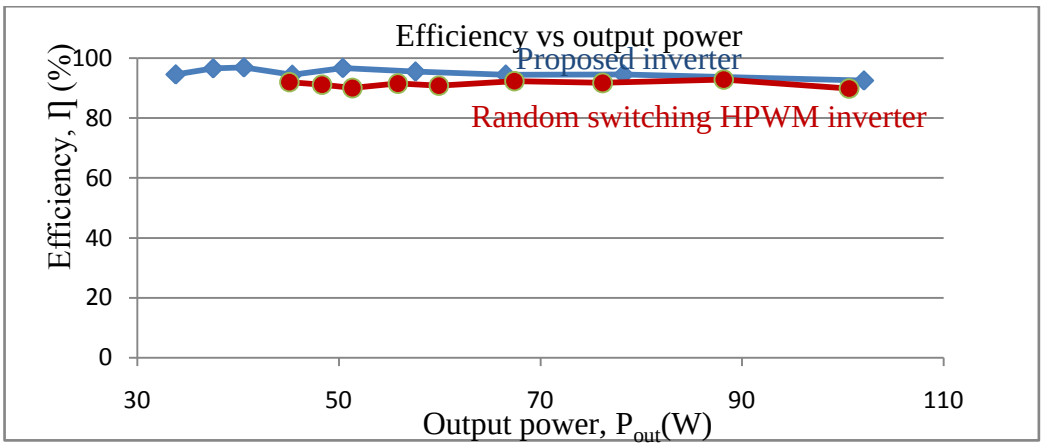


Figure 5.34: Efficiency of the proposed inverter and random switching HPWM inverter with different output power

In term of harmonic distortion, it appears that the proposed inverter has much lower THD value compared to the random switching HPWM inverter. Figure 5.35 depict the THD comparison between the proposed inverter and the random switching HPWM inverter. It can be observed that the proposed inverter is operating with THD approximately between 3 % to 5 % while the random switching HPWM inverter is operating with THD approximately between 12 % to 24 %.

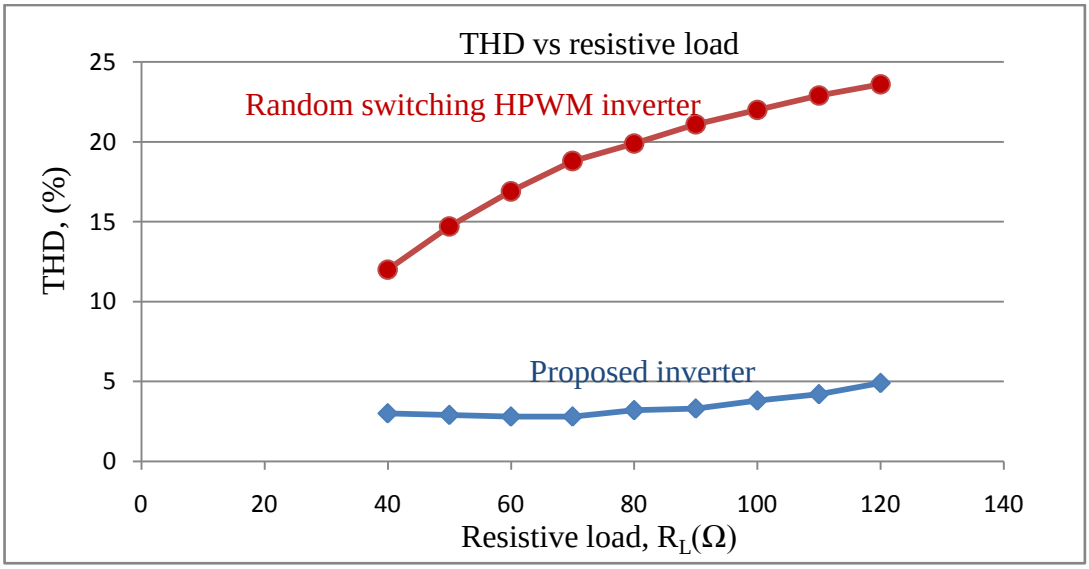


Figure 5.35: THD of the proposed inverter and random switching HPWM inverter as a function of the resistive load

5.5 Discussion of results

Both inverter topologies i.e. the proposed novel single phase DC-AC inverter and random switching HPWM inverter produce sinusoidal output voltage and current. For both inverters, the efficiency performance shows that the inverters have efficiency higher than 90 % for output power range from 30 W to 100 W.

For the proposed inverter, the experimental results show that the inverter is able to produce nearly pure sinusoidal output voltage and current. The results also show that the output produced is less distorted. The measured THD show that the

proposed inverter has the lowest THD percentage of approximately 2.8 % for output load 60 Ω and 70 Ω. It was also observed that the proposed inverter operate with THD between 2.8 % to 4.9 %. The rms output voltages produced were between 61.5 V to 63.8 V for input voltage V_{in} equal to 100 V. The performance data showed that the proposed inverter operates with high efficiency which is ranged from 92.5 % to 96.8 %. This proves that the proposed inverter has significantly lower power losses.

For the random switching HPWM inverter, the experimental results showed that the current produced is having a distortion. The measured THD showed that the random switching HPWM inverter has quite high percentages of THD where it ranged between 12 % to 23.6 %. The rms output voltages produced were between 64.5 V to 73.9 V. The performance data showed that the random switching inverter operates with efficiency from 89.8 % to 92.8 %.

CHAPTER 6

CONCLUSION AND FUTURE WORK

6.1 Conclusion

In this thesis, a novel single phase DC-AC inverter has been designed, developed, tested and evaluated. The performance of the novel single phase DC-AC inverter was evaluated both by simulation and experimental results. The simulation was performed by using Pspice and experimental prototype was built and the obtained results were presented. From the presented results, it was proven that the proposed topology was able to produce a clean sinusoidal output waveform with low distortion and with minimum switching losses, thus yielded high quality output at high efficiency.

In the beginning of this work, the novel single phase DC-AC inverter was proposed. The proposed inverter was basically a new topology which required five switches to work. In this topology, four switches were connected to form a full-bridge configuration and one switch was connected at the lower arm of the full-bridge. The switch connected at the lower arm was operated using SPWM at high frequency and the four switches of full-bridge were operated with square wave at output frequency. Therefore, only one switch was operated at high frequency, consequently the switching loss occurred in only one switch. As a result, proposed topology was able to perform the power conversion from DC to AC with high efficiency.

Next, a random switching HPWM inverter was designed and implemented. This inverter was developed in order to compare its performance with the proposed inverter. The random switching HPWM inverter typically operates by applying only two of the four switches at the full-bridge switches with high switching frequency at a time while keeping the other two switches with low switching frequency. The four switches toggled between high switching frequency and low switching frequency symmetrically. During the implementation, the use of microcontroller had made the random switching HPWM technique implemented with easier design.

From the experimental results of both inverters, it was proven that the proposed novel single phase DC-AC inverter has superior performance compared to random switching HPWM inverter. The proposed inverter was operated with higher efficiency which was more than 92 % than its conventional counterpart which was equal or less than 92%. Furthermore, the proposed inverter was able to produce output voltage and current with less ripple and low THD which was less than 5%. It also has some additional advantages such as better voltage regulation and smaller filter size required.

6.2 Future work

Although this study has achieved its objectives, a lot of continuation work can be done in order to implement the proposed topology in applications. An implementation of proposed inverter in PV system can be designed since solar energy has become very popular and demanding nowadays. A further work also can be done in grid connected inverter system. Solar power plant has now become popular because of its abundant power and pollution free characteristic. Thus, requirement for inverter system that has grid connected feature is huge. The proposed

inverter also can be implemented in UPS system. Since the proposed inverter can produce pure sinusoidal output with good power quality which is low THD and high efficiency, it is well suit for application like UPS that require such features.

Furthermore, the implementation of full system with exact scale prototype can be done. A proper design of circuit layout for the full inverter system which includes DC-DC converter, inverter and their control circuits implemented on the same board is required. This is to ensure that the exact overall system efficiency can be determined. In addition, a robust and compact design can be manufactured. Thus give flexibility for the system to be applied in any condition and environment.

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1 M. F. Abdullah, S. Iqbal, and S. Masri. "A novel single phase DC-AC inverter," in *IEEE Student Conference on Research and Development (SCOReD)*, 5-6 Dec 2012, pp. 172-177.

APPENDICES

APPENDIX A

PROGRAM CODE FOR RANDOM SWITCHING HPWM TECHNIQUE USING PIC16F877

```
'*****************************************************************
'*  Name    : RS-HPWM Inverter                                   *
'*  Author  : Muhammad Faizal                                    *
'*  Notice  : Copyright (c) 2012 [select VIEW...EDITOR OPTIONS] *
'*          : All Rights Reserved                                *
'*  Date    : 9/14/2012                                          *
'*  Version : 1.0                                                *
'*  Notes   :                                                    *
'*          :                                                    *
'*****************************************************************
DEFINE OSC 20
    @ device hs_osc

i var byte
x var byte
TRISB=%00000000

i=0
x=0

' 8-bit A/D conversion on LCD
' Connect analog input to channel-0 (RA0)
' Define ADCIN parameters
Define  ADC_BITS        8     ' Set number of bits in result
Define  ADC_CLOCK       3           ' Set clock source (3=rc)
Define  ADC_SAMPLEUS    50          ' Set sampling time in uS


TRISA = 255               ' Set PORTA to all input
ADCON1= 0               ' Set PORTA analog and right justify result


MAIN:

ADCIN 0, i                          ' Read channel 0 to i
adcin 1, x

if (x<255) then
gosub PWMLOOP
endif
if (x=255) then
PORTB=%00000000: PAUSE 1000
endif
goto main

PWMLOOP:
if (i>=0)   and (i<=89) then
gosub BLINK
endif
if (i>=90) and (i<=101) then
gosub LOOP1
```

```
endif
if (i>=102) and (i<=109) then
gosub LOOP2
endif
if (i>=110) and (i<=255) then
gosub LOOP3
endif
return

BLINK:
PORTB=%00001000: PAUSE 500 : PORTB=%00001000: PAUSE 500
PORTB=%00000100: PAUSE 500 : PORTB=%00000100: PAUSE 500
PORTB=%00000010: PAUSE 500 : PORTB=%00000010: PAUSE 500
return

LOOP1:   'duty cycle = 99%
'1st half(1)
PORTB=%11001000: PAUSEUS  6 :       PORTB=%01001000: PAUSEUS 194
PORTB=%11001000: PAUSEUS 18 :       PORTB=%01001000: PAUSEUS 182
PORTB=%11001000: PAUSEUS 30 :       PORTB=%01001000: PAUSEUS 170
PORTB=%11001000: PAUSEUS 42 :       PORTB=%01001000: PAUSEUS 158
PORTB=%11001000: PAUSEUS 54 :       PORTB=%01001000: PAUSEUS 146
PORTB=%11001000: PAUSEUS 66 :       PORTB=%01001000: PAUSEUS 134
PORTB=%11001000: PAUSEUS 78 :       PORTB=%01001000: PAUSEUS 122
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PORTB=%11001000: PAUSEUS 112 :      PORTB=%01001000: PAUSEUS 88
PORTB=%11001000: PAUSEUS 122 :      PORTB=%01001000: PAUSEUS 78
PORTB=%11001000: PAUSEUS 132 :      PORTB=%01001000: PAUSEUS 68
PORTB=%11001000: PAUSEUS 140 :      PORTB=%01001000: PAUSEUS 60
PORTB=%11001000: PAUSEUS 148 :      PORTB=%01001000: PAUSEUS 52
PORTB=%11001000: PAUSEUS 156 :      PORTB=%01001000: PAUSEUS 44
PORTB=%11001000: PAUSEUS 164 :      PORTB=%01001000: PAUSEUS 36
PORTB=%11001000: PAUSEUS 170 :      PORTB=%01001000: PAUSEUS 30
PORTB=%11001000: PAUSEUS 176 :      PORTB=%01001000: PAUSEUS 24
PORTB=%11001000: PAUSEUS 182 :      PORTB=%01001000: PAUSEUS 18
PORTB=%11001000: PAUSEUS 186 :      PORTB=%01001000: PAUSEUS 14
PORTB=%11001000: PAUSEUS 190 :      PORTB=%01001000: PAUSEUS 10
PORTB=%11001000: PAUSEUS 193 :      PORTB=%01001000: PAUSEUS  7
PORTB=%11001000: PAUSEUS 196 :      PORTB=%01001000: PAUSEUS  4
PORTB=%11001000: PAUSEUS 198 :      PORTB=%01001000: PAUSEUS  2
PORTB=%11001000: PAUSEUS 199 :      PORTB=%01001000: PAUSEUS  1
PORTB=%11001000: PAUSEUS 199 :      PORTB=%01001000: PAUSEUS  1
PORTB=%11001000: PAUSEUS 198 :      PORTB=%01001000: PAUSEUS  2
PORTB=%11001000: PAUSEUS 196 :      PORTB=%01001000: PAUSEUS  4
PORTB=%11001000: PAUSEUS 193 :      PORTB=%01001000: PAUSEUS  7
PORTB=%11001000: PAUSEUS 190 :      PORTB=%01001000: PAUSEUS 10
PORTB=%11001000: PAUSEUS 186 :      PORTB=%01001000: PAUSEUS 14
PORTB=%11001000: PAUSEUS 182 :      PORTB=%01001000: PAUSEUS 18
PORTB=%11001000: PAUSEUS 176 :      PORTB=%01001000: PAUSEUS 24
PORTB=%11001000: PAUSEUS 170 :      PORTB=%01001000: PAUSEUS 30
PORTB=%11001000: PAUSEUS 164 :      PORTB=%01001000: PAUSEUS 36
PORTB=%11001000: PAUSEUS 156 :      PORTB=%01001000: PAUSEUS 44
PORTB=%11001000: PAUSEUS 148 :      PORTB=%01001000: PAUSEUS 52
PORTB=%11001000: PAUSEUS 140 :      PORTB=%01001000: PAUSEUS 60
PORTB=%11001000: PAUSEUS 132 :      PORTB=%01001000: PAUSEUS 68
PORTB=%11001000: PAUSEUS 122 :      PORTB=%01001000: PAUSEUS 78
PORTB=%11001000: PAUSEUS 112 :      PORTB=%01001000: PAUSEUS 88
PORTB=%11001000: PAUSEUS 102 :      PORTB=%01001000: PAUSEUS 98
PORTB=%11001000: PAUSEUS 90 :       PORTB=%01001000: PAUSEUS 110
PORTB=%11001000: PAUSEUS 78 :       PORTB=%01001000: PAUSEUS 122
```

```
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PORTB=%11001000: PAUSEUS 54 :       PORTB=%01001000: PAUSEUS 146
PORTB=%11001000: PAUSEUS 42 :       PORTB=%01001000: PAUSEUS 158
PORTB=%11001000: PAUSEUS 30 :       PORTB=%01001000: PAUSEUS 170
PORTB=%11001000: PAUSEUS 18 :       PORTB=%01001000: PAUSEUS 182
PORTB=%11001000: PAUSEUS  6 :       PORTB=%01001000: PAUSEUS 194
PORTB=%00000000: PAUSEUS  1

'2nd half(1)
PORTB=%00111000: PAUSEUS  6 :       PORTB=%00011000: PAUSEUS 194
PORTB=%00111000: PAUSEUS 18 :       PORTB=%00011000: PAUSEUS 182
PORTB=%00111000: PAUSEUS 30 :       PORTB=%00011000: PAUSEUS 170
PORTB=%00111000: PAUSEUS 42 :       PORTB=%00011000: PAUSEUS 158
PORTB=%00111000: PAUSEUS 54 :       PORTB=%00011000: PAUSEUS 146
PORTB=%00111000: PAUSEUS 66 :       PORTB=%00011000: PAUSEUS 134
PORTB=%00111000: PAUSEUS 78 :       PORTB=%00011000: PAUSEUS 122
PORTB=%00111000: PAUSEUS 90 :       PORTB=%00011000: PAUSEUS 110
PORTB=%00111000: PAUSEUS 102 :      PORTB=%00011000: PAUSEUS 98
PORTB=%00111000: PAUSEUS 112 :      PORTB=%00011000: PAUSEUS 88
PORTB=%00111000: PAUSEUS 122 :      PORTB=%00011000: PAUSEUS 78
PORTB=%00111000: PAUSEUS 132 :      PORTB=%00011000: PAUSEUS 68
PORTB=%00111000: PAUSEUS 140 :      PORTB=%00011000: PAUSEUS 60
PORTB=%00111000: PAUSEUS 148 :      PORTB=%00011000: PAUSEUS 52
PORTB=%00111000: PAUSEUS 156 :      PORTB=%00011000: PAUSEUS 44
PORTB=%00111000: PAUSEUS 164 :      PORTB=%00011000: PAUSEUS 36
PORTB=%00111000: PAUSEUS 170 :      PORTB=%00011000: PAUSEUS 30
PORTB=%00111000: PAUSEUS 176 :      PORTB=%00011000: PAUSEUS 24
PORTB=%00111000: PAUSEUS 182 :      PORTB=%00011000: PAUSEUS 18
PORTB=%00111000: PAUSEUS 186 :      PORTB=%00011000: PAUSEUS 14
PORTB=%00111000: PAUSEUS 190 :      PORTB=%00011000: PAUSEUS 10
PORTB=%00111000: PAUSEUS 193 :      PORTB=%00011000: PAUSEUS  7
PORTB=%00111000: PAUSEUS 196 :      PORTB=%00011000: PAUSEUS  4
PORTB=%00111000: PAUSEUS 198 :      PORTB=%00011000: PAUSEUS  2
PORTB=%00111000: PAUSEUS 199 :      PORTB=%00011000: PAUSEUS  1
PORTB=%00111000: PAUSEUS 199 :      PORTB=%00011000: PAUSEUS  1
PORTB=%00111000: PAUSEUS 198 :      PORTB=%00011000: PAUSEUS  2
PORTB=%00111000: PAUSEUS 196 :      PORTB=%00011000: PAUSEUS  4
PORTB=%00111000: PAUSEUS 193 :      PORTB=%00011000: PAUSEUS  7
PORTB=%00111000: PAUSEUS 190 :      PORTB=%00011000: PAUSEUS 10
PORTB=%00111000: PAUSEUS 186 :      PORTB=%00011000: PAUSEUS 14
PORTB=%00111000: PAUSEUS 182 :      PORTB=%00011000: PAUSEUS 18
PORTB=%00111000: PAUSEUS 176 :      PORTB=%00011000: PAUSEUS 24
PORTB=%00111000: PAUSEUS 170 :      PORTB=%00011000: PAUSEUS 30
PORTB=%00111000: PAUSEUS 164 :      PORTB=%00011000: PAUSEUS 36
PORTB=%00111000: PAUSEUS 156 :      PORTB=%00011000: PAUSEUS 44
PORTB=%00111000: PAUSEUS 148 :      PORTB=%00011000: PAUSEUS 52
PORTB=%00111000: PAUSEUS 140 :      PORTB=%00011000: PAUSEUS 60
PORTB=%00111000: PAUSEUS 132 :      PORTB=%00011000: PAUSEUS 68
PORTB=%00111000: PAUSEUS 122 :      PORTB=%00011000: PAUSEUS 78
PORTB=%00111000: PAUSEUS 112 :      PORTB=%00011000: PAUSEUS 88
PORTB=%00111000: PAUSEUS 102 :      PORTB=%00011000: PAUSEUS 98
PORTB=%00111000: PAUSEUS 90 :       PORTB=%00011000: PAUSEUS 110
PORTB=%00111000: PAUSEUS 78 :       PORTB=%00011000: PAUSEUS 122
PORTB=%00111000: PAUSEUS 66 :       PORTB=%00011000: PAUSEUS 134
PORTB=%00111000: PAUSEUS 54 :       PORTB=%00011000: PAUSEUS 146
PORTB=%00111000: PAUSEUS 42 :       PORTB=%00011000: PAUSEUS 158
PORTB=%00111000: PAUSEUS 30 :       PORTB=%00011000: PAUSEUS 170
PORTB=%00111000: PAUSEUS 18 :       PORTB=%00011000: PAUSEUS 182
PORTB=%00111000: PAUSEUS  6 :       PORTB=%00011000: PAUSEUS 194
PORTB=%00000000: PAUSEUS  1
```

```
'1st half(2)
PORTB=%11001000: PAUSEUS  6 :       PORTB=%10001000: PAUSEUS 194
PORTB=%11001000: PAUSEUS 18 :       PORTB=%10001000: PAUSEUS 182
PORTB=%11001000: PAUSEUS 30 :       PORTB=%10001000: PAUSEUS 170
PORTB=%11001000: PAUSEUS 42 :       PORTB=%10001000: PAUSEUS 158
PORTB=%11001000: PAUSEUS 54 :       PORTB=%10001000: PAUSEUS 146
PORTB=%11001000: PAUSEUS 66 :       PORTB=%10001000: PAUSEUS 134
PORTB=%11001000: PAUSEUS 78 :       PORTB=%10001000: PAUSEUS 122
PORTB=%11001000: PAUSEUS 90 :       PORTB=%10001000: PAUSEUS 110
PORTB=%11001000: PAUSEUS 102 :      PORTB=%10001000: PAUSEUS 98
PORTB=%11001000: PAUSEUS 112 :      PORTB=%10001000: PAUSEUS 88
PORTB=%11001000: PAUSEUS 122 :      PORTB=%10001000: PAUSEUS 78
PORTB=%11001000: PAUSEUS 132 :      PORTB=%10001000: PAUSEUS 68
PORTB=%11001000: PAUSEUS 140 :      PORTB=%10001000: PAUSEUS 60
PORTB=%11001000: PAUSEUS 148 :      PORTB=%10001000: PAUSEUS 52
PORTB=%11001000: PAUSEUS 156 :      PORTB=%10001000: PAUSEUS 44
PORTB=%11001000: PAUSEUS 164 :      PORTB=%10001000: PAUSEUS 36
PORTB=%11001000: PAUSEUS 170 :      PORTB=%10001000: PAUSEUS 30
PORTB=%11001000: PAUSEUS 176 :      PORTB=%10001000: PAUSEUS 24
PORTB=%11001000: PAUSEUS 182 :      PORTB=%10001000: PAUSEUS 18
PORTB=%11001000: PAUSEUS 186 :      PORTB=%10001000: PAUSEUS 14
PORTB=%11001000: PAUSEUS 190 :      PORTB=%10001000: PAUSEUS 10
PORTB=%11001000: PAUSEUS 193 :      PORTB=%10001000: PAUSEUS  7
PORTB=%11001000: PAUSEUS 196 :      PORTB=%10001000: PAUSEUS  4
PORTB=%11001000: PAUSEUS 198 :      PORTB=%10001000: PAUSEUS  2
PORTB=%11001000: PAUSEUS 199 :      PORTB=%10001000: PAUSEUS  1
PORTB=%11001000: PAUSEUS 199 :      PORTB=%10001000: PAUSEUS  1
PORTB=%11001000: PAUSEUS 198 :      PORTB=%10001000: PAUSEUS  2
PORTB=%11001000: PAUSEUS 196 :      PORTB=%10001000: PAUSEUS  4
PORTB=%11001000: PAUSEUS 193 :      PORTB=%10001000: PAUSEUS  7
PORTB=%11001000: PAUSEUS 190 :      PORTB=%10001000: PAUSEUS 10
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PORTB=%11001000: PAUSEUS 182 :      PORTB=%10001000: PAUSEUS 18
PORTB=%11001000: PAUSEUS 176 :      PORTB=%10001000: PAUSEUS 24
PORTB=%11001000: PAUSEUS 170 :      PORTB=%10001000: PAUSEUS 30
PORTB=%11001000: PAUSEUS 164 :      PORTB=%10001000: PAUSEUS 36
PORTB=%11001000: PAUSEUS 156 :      PORTB=%10001000: PAUSEUS 44
PORTB=%11001000: PAUSEUS 148 :      PORTB=%10001000: PAUSEUS 52
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PORTB=%11001000: PAUSEUS 102 :      PORTB=%10001000: PAUSEUS 98
PORTB=%11001000: PAUSEUS 90 :       PORTB=%10001000: PAUSEUS 110
PORTB=%11001000: PAUSEUS 78 :       PORTB=%10001000: PAUSEUS 122
PORTB=%11001000: PAUSEUS 66 :       PORTB=%10001000: PAUSEUS 134
PORTB=%11001000: PAUSEUS 54 :       PORTB=%10001000: PAUSEUS 146
PORTB=%11001000: PAUSEUS 42 :       PORTB=%10001000: PAUSEUS 158
PORTB=%11001000: PAUSEUS 30 :       PORTB=%10001000: PAUSEUS 170
PORTB=%11001000: PAUSEUS 18 :       PORTB=%10001000: PAUSEUS 182
PORTB=%11001000: PAUSEUS  6 :       PORTB=%10001000: PAUSEUS 194
PORTB=%00000000: PAUSEUS  1

'2nd half(2)
PORTB=%00111000: PAUSEUS  6 :       PORTB=%00101000: PAUSEUS 194
PORTB=%00111000: PAUSEUS 18 :       PORTB=%00101000: PAUSEUS 182
PORTB=%00111000: PAUSEUS 30 :       PORTB=%00101000: PAUSEUS 170
PORTB=%00111000: PAUSEUS 42 :       PORTB=%00101000: PAUSEUS 158
PORTB=%00111000: PAUSEUS 54 :       PORTB=%00101000: PAUSEUS 146
PORTB=%00111000: PAUSEUS 66 :       PORTB=%00101000: PAUSEUS 134
PORTB=%00111000: PAUSEUS 78 :       PORTB=%00101000: PAUSEUS 122
```

```
PORTB=%00111000: PAUSEUS 90 :       PORTB=%00101000: PAUSEUS 110
PORTB=%00111000: PAUSEUS 102 :      PORTB=%00101000: PAUSEUS 98
PORTB=%00111000: PAUSEUS 112 :      PORTB=%00101000: PAUSEUS 88
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PORTB=%00111000: PAUSEUS 140 :      PORTB=%00101000: PAUSEUS 60
PORTB=%00111000: PAUSEUS 148 :      PORTB=%00101000: PAUSEUS 52
PORTB=%00111000: PAUSEUS 156 :      PORTB=%00101000: PAUSEUS 44
PORTB=%00111000: PAUSEUS 164 :      PORTB=%00101000: PAUSEUS 36
PORTB=%00111000: PAUSEUS 170 :      PORTB=%00101000: PAUSEUS 30
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PORTB=%00111000: PAUSEUS 182 :      PORTB=%00101000: PAUSEUS 18
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PORTB=%00111000: PAUSEUS 190 :      PORTB=%00101000: PAUSEUS 10
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PORTB=%00111000: PAUSEUS 196 :      PORTB=%00101000: PAUSEUS  4
PORTB=%00111000: PAUSEUS 198 :      PORTB=%00101000: PAUSEUS  2
PORTB=%00111000: PAUSEUS 199 :      PORTB=%00101000: PAUSEUS  1
PORTB=%00111000: PAUSEUS 199 :      PORTB=%00101000: PAUSEUS  1
PORTB=%00111000: PAUSEUS 198 :      PORTB=%00101000: PAUSEUS  2
PORTB=%00111000: PAUSEUS 196 :      PORTB=%00101000: PAUSEUS  4
PORTB=%00111000: PAUSEUS 193 :      PORTB=%00101000: PAUSEUS  7
PORTB=%00111000: PAUSEUS 190 :      PORTB=%00101000: PAUSEUS 10
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PORTB=%00111000: PAUSEUS 182 :      PORTB=%00101000: PAUSEUS 18
PORTB=%00111000: PAUSEUS 176 :      PORTB=%00101000: PAUSEUS 24
PORTB=%00111000: PAUSEUS 170 :      PORTB=%00101000: PAUSEUS 30
PORTB=%00111000: PAUSEUS 164 :      PORTB=%00101000: PAUSEUS 36
PORTB=%00111000: PAUSEUS 156 :      PORTB=%00101000: PAUSEUS 44
PORTB=%00111000: PAUSEUS 148 :      PORTB=%00101000: PAUSEUS 52
PORTB=%00111000: PAUSEUS 140 :      PORTB=%00101000: PAUSEUS 60
PORTB=%00111000: PAUSEUS 132 :      PORTB=%00101000: PAUSEUS 68
PORTB=%00111000: PAUSEUS 122 :      PORTB=%00101000: PAUSEUS 78
PORTB=%00111000: PAUSEUS 112 :      PORTB=%00101000: PAUSEUS 88
PORTB=%00111000: PAUSEUS 102 :      PORTB=%00101000: PAUSEUS 98
PORTB=%00111000: PAUSEUS 90 :       PORTB=%00101000: PAUSEUS 110
PORTB=%00111000: PAUSEUS 78 :       PORTB=%00101000: PAUSEUS 122
PORTB=%00111000: PAUSEUS 66 :       PORTB=%00101000: PAUSEUS 134
PORTB=%00111000: PAUSEUS 54 :       PORTB=%00101000: PAUSEUS 146
PORTB=%00111000: PAUSEUS 42 :       PORTB=%00101000: PAUSEUS 158
PORTB=%00111000: PAUSEUS 30 :       PORTB=%00101000: PAUSEUS 170
PORTB=%00111000: PAUSEUS 18 :       PORTB=%00101000: PAUSEUS 182
PORTB=%00111000: PAUSEUS  6 :       PORTB=%00101000: PAUSEUS 194
PORTB=%00000000: PAUSEUS  1
return

LOOP2:   'duty cycle = 90%
'1st half(1)
PORTB=%11000100: PAUSEUS  6 :       PORTB=%01000100: PAUSEUS 194
PORTB=%11000100: PAUSEUS 16 :       PORTB=%01000100: PAUSEUS 184
PORTB=%11000100: PAUSEUS 28 :       PORTB=%01000100: PAUSEUS 172
PORTB=%11000100: PAUSEUS 40 :       PORTB=%01000100: PAUSEUS 160
PORTB=%11000100: PAUSEUS 50 :       PORTB=%01000100: PAUSEUS 150
PORTB=%11000100: PAUSEUS 62 :       PORTB=%01000100: PAUSEUS 138
PORTB=%11000100: PAUSEUS 72 :       PORTB=%01000100: PAUSEUS 128
PORTB=%11000100: PAUSEUS 82 :       PORTB=%01000100: PAUSEUS 118
PORTB=%11000100: PAUSEUS 92 :       PORTB=%01000100: PAUSEUS 108
PORTB=%11000100: PAUSEUS 102 :      PORTB=%01000100: PAUSEUS 98
PORTB=%11000100: PAUSEUS 111 :      PORTB=%01000100: PAUSEUS 89
PORTB=%11000100: PAUSEUS 120 :      PORTB=%01000100: PAUSEUS 80
PORTB=%11000100: PAUSEUS 128 :      PORTB=%01000100: PAUSEUS 72
```

```
PORTB=%11000100: PAUSEUS 136 :      PORTB=%01000100: PAUSEUS 64
PORTB=%11000100: PAUSEUS 143 :      PORTB=%01000100: PAUSEUS 57
PORTB=%11000100: PAUSEUS 150 :      PORTB=%01000100: PAUSEUS 50
PORTB=%11000100: PAUSEUS 156 :      PORTB=%01000100: PAUSEUS 44
PORTB=%11000100: PAUSEUS 162 :      PORTB=%01000100: PAUSEUS 38
PORTB=%11000100: PAUSEUS 166 :      PORTB=%01000100: PAUSEUS 34
PORTB=%11000100: PAUSEUS 170 :      PORTB=%01000100: PAUSEUS 30
PORTB=%11000100: PAUSEUS 173 :      PORTB=%01000100: PAUSEUS 27
PORTB=%11000100: PAUSEUS 175 :      PORTB=%01000100: PAUSEUS 25
PORTB=%11000100: PAUSEUS 177 :      PORTB=%01000100: PAUSEUS 23
PORTB=%11000100: PAUSEUS 179 :      PORTB=%01000100: PAUSEUS 21
PORTB=%11000100: PAUSEUS 180 :      PORTB=%01000100: PAUSEUS 20
PORTB=%11000100: PAUSEUS 180 :      PORTB=%01000100: PAUSEUS 20
PORTB=%11000100: PAUSEUS 179 :      PORTB=%01000100: PAUSEUS 21
PORTB=%11000100: PAUSEUS 177 :      PORTB=%01000100: PAUSEUS 23
PORTB=%11000100: PAUSEUS 175 :      PORTB=%01000100: PAUSEUS 25
PORTB=%11000100: PAUSEUS 173 :      PORTB=%01000100: PAUSEUS 27
PORTB=%11000100: PAUSEUS 170 :      PORTB=%01000100: PAUSEUS 30
PORTB=%11000100: PAUSEUS 166 :      PORTB=%01000100: PAUSEUS 34
PORTB=%11000100: PAUSEUS 162 :      PORTB=%01000100: PAUSEUS 38
PORTB=%11000100: PAUSEUS 156 :      PORTB=%01000100: PAUSEUS 44
PORTB=%11000100: PAUSEUS 150 :      PORTB=%01000100: PAUSEUS 50
PORTB=%11000100: PAUSEUS 143 :      PORTB=%01000100: PAUSEUS 57
PORTB=%11000100: PAUSEUS 136 :      PORTB=%01000100: PAUSEUS 64
PORTB=%11000100: PAUSEUS 128 :      PORTB=%01000100: PAUSEUS 72
PORTB=%11000100: PAUSEUS 120 :      PORTB=%01000100: PAUSEUS 80
PORTB=%11000100: PAUSEUS 111 :      PORTB=%01000100: PAUSEUS 89
PORTB=%11000100: PAUSEUS 102 :      PORTB=%01000100: PAUSEUS 98
PORTB=%11000100: PAUSEUS 92 :       PORTB=%01000100: PAUSEUS 108
PORTB=%11000100: PAUSEUS 82 :       PORTB=%01000100: PAUSEUS 118
PORTB=%11000100: PAUSEUS 72 :       PORTB=%01000100: PAUSEUS 128
PORTB=%11000100: PAUSEUS 62 :       PORTB=%01000100: PAUSEUS 138
PORTB=%11000100: PAUSEUS 50 :       PORTB=%01000100: PAUSEUS 150
PORTB=%11000100: PAUSEUS 40 :       PORTB=%01000100: PAUSEUS 160
PORTB=%11000100: PAUSEUS 28 :       PORTB=%01000100: PAUSEUS 172
PORTB=%11000100: PAUSEUS 16 :       PORTB=%01000100: PAUSEUS 184
PORTB=%11000100: PAUSEUS  6 :       PORTB=%01000100: PAUSEUS 194
PORTB=%00000000: PAUSEUS  1

'2nd half(1)
PORTB=%00110100: PAUSEUS  6 :       PORTB=%00010100: PAUSEUS 194
PORTB=%00110100: PAUSEUS 16 :       PORTB=%00010100: PAUSEUS 184
PORTB=%00110100: PAUSEUS 28 :       PORTB=%00010100: PAUSEUS 172
PORTB=%00110100: PAUSEUS 40 :       PORTB=%00010100: PAUSEUS 160
PORTB=%00110100: PAUSEUS 50 :       PORTB=%00010100: PAUSEUS 150
PORTB=%00110100: PAUSEUS 62 :       PORTB=%00010100: PAUSEUS 138
PORTB=%00110100: PAUSEUS 72 :       PORTB=%00010100: PAUSEUS 128
PORTB=%00110100: PAUSEUS 82 :       PORTB=%00010100: PAUSEUS 118
PORTB=%00110100: PAUSEUS 92 :       PORTB=%00010100: PAUSEUS 108
PORTB=%00110100: PAUSEUS 102 :      PORTB=%00010100: PAUSEUS 98
PORTB=%00110100: PAUSEUS 111 :      PORTB=%00010100: PAUSEUS 89
PORTB=%00110100: PAUSEUS 120 :      PORTB=%00010100: PAUSEUS 80
PORTB=%00110100: PAUSEUS 128 :      PORTB=%00010100: PAUSEUS 72
PORTB=%00110100: PAUSEUS 136 :      PORTB=%00010100: PAUSEUS 64
PORTB=%00110100: PAUSEUS 143 :      PORTB=%00010100: PAUSEUS 57
PORTB=%00110100: PAUSEUS 150 :      PORTB=%00010100: PAUSEUS 50
PORTB=%00110100: PAUSEUS 156 :      PORTB=%00010100: PAUSEUS 44
PORTB=%00110100: PAUSEUS 162 :      PORTB=%00010100: PAUSEUS 38
PORTB=%00110100: PAUSEUS 166 :      PORTB=%00010100: PAUSEUS 34
PORTB=%00110100: PAUSEUS 170 :      PORTB=%00010100: PAUSEUS 30
PORTB=%00110100: PAUSEUS 173 :      PORTB=%00010100: PAUSEUS 27
```

```
PORTB=%00110100: PAUSEUS 175 :      PORTB=%00010100: PAUSEUS 25
PORTB=%00110100: PAUSEUS 177 :      PORTB=%00010100: PAUSEUS 23
PORTB=%00110100: PAUSEUS 179 :      PORTB=%00010100: PAUSEUS 21
PORTB=%00110100: PAUSEUS 180 :      PORTB=%00010100: PAUSEUS 20
PORTB=%00110100: PAUSEUS 180 :      PORTB=%00010100: PAUSEUS 20
PORTB=%00110100: PAUSEUS 179 :      PORTB=%00010100: PAUSEUS 21
PORTB=%00110100: PAUSEUS 177 :      PORTB=%00010100: PAUSEUS 23
PORTB=%00110100: PAUSEUS 175 :      PORTB=%00010100: PAUSEUS 25
PORTB=%00110100: PAUSEUS 173 :      PORTB=%00010100: PAUSEUS 27
PORTB=%00110100: PAUSEUS 170 :      PORTB=%00010100: PAUSEUS 30
PORTB=%00110100: PAUSEUS 166 :      PORTB=%00010100: PAUSEUS 34
PORTB=%00110100: PAUSEUS 162 :      PORTB=%00010100: PAUSEUS 38
PORTB=%00110100: PAUSEUS 156 :      PORTB=%00010100: PAUSEUS 44
PORTB=%00110100: PAUSEUS 150 :      PORTB=%00010100: PAUSEUS 50
PORTB=%00110100: PAUSEUS 143 :      PORTB=%00010100: PAUSEUS 57
PORTB=%00110100: PAUSEUS 136 :      PORTB=%00010100: PAUSEUS 64
PORTB=%00110100: PAUSEUS 128 :      PORTB=%00010100: PAUSEUS 72
PORTB=%00110100: PAUSEUS 120 :      PORTB=%00010100: PAUSEUS 80
PORTB=%00110100: PAUSEUS 111 :      PORTB=%00010100: PAUSEUS 89
PORTB=%00110100: PAUSEUS 102 :      PORTB=%00010100: PAUSEUS 98
PORTB=%00110100: PAUSEUS 92 :       PORTB=%00010100: PAUSEUS 108
PORTB=%00110100: PAUSEUS 82 :       PORTB=%00010100: PAUSEUS 118
PORTB=%00110100: PAUSEUS 72 :       PORTB=%00010100: PAUSEUS 128
PORTB=%00110100: PAUSEUS 62 :       PORTB=%00010100: PAUSEUS 138
PORTB=%00110100: PAUSEUS 50 :       PORTB=%00010100: PAUSEUS 150
PORTB=%00110100: PAUSEUS 40 :       PORTB=%00010100: PAUSEUS 160
PORTB=%00110100: PAUSEUS 28 :       PORTB=%00010100: PAUSEUS 172
PORTB=%00110100: PAUSEUS 16 :       PORTB=%00010100: PAUSEUS 184
PORTB=%00110100: PAUSEUS  6 :       PORTB=%00010100: PAUSEUS 194
PORTB=%00000000: PAUSEUS  1

'1st half(2)
PORTB=%11000100: PAUSEUS  6 :       PORTB=%10000100: PAUSEUS 194
PORTB=%11000100: PAUSEUS 16 :       PORTB=%10000100: PAUSEUS 184
PORTB=%11000100: PAUSEUS 28 :       PORTB=%10000100: PAUSEUS 172
PORTB=%11000100: PAUSEUS 40 :       PORTB=%10000100: PAUSEUS 160
PORTB=%11000100: PAUSEUS 50 :       PORTB=%10000100: PAUSEUS 150
PORTB=%11000100: PAUSEUS 62 :       PORTB=%10000100: PAUSEUS 138
PORTB=%11000100: PAUSEUS 72 :       PORTB=%10000100: PAUSEUS 128
PORTB=%11000100: PAUSEUS 82 :       PORTB=%10000100: PAUSEUS 118
PORTB=%11000100: PAUSEUS 92 :       PORTB=%10000100: PAUSEUS 108
PORTB=%11000100: PAUSEUS 102 :      PORTB=%10000100: PAUSEUS 98
PORTB=%11000100: PAUSEUS 111 :      PORTB=%10000100: PAUSEUS 89
PORTB=%11000100: PAUSEUS 120 :      PORTB=%10000100: PAUSEUS 80
PORTB=%11000100: PAUSEUS 128 :      PORTB=%10000100: PAUSEUS 72
PORTB=%11000100: PAUSEUS 136 :      PORTB=%10000100: PAUSEUS 64
PORTB=%11000100: PAUSEUS 143 :      PORTB=%10000100: PAUSEUS 57
PORTB=%11000100: PAUSEUS 150 :      PORTB=%10000100: PAUSEUS 50
PORTB=%11000100: PAUSEUS 156 :      PORTB=%10000100: PAUSEUS 44
PORTB=%11000100: PAUSEUS 162 :      PORTB=%10000100: PAUSEUS 38
PORTB=%11000100: PAUSEUS 166 :      PORTB=%10000100: PAUSEUS 34
PORTB=%11000100: PAUSEUS 170 :      PORTB=%10000100: PAUSEUS 30
PORTB=%11000100: PAUSEUS 173 :      PORTB=%10000100: PAUSEUS 27
PORTB=%11000100: PAUSEUS 175 :      PORTB=%10000100: PAUSEUS 25
PORTB=%11000100: PAUSEUS 177 :      PORTB=%10000100: PAUSEUS 23
PORTB=%11000100: PAUSEUS 179 :      PORTB=%10000100: PAUSEUS 21
PORTB=%11000100: PAUSEUS 180 :      PORTB=%10000100: PAUSEUS 20
PORTB=%11000100: PAUSEUS 180 :      PORTB=%10000100: PAUSEUS 20
PORTB=%11000100: PAUSEUS 179 :      PORTB=%10000100: PAUSEUS 21
PORTB=%11000100: PAUSEUS 177 :      PORTB=%10000100: PAUSEUS 23
PORTB=%11000100: PAUSEUS 175 :      PORTB=%10000100: PAUSEUS 25
```

```
PORTB=%11000100: PAUSEUS 173 :      PORTB=%10000100: PAUSEUS 27
PORTB=%11000100: PAUSEUS 170 :      PORTB=%10000100: PAUSEUS 30
PORTB=%11000100: PAUSEUS 166 :      PORTB=%10000100: PAUSEUS 34
PORTB=%11000100: PAUSEUS 162 :      PORTB=%10000100: PAUSEUS 38
PORTB=%11000100: PAUSEUS 156 :      PORTB=%10000100: PAUSEUS 44
PORTB=%11000100: PAUSEUS 150 :      PORTB=%10000100: PAUSEUS 50
PORTB=%11000100: PAUSEUS 143 :      PORTB=%10000100: PAUSEUS 57
PORTB=%11000100: PAUSEUS 136 :      PORTB=%10000100: PAUSEUS 64
PORTB=%11000100: PAUSEUS 128 :      PORTB=%10000100: PAUSEUS 72
PORTB=%11000100: PAUSEUS 120 :      PORTB=%10000100: PAUSEUS 80
PORTB=%11000100: PAUSEUS 111 :      PORTB=%10000100: PAUSEUS 89
PORTB=%11000100: PAUSEUS 102 :      PORTB=%10000100: PAUSEUS 98
PORTB=%11000100: PAUSEUS 92 :       PORTB=%10000100: PAUSEUS 108
PORTB=%11000100: PAUSEUS 82 :       PORTB=%10000100: PAUSEUS 118
PORTB=%11000100: PAUSEUS 72 :       PORTB=%10000100: PAUSEUS 128
PORTB=%11000100: PAUSEUS 62 :       PORTB=%10000100: PAUSEUS 138
PORTB=%11000100: PAUSEUS 50 :       PORTB=%10000100: PAUSEUS 150
PORTB=%11000100: PAUSEUS 40 :       PORTB=%10000100: PAUSEUS 160
PORTB=%11000100: PAUSEUS 28 :       PORTB=%10000100: PAUSEUS 172
PORTB=%11000100: PAUSEUS 16 :       PORTB=%10000100: PAUSEUS 184
PORTB=%11000100: PAUSEUS  6 :       PORTB=%10000100: PAUSEUS 194
PORTB=%00000000: PAUSEUS  1

'2nd half(2)
PORTB=%00110100: PAUSEUS  6 :       PORTB=%00100100: PAUSEUS 194
PORTB=%00110100: PAUSEUS 16 :       PORTB=%00100100: PAUSEUS 184
PORTB=%00110100: PAUSEUS 28 :       PORTB=%00100100: PAUSEUS 172
PORTB=%00110100: PAUSEUS 40 :       PORTB=%00100100: PAUSEUS 160
PORTB=%00110100: PAUSEUS 50 :       PORTB=%00100100: PAUSEUS 150
PORTB=%00110100: PAUSEUS 62 :       PORTB=%00100100: PAUSEUS 138
PORTB=%00110100: PAUSEUS 72 :       PORTB=%00100100: PAUSEUS 128
PORTB=%00110100: PAUSEUS 82 :       PORTB=%00100100: PAUSEUS 118
PORTB=%00110100: PAUSEUS 92 :       PORTB=%00100100: PAUSEUS 108
PORTB=%00110100: PAUSEUS 102 :      PORTB=%00100100: PAUSEUS 98
PORTB=%00110100: PAUSEUS 111 :      PORTB=%00100100: PAUSEUS 89
PORTB=%00110100: PAUSEUS 120 :      PORTB=%00100100: PAUSEUS 80
PORTB=%00110100: PAUSEUS 128 :      PORTB=%00100100: PAUSEUS 72
PORTB=%00110100: PAUSEUS 136 :      PORTB=%00100100: PAUSEUS 64
PORTB=%00110100: PAUSEUS 143 :      PORTB=%00100100: PAUSEUS 57
PORTB=%00110100: PAUSEUS 150 :      PORTB=%00100100: PAUSEUS 50
PORTB=%00110100: PAUSEUS 156 :      PORTB=%00100100: PAUSEUS 44
PORTB=%00110100: PAUSEUS 162 :      PORTB=%00100100: PAUSEUS 38
PORTB=%00110100: PAUSEUS 166 :      PORTB=%00100100: PAUSEUS 34
PORTB=%00110100: PAUSEUS 170 :      PORTB=%00100100: PAUSEUS 30
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PORTB=%00110100: PAUSEUS 177 :      PORTB=%00100100: PAUSEUS 23
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PORTB=%00110100: PAUSEUS 179 :      PORTB=%00100100: PAUSEUS 21
PORTB=%00110100: PAUSEUS 177 :      PORTB=%00100100: PAUSEUS 23
PORTB=%00110100: PAUSEUS 175 :      PORTB=%00100100: PAUSEUS 25
PORTB=%00110100: PAUSEUS 173 :      PORTB=%00100100: PAUSEUS 27
PORTB=%00110100: PAUSEUS 170 :      PORTB=%00100100: PAUSEUS 30
PORTB=%00110100: PAUSEUS 166 :      PORTB=%00100100: PAUSEUS 34
PORTB=%00110100: PAUSEUS 162 :      PORTB=%00100100: PAUSEUS 38
PORTB=%00110100: PAUSEUS 156 :      PORTB=%00100100: PAUSEUS 44
PORTB=%00110100: PAUSEUS 150 :      PORTB=%00100100: PAUSEUS 50
PORTB=%00110100: PAUSEUS 143 :      PORTB=%00100100: PAUSEUS 57
PORTB=%00110100: PAUSEUS 136 :      PORTB=%00100100: PAUSEUS 64
```

```
PORTB=%00110100: PAUSEUS 128 :      PORTB=%00100100: PAUSEUS 72
PORTB=%00110100: PAUSEUS 120 :      PORTB=%00100100: PAUSEUS 80
PORTB=%00110100: PAUSEUS 111 :      PORTB=%00100100: PAUSEUS 89
PORTB=%00110100: PAUSEUS 102 :      PORTB=%00100100: PAUSEUS 98
PORTB=%00110100: PAUSEUS 92 :       PORTB=%00100100: PAUSEUS 108
PORTB=%00110100: PAUSEUS 82 :       PORTB=%00100100: PAUSEUS 118
PORTB=%00110100: PAUSEUS 72 :       PORTB=%00100100: PAUSEUS 128
PORTB=%00110100: PAUSEUS 62 :       PORTB=%00100100: PAUSEUS 138
PORTB=%00110100: PAUSEUS 50 :       PORTB=%00100100: PAUSEUS 150
PORTB=%00110100: PAUSEUS 40 :       PORTB=%00100100: PAUSEUS 160
PORTB=%00110100: PAUSEUS 28 :       PORTB=%00100100: PAUSEUS 172
PORTB=%00110100: PAUSEUS 16 :       PORTB=%00100100: PAUSEUS 184
PORTB=%00110100: PAUSEUS  6 :       PORTB=%00100100: PAUSEUS 194
PORTB=%00000000: PAUSEUS  1
Return
```

APPENDIX B

MATLAB CODE FOR GENERATING HPWM LOOKUP TABLES

```
%A program to calculate switching instant of
%Sinusoidal Pulse Width Modulation for PIC proggramming.
%By: Muhammad Faizal Bin Abdullah
%Date: 5 June 2012

%PART I (intro)
%All the interface is cleared include functions, figures, and
variables.
%The name of the program is displayed.
clc
clear all
display('Switching instant of Sinusoidal Pulse Width Modulation for
PIC programming')
disp('    ')

%PART II (user interface)
%In this part, user is asked to enter variables
f=input('The frequency of Sinusoidal waveform, f = ');
fs=input('The frequency of sawtooth waveform, fs = ');
ma=input('The modulation index, ma, (0<ma<1), ma = ');
Vs_rms_pu=1;
N=(1/f)/(1/fs);

%PART III (calculation)
%Bilding th sawtooth waveform,Vt, the input voltage,Vin,
%the output voltage waveform,Vout, and finding switching instant
%between alpha(beginning) and beta(the end).
for k=1:2*N
    for j=1:50
        i=j+(k-1)*50;
        wt(i)=i*pi/(N*50);
        Vs(i)=sqrt(2)*Vs_rms_pu*sin(wt(i));
        ma1(i)=ma*abs(sin(wt(i)));

        if rem(k,2)==0
            Vt(i)=0.02*j;
            if abs(Vt(i)-ma*abs(sin(wt(i))))<=0.011
                m=j;
                beta(fix(k/2)+1)=3.6*((k-1)*50+m)/N;
            else
                j=j;
            end

        else
            Vt(i)=1-0.02*j;
            if abs(Vt(i)-ma*abs(sin(wt(i))))<0.011
                l=j;
                alpha(fix(k/2)+1)=3.6*((k-1)*50+l)/N;
            else
                j=j;
            end
        end
```

```
        if Vt(i)>ma*abs(sin(wt(i)))
            Vout(i)=0;
        else
            Vout(i)=Vs(i);
        end
    end
end
beta(1)=[];
w=beta-alpha;
width=(w/360)*0.02;
tON=width*1e6;
tOFF=100-tON;
disp('    ')
n=0;
while n<100;
    n=n+1;
    fprintf('PORTB=$10100001: PAUSEUS %2.0f :\t',
tON(n)'),fprintf('PORTB=$00100001: PAUSEUS %2.0f \n', tOFF(n)')
end
```