ACS APPLIED MATERIALS & INTERFACES

Research Article

Cite This: ACS Appl. Mater. Interfaces 2019, 11, 29022−29028

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Temperature-Dependent Opacity of the Gate Field Inside MoS_2 Field-Effect Transistors

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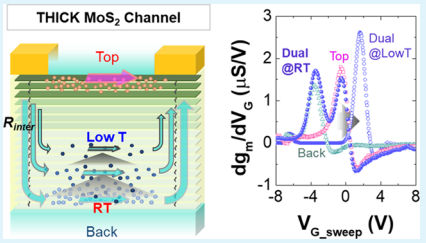
Supporting Information

ABSTRACT: The transport behaviors of MoS_2 field-effect transistors (FETs) with various channel thicknesses are studied. In a 12 nm thick MoS_2 FET, a typical switching behavior is observed with an I_{on}/I_{off} ratio of 10^6. However, in 70 nm thick MoS_2 FETs, the gating effect weakens with a large off-current, resulting from the screening of the gate field by the carriers formed through the ionization of S vacancies at 300 K. Hence, when the latter is dual-gated, two independent conductions develop with different threshold voltage (V_{TH}) and field-effect mobility (μ_{FE}) values. When the temperature is lowered for the latter, both the ionization of S vacancies and the gate-field screening reduce, which revives the strong I_{on}/I_{off} ratio and merges the two separate channels into one. Thus, only one each of V_{TH} and μ_{FE} are seen from the thick MoS_2 FET when the temperature is less than 80 K. The change of the number of conduction channels is attributed to the ionization of S vacancies, which leads to a temperature-dependent intra- and interlayer conductance and the attenuation of the electrostatic gate field. The defect-related transport behavior of thick MoS_2 enables us to propose a new device structure that can be further developed to a vertical inverter inside a single MoS_2 flake.



KEYWORDS: *MoS_2, S vacancies, interlayer coupling, temperature-dependent gate-field attenuation, dual-gated transistor*

INTRODUCTION

Transition metal dichalcogenides (TMDs) provide a wide variety of material compositions and exhibit a variety of material properties, including metal, semimetal, magnetic, superconductor, and semiconductor properties.[1−4] The physics of these materials is rich. Among them, semiconducting TMDs (s-TMDs) have emerged as new candidates for ushering in the post-Si era. The band gap of a single layer ranges around 1−2 eV, which is comparable to that of Si.[5−7] However, what is more important is the existence of a direct band in a single layer of MoS_2 and WS_2. This enables light emission and opens the possibility for their use in optoelectronic devices. This capability is absent in Si devices.[8,9] An indirect band is observed in the bulk. Hence, the strong photoluminescence from monolayer MoS_2 and WS_2 is a consequence of the absence of layer-to-layer interactions. The result indicates that layer-to-layer interactions in TMDs play a significant role and must be taken into consideration when they are applied in various devices.

In addition, the electrical properties of s-TMDs depend on the number of layers. For instance, the highest carrier mobility is obtained for a thickness of 10 nm, rather than a monolayer.[10−13] In multilayers, the penetration of the gate field and layer-to-layer carrier flow plays a significant role in the transport. This indicates that the device performance can be optimized by controlling the number of layers in s-TMDs. In layered s-TMDs, carrier transport is highly asymmetric, that is, a much higher electrical conductivity is obtained for the in-plane direction compared to the out-of-plane direction. As the thickness increases, in contrast to lateral transport, the portion of vertical transport in carrier conduction weighs more together with electrostatic screening because, in multilayer s-TMD devices, source/drain electrodes are formed on the topmost layer. Thus, carrier injection occurs from the top layers.[10,14] The application of a back-gate field induces carrier attraction toward to the bottom layers. Hence, different carrier polarities and concentrations could be found between the top and bottom layers of thick TMDs.[15] What makes the understanding of transport behavior in thick TMDs more difficult is that the carrier across different layers in s-TMDs is

Received: April 17, 2019
Accepted: July 17, 2019
Published: July 17, 2019

DOI: 10.1021/acsami.9b06715
ACS Appl. Mater. Interfaces 2019, 11, 29022−29028

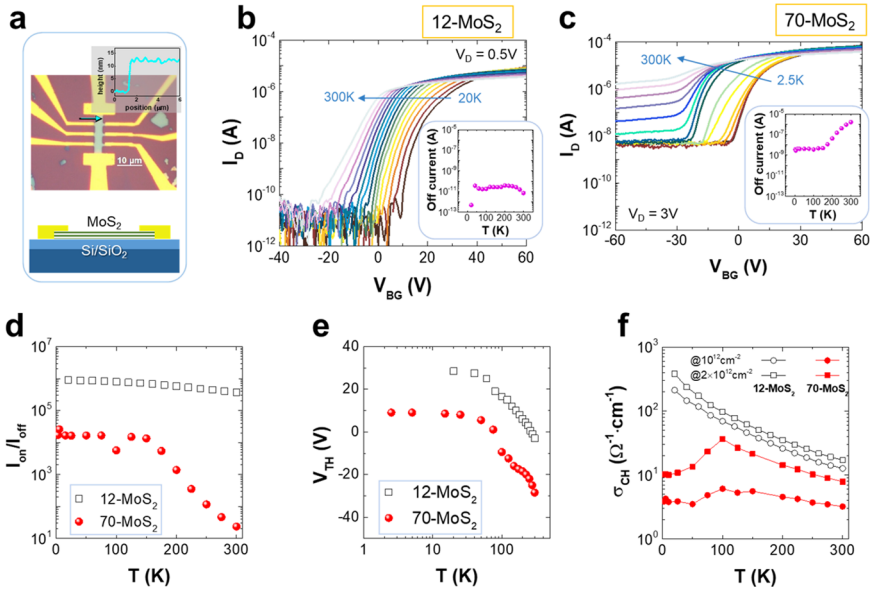


Figure 1. (a) Optical image of the Hall bar structure of a 12-MoS_2 FET with the MoS_2 height profile by AFM in the inset and a schematic of the cross section. (b) I_D−V_{BG} transfer curves of the 12-MoS_2 FET as a function of temperature. The inset shows the off-current of the device. (c) I_D−V_{BG} transfer curves of 70-MoS_2 FET as a function of temperature. The inset shows the off-current of the device. (d) I_{on}/I_{off} ratio. (e) Threshold voltage V_{TH} values of the 12- and 70-MoS_2 FETs as a function of temperature. (f) Channel conductivity σ_{CH} at channel carrier densities of 1×10^{12} cm^{-2} and 2×10^{12} cm^{-2} of the 12- and 70-MoS_2 FETs as a function of temperature.

subject to variation depending on the interlayer coupling strength, which is affected by the gate-field strength, temperature, substrates, and ionization of defect sites.[10−12] Such a strong asymmetric transport behavior is absent in conventional Si devices. Using thick s-TMDs for the real device applications has been shown elsewhere, including vertical diodes and phase shifters.[15,16] However, carrier transport upon the interlayer coupling, which is highly subject to change due to the gate bias and temperature, has not been addressed in previous studies. The lack of an understanding of the effect of the van der Waals interaction between the layers on the carrier conduction in thick s-TMDs hinders the application and realization of a layered semiconductor for use in modern digital electronics. In this regard, detailing the characteristics of the vertical carrier transport, gate-field attenuation, and ionization of impurities inside TMDs are essential, but their interplays in the transport behaviors inside thick TMDs need to be studied further.

In this study, the gate-controlled vertical transport of thick MoS_2 has been explored to understand as to how interlayer conduction is affected by the thickness. We investigated the transport characteristics of MoS_2 FETs with different thicknesses, 12, 60, and 70 nm, since the calculations show that the maximum depletion depth in s-TMD FETs extends to several tens of nanometers, ∼48−55 and ∼48.5−68.5 nm, depending on the concentration of the mobile charge carriers.[17−19] The transport behaviors of the device including the threshold voltage V_{TH} and temperature-dependent mobility $\mu_{FE} \sim T^{\beta}$ are characterized. In this regard, our devices are fabricated with single or dual gates. Assuming that the doping concentration by S vacancies or other charged impurities is the same in MoS_2 of 12 and 70 nm thicknesses at 300 K, the whole channel of 12 nm thick MoS_2 is fully under the electrostatic control by the back-gate field, whereas the electrostatic control by the back gate for the surface region of the 70 nm thick MoS_2 may weaken or become almost ineffective due to dielectric screening, which is known to be approximately 5−8 nm in MoS_2.[10,1410,14] Due to the screening of free carriers released from S vacancies, at 300 K, dual-gate control of the MoS_2 channel using the top- and bottom-gate electrodes physically splits the carrier conduction inside MoS_2, that is, two separate conduction channels are located near the top- and bottom-gate dielectrics. Unlike at 300 K, at temperatures below 80 K, only a single channel conduction is observed, namely the top channel conduction. The termination of the bottom conduction channel by the back gate is expectedly owing to the increased intralayer resistance of MoS_2 by neutral S vacancies that subsequently suppresses the vertical transport. The correlation of S vacancy-affected screening and interlayer resistance changes with temperature and causes significant change of V_{TH} and μ_{FE} as the temperature decreases.

RESULTS AND DISCUSSION

Device Characterization for Single-Gated Thin and Thick MoS_2 FETs. A single-gated (SG) MoS_2 FET was constructed on a SiO_2 (300 nm)/Si (500 μm) substrate where the material thickness is confirmed by atomic force microscopy (AFM) as shown in Figure 1a. To remove the contact resistance, an 8 bar structure was made on the substrate. For metal electrodes, Cr (5 nm)/Au (60 nm) were deposited inside an electron-beam evaporator. In addition, a dual-gated (DG) FET for 60 nm thick MoS_2 with a symmetric gate dielectric was fabricated using h-BN layers on the same Si substrate. The images of the structure and measurement configuration for the dual-gated MoS_2 FET are shown in Figure S1. Details of the fabrication and characterization of all devices are described in the Experimental Methods.

Transfer curves of the 12 nm thick MoS_2 FET, referred to as 12-MoS_2 FET, was characterized with a back-gate bias varying from −40 to 60 V as a function of temperature, as shown in Figure 1b. The device exhibits a metal−insulator transition (MIT) depending on the back-gate bias, which is attributed to S vacancies.[20] The population of mono- or bi-vacancies of S

DOI: 10.1021/acsami.9b06715
ACS Appl. Mater. Interfaces 2019, 11, 29022−29028

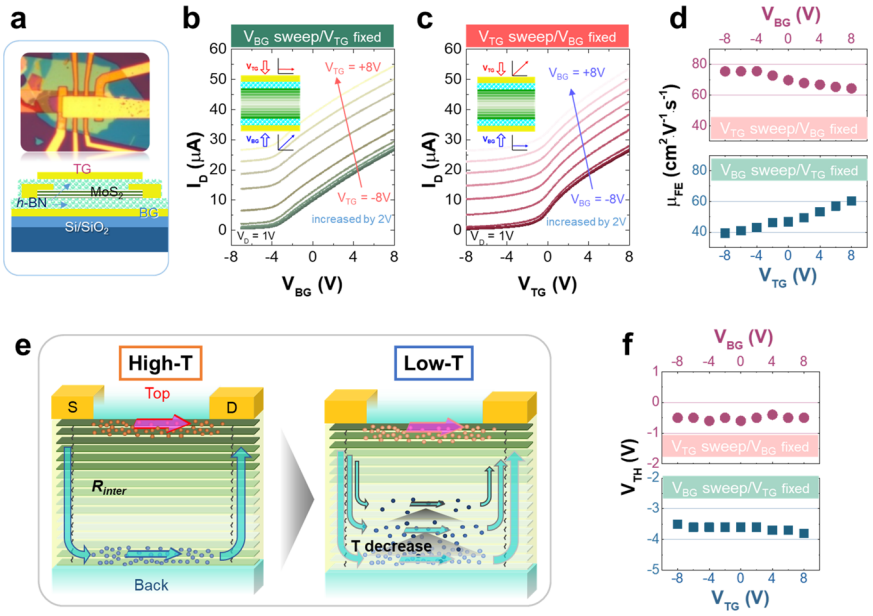


Figure 2. (a) Optical image of a 60-MoS_2 dual-gated FET and a schematic of the cross section. Transfer curves of the dual-gated 60-MoS_2 FET under (b) sweeping back gate at a fixed top-gate bias, V_{BG}^{TG}, and (c) sweeping top-gate at a fixed back-gate bias, V_{TG}^{BG}. (d) Peak field-effect mobility μ_{FE} of the dual-gated 60-MoS_2 FET under the operation of V_{TG}^{BG} and V_{BG}^{TG}. (e) Schematic of the carrier conduction in the 60-MoS_2 dual-gated FET depending on the temperature. (f) Threshold voltage V_{TH} of the dual-gated 60-MoS_2 FET under the operation of V_{TG}^{BG} and V_{BG}^{TG}.

atoms is over approximately 8×10^{13} cm^{-2} and their energy level locates only about 15 meV below the conduction band edge.[21,22] At 300 K, a considerable number of S defect sites are supposed to release electrons into the conduction band, leading to the n-type doping of MoS_2.[23−25] Thus, as the temperature lowers, S vacancies are deionized. In addition to S vacancies, other sources of n-type doping of MoS_2 have been theoretically proposed elsewhere.[26,27] The detailed doping mechanism of MoS_2 requires future studies. The channel current I_D is approximately 10^{-11} A in the inset of Figure 1b and ranges over a few microamps for the off- and on-states, respectively. An I_{on}/I_{off} ratio of approximately 10^6 is achieved within our temperature range from 12-MoS_2 FET, as exhibited in Figure 1d, although the V_{TH} shifts from −3 V at 300 K to 28.5 V at 20 K. The variation of the corresponding charge density is 2.3×10^{12} cm^{-2} in the channel. In contrast to 12-MoS_2 FET, stark differences are observed when 70 nm thick MoS_2 FET, referred to as 70-MoS_2 FET, is characterized. One of the important features of 70-MoS_2 FET is a large off-current at 300 K, and the temperature dependence of I_{off} is quite sensitive, although such a behavior is not seen in 12-MoS_2 FET, that is, the I_{off} gradually decreases from the microamp range and saturates at the nanoamp range, when the temperature lowers from 300 to 2.5 K, as shown in the inset of Figure 1c (see Figure S2 for the leakage currents of 12- and 70-MoS_2 FETs). Unlike the switching behavior of 12- and 70-MoS_2 FETs, both devices experience a similar shift of V_{TH}. It changes toward a positive bias in Figure 1e with decreasing temperature. The *n* doping reduces at low temperatures. From the temperature-dependent V_{TH} in Figure 1e, a larger shift is observed in the 70-MoS_2 FET than in the 12-MoS_2 FET. This implies that the number of channel carriers varies faster in the 70-MoS_2 FET than in the 12-MoS_2 FET with temperature (see Figure S3 for temperature-dependent carrier densities). Together with the S vacancy-affected switching behavior of the devices, we propose another possibility that can partially or equally contribute to the device properties shown in Figure 1b,c. Figure 1f presents the channel conductivity σ_{CH} of two FETs at a given carrier concentration *n*. In the case of the 12-MoS_2 FET, σ_{CH} is inversely proportional to the temperature, exhibiting a metallic behavior, whereas in the 70-MoS_2 FET, it exhibits a semiconducting trait, whereby σ_{CH} increases with temperature up to 100 K and then metallic characteristics appear from 100 to 300 K. In the figure, the carrier concentration is fixed. Because V_{TH} changes depending on the temperature, for an easy comparison, we plot $\sigma_{CH}-T$ in Figure 1f at the same carrier concentrations, 1×10^{12} cm^{-2} and 2×10^{12} cm^{-2}. We propose that a stark difference in the conductivity σ is found depending on the carrier flow direction. The channel conductivity σ_{CH} is proportional to μ, which can be written further as $\mu = q \cdot \tau \cdot m^{*-1}$. Here, m* is the effective mass of the carrier, which shows a directional dependence. The effective mass in the vertical direction $m_{\perp}^{*}$ is even larger than its in-plane counterpart $m_{\parallel}^{*}$.[28] In a thicker flake, the portion of the out-of-plane carrier flow becomes higher, resulting in a degradation of μ, which is be discussed further in Figure 2. The vertical carrier flow is affected by the layer conductance itself and by layer-to-layer conductance. The screening or penetration of the back-gate field in the vertical direction is expected to influence the interlayer interaction.[14,29] Therefore, the exotic $\sigma_{CH}-T$ curve at a given carrier concentration is an outcome of the interplay of doping, interlayer coupling strength, and screening of the back-gate field.

Two Independent Channels of Thick MoS_2 at Room Temperature. To study the effect of the interplay of the screening of the gate field, interlayer coupling, intralayer conductance, and ionization of S vacancies or other impurities on the performance of MoS_2 FETs, we fabricated a dual-gated MoS_2 FET using 30 nm thick h-BN for the top and bottom dielectrics as shown in Figure 2a. Details of the device structure and fabrication procedures are presented in Figure S1. We regulated the conductance of the 60 nm thick MoS_2 channel using top and bottom gates. Figure 2b,c demonstrate transfer curves I_D-V_G, in which different modes of gate bias

DOI: 10.1021/acsami.9b06715
ACS Appl. Mater. Interfaces 2019, 11, 29022−29028

sweep were applied. For instance, in Figure 2b, the back-gate bias was swept at a fixed top-gate bias, whereas the top-gate bias was swept at a fixed back-gate bias in Figure 2c. Each gate sweep was nomenclatured as $V_{G\_sweep}^{G\_fixed}$; therefore V_{BG}^{TG} refers to Figure 2b and V_{TG}^{BG} refers to Figure 2c. In these operations, the sweeping gate was increased from −8 to +8 V with a 0.1 V step and the fixed gate bias was increased by 2 V from −8 to +8 V. Refer to Figure S4 for the synchronized modulation of both top and bottom gates, called as the symmetric dual-gate sweep and coined as V_{DG}.

In the asymmetric gate sweep in Figure 2b, the transfer curve measured at 300 K shows the V_{TH} at V_{BG} = −3.5 V with V_{TG} = −8 V. As the top-gate bias increases, the transfer curves are upshifted with a higher I_{off}. With an increasing I_{off}, the I_{on}/I_{off} ratio drops lower from an order of 10^2 at V_{TG} = −8 V to a few factors at V_{TG} = +8 V. On the same device, the top-gate bias is swept at a given back-gate bias, as shown in Figure 2c. The increase of I_{off} and weakening of the I_{on}/I_{off} ratio are reproduced with an ascending fixed back-gate bias in Figure 2c. A much higher V_{TG} is required to turn on the channel. Nearly V_{TG} = 0 V is needed to bring the device to the on-state compared to V_{BG} = −3.5 V from the V_{BG}^{TG} sweep. In addition, a smaller I_{on}/I_{off} ratio is regenerated with a higher V_{BG}. The reduction of the gating effect at a high fixed gate bias in Figure 2b,c is caused by the attenuation of the gate field by the doping of the channel near the fixed gate bias. It is also interesting to note that different turn-on voltages are observed depending on the gate-sweep mode.

To evaluate the device performance, the I_D−V_G curves acquired at different fixed gate bias in Figure 2b,c were studied further by evaluating the device parameters. The transconductance expressed as

$$g_m = \frac{\Delta I_D}{\Delta V_G} = \frac{\mu_{FE} \cdot C_{OX} \cdot W}{L} V_D \quad (1)$$

from each gate sweep in Figure 2b,c is obtained as shown in the transconductance curves in Figure S5. Here, C_{OX} is the gate dielectric capacitance per unit area[30] and μ_{FE} is the field-effect carrier mobility. The evaluation indicates that the peak position and height of the g_m−V_G curves for V_{TG}^{BG} and V_{BG}^{TG} slightly vary depending on different fixed gate bias, V^{G_fixed}, which are shown in Figure S5. Using Figure S5, we can characterize μ_{FE} from a four-probe measurement using eq 1 as a function of V^{G_fixed}. Figure 2d summarizes the shift of the peak value of μ_{FE} at different values of V^{G_fixed}. The peak values of μ_{FE} are considerably different for V_{TG}^{BG} and V_{BG}^{TG} and furthermore, the trend of the peak values of μ_{FE} with respect to V^{G_fixed} is opposite. At a low V^{G_fixed}, the peak μ_{FE} was determined to be 39.4 $cm^2\ V^{-1}\ s^{-1}$ for V_{BG}^{TG} and 75.4 $cm^2\ V^{-1}\ s^{-1}$ for V_{TG}^{BG}, whereas at high V^{G_fixed}, an almost similar value of approximately 60 $cm^2\ V^{-1}\ s^{-1}$ is observed for both V_{BG}^{TG} and V_{TG}^{BG}. It is interesting to note that under V_{TG}^{BG} sweep, μ_{FE} gradually decreases with increasing V^{G_fixed}, although the opposite behavior is observed from the V_{BG}^{TG} operation.

We propose that the stark contrast in the dependence of μ_{FE} on V^{Ghe_fixed} in Figure 2d originates from the different carrier conducting paths in a MoS_2 flake between V_{TG}^{BG} and V_{BG}^{TG} sweeps, which is invoked by the device geometry. In our device, source/drain electrodes touch the topmost layer of the MoS_2 flake. Therefore, the carriers are always injected into the topmost layers. During the V_{TG}^{BG} sweep, the increase of the fixed back gate suppresses μ_{FE}. We attribute the reducing μ_{FE} in V_{TG}^{BG} to the deflection of the conduction channel by the fixed back gate. With an increasing back-gate bias, the carriers are attracted toward the bottom gate and travel in the out-of-plane direction with regard to MoS_2 (cyan arrow) as shown in Figure 2e. The out-of-plane transport in V_{TG}^{BG} keeps growing with increasing V^{G_fixed}, in which direction the carrier mobility is very low, compared to that in the in-plane direction (magenta arrow).

However, μ_{FE} keeps increasing with a fixed gate bias, when the device is under the V_{BG}^{TG} sweep mode. In this mode, the carriers from the source electrode enter the top MoS_2 layers and flow down toward the bottom MoS_2 layers due to the bottom-gate bias, as shown in Figure 2e. At low V^{G_fixed}, electron carriers toward the bottom gate are repelled by the top gate. Because of the anisotropic electrical resistivity of MoS_2, the carriers will possess a much lower mobility in the out-of-plane direction than in the in-plane flow.[11,15,29] This is the reason that μ_{FE} from V_{BG}^{TG} is always lower than μ_{FE} from V_{TG}^{BG}. With a stronger top-gate bias, the carriers injected into the channel are pulled toward the top gate, leading to the decrease of vertical flow. Thus, μ_{FE} continues to increase with a higher top-gate bias. Refer to S5 for the carrier mobility for symmetric dual sweep.

Together with the change of the conduction path by V^{G_fixed}, we would like to address the role of the interlayer resistance R_{inter} in Figure 2e. For MoS_2, it is estimated to be R_{inter} = 2.0−2.4 kΩ μm.[10,14,31] In addition, R_{inter} modulates depending on the degree of interlayer coupling and the intralayer resistance, both of which can be controlled by the gate bias.[10,14] A lower R_{inter} value could occur at a higher gate bias due to a stronger layer-to-layer coupling and lower intralayer resistance. Therefore, at a higher gate bias, carrier conduction in the vertical direction becomes easier such that the R_{CH} dependence on T is much more stronger, as evidenced in Figure 1f, that is, a high carrier concentration gives rise to a lower R_{CH} under a bottom-gate sweep.

In addition, we investigate the threshold voltage V_{TH} among different gate-sweep modes by taking the derivative of g_m with respect to $V_{G\text{-}sweep}$,[32−34] which is shown in Figure S6. The V^{G_fixed}-dependent V_{TH} is shown in Figure 2e for both V_{BG}^{TG} and V_{TG}^{BG}, respectively. It is revealed that our device operates at different V_{TH} values depending on gate-sweep mode: V_{TH} = −3.5 V for V_{BG}^{TG} and V_{TH} = −0.5 V for V_{TG}^{BG}. The lower value of V_{TH} coincides with the early turn-on of the device, shown in Figure 2a. What should be emphasized here is that compared to μ_{FE}, V_{TH} does not change significantly depending on V^{G_fixed}. The experimental results in Figure 2f support the fact that the fixed gate bias is not capable of controlling the nature of the junction between MoS_2 and the metal electrode. We think that at room temperature and with thick MoS_2, the fixed gate is local, and not global. It can control only the interlayer resistance to some extent in the vertical direction. If this is the case, then when the device is in dual sweep at the same time, two independent channels can be formed in a 60-MoS_2 FET.[35−37] As predicted, two peaks emerge in the g_m−V_G curve from the device under V_{DG} in Figure S6a. The result indicates that the two separate channels are in concurrent operation in MoS_2, which are spatially segregated inside a single thick MoS_2 flake.

Temperature-Dependent Conduction in Thick MoS_2 DG FETs. Inside the 60-MoS_2 FET, spatially divided channels are substantially developed, and such a channel formation is strongly affected by the interlayer resistance and screening. It is

DOI: 10.1021/acsami.9b06715
ACS Appl. Mater. Interfaces 2019, 11, 29022−29028

important to note that in this course, the ionization of S vacancies or other impurities is expected to play a significant role, defining how the intralayer resistance and the screening of the gate field are involved in the gating effect of the thick MoS_2 layer. We conducted a temperature-dependent transport study of the 60-MoS_2 FET to determine how the two different channels formed by the dual sweep are affected by the parameters mentioned above. The dual-sweep V_{DG} of the 60-MoS_2 FET was studied as a function of temperature with the electrical configuration as shown in the inset of Figure 3a.

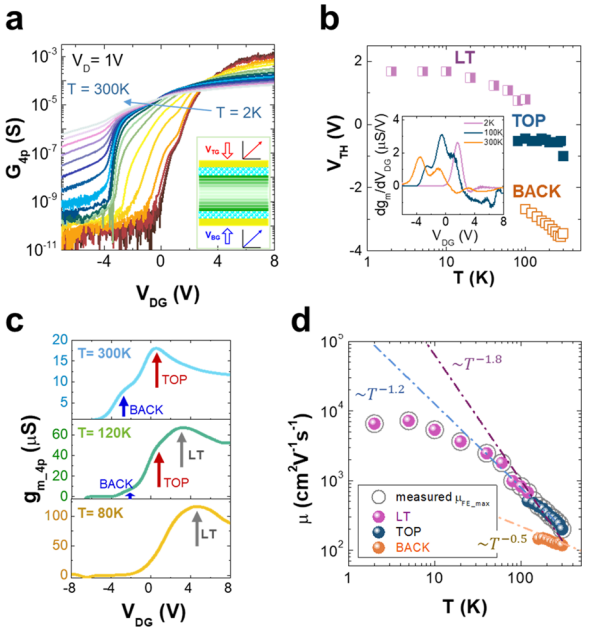


Figure 3. (a) Temperature-dependent transfer curves of G_{4p}–V_{DG} for the dual-gated 60-MoS_2 FET under symmetric DG sweeps as a function of temperature. (b) Threshold voltage V_{TH} of the 60-MoS_2 DG FET as a function of temperature. The inset shows the dg_m/dV_{DG}–V_{DG} curves for various temperatures. (c) $g_{m\text{-}4p}$–V_{DG} plots as a function of temperature. (d) Temperature-dependent field-effect mobility μ_{FE} plots and their power-law fits.

Under the V_{DG} mode, G_{4p}–V_{DG} curves are plotted at temperatures ranging from 300 to 2 K in Figure 3a, where G_{4p} is the channel conductance from the four-probe measurement (see Figure S7 for MIT). However, we propose another probable mechanism for the MIT in Figure 3a that has an origin in the dual-channel transport behavior in MoS_2, where two different transport channels are opened or closed depending on temperature, which will be further discussed below.

The I_D–V_{DG} curves of the 60-MoS_2 FET in Figure 3a were further analyzed. The temperature-dependent V_{TH} curves in Figure 3b demonstrate two different V_{TH} values at 300 K, V_{TH} = −3.5 and −0.5 V (see Figure S8 for the extraction of V_{TH}), a signature of the existence of two separate channels. The V_{TH} values were extracted according to the dg_m/dV_G method detailed in S8, and the graph for three temperatures of 2, 100, and 300 K in the inset are shown as examples. The two-channel conductions of the 60-MoS_2 FET exist when T > 80 K, but a single channel is seen when T < 80 K together with a gradual shift of V_{TH} from V_{TH} = 0.92 V at 80 K to 1.68 V at 2 K. The conduction initiated with V_{TH} = −3.5 V at 300 K, activated by the bottom-gate bias, experiences growing interlayer resistance as the electrical conductivity of each semiconducting MoS_2 layer and the band overlap of each layer reduce at low temperatures.[38,39] Thus, it is assumed that the channel by the bottom-gate bias at around room temperature is not able to maintain the conducting path and could be very shallow at low temperatures, as shown in Figure 2e (cyan arrow). However, the effect of the interlayer resistance at low temperatures is not significant for the top-gate bias, because the carrier flows through the top layers. Thus, the distinct separation of the carrier conduction path at low temperatures may be prohibited by the interlayer resistance, which could contribute to a single V_{TH} in Figure 3b at temperatures below 80 K. Hence, at low temperatures, the top-channel conduction governs the 60-MoS_2 FET because the growing vertical resistance confines the carriers near top layers.

The temperature-dependent conduction channel formation is further characterized. In addition to V_{TH}, the dependence of the carrier mobility in each channel on temperature is analyzed. Prior to the extraction of μ_{FE}, g_m–V_{DG} curves are obtained as a function of temperature, as shown in Figure 3c, whose shape evolves as a function of temperature. The peak value in the g_m–V_{DG} curve corresponds to the maximum μ_{FE} value. The g_m–V_{DG} curves from 300, 120, and 80 K are shown in Figure 3c. At 300 K, the two peaks indicated by arrows are observed in the g_m–V_{DG} curve a little after V_G = −3.5 and −0.5 V, which are consistent with independent conduction in the bottom and top channels as described in Figure 2. However, at 120 K, the former (referred to as back) after V_{DG} = −3.5 V begins to deflate, whereas the latter (referred to as top) after V_{DG} = −0.5 V inflates. Moreover, another peak at V_{DG} > 2 V appears at low temperatures (marked as "LT" in Figure 3b,d). When the temperature reaches 80 K, only a single peak is evident in the bottom g_m–V_{DG} plot of Figure 3c.

The temperature dependence of the mobility is summarized in Figure 3d. The overall temperature dependence of the carrier mobility is that it increases from 50.6 $cm^2\ V^{-1}\ s^{-1}$ at 300 K as the temperature decreases and then saturates at approximately ~1.6 × 10^3 $cm^2\ V^{-1}\ s^{-1}$ below 10 K. The higher carrier mobility at low temperatures is attributed to the suppression of scattering by optical phonons, a dominant scattering source at room temperature but vanishing at low temperatures.[39] What is more important is the existence of the two separate channel mobilities at 300 K with a distinct temperature dependence $\mu \sim T^{-\beta}$: $\mu \sim T^{-0.5}$ for the bottom channel and $\mu \sim T^{-1.2}$ for the top channel. The channel developed by the back-gate bias has a low carrier mobility and fades out at temperatures below 100 K. A value of β = 0.5 was observed in a previous study,[40] but we consider that the origin is different. From this channel, a weak temperature dependence is probably attributed to either a fast-growing interlayer resistance or to a different power-law behavior of carrier mobility in the out-of-plane direction. In the case of the top channel, a careful examination of the power-law dependence of μ_{FE} on the temperature reveals a slight deflection of the slope in Figure 3d. For instance, between 100 and 300 K, the mobility scales as $\mu_{FE} \sim T^{-1.2}$, and then, it changes to $\mu_{FE} \sim T^{-1.8}$ when the temperature is lower than 100 K. In MoS_2 FETs, optical phonon-mediated carrier-scattering exhibits values of $1 < \beta < 2$,[40−42] whereas an even greater value of β = 2.6 is reported from a bulk MoS_2 at the temperature T above 300 K.[43,44] Since, in our device, the channel thickness is rather high, the influence of the substrate is expected to be minimal. The variations of the slope in Figure 3d imply that the degree

DOI: 10.1021/acsami.9b06715
ACS Appl. Mater. Interfaces 2019, 11, 29022−29028

of involvement of the vertical transport in the overall carrier conduction on the channel is subject to change owing to the temperature and gate bias. The conduction inside bulk MoS_2 is much more sensitive and dynamic with respect to temperature than the present understanding. Within the framework of the complicated interaction of the ionization of S vacancies or other impurities, the penetration of the gate field, intralayer conductance, and interlayer coupling strength, it is possible to postulate that MIT in Figure 3a could be responsible for the collateral consequence of the intermixed interactions among the S vacancy or impurity ionization, interlayer resistance, gate-field screening, and the variation of the number of conduction channels.[45,46] Systematic studies on bulk MoS_2 are essential for understanding the intrinsic transport properties.

CONCLUSIONS

In summary, unlike conventional semiconducting nanomaterials, the layered structure of s-TMD exhibits an exotic physical property, namely separated transport of carriers in the channel owing to the interplay of temperature-dependent attenuation of the gate field and out-of-plane resistance. Such a property can be further developed for use in a resistive-load vertical inverter if the top and bottom layers can be independently controlled by a dual-gated device structure. The incorporation of s-TMDs into various unprecedented device structures and their operation requires profound understanding of the fundamental behavior of carrier transport in these materials.

EXPERIMENTAL METHODS

Device Fabrication and Characterization of Single-Gated and Dual-Gated MoS_2 FETs. The fabrication of a single-gated multilayer MoS_2 FET follows the typical nanodevice fabrication processes. After mechanical exfoliation of multilayered MoS_2 flakes from the bulk onto a Si/SiO_2 (with a thickness of 500 μm/300 nm) substrate, the proper sample flakes were confirmed by a thickness investigation by atomic force microscopy (AFM). Through the conventional electron beam (e-beam) lithography technique, the electrodes were created, and the metal deposition of Cr/Au = 5/50 nm using the e-beam evaporation was followed. The back-gate voltage is applied through the heavily doped silicon.

In the case of a dual-gated MoS_2 FET, to implant a symmetric-gate dielectric onto the device, we deposit a thin Au film on the top of a SiO_2 layer. Specifically, Cr and Au layers are deposited inside an e-beam evaporator with thicknesses of 5 and 20 nm, respectively. The back-gate electrode is approximately 20 μm in length and 10 μm in width. Subsequently, a mechanically exfoliated h-BN flake was transferred to the bottom-gate electrode via a dry transfer process. The AFM images in the middle inset of Figure S1a show that the h-BN back-gate dielectric exhibits a thickness of approximately 30 nm and an area of approximately 34 μm × 35 μm. The MoS_2 channel is then formed by locating a thick flake inside the h-BN back-gate dielectric as well as the back-gate electrode. The thickness of the MoS_2 channel is approximately 59 nm as shown in the middle inset of the right panel in Figure S1a. This type of a thick MoS_2 flake is selected to independently control the carrier conduction in TMD films by both gate fields. We construct a Hall bar-type device containing 6 Cr (5 nm)/Au (60 nm) electrodes connected to the top surface of the MoS_2 channel as shown in the bottom inset of Figure S1a. With respect to the configuration of the top-gate electrode, another exfoliated h-BN layer with a thickness of approximately 30 nm is placed on top of MoS_2 (top inset in the right panel of Figure S1a). The area of the top-gate dielectric is approximately 32 μm × 31 μm. We adopt the same metallization process for the top-gate electrode (Cr (5 nm)/Au (60 nm)). An optical image of the symmetric dual-gated device is shown in the bottom inset of Figure S1a. Figure S1b shows an adopted bias scheme to control the transport behavior in a thick MoS_2 FET.

The electrical properties of all of the devices are examined via a B1500A semiconductor device analyzer (Keysight Technology) and a physical property measurement system (PPMS) (Quantum Design).

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsami.9b06715.

Dual-gated MoS_2 FET structure and electrical characterization (S1), gate leakage current of single-gated MoS_2 FETs (S2), carrier concentration depending on the temperature (S3), transfer curve under the symmetric dual-gate sweep (S4), transconductance characteristics (S5), extraction of V_{TH} values at room temperature (S6), metal insulator transition properties (S7), and V_{TH} extraction depending on the temperature (S8) (PDF)

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Notes

The authors declare no competing financial interest.

ACKNOWLEDGMENTS

This research was supported by the Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education (NRF-2019R1A2C1010742) of Korea and by IBS-R011-D1.

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