Electrostatically transparent graphene quantum-dot trap layers for efficient nonvolatile memory

Young Rae Kim, Yong Eun Jo, Yong Seon Shin, Won Tae Kang, Yeo Hyun Sung, Ui Yeon Won, Young Hee Lee , and Woo Jong Yu

Articles you may be interested in

Nonvolatile memory thin film transistors using CdSe/ZnS quantum dot-poly(methyl methacrylate) composite layer formed by a two-step spin coating technique
J. Appl. Phys. **112**, 034518 (2012); 10.1063/1.4745041

Electrical characteristics and operating mechanisms of nonvolatile memory devices fabricated utilizing core-shell CuInS2-ZnS quantum dots embedded in a poly(methyl methacrylate) layer
Appl. Phys. Lett. **99**, 193302 (2011); 10.1063/1.3659473

Ultra-fast switching in solution processed quantum dot based non-volatile resistive memory
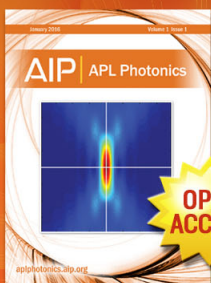Appl. Phys. Lett. **99**, 143504 (2011); 10.1063/1.3647629

All-inorganic spin-cast quantum dot based bipolar nonvolatile resistive memory
J. Appl. Phys. **109**, 086103 (2011); 10.1063/1.3573601

High-Speed and Non-Volatile Nano Electro-Mechanical Memory Incorporating Si Quantum Dots
AIP Conf. Proc. **772**, 1589 (2005); 10.1063/1.1994726

Electrostatically transparent graphene quantum-dot trap layers for efficient nonvolatile memory

Young Rae Kim,[1,a)] Yong Eun Jo,[1,a)] Yong Seon Shin,[1,2] Won Tae Kang,[1,2] Yeo Hyun Sung,[1] Ui Yeon Won,[1] Young Hee Lee,[2,3,b)] and Woo Jong Yu[1,2,b)]

[1]Department of Electronic and Electrical Engineering, Sungkyunkwan University, Suwon 440-746, South Korea
[2]Center for Integrated Nanostructure Physics, Institute for Basic Science (IBS), Sungkyunkwan University, Suwon 440-746, South Korea
[3]Department of Energy Science, BK21 Physics Division, Sungkyunkwan University, Suwon 440-746, South Korea

In this study, we have demonstrated nonvolatile memory devices using graphene quantum-dots (GQDs) trap layers with indium zinc oxide (IZO) semiconductor channel. The Fermi-level of GQD was effectively modulated by tunneling electrons near the Dirac point because of limited density of states and weak electrostatic screening in monolayer graphene. As a result, large gate modulation was driven in IZO channel to achieve a subthreshold swing of 5.21 V/dec (300 nm SiO_2 gate insulator), while Au quantum-dots memory shows 15.52 V/dec because of strong electrostatic screening in metal quantum-dots. Together, discrete charge traps of GQDs enable stable performance in the endurance test beyond 800 cycles of programming and erasing. Our study suggests the exciting potential of GQD trap layers to be used for a highly promising material in non-volatile memory devices. © 2015 AIP Publishing LLC.
[http://dx.doi.org/10.1063/1.4914306]

Graphene, with remarkable properties such as high carrier mobility,[1,2] thermal conductivity,[3] one atomic thick planner structure, and high transparency and flexibility,[4–8] exhibits exciting potential for electronic device and nonvolatile memories.[9–16] Several studies have tried to employ graphene or graphene-related materials for charge storage layer in nonvolatile memories.[17,18] Because graphene trap layer is a single continuous material; however, local defects in the tunneling oxide (TO) produce the leakage of whole trap charges in graphene trap layer by lateral charge movement, which can limit data retention and density. Recently, graphene quantum-dots (GQDs) have been suggested for a discrete charge trap layer.[19] GQDs offer an advantage of preventing lateral charge movement as a result of their lower sensitivity to local defects, thereby enhancing memory data-retention.[20] However, multi-layer GQDs in this device strongly screen the gate field and thus reduce the effect of gate modulation in energy band of semiconductor channel, while gate electric field can effectively penetrate through monolayer graphene to modulate the energy band of semiconductor channel because of the finite density of states (DOS) and weak screening effect by monolayer graphene.[21–24]

Here, we have demonstrated the non-volatile memory device with monolayer GQD trap layer. Applied gate field penetrates through ultra thin monolayer GQDs and effectively modulates the energy band of indium zinc oxide (IZO) channel. As a result, our device achieved a fast subthreshold swing of 5.21 V/dec (300 nm SiO_2 gate insulator) that is three times lower than that of Au quantum-dots (Au QDs)

memory (15.52 V/dec). Together, discrete charge traps of GQDs provide high stability in the endurance test up to 800 cycles of programming and erasing.

Figure 1 shows a schematic illustration of experimental fabrication procedure of a nonvolatile memory device with GQD trap layer. Graphene monolayer was synthesized on copper foil using a chemical vapor deposition (CVD) method,[25] and transferred on the Si/SiO_2 wafer using poly methyl methacrylate (PMMA).[26] After etching PMMA in acetone solution, 10 nm of Au film was deposited on graphene by thermal evaporation. Au film was aggregated to form Au QDs by annealing at 300 °C for 1 h in the furnace. Oxygen plasma was used to remove the exposed graphene, leaving only the graphene protected underneath the Au QDs to form GQDs.[27] Au QDs were removed by dipping in Au etchant for 3 s, and only GQDs remained on the substrate. 10 nm of Al_2O_3 layer was deposited for tunneling oxide layer using atomic layer deposition (ALD). The 60 nm of IZO semiconductor layer was formed on the GQD trap layer by spin-coating and annealing IZO solution. The IZO channel was patterned in selective area by photo-resist mask and dipping in HCl solution to remove the exposed IZO, and then photo-resist mask was removed by acetone solution. For the final step, the source and drain electrodes (Cr/Au 10/60 nm) were patterned on the IZO channel by conventional photolithography process. The SiO_2/Si substrate was used as a back gate dielectric/back gate for electrical measurements.

Figure 2(a) shows scanning electron microscope (SEM) images of Au QDs formed by thermal annealing of 10 nm Au film. The nonvolatile memory device was fabricated with Au QDs trap for the comparison with GQD trap layer. Figure 2(b) is the SEM image of the patterned GQDs by oxygen plasma etching of exposed graphene while leaving the

---

a)These authors contributed equally to this work.
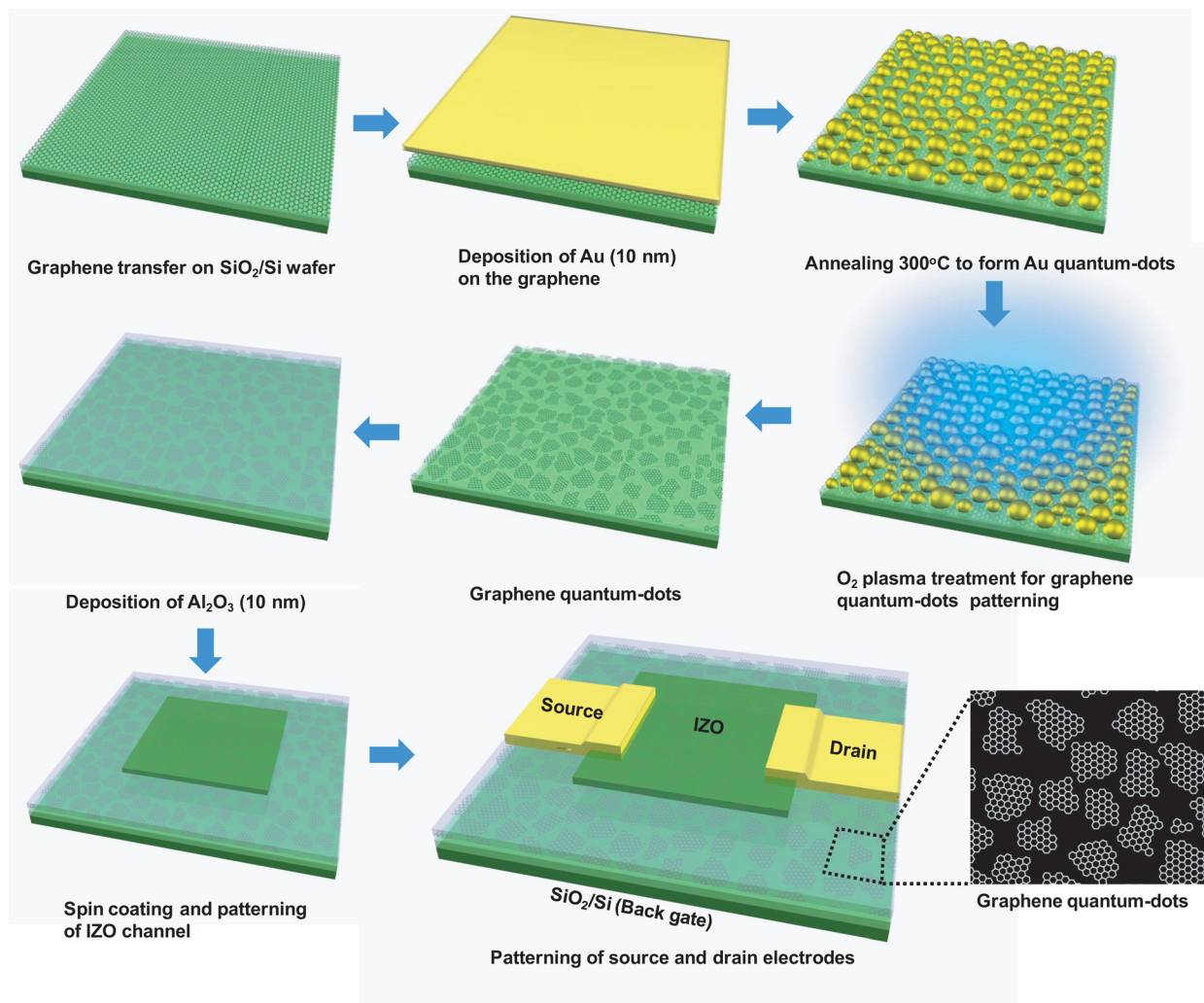b)Corresponding authors. E-mail: leeyoung@skku.edu, micco21@skku.edu

FIG. 1. Schematic illustration for the fabrication of nonvolatile memory device using GQD trap layer.

graphene protected underneath the Au quantum-dots to form GQDs. The size of the Au-QDs was measured to be about 20–30 nm and the size of GQDs is almost matched to Au quantum-dots protectors. The thickness of Au-QDs was measured by atomic force microscopy (AFM) in Figure 2(c). The thickness of Au-QDs was measured to be about

FIG. 2. SEM images of (a) Au QDs and (b) GQDs trap layer. AFM images of (c) Au QDs and (d) GQDs trap layer.

10–20 nm. In Figure 2(d), GQDs were clearly visible in AFM image with a thickness 2–3 nm. The GQDs have a thickness of 2–3 nm, which is thicker than that of monolayer graphene ($\sim$1 nm on SiO_2 substrate), because SiO_2 substrate was also etched by oxygen plasma during graphene etching process.

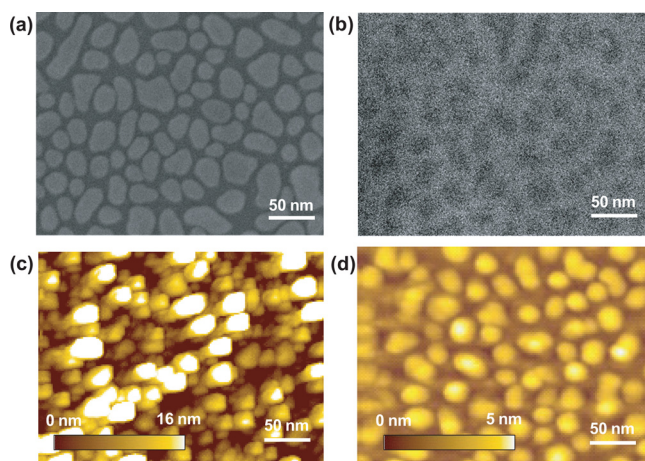Nonvolatile memory devices were fabricated by spin-coating and patterning of IZO semiconductor layer on the quantum-dots covered with tunneling Al_2O_3 layer of 10 nm (Fig. 3(a)). The source and drain electrodes were located on the IZO channel with 25 μm in width and 5 μm in length. The transfer characteristic of the IZO transistor without trap layer is shown in Figure 3(b). A small hysteresis of 15 V was observed initially which originates from defects in IZO layer and SiO_2 surface. Charge trap layer is necessary in order to construct a memory device in the present configuration. Charge storage in discrete charge traps such as metal quantum-dots instead of the commercially used polysilicon layer has been intensively studied to prevent lateral charge leakage through local defects and thus enhance memory data-stability.[19] In this study, GQDs and Au QDs are introduced for discrete charge traps. Hysteresis of IZO transistor was remarkably increased to 55 V and 60 V by the trapped charges of GQDs (red line) and Au quantum-dots (blue line), respectively (Fig. 3(c),
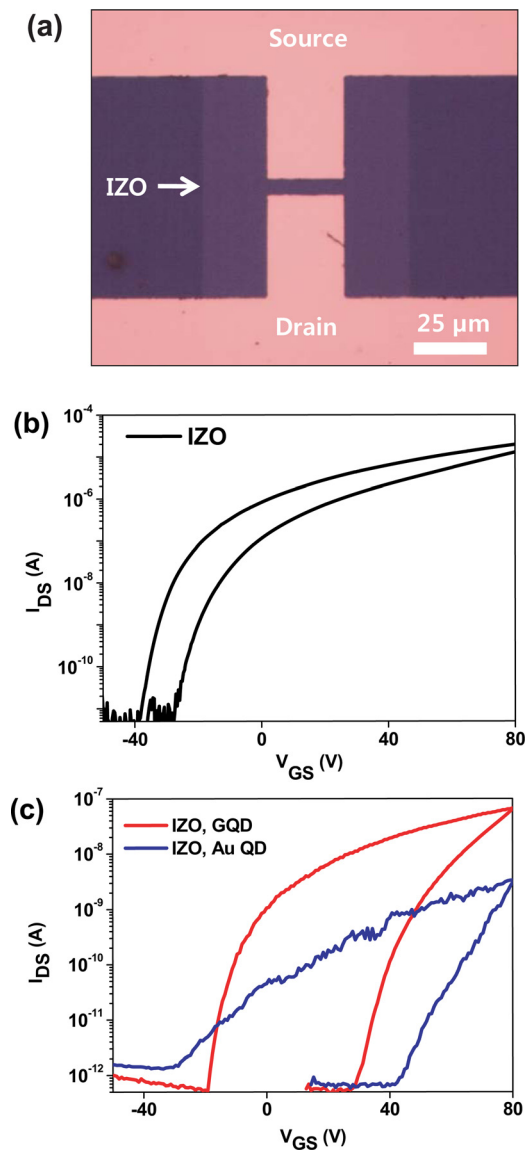
FIG. 3. (a) Optical image of the nonvolatile memory device with GQD trap layer. In this device, IZO of 20 nm was used for channel and Cr/Au (10/60 nm) was used for source and drain electrodes. (b) Transfer (I_{DS}-V_G) characteristics of IZO transistor without trap layer. (c) Transfer characteristics of nonvolatile memory devices with GQDs trap layer (red line) and Au QDs (blue line). All devices were measured with same speed of 9.55 V/s.

Table I). It is of note that the GQD memory revealed a fast subthreshold swing of 5.21 V/dec, three times smaller than Au QDs memory (15.53 V/dec) and similar to IZO transistor (3.73 V/dec) (Table I). Because of this fast subthreshold swing characteristics in GQDs compared to that in Au QD memory, the source-drain current in GQD memory was effectively modulated by an applied gate bias (Fig. 3(c)). As a result, on current (I_{on}) in GQD memory was enhanced to

TABLE I. Device parameters of IZO transistor and IZO nonvolatile memory device with GQDs and Au QDs charge-trap materials.

Confined structures	Hysteresis (V)	Subthreshold swing (V/dec)	I_{on} (A)	$I_{on/off}$
IZO	15	3.73	2.29×10^{-6}	2.10×10^{6}
IZO- GQDs	55	5.21	6.68×10^{-8}	1.00×10^{5}
IZO- Au QDs	60	15.53	3.33×10^{-9}	4.75×10^{3}

6.68×10^{-8} A from 3.33×10^{-9} A and on/off ratio to 10^{5} from $\sim 10^{3}$ in the same gate voltage range.

Fast modulation in GQDs memory can be explained by the band diagrams shown in Figure 4, depicting the cases of GQDs memory (Figs. 4(a) and 4(b)) and Au QDs memory (Figs. 4(c) and 4(d)) at negative and positive gate voltages. The gate electric field is applied between silicon back gate and IZO channel across the QD trap layer. The Fermi-level of GQD can be effectively modulated near the Dirac point because of limited electron density of states (Figs. 4(a) and 4(b)).[21] When a negative gate voltage (V_g) is applied between Si substrate and IZO layer, electrons in GQDs tunnel cross the TO and reach the IZO channel, as shown schematically in Figure 4(a). Fermi-level (E_F) in GQDs is largely downshifted from the Dirac point with tunneling electrons because of limited DOS near the Dirac point of GQDs. The decrease of the Fermi energy E_F in the GQDs could lead to effectively increase the energy band of TO and IZO. With a positive gate voltage, electrons from IZO tunnel to GQDs (Fig. 4(b)). The E_F in GQDs is largely shifted up by tunneling electrons from IZO, and then the energy bands of TO and IZO are effectively decreased. In contrast, the Fermi-level of Au QDs can barely be shifted by the tunneling electrons due to the large DOS and strong screening effect of the metal quantum-dots (Figs. 4(c) and 4(d)). As a result, the energy band of TO and IZO is hardly modulated by the applied gate bias. We emphasize that the use of GQDs in memory device is critical because graphene's low DOS enables greater shift in E_F by a given gate bias compared with a conventional metal trap layers. Furthermore, weak electrostatic screening of atomic sized monolayer graphene (~ 1 nm) effectively transfer the gate electric field, while relatively thicker Au-QD (~ 15 nm) largely screen the gate field and interrupt the IZO gate modulation.

Figure 5(a) shows the memory window with various gate voltage sweep speed. The memory window was increased
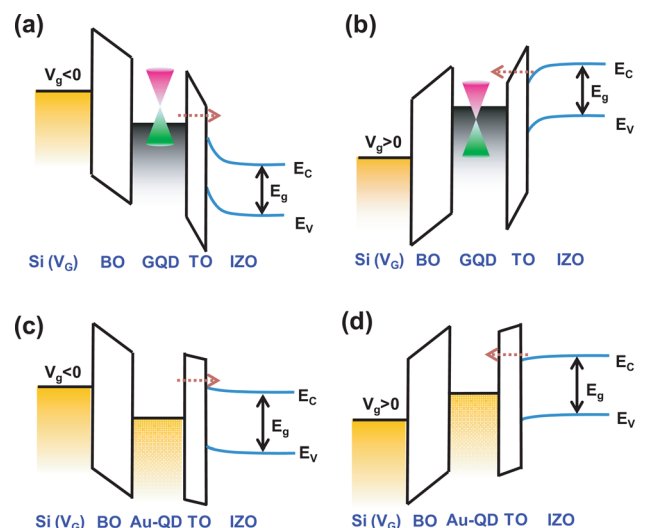

FIG. 4. Schematic illustration of energy band diagrams of nonvolatile memory devices with GQD charge-trap at (a) negative gate voltage and (b) positive gate voltage. BO is blocking oxide and TO is tunneling oxide. Schematic illustration of energy band diagrams of nonvolatile memory devices with Au QD charge-trap at (c) negative gate voltage and (d) positive gate voltage. Weak electrostatic screening in GQDs enables efficient modulation of IZO energy band, while gate field is primarily screened by Au QDs.
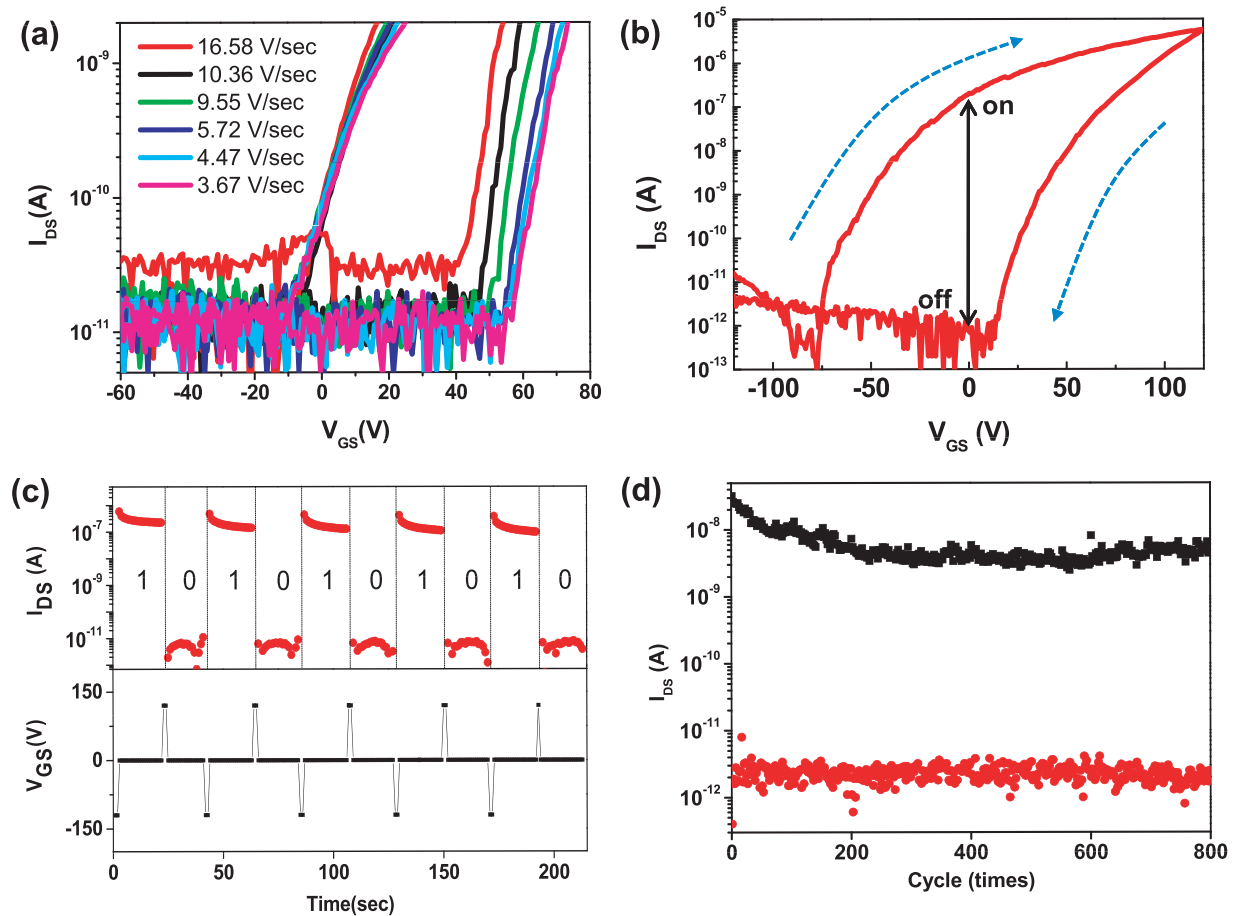
FIG. 5. (a) Memory window of GQD memory device measured with various gate voltage sweep speed. (b) Hysteresis in transfer characteristics of GQDs trap layer. Arrows indicate the gate voltage sweeping direction. (c) Programming/erasing corresponding (0, 1) series of 1-bit memory cell. (d) Endurance test with repeating programming ($V_G = -120\,V$) and erasing ($V_G = 120\,V$) cycles.

with decreasing sweep speed because more charges are trapped in GQDs charge trap. Figure 5(b) shows the procedure for charge trapping and the corresponding transfer characteristics. When the gate bias sweeps from $-120\,V$ to $+120\,V$, holes are trapped in GQD charge traps. Positive electric field is applied to the IZO channel by the trapped holes, and as a consequence, the threshold voltage is shifted to $V_{GS} = -70\,V$. On the contrary, the electrons were trapped in GQD layer when the gate bias sweeps from $+120\,V$ to $-120\,V$. The trapped electrons apply the negative electric field to the IZO channel, causing the threshold voltage shift to $V_{GS} = +10\,V$. As a result, large hysteresis of $80\,V$ is induced by the gate voltage sweeping from $+120\,V$ to $-120\,V$. The on/off ratio of 10^5 is observed at a reading voltage of $V_{GS} = 0\,V$. We measure the endurance characteristics of our GQD memory device (Figs. 5(c) and 5(d)). Programming and erasing are repeated with $V_{GS} = -120\,V$ and $V_{GS} = +120\,V$, respectively, and the current was measured with $V_{GS} = 0\,V$ between the programming and erasing. The program and erase states are clearly demonstrated with an on/off ratio of 10^5 (Fig. 5(c)), and each state shows almost the same current in the subsequent repetitions. The endurance test was repeated over 800 cycles (Fig. 5(d)). The on and off states were well maintained without significant changes.

In conclusion, we have demonstrated non-volatile memory device using discrete GQD trap layer. The Fermi-level of GQDs was effectively modulated near the Dirac point

because of limited density of states and weak electrostatic screening in monolayer graphene. As a result, GQD memory achieved three times faster subthreshold swing of 5.21 V/dec ($300\,nm\ SiO_2$ gate insulator) than that of Au QD memory (15.53 V/dec) which has strong electrostatic screening with overlapped parabolic DOS dispersion. Together, our devices with discrete charge traps enable stable endurance up to 800 cycles of programming and erasing. This study suggests the exciting potential of GQD trap layer for a highly promising material in non-volatile memory devices.

Graphene was synthesized by copper-catalyzed atmospheric pressure CVD using a gas mixture of Ar, H_2 and diluted CH_4, where CH_4 gas is a carbon-containing precursor.[25] The 10 nm Au film was deposited on the graphene by thermal evaporation at 2×10^6 Torr. Au film was aggregated to form Au quantum-dots by annealing at $300\,^\circ C$ for 1 h under ambient conditions. To form the GQDs, O_2 plasma etching was performed at an O_2 flow rate of 5 sccm and a power of 1 W for 20 s. Au QDs were removed by dipping in Au etchant (GE 8111) with an etch rate of 3 nm/s at room temperature. The Al_2O_3 tunneling oxide was deposited by commercial ALD apparatus (Lucida D100, NCD Technology, Korea). For IZO semiconductor channel, a 0.03 M mixture of zinc acetate dehydrate [$Zn(OAc)_2\cdot2H_2O$] and indium nitrate hydrate [$In(NO_3)_3\cdot4H_2O$] was used as a sol−gel precursor; a mole ratio of In/Zn was fixed at 1:1, which were dissolved in 2-ME. Monoethanolamine (EA) was added with a mole ratio of In/

EA = 1:10 and then stirred for 1 h at room temperature to form stable IZO precursor solution.[28] IZO precursor solution was spin-coated at 3000 rpm for 1 min and prebaked on a hot plate at 160 °C for 10 min to remove organic solvent. The prebaked IZO film was cooled at room temperature, and then 20 nm of IZO film was formed. The aforementioned processes were repeated 3 times to make 60 nm IZO film. IZO thin films were annealed at 400 °C for 1 h in the furnace. The source and drain electrodes of Cr (5 nm)/Au (60 nm) were patterned by photolithography and e-beam evaporation. Electrical transport measurements were conducted with a probe station and a source/measure unit (Agilent B2900A) at room temperature. Scanning electron microscope (JEOL, JSM-7401 F) images were taken in a secondary electron image mode under a pressure of 4×10^3 Torr (1 Torr–133.3 Pa).

[1]S. V. Morozov, K. S. Novoselov, M. I. Katsnelson, F. Schedin, D. C. Elias, J. A. Jaszczak, and A. K. Geim, Phys. Rev. Lett. **100**, 016602 (2008).

[2]K. I. Bolotin, K. J. Sikes, Z. Jiang, M. Klima, G. Fudenberg, J. Hone, P. Kim, and H. L. Stormer, Solid State Commun. **146**, 351–355 (2008).

[3]S. Ghosh, I. Calizo, D. Teweldebrhan, E. P. Pokatilov, D. L. Nika, A. A. Balandin, W. Bao, F. Miao, and C. N. Lau, Appl. Phys. Lett. **92**, 151911 (2008).

[4]R. R. Nair, P. Blake, A. N. Grigorenko, K. S. Novoselov, T. J. Booth, T. Stauber, N. M. R. Peres, and A. K. Geim, Science **320**, 1308 (2008).

[5]S. Bae, H. Kim, Y. Lee, X. Xu, J. S. Park, Y. Zheng, J. Balakrishnan, T. Lei, T. Lei, H. R. Kim II, Y. Song, Y. J. Kim, K. S. Kim, B. Ozyilmaz, J. H. Ahn, B. H. Hong, and S. Iijima, Nat. Nanotechnol. **5**, 574–578 (2010).

[6]S. H. Chae, W. J. Yu, J. J. Bae, D. L. Duong, D. Perello, H. Y. Jeong, Q. H. Ta, T. H. Ly, Q. A. Vu, M. Yun, X. Duan, and Y. H. Lee, Nat. Mater. **12**, 403–409 (2013).

[7]W. J. Yu, S. Y. Lee, S. H. Chae, D. Perello, G. H. Han, M. Yun, and Y. H. Lee, Nano Lett. **11**, 1344–1350 (2011).

[8]W. J. Yu, S. H. Chae, S. Y. Lee, D. L. Duong, and Y. H. Lee, Adv. Mater. **23**, 1889–1893 (2011).

[9]K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, and A. A. Firsov, Science **306**, 666–669 (2004).

[10]K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, M. I. Katsnelson, I. V. Grigorieva, S. V. Dubonos, and A. A. Firsov, Nature **438**, 197–200 (2005).

[11]C. R. Dean, A. F. Young, I. Meric, C. Lee, L. Wang, S. Sorgenfrei, K. Wantanabe, T. Taniguchi, P. Kim, K. L. Shepard, and J. Hone, Nat. Nanotechnol. **5**, 722–726 (2010).

[12]Y. Q. Wu, Y. M. Lin, A. A. Bol, K. A. Jenkins, F. Xia, D. B. Farner, Y. Zhu, and P. Avouris, Nature **472**, 74–78 (2011).

[13]L. Liao, Y. C. Lin, M. Q. Bao, R. Cheng, J. W. Bai, Y. Liu, Y. Q. Qu, L. W. Kang, Y. Huang, and X. Duan, Nature **467**, 305–308 (2010).

[14]F. Schwierz, Nat. Nanotechnol. **5**, 487–496 (2010).

[15]F. Wang, Y. B. Zhang, C. S. Tian, C. Girit, A. Zettl, M. Crommie, and Y. R. Shen, Science **320**, 206–209 (2008).

[16]N. O. Weiss, H. Zhou, L. Liao, Y. Liu, S. Jiang, Y. Huang, and X. Duan, Adv. Mater. **24**, 5782–5825 (2012).

[17]A. J. Hong, E. B. Song, H. S. Yu, M. J. Allen, J. Kim, J. D. Fowler, J. K. Wassei, Y. Park, Y. Wang, J. Zou, R. B. Kaner, B. H. Weiller, and K. L. Wang, ACS Nano **5**, 7812–7817 (2011).

[18]S. Wang, J. Pu, D. S. H. Chan, B. J. Cho, and K. P. Loh, Appl. Phys. Lett. **96**, 143109 (2010).

[19]J. K. Park, K. J. Choi, J. H. Yeon, S. J. Lee, and C. H. Kim, Appl. Phys. Lett. **88**, 071916 (2006).

[20]B. Eitan, P. Pavan, I. Bloom, E. Aloni, A. Frommer, and D. Finzi, IEEE Electron Device Lett. **21**, 543–545 (2000).

[21]W. J. Yu, Z. Li, H. Zhou, Y. Chen, Y. Wang, Y. Huang, and X. Duan, Nat. Mater. **12**, 246–252 (2013).

[22]W. J. Yu, Y. Liu, H. Zhou, A. X. Yin, Z. Li, Y. Huang, and X. Duan, Nat. Nanotechnol. **8**, 952–958 (2013).

[23]L. Britnell, R. V. Gorbachev, R. Jalil, B. D. Belle, F. Schedin, A. Mishchenko, T. Georgiou, M. I. Katsnelson, L. Eaves, S. V. Morozov, N. M. R. Peres, J. Leist, A. K. Geim, K. S. Nonvoselov, and L. A. Ponomarenko, Science **335**, 947–950 (2012).

[24]H. J. Yang, J. Heo, S. Park, H. J. Song, D. H. Seo, K. E. Byun, P. Kim, I. Yoo, H. J. Chung, and K. Kim, Science **336**(6085), 1140–1143 (2012).

[25]H. Zhou, W. J. Yu, L. Liu, R. Cheng, Y. Chen, X. Huang, Y. Liu, Y. Wang, Y. Huang, and X. Duan, Nat. Commun. **4**, 2096 (2013).

[26]J. W. Suk, A. Kitt, C. W. Magnuson, Y. F. Hao, S. Ahmed, J. H. An, A. K. Swan, B. B. Goldberg, and R. S. Ruoff, ACS Nano **5**, 6916 (2011).

[27]W. J. Yu and X. Duan, Sci. Rep. **3**, 1248 (2013).

[28]X. Liu, C. Wang, B. Cai, X. Xiao, S. Guo, Z. Fan, J. Li, X. Duan, and L. Liao, Nano Lett. **12**(7), 3596–3601 (2012).