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Mixed Analog Digital (MAD) Converters for High Power Density DC-DC Conversions

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***Abstract*- Conventional switched-mode power supplies (SMPSs) have intrinsic instantaneous power pulsation at the switching frequency thus require bulky filters. To improve the power density, this paper proposes a concept named the Mixed Analog-Digital (MAD) which can be applied as DC-DC converters. By inserting an analog voltage component between the load and source, the output voltage naturally has much smaller fluctuation thereby much smaller passive filter is required. Simulations and experiments validate that the proposed MAD concept can be applied as DC-DC converters to significantly increase the power density.**

***Index Terms*- dc-dc converter, high power density, mixed analog-digital (MAD) converter.**

I. Introduction

DC-DC converters are normally in either linear mode or switched mode. Switched-mode power supplies (SMPSs) are digital-based converters employing semiconductors as switches.[1, 2] The switching operations generate square voltage/current waveforms containing significant ripples at the switching frequency. Therefore, bulky low-pass filters (LPFs) are required to reduce ripples.

To reduce the filter size, three methods can be applied as shown in Fig. 1: 1) decreasing the ripple magnitude from the source, 2) increasing the attenuation gain of the LPF at the transmitting paths, and 3) introducing advanced control techniques.

1) Multilevel converters can decrease the ripple magnitude from the source [3]. However, multilevel converters require more semiconductors. Moreover, the power balance among sub-modules requires complex controls.

2) Increasing the switching frequency (f_{sw}) [4] can increase the attenuation gain of the LPF. However, increasing the f_{sw} raises the power loss of semiconductors and magnetic components. Moreover, at high frequencies, parasitic components (including the capacitance, inductance, and resistance) can deteriorate the filter's insertion gain [5, 6], causing ineffectiveness by increasing the f_{sw}.

Switched capacitor converters (SCCs) use capacitors rather than inductors as the major energy storage devices.[7-9] Because the energy density of the capacitors is much higher than that of the inductors, the switched-capacitor converters can use small LPF and achieve high power density. But the power ripple still exists, and the power density decreases sharply with the load increase.

3) Advanced control techniques, e.g., active capacitors [10], divert the ripple power into the energy storage devices thus lower ripples at the load. However, the control bandwidth (BW) of DC-DC converters is limited by the f_{sw} [11]. Therefore, active control techniques are invalid in attenuating harmonics at switching frequencies or higher.

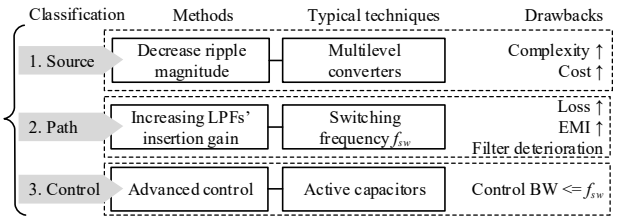

Fig. 1. The common techniques to increase power density of SMPSs.

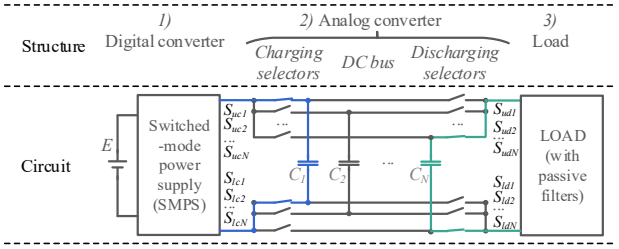

Fig. 2. The topology of the proposed MAD converter when C_1 is charging, C_2 -C_{N-1} are floating, and C_N is discharging. S_{uc1}-S_{ucN} are the upper charging selectors, S_{lc1}-S_{lcN} are the lower charging selectors, S_{ud1}-S_{udN} are the upper discharging selectors, S_{ld1}-S_{ldN} are the lower discharging selectors.

Comparing to the SMPS, linear power supplies, such as low-dropout regulators (LDOs), are analog-based converters. LDOs use MOSFETs as controlled resistors rather than switches. By adjusting the resistance, LDOs can control the voltage drops across the resistor thereby regulate the output voltage. Ripples in LDOs are negligible due to the absence of voltage/current switching. However, the power loss of this controlled resistor is significant. Therefore, LDOs exhibit low efficiencies and have been mainly used in low power applications.

This letter proposes a Mixed Analog-Digital (MAD) concept for DC-DC converters. The circuit of the MAD converter is shown in Fig. 2. This MAD converter comprises a digital converter and an analog converter. The analog converter consists of the voltage selectors which charging and discharging DC capacitors. With the charging selectors, the DC bus capacitors are charged to the required load voltage (V_L); with the discharging selectors, the load is charged by the DC bus capacitors. Because the load is always connected with DC Bus capacitors, no large voltage changes between 0 and E exist in MAD converters. The digital converter only regulates the voltage superimposed to the analogue voltage from the selector, so the ripple is intrinsically small. It is worth noting that the digital converter is not compulsory. The variant of the

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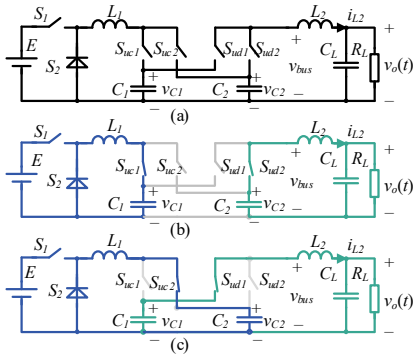

Fig. 3. Buck-based MAD converter and the equivalent circuits: (a) topology, and the equivalent circuits when (b) C_1 is charging while C_2 is discharging, and (c) C_1 is discharging while C_2 is charging.

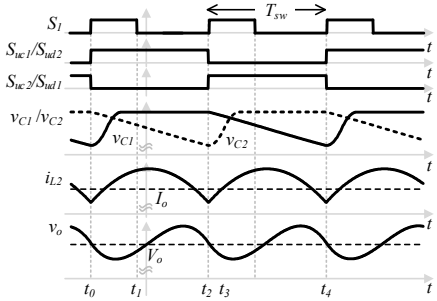

Fig. 4. Waveforms of the Buck-based MAD converter. Their time-domain expressions are in (8)-(10), and simulation files are included in the multimedia folder.

MAD without the digital converter will be used for experimental validation in this paper in the following sections.

II. Proposed Circuits and Operation Principles

A. Typical MAD Converter and Operation Principle

Fig. 2 shows the typical MAD converter which is composed of three portions: 1) a digital converter; 2) an analog converter, and 3) a load with a filter. The digital converter can employ typical DC-DC topologies such as the Buck and *LLC*; the analog converter is formed by voltage selectors and multiple capacitors at the DC bus. Each capacitor has two discharging selectors and two charging selectors. The charging and discharging selectors are controlled to ensure balanced charging/discharging power in each capacitor. The DC capacitors can be connected in series or parallel. The inserted analog converter can reduce the voltage ripple because:

1) The load draws power from capacitors one by one. Therefore, the voltage across the load is close to constant.

2) Charging loops and discharging loops (i.e., the blue and green loops) in Fig. 2, can be separated. Therefore, the ripple power can be diverted to the capacitors rather than the load.

B. MAD Converter in form of Buck Converter and Paralleled-Connected DC Capacitors

The proposed circuit is shown in Fig. 3: the digital converter employs a Buck converter, and the analog converter employs paralleled connected C_1 and C_2 in the DC bus; S_{uc1} and S_{uc2} are the charging switches; S_{ud1} and S_{ud2} are the discharging switches. Because C_1 and C_2 are paralleled with a common ground, the lower selectors for charging and discharging (i.e., S_{lc1}, S_{lc2} and S_{ld1}, S_{ld2}) in Fig. 2 are unnecessary. The operation principles are presented in Fig. 4 and summarized below:

1) S_1/S_2 follows the operation principle of Buck converters. Because the discontinuous conduction mode (DCM) requires small inductance[12] and can achieve zero voltage switching, DCM is widely applied in Buck converters and is compared in this letter. The modulation index M is:

$$M = V_{bus} / E = 2 / \left(1 + \sqrt{1 + 8L_1 f_{sw} / \left(R_L D^2\right)}\right) \tag{1}$$

where V_{bus} is the voltage of the DC bus capacitors, D is the duty cycle, R_L is the load resistor, and the f_{sw}/T_{sw} is the switching frequency/period of the Buck circuit in Fig. 4.

2) Within [t_0, t_2] in Fig. 4, C_1 is charged and maintained at V_{bus} and C_2 is discharging; the equivalent circuit is shown in Fig. 3(b). The S_1 operates as the switch of the Buck converter: within [t_0, t_1], the S_1 is on, and within [t_1, t_2], S_1 is off.

3) Within [t_2, t_4] in Fig. 4, C_2 is charged and maintained at V_{bus}, C_1 is discharging. The equivalent circuit is shown in Fig. 3(c). The S_1 operates as the switch of the Buck converter: within [t_2, t_3], the S_1 is on, and within [t_3, t_4], S_1 is off.

Because the discharging loop is separated from the charging loop, the output ripple is determined by the discharging loop only. Fig. 4 shows that the discharging circuit has three energy storage devices (the DC bus capacitance C_{bus}, L_2, and C_L). Using the state-space approach of the network theory, three state equations (i.e., (2)–(4)) can identify the general solutions, and three equations (i.e., (5)–(7)), can identify the initial states.

$$\begin{cases} C_{bus} dv_{Cbus}(t)/dt = -I_o & (2) \\ L_2 di_{L2}(t)/dt = v_{Cbus}(t) - V_o & (3) \\ C_L dv_{CL}(t)/dt = i_{L2}(t) - I_o & (4) \end{cases}$$

$$\begin{cases} \dfrac{1}{T_{SW}} \int_{-T_{SW}/2}^{T_{SW}/2} v_{Cbus}(t)dt = V_o & (5) \\ \dfrac{1}{T_{SW}} \int_{-T_{SW}/2}^{T_{SW}/2} i_L(t)dt = I_o & (6) \\ \dfrac{1}{T_{SW}} \int_{-T_{SW}/2}^{T_{SW}/2} v_{CL}(t)dt = V_o & (7) \end{cases}$$

The solutions for (2)–(7) are below:

$$\begin{cases} v_{Cbus}(t) = -I_o t / C_{bus} + V_o & (8) \\ i_L(t) = -I_o t^2 / (2L_2 C_{bus}) + I_o \left(1 + T_{sw}^2 / (24 L_2 C_{bus})\right) & (9) \\ v_{CL}(t) = -I_o t^3 / (6 L_2 C_{bus} C_L) + I_O T_{sw}^2 t / (24 L_2 C_{bus} C_L) + V_o(0) & (10) \end{cases}$$

Eqs. (8)-(10) shows that v_{Cbus} (i.e., v_{C1} and v_{C2}) is proportional to ($-t$), i_L is proportional to ($-t^2$), and v_o (i.e., $v_{CL}(t)$) is proportional to ($-t^3$).

From (10), letting $dv_{CL}(t)/dt = 0$, the minimum and maximum $v_{CL}(t)$ (donated as V_{CL_min} and V_{CL_max}) are:

$$\begin{cases} V_{CL\_min} = -I_o T_{sw}^3 / \left(72\sqrt{3} L_2 C_i C_L\right) + V_o, @t = -T_{SW}/2\sqrt{3} \\ V_{CL\_max} = I_o T_{sw}^3 / \left(72\sqrt{3} L_2 C_i C_L\right) + V_o \ , @t = T_{SW}/2\sqrt{3} \end{cases} \tag{11}$$

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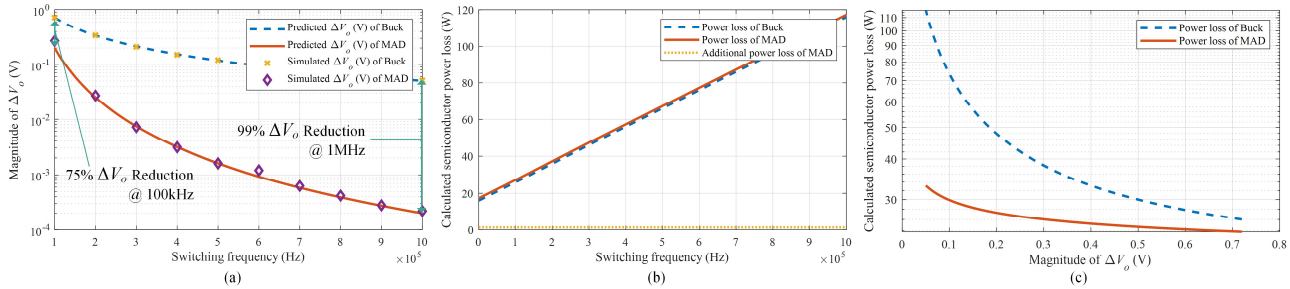

Fig. 5. The comparison between the Buck converter in DCM and the proposed MAD converter with P = 1000 W, E = 400 V, and V_o= 200 V. For the MAD converter L_1= L_2= 1 μH, and C_1= C_2= C_L= 20 μF; for the Buck converter, L_{total} = 2 μH, and C_{total} = 60 μF: (a) the magnitude of ΔV_o versus f_{sw}, (b) calculated power loss versus f_{sw}, and (c) the calculated power loss versus the magnitude of ΔV_o. The ΔV_o reduction is calculated by $(\Delta V_{o\text{-}Buck} - \Delta V_{o\text{-}MAD}) / \Delta V_{o\text{-}Buck}$. The simulation files for the ΔV_o of both converters are included in the multimedia folder.

From (11), the ripple voltage of the MAD converter, donated as ΔV_{o_MAD}, is derived as (12) and can be verified by the simulation attached in the multimedia folder.

$$\Delta V_{o\_MAD} = V_{CL\_\max} - V_{CL\_\min} = I_o / \left(36\sqrt{3} L_2 C_1 C_L f_{sw}^3\right) \quad (12)$$

C. Comparison between the Proposed MAD Converter and Buck Converter

The ripple voltage of the DCM Buck converter, donated by ΔV_{o_Buck}, is:

$$\Delta V_{o\_BUCK} = \frac{V_o}{f_{sw} C_L R_L} + \frac{LEV_o}{2C_L R_L^2 (E - V_o)} - \frac{V_o}{C_L}\sqrt{\frac{2LE}{f_{sw} R_L^3 (E - V_o)}} \quad (13)$$

The comparison between (12) and (13) shows that ΔV_o in the MAD converter is reduced because ΔV_{o_MAD} is proportional to $1/f_{sw}^3$ while ΔV_{o_buck} of the DCM Buck converter is proportional to $1/f_{sw}$. Moreover, the coefficient in (12) is smaller than the coefficient in (13).

Fig. 5(a) shows both the calculated and the simulated ΔV_o for the DCM Buck converter and the proposed MAD converter. The comparison between ΔV_{o_MAD} (the blue lines and the yellow dots) and ΔV_{o_Buck} (the red lines and the purple dots) shows that the proposed MAD converter effectively reduces ΔV_o, especially at high f_{sw}. With the same total inductance (2 μH) and total capacitance (60 μF), the ΔV_o in the proposed MAD converter is much smaller than that in the DCM Buck converter.

The MAD converter requires four additional switches than the Buck converter, i.e. S_{uc1}, S_{uc2}, S_{ud1}, and S_{ud2} as shown in Fig. 3. The voltage and current stress of these switches are listed in TABLE I and are compared with that of the Buck converter. By using parameters shown in Fig. 5, the voltage stress of S_{uc1} to S_{uc2} is $I_o/(2f_{sw}C_{bus})$ = 5/(2×20μ×f_{sw}) ≤ 1.25V when f_{sw} ≥ 100kHz. The commercialized components are listed in TABLE II to analyse the cost differences between the Buck converter and the MAD converter. Because the voltage across the additional switches, S_{uc1}–S_{ud2}, can be both positive and negative, a four-quadrant switch, CSD85312Q3E, can be selected. The MAD converter has a higher cost than the Buck converter mainly due to additional isolated power supplies. Similar cost increases have also been found in the SCCs [7, 13] and the converters hybridizing an SCC and a Buck converter [14-17] which are commonly used in certain applications [7, 13, 14]. Although the cost of the MAD converter is higher than the cost of the Buck converter, the output voltage ripple reduction is significant, for example, 72% at f_{sw} =100kHz or 99% at f_{sw}=1MHz as shown in Fig. 5(a).

TABLE I
SWITCH SPECIFICATIONS OF THE MAD CONVERTER IN FIG. 3

	S_1-S_2	S_{uc1}-S_{uc2}	S_{ud1}-S_{ud2}
Voltage stress	E	$I_o/(2f_{sw}C_{bus})$ (Note1)	$I_o/(2f_{sw}C_{bus})$ (Note2)
I_{RMS}	P/E	P/E	$P/\left(\sqrt{2}V_o\right)$

Note1: the voltage across S_{uc1}/S_{uc2} is $|v_{C1}(t) - v_{C2}(t)|$. From Fig. 4 and (8), $|v_{C1}(t) - v_{C2}(t)|_{\max} = |(-I_o/C_{bus}\times t + V_o) - V_o|_{\max} = I_o/(2f_{sw}C_{bus})$.
Note2: the voltage across S_{ud1}/S_{ud2} is $|v_{Cbus}(t) - v_{CL}(t)|$. From Fig. 4 and (8), $|v_{C1}(t) - v_{C2}(t)|_{\max} \approx (-I_o/C_{bus}\times t + V_o) - V_o|_{\max} = I_o/(2f_{sw}C_{bus})$.

TABLE II
COST OF MAJOR DEVICES BETWEEN THE BUCK CONVERTER AND MAD CONVERTER

	Type	Specification	Cost (GBP)
S_1, S_2	STP12NK60Z	MOSFET, 650V, 10A, t_r=18.5ns, t_f=31.5 ns, $R_{DS(on)}$= 640 mΩ	1.44
S_{uc1}, S_{uc2}, S_{ud1}, S_{ud2}	CSD85312Q3E	MOSFET, 20V, 12A, t_r=27ns, t_f=6ns, $R_{DS(on)}$=10.3mΩ.	0.27
C	C4AQCBW5200A3FJ	Film capacitor, 20 μF, 650V	1.81
L	7443340100	Inductor, 1μH, 17A	1.42
PS	RFM-0505S	Isolated power supply, 5V output	0.87
Q	ZXGD3103N8TC	MOSFET driver, both high side and low side	0.34
Buck	2× STP12NK60Z + 3×C + 2×L + 2×PS + 2×Q		13.57
MAD	2× STP12NK60Z + 4× CSD85312Q3E + 3×C + 2×L + 6×PS + 6×Q		19.49

Note1: the price data were in digikey.co.uk, at the maximum quantity, without tax, on November 24, 2019.
Note2: the parameter is the same with Fig. 5, i.e. P = 1000 W, E = 400 V, V_o= 200 V, L_{total} = 2 μH, and C_{total} = 60 μF.

By using the components in TABLE II, the loss of the MAD converter and Buck converter at the same f_{sw} is plotted in Fig. 5(b), showing a negligible difference. This is because that 1) the $R_{DS(ON)}$ of the additional switches is small due to low voltage rating devices; 2) low operation voltage of the additional devices thus low switching losses.

The additional devices in MAD converters do not inevitably compromise its reliability. As shown in Fig. 5(c), the MAD converter exhibits lower losses compared with the Buck converter because the f_{sw} of the MAD converter is much lower if the output ripple voltage ΔV_o is the same. It has been commonly accepted that the power loss reduction can decrease

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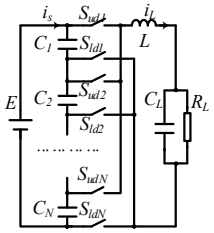

Fig. 6 Topology of the N:1 voltage divider based MAD converter.

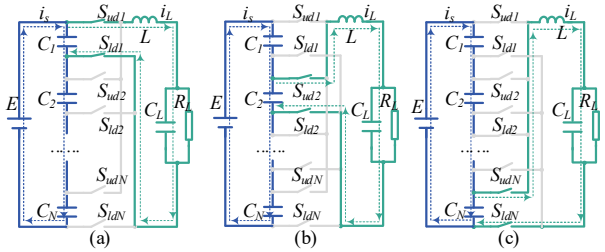

Fig. 7 Equivalent circuits and current paths when (a) C_1 is charging, (b) C_2 is charging, and (c) C_N is charging. N is the number of capacitors.

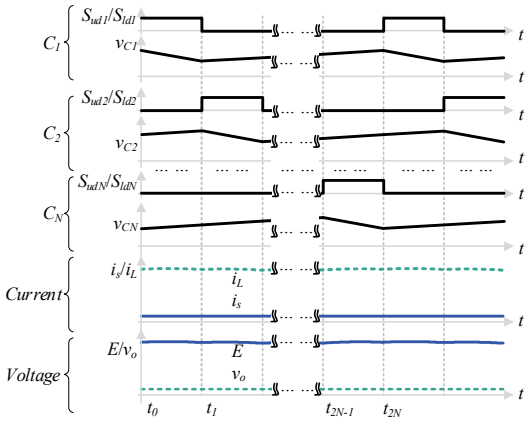

Fig. 8. Waveforms of the N:1-voltage-divider-based MAD converter. The simulated circuit with N=2 is attached to the multimedia folder.

the junction temperature, and reduce the failure probability [18].

D. MAD Converter comprising the N:1 Voltage Divider

The MAD converter comprising a voltage divider as the analogue converter is one variant of the MAD converter breed. This variant can operate without having the digital converter.

As shown in Fig. 6, C_1–C_N are connected in series to form an *N:1* voltage divider and the DC bus capacitors. Because the voltage divider comprises no switches, the charging selectors in Fig. 2 (i.e., S_{uc1}–S_{ucN}, and S_{lc1}–S_{lcN}) are removed. The equivalent circuits at different operation stages are shown in Fig. 7(a)–(c), and the waveforms are shown in Fig. 8.

Similar to the Buck based MAD converter in Section B, the modulation index M and ΔV_o are determined by the charging and discharging loop respectively. For a voltage divider, M equals $1/N$; for ΔV_o, the differences between Fig. 4 and Fig. 8 are that the ripple frequency is Nf_{sw} and the discharging current of C_{bus} is (I_o–I_s). Therefore, the ΔV_o in Fig. 8 can be obtained from (12) by replacing Nf_{sw} by f_{sw}, and (I_o–I_s) by I_o:

$$\Delta V_o = \frac{I_o - I_s}{36\sqrt{3}LC_{bus}C_L\left(Nf_{sw}\right)^3} = \frac{\left(N-1\right)I_o}{36\sqrt{3}N^4LC_{bus}C_Lf_{sw}^3} \quad (14)$$

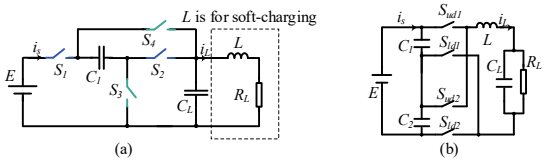

Fig. 9 The circuits of (a) the *2:1* series-paralleled SCC [9], and (b) the *2:1* MAD converter in Fig. 7. For the SCC, S_1 and S_2 are synchronized, while S_3/S_4 are complementary to S_1/S_2; for the MAD converter, S_{ud1} and S_{ld1} are synchronized, while S_{ud2}/S_{ld2} are complementary to S_{ud1}/S_{ld1}.

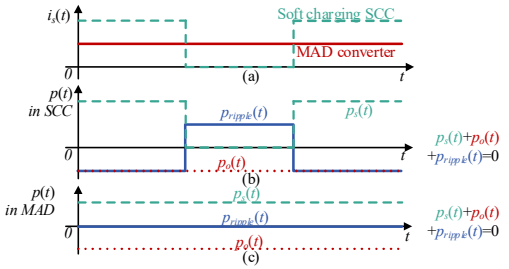

Fig. 10 Comparison of the input current, $i_s(t)$, and the instantaneous power, $p(t)$, between the SCC and MAD converter. The difference between the input power $p_s(t) = Ei_s(t)$ and output power $p_o(t) = -v_o(t)i_L(t)$ is the ripple power $p_{ripple}(t) = -(p_s(t) + p_o(t))$. The $p_{ripple}(t)$ is provided by capacitors: charging when $p_{ripple}(t)<0$ and discharging when $p_{ripple}(t)>0$. For the MAD converter, the p_{ripple} is small thus less capacitance is required to store ripple power.

E. Comparison between the proposed MAD Converter with the Switched Capacitors Converters (SCCs)

Fig. 9 shows the circuits of the *2:1* series-parallel SCC [9] and the proposed *2:1* MAD converter. The operation of the SCC incorporates two stages: Stage 1, the power supply, E, charges both the capacitors and the load; Stage 2: E is disconnected, and the load is powered by the capacitors. In contrast, for the MAD converter, E is connected at all operation stages thus the input current, i_s, is continuous as shown in Fig. 10(a). Therefore, the input current ripple of the MAD converter is naturally smaller than that of the SCC as shown in Fig. 10(a). The reduced current ripple decreases the current ratings of the power source and relieves the EMI issue.

The magnitude of the ripple power, p_{ripple}, differentiates the MAD converter over the SCC converter. Fig. 10(b), in an SCC, the input power, p_s, fluctuates due to the square wave input voltage E. Therefore, the ripple power, p_{ripple}, fluctuates significantly as the output power needs to be constant. In contrast, Fig. 10(c) shows that the absence of voltage fluctuation between 0 to E at the input results in small ripple power p_{ripple}. Therefore, the capacitance required to smooth the ripple power is small.

For an SCC, the charge ripple, ΔQ_{SCC}, and the output voltage ripple, $\Delta V_{o\text{-}SCC}$, are expressed as (15) and (16), respectively:

$$\Delta Q_{SCC} = I_oT_{sw}/2 = 2C\Delta V_{o-SCC} \quad (15)$$

$$\Delta V_{o-SCC} = I_o/\left(4Cf_{sw}\right) = I_o/\left(2C_{total}f_{sw}\right) \quad (16)$$

where C_1=C_L=C and C_{total} = 2C is the total capacitance.

For the *2:1* MAD converter, the ΔV_o can be derived by substituting N = 2 into (14), and its expression is (17):

$$\Delta V_{o-MAD} = I_o/\left(576\sqrt{3}LC_{bus}C_Lf_{sw}^3\right) = I_o/\left(64\sqrt{3}LC_{total}^2f_{sw}^3\right) \quad (17)$$

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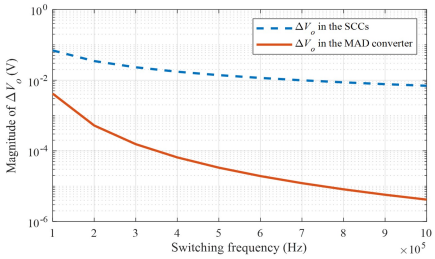

Fig. 11 Comparison of output voltage ripple against switching frequencies between the SCC and the MAD converter at $P = 100$ W, $E = 48$ V, and $V_o = 24$ V. For the MAD converter $L = 100$ nH, and $C_1 = C_2 = C_L = 100$ µF; for the SCC, $C_1 = C_L = 150$ µF. The MAD converter requires a 100 nH inductor which can be realized by PCB traces, and the SCC needs a large inductor to achieve the soft-charging technique. [9]

TABLE III
COMPARISON BETWEEN THE SERIES-PARALLEL SCC [9] AND THE MAD CONVERTER IN FIG. 9(B)

	Series-parallel SCC	MAD IN FIG. 7
Number of switches	4	4
Voltage rating of switches	V_o	V_o
$\sum(V_{rated} I_{avg})$ of switches	$2V_oI_o$	$2V_oI_o$
Number of capacitors	2	3
Voltage rating of capacitors	V_o	V_o
Maximum input current	I_o	$0.5I_o$
Shape of input current	square wave	dc current
Magnitude of p_{ripple}	large	small

where $C_{bus}=C_L=C_{total}/3$.

From (16) and (17), the comparison of the ΔV_o against the f_{sw} is plotted in Fig. 11. This comparison verifies that the proposed MAD converter can achieve lower voltage ripple at the same f_{sw}, requiring less capacitance, and hence achieving a higher power density of the converter.

A comparison is summarized in TABLE III, showing that both converters have the same number of switches and voltage ratings of the switches and the capacitors. The MAD converter needs one more capacitor but less total capacitance. However, it should be noted that the total weight/volume of the capacitor is proportional to the total capacitance as C_{total} rather than the number of the capacitors. The nature of low voltage ripples in MAD converters only requires small total capacitance C_{total}, which reduces the weight/volume of the capacitors so does weight/volume of the converter.

III. Experimental Verification

Experiments have been conducted with a *2:1* voltage divider-based MAD converter. Fig. 12(a) and (b) show its circuit and operation points. The circuit can be built with two MOSFETs and two diodes as shown in Fig. 12(c) or four MOSFETs as shown in Fig. 12(d). To reduce the conduction loss, Fig. 12(d) is built and tested and the porotype is shown in Fig. 13. The prototype parameters are summarized in TABLE IV. It is worth noting that the capacitance of MLCC capacitors, C3216X5R1H106K, decreases from 10 µF to 2.7 µF at 24 V. Moreover, unlike resonance-based techniques, this circuit is insensitive to inductance variation thus the micro-strip inductor can be used for the implementation of L. Fig. 14 shows the experimental results with the prototype. Fig. 14(a)

TABLE IV
PARAMETERS OF THE PROPOSED MAD CONVERTER

Symbol	Parameters	Circuit Realization
f_{sw}	100 kHz	DSP 28379d
C_1, C_2, C_L	160 (43) µF (Note)	16 × C3216X5R1H106K
L	30 nH	microstrip trace inductance
S_1, S_2, S_3, S_4	40V, 80A, 2.1 mΩ	FDMC8360L

Note: The rated capacitance of C3216X5R1H106K is 10 µF, but according to the datasheet, the capacitance decreases to 2.7 µF at the 24V DC voltage bias.

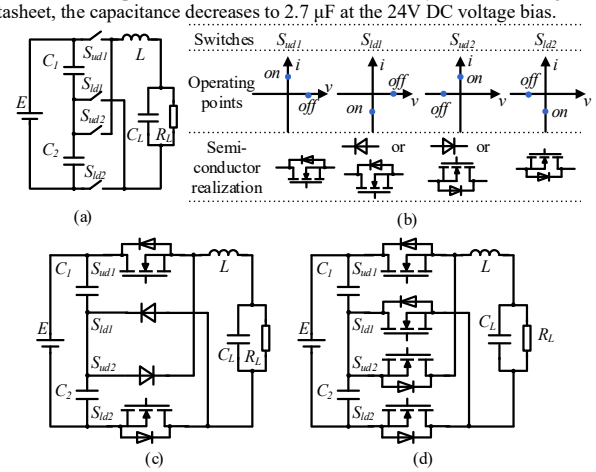

Fig. 12. The *2:1* voltage divider based MAD converter: (a) circuit, (b) operation points of S_1-S_4, and the circuit implemented with (b) two MOSFETs and two diodes, and (d) four MOSFETs.

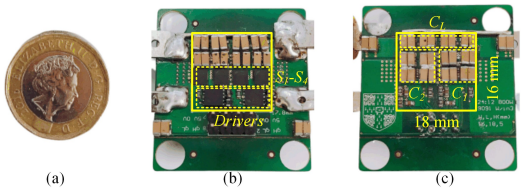

Fig. 13. The 960-W prototype: (a) a 1 British pound coin for perspective, (b) the top view, and (b) the bottom view. The height/width/length is 4.8/16/18 mm (0.19/0.63/0.71 inch), and the power density is 694 kW/L (10909 W/in^3).

show that the ΔV_o is less than 2% of V_o when converting 48 V to 24 V at 960 W. Furthermore, Fig. 14(b) and (c) show that the dynamic response of the load change between 100 W to 960 W is less than 6 µs. Fig. 14(d) verifies the switching sequences in Fig. 8 and the voltage stress polarity of each switch in Fig. 12 (b). Fig. 14(e) shows the 99.2% efficiency at 100 W and 92.9% efficiency at 960 W. Fig. 15 shows the thermal image of the converter at 480 W with only fan cooling. In conclusion, the proposed converter can achieve a power density of 694 kW/L (10909 W/in^3), small ΔV_o, and fast dynamic response (as shown in Fig. 14 (b) and (c)).

IV. Conclusions

This letter proposes the concept of the MAD converter, which can comprise a digital SMPS converter and an analogue converter formed by voltage selectors. By using the selector, the output voltage is maintained between the voltages across selected capacitors to avoid voltage ripples. The source and output terminals can be separated, and thus the ripple from the source can be diverted into the DC bus rather than the output. Two different circuits have been proposed based on the MAD converter concept. The realization of the additional switches

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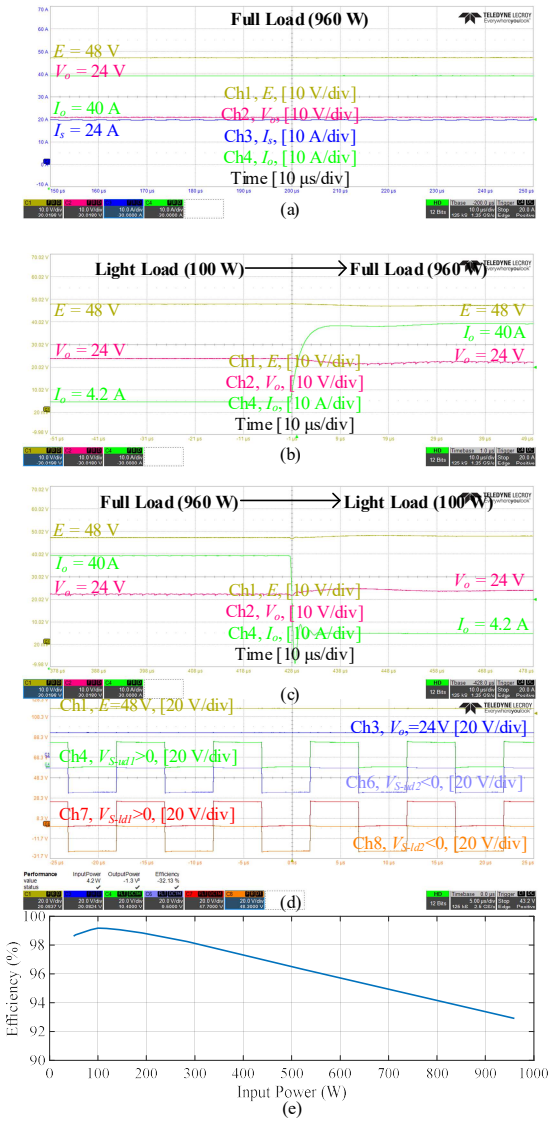

Fig. 14. Experiments at (a) 960 W, (b) the load transition from 100 W to 900 W, (c) the load transition from 960 W to 100 W, (d) the detailed waveforms, and (e) the power efficiency. The video of the dynamic response can be found in the multimedia folder.

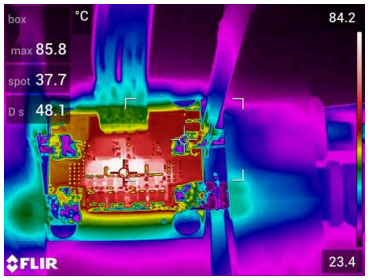

Fig. 15. Thermal performance with fan cooling only (E=48V, P = 480W).

for each converter has been discussed. Simulations and experiments validate that the proposed MAD converter can significantly increase the power density.

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