A positive feedback-based op-amp gain enhancement technique for high precision applications

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Abstract

A power-efficient, voltage gain enhancement technique for op-amps has been described. The proposed technique is robust against Process, Voltage, and Temperature (PVT) variations. It exploits a positive feedback-based gain enhancement technique without any latch-up issue, as opposed to previously proposed conductance cancellation techniques. In the proposed technique, four additional transconductance-stages (gm stages) are used to boost the gain of the main gm stage. The additional gm stages do not significantly increase the power dissipation. A prototype was designed in 65nm CMOS technology. It results in 81dB voltage gain, which is 21dB higher than the existing gain-boosting technique. The proposed opamp works with as low a power supply as 0.8V, without compromising the performance, whereas the traditional gain-enhancement techniques start losing gain below a 1.1V supply. The circuit draws a total static current of 295µA and occupies 5000µm2 of silicon area.

Keywords—Op-amp, gain, feedback, latch-up, phase-margin.

1. Introduction

The advancement of CMOS technologies paved the way for the growing electronics markets. This growth is driven by the high-level integration of highly sensitive analog circuits with digital signal processors. Digital circuits benefit from CMOS scaling, such as low power, high speed and small chip area. Currently, in most devices the systems on chip (SOC) digital processor constitutes above 90% of the chip area, hence scaling is moving towards even smaller geometry, such as 16nm CMOS with digital performance enhancement as the primary goal.

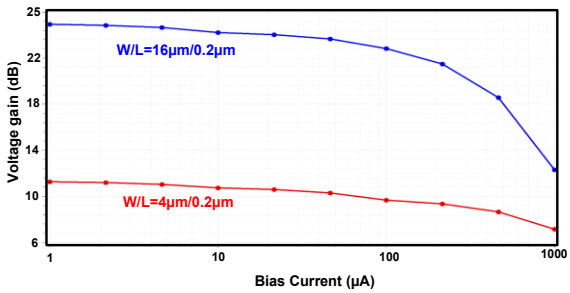

Fig. 1. Voltage gain versus bias current for a single transistor.

Unfortunately, however this scaling negatively affects the analog performance in the following aspects: 1. As the gate oxide thickness decreases due to shrinking the minimum feature size, this in turn lowers the allowable supply voltages [1]. The state-of-the-art 45nm technology node features a maximum supply voltage of only 1V for the standard MOSTs. This supply is expected to decrease to 0.5 V for the nodes by 2020. The threshold voltage (V_{TH}) does not scale down in pace with the supply voltage, which leads to a reduction in the achievable dynamic range, especially in the output stages. The gain

of a single transistor biased in the saturation region can be expressed as (1) [2], which reveals that it is inversely proportional to bias current (I_B). Of course, decreasing I_B to an extremely low value is not desirable (1), because the transistor moves into weak-inversion region and the intrinsic gain becomes independent of I_B.

$$A_V = g_m r_o = \sqrt{2\mu_n C_{OX} \frac{W}{L} I_B}.\frac{1}{I_B \lambda} \quad \alpha \quad \frac{1}{\sqrt{I_B}} \tag{1}$$

Fig.1 depicts how A_v varies with I_B for different aspect ratios (W/L). The maximum achievable gain is <20dB with minimal I_B. High precision applications, such as bio-medical and high-resolution ADCs requires a gain >75dB, which is much higher than a single transistor could achieve. To improve the gain, a few techniques have been introduced in the literature.

(a) Cascading single stage amplifiers into what is known as a multistage-amplifier. This will result in a very high gain (~60dB), but makes frequency compensation very difficult and results in an area penalty due to additional capacitors.
(b) The use of cascode transistors as shown in Fig. 2(a). This technique, however, requires a higher V_{dd}, which is very difficult due to the scaling. The gain of this topology can be expressed as 2(a).
(c) The gain boosting technique as proposed in [3], to increase the output impedance, hence the voltage gain by adding an additional opamp to create local negative feedback. Unfortunately, this will create closed loop pole-zero doublets, which will compromise the settling time of the step response. The gain of this architecture has been expressed as 2(b).
(d) The recycling gain enhancement technique as proposed in [4], which is only limited to cascade opamps.
(e) The split cascode technique as proposed in [5], which will increase gain only by ~12dB without dissipating any significant additional amount of power.

All the above techniques result in a limited gain enhancement of only 10-15dB. In [6] as depicted in Fig. 2(c), a technique has been proposed to enhance the gain by adding negative resistance at the output to cancel the device gds, which will in theory increase the voltage gain to infinity. Practically, however, the boost in gain is limited due to finite loop gain and matching. The gain of this technique is expressed in equation 2(c). A disadvantage of this technique is the latch-up problem due to the positive feedback; hence it is very sensitive to PVT variations, making it an unpopular technique for gain-enhancement.

$$G_{Cascode} = \frac{g_{m1} g_{m2}}{g_{o1} g_{o2}} \tag{2(a)}$$

$$G_{Gain\_Boosting} = \frac{g_{m1} g_{m2}}{g_{o1} g_{o2}} \tag{2(b)}$$

$$G_{Negative} = \frac{g_{m1}}{\frac{g_{o1} g_{o2}}{g_{m2}} - \frac{1}{R_N}} \tag{2(c)}$$

Various authors have presented derivatives of the above techniques, but none of them provides gain above 70dB. [8] proposed a gain and slew rate enhancement technique by steering the current in the load PMOS devices. [9] proposed a technique with adaptive bias current based –ve o/p resistance. In this paper, we propose a technique, which enhances the output impedance through positive feedback, without having any latch-up issue [10][11]. The proposed technique is also insensitive to PVT variation. The rest of the paper is organized as follows. Section II explains the proposed technique and section III presents implementation details of the technique. Section IV discusses the simulation results and comparing them with existing techniques.

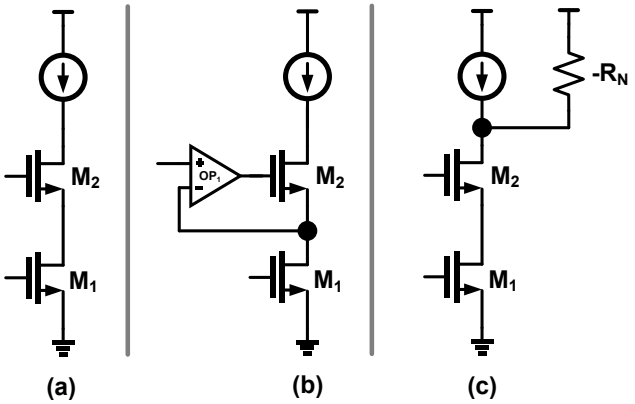

Fig.2. (a) Cascode technique (b) Gain boosting (c) Negative resistance based gain boosting.

2. Proposed Technique

Fig. 3(a) shows the simple common source amplifier, where M_1 acts as a transconductance amplifier, whose gain can be expressed as $g_{m1}r_{01}$. To increase the gain either g_m or r_o can be increased, but increasing g_m will impact the linear range of the amplifier and requires additional power. This means that exploring techniques to increase r_o would result in much higher voltage gain improvement with minimal extra power penalty. Using a cross-coupled negative resistance would increase the impedance, but the transistors will experience a high voltage swing, hence they are not robust against PVT variations and mismatch. From basic feedback theory, shunt negative feedback will decrease the output impedance, whereas positive feedback will increase it. Based on this principle, we propose a method to increase r_o, as shown in Fig. 3(b). One major issue with the previously proposed positive feedback-based boosting technique [6] is that a very large signal will appear as input to the feedback devices, which is the main reason for the latch-up problem. We propose a local positive feedback around the output with a transconductance g_{mf} followed by an attenuator of value β such that the output swing at the Vx node will be attenuated by β. Hence g_{mf} doesn't experience full swing. Assuming

the output impedance of M_1 is r_{o1}, the loop-gain of the circuit is $g_{mf}r_{01}\beta$, and output impedance can be expressed as (3). Hence by increasing the loop-gain, one could obtain very high impedance. Interestingly, by adjusting β according to (4), we could achieve infinite impedance.

$$r_{out} = \frac{r_{01}}{1-g_{mf}r_{01}\beta} \tag{3}$$

$$\beta = \frac{1}{g_{mf}r_{01}} \tag{4}$$

To implement an attenuator whose gain function is proportional to $g_{mf}r_0$, a simple potential divider will not work because of its passive nature. Here, we could again explore the positive-feedback technique to implement this attenuator. Since the closed loop-gain of any feedback network is equal to the inverse function of the feedback network, by using an amplifier in the feedback path we could implement the required β.

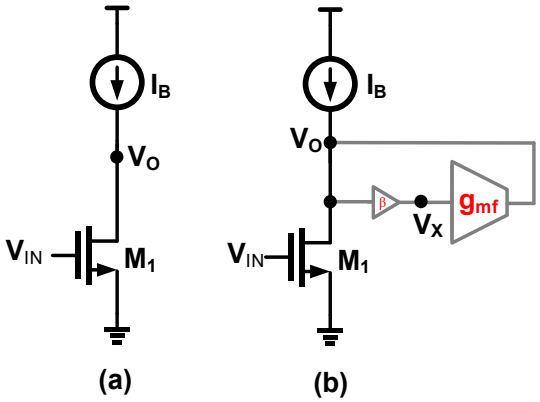

Fig. 3. (a) Simple common Source Amplifier (b) Concept of the proposed technique

Fig. 4 shows the proposed attenuator concept. g_{m3} receives an input signal from the amplifier output (V_0) and converts it into current. The g_{m3} output is loaded with the negative feedback loop formed by $-g_{m3}$, g_{m2}. The impedance looking into this loop can be expressed as:

$$Z_{FB}=\frac{1}{g_{m3}g_{m2}r_{02}} \tag{5}$$

The equivalent impedance at node X is the parallel combination of r_{01} and Z_{FB} and is given by:

$$Z_X = \frac{r_{01}}{1+g_{m3}g_{m2}r_{01}r_{02}} \tag{6}$$

The voltage at node X can be expressed as:

$$V_X = V_o \frac{g_{m3}r_{01}}{1+g_{m3}g_{m2}r_{01}r_{02}} \approx V_o \frac{1}{g_{m2}r_{02}} \text{ Hence } \beta=\frac{1}{g_{m2}r_{02}} \tag{7}$$

Equation (7) reveals that the proposed attenuator gives attenuation inversely proportional to the gain of an amplifier and node x contains the attenuated signal of the amplifier output. Fig. 5 shows the block diagram of the proposed amplifier including the attenuation network. By substituting (7) into (2), we could express the gain of the amplifier as:

$$\frac{V_0}{V_{IN}} = \frac{g_{m1}r_{01}}{1-\frac{g_{mf}r_{01}}{g_{m2}r_{02}}} \tag{8}$$

Looking at equation (8), we notice that by increasing the g_{mf} one could increase the gain because the denominator decreases. More importantly, the denominator consists of a ratio of g_m's and r_o's, which will result in robustness against PVT corners and component mismatch. Although we show transistor M_1 along with other transconductors, we could also replace the transistor with a simple transconductor, say g_{m1}. The linearity of the attenuator is strongly dependent on the linear range of g_{m2}. The voltage swing at node x, however, is very low, hence a simple differential pair would be sufficient from the linearity point of view without the need for source degeneration [10][11].

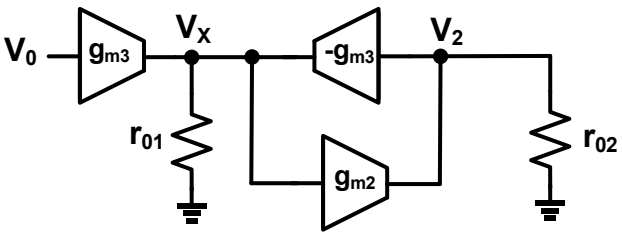

Fig. 4. Attenuation Network (β) concept

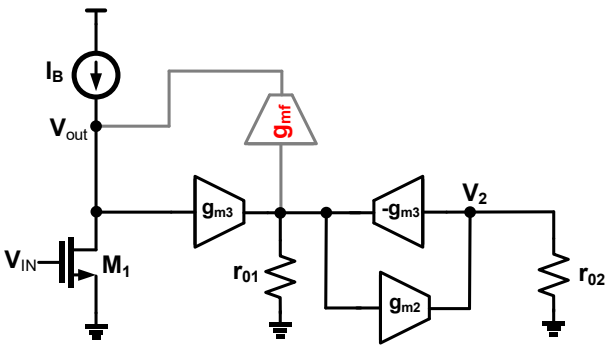

Fig. 5. Proposed amplifier block level schematic

3. Implementation Details.

A fully differential version of the proposed amplifier has been designed to demonstrate its high gain enhancement in comparison with a conventional cascode amplifier. Fig. 6 shows the block diagram of the implementation. For simplicity, the node parasitic capacitance and resistance are not shown on the schematic, however they have been considered in the analysis. In the proposed design, only g_{m1} requires a high bias current and the rest of the g_m stages require very small bias currents. This is because the unity gain bandwidth (UGB), noise and input referred mismatch are strongly dependent on g_{m1}, hence its current needs to be adjusted to meet the design specifications.[12] Fig. 7 shows the implementation of the transconductance, M_{1a}, M_{1b} are the input devices and M_{2a}, M_{2b} act as active loads. The gain of this amplifier can be expressed as $g_{m1a}.r_{02a}$. Since we are trying to show the gain enhancement, we have chosen a simple amplifier without having a cascode to demonstrate the ultra-low voltage capability of the amplifier. One drawback however, of the fully differential amplifier is the necessity of a common mode feedback (CMFB) circuit. Instead of using the traditional CMFB with an extra opamp and large resistors for sensing the common-mode, for sensing we have used two transistors (M_{ca}, M_{cb}) biased in the triode region. Their equivalent impedance is inversely proportional to the output common mode voltage (V_{ocm}) [2] and expressed as follow:

$$R_{eq} = \frac{1}{2\mu_n C_{ox}\frac{W}{L}(\frac{V_{op}+V_{on}}{2}-V_{th})} \tag{9}$$

When the V_{ocm} increases, R_{eq} will increase, hence, the degeneration resistance of M_{2a}, M_{2b} increases, and V_{ocm} will decrease[17]. Unfortunately, this CMFB output common mode voltage is sensitive to Process, Voltage and Temperature (PVT) variations.

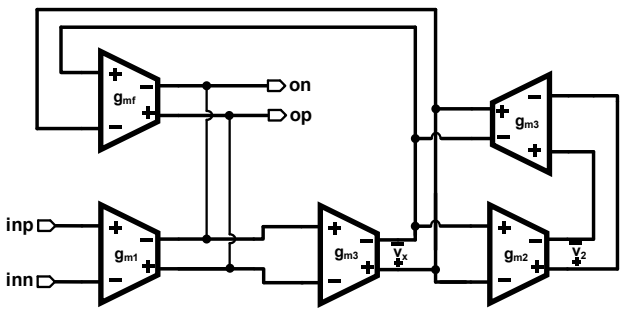

Fig. 6. Fully differential Implementation.

To overcome this disadvantage, we proposed a replica-based bias circuit for M_{2a} and $M_{2b,}$ such that the resulting output common mode voltage is insensitive to PVT variations. The replica circuit consists of M_{c1}, M_{c2}, M_{c3}, M_{t2}. The size of $M_{c1}$and M_{c2} are equal to M_{ca} and M_{2a} to represent the common mode equivalent of the amplifier. The M_{c1}

gate is biased with the required output common voltage reference (V_{OCM}), and M_{c3} is biased with the input common mode voltage (V_{ICM}). The replica circuit adjusts the gate voltage of M_{c2} such that the desired output common mode voltage is reached. An advantage of this implementation of the CMFB in comparison to the conventional opamp-based CMFB is that there is no common stability concern and consequently no need to use a large compensation capacitor [19]. The g_m shown in Fig. 7 has been deployed in Fig. 6, with different bias currents to obtain the appropriate g_m values. The denominator of (8) decides how much gain enhancement is achieved; too high a value reduces the voltage gain, and too low a value will compromise the noise figure[15][16]. From the simulation results, we found that the optimal denominator value is ~0.08 ($\frac{g_{mf}r_{01}}{g_{m2}r_{02}} = 0.92$). By choosing an appropriate bias current a ~12.9 times gain enhancement has been achieved.

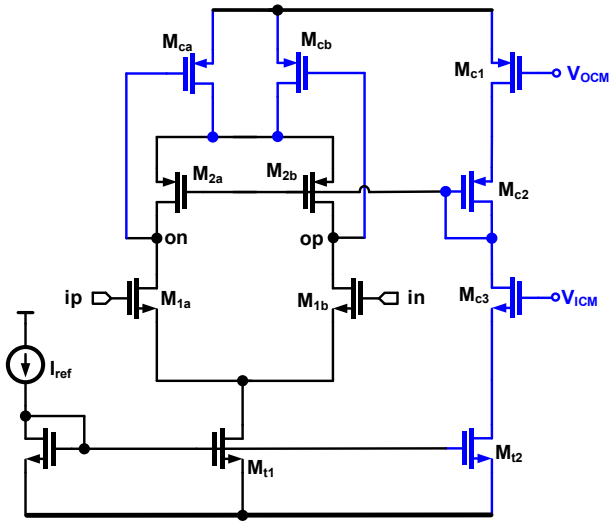

Fig. 7. Gm stage with the proposed CMFB

4. Simulation results.

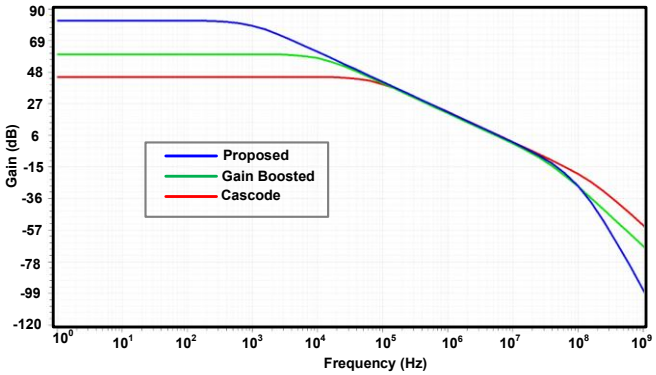

Fig. 8. Frequency response of the proposed and existing techniques.

The proposed technique has been implemented in 65nm CMOS TSMC technology. To compare the gain enhancement with the existing techniques, a cascode amplifier and a gain-boosted amplifier [3] have also been designed. Fig. 8 shows the simulated frequency response of the amplifiers. Simulation results show a low-frequency gain of 45, 60 and 82 dB for the cascode, gain-boosted and the proposed amplifier respectively. This shows that the proposed technique has enhanced the gain by 22dB over the current state of the art technique. The sharp roll-off (60dB/decade) in the frequency response at frequencies well above the UGB is due to the few non-dominant poles contributing to the frequency response as a result of using several stages.

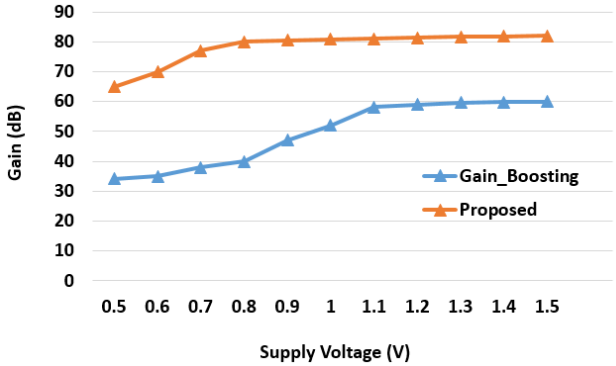

Fig. 9. Supply Sensitivity of the Gain for the proposed and gain boosting technique

As explained in the previous section, this technique can be applied in a simple op-amp or cascode amplifier. However, to enable low voltage operation we have implemented the technique without a cascode. Fig. 9 shows the gain versus the power supply voltage (vdd). The implemented technique works without losing its gain for power supplies as low as 0.7V, whereas the traditional techniques [3][6][13] starts to lose gain as soon as the supply drops below 1.1V. This shows that the proposed technique yields the maximum possible gain with the lowest supply voltage. Unlike any other positive

feedback-based gain enhancement technique, this technique does not suffer from latch-up issues. To demonstrate this, a Monte-Carlo simulation has been carried out with local mismatch models [20]. Fig. 10 depicts the gain histogram and shows an 82dB mean and 1dB standard deviation. Such a low standard deviation indicates there is no latch-up issue [21]. The layout of the proposed circuit is shown in Fig. 11, and the active area is 56µm*49µm. Every transistor has been laid with proper care to avoid mismatch. Special care has been taken for well proximity effect (WPE) and shallow trench isolation (STI), by adding enough dummies for each device and keeping MOSFET away from NWELL[14]. Table-I describes the transistor dimensions of the proposed technique and table-II summarizes the performance parameters of the proposed design and some of the previous proposals. This technique out performs the some of the critical parameters like small & large signal FOM[17]

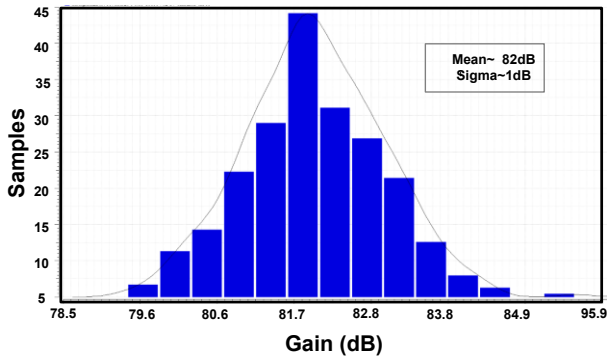

Fig. 10. Histogram of the voltage gain (dB)

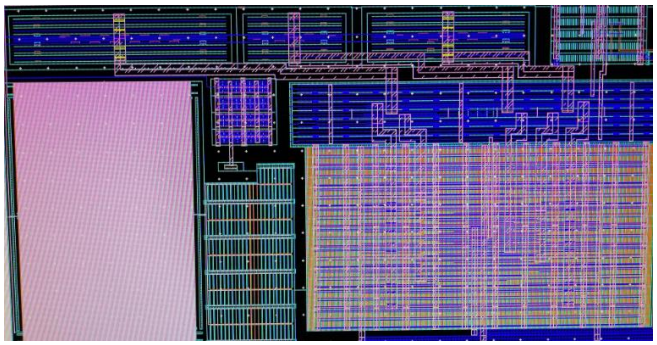

Fig. 11. Layout of the proposed Circuit.

TABLE-I Transistor dimension

Name	Size (W/L)	Name	Size (W/L)	Name	Size (W/L)
M_{t0}	6/.25	M_{1b}	8/.5	M_{1b}	6/.5
M_{t1}	6/.25	M_{c3}	2/.5	M_{ca}	16/.5
M_{t2}	6/.25	M_{2a}	24/.5	M_{cb}	16/.5
M_{1a}	8/.5	M_{2b}	24/.5	M_{c1}	4/.5

TABLE-II Performance Summary

Parameter	This work	[8]	[9]	Units
Minimum Supply Voltage	0.8	1.8	1	V
Current consumption	295	362	85	µA
Voltage Gain	82.7	74	79	dB
Standard deviation of Gain	1	-	-	dB
Unity Gain Bandwidth	12	160	4.7	MHz
Slew rate	31.3	26.8	17	V/µS
Integrated Noise	19.8	-	-	nV
CMRR	72	-	142	dB
FOMS	1525	773	3284	MHz.pF/mW
FOML	3978	129	829	(V/µS).pF/mW
Technology	65	180	350	nm
Area	5000	-	-	µm2

5. Conclusion

In this paper a positive feedback based opamp gain enhancement technique has been proposed. With this technique, opamp gain is very much insensitive to the PVT variation and unlike other proposed techniques this solution has no latch-up problem.

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