THEORY AND METHODOLOGY OF INTEGRATED LADDER FILTER DESIGN

A Thesis submitted to the

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TO MY PARENTS

SUMMARY

This thesis presents a systematic study of integrated ladder filter design. A theoretical model of ladder structures is first established in terms of a family of symmetric matrix polynomial systems (SMPS's). It is shown that SMPS's are a natural mathematical abstraction of ladder circuits. The properties of stability, canonical (or minimal) realisation, low–sensitivity and low–noise, are proved for SMPS's under certain very simple conditions.

A design methodology is then presented for active–RC, SC and digital ladders. The basic principle is that a SMPS can be decomposed by means of matrix factorisation into several linear systems, which can then be easily realised by active or digital circuits. It is shown that many existing methods, such as leapfrog or coupled biquads, result from some special decompositions. It is further shown that LU and UL factorisations drawn from numerical methods can be used to develop several novel structures (so–called LUD and ULD structures) which demonstrate significant improvments over existing ones regarding sensitivity, component area and dynamic range. This is confirmed by examples and statistical investigations.

Besides the matrix methods applicable to standard lowpass and bandpass cases, further research is undertaken for bandstop, highpass and allpass filter designs. It is demonstrated that frequency transformations can be used to reduce the hardware cost in many classical filtering cases. A novel building block, the so called TWINTOR, is introduced in bandstop design to reduce the switching rate. Active–RC and SC allpass ladders are constructed and proved to have significant advantages over the existing biquad circuits.

Matrix methods also provide an efficient vechicle for the development of a filter design software package called PANDDA. Its many outstanding features are described.

Finally measured results from two fabricated LUD SC filters are presented. They confirm the high quality of the novel circuit structures developed by this research.

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1.1 BACKGROUND

Filter circuits are of great importance in communication systems, signal processing and control devices. They direct, channel, separate and transform electrical signals.

The majority of voice band filters were realised as RLC passive circuits, Fig.1.1a, [1−11] until the 1960s when it was recognised that size and eventual cost reduction could be achieved by replacing the large, costly inductors with active−RC networks, Fig.1.1b, [12−21]. The progress of integrated circuit (IC) technology, such as the monolithic operational amplifier and the thick and thin−film circuits, later enabled one to realize high−quality, miniature, hybrid active−RC circuits with very low cost. With the emergence of VLSI (Very Large Scale Integration) technology in the 1970's, it became possible to realise high order analogue filters on microminiature silicon chips [13,22−25].

In VLSI, it is easier to fabricate capacitors and switches than resistors with the required accuracy. This gave rise to a new analogue sampled−data system, the switched capacitor (SC) circuits, Fig.1.1c, [25−72]. Recent interest has grown in Gallium−Arsenide (GaAs) implementations of SC circuits for high frequency applications [31,41].

In the last two decades, digital filters (Fig.1.1d) have been increasingly employed in communications, signal processing and control functions [73−94]. This is due to the accuracy, flexibility, programmability and modularity of digital systems, in addition to the high level of integration achievable in VLSI.

1.2 NETWORK ANALYSIS AND MATRIX PRINCIPLES

Circuit theory is now divided into two major branches; analysis and design, each with its own distinct methodology. In circuit analysis, methods have been developed to handle systematically large, sparsely connected networks, a task which has been expedited by modern matrix and graph theory [95,96]. This rationalisation has not been reflected in the field of circuit design. Design methods, more or less, still focus on local building blocks rather than take an overall view of target systems.

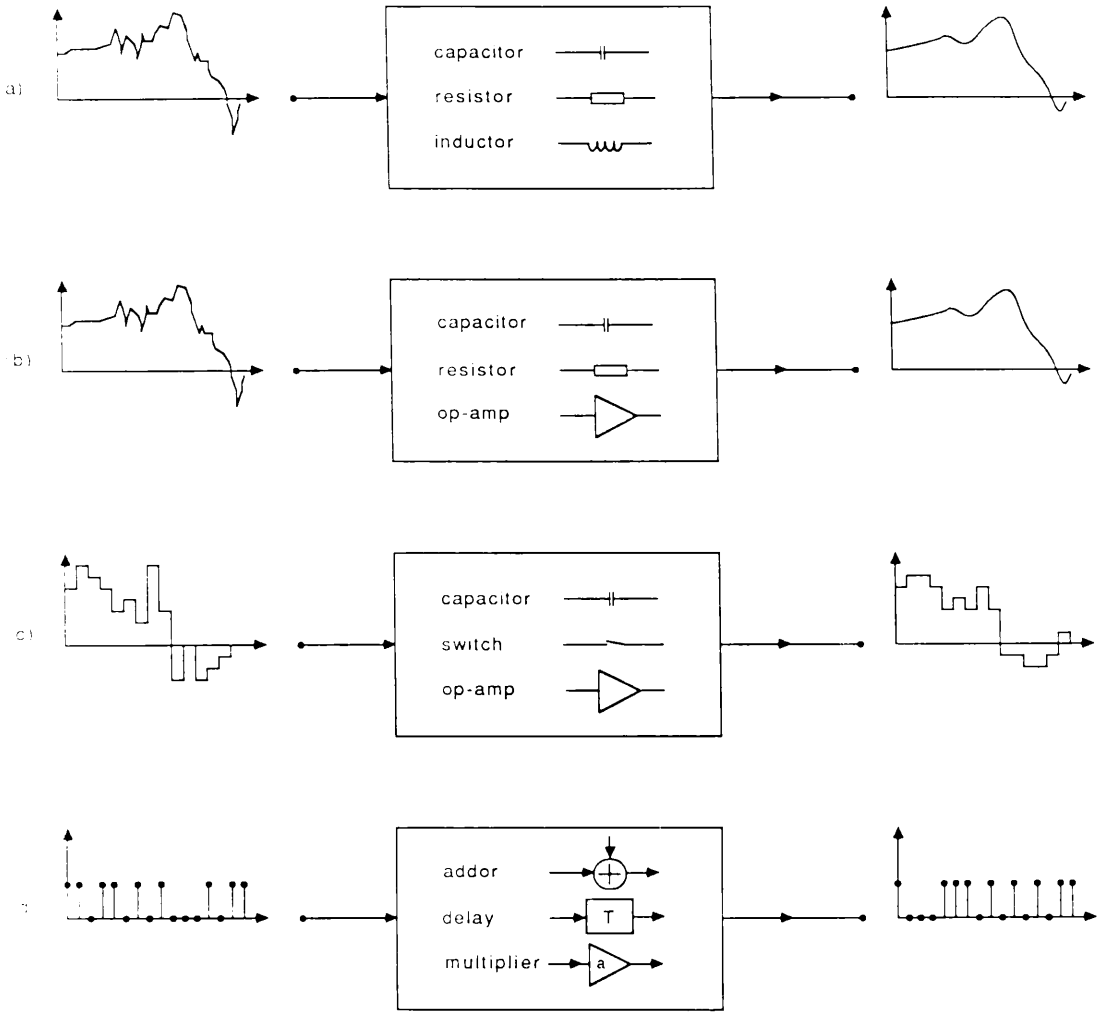


Fig. 1.1 Various circuit implementations of electronic filters

(a) Passive RLC filter

(b) Active– RC filter

(c) Switched– capacitor filter

(d) Digital filter

The strategy of the research presented in this thesis is to incorporate network analysis techniques in circuit design. For this reason a brief review of circuit analysis is necessary.

1.2.1) Formulation of passive network descriptions

Nodal approaches are most popular in formulating network equations. Suppose a network has n ungrounded nodes and m passive admittance elements. Let J_i be the current flowing into the i^{th} node from n external independent current sources. The network behaviour is described by an admittance matrix equation of the form [95,96]:

$$\begin{bmatrix} y_{11} & y_{12} & \cdots & y_{nn} \\ y_{21} & y_{22} & \cdots & y_{2n} \\ \cdots & \cdots & \cdots & \cdots \\ y_{n1} & y_{n2} & \cdots & y_{nn} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ \vdots \\ v_n \end{bmatrix} = \begin{bmatrix} J_1 \\ J_2 \\ \vdots \\ J_n \end{bmatrix} \qquad (1.1)$$

or

$$Y\ V = J \qquad (1.2)$$

Topological matrix decomposition:

Y can be decomposed on a topological basis as [96]

$$Y = A\ Y_b\ A^T \qquad (1.3)$$

where $\mathbf{Y_b} = \text{diag}\ \{ y_1, y_2, \ldots y_m \}$ is a m×m diagonal matrix and **A** is a n×m incidence matrix defined by

$$a_{ij} = \begin{cases} -1 & \text{if branch j is incident to and directed towards node i} \\ 0 & \text{if branch j is not incident to node i} \\ 1 & \text{if branch j is incident to and directed outwards from node i} \end{cases} \qquad (1.4)$$

Polynomial expression of the admittance matrix:

For an RLC network, the contributions of capacitor C_k, inductor L_k and conductors G_k to the admittance matrix are, respectively, sC_k, $s^{-1}L_k^{-1}$ and G_k. Consequently Y is a matrix polynomial in s with

$$Y = s C + s^{-1} \Gamma + G \qquad (1.5)$$

Notice here Γ consists of the inverse inductance values. C, Γ and G can also be topologically decomposed by considering only the capacitance, inductance or resistance subnetworks respectively.

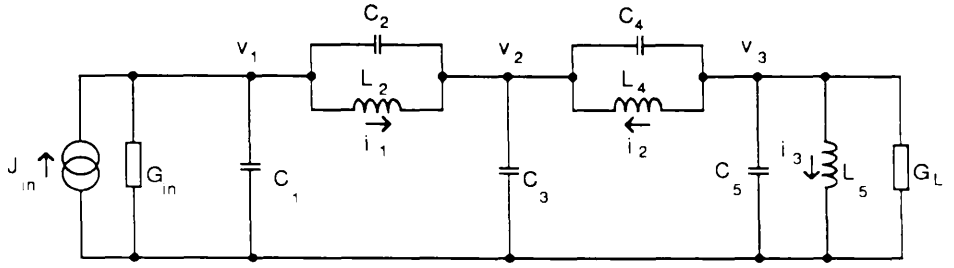


Fig. 1.2 A 6th order passive doubly– terminated ladder filter

Example 1.1: For a 6th order ladder, Fig.1.2, the nodal formulation leads to the following matrix equations,

$$\left\{ s \begin{bmatrix} C_1+C_2 & -C_2 & \\ -C_2 & C_2+C_3+C_4 & -C_4 \\ & -C_4 & C_4+C_5 \end{bmatrix} + s^{-1} \begin{bmatrix} L_2^{-1} & -L_2^{-1} & \\ -L_2^{-1} & L_2^{-1}+L_4^{-1} & -L_4^{-1} \\ & -L_4^{-1} & L_4^{-1}+L_5^{-1} \end{bmatrix} + \right.$$

$$\left. + \begin{bmatrix} G_{in} & & \\ & 0 & \\ & & G_L \end{bmatrix} \right\} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix} = \begin{bmatrix} J_{in} \\ 0 \\ 0 \end{bmatrix} \qquad (1.6a)$$

and the topological decompositions of C and Γ are

$$C = \begin{bmatrix} 1 & 1 & & \\ & -1 & 1 & 1 \\ & & -1 & 1 \end{bmatrix} \begin{bmatrix} C_1 & & & & \\ & C_2 & & & \\ & & C_3 & & \\ & & & C_4 & \\ & & & & C_5 \end{bmatrix} \begin{bmatrix} 1 & \\ 1 & -1 \\ & 1 \\ & 1 & -1 \\ & & 1 \end{bmatrix} \qquad (1.6b)$$

$$\Gamma = \begin{bmatrix} 1 & & \\ -1 & 1 & \\ & -1 & 1 \end{bmatrix} \begin{bmatrix} L_2^{-1} & & \\ & L_4^{-1} & \\ & & L_5^{-1} \end{bmatrix} \begin{bmatrix} 1 & -1 & \\ & 1 & -1 \\ & & 1 \end{bmatrix} \qquad (1.6c)$$

1.2.2) Ladder system matrices: sparse and symmetric

If a ladder circuit is labelled so that every node i is joined only to either nodes i−1 or i+1 or both, Fig.1.2, then matrices **C**, **Γ**, **G** and so **Y** are all tridiagonal, as can be seen from (1.6a). Therefore ladders are typical sparse systems [97].

From (1.3) it is seen that **C**, **Γ**, **G** and **Y** are all symmetric matrices. Furthermore it is easy to verify that **C**, **Γ** and **G** are non−negative definite [98] provided that only positive RLC elements are considered. Notice that the reverse is not always true. For example, let matrices **C** and **Γ** be

$$C = \begin{bmatrix} 2 & 1 \\ 1 & 2 \end{bmatrix} \qquad \Gamma = \begin{bmatrix} 2 & -1 \\ -1 & 2 \end{bmatrix} \qquad (1.7)$$

They are both positive definite but $\mathbf{Y} = s\mathbf{C} + s^{-1}\mathbf{\Gamma}$ can not be realised by an RLC circuit with positive elements.

1.2.3) LU and UL matrix decompositions

The solution of the algebraic equations,

$$\mathbf{Y}\,\mathbf{V} = \mathbf{J} \qquad (1.8)$$

can be performed by the *triangular* or *LU decomposition* technique [95,99]. The main advantage of LU decomposition over Gaussian elimination is that it enables efficient solution of system with different excitation vectors **J**. By LU decomposition a matrix **Y** is factorised as follows

$$\mathbf{Y} = \mathbf{L}\,\mathbf{U} \qquad (1.9)$$

where **L** stands for the *lower triangular* and **U** for the *upper triangular* matrix. The system (1.8) is now written as

$$\mathbf{L}\,\mathbf{U}\,\mathbf{V} = \mathbf{J} \tag{1.10}$$

Define an auxiliary vector **W** as

$$\mathbf{U}\,\mathbf{V} = \mathbf{W} \tag{1.11}$$

Substitute **W** into (1.10)

$$\mathbf{L}\,\mathbf{W} = \mathbf{J} \tag{1.12}$$

Due to the special form of **L** and **U**, the vectors **W** and the solution **V** can be calculated very efficiently. Consider the most simple case when **Y** is tridiagonal so that **L** and **U** will have the form,

$$\mathbf{L} = \begin{bmatrix} l_{11} & & & & \\ l_{21} & l_{22} & & 0 & \\ & l_{32} & l_{33} & & \\ & & \ddots & \ddots & \\ & 0 & & l_{n(n-1)} & l_{nn} \end{bmatrix} \tag{1.13a}$$

and (notice the unity valued entries on the main diagonal of U)

$$\mathbf{U} = \begin{bmatrix} 1 & u_{12} & & & \\ & 1 & u_{23} & 0 & \\ & & 1 & u_{34} & \\ & & & \ddots & u_{(n-1)n} \\ & 0 & & & 1 \end{bmatrix} \tag{1.13b}$$

The solution of (1.12) can then be written as

$$w_1 = J_1/l_{11}$$
$$w_i = J_i/l_{ii} - [l_{i(i-1)}/l_{ii}]w_{i-1} \qquad i=2,3,\ldots n \tag{1.14a}$$

This is called the *forward substitution* process, Fig.1.3a. To solve for the unknown vector **V** in (1.11), start with the last equation and work upward,

$$v_n = w_n$$
$$v_i = w_i - u_{i(i+1)}w_{i+1} \qquad i=n-1,n-2,\ldots 1 \tag{1.14b}$$

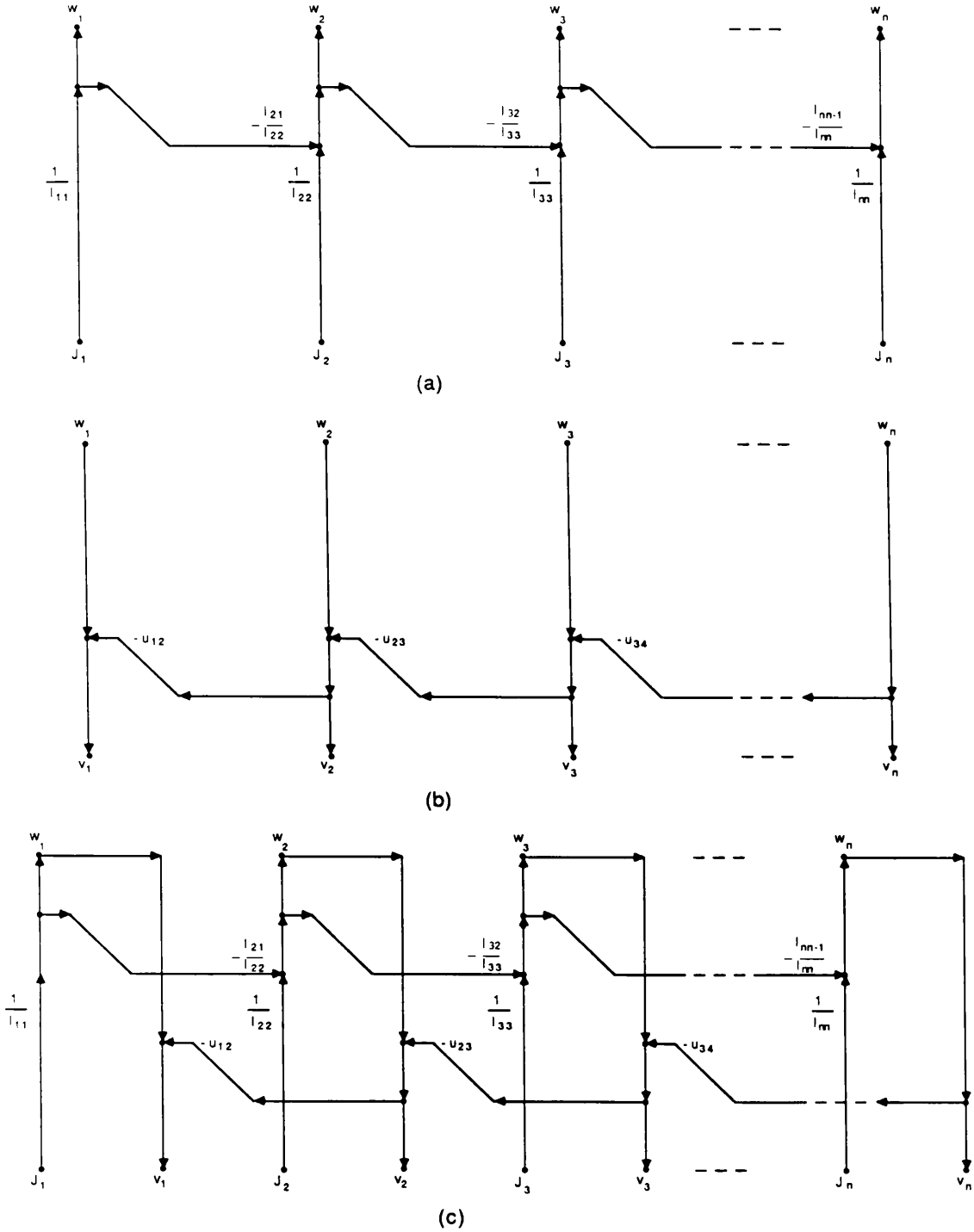


Fig. 1.3 Signal–flow–graph for solving a linear system by LU decomposition method

(a) Forward substitution

(b) Backward substitution

(c) Overall process

This process is called *backward substitution*, Fig.1.3b. The whole forward and backward procedures can be visualised in a signal–flow–graph (SFG) form, Fig.1.3c. Notice a special relationship for (1.14) and Fig.1.3; *if* **Y** *is symmetric then* [99]

$$l_{i(i-1)}/l_{ii}=u_{i(i+1)} \tag{1.15}$$

A similar procedure can be developed if **Y** is factorised by UL decomposition,

$$\mathbf{Y} = \mathbf{U}\,\mathbf{L} \tag{1.16}$$

A SFG is given in Fig.1.4 for solving (1.8) via (1.16). Again if **Y** is symmetric then (1.15) holds.

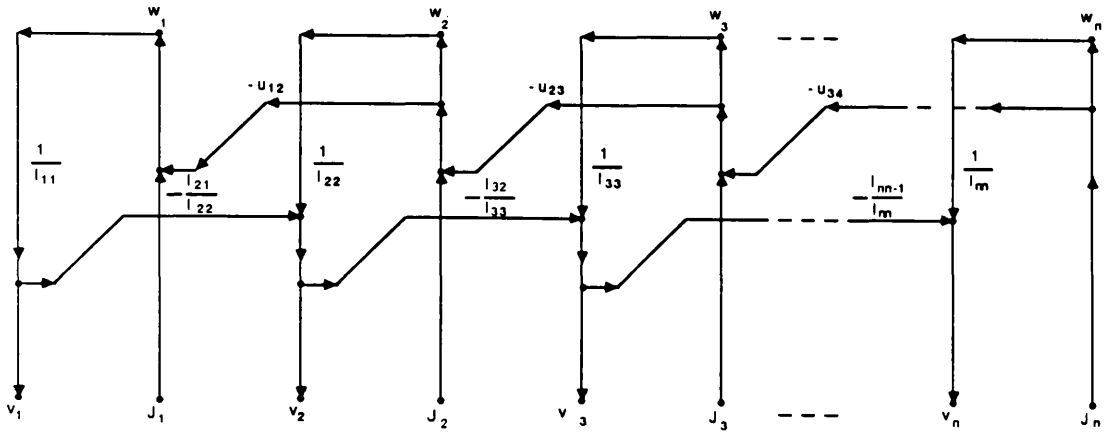


Fig. 1.4 Signal–flow–graph for solving linear system by UL decomposition method

1.3 FILTER DESIGN METHODS

Generally speaking there are two approaches to filter structure design; direct methods and simulation methods. The former starts directly from a transfer function, either as a single polynomial or ratio of polynomials, and the networks are derived by some algebraic expansions of the transfer function. The latter transforms some prototype circuit into different implementations while preserving the transfer function. This is done in order to inherit certain beneficial properties from the prototype. Examples of direct design methods are:

1) direct realisation without any expansion, *e.g., follow–the–leader* type circuits [12,73]
2) expansion into the product or sum of second order sections, *e.g., cascade, parallel biquads and allpass LC lattice* [1,12,73]
3) expansion into partial fraction form, *e.g., ladder and Gray–Markel's digital lattice* [2,3,82]

A simulation is based on some sort of one–to–one correspondance between the prototype and the simulated circuit [3,12,73]. This correspondance could be between the port characteristics of the components in the two circuits, called component simulation, or between the signal–flow–graphs (SFGs) representing the two circuits, called functional simulation.

Component simulation methods, such as those using gyrators [17,60] and GICs [18] to simulate inductors, generally require floating opamps or floating capacitors which are prone to errors during manufacture. Functional simulation methods have been more successfully developed and have found wide industrial application, especially for SC circuits [19–21, 51–59]. They form the main topic investigated in this thesis.

1.3.1) Passive ladder and lattice network synthesis

For amplitude filtering the *doubly terminated ladders*, Fig.2, are the most widely used passive structures with well established theory [1–11]. Ladder circuits are well known for their distinguished property of being very insensitive to component deviations.

For delay equalisation, passive all–pass circuits are mostly realised as lattice derived bridged–T networks [1]. They are basically cascade second order filters,

with a unique fixed port resistance for both ports of each section. Since they are impedance matched they can be cascaded without introducing any distortion. Each second order section usually has 5 reactance elements, as shown in Fig. 1.5.

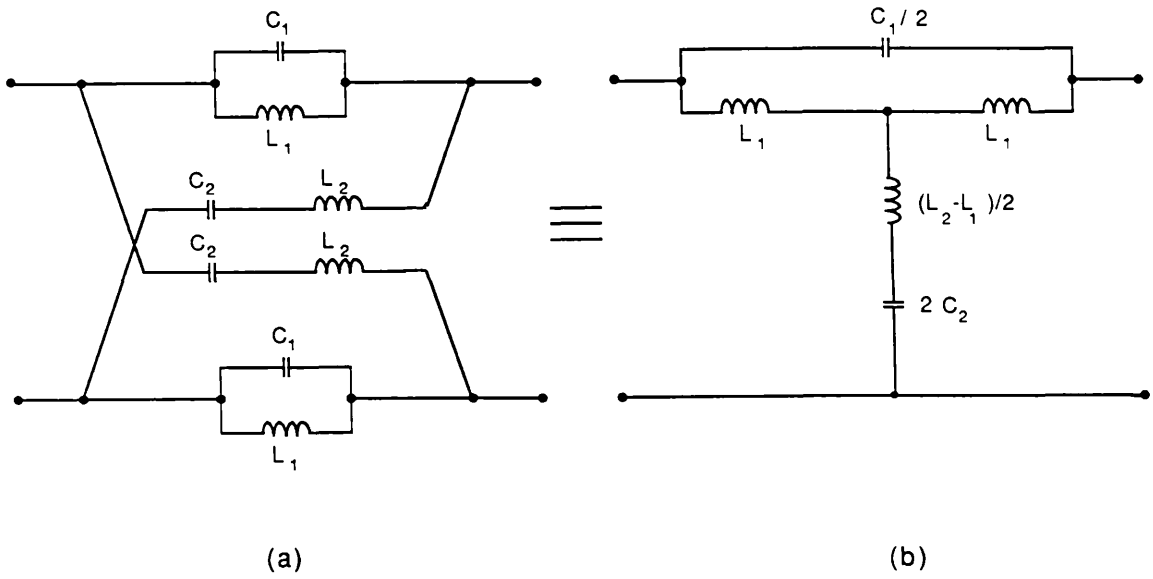


Fig. 1.5 A second order allpass lattice section and its equivalent bridged– T form

1.3.2) First and second order circuit building blocks

Most active and digital networks can be regarded as the repeated connection of a few regular structured subnetworks, so–called building blocks [3,12,16,73].

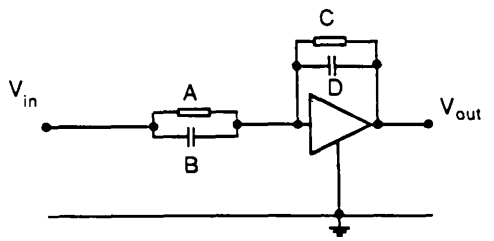
A list of first order active–RC, SC and digital building blocks is given in Fig.1.6. It can be verified that the transfer functions of the circuits in Fig.1.6 are, respectively,

(a) $$H(s) = -(A+sB)/(C+sD) \qquad (1.17a)$$

(b) $$H(z) = [-A(1-z^{-1})+Bz^{-1}-C]/(D+E-Dz^{-1}) \qquad (1.17b)$$

(c) $$H(z) = (b_0+b_1z^{-1})/(1+a_1z^{-1}) \qquad (1.17c)$$

(a)



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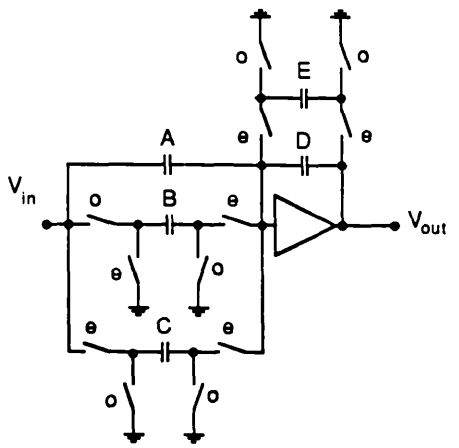

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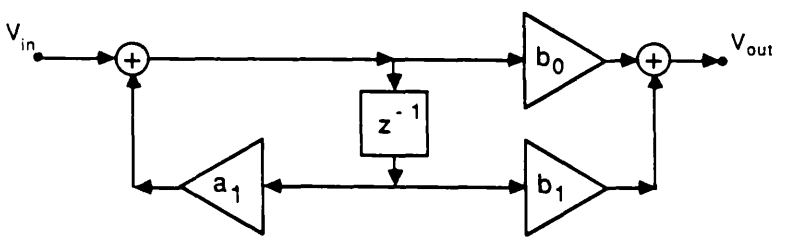


Fig. 1.6 First order building blocks

(a) Active– RC circuit

(b) Switched– capacitor circuit

(c) Digital circuit

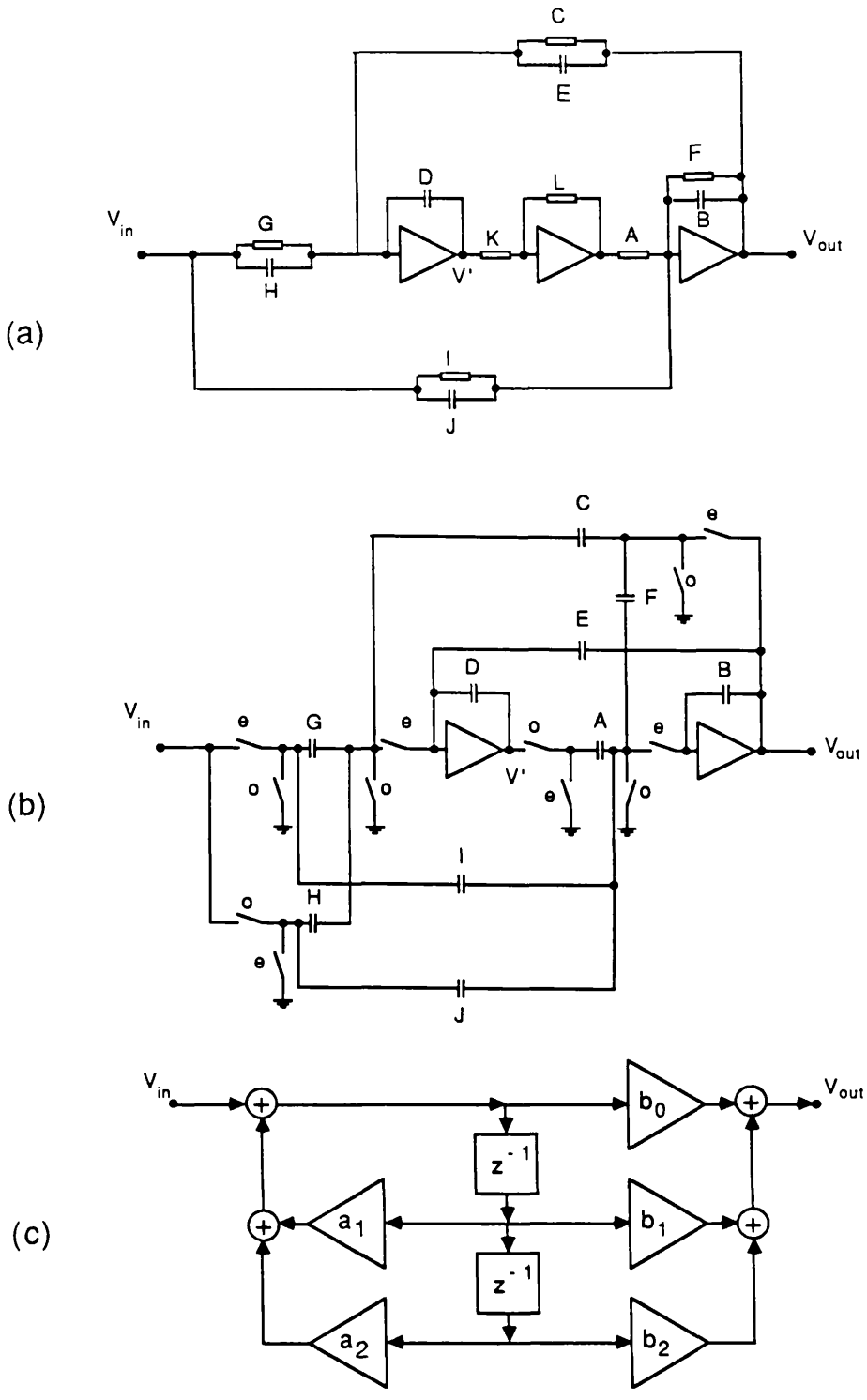


Fig. 1.7 Second order building blocks

(a) Active– RC circuit

(b) Switched– capacitor circuit

(c) Digital circuit

Second order building blocks, more often referred to as biquad sections, are particular useful as they can be assembled to form cascade or parallel biquad structures, based on the fact that any real rational function H(p) (p may be either s or z for the continuous domain or the discrete domain respectively) can be factorised as,

$$H(p) = \prod \frac{b_{0i} + b_{1i}p^{-1} + b_{2i}p^{-2}}{a_{0i} + a_{1i}p^{-1} + a_{2i}p^{-2}} \qquad (1.18a)$$

or alternatively can be partial fractioned as

$$H(p) = \sum \frac{d_{0i} + d_{1i}p^{-1} + d_{2i}p^{-2}}{c_{0i} + c_{1i}p^{-1} + c_{2i}p^{-2}} \qquad (1.18b)$$

The design of cascade and parallel biquads can be easily carried out using the active–RC, SC and digital biquads shown in Fig.1.7, with the transfer functions,

$$\text{(a)} \quad H(s) = -\frac{DLJ+(HKA+DLI)s^{-1}+GKAs^{-2}}{DLB+(DLE+FKA)s^{-1}+(CKA)s^{-2}} \qquad (1.19a)$$

$$\text{(b)} \quad H(z) = -\frac{DI+(AC-DI-DJ)z^{-1}+(DJ-AH)z^{-2}}{D(F+B)+(AC+AE-DF-2DB)z^{-1}+(DB-AE)z^{-2}} \qquad (1.19b)$$

$$\text{(c)} \quad H(z) = \frac{b_{0i} + b_1z^{-1} + b_2z^{-2}}{1 + a_1z^{-1} + a_2z^{-2}} \qquad (1.19c)$$

It is also convenient to separate the active–RC and SC realisations using only E–capacitor damping (F= 0) or only F–capacitor damping (E= 0). These two cases are referred to as the E–type and F–type circuits, respectively [12]. In particular, set H= I= 0 in Fig.1.7a, to realise a pair of zeroes on the imaginary axis for active–RC circuits, or set I= J and H= 0, to realise a pair of zeroes on the unit circle for SC circuits. In these cases the transfer functions can be simplified to,

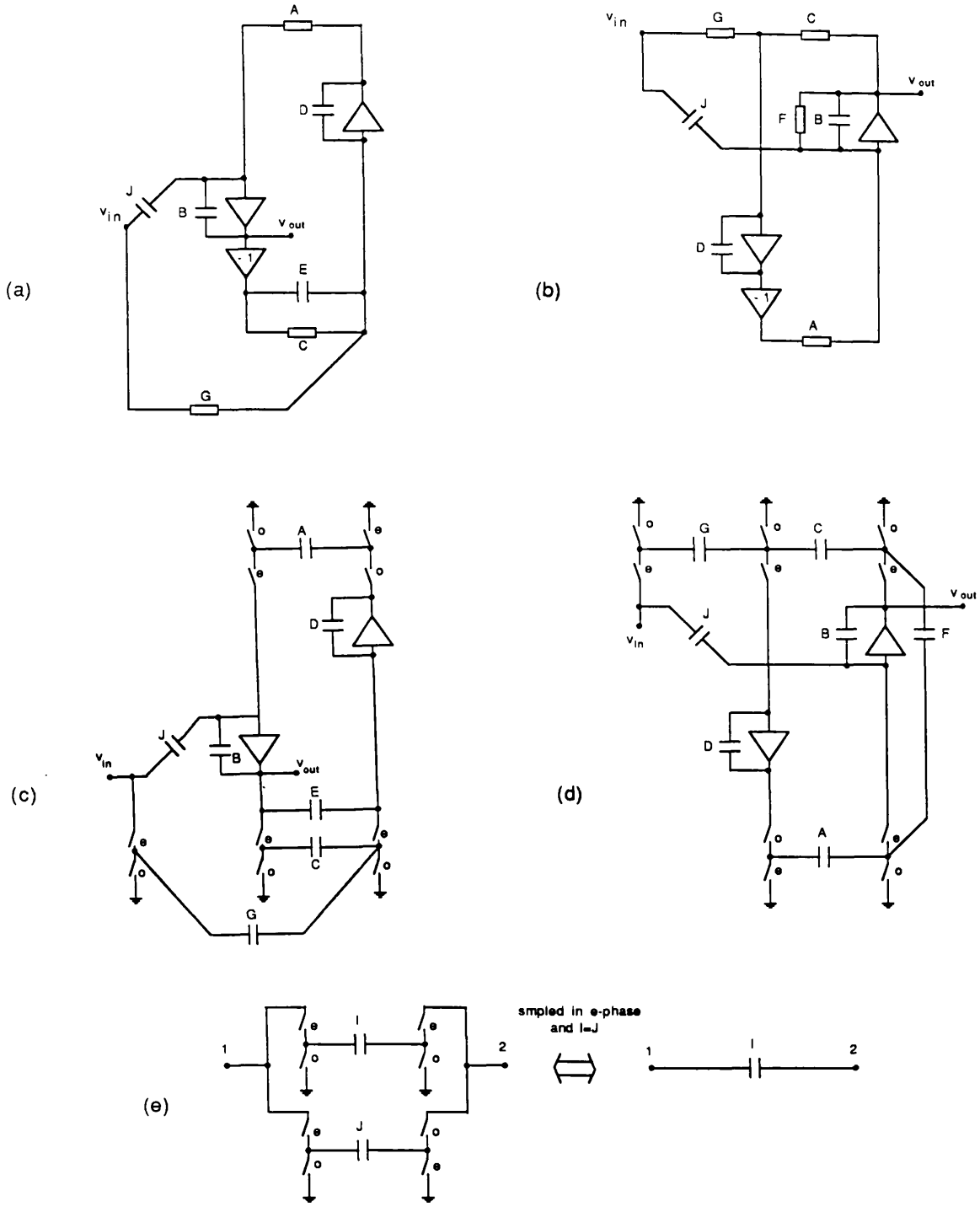


Fig. 1.8 E– type and F– type second order building blocks

(a) E– type active– RC circuit

(b) F– type active– RC circuit

(c) E– type switched– capacitor circuit

(d) F– type switched– capacitor circuit

(e) Switched capacitor circuit equivalence

$$(a) \qquad H(s) = - \frac{DJ+GAs^{-2}}{DB+DEs^{-1}+CAs^{-2}} \qquad \text{with } L=K=1 \qquad (1.20a)$$

$$(b) \qquad H(s) = - \frac{DJ+GAs^{-2}}{DB+FAs^{-1}+CAs^{-2}} \qquad \text{with } L=K=1 \qquad (1.20b)$$

$$(c) \qquad H(z) = - \frac{DJ+(AG-2DJ)z^{-1}+DJz^{-2}}{DB+(AC+AE-2DB)z^{-1}+(DB-AE)z^{-2}} \qquad (1.20c)$$

$$(d) \qquad H(z) = - \frac{DJ+(AG-2DJ)z^{-1}+DJz^{-2}}{D(F+B)+(AC-DF-2DB)z^{-1}+DBz^{-2}} \qquad (1.20d)$$

In Fig.1.8 circuit realisations are given for these special cases. Notice that when I= J, the parallel combination of two switched capacitors is equivalent to a single unswitched capacitor, Fig.1.18e and this property has been used in Fig.1.8c,d. It should also be noticed that the biquads in Fig.1.8 are special examples of the ladder structures developed in this thesis when order= 2 .

Cascade biquads structures are very regular and their design procedure can be easily automated. However they are also notorious for their poor sensitivity and noise behaviour.

The first and second order SC sections listed in Fig.1.6 and 1.7 are all insensitive to grounded stray capacitance [12,32]. This stray− insensitive property is vital for high precision circuit performance in the presence of significant bottom and top plate stray capacitance effects in current MOS technology. For practical considerations, only these stray− insensitive SC building blocks will be used in this thesis.

1.3.3) Ladder simulations for active− RC and SC network design

In 1966 Orchard presented his well− known observation that a properly designed terminated LC ladder would demonstrate very low sensitivity in the passband, with respect to the drift of component values [15]. Since then, various approaches have been proposed to simulate LC ladders by active and digital circuits [17− 21,51− 67,76− 81] to benefit from this important property.

In an operational simulation approach, a set of equations is established which is sufficient to describe the LC ladder prototype. Each equation is then simulated by a simple active or digital network. In a leapfrog design these equations simply represent the voltage–current relationship of individual elements in the prototype [19,20,51], so they are linear with respect to frequency $s = j\omega$. Only first order sections are required to form the network. In a coupled biquad design the equations are set up for the voltage–voltage relationship between nodes and are generally quadratic with respect to s [21,53]. Biquad sections are required in simulation and hence the name.

Example 1.2:

Take a 6th order active–RC ladder design as a example. Use the circuit shown in Fig.1.2 as prototype. In a leapfrog design the following network equations are obtained,

$$\begin{aligned}
c_{11}v_1 &= (-1/s)(i_1 - Jin + g_{in}v_1) - C_2v_2 & c_{11} &= C_1 + C_2 \\
L_1i_1 &= (1/s)(v_1 - v_2) & & \\
-c_{22}v_2 &= (-1/s)(i_1 + i_2) - C_2v_1 - C_4v_3 & c_{22} &= C_2 + C_3 + C_4 \\
L_4i_2 &= (1/s)(-v_2 + v_3) & & \\
c_{33}v_3 &= (-1/s)(i_{2+}g_Lv_3) - C_4v_2 & c_{33} &= C_4 + C_5 \\
L_5i_3 &= (1/s)v_3 & &
\end{aligned} \qquad (1.21)$$

These equations are represented by the SFG shown in Fig.1.9a. To convert the SFG into active–RC circuit, one can use Fig.1.6 and replace the branches in the SFG by the corresponding active–RC branches. The resulting circuit is shown in Fig.1.9b.

In a coupled biquad method the prototype, Fig.1.2, is described by a set of second order eqution,

$$v_1 = \frac{-(s^2c_{12}+\lambda_{12})v_2 - (-sJ_{in})}{s^2c_{11} + sg_{11} + \lambda_{11}} \qquad \begin{aligned} &c_{12}=C_2 \ \lambda_{11}=\lambda_{12}=1/L_2 \\ &c_{11}=C_1+C_2 \ g_{11}=g_{in} \end{aligned}$$

$$-v_2 = \frac{-(s^2c_{21}+\lambda_{21})v_1-(s^2c_{23}+\lambda_{23})v_3}{s^2c_{22} + \lambda_{22}} \qquad \begin{aligned} &c_{21}=C_2 \ \lambda_{21}=1/L_2 \ c_{23}=C_4 \ \lambda_{23}=1/L_4 \\ &c_{22}=C_2+C_3+C_4 \ \lambda_{22}=1/L_2+1/L_4 \end{aligned}$$

$$v_3 = \frac{-(s^2c_{32}+\lambda_{32})v_2}{s^2c_{33} + sg_{nn} + \lambda_{33}} \qquad \begin{matrix} c_{32}=C_4 \;\; \lambda_{32}=1/L_4 \\ c_{33}=(C_4+C_5) \;\; g_{nn}=g_L \;\; \lambda_{33}=1/L_4+1/L_5 \end{matrix}$$

(1.22)

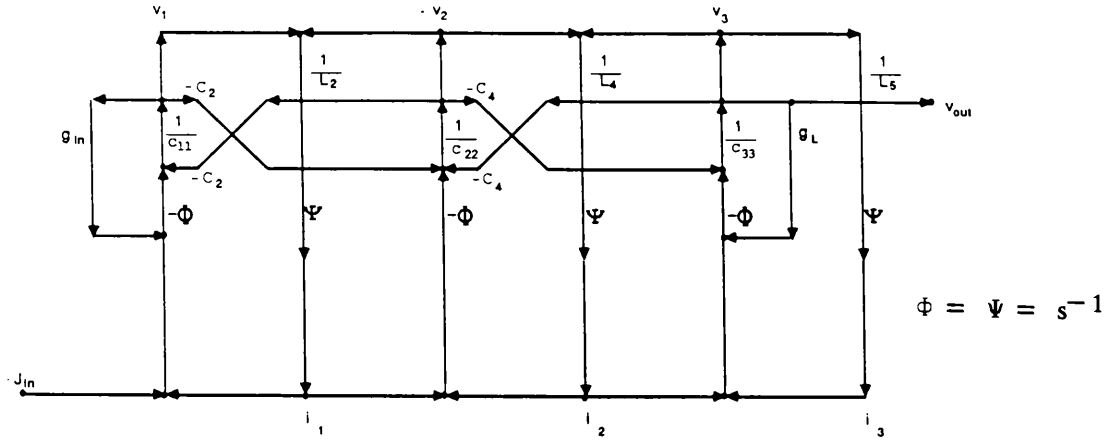
These equations are again represented by the SFG shown in Fig.1.10a (note $a_{ij}=a_{ji}$ and $\lambda_{ij}=\lambda_{ji}$) and can be replaced by connection of second order active–RC E–type biquads in Fig.1.7, resulting in the circuit in Fig. 1.10b.

In the leapfrog method there is a clear link between individual elements in the prototype and the building blocks in the simulated circuit. If the prototypes have an excessive number of components, such as in the bandpass case, an excessive number of integrators will be required. There are various ways to eliminate the redundant opamps [3] but they become tedious even for moderate design orders. In SC design very high capacitance spreads are often observed for bandpass leapfrog design. So normally leapfrog is only considered for the lowpass design case.

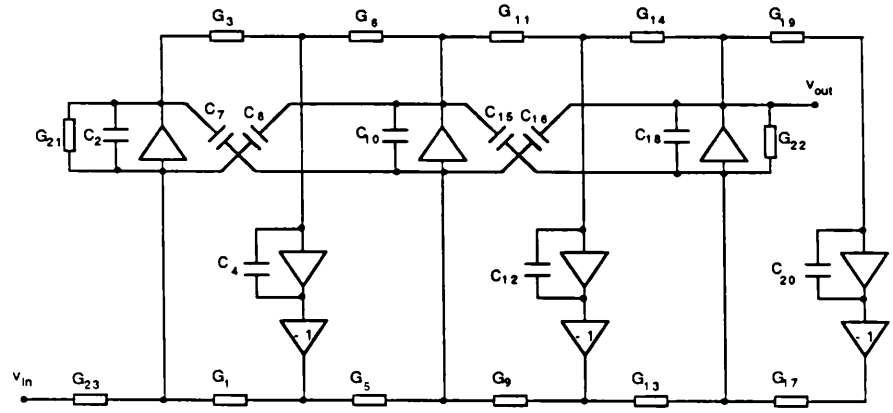
Coupled biquad filters always require an even number of opamps (not including inverters), which doubles the number of nodes. It is only efficient for even order filters whose node number is just half of the order e.g. a bandpass filter frequency–transformed from an odd order lowpass one.

SC simulations of passive ladders follow the same principle although some manipulation is required in adopting LDI type integrators [51,53].

In general leapfrog and coupled biquad active–RC and SC circuits will possess capacitor coupled opamp loops, as shown by the loop $c_2-c_7-c_{10}-c_8$ in Fig.1.9b and $c_4-c_7-c_{12}-c_8$ in Fig.1.10b. These loops are detrimental to the performance of active–RC and SC circuits, since high frequency noise can oscillate around such loops, when non–ideal factors, such as on–switch resistances and finite GB product of the opamps, are included [35]. Examining the SFGs and the circuits carefully, it can be seen that such loops will exist if there are loops in the SFG with constant transmission (without frequency dependent factor s or z). In the z–domain, such loops are called *delay–free–loops*, and they cannot be realised by digital circuits. This explains why leapfrog and coupled–biquad methods are difficult to apply to digital filter



(a)



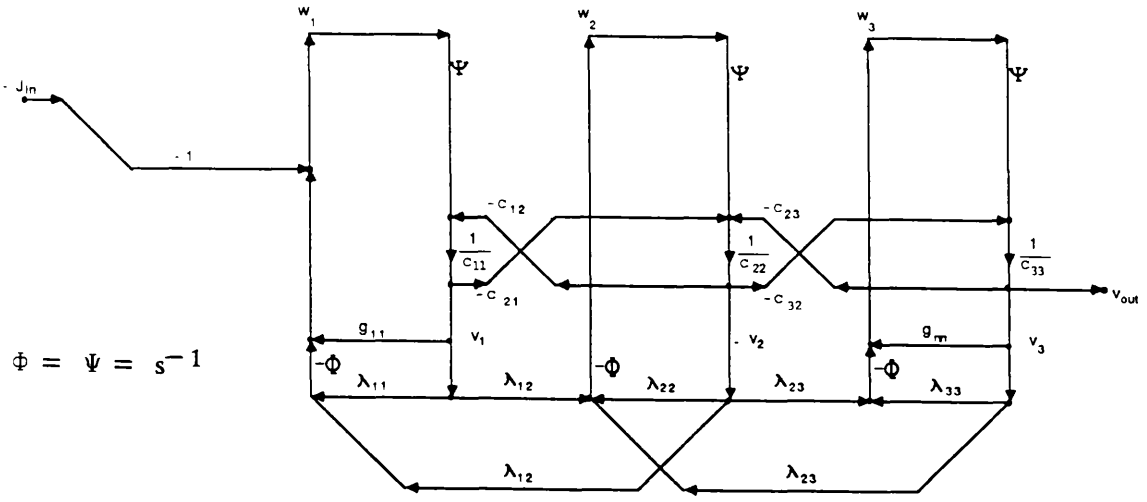
$G_1 = 1$ $C_2 = C_{11}$ $G_3 = 1$ $C_4 = L_2$ $G_5 = 1$ $G_6 = 1$ $C_7 = C_2$ $C_8 = C_2$
$G_9 = 1$ $C_{10} = C_{22}$ $G_{11} = 1$ $C_{12} = L_4$ $G_{13} = 1$ $G_{14} = 1$ $C_{15} = C_4$ $C_{16} = C_4$
$G_{17} = 1$ $C_{18} = C_{33}$ $G_{19} = 1$ $C_{20} = L_5$ $G_{21} = g_{in}$ $G_{22} = g_L$ $G_{23} = 1$

(b)

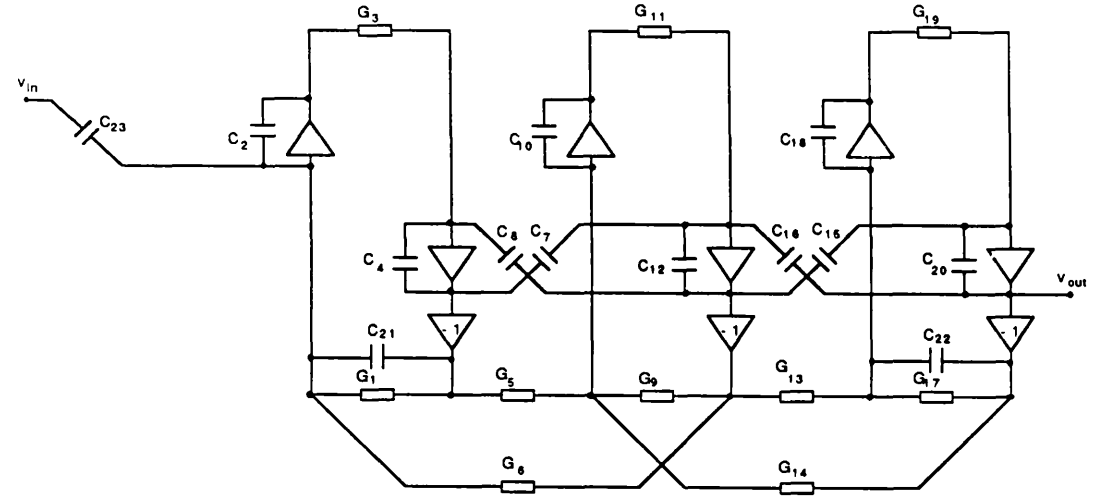
Fig. 1.9 Leapfrog type ladder simulation

(a) Signal– flow– graph

(b) Active– RC circuit realisation



(a)



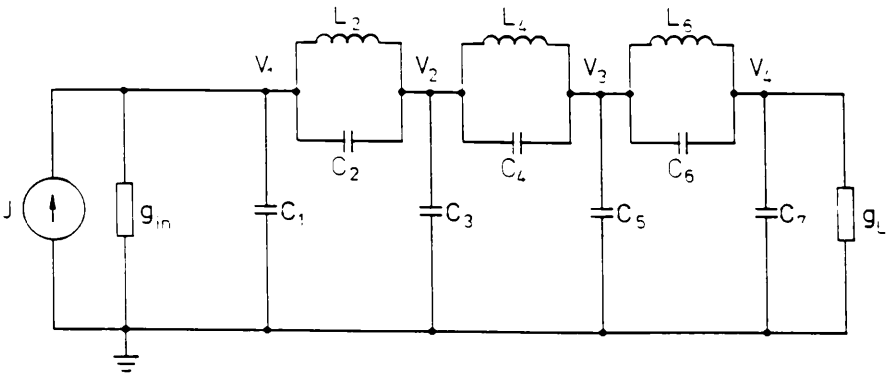
$G_1 = \lambda_{11}$ $C_2 = 1$ $G_3 = 1$ $C_4 = C_{11}$ $G_5 = \lambda_{12}$ $G_6 = \lambda_{12}$ $C_7 = C_{21}$ $C_8 = C_{12}$
$G_9 = \lambda_{22}$ $C_{10} = 1$ $G_{11} = 1$ $C_{12} = C_{22}$ $G_{13} = \lambda_{23}$ $G_{14} = \lambda_{23}$ $C_{15} = C_{32}$ $C_{16} = C_{23}$
$G_{17} = \lambda_{33}$ $C_{18} = 1$ $G_{19} = 1$ $C_{20} = C_{33}$ $G_{21} = g_{11}$ $G_{22} = g_{nn}$ $G_{23} = 1$

(b)

Fig. 1.10 Coupled– Biquads type ladder simulation

(a) Signal– flow– graph

(b) Active– RC circuit realisation

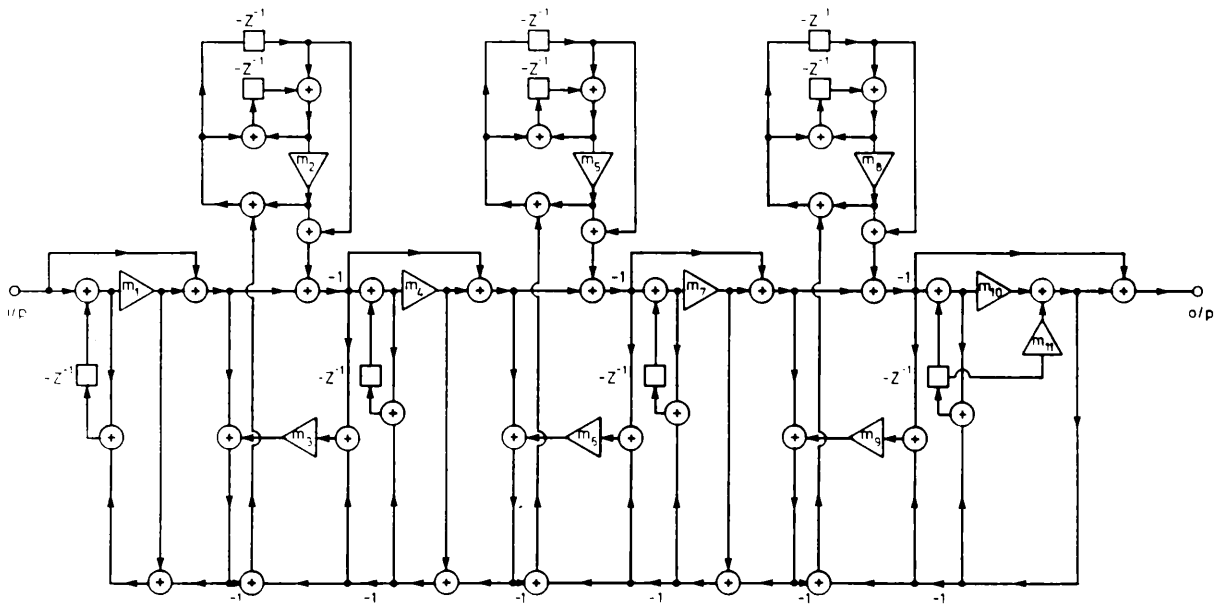


$C_1 = 3.450$ F $\quad C_2 = 0.1717$ F $\quad L_2 = 4.137$ H $\quad C_7 = 3.082$ F

$C_3 = 5.601$ F $\quad C_4 = 0.8016$ F $\quad L_4 = 3.828$ H $\quad g_{in} = 1$S

$C_5 = 5.328$ F $\quad C_5 = 0.5772$ F $\quad L_6 = 3.659$ H $\quad g_L = 1$S

(a)



$m_1 = -0.7748$ $\quad m_5 = -0.7532$ $\quad m_9 = 0.1203$

$m_2 = -0.4140$ $\quad m_6 = 0.1511$ $\quad m_{10} = -0.6899$

$m_3 = 0.08522$ $\quad m_7 = -0.8550$ $\quad m_{11} = -0.5851$

$m_4 = -0.9366$ $\quad m_8 = -0.6774$

(b)

Fig. 1.11 Wave digital filter

(a) A 7th order ladder prototype

(b) A wave digital circuit simulation

design. Wave digital filters have been proposed to solve the unrealisability problem in ladder simulations [77].

1.3.4) Wave digital filter

The effects of coefficient quantisation in digital filters are analogous to the sensitivity problem of analogue filters. The *wave digital filter* method was originally proposed by Fettweis as the low sensitivity alternative to direct approaches, later it attracted much attention due to its good noise properties [77].

A wave digital filter is also a ladder simulation. However, it simulates the relationships between so–called *wave variables*, instead of voltages and currents. A passive ladder is regarded as a combination of a number of 2–port circuit elements and 3–port series and parallel wire interconnection called adaptors [73,77]. An example of the simulation of the 7th order circuit in Fig.11a is shown in Fig.1.11b.

1.4 COMPUTER AIDED FILTER DESIGN

The large number of circuit options exaggerates the problem of design time and effort. Although design tables are available for some standard filters [2], they cannot cover all possible requirements. The performance of different structures under non–ideal conditions largely depends on the desired specifications, and is therefore a complex function of a large number of parameters such as Q factor, response class, order, filter structure and so on. Consequently, an exact prediction of the performance amongst different realisations is difficult, if not impossible. A full comparision of different approaches is preferable before deciding on a particular one. It seems that this can only be approached with the help of modern CAD (computer aided design) techniques. A great amount of effort has been expended [102–113] but, essentially, all the design software published so far remains at the development stage. The reason may lie in the mathematical and programming difficulties involved, as well as the fact that the fabrication technology has changed so rapidly since the 1970s.

1.5 GENERAL AIM AND OUTLINE OF THE THESIS

1.5.1) Motivation

Despite their obvious advantages regarding size, weight, cost and flexibility, active and digital circuits still suffer from some drawbacks, such as

1) Active components, such as transistors and opamps, have a finite gain– bandwidth (GB) product which imposes a limitation on their useful range of operation [33– 35].

2) Active filters are likely to be affected by inaccuracies during manufacture or component drift due to environmental changes. For the digital case, an equivalent effect is caused by truncation of multiplier coefficients in finite wordlength storage [3,12,73].

3) In active filters a significant noise level issues from the active devices. Digital filters introduce noise due to signal quantisations [3,12,73].

The influence of the above problems depends, to a large extent, on the network topology adopted. A carefully designed structure will greatly improve the performance of the resulting filters.

1.5.2) Purpose of the research

It has long been known that highly stable, low sensitivity and low noise properties may be obtained by employing multi– feedback circuits. However, as the degree of circuit coupling increases, the current design methods, rooted in their view of local circuit connections, become intractable.

Effort has been devoted to regularise the design process by viewing a filter in terms of system theory. Marshall first introduced UL matrix decomposition into wave digital ladder simulations based on state space variables [81]. Snelgrove, Roberts and Sedra have also investigated state– space models in active ladder design [114][118]. They indicated that a proper choice of intermediate state variables can improve system performance. However, it is difficult to use the standard state space model to provide a clear insight into the relationship between the structure and performance of the filter system.

The research presented in this thesis will deal with the above– mentioned difficulty. Departing from the state space concept, a system description adopting high order matrix polynomials is studied as a fundamental mathematical framework. Ladder based structures are the most natural representation of such

systems. Very simple, attainable criteria have thus been formalised for deriving stable filter structures with low sensitivity and low noise.

Some very regular procedures are established to linearise the system description into a set of matrix equations which are realisable by basic circuit building blocks. By arranging the filter system in a form amenable to some well studied methods of linear algebra, present clumsy equation–by–equation procedures for ladder simulation can be replaced by single matrix processing steps. A unification of the existing methods is revealed, together with a family of novel structures. Various techniques will also be proposed for individual applications where standard methods meet difficulties, such as for bandstop, highpass or allpass functions or result in inefficient realisations, such as for all–pole filters.

1.5.3) Organisation of the thesis

A review of the circuit analysis and design is included in the present chapter, together with some comments on the limitations of state–of–the–art filter design.

In Chapter 2 a theoretical investigation is presented for a family of matrix polynomial systems. Definitions and criteria are formulated for canonical ladder prototypes. It is shown that important properties like boundedness and pseudopassivity, which are essential to achieve low sensitivity and low noise systems, are closely related to the matrix symmetry. Sensitivity formulae are derived for both symmetric or asymmetric deviations of matrix entries.

The realisation of the matrix polynomial system by active–RC circuits is considered in Chapter 3. It is shown that the existing ladder simulation methods can be unified into a general family of circuits derived by adopting different matrix decompositions. Novel circuit structures are obtained by employing the LU decomposition drawn from numerical methods. Some of these structures, so–called left–LUD, UL–LU and LU–UL structures have a notable advantage of being free from capacitance–coupled–opamp loops. Due to the flexibility introduced by matrix methods, there is a wide choice of structures available to realise a given prototype. While a number of special techniques are discussed for individual design cases, a unified approach is also proposed to realise general transfer function by very regular circuit structures.

The matrix decomposition methods are extended to SC and digital filter

design in Chapter 4. The bilinear transformation is used to convert the prototype from the s−domain to the z−domain. For efficient simulation, a rearrangement is introduced to modify the system into a form realisable by LDI integrators [79]. These so− called bilinear− LDI structures were first discovered by Lee and Chang [51] for SC design by adopting negative elements in the prototype. In this thesis this principle is formalised in terms of matrix principles. The novel LUD approach to SC and digital filter design is discussed in detail. It is shown that negative elements can be placed in the prototypes to cancel the unecessary components in their simulations and to improve the parallelism for digital realisation, which is further enhanced by a new scaling technique. Some detailed comparisons of the new circuit structures with existing ones are given, demonstrating that some significant advantages such as low sensitivity and low capacitance spread, can be gained by employing the new design methods.

Chapter 5 concerns the design of non− lowpass filters by using frequency transformations. It is shown that circuits with different filtering types can be derived from a lowpass network by simply replacing the LDI integrators with some special operators. Towards the same objective, a novel second order building block is presented for strays− insensitive bandstop switched− capacitor (SC) ladder design. A two channel scheme obviates the need for term cancellation in realising bandstop type operators and is less demanding on opamp settling time. It is shown highpass SC filters can be obtained simply by adding a modulation stage to a corresponding lowpass filter.

Chapter 6 deals with all− pass filter design for active RLC, active RC, SC and digital realisations. The matrix decomposition approach is readily applied to the ladder simulation part, in this case, a singly− terminated ladder is shown to have advantages. The resulting circuits have the attractive properties of parallel sturctures and very low amplitude sensitivity to component changes. Analogue implementations are canonical in opamp number and digital ones are canonical in multiplier number. Detailed examples are given for SC designs and these are critically assessed for capacitance spread and sensitivities.

Matrix methods are highly suitable for computer software development. They offer a concise form of circuit description which eases data storage and can then be manipulated systematically by well developed algorithms for filter derivation. A computer software package for advanced filter design, PANDDA is developed by the author in co− operation with R. K. Henderson. Its many distinguished features are outlined in Chapter 7 where some practical design examples are also given.

Measured response of SC fabrications by LUD and mixed LUD– biquad methods are illustrated.

Finally the main results obtained in this thesis will be summarised in Chapter 8. Some suggestions for further research in integrated filter design will also be given.

1.6 STATMENT OF ORIGINALITY

The following most significant results of the research work presented in this thesis are, to the best of author's knowledge, original and, as indicated below, some of the results have been or will be published.

Chapter 2 —— The theoretical investigation of symmetric matrix systems, proof of boundedness and pseudopassivity, are the subjects of the papers,

Li Ping and J.I. Sewell," On low sensitivity/ noise digital filter design", Proc. IEEE 1989 International Conference on Accoustics, Speech and Signal Processing, pp.1063–1066, Glasgow, UK, May 1989.

Li Ping and J.I. Sewell, "High performance circuit structures and symmetric matrix systems", Proc. IEE, vol.136, Part–G, no.6, pp.327–336, Dec. 1989.

Chapter 3, 4 —— The LUD structure was first proposed for switched capacitor filter design in,

Li Ping and J.I. Sewell, "The LUD approach to switched capacitor network design", IEEE Trans Circuits Syst., vol.CAS–34, no.12, pp.1611–1614, December 1987.

which is followed by further studies revealing a whole family of circuit derived from matrix principles, as discussed in

Li Ping, R.K. Henderson and J.I. Sewell, "Matrix methods for switched–capacitor filter design", Proc. IEEE ISCAS, pp.1021–1024, Espoo Finland, June 1988.

R.K. Henderson, Li Ping and J.I. Sewell, "A unified approach to the design of canonical integrated ladder filters", to be published in Proc. IEEE ISCAS, New

Orleans USA, May 1990.

The matrix methods have been extended into active–RC and digital circuits in

Li Ping and J.I.Sewell, "Filter realisation by passive circuit simulations," Proc. IEE, vol.135, Part–G, no.4, pp.167–176, August 1988.

Chapter 5 —— The frequency transformation techniques for discrete domain filter design is covered in

Li Ping and J.I. Sewell, "Digital Filter Realisation by Passive Circuit Simulation", IEE Saraga Colloqium on Electronic Filters, Colloquium Digest, pp.8/1–8/8, May 1988.

A continuation of this research discovered the TWINTOR circuits for bandstop SC design, as described in

Li Ping, J.I. Sewell, "The TWINTOR in bandstop switched–capacitor ladder filter realisation", IEEE Trans. Circuits Syst., vol.CAS–36, no.7, pp.1041–1044, July 1987.

Chapter 6 —— All–pass ladder structures are the subject of a recently completed paper,

Li Ping and J.I. Sewell, "Switched capacitor and active–RC allpass ladder filters", to be published in Proc. IEEE ISCAS, New Orleans USA, May 1990.

Chapter 7 —— The author's contribution to PANDDA software package is mainly in the circuit realisation and analysis parts. The development of PANDDA has been progressively reported in the following papers,

R. K. Henderson, Li Ping and J.I.Sewell, "PANDDA : A program for advanced network design : digital and analogue", Digest of IEE Saraga Colloquium on Electronic Filters, pp.4/1–4/8, London 1988.

R. K. Henderson, Li Ping and J.I.Sewell, "A program for digital and analogue filter design: PANDDA", Proc. European Conference on Circuit Theory and Design, pp.289–293, *Brighton, U.K., September 1989.*

CHAPTER 2

SYMMETRIC MATRIX POLYNOMIAL SYSTEMS

2.1 INTRODUCTION

Background

There are a number of attractive features about filter structures derived from passive RLC network simulations: they show very low sensitivity in the passband which is an important factor for active–RC and switched–capacitor (SC) filter fabrications [19–21,51–64]; they can be made limit cycle free for digital filter implementation, as shown for wave structures [76–83]; and they usually have better dynamic range compared with cascade biquads or other direct–form structures, which can be observed from many practical designs. Limit cycle supression and better dynamic range can improve the noise behaviour of the circuits.

Theories have been proposed to analyse and generalise the properties of passive ladders and their simulations [3,12,15]. A unified investigation has been proposed in [86,87] for digital circuits. It was shown that general low sensitivity filters can be constructed by properly connecting LBR (lossless–bounded–real) sections, which include adaptors for wave digital circuits as specific examples. In general, this approach is mainly concerned with the topological point of view.

The work of this chapter investigates the theoretical aspects of high quality network design based on matrix principles. A difference between the topological [19–21,51–64,76–87] and matrix approaches is that the former analyses the behaviour of local building–blocks while the latter examines the overall system. The two approaches complement each other to provide insight into the filter design problem.

Conventions

Attention is given to the properties of the system descriptions of circuits of the following form,

$$Y\,V = J \qquad (2.1a)$$

$$Y = s\,C + s^{-1}\,\Gamma + G \qquad (2.1b)$$

where all the matrices symmetric. This will be called a *symmetric matrix polynomial system (SMPS)*. Output functions may be added in the form

$$y = D\,V + E\,J \qquad (2.1c)$$

but only system (2.1a,b) will be considered since sensitivity and noise problems arise mainly from the feedback loops in (2.1a.b).

The most natural interpretation of system (2.1) is in the formulation of the network equations (nodal, loop, or hybrid) of passive RLC ladders [95,96]. In this case C, Γ and G represent the contributions of capacitors, inductors (inversed values) and conductors respectively and it can easily be shown that they are all non−negative definite, provided that nodal or loop formulations are used for the network with only positive−valued elements. The reverse procedure, from an equation with symmetric non−negative matrices to a network, is not always possible unless negative element values are allowed. Negative elements offer some advantages, such as to provide more regular structures which can be fabricated with greater ease [67]. Questions arise about the stability, sensitivity and noise problems associated with the introduction of negative elements. These will be answered by the theorems developed in this chapter.

In particular, the nodal description of a passive ladder is a tridiagonal SMPS and henceforth we will simply call a tridiagonal SMPS a ladder, as ladders are more familiar to most circuit designers and also as most SMPSs used in this thesis are derived from passive ladder prototypes.

Relationship between *SMPSs* and other systems concepts

System (2.1) is also a generalised form of the standard state−space equation. Indeed, (2.1) reduces to a standard state−space system when $\Gamma = 0$.

$$(sC + G)\, V = J \qquad (2.2)$$

Alternatively (2.1) can always be rearranged into the form of (2.2) by introducing some intermediate variables. However, the advantage of using the system description of (2.1) is that optimal performance can be achieved by imposing some simple conditions (notably symmetry) on the matrices. Conversely, if the matrices in (2.2) are constrained to be symmetric then the system can only have real poles, which is too restrictive for most applications.

System (2.1) can be further used to produce prototypes for various simulations discussed in detail in succeeding chapters.

Aspects covered in this chapter

In the first part of this chapter, some elementary criteria for checking the stability of SMPSs will first be established.

Then the efficiency with which the SMPSs can be realised will be considered. A canonical system is defined to be one which realises a given order of transfer function with the smallest possible matrices. It is shown that the parity of the numerator of the transfer function will decide whether it has a canonical realisation. This knowledge is useful in succeeding chapters for obtaining integrated ladders with minimum implementation cost.

The more sophisticated concepts considered by many authors, boundedness and pseudopassivity, are crucial in predicting the sensitivity and limit cycle behaviour of filter systems. They are now proved to be closely related to the matrix symmetry and to be basic properties of SMPSs.

In active–RC or SC implementations of SMPSs, the component deviations may destroy the symmetry of the system description. From practical observations the sensitivities of active–RC and SC ladder simulations are nevertheless very good, this is attributed to their multi–feedback nature. Sensitivity formulae are presented for asymmetric deviations, clearly indicating that better performance can be assured by more complete symmetry.

2.2 STABILITY CRITERIA

Besides synthesis methods, an optimisation procedure could also be used to adjust the entries of the matrices of (2.1) to make the transfer function fit the prescribed specifications. In this case conditions are required for testing the stability of the resulting system.

2.2.1) Critical Stability

Remark 2.1: System (2.1) is critically stable if C, Γ and G are all symmetric non–negative.

Proof: Let $\{ s_k = \sigma_k + j\omega_k \}$ be the set of roots of detY(s) of (2.1),

$$\det\ (\ s_k^2\ C + s_k G + \Gamma\ ) = 0 \qquad (2.3)$$

So there is a non−zero vector **X** which satisfies [101] the equation

$$X^*\ (\ s_k^2\ C + s_k\ G + \Gamma\ )\ X = 0 \qquad (2.4)$$

(X^* denotes the transposed conjugate of **X**)

or

$$as_k^2 + bs_k + c = 0 \qquad (2.5)$$

with $\quad a = X^*CX \qquad b = X^*GX \qquad c = X^*\Gamma X \qquad (2.6)$

As **C**, **G**, and Γ are all definite non−negative, a, b, and c are all non−negative numbers [101]. But in this case (2.5) has no roots with

$$\mathrm{Re}(s_k) = \sigma_k > 0 \qquad (2.7)$$

That is, system (2.1) has no poles in the right half plane if **C**, Γ and **G** are all symmetric non−negative.

2.2.2) Absolute Stability

The absolute stability condition for system (2.1) is that $\sigma_k < 0$ for all k. Therefore some extra constraints should be added to ensure that no roots lie on the imaginary axis. This can be checked by evaluating $\det|Y(j\omega)|$. In most cases system (2.1) is designed to realise a transfer function H(s) which has no poles on the imaginary axis. If the system is properly designed without redundancy, so that the order of the system is equal to the order of H(s), or in other words if it is observable from the output, then it will have no poles on the imaginary axis, as in this case H(s) and the system have the same set of poles.

The non−negative property of the symmetric matrices C, Γ and G can be easily tested. For instance, decompose C into symmetric LU form [97−100],

$$C = L_c D_c L_c^T \qquad (2.8)$$

where D_c is a diagonal matrix. **C** is non−negative if and only if all the entries

of D_c are non− negative. The computational requirement for this test is nearly equal to performing Gaussian elimination.

2.3 CANONICAL SYSTEMS

The system order of (2.1) is defined as the number of the roots of $\det|Y(s)|$. This should be clearly distinguished from the order of the matrices making up the system, although these two parameters are closely related to each other, since higher order systems obviously entail higher order matrix descriptions. As will be seen, the order, or more simply, the size of the matrices decides the size of the realisations by physical networks. For the sake of efficiency, it is usually desirable to design a given order system by matrices with order as small as possible and those systems with minimum size will be said to be canonical. The constraints for a transfer function to have a canonical realisation is explored in this section.

2.3.1) System order

The system polynomial of (2.1) is defined by

$$\Delta(s) = |Y(s)| = | sC + s^{-1}\Gamma + G | \qquad (2.9)$$

Using the Laplace expansion [100,101] repeatedly it can be shown

<u>Remark 2.2:</u> The determinant of $\Delta(s)$ can be expanded as (let n be the size of the coefficient matrices)

$$\Delta(s) = |C|s^n + a_{n-1}s^{n-1} + \ldots + a_{-(n-1)}s^{-(n-1)} + |\Gamma|s^{-n} \qquad (2.10)$$

The system order is defined by the difference between the highest and lowest index of the power of s in $\Delta(s)$. Again by using the Laplace expansion repeatedly, it can be shown that the highest coefficient of s will be accompanied by the highest non− zero cofactor of C, which is determined by the rank of C. Therefore the upper bound of the power of s is the rank of C. Similarly, it can be proved that the upper bound of the power of s^{-1} is the rank of Γ. The upper bound of the number of roots of $\det|Y|$ is then given by $\text{rank}(C)+\text{rank}(\Gamma)$.

Remark 2.3: *An upper bound of the order of the system, m, is given by*

$$m \leqslant r_C + r_\Gamma \leqslant 2n \qquad (2.11)$$

where r_C *and* r_Γ *are the ranks of* C *and* Γ *respectively.*

2.3.2) Condition for canonical ladder systems

From (2.11) the upper bound for a SMPS is 2n. However, if a SMPS is specially designed to realise an odd order function, then the upper bound will become 2n−1. Thus we have,

Definition 2.1: *A SMPS with size n is said to be canonical if it realises an* $2n^{th}$ *or* $2n-1^{th}$ *order transfer function.*

Definition 2.2: *A doubly−terminated* tri−diagonal *SMPS, or simply a ladder, meets the following conditions*

1) C, Γ *and* G *are all tri−diagonal matrices. So* Y *is also tri−diagonal.*

2) J *has only one non−zero element, i.e.* $J = (J_1, 0,...0)$.

3) G *has only two non−zero elements* $g_{11} = g_{in}$ *and* $g_{nn} = g_L$, *so that in general*

$$y_{(i+1,i)} = sc_{(i+1,i)} \cdot s^{-1} \gamma_{(i+1,i)} \qquad (2.12)$$

4) The output is the nodal voltage v_n.

There are some constraints for a transfer function to be realisable by a canonical doubly− terminated SMPS.

Theorem 2.1

i) The numerator of the transfer function v_n / J_1 *of a canonical even order doubly−terminated ladder is an odd polynomial.*

ii) The numerator of the transfer function v_n / J_1 *of an odd order doubly−terminated ladder is an odd polynomial if* $|C|$ *is non−singular or an even polynomial if* $|\Gamma|$ *is* non− *singular.*

Proof:

From Definition 2.2 a doubly− terminated ladder has the following expanded form

$$
\begin{bmatrix}
y_{11} & y_{12} & & & & & & \vdots & \\
y_{21} & y_{22} & y_{23} & & & & & \vdots & \\
 & y_{32} & y_{33} & y_{34} & & & & \vdots & \\
 & & y_{43} & y_{44} & y_{45} & & & \vdots & \\
 & & & \ddots & \ddots & \ddots & & \vdots & \\
 & & & & \ddots & \ddots & & \vdots & \\
 & & & & & \ddots & \ddots & \vdots & y_{n-1n} \\
 & & & & & & y_{nn-1} & \vdots & y_{nn}
\end{bmatrix}
\begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \\ \vdots \\ v_{n-1} \\ v_n \end{bmatrix}
=
\begin{bmatrix} J_1 \\ 0 \\ 0 \\ 0 \\ \vdots \\ 0 \\ 0 \end{bmatrix}
\tag{2.13}
$$

From these properties and Cramer's rule it can be found for the output v_n [101]

$$
\frac{v_n}{J_1} = \frac{\pm \Delta_{1n}}{\Delta(s)} \tag{2.14}
$$

where $\Delta(s)$ is the determinant of Y and Δ_{1n} stands for the determinant of the submatrix of Y by deleting its first row and nth column, which can be seen as the lower– left $n-1-$th block of Y in (2.13). It can be shown that

$$
\frac{v_n}{J_1} = \frac{\prod_{i=1}^{n-1} [sc_{i+1,i} - s^{-1}\gamma_{i+1,i}]}{\Delta(s)} \tag{2.15a}
$$

where $\Gamma = \{\gamma_{i,j}\}$ and $C = \{c_{i,j}\}$. Let v_n/J_1 be expressed in the form of a rational function

$$
\frac{v_n}{J_1} = \frac{N(s)}{D(s)} \tag{2.15b}
$$

D(s) and N(s) are denominator and numerators respectively and they are pure

polynomials which means they contain only non− negative powers of s. Consider first the case of an even canonical realisation. From Remark 2.2, Γ must be nonsingular to be canonical and so

$$D(s) = s^n \Delta(s) \tag{2.16a}$$

$$N(s) = s^n \prod_{i=1}^{n-1} [sc_{i+1,i} - s^{-1}\gamma_{i+1,i}] \tag{2.16b}$$

Here $c_{i+1,i}$ and $\gamma_{i+1,i}$ (for all i) cannot both be zero otherwise the transfer function is zero. Suppose $c_{i+1,i}$ are nonzero for all i then it is seen that N(s) is a $2n-1^{th}$ polynomial with only odd terms. If any $c_{i+1,i}$ is zero then N(s) will reduce to a $2n-3^{th}$ polynomial (since in this case $\gamma_{i+1,1}$ must be non− zero) and N(s) will stay odd. It is easy to deduce that N(s) will remain odd for cases of more zero $\{c_{i+1,i}\}$. The same reasoning can be applied to the cases that some $\{\gamma_{i,i+1}\}$ are zero.

Now consider the case of odd order design, where either **C** or Γ must be singular to make $\Delta(s)$, (2.9), odd. If Γ is nonsingular exactly the same reasoning as for even case can used to show that N(s) must be odd. If **C** is nonsingular then

$$D(s) = s^{n-1} \Delta(s) \tag{2.17a}$$

$$N(s) = s^{n-1} \prod_{i=1}^{n-1} [sc_{i+1,i} - s^{-1}\gamma_{i+1,i}] \tag{2.17b}$$

and it is easily shown that N(s) must be even polynomial.

Theorem 2.1 establishes some necessary conditions for a transfer function to have a canonical realisation. In the authors' experience the conditions are also sufficient for realisability provided that the transfer function is stable.

It is seen from Theorem 2.1 that the constraint on the parity of the numerator is related to the singularity of the matrices C and Γ. The singularities, however, cannot be arbitrarily chosen according to the following theorem.

Theorem 2.2: *A doubly terminated ladder has a non-zero response at $\omega=\infty$ only if C is singular and has a non-zero response at $\omega=0$ only if Γ is singular.*

Proof: Let $s=j\omega$. From (2.10) it can be seen that when $\omega \to \infty$

$$\Delta(s) \to |C| s^n + a_{n-1} s^{n-1} \qquad (2.18)$$

and from (2.15) the numerator is at most to the power of s^{n-1}. Therefore if $|C|$ is not zero then (2.15) must be zero. Similar reasoning can be used at $\omega \to 0$.

It is mandatory that lowpass transfer functions have non-zero values at $\omega=0$ and for highpass and bandstop at $\omega=\infty$. This indicates that the singularity of the matrices is pre-determined by the filtering types and therefore the parity of the numerators of odd order cases is also constrained.

Since the singularities of C and Γ mean that their rank can at most be n-1, according to (2.11) a list of the upper bounds for various filtering types by a ladder with size n is obtained in Table 2.1

CLASSES	CONSTRAINT	UPPER BOUND OF SYSTEM ORDER
lowpass	$H(0)\neq 0$ Γ singular	2n-1
bandpass		2n
highpass	$H(\infty)\neq 0$ C singular	2n-1
bandstop	$H(0)\neq 0$ $H(\infty)\neq 0$ both C and Γ singular	2n-2

Table 2.1 Upper bounds for various filtering types by a doubly-terminated ladder with size n

It is easily seen that canonical designs can be achieved only by bandpass, odd order lowpass and odd order highpass. For other cases, constraints given in Theorem 2.2 make it impossible for a canonical realisation. In the succeeding chapters it will be seen that a non–canonical ladder prototype will lead to an unnecessarily large size integrated circuit simulation, unless some complicated procedure is adopted. It will also be shown that the wrong parity of numerator can be easily corrected and a simple technique is introduced to eliminate the error caused by this modification. This results in a unified procedure, with very regular structures, to realise a wide family of transfer functions.

2.4 BOUNDEDNESS

2.4.1) The concept

The concept of boundedness can be traced back to an observation by Orchard about the low sensitivity properties of doubly–terminated ladders [15].

Definition 2.3: Boundedness *The transfer function, $H(P)$, of a system is said to be bounded with respect to the change of a set of parameters, $P = \{ p_i \}$, if there is a positive number M and*

$$|H(P)| \leqslant M \tag{2.19}$$

is always satisfied when P varies within the allowed range.

When a bounded system is properly designed to make $|H(P)|$ attain M at a frequency point in the passband, $j\omega_m$, then the deviation of $\mathbf{P}$ can only cause $|H(P)|$ to decrease. This means that $|H(P)|$ must have zero derivative with respect to any parameter p_i at $j\omega_m$, and consequently the sensitivity is also zero, i.e.,

$$S^{|H|}_{p_i} = \frac{p_i}{|H(P)|} \frac{\partial |H(P)|}{\partial p_i} = 0 \quad \text{at } s=j\omega_m \tag{2.20}$$

and it may be reasonably expected that over the whole passband the sensitivity will remain small, a reassuring argument used by many other authors for ladders as well as various simulation methods [3,12,73].

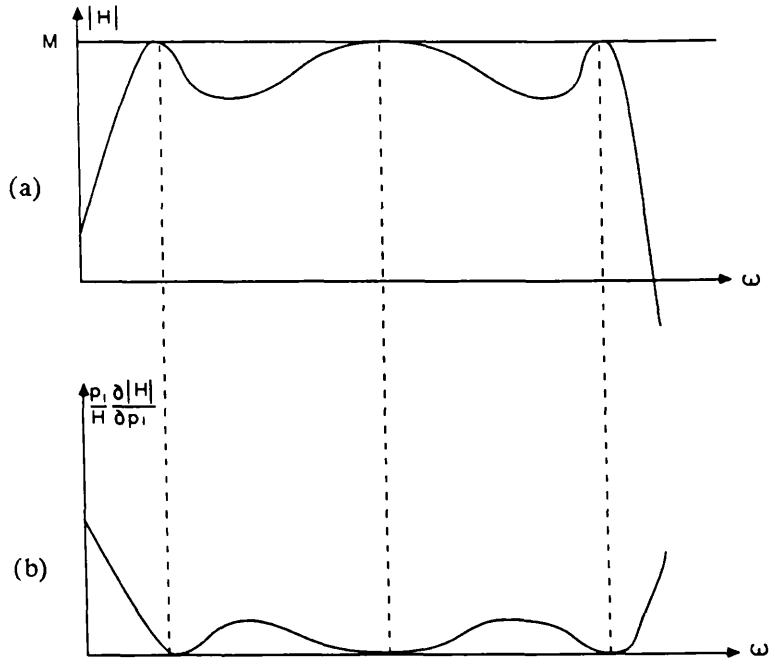


Fig.2.1 Illustration of boundedness and low– sensitivity
(a) Transfer function of a bounded system
(b) Sensitivity

2.4.2) Boundedness in the continuous domain

From network topology it is known that the output power of a doubly terminated ladder is bounded by maximum input power, a reasonable fact since a passive ladder cannot create power within itself. This result can also applied to the system (2.1) in a more abstract sense. Let (2.1) be evaluated on the imaginary axis, $s = j\omega$, and denote

$$Q = \omega C - \omega^{-1} \Gamma \qquad (2.21)$$

The system can be written as,

$$Y\,V = (\,jQ + G\,)\,V = J \qquad (2.22)$$

Suppose matrix G in (2.22) can be separated according to input and output parts respectively

$$G = G_{in} + G_{out}\,. \qquad (2.23)$$

Then (2.22) can be written as

$$j\,Q\,V + G_{out}V + G_{in}V = J \qquad (2.24)$$

We first prove a general relation.

Theorem 2.3: *Assume that in (2.1),*
(i) $G_{in}\,X = J$ *has at least one solution.*
(ii) all matrices are symmetric non−negative definite.
Then the following inequality holds,

$$V^{*}G_{out}V \leqslant \frac{1}{4}\,J^{*}R_{in}J \qquad (2.25)$$

where R_{in} *is the Moore−Penrose inverse of* G_{in}.

Proof: According to Moore− Penrose's theories [115,116], R_{in} is defined by

$$G_{in}R_{in}G_{in} = G_{in} \qquad R_{in}G_{in}R_{in} = R_{in}$$

$$(G_{in}R_{in})^{T} = G_{in}R_{in} \qquad (R_{in}G_{in})^{T} = R_{in}G_{in} \qquad (2.26)$$

and $X_S = R_{in}J$ is a solution of $G_{in}X = J$, if it has a solution at all, which means

$$G_{in}\,R_{in}\,J = J \qquad (2.27)$$

Now multiply (2.24) by V^{*},

$$j\,V^{*}\,Q\,V + V^{*}G_{out}V + V^{*}G_{in}V = V^{*}J \qquad (2.28)$$

Take the real part of (2.28)

$$V^*G_{out}V = Re\{V^*J\} - V^*G_{in}V \tag{2.29}$$

Notice from (2.26) and (2.27)

$$\begin{aligned} &[\ J^*R_{in}J - (J^* - 2V^*G_{in})R_{in}(J - 2G_{in}V)\ ]/4 \\ &= [\ 2\ J^*R_{in}G_{in}V - 2V^*G_{in}R_{in}J - 4V^*G_{in}R_{in}G_{in}V\ ]/4 \\ &= Re\{V^*J\} - V^*G_{in}V \end{aligned} \tag{2.30}$$

From (2.29) and (2.30)

$$V^*G_{out}V = [\ J^*R_{in}J - (J^* - 2V^*G_{in})R_{in}(J - 2G_{in}V)\ ]/4 \tag{2.31}$$

If G_{in} is non−negative then from (2,26) R_{in} is also non−negative which means that $(J^* - 2Y^*G_{in})R_{in}(J - 2G_{in}V)$ is a non−negative number. Theorem 2.3 follows from (2.31) immediately.

2.4.3) Boundedness for Terminated Reactance Network

Equation (2.25) is a general expression which can be applied to multi−input/output systems. To provide some insight of its physical interpretation, consider the special case of a single input/output system. Suppose (2.1) has only one input $J = [\ J_1,\ 0,\ldots\ 0\ ]$ and one output v_n. G_{in} and G_{out} have only one non−zero diagonal entry, respectively, corresponding to the input and output, i.e.,

$$G_{in} = diag(\ g_{11}, 0, 0, \ldots 0\ ) \tag{2.32a}$$

$$G_{out} = diag(\ 0, 0, \ldots 0, g_{nn}\ ) \tag{2.32b}$$

Then R_{in} can be generated by

$$R_{in} = diag(\ g_{11}^{-1}, 0, 0, \ldots 0,\ ) \tag{2.33}$$

Therefore in this case (2.31) reduces to

Therefore in this case (2.31) reduces to

$$g_{nn}|v_n|^2 = [\ 1 - |1 - 2g_{11}v_1/J_1|^2\ ]\ \frac{1}{4g_{11}}\ |J_1|^2 \qquad (2.34)$$

so

$$g_{nn}|v_n|^2 \leqslant \frac{1}{4\ g_{11}}\ |J_1|^2 \qquad (2.35)$$

or

$$|v_n| \leqslant \frac{1}{2(g_{11}g_{nn})^{1/2}}\ |J_1| \qquad (2.36)$$

A typical example of the system constrained by the conditions of (2.32) is a doubly– terminated ladder, in which case (2.1) are its nodal equations with input and output nodes labelled 1 and n respectively. The physical interpretation of (32) can be seen by rewriting it as

$$g_{nn}|v_n|^2 = [\ 1 - |\rho|^2\ ]\ g_{11}{}^{-1}|J_1|^2\ /4 \qquad (2.37)$$

with ρ defined by

$$\rho = 1 - 2g_{11}v_1/J_1 \qquad (2.38)$$

Consider a passive ladder with the source resistor being $r_{11} = g_{11}{}^{-1}$ and input impedance of the 2– port ladder including the load is $z_{in} = y_{in}{}^{-1}$.

$$\rho = 1 - 2g_{11}v_1/J_1 = 1 - \frac{2g_{11}}{y_{in}+g_{11}}$$

$$= \frac{y_{in}-g_{11}}{y_{in}+g_{11}} = \frac{r_{11}-z_{in}}{r_{11}+z_{in}} \qquad (2.39)$$

So ρ is just the reflection function and the upper bound of $|v_n|$ is attained at $\rho = 0$. This result is well known in network theory.

In the proof of boundeness, no conditions have been imposed on C and Γ except that they must be symmetric and non– negative. Accordingly, zero– sensitivity with respect to symmetric deviation can be achieved at the frequency points where the transfer function attains its upper bound.

2.5 SENSITIVITY FORMULAE

The above result provides only an estimate of sensitivity for symmetric deviations. More general sensitivity formulae are now derived. To simplify the problem, only single input/output system will be considered.

A useful equation

An equation is now derived as the preliminary to the main discussion. Suppose a single input/output system meets the conditions of Theorem 2.3 and (2.32). Let system (2.1a) be excited by another arbitrary input **J'** instead of J and let the response be **U**. The system can be written as

$$Y\,V' = J' \tag{2.40}$$

Left multiplying by **V*** gives

$$V^* Y V' = V^* J' \tag{2.41}$$

Note that when J is a real vector, ($\bar{}$ indicates conjugate)

$$\begin{aligned}(V^*Y)^T = Y\bar{V} &= (\,jQ + G\,)\bar{V} \\ &= -(-jQ + G)\bar{V} + 2G\bar{V} \\ &= 2G\bar{V} - J \\ &= (\,2g_{11}\bar{v}_1 - J_1,\ 0 \ldots 0,\ 2g_{nn}\bar{v}_n\,)^T \\ &= (\,\bar{\rho}J_1,\ 0 \ldots 0,\ 2g_{nn}\bar{v}_n)^T \end{aligned} \tag{2.42}$$

Substitute (2.42) into (2.41) and make some rearrangement to get

$$2g_{nn}\bar{v}_n\, v_n' - \bar{\rho}\, J_1\, v_1' + V^*J' = 0 \tag{2.43}$$

Again left multiplying (2.40) by V^T and noticing that $V^TY = J^T = [J_1,0,\ldots 0]$ we have

$$V^T J' = V^T Y V' = J^T V' = J_1\, v_1' \tag{2.44}$$

Finally substituting (2.44) into (2.43) leads to the following equation linking the output of the new system with the old system and the input,

$$v_n = (2g_{nn}\bar{v}_n)^{-1}(\rho\bar{V}^T - V^*)J' \qquad (2.45)$$

Sensitivity Formulae

Differentiate (2.11) w.r.t. some network element ξ to get

$$Y\ dV/d\xi + dY/d\xi\ V = 0 \qquad (2.46)$$

Here the second term can be viewed as the new input vector for (2.45) and we have

Theorem 2.4:

$$dv_n/d\xi = (2g_{nn}v_n)^{-1}(-\rho\bar{V}^t + \bar{V}^*)\ dY/d\xi\ V \qquad (2.47a)$$

and

$$d|v_n|/d\xi = Re[\ v_n\bar{dv}_n/d\xi\ ]/|v_n| = (2g_{nn}|v_n|)^{-1}Re[(-\rho\bar{V}^t + \bar{V}^*)dY/d\xi V] \qquad (2.47b)$$

In particular, if the deviation of ξ only perturbs the imaginary part of **Y**, j**X** say, and $dY/d\xi = jdX/d\xi$ is symmetric then

$$\begin{aligned} d|v_n|/d\xi &= (2g_{nn}|v_n|)^{-1}\ Re[-j\bar{\rho}\ V^T dX/d\xi V + j|V^* dX/d\xi\ V|] \\ &= (2g_{nn}|v_n|)^{-1}\ Re[\ -j\bar{\rho}\ V^T\ dX/d\xi\ V\ ] \\ &= -(2g_{nn}|v_n|)^{-1}\ Im[\ \rho\ V^T\ dX/d\xi\ V\ ] \end{aligned} \qquad (2.48)$$

So $d|v_n|/d\xi = 0$ when $\rho = 0$. This again confirms the conclusion for single input/output system, that $|v_n|$ attains its upper bound and has zero-sensitivity at $\rho = 0$, if the deviation is symmetric.

Application to Passive Networks

When system (2.1) is implemented by a real passive RLC network, $\xi \in \{ R_i, L_i, C_i \}$ and $dY/d\xi$ is always symmetric. Then a very simple alternative to the topological derivation of sensitivity follows. Let the contribution to **Y** of a branch admittance jq_k between nodes a,b be $jq_k M_{ab}$ where

$$M_{ab} = \begin{array}{c} \\ \\ a \\ b \\ \\ \end{array} \begin{array}{c} \begin{bmatrix} 0 & \vdots & \vdots & 0 \\ \cdots & 1 & -1 & \cdots \\ \cdots & -1 & 1 & \cdots \\ 0 & \vdots & \vdots & 0 \end{bmatrix} \\ a \quad b \end{array} \tag{2.49}$$

So

$$dY/dq_k = j\, M_{ab} \tag{2.50}$$

It is easily seen that

$$V^T M_{ab} V = v_k^2 \quad \text{and} \quad V^* M_{ab} V = |v_k|^2 \tag{2.51}$$

where v_k is the voltage across jq_k. Then (2.47) reduces to

$$dv_n/dq_k = (2g_{nn}|v_n|)^{-1}(-j\rho v_k^2 + |v_k|^2) \tag{2.52a}$$

and

$$d|v_n|/dq_k = (2g_{nn}|v_n|)^{-1}\ \mathrm{Im}\ [\ \rho v_k^2\ ] \tag{2.52b}$$

(2.52b) is zero at the frequency points where $\rho = 0$ or equivalently $|v_n|$ attains maximum bound. This is just the well known zero-sensitivity property for doubly-terminated ladders.

Application to Digital and Active Networks

In the following chapters it will be shown that system (2.1) can be simulated by digital or active networks. For digital simulations, even in non-ideal cases, it is still possible to keep deviations in Y symmetric by carefully selecting the coefficient quantisations, so the zero-sensitivity property can be preserved. For active-RC and SC simulations, it is difficult to keep deviations of Y symmetric, since the element value drift is a random phenomenon. The component drift may cause the equivalent system description (2.1) to become non-symmetric so

that the output may exceed the bound given by (2.25) or (2.36). However in practical active–RC or SC implementations, low sensitivity is still observed, a property due to the multi–feedback nature of the structures. (2.47) are valid for these general cases.

2.6 DISCRETE SYMMETRIC MATRIX POLYNOMIAL SYSTEMS

The results in last section can be readily extended to the discrete domain if a bilinear transformation is applied to system (2.1)

$$\Upsilon V = J \tag{2.53a}$$

with

$$\Upsilon = \Psi C + \Psi^{-1} \Gamma + G \tag{2.53b}$$

where

$$\Psi = \frac{2}{T} \frac{1 - z^{-1}}{1 + z^{-1}} \tag{2.53c}$$

(2.53) can be rearranged as

$$(P + z^{-1} Q + z^{-2} R) V = (1 - z^{-2}) J \tag{2.54a}$$

with

$$P = (\frac{2}{T} C + \frac{T}{2} \Gamma + G) \quad Q = -2 (\frac{2}{T} C - \frac{T}{2} \Gamma) \quad R = (\frac{2}{T} C + \frac{T}{2} \Gamma - G) \tag{2.54b}$$

which can be seen as a generalised form of the standard state–space equation, by introducing a second order term.

Because bilinear transformation will keep the stability property and map the imaginary axis in the s domain to the unit circle in the z domain, it is easily shown that,

Remark 2.4: *System (2.53) has no poles outside the unit circle $z=e^{j\omega T}$ if C, Γ and G are all symmetric non–negative definite and has the same boundeness and*

sensitivity properties as indicated by Theorems 2.3 and 2.4, except that (3.53) is evaluated on the unit circle $z=e^{j\omega T}$

2.7 PSEUDOPASSIVITY AND LIMIT CYCLE SUPRESSION

2.7.1) The concept

The generalised concept of pseudopassivity has been employed in discussion of wave digital filters [77], which is, in fact, based on the principle of the Lyapunov function. Consider a standard state−space system in the continuous domain:

$$sX = AX + BJ \tag{2.55}$$

or in the discrete domain:

$$X = z^{-1} AX + BJ \tag{2.56}$$

Definition 2.5: Pseudopassivity *A state space system (2.53) or (2.56) is said to be pseudopassive if*

$$e(t) = x^T(t)x(t) \tag{2.57}$$

is a monotonically decreasing function for any initial value $\mathbf{x}(0)=\mathbf{x}_0$ *with* $J = 0$. *(For a discrete system x(t) is examined at a discrete instance, i.e.,* $t=nT$*).*

e(t) can be seen as an energy function and it is always decreasing for a pseudopassive system without excitation. The pseudopassive property in a discrete system is important for the supression of parasitic oscillations. If the input $\mathbf{J=0}$, the state space variables $\mathbf{x}$(nT), and so all the variables, in a stable digital system (2.56) will approach zero regardless of the initial state in the ideal linear case. However when the necessary quantisations are adopted in a digital filter, $\mathbf{x}$(nT) may oscillate and take non−zero values due to non−linear effects which may even cover the entire numerical range in the filter when overflow occurs. These parasitic oscillations, or so called limit cycles, can be avoided if the discrete system is pseudopassive and magnitude rounding for quantisation of $\mathbf{x}$(nT) is adopted. In magnitude rounding, a number a, is truncated to a finite number of bits, Q[a] with $|Q[a]| \leqslant |a|$. Let Q[$\mathbf{x}$] denote the vector of $\mathbf{x}$ after magnitude

rounding and suppose in a pseudopassive system (2.56) these are the only quantisation operations, then according to (2.57)

$$Q^T[x(nT)]Q[x(nT)] \leqslant x^T(nT)x(nT)$$
$$\leqslant Q^T[x((n-1)T)]Q[x((n-1)T)] \leqslant x^T((n-1)T)x((n-1)T) \leqslant \ldots \tag{2.58}$$

Therefore if $\mathbf{x}(nT) \to 0$ in the ideal case, then in the non-ideal case it will still approach zero. This will completely supress limit cycles [77].

The second norm of a matrix $\mathbf{A}$ is given by [101]

$$||A|| = \max_{x \neq 0} \frac{x^T A^T A\, x}{x^T x} \tag{2.59}$$

The time domain equation of (2.56) gives (when J= 0)

$$x(n) = A\, x(n-1) \tag{2.60}$$

Hence from (2.58) and (2.59) a necessary and sufficient condition for pseudopassivity is

$$||A|| \leqslant 1 \tag{2.61}$$

in this case

$$x^T(n+k)x(n+k) \leqslant \ldots \leqslant x^T(n)x(n) = x^T(n-1)A^TAx(n-1) \leqslant x^T(n-1)x(n-1) \tag{2.62}$$

It has been proved on a topological basis that condition (2.61) is met by wave, normalised lattice and LBR structures [87], and the same concept has been used in the design of second order "minimum norm" building blocks [88]. In this section it will be shown that higher order networks, based on a symmetric matrix decomposition approach, can also be designed to meet this condition.

2.7.2) Psudopassivity for symmetric matrix polynomial systems

Consider the problem of constructing a peudopassive state-space system from (2.53), this can be written in an equivalent form

$$\left(\frac{2}{T} C + \frac{T}{2} \Gamma + G \right) V + \left(\frac{2}{T} \frac{-2z^{-1}}{1+z^{-1}} C + \frac{T}{2} \frac{2z^{-1}}{1-z^{-1}} \Gamma \right) V = J \qquad (2.63)$$

Let C and Γ be decomposed into symmetric forms.

$$\frac{2}{T} C = C_l \, C_l^T \qquad \frac{T}{2} \Gamma = \Gamma_l \, \Gamma_l^T \qquad (2.64)$$

Define

$$X = \begin{bmatrix} X_C \\ X_\Gamma \end{bmatrix} = \begin{bmatrix} \frac{2z^{-1}}{1+z^{-1}} C_l \\ \frac{-2z^{-1}}{1-z^{-1}} \Gamma_l \end{bmatrix} V \qquad (2.65)$$

From (2.64) and (2.65)

$$V = \left(\frac{2}{T} C + \frac{T}{2} \Gamma + G \right)^{-1} \left\{ \begin{bmatrix} C_l & \Gamma_l \end{bmatrix} \begin{bmatrix} X_C \\ X_\Gamma \end{bmatrix} + J \right\} \qquad (2.66)$$

Substitute (2.66) into (2.65) we get a state space description

$$X = z^{-1} A X + z^{-1} B U \qquad (2.67)$$

with

$$A = 2 \begin{bmatrix} C_l^T \\ -\Gamma_l^T \end{bmatrix} \left(\frac{2}{T} C + \frac{T}{2} \Gamma + G \right)^{-1} \begin{bmatrix} C_l & \Gamma_l \end{bmatrix} + \begin{bmatrix} -I & \\ & I \end{bmatrix} \qquad (2.68a)$$

$$B = 2 \begin{bmatrix} C_l^T \\ -\Gamma_l^T \end{bmatrix} \left(\frac{2}{T} C + \frac{T}{2} \Gamma + G \right)^{-1} \qquad (2.68b)$$

Theorem 2.5: *If C, Γ and G are non-negative definite and the state variable vector is chosen as that in (2.65) then the system is pseudopassive, i.e.,* $\|A\| \leqslant 1$.

Proof: First, only if C and Γ are both non-negative can the decompositions of (2.64) be carried out. Substantial manipulation of (2.65) and (2.68a) gives

$$A^T A = \begin{bmatrix} I & \\ & I \end{bmatrix} - 4 \begin{bmatrix} C_l^T \\ \Gamma_l^T \end{bmatrix} \left(\frac{2}{T} C + \frac{T}{2} \Gamma + G \right)^{-T} G \left(\frac{2}{T} C + \frac{T}{2} \Gamma + G \right)^{-1} \begin{bmatrix} C_l & \Gamma_l \end{bmatrix} \qquad (2.69)$$

From (2.66) and (2.69) it can be seen that the following relationships hold when $J = [0]$

$$x^T(n)\ A^T\ A\ x(n) = x^T(n)\ x(n) - v^T(n)\ G\ v(n) \cdot 4 \qquad (2.70a)$$

If G is non–negative then $v^T(n)\ G\ v(n)$ is a non–negative number and therefore

$$x^T(n)\ A^T\ A\ x(n) \leqslant x^T(n)\ x(n) \qquad (2.70b)$$

no matter what the value of $\mathbf{x}(n)$. The theorem follows from (2.59) and (2.61). Incidentally, from (2.70a) it can be seen that matrix A is orthogonal if $\mathbf{G} = [0]$.

2.7.3) Wave variables

Wave digital filters have long been known for their distinguished property of being free from limit cycles. It will be shown here that, apart from some scaling factors, the wave variables are a special case of the state–space variables defined in (2.65).

When (2.1) is derived from a passive ladder by nodal formulation, the matrices can be generated by topological means [96].

$$C = A_C D_C A_C^T \qquad (2.71a)$$

$$\Gamma = A_\Gamma D_\Gamma A_\Gamma^T \qquad (2.71b)$$

where D_C and D_Γ are diagonal branch–admittance matrices with entries consisting of the corresponding capacitance or inverse inductance values. A_C and A_Γ are the corresponding incidence matrices Let V_C, I_C, V_Γ and I_Γ be vectors of the voltages and currents of the capacitance and inductance branches respectively, then the voltage vectors are related to the nodal voltage vector V by

$$V_C = A_C^T\ V \qquad (2.72a)$$

$$V_\Gamma = A_\Gamma^T\ V \qquad (2.72b)$$

The current vectors are related to the nodal voltage vector by

$$I_C = -\frac{2}{T}\frac{1-z^{-1}}{1+z^{-1}} D_C A_C^T V \tag{2.73a}$$

$$I_\Gamma = -\frac{T}{2}\frac{1+z^{-1}}{1-z^{-1}} D_\Gamma A_\Gamma^T V \tag{2.73b}$$

According to the definition of wave variables [77]

Incident wave vectors

$$W_{CI} = V_C + (\frac{2}{T} D_C)^{-1} I_C = \frac{2}{1+z^{-1}} A_C^T V \tag{2.74a}$$

$$W_{\Gamma I} = V_\Gamma + (\frac{T}{2} D_\Gamma)^{-1} I_\Gamma = \frac{2}{1-z^{-1}} A_\Gamma^T V \tag{2.74b}$$

Reflected wave vectors

$$W_{CR} = V_C - (\frac{T}{2} D_C)^{-1} I_C = \frac{2z^{-1}}{1+z^{-1}} A_C^T V = z^{-1} W_{CI} \tag{2.75a}$$

$$W_{\Gamma R} = V_\Gamma - (\frac{2}{T} D_\Gamma)^{-1} I_\Gamma = \frac{-2z^{-1}}{1-z^{-1}} A_\Gamma^T V = -z^{-1} W_{\Gamma I} \tag{2.75b}$$

By comparing (2.71) and (2.65) it can be seen A_C^T and A_Γ^T differ from C_l^T and Γ_l^T only by factors $D_C^{1/2}$ and $D_\Gamma^{1/2}$ respectively. It can be found that

$$x^T(n)x(n) = w_{CR}^T(n) \frac{2}{T} D_C w_{CR}(n) + w_{\Gamma R}^T(n) \frac{T}{2} D_\Gamma w_{\Gamma R}(n) \tag{2.76}$$

When the branch admittance matrices D_C and D_Γ are diagonal with positive

element values, the magnitude rounding of w_{CR} and $w_{\Gamma R}$ will have the same effect as magnitude rounding on x(n) to cause a reduction of $\mathbf{x}^T(n)\mathbf{x}(n)$.

2.7.4) Continuous time domain pseudopassive systems

Conditions for the continuous time domain systems have no direct practical applications, however for completeness a derivation is given as the follows.

We first show that in the continuous time domain a state space system

$$\mathbf{X}' = \mathbf{AX} + \mathbf{BJ} \tag{2.77}$$

is pseudopassive iff $-(\mathbf{A}+\mathbf{A}^T)$ is non−negative. Set J=0 in (2.77). Then the time domain solution is given by

$$x(t) = \exp(At)\, x_0 \tag{2.78}$$

where x_0 is the initial value vector. Take the derivative of $e(t)=\mathbf{x}^T(t)\mathbf{x}(t)$

$$de/dt = x_0{}^T \exp(At)^T (A+A^T)t \exp(A^T t)\, x_0 \tag{2.79}$$

e(x(t)) is monotonically decreasing iff $de/dt \leqslant 0$ or equivalently, system (2.77) is pseudopassive iff $-(\mathbf{A}+\mathbf{A}^T)$ is non−negative. Now let a state space system be constructed from (2.1) by

$$\mathbf{X} = \begin{bmatrix} X_C \\ X_L \end{bmatrix} = \begin{bmatrix} L_C{}^T \\ L_\Gamma{}^T \end{bmatrix} \mathbf{V} \tag{2.80}$$

with

$$C = L_C\, L_C{}^T \qquad \Gamma = L_\Gamma\, L_\Gamma{}^T \tag{2.81a}$$

and

$$\mathbf{A} = \begin{bmatrix} -L_C^{-1} G L_C^{-T} & -L_C^{-1} L_\Gamma \\ L_\Gamma^T L_C^{-T} & 0 \end{bmatrix} \tag{2.81b}$$

It is easily seen that

$$-(A + A^T) = 2\begin{bmatrix} L_C^{-1}GL_C^{-T} & 0 \\ 0 & 0 \end{bmatrix} \qquad (2.82)$$

is non− negative. The pseudopassivity of (2.77) follows.

2.8 SUMMARY

We started this chapter by introducing the concept of SMPSs. They are extended forms of the well known state space systems and are also generalised mathematical abstractions of passive networks such as ladders.

The basic stability properties have been covered. Then a necessary condition for canonical realisation has been derived. A relationship is revealed between the filtering types, order of the system and orders and ranks of the matrices. Two theoretical properties of SMPSs, boundedness and psudopassivity, have been studied with the emphasis on filtering applications. It has been shown that SMPSs can be designed with optimal performance if some simple requirements are fulfilled. Sensitivity can be minimised if the deviation of component values is kept symmetric. Limit cycle oscillations can be efficiently eliminated by properly choosing the intermediate variables.

The above results form a mathematical foundation for matrix methods for advanced filter design developed in the succeeding chapters.

CHAPTER 3

MATRIX METHODS FOR ACTIVE–RC LADDER DESIGN

3.1 INTRODUCTION

3.2 MATRIX DESCRIPTION FOR ACTIVE– RC CIRCUITS

3.3 MATRIX METHODS FOR ACTIVE–RC CIRCUIT DESIGN

- 3.3.1) Alternating sign for nodal voltages
- 3.3.2) System linearisation by matrix decompositions
- 3.3.3) Various ways to perform the matrix decompositions
- 3.3.4) Examples of various circuit structures
- 3.3.5) A comparison of left– and right– LUD methods

3.4 UL– LU and LU– UL METHODS

- 3.4.1) System linearisation by UL– LU methods
- 3.4.2) Procedure to solve (3.10)
- 3.4.3) Formulae for LU– UL design

3.5 CANONICAL LADDER FILTER DESIGN

- 3.5.1) Restrictions of the standard methods
- 3.5.2) Modified canonical prototype
- 3.5.3) Canonical ladder simulation by active circuits

3.6 SPECIAL DESIGN TECHNIQUES

- 3.6.1) Hybrid matrix approaches
- 3.6.2) Inverse matrix approaches

3.7 CASCADE BIQUADS DESIGN.

3.8 SUMMARY

3.1 INTRODUCTION

In the last chapter, a theoretical study of symmetric matrix polynomial systems was undertaken. The realisation of these system by physical networks involves further design steps. In this chapter a detailed investigation of realisations by active– RC circuits is presented.

A SMPS or simply a ladder is nonlinear with respect to s^{-1} and it is difficult to realise directly by active– RC circuits based on Miller type integrators with transfer function s^{-1}. Therefore, some constraints and rules will first be stated to define a family of matrix equations which are directly realisable. These equations are linear in s^{-1} so that op– amp circuits can be used to perform additions, multiplications and integrations.

Techniques are then introduced to render matrix description of a ladder prototype realiseable, by decomposing it into several linear sub– equations. The matrix representation is a convenient and flexible vehicle for the design procedures. Numerical methods drawn from linear algebra can be applied to derive existing as well as novel active– RC structures. Leapfrog and coupled– biquad structures are shown to belong to the same family, simply resulting from different matrix transformations. Some new structures, notably those derived by LU matrix factorisation, demonstrate attractive properties.

The design of cascade biquads will be also be mentioned briefly. It is shown that, although cascade biquads are strictly asymmetric systems, they can be expressed in exactly the same concise form as ladder circuits. Thus a unified description of various circuit structures is possible and this assists the development of efficient computer algorithms considered in Chapter 7.

Biquadratic cascade filters have a very regular structure which grows by a uniform progression with increasing filter order, regardless of the type of transfer function, such as lowpass, bandpass, highpass and bandstop. On the other hand, design techniques for ladder based structures are strongly dependent on the type of the transfer functions. In this chapter, a unified method will be introduced to synthesise canonical prototypes and active ladders realising a wide family of transfer functions. It will be shown that ladder simulations can be designed with the same regular progression as for biquadratic cascades.

3.2 DIRECTLY REALISABLE MATRIX SYSTEMS

Matrix methods are known to be an efficient means of representing large interconnected networks. The inverse procedure is how to construct an active–RC circuit from a set of pre–determined matrix equations. If the equations are linear with respect to the transfer functions of the basic building blocks, then the problem becomes most simple. For example, consider the following single algebraic equation

$$v_n + c_{nn-1}\, v_{n-1} = s^{-1} w_n \qquad (3.1)$$

This equation can be directly represented by the SFG in Fig.3.1a. Let the variables $\{v_i\}$ and $\{w_i\}$ be the voltages of opamp outputs, then the SFG can be replaced by an active RC network shown in Fig.3.1b.

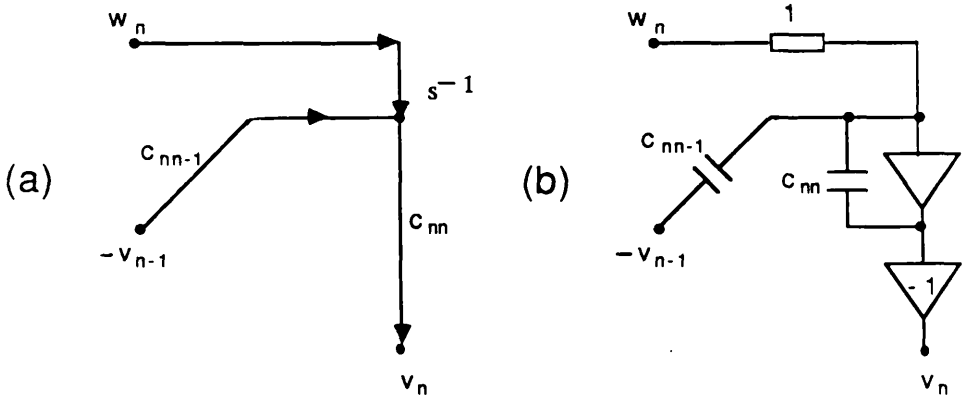


Fig.3.1. Representaion of a linear equation by (a) an SFG and (b) an active–RC circuit

This simple example can be generalised to the case of constructing a SFG and an active–RC circuit from a set of algebraic equations in matrix form. A matrix equation is considered to be *directly realisable* if it meets the following conditions,

Assumptions:

i) The matrix equation is linear with respect to the transfer function of the basic building blocks.

ii) In each matrix equation only one variable vector and associated coefficient matrix will be written on the left–hand side.

iii) The coefficient matrix on the left hand side is square and non–singular with all the diagonal elements of a_{ii} *non–zero.*

With the above assumptions a *directly realisable* matrix equation will have the following form,

$$A_{ii}\, X_i = \sum_k \varsigma_{ik}\, A_{ik}\, X_k + \varsigma_k\, J_k \qquad (3.2)$$

where $\{ X_k \}$ are vectors of variables

$\{ J_k \}$ are input vectors

$\{ A_k \}$ are matrices

$\{ \varsigma_{ik} \}$ and $\{ \varsigma_k \}$ are the transfer functions of the building blocks

The following rules are used to derive SFGs and circuits directly from matrix equations throughout this thesis:

1) Every entry in the variable vectors is represented by a nodal variable in the SFG and by an output of an opamp in the circuit. The input variables are represented by independent voltage sources.

2) The i–th row equation represents the linear relationship at the node corresponding to x_{im} *or, for the circuit, the input–output voltage relationship of the op–amp corresponding to* x_{im}

3) Each diagonal entry of $\mathbf{A}_{ii}$ *is realised by an integrating element. Every other non−zero entry in a matrix represents the connection of a circuit element between op−amps.*

Notice assumptions (i)−(iii) are only sufficient conditions for realisability. If a matrix system meets these assumptions then its realisation is straightforward and unique using the above rules. The major task of this research is to develop systematic procedures to synthesise the prototype and realise matrix systems which initially fail to meet these assumptions.

Example 3.1: To illustrate the principle, construct a SFG and a active−RC circuit from a set of matrix equations,

$$\mathbf{I}\ \mathbf{W} = -(s^{-1}\ \Gamma + \mathbf{G}\ )\ \mathbf{V} + \mathbf{J} \qquad (3.3a)$$

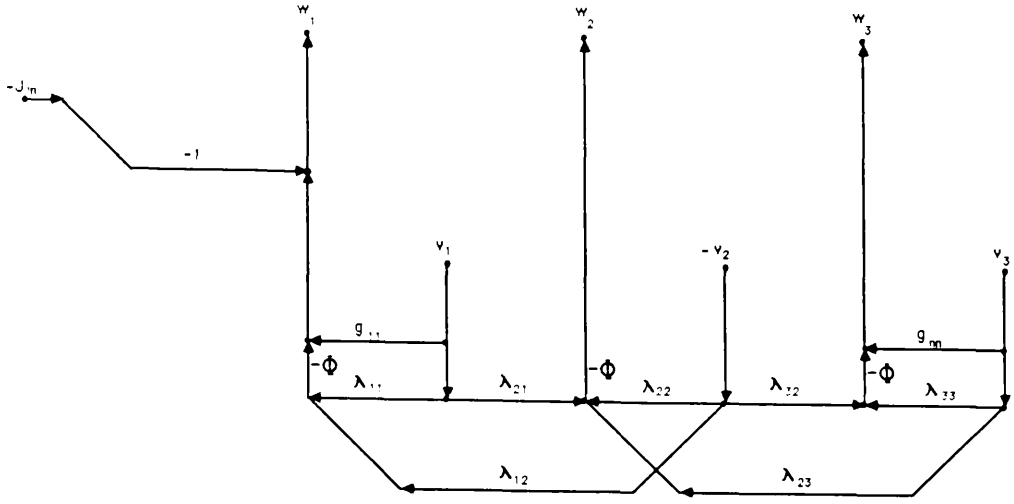
where **W** and **V** are two vectors of variables. **I** is the identity matrix and Γ and **G** have been given in (1.6). Then (3.3a) can be realised by the SFG and the circuit in Fig.3.2a (where $\Phi = s^{-1}$) respectively.

Example 3.2: A multi−equation system can be realised in the same way. For example combine (3.3a) and the following equation,

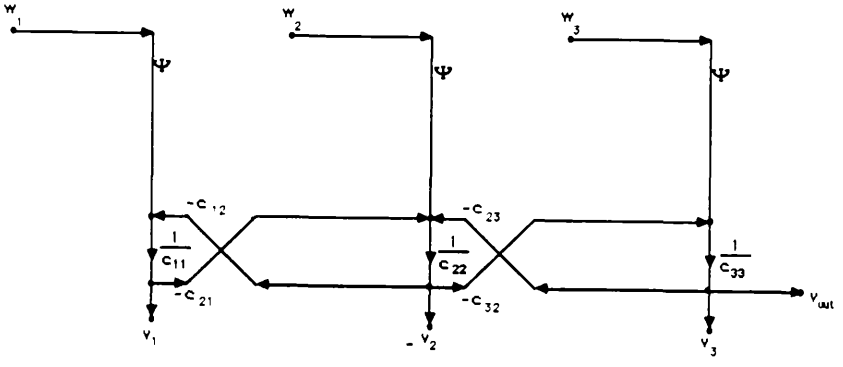
$$\mathbf{C}\ \mathbf{V} = s^{-1}\ \mathbf{W} \qquad (3.3b)$$

(3.3b) can be realised by the SFG shown in Fig.3.2b (where $\Psi = s^{-1}$). Notice the coupling relationship of (3.3a) and (3.3b). Fig.3.2a and b can be united to form a complete multi−feedback circuit using the same sets of nodal variables to realise variables of **V** and **W**, Fig.3.2c, which can be replaced by the active−RC circuit, Fig.3.2d. Interestingly, this circuit can be identical to the circuit in Fig.1.10.

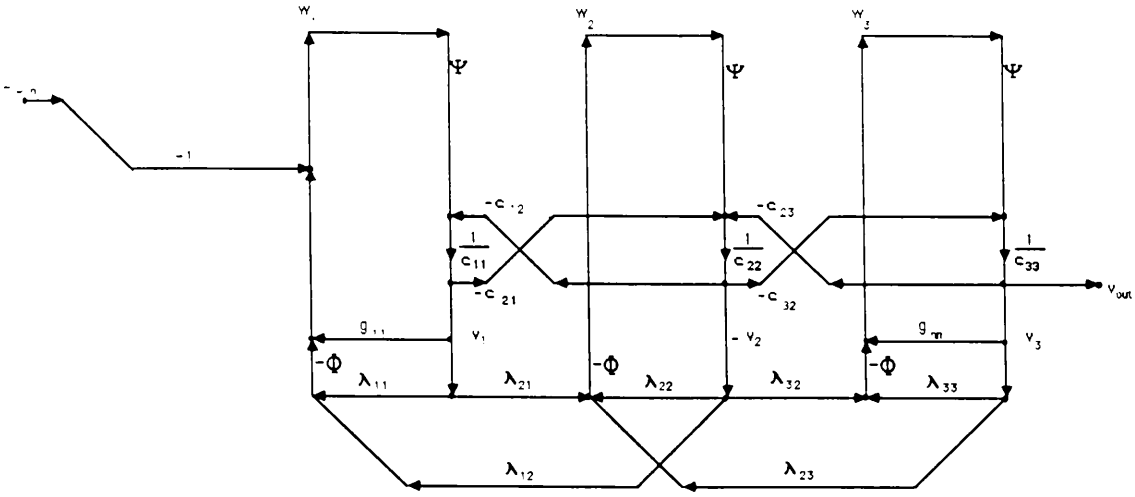
The capacitor coupled opamp loops may be seen from (3.3b) to be dependent on the presence of non−zero, off−diagonal entries in matrix **C**. When these entries occupy positions above and below the main diagonal, such as c_{12} and c_{21}, they cause cross−coupling of op−amp inputs and outputs by capacitors. If **C** is tridiagonal no such loops are formed, a property exploited by the LUD method shown later.


w1
w2
w3
-Jin
-1
v1
-v2
v3
g11
gnn
-Φ
-Φ
-Φ
λ11
λ21
λ22
λ32
λ33
λ12
λ23

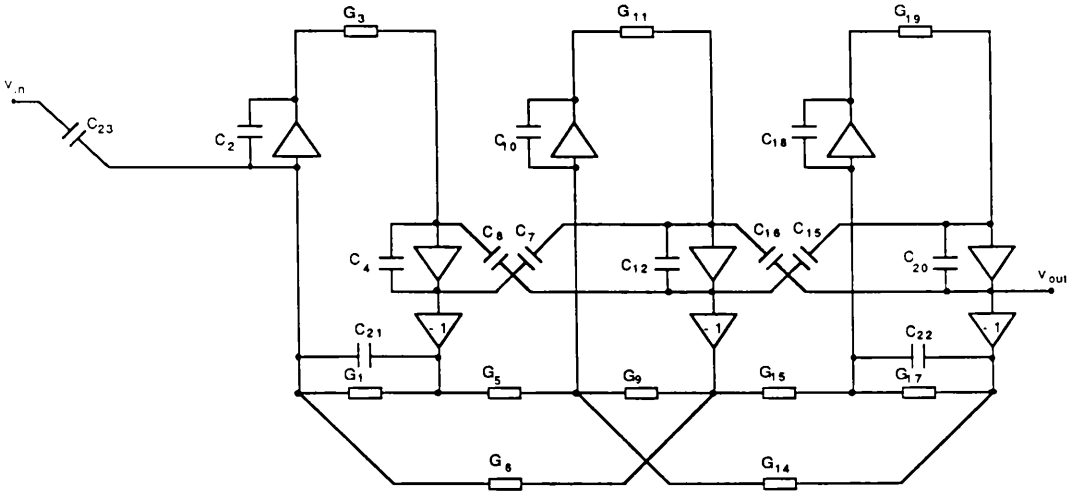
(a)


w1
w2
w3
Ψ
Ψ
Ψ
-c12
-c23
1/c11
1/c22
1/c33
-c21
-c32
vout
v1
-v2
v3

(b)



(c)



(d)

Fig.3.2 An example of realisation of a pair of matrix systems

(a) The SFG representation of eqn. (3.3a)

(b) The SFG representation of eqn. (3.3b)

(c) The overall SFG

(d) The active– RC realisation

3.3 MATRIX METHODS FOR ACTIVE–RC CIRCUIT DESIGN

3.3.1) Alternating sign for nodal voltages

Rewrite here (2.1) for a passive ladder

$$(s C + s^{-1} \Gamma + G) V = J \qquad (3.4)$$

From Example 1.1, it can be seen that the entries of C and Γ may be either positive or negative values. This may cause difficulty in realisation as negative entries require inverters. To avoid confusion, we introduce alternating signs in V, i.e., let $V=[v_1,-v_2,v_3,-v_4,...]$, which ensures that all the entries in (3.4) are positive. This can be seen in an example,

Example 3.3: For a 6th order ladder, Fig.1.2, nodal formulation leads to the following matrix equations,

$$\left\{ s \begin{bmatrix} C_1+C_2 & C_2 & \\ C_2 & C_2+C_3+C_4 & C_4 \\ & C_4 & C_4+C_5 \end{bmatrix} + s^{-1} \begin{bmatrix} L_2^{-1} & L_2^{-1} & \\ L_2^{-1} & L_2^{-1}+L_4^{-1} & L_4^{-1} \\ & L_4^{-1} & L_4^{-1}+L_5^{-1} \end{bmatrix} + \right.$$

$$\left. + \begin{bmatrix} G_{in} & & \\ & 0 & \\ & & G_L \end{bmatrix} \right\} \begin{bmatrix} v_1 \\ -v_2 \\ v_3 \end{bmatrix} = \begin{bmatrix} J_{in} \\ 0 \\ 0 \end{bmatrix} \qquad (3.5a)$$

$$C = \begin{bmatrix} 1 & 1 & & & \\ & 1 & 1 & 1 & \\ & & & 1 & 1 \end{bmatrix} \begin{bmatrix} C_1 & & & & \\ & C_2 & & & \\ & & C_3 & & \\ & & & C_4 & \\ & & & & C_5 \end{bmatrix} \begin{bmatrix} 1 & & \\ 1 & 1 & \\ & 1 & \\ & 1 & 1 \\ & & 1 \end{bmatrix} \qquad (3.5b)$$

$$\Gamma = \begin{bmatrix} 1 & & \\ 1 & 1 & \\ & 1 & 1 \end{bmatrix} \begin{bmatrix} L_2^{-1} & & \\ & L_4^{-1} & \\ & & L_5^{-1} \end{bmatrix} \begin{bmatrix} 1 & 1 & \\ & 1 & 1 \\ & & 1 \end{bmatrix} \qquad (3.5c)$$

Notice that all the entries of C, Γ and their relevant incidence matrices are positive. Hereafter unless otherwise stated, it will be assumed that all matrix entries are positive so that they can be directly realised by positive elements.

3.3.2) System linearisation by matrix decompositions

Equation (3.4) contains nonlinear combinations of the basic function s^{-1} so it does not meet Assumption i). It is more convenient to linearise the system into the form of (3.2). This can be done by creating a set of intermediate variables and decomposing the system of (3.4) into two inter-related systems. This decomposition can be performed in various ways.

Left Matrix Decomposition

Factorise the left hand matrix C into

$$C = C_l C_r \tag{3.6a}$$

The following pair of equations is equivalent to (3.4)

$$\begin{cases} C_l W = -(s^{-1} \Gamma + G) V - (-J) & (3.6b) \\ C_r V = s^{-1} W & (3.6c) \end{cases}$$

where W is the vector of intermediate variables.

Right Matrix Decomposition

Γ can also be factorised as

$$\Gamma = \Gamma_l \Gamma_r \tag{3.7a}$$

The following pair of equations is equivalent to (3.4)

$$\begin{cases} CV = -s^{-1} [\Gamma_l W + GV + (-J)] & (3.7b) \\ IW = s^{-1} \Gamma_r V & (3.7c) \end{cases}$$

Both (3.6) and (3.7) have a similar appearance to the system realised in Example 3.1 and 3.2. In fact it can be seen that (3.3) is a special case of (3.7b,c) when $C_l = C$, $C_r = I$.

From the rules given in Section 3.2, (3.6) and (3.7) can be realised by active– RC circuits, provided that the relevant matrices are obtained by certain decompositions. The one– to– one correspondence between the circuit elements and the matrix entries indicates that the efficiency of the active– RC implementation in terms of numbers of capacitors is related to the sparsity of the system matrices. Consequently a good simulation of a prototype by matrix methods will attempt to maintain the sparsity property of (3.4), in the design procedure.

3.3.3) Various ways to perform the matrix decompositions

The following methods are commonly known to preserve the sparsity of the matrices to be decomposed: the LU or UL methods (Section 1.2.3), the topological method (Section 1.2.2) and, simplest of all, the direct methods which decompose matrix **A** into **AI** or **IA**.

CATEGORY	NAME	MATRIX DECOMPOSOTIONS		
Left Decompositions	Left-LUD	$C=L_cL_c^T$	$C_l=L_c$	$C_r=L_c^T$
	Left-direct(IC)	$C=IC$	$C_l=I$	$C_r=C$
Right Decompositions	Right-LUD	$\Gamma=L_\Gamma L_\Gamma^T$	$\Gamma_l=L_\Gamma$	$\Gamma_r=L_\Gamma^T$
	Right-direct(ΓI)	$\Gamma=\Gamma I$	$\Gamma_l=\Gamma$	$\Gamma_r=I$
	Leapfrog	$\Gamma=A_\Gamma D_\Gamma A_\Gamma T$	$\Gamma_l=A_\Gamma$	$\Gamma_r=D_\Gamma A_\Gamma^T$

Table 3.1 Various ways to perform the matrix decompositions

Notice that a symmetric matrix $\mathbf{A}$ can be decomposed into symmetric LU form $\mathbf{A}=\mathbf{L}\mathbf{L}^T$. This property is used in the derivation of Table 3.1 as all the matrices in (3.4) are symmetric.

There are some duals to the systems listed in Table 2.1. which can be obtained by replacing LU decomposition by UL decompositions, or by replacing $\mathbf{C}=\mathbf{I}\mathbf{C}$ and $\Gamma=\Gamma\mathbf{I}$ by $\mathbf{C}=\mathbf{C}\mathbf{I}$ and $\Gamma=\mathbf{I}\Gamma$, respectively. The dual methods are useful in realising one family of canonical structures presented later.

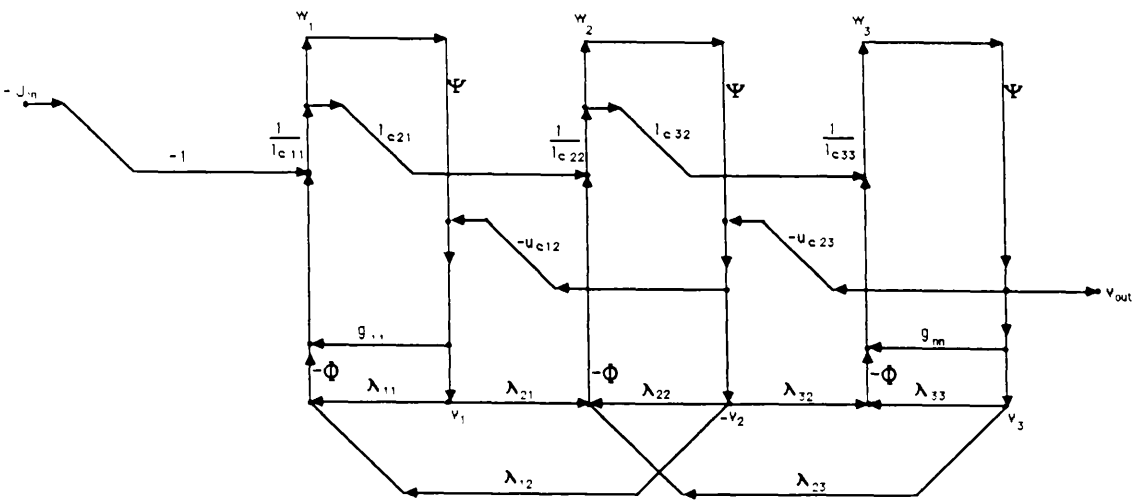
From network topology it is known that $\mathbf{D}_\Gamma\mathbf{A}_\Gamma^T\mathbf{V}=\mathbf{I}_L$ is the current vector of the inductance branches. This confirms that by topological decomposition of Γ, as shown at the bottom of Table 3.1, the same structures will be derived as those by a conventional leapfrog method (Example 1.2). In general, if topological decomposition is applied to the left-hand matrix $\mathbf{C}$, it cannot be assured that the resulting $\mathbf{C}_l$ and $\mathbf{C}_r$ will be square. Consequently, the resulting system (3.6) may violate the assumption (iii) in Section 3.2. If $\mathbf{C}_l$ and $\mathbf{C}_r$, obtained from a topological decomposition, are square then in most cases they are identical to those derived by LU decomposition. Therefore the topological decomposition will not be considered for left-hand matrices.

3.3.4) Examples of various circuit structures

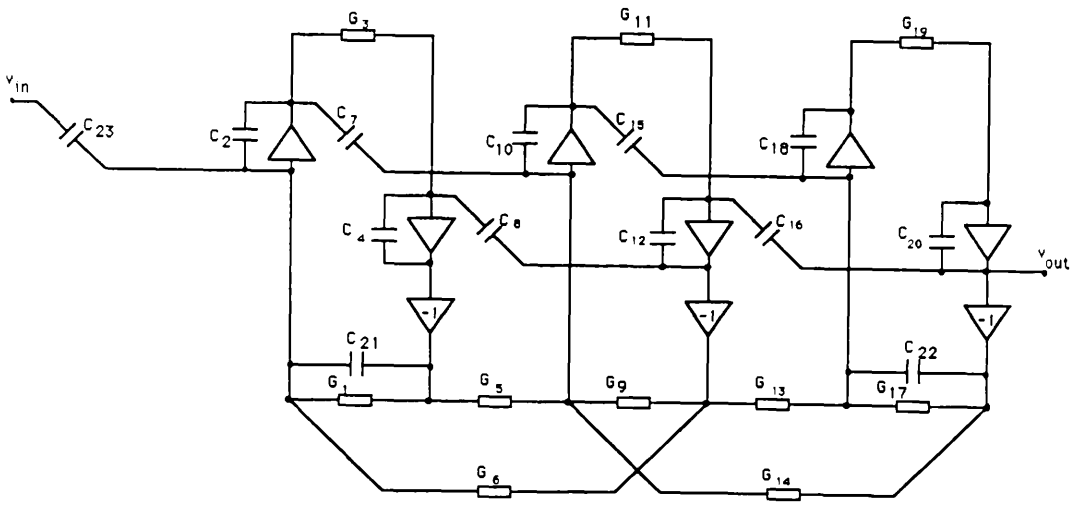
As examples, left-LUD, left-direct, right-LUD and right-direct SFGs and circuits are shown in Fig.3.3-3.6, using the matrix description (3.5) of the passive ladder in Fig.1.2 as the prototype. Notice for the s-domain design $\Phi=\Psi=s^{-1}$ but exactly the same SFGs can be used for the z-domain design discussed in Chapter 4 by redefining $\Phi=1/(1-z^{-1})$ and $\Psi=z^{-1}/(1-z^{-1})$.

Interestingly, it is found that the circuit in Fig.3.4 and 3.6 resulting from direct decompositions can be identified as a coupled type-E and type-F biquad circuit respectively. By comparing the intermediate variables introduced in the two approaches it can be shown that they differ only by voltage scaling factors.

For the prototype circuit of Fig.1.2, the leapfrog method results in exactly the same structure as that in Fig.3.5 by a right-LUD, which can clearly be seen by comparing it with Fig.1.9. In the low-pass case Γ_l and Γ_r obtained from leapfrog methods are also identical to those obtained from a right-LUD methods. An example is shown in Fig.3.7. However, in general the leapfrog method will lead to more simple simulations than the right-LUD method.



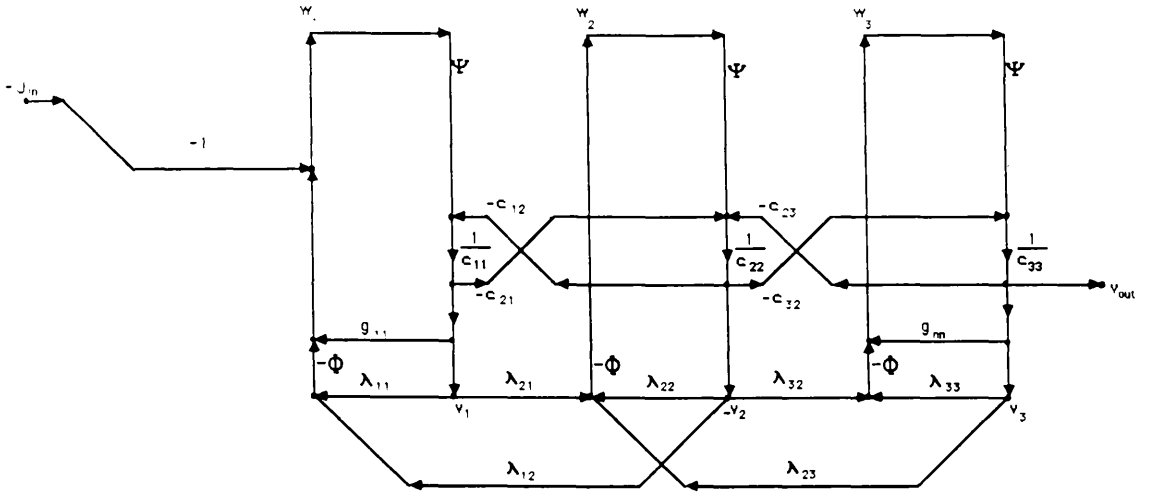
(a)



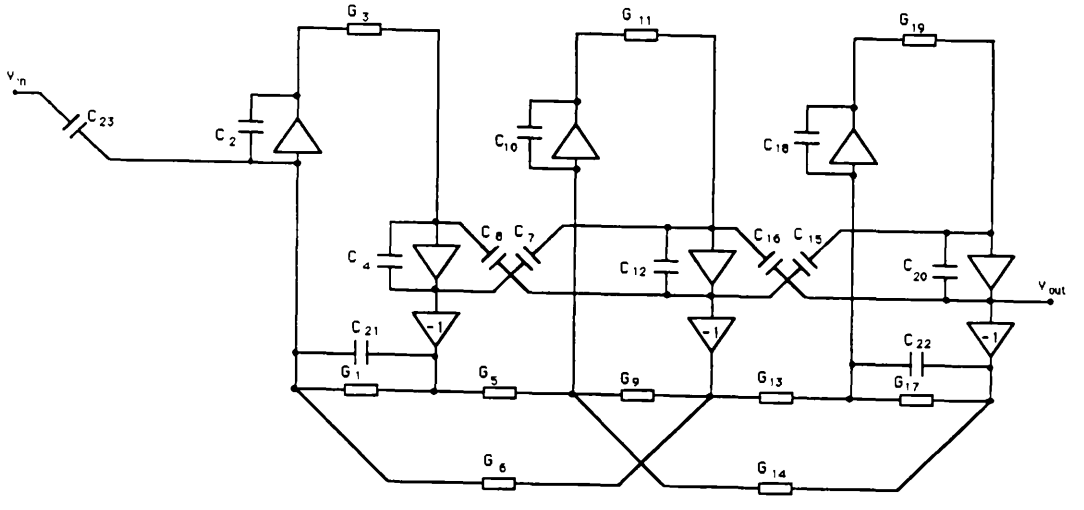
(b)

Fig.3.3 (a) Left– LUD type SFG

(b) Left– LUD type active– RC circuit



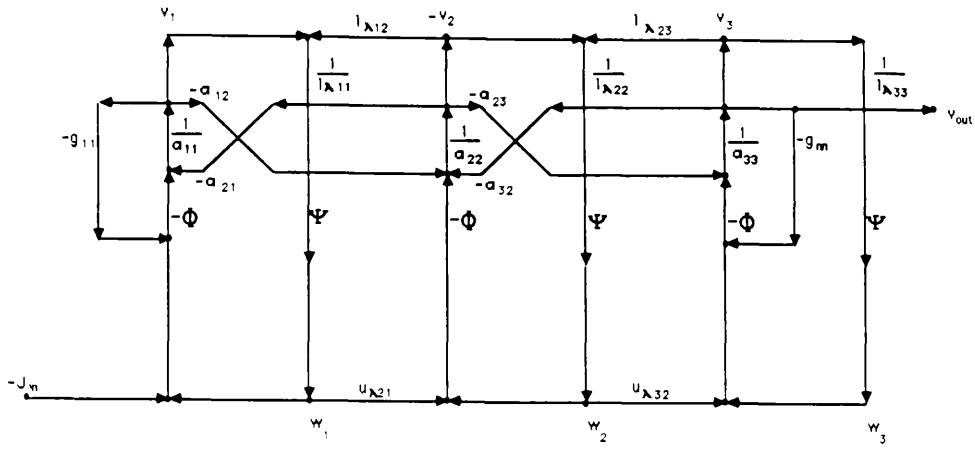
(a)



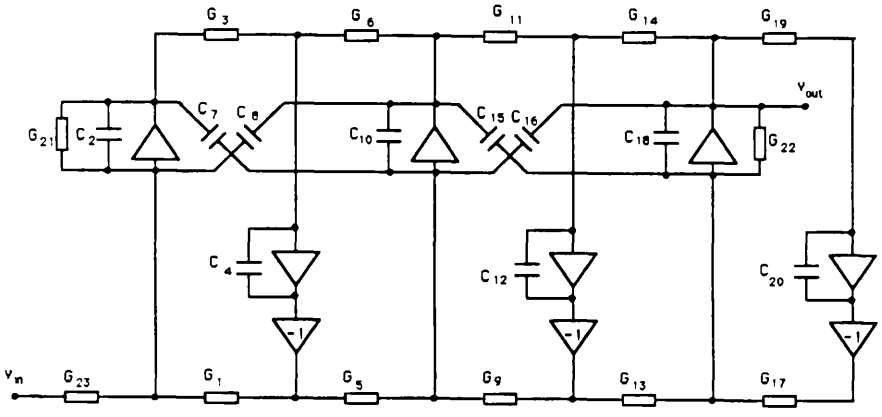
(b)

Fig.3.4 (a) Left– Direct(IC) type SFG

(b) Left– Direct(IC) type active– RC circuit



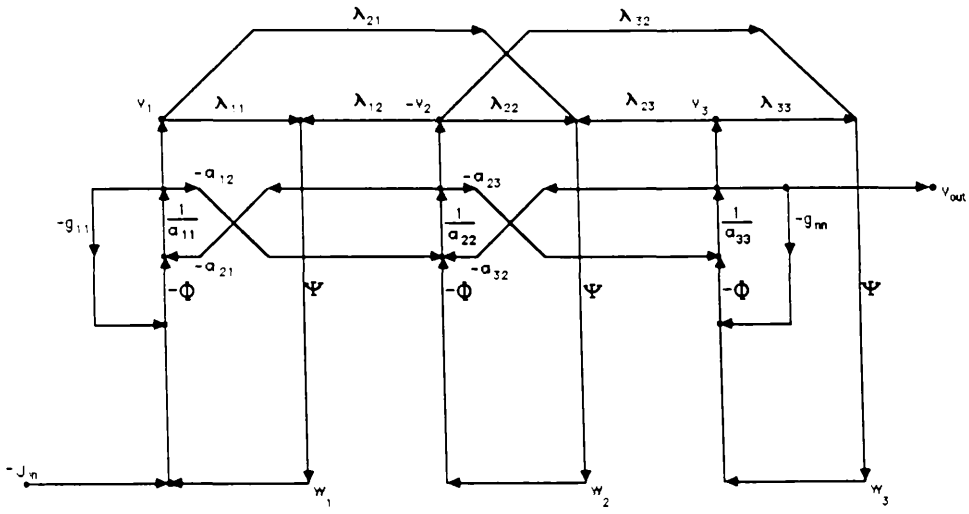
(a)



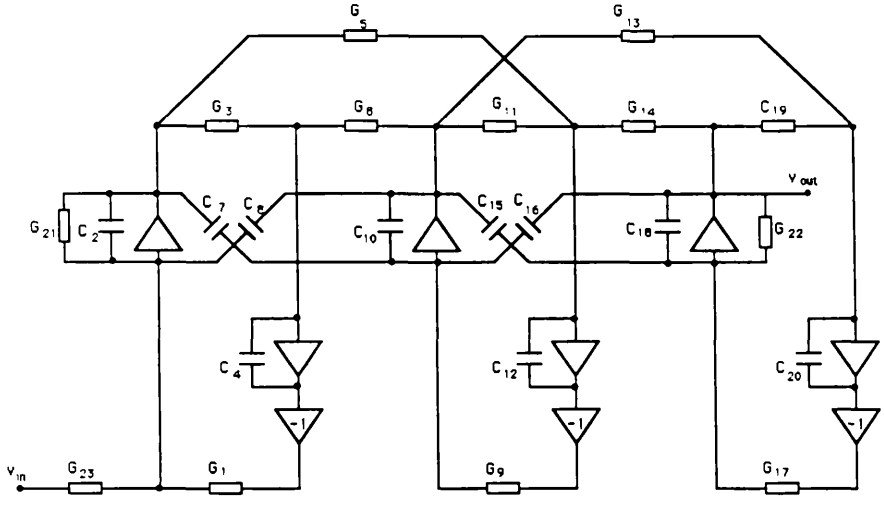
(b)

Fig.3.5 (a) Right– LUD type SFG

(b) Right– LUD type active– RC circuit



(a)

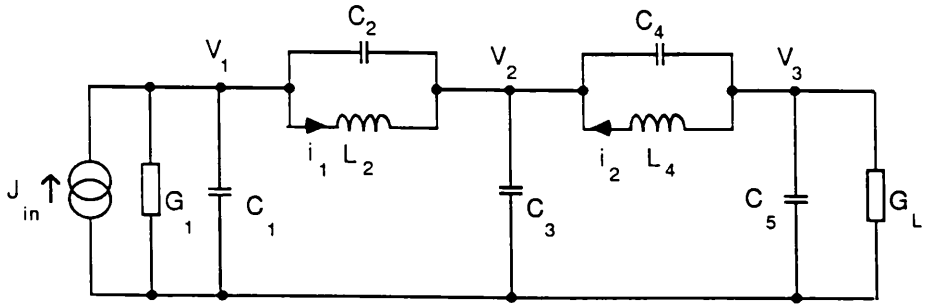


(b)

Fig.3.6 (a) Right– Direct(ΓΠ) type SFG

(b) Right– Direct(ΓΠ) type active– RC circuit

(a)



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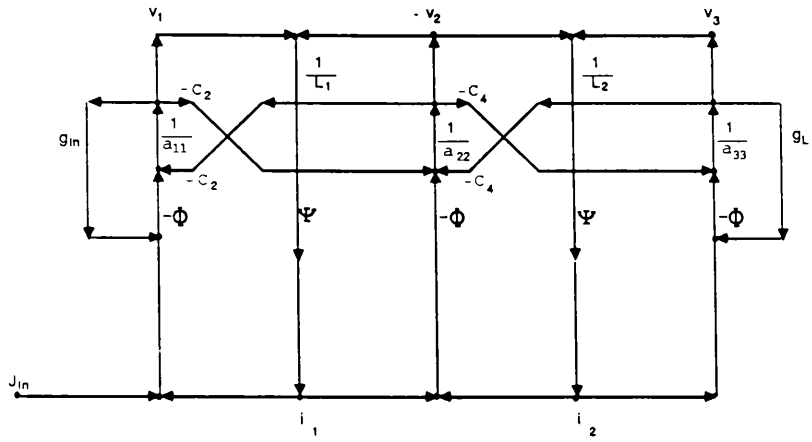

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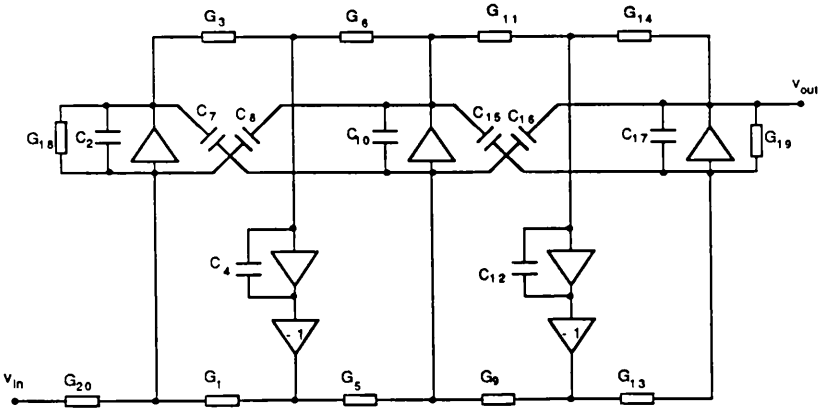


Fig.3.7. Lowpass circuit design by the right– LUD method

(a) A 5th order passive ladder

(b) Right– LUD type SFG

(c) Right– LUD type active– RC circuit

3.3.5) A comparison of left− and right− LUD methods

Two notable novel categories of ladder simulations presented in Table 3.1 are left− LUD and right− LUD (and their duals by UL decompositions). They both have some characteristic features.

In the left− LUD method the below− diagonal and above− diagonal elements of **C** are separated to matrices $\mathbf{L}_c$ and $\mathbf{L}_c^T$, respectively, effectively removing all capacitor− coupled− opamp loops, Fig.3.3. They also demonstrate excellent properties regarding component spread and dynamic range for bandpass design (see Section 4.7). However since $\mathbf{L}_c$ and $\mathbf{L}_c^T$ are restricted to be square, from (3.6) the dimension of the intermediate variable vector is n (n is the number of nodes, i.e., the dimension of **V**) and so altogether **W** and **V** contain 2n variables. Sometimes this is more than necessary. Taking the odd order lowpass design of Fig.3.7 as an example, Left− LUD simulation of the 5th order prototype results in exactly the same network topology as that of Fig.3.3, although we know that it can be used to simulate the 6th order prototype of Fig.1.2. On the other hand, right− LUD methods would use only 2n− 1 variables, a canonical number, for the particular prototype in Fig.3.7.

For right matrix decompositions, Γ_l and Γ_r can be made rectangular and the dimensions of **V** and **W** are not necessarily equal. Consequently the dimension of **W** can be smaller than that of **V**. In the case of a low− pass filter simulated by LUD methods, from Table 2.1 it is mandatory that Γ be singular so that a zero column in $\mathbf{L}_\Gamma$ will appear after LU decomposition. It can be then deleted, making $\mathbf{L}_\Gamma$ a $n\times(n-1)$ matrix. Thus a variable is saved in forming **W**.

Beside the inefficiency mentioned above, there is also a sensitivity problem in lowpass design for all the methods mentioned above except right− LUD. Deviation in the entries of Γ, caused by the inaccuracy of the element values associated with these entries, may cause Γ to become non− singular, introducing a zero at $\omega = 0$ (see Section 2.3). Extra zeros introduced at the origin, can be viewed either as an advantage or disadvantage, for instance low frequency noise suppression can be facilitated by these zeros. The right− LUD method does not have this problem as it involve multiplications of matrices with only (n− 1) rows or columns. The resulting matrices can never have a full rank n.

The right− LUD method, however, also has the drawback of posessing capacitor− coupled− opamp loops. Undesirable large component spread and poor

dynamic range are also observed for certain bandpass designs.

These arguments indicate that left− LUD is a good candidate for bandpass design and right− LUD is better for lowpass design, which will be further confirmed by the statistical data provided in Section 4.7.

3.4 UL–LU AND LU–UL METHODS

It is possible to develop structures by applying LU and UL decompositions to both left and right side matrices. Restricted by the requirements of preserving matrix sparsity and maintaining a canonical number of variables, derivations for such structures are not straightforward and are explored in this section.

3.4.1) System linearisation by UL− LU methods

UL and LU factorisations can be applied to both the left and right hand matrices of (3.4), respectively,

$$C = U_C \, L_C \tag{3.8a}$$

$$\Gamma = L_\Gamma \, U_\Gamma \tag{3.8b}$$

Define

$$W_C = s \, L_C \, V \tag{3.9a}$$

$$W_\Gamma = U_\Gamma \, V \tag{3.9b}$$

Suppose a upper triangular matrix U_{CS} and a lower triangular matrix $L_{\Gamma S}$ can be found so that

$$U_{CS} \, L_C = L_{\Gamma S} \, U_\Gamma \tag{3.10}$$

Denote

$$G_1 = \mathrm{diag}[\, g_{11}, \, 0, \ldots, 0 \,] \tag{3.11a}$$

$$G_n = \mathrm{diag}[\, 0, \ldots, 0, \, g_{nn} \,] \tag{3.11b}$$

so

$$G = G_1 + G_n \tag{3.11c}$$

Also denote

$$G_{1s} = G_1 \, L_c^{-1} \tag{3.12a}$$

$$G_{ns} = G_n \, U_\Gamma^{-1} \tag{3.12b}$$

Due to the lower triangular property of L_c^{-1}, it can be verified that G_{1s} has exactly one non-zero element at the upper left corner. It is also true that G_{ns} has only one non-zero element at the lower right corner due to the upper triangular property of U_Γ^{-1}. It is in order to preserve the sparsity of G_{1s} and G_{ns} that both UL and LU decomposition must be employed.

With (3.9-3.12), (3.4) can be decomposed into the following pair of equations,

$$\begin{cases} U_c \; W_c = -[(s^{-1}L_\Gamma + G_{ns})W_\Gamma + s^{-1}G_{1s}W_c] - (-J) & (3.13a) \\ L_{\Gamma s} \; W_\Gamma = s^{-1} \; U_{cs} \; W_c & (3.13b) \end{cases}$$

Realisations of a 6th order UL-LU active-RC circuit realisations is shown in Fig.3.8 using the passive ladders in Fig.1.2 as the prototypes. Notice now that the output is $w_{\Gamma n}$. From (3.9b), as U_Γ is upper trangular, $w_{\Gamma n}$ differs from original output v_n by only a constant.

3.4.2) Procedure to solve (3.10)

A important step which has not yet been explained is how to find matrices U_{cs} and $L_{\Gamma s}$ to meet identity (3.10).

When C and Γ are tridiagonal L_c and U_Γ are also tridiagonal as well as triangular. Separate the diagonal and off-diagonal parts of the matrices

$$L_c = L_{cdiag} + L_{coffd} \tag{3.14a}$$

$$U_\Gamma = U_{\Gamma diag} + U_{\Gamma offd} \tag{3.14b}$$

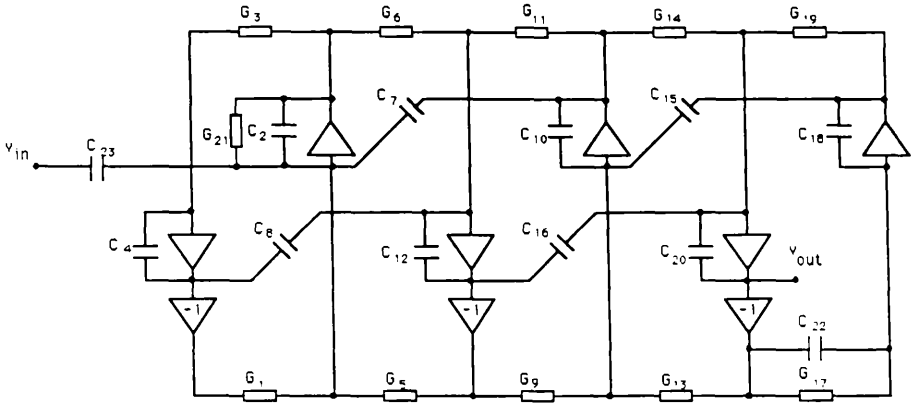


Fig.3.8. A UL–LU ladder circuit

where L_{cdiag} and $L_{\Gamma diag}$ are diagonal matrices, L_{coffd} has non– zero entries only on the first lower off diagonal and $U_{\Gamma offd}$ has non– zero entries only on the first upper off diagonal, i.e., L_{coffd} and $U_{\Gamma offd}$ have the following form

$$L_{coffd} = \begin{bmatrix} 0 & & & \\ * & 0 & & \\ & \ddots & \ddots & \\ & & * & 0 \end{bmatrix} \qquad U_{\Gamma offd} = \begin{bmatrix} 0 & * & & \\ & 0 & * & \\ & & \ddots & \ddots \\ & & & 0 \end{bmatrix} \qquad (3.15)$$

where * stands for the non– zero entries. Assume that U_{cs} and $L_{\Gamma s}$ are also tridiagonal and triangular matrices. Similar to the notation of (3.14) separate U_{cs} and $L_{\Gamma s}$ as

$$U_{cs} = U_{csdiag} + U_{csoffd} \tag{3.16a}$$

$$L_{\Gamma s} = L_{\Gamma sdiag} + L_{\Gamma soffd} \tag{3.16b}$$

Equate the different parts of (3.10) according to the position of the non−zero entries,

$$U_{csdiag}L_{coffd} = L_{\Gamma soffd}U_{\Gamma diag} \tag{3.17a}$$

$$U_{csoffd}L_{cdiag} = L_{\Gamma sdiag}U_{\Gamma offd} \tag{3.17b}$$

$$U_{csdiag}L_{cdiag} + U_{csoffd}L_{coffd}$$

$$= L_{\Gamma sdiag}U_{\Gamma diag} + L_{\Gamma soffd}U_{\Gamma offd} \tag{3.17c}$$

Since in (3.17a−c) the number of constraints is less than the number of variables, we can assign

$$L_{\Gamma sdiag} = I \tag{3.18}$$

which guarantees the realisability of system (3.13). From (3.17) and (3.18) we have

$$\begin{aligned} U_{csdiag} = &(L_{cdiag} - L_{coffd}U_{\Gamma diag}{}^{-1}U_{\Gamma offd})^{-1} \\ &\times (U_{\Gamma diag} - U_{\Gamma offd}L_{cdiag}{}^{-1}L_{coffd})) \end{aligned} \tag{3.19}$$

and remaining variables can be solved from (3.17)

$$L_{\Gamma soffd} = U_{csdiag}L_{coffd}U_{\Gamma diag}{}^{-1} \tag{3.20a}$$

$$U_{csoffd} = U_{\Gamma offd}L_{cdiag}{}^{-1} \tag{3.20b}$$

The matrices in (3.19) and (3.20) may be singular and the normal inverses do not exist. In these circumstances Moore− Penrose's generalised inverse can be used [115,116]. As the matrices in (3.19) and (3.20) are all diagonal, the procedure to obtain their Moore− Penrose inverse is very simple. The Moore− Penrose inverse of a diagonal matrix $D= diag[d_{11},\ldots,d_{nn}]$ is also a diagonal matrix given by

$M = \text{diag}[m_{11},\ldots,m_{nn}]$ with

$$m_{ii} = \begin{cases} 1/d_{ii} & \text{if } d_{ii}\neq 0 \quad (3.21a) \\ 0 & \text{if } d_{ii}=0 \quad (3.21b) \end{cases}$$

For an odd order deisgn with Γ singular , Fig.3.7a, matrix U_{cs} derived from the above procedure has a zero row. The corresponding variable of W_Γ can be deleted, resulting in a canonical realisation.

3.4.3) Formulae for LU– UL design

The dual of the above described UL– LU method is an LU– UL one. Its design formulae are given as the follows without derivation. Define

$$C = L_c\ U_c \quad (3.22a)$$

$$\Gamma = U_\Gamma\ L_\Gamma \quad (3.22b)$$

$$W_c = U_c\ V \quad (3.22c)$$

$$W_\Gamma = s^{-1}\ L_\Gamma\ V \quad (3.22d)$$

$$G_1 = \text{diag}[\ g_{11},\ 0,\ldots,0\ ] \quad (3.22e)$$

$$G_n = \text{diag}[\ 0,\ldots,0,\ g_{nn}\ ] \quad (3.22f)$$

$$G_{1s} = G_1\ L_\Gamma^{-1} \quad (3.22g)$$

$$G_{ns} = G_n\ U_c^{-1} \quad (3.22h)$$

The lower triangular matrix L_{cs} and upper triangular matrix $U_{\Gamma S}$ are defined to satisfy the identity

$$L_{cs}\ U_c = U_{\Gamma s}\ L_\Gamma \quad (3.22i)$$

We have finally

$$\begin{cases} L_C \; W_c = -[(s^{-1}U_\Gamma + G_{1s})W_\Gamma + s^{-1}G_{ns}W_c] - s^{-1}(-J) & (3.23a) \\ U_{\Gamma s} \; W_\Gamma = s^{-1} \; L_{Cs} \; W_c & (3.23b) \end{cases}$$

The output is w_{cn}. A LU− UL simulation of the prototype ladder, Fig.2.1, is shown in Fig.3.8.

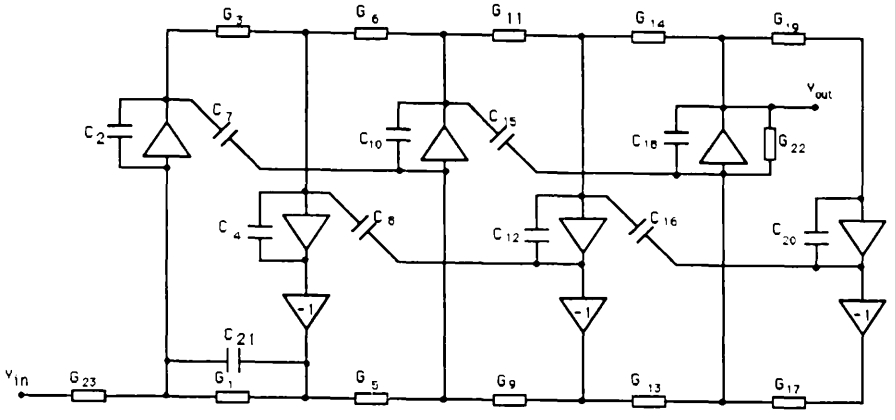


Fig.3.9. A LU− UL ladder circuit

Although UL− LU and LU− UL circuits were originally expected to comprise the advantages of both left− LUD and right− LUD ones, it turns out that they do not have notable features, as can be seen from the statistical study in Section 4.7. It is observed that F− type terminations (conductor G_{21} in Fig.3.7 and G_{22} in Fig.3.8) are not suitable for bandpass design as they produce large component spreads. If some technique can be found to incorporate two E− type (or two F− type) terminations the circuit performance may be improved, which should not be done at the cost of extra components.

3.5 CANONICAL LADDER FILTER DESIGN

3.5.1) Restrictions of the standard methods

The advantages of adopting low sensitivity ladder simulation in integrated circuit realisation have always been compromised by their complicated design procedures and associated implementation cost. Various design techniques must be used in ladder design to meet different specifications.

The difficulty is due to two problems; first the prototype ladder itself cannot be synthesised from certain types of transfer functions and second the standard simulation methods cannot be applied efficiently to certain types of the prototypes.

A common example of the first problem occurs in the realisation of even order elliptic functions. Passive ladder networks must have open or short circuit characteristics (implying full or zero transmission) at zero or infinite frequency respectively [3]. Therefore, lowpass or bandpass functions with finite (non−zero) stopband transmission at these extreme frequencies cannot be synthesised as passive ladders. 'Pure' even order elliptic functions and their frequency−transformed versions belong to this category. To obtain a realiseable function, a finite transmission zero must be shifted to infinite frequency [3]. This has the dual penalty of degraded filter performance and non−uniform passive ladder structure between odd and even order design, reflected also in the simulation by integrated circuits. For this reason, such transfer functions are practically undesirable for ladder simulation, since they are so close in cost to their related higher odd order function.

As an example a 8th order bandpass pure elliptic function and its modified form are shown in Fig.3.10. It can be seen that the cost of modifying the function is a loss of about 4dB attenuation in the stopband.

An example of the second problem may be seen from the discussion of Section 3.3. The design methods there generally use 2n or 2n−1 opamps (excluding inverters). The canonical prototypes defined in Section 2.3 are required to produce canonical simulations but from Theorem 2.1 and Theorem 2.2 whether a given transfer function can be synthesised as a canonical prototype depends on the parity of its numerator.

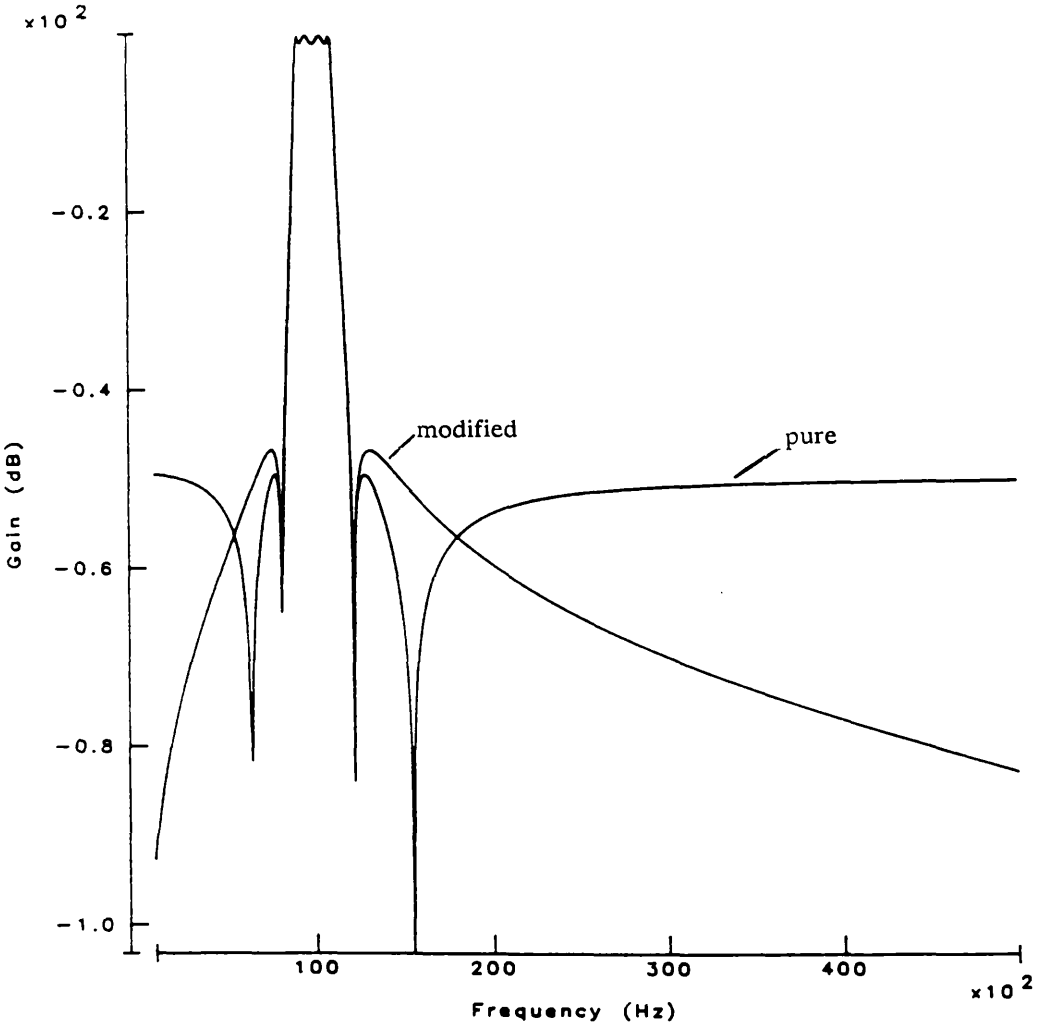


Fig.3.10. Pure and modified 8− th elliptic functions

In the following, a general method is introduced to design canonical active ladder circuits applied to both left and right decompositions. The basic principle is that any transfer function with only imaginary zeros can be modified so that they can be realised by a canonical prototype (a doubly− terminated SMPS or simply a ladder). Then a canonical simulation can be obtained with minimum numbers of intermediate variables (thus also the number of opamps). There is a uniform progression in the form of the circuit structures regardless of the type of specification or order.

3.5.2) Modified canonical prototype

Let H(s) be a transfer function with all its zeros on the imaginary axis or at infinity. If the order of H(s) is m, then it can be realised by a canonical ladder prototype, with m/2 nodes (for m even) or (m+1)/2 nodes (for m odd), provided that the constraints on the parity of the numerator given in Theorem 2.1 are met. However, even if the constraints are not met or more precisely if N(s) has the wrong parity, some simple manipulation of the transfer function can be made to cope with the problem. Consider three possibilities,

i) The numerator of H is a constant
ii) The numerator of H has a single root at $w_i=0$
iii) The numerator of H has a pair of imaginary roots at $\pm\omega_i$ (ω_i can be zero)

To change the parity

for i) let $H'(s) = H(s)s$
for ii) let $H'(s) = H(s)s$ or $H'(s) = H(s)/s$
for iii) let $H'(s) = H(s)s/(s^2+ \omega_i^2)$

Then the parity of H' is opposite to that of H and H'(s) can now be realised by a canonical prototype ladder described by the nodal equation

$$(sC + s^{-1}\Gamma + G)\ V = J \qquad (3.24)$$

3.5.3) Canonical ladder simulation by active circuits

A system realising the original transfer function H(s) can be obtained by multiplying the input vector J by inverse of the modification function. For case iii), we have

$$(sC + s^{-1}\Gamma + G)V = (s + \omega_i^2 s^{-1})J \qquad (3.25)$$

This system can now be expressed in realiseable form by the matrix methods of Section 3.3 and 3.4.

Left Matrix Decomposition form

Let $C = C_l C_r$ then the system can be witten as

$$\begin{cases} C_l W = -s^{-1} [\, \Gamma V + GV + \omega_i^2(-J)\,] & (3.26a) \\ C_r V = s^{-1} W - C_l^{-1}(-J) & (3.26b) \end{cases}$$

Right Matrix Decomposition form

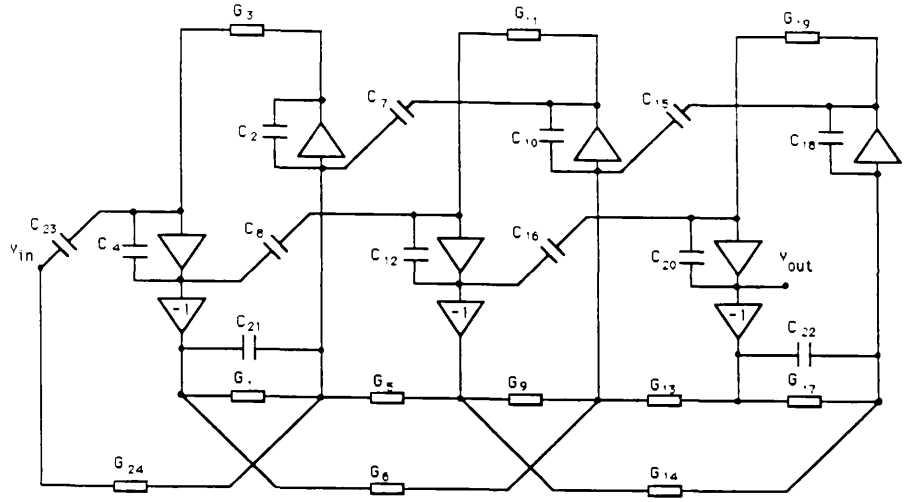
Let $\Gamma = \Gamma_l \Gamma_r$ then the system can be written as,

$$\begin{cases} CV = -s^{-1} (\Gamma_l W + GV) - (-J) & (3.27a) \\ W = s^{-1} [\, \Gamma_r V + \omega_i^2 \Gamma_l^{-1}(-J)\,] & (3.27b) \end{cases}$$

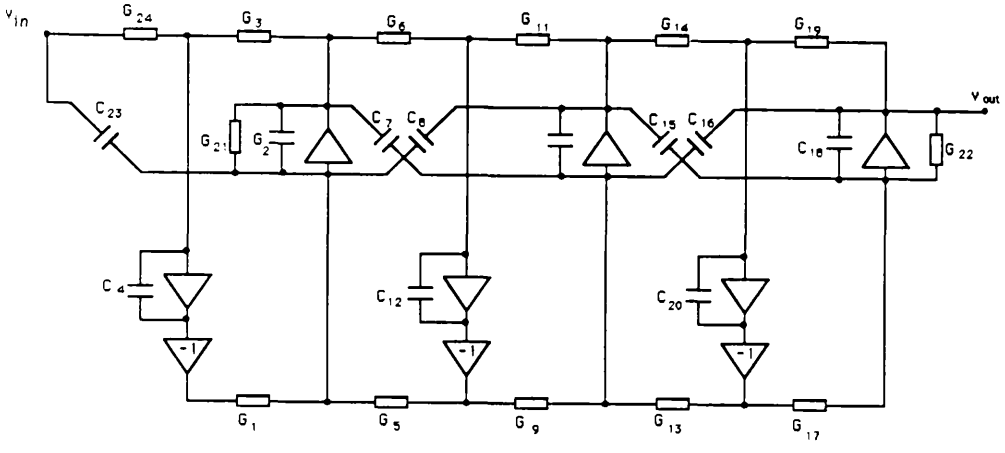
Active– RC networks can be directly obtained according to these two equations. It is found that the most efficient method in either case is to use UL factorisation which minimises the required number of input branches (only two).

Two canonical 6th order left– LUD and right– LUD circuits are shown in Fig.3.11. Their prototype is again the passive ladder shown in Fig.1.2, which is synthesised from the partitioned transfer function instead of the original transfer function. These canonical designs differ from standard ones in the position of the input stage branches.

The sensitivity behaviour of the new structures must be examined as they are no longer strictly ladder simulation and seem to depart from Orchard's low– sensitivity criterion [15]. From the many examples studied by computer simulation, the sensitivity for the new structures has been confirmed to be much better than their biquad counterparts, and very close to traditional ladder simulations.



(a)



(b)

Fig.3.11. Canonical ladder circuits

(a) Left– ULD type circuit

(b) Right– ULD type circuit

3.6 SPECIAL DESIGN TECHNIQUES

3.6.1) Hybrid matrix approaches

So far, only nodal equations have been employed to establish the SMPSs from the prototype. However, for certain prototypes, more general hybrid matrix descriptions can be adopted to minimise the size of the matrix systems and their resulting simulated circuits. The drawback of the hybrid method is that there is no unified rule. The exact design method depends on the individual prototype structures and the selection of the internal variables, which can be seen from the following examples,

Example 3.4:

An even order low-pass circuit shown in Fig.3.12 has n+1 nodes but the filter order is 2n. The rank of Γ is n as there are n inductors in the circuit, making the total number of op-amps required 2n+1, so even a leapfrog design cannot directly provide a canonical circuit. However If the nodal voltages, $v_1, \ldots v_n$, and a single mesh current i_n are selected as variables to replace v_{n+1}. The last two row equations have the following form

$$\left\{ s \begin{bmatrix} & \cdots & \\ \cdots c_{m-2} & c_{m-1}+c_{m-2} & 0 \\ & \cdots & L_{n-2} \end{bmatrix} + s^{-1} \begin{bmatrix} & \cdots & \\ \cdots L_{m-1}^{-1} & L_{m-1}^{-1} & 0 \\ & \cdots & 0 \quad 0 \end{bmatrix} + \begin{bmatrix} & \cdots & \\ \cdots & 0 & 1 \\ \cdots & -1 & 1/g_L \end{bmatrix} \right\} \begin{bmatrix} -v_{n-1} \\ v_n \\ i_n \end{bmatrix} = J \tag{3.28}$$

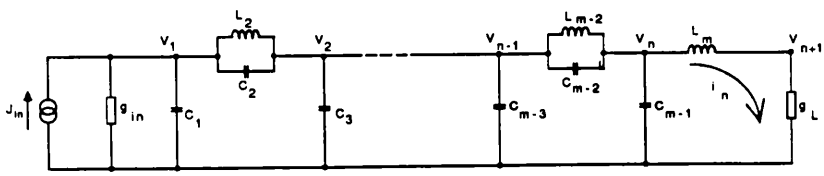


Fig.3.12. An even order lowpass ladder

The resulting equation will have the same form as (3.4) and will be canonical. The output is now i_n which differs from v_{n+1} by only a constant g_L. The rank of matrix Γ will be $n-1$ since the contribution of the $n-1$th inductor is now moved to the first matrix. This means that the number of intermediate variables to be introduced is n, providing a canonical solution.

Example 3.5:

The same technique, can be applied to the Left–decomposition designs for a 2n order bandpass prototype, Fig.3.13, derived from a n^{th} order lowpass reference with n even. There are $n+1$ nodes in the ladder, so a nodal description is not efficient. If the nodal voltages, $v_1, \ldots v_{n-2}$, and a single mesh current i_n are selected as variables to replace v_n and v_{n+1}. The last two row equations have the following form

$$\left\{ s \begin{bmatrix} & \cdots & \\ \cdots c_{m-2} & c_{m-1}+c_{m-2} & 0 \\ & \cdots & L_m \end{bmatrix} + s^{-1} \begin{bmatrix} & \cdots & \\ \cdots L_{m-1}^{-1} & L_{m-1}^{-1} & 0 \\ & \cdots & c_m^{-1} \end{bmatrix} + \begin{bmatrix} & \cdots & \\ \cdots & 0 & 1 \\ \cdots & -1 & 1/g_L \end{bmatrix} \right\} \begin{bmatrix} -v_{n-2} \\ v_{n-1} \\ i_n \end{bmatrix} = J \tag{3.29}$$

which provides a canonical solution.

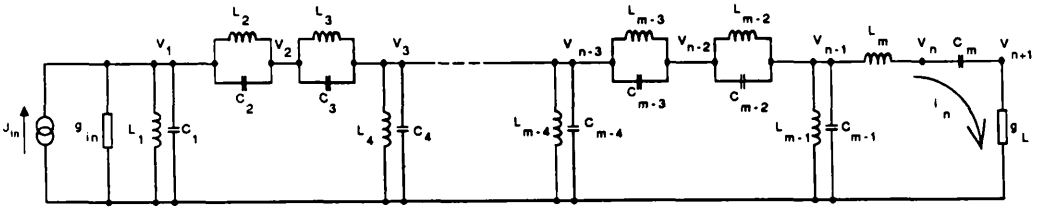


Fig.3.13. A bandpass ladder derived from an even order lowpass one

3.6.2) Inverse matrix approaches

The following system is apparently equivalent to (3.4).

$$W = -(s^{-1}\Gamma + G) V + J \qquad (3.30a)$$

$$V = s^{-1}PW \qquad (3.30b)$$

where $P = C^{-1}$. There are two notable properties of the system realised according to (3.30). First, it minimises the use of capacitors as the number of non–zero entries in matrices on the left hand side of (3.30) are minimised. This may be useful for certain fabrication technologies where the use of resistors is preferred to the use of capacitors. Second, the length of the capacitor–opamp chains is shortest, an important feature for fast op–amp settling time in SC circuits (Chapter 4).

The disadvantage of this method is that even when C is a tridiagonal matrix C^{-1} is usually a full matrix, representing a fully interconnected system. For larger C realisation will cost extra capacitors increasing with the square of the matrix order. For orders higher than 3, more components are generally required. However for a third order matrix fewer capacitors can be assured by using the following equivalence of (3.30b)

$$\begin{bmatrix} c_{11} & c_{12} & 0 \\ 0 & 1 & 0 \\ 0 & c_{32} & c_{33} \end{bmatrix} \begin{bmatrix} v_1 \\ -v_2 \\ v_3 \end{bmatrix} = s^{-1} \begin{bmatrix} 1 & 0 & 0 \\ p_{21} & p_{22} & p_{23} \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} w_1 \\ w_2 \\ w_3 \end{bmatrix} \qquad (3.31)$$

Only the middle row of (3.30b) is replaced by the inverse of C. The chain is still broken in the middle without the penalty of extra capacitors.

For high order filters with multiple zeros at infinity, C can be made a block diagonal matrix with second or third order diagonal blocks. Each of the blocks can be realised in the form of (3.30) or (3.31).

3.7 CASCADE BIQUADS DESIGN.

Finally we examine the design of cascade biquads filters which are in fact asymmetric matrix polynomial systems. Apart from the matrix symmetry, they can be described in exactly the same form as SMPSs,

$$AX = s^{-1}BX + s^{-1}CY + DY + EJ \qquad (3.32a)$$

$$FY = s^{-1}GY + s^{-1}HX + LX + MJ \qquad (3.32b)$$

where J is a vector of inputs

A, B, C, D, E, F, G, H, L and M are matrices

Rules from Section 3.2 can be applied to (3.32) in order to implement active– RC filters. Although the notation of (3.32) does not bring any advantages for biquad design, it provides a unified approach for internal processing of active– RC filters by computer, since both ladder and biquad simulations can be represented by tridiagonal matrix systems. Much advantage can be gained from this property in developing a unified strategy for the description of filter systems in computer arrays, as will be seen in Chapter 7.

3.8 SUMMARY

In the first part of this chapter, we defined certain forms of matrix equations as being directly realisable. It has been shown that other more complicated matrix systems can be transformed into directly realisable form by expansion, linearisation and the proper introduction of some intermediate variables.

A methodology was then developed to realise the SMPSs. A wide range of circuits were derived by adopting different matrix factorisations, notably LU and UL decompositions, including both existing and novel structures. A family of canonical ladder circuits were introduced to realise general transfer functions with regular, minimum sized circuits. It is also illustrated that a hybrid approach can be used to achieve canonical design for certain prototype where the nodal approach would be inefficient. A detailed comparison of these various circuit structures will be given in Chapter 7, regarding component spread, dynamic range and sensitivity.

It was shown that a matrix form description can also be used for cascade

biquad design, which incorporates various filter designs in a unified form.

Numerical designs and comparisons have not been given for active–RC circuits, but will be provided in Section 4.7 for SC circuits. This is partly because the industrial collaborators in this research have a major interest in SC filters. It can also be shown that the behaviour of active–RC, SC and digital ladders derived by the same prototype and the same technique would be very much the same if the ratio of sampling frequency to upper passband frequency is large enough. In fact under such a condition, a SC or digital circuit can be directly obtained from an active–RC circuit by replacement of continuous–time integrators by LDI–type integrators [25,51,79] and the frequency response will be approximately preserved as well as the sensitivity, component spread and dynamic range properties. Since the results are similar, a single comparison for SC circuits will be sufficient.

Both approximate and exact design procedures for SC and digital filters will be discussed in Chapter 4 by extending the matrix methods covered above.

CHAPTER 4

MATRIX METHODS FOR SC AND DIGITAL LADDER DESIGN

4.1 INTRODUCTION

In the last chapter a detailed investigation of matrix methods for active– RC ladder design has been presented. Now the extension of these techniques to the discrete domain systems of SC and digital circuits will be considered .

The design procedure of a discrete domain (or z– domain) ladder starts from a prototype in the s– domain. Some frequency mappings, namely LDI or bilinear transformations, are applied to transform the prototype system from the s– domain to the z– domain. Matrix methods will then be developed to represent the system by SFGs realisable by SC or digital circuits.

For LDI transformed systems [79], it is shown that the design procedure is nearly the same as that in the continuous domain since, apart from some frequency pre– warping, a pair of continuous– time integrators can be directly replaced by a pair of LDI type SC or digital integrators. However the LDI design requires a complicated procedure to eliminate the distortion caused by improperly realised terminations [63,64]. The bilinear transformation, on the other hand, has the advantage of both stability and exactness [12]. Unfortunately, SC bilinear integrators are sensitive to the stray capacitance [35] and are not practically useful. Digital circuits using bilinear integrators are unrealisable due to delay– free loops [18]. A compromise approach is to realise the bilinearly transformed system by employing LDI integrators. This so– called bilinear– LDI type design has attracted much attention from researchers [51][53][80].

In this chapter LDI type ladders are first introduced to illustrate the principles of the matrix methods in the discrete domain. Then bilinear– LDI type ladder systems are derived from a matrix approach, which is shown to be much more concise than present topological derivations. A discussion of the relative network complexities of LDI and bilinearly transformed systems will follow. In many cases, the structures are identical except for different input stages. However, for prototypes with purely inductive branches (without a parallel capacitor) the LDI structure is simpler than the corresponding bilinear– LDI one. A simple technique is introduced to cancel excess components in the bilinear– LDI structures, combining the advantages of simple structure of LDI and exact frequency response of bilinear transformations.

An important feature of the LUD decomposition method applied to discrete filter design is that it can produce ladder simulations without delay free loops,

which is vital for digital implementaions. Although the principle of LUD type digital filter design is very similar to that of LUD SC one, there are some special considerations for reducing the cost of components with the help of the flexibility of digital circuits. In a digital circuit, multiplication is most costly in terms of both time and storage. It is shown in this chapter that a combination of left and right decomposition methods can greatly reduce the number of multiplication operations.

Another important concept in digital signal processing is parallelism [75]. In some low sensitivity digital structures, such as wave digital circuits [73], the operations must follow a certain sequence which limits the extent to which their operation speed can be optimised by adopting parallel processing techniques. An interesting property is that structures with a low degree of parallelism in digital implementation will also possess the problem of unswitched opamp–capacitor chains in SC implementation. Indeed, the procedure of capacitor charging along such loops is comparable to a series of sequential operations in a digital circuit. Two techniques are introduced in this chapter to increase the parallelism of a digital ladder. The first is to place zeros on the real frequency axis to break the series feedthrough chains. Further improvements are possible by the inverse matrix discussed Section 3.6.2. The second is a scaling method for digital circuits, whereby multiplication coefficients are scaled to powers of two, which can be easily implemented by some series shifts of bit patterns followed by some parallel multiplications.

Detailed examples will be given to illustrate the new design procedure and comparisons of the novel structures with existing ones will be presented.

4.2 LDI TRANSFORMED DISCRETE LADDERS

4.2.1) LDI transformed systems

Define LDI transformation (T is the sampling period)

$$s \rightarrow \frac{2}{T} \frac{1 - z^{-1}}{z^{-1/2}} \qquad (4.1a)$$

and a pair of LDI integration operators

$$\Phi = 1/(1-z^{-1}) \tag{4.1b}$$

$$\Psi = z^{-1}/(1-z^{-1}) \tag{4.1c}$$

Applying the LDI transformation to (3.4) and introducing an extra half period delay at the terminations for stability [79], (3.1) becomes

$$Y(z)\ V = J \tag{4.2a}$$

$$Y(z) = \left[\frac{2}{T} \frac{1 - z^{-1}}{z^{-1/2}} C + \frac{T}{2} \frac{z^{-1/2}}{1 - z^{-1}} \Gamma + z^{\pm 1/2} G \right] \tag{4.2b}$$

Multiply equation (4.2a) through by $z^{1/2}$ to get

$$\left(\frac{1}{\Psi} A + \Phi B + G \right) V = J' \tag{4.3a}$$

$$A = (2/T)C,\ B = (T/2)\Gamma,\ J' = z^{1/2}J \tag{4.3b}$$

Multiply equation (4.2) through by $z^{-1/2}$ to get

$$\left(\frac{1}{\Phi} A + \Psi B + G \right) V = J' \tag{4.3c}$$

$$A = (2/T)C,\ B = (T/2)\Gamma,\ J' = z^{-1/2}J \tag{4.3d}$$

As the transfer functions from J and J' to the output differ only by a delay of a half period, we will not distinguish between them in the following discussion.

Both systems in (4.3) have a similar appearance to the continuous system (3.4) and matrix decomposition techniques can be applied again to create a set of intermediate variables relating two linear subsystems. Due to the difficulty of realising the terminating stages, it is found convenient to use (4.3a) as the basis for left decomposition design and (4.3c) for right decomposition.

Left Matrix Decomposition

Factorisation of the left hand matrix **A** in (4.3a) into $\mathbf{A} = \mathbf{A}_l\mathbf{A}_r$ results in the following pair of equations

$$A_l W = -(\Phi B + G) V + J \qquad (4.4a)$$

$$A_r V = \Psi W \qquad (4.4b)$$

Right Matrix Decomposition

B can also be factorised as $B = B_l B_r$ in (4.3c), leading to the right decomposition system

$$AV = -\Phi (B_1 W + GV) + \Phi J \qquad (4.5a)$$

$$W = \Psi B_r V \qquad (4.5b)$$

4.2.2) SC LDI ladders

The same procedure can be applied to convert the system description of (4.4) and (4.5) to a SC circuit realisation as described in the last chapter for active– RC implementation, with the replacement of the continuous time operator s^{-1}, by a pair of LDI SC operators, Ψ and Φ, Fig.4.1. The matrix decompositions can again be carried out by LU or by direct methods, resulting in the various SC circuits in Fig.4.2.

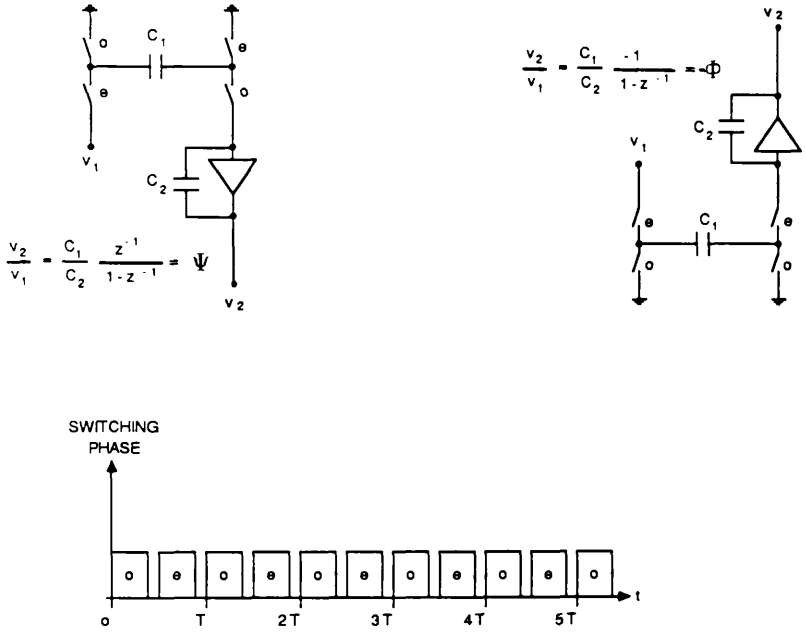
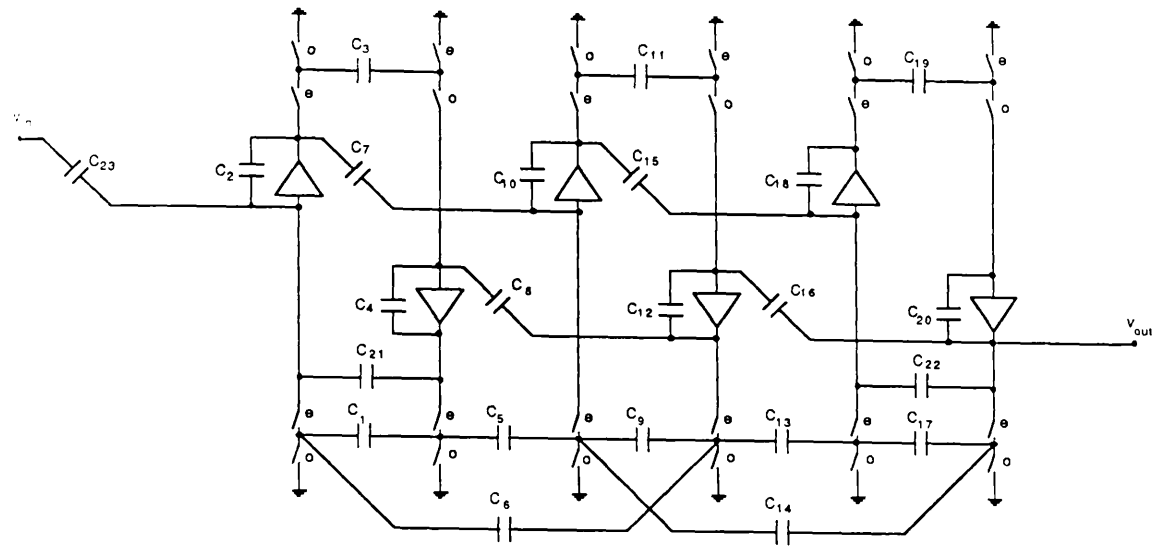
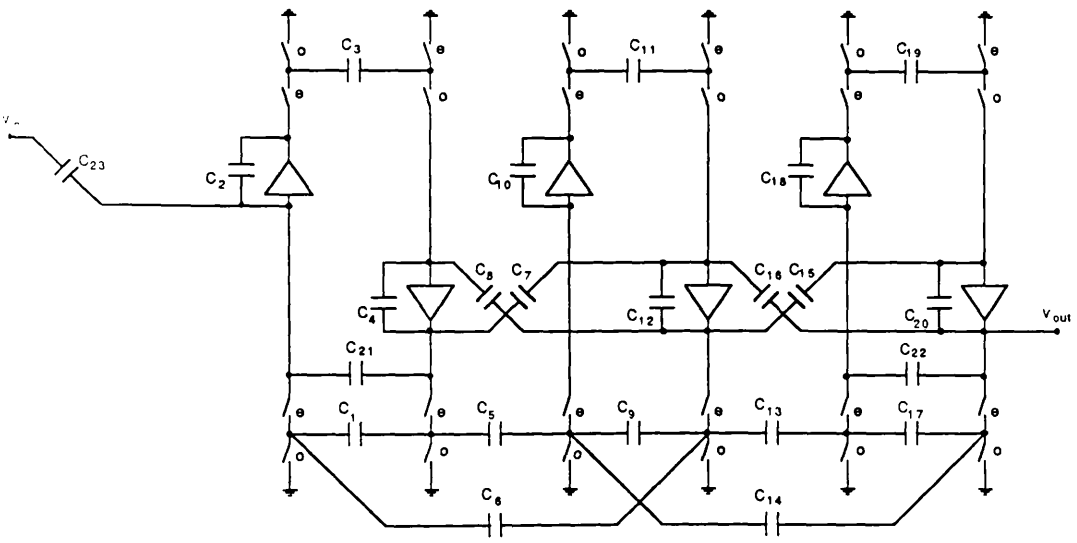


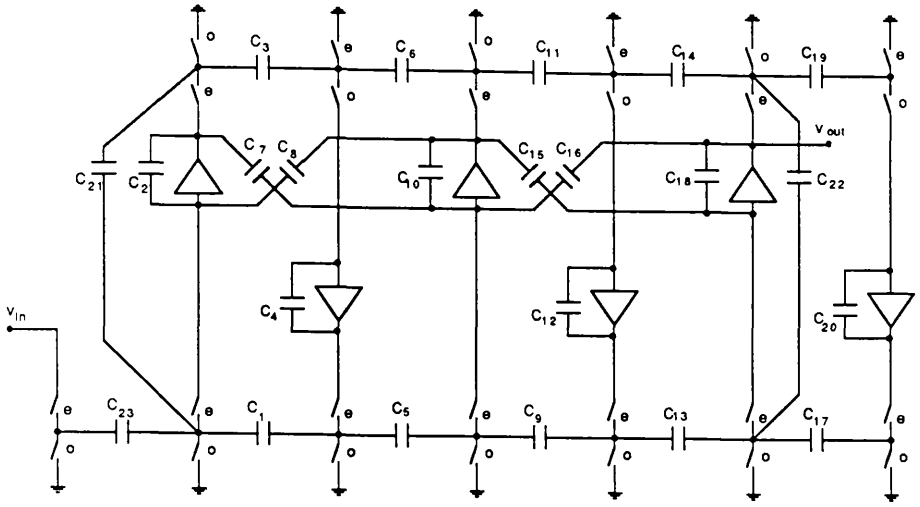
Fig.4.1 A pair of SC LDI integrators


C3
C11
C19
C23
C2
C7
C10
C15
C18
C4
C8
C12
C16
C20
Vout
C21
C22
C1
C5
C9
C13
C17
C6
C14

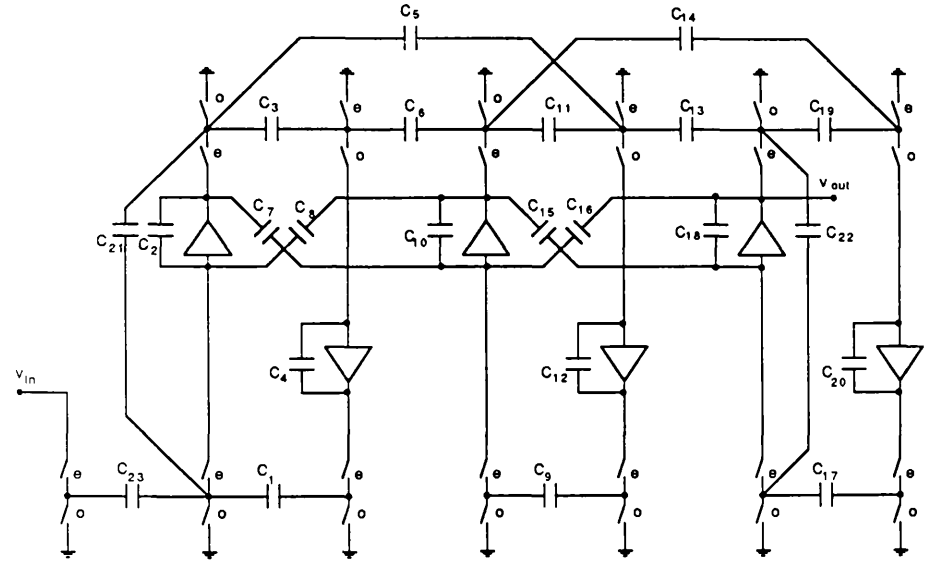
(a)


C3
C11
C19
C23
C2
C10
C18
C8
C7
C16
C15
C4
C12
C20
Vout
C21
C22
C1
C5
C9
C13
C17
C6
C14

(b)



(c)



(d)

Fig.4.2 Various SC circuit structures

(a) Left– LUD type SC circuit

(b) Left– Direct(IA) type SC circuit

(c) Right– LUD type SC circuit

(d) Right– Direct(BI) type SC circuit

The left−LUD SFG is distinguished by the absence of delay−free−loops, which may be seen from Fig.4.2 to be dependent on the presence of non−zero, off−diagonal entries in matrix **A**. If **A** is LU decomposed no delay−free−loop are formed, since the upper and lower off−diagonal elements are separated. Removal of such loops will reduce the opamp voltages settling time so that filter performance is less prone to finite switch resistance and op−amp GB effects [35].

4.3 BILINEARLY TRANSFORMED DISCRETE LADDERS

4.3.1) Bilinear−LDI systems

In LDI transformed ladders, a $z^{\pm 1/2}$ factor is introduced to represent the improperly realised terminations and to ensure stability, causing a distortion of the designed frequency response. The bilinear transformation, on the other hand, has the advantage of both stability and exactness. Unfortunately, bilinear integrators are sensitive to the stray capacitance and are not practically useful. Instead an equivalent SC ladder utilising LDI integrators can be formed.

After bilinear transformation

$$s \rightarrow \frac{2}{T}\,\frac{1-z^{-1}}{1+z^{-1}} \tag{4.6}$$

(3.4) becomes

$$\left[\frac{2}{T}\,\frac{1-z^{-1}}{1+z^{-1}}\,C + \frac{T}{2}\,\frac{1+z^{-1}}{1-z^{-1}}\,\Gamma + G\right]V = J \tag{4.7a}$$

and multiplying the system through by $(1+z^{-1})/(1-z^{-1})$ to get

$$\left[\frac{2}{T} C + \frac{T}{2} \left[\frac{1 + z^{-1}}{1 - z^{-1}} \right]^2 \Gamma + \frac{1 + z^{-1}}{1 - z^{-1}} G \right] V = - \frac{1 + z^{-1}}{1 - z^{-1}} J \qquad (4.7b)$$

Eq.(4.7) can be rearranged as

$$\left(\frac{1}{\Psi} A + \Phi B + D \right) V = J' \qquad (4.8a)$$

$$A = 2/TC+T/2\Gamma+G \quad B = 2T\Gamma \quad D = 2G \quad J'' = (1+z)J \qquad (4.8b)$$

or

$$\left(\frac{1}{\Psi} A + \Phi B + D \right) V = J' \qquad (4.8c)$$

$$A = 2/TC+T/2\Gamma-G \quad B = 2T\Gamma \quad D = 2G \quad J'' = (1+z^{-1})J \qquad (4.8d)$$

4.3.2) SC bilinear– LDI ladders

Although based on two different transformations, (4.3) and (4.8) have the same appearance apart from the input terms. This equivalence makes it possible to design bilinear ladder using LDI integrators, a fact indicated first by Lee and Chang [51] from a topological basis for SC circuits. Application of the methods of Section 4.2.2 to (4.8) results in a similar range of circuit structures.

The input of (4.8) has a $(1+z)$ or $(1+z^{-1})$ multiplier. The realisation of the noncausality of $(1+z)$ can be accomplished by multiplying by z^{-1} giving $(1+z^{-1})$, introducing a delay of one period. Its realisation has a range of choices.

i) Direct realisations of $(1+z^{-1})$ for left–decomposition designs and $(1+z^{-1})/(1-z^{-1})$ for right decomposition designs can be achieved by using some special circuit arrangements, Fig.4.3.

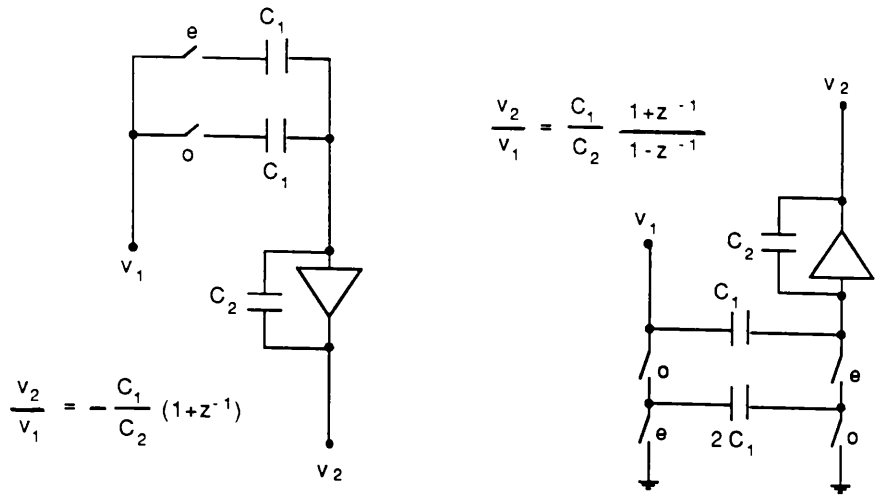


Fig.4.3 SC realisation of bilinear input functions

ii) Alternatively the following systems can be used for left and right decompositions

Left Matrix Decomposition

$$A_l W = -(\Phi B + D) V - 2(-J) \qquad (4.9a)$$

$$A_r V = \Psi W - A_l^{-1} (-J) \qquad (4.9b)$$

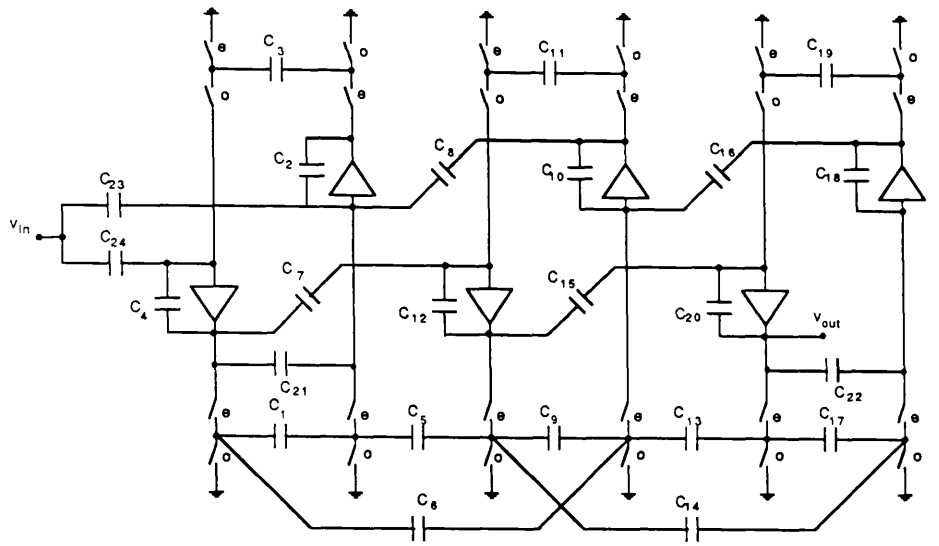
Right Matrix Decomposition

$$AV = -\Phi (B_l W + DV) - J \qquad (4.10a)$$

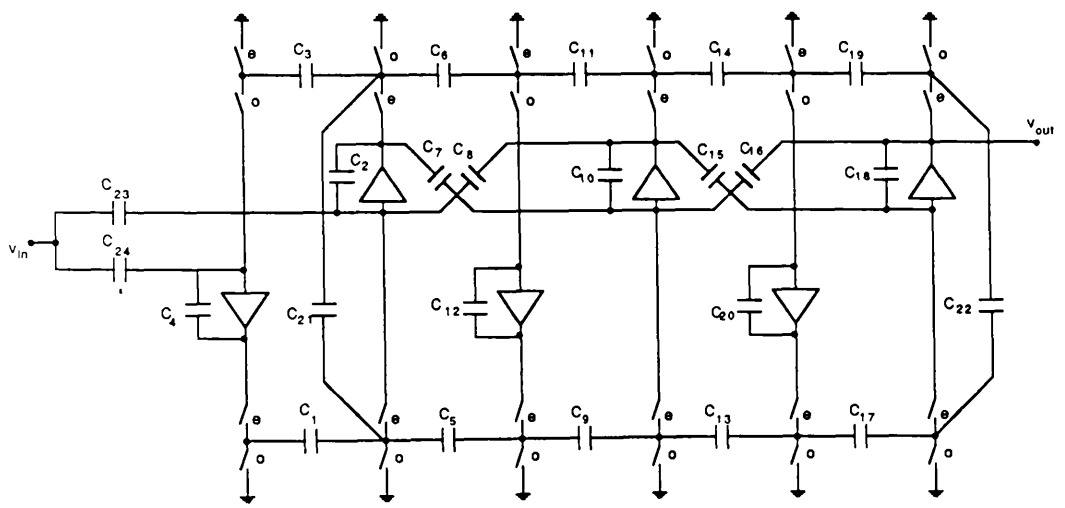
$$W = \Psi B_r V - 2B_l^{-1} J \qquad (4.10b)$$

It can be verified that (4.9) and (4.10) are equivalent to the original system (4.8b,c) respectively. They can be directly simulated by SC circuits with LDI type integrators. Notice if J has only one nonzero input, i.e., J = [J_1, 0,...0], it is preferable to have the first column of A_l^{-1} and B_l^{-1} with as few nonzero entries as possible. This number is minimised to one when A_l^{-1} and B_l^{-1} are

upper triangular matrices or in other words when UL or IA or IB decompositions are selected. For digital realisation this method is canonical in sense of the number of the delays. Examples of sixth order left– and right–LUD designs are shown in Fig.4.4.



(a)



(b)

Fig.4.4 Exact Bilinear–LDI SC ladders

(a) Left–ULD type circuit

(b) Right–ULD type circuit

iii) Both the above methods require some extra components which may be a significant layout overhead for low order filters. They may be simply dispensed with by replacing the $(1+z^{-1})$ factor in the numerator function by 1 or z^{-1}, resulting the same circuit structures as LDI ones. However this incurs a penalty warping function of $(1+z)^{-1}$ or $z^{-1/2}\cos^{-1}(\omega T/2)$ and a zero at half the sampling frequency is lost. The distortion introduced in the passband by $\cos(\omega T/2)$ can be corrected by prewarping the original prototype ladder. This can also be conveniently combined with sin(x)/x correction resulting in a x/tan(x) function, which can then be superimposed on the frequency response specifications [117]. If the sampling frequency is very high compared with central frequency, which is met by most practical design, $x/\tan(x) \simeq 1$ and no real compensation is necessary.

Example 4.1:

The bandpass ladder of Fig.1.2 is simulated by four switched–capacitor circuits as shown in Fig.4.2. The design data are given in Table 4.1 and Table 4.2. All the simulation circuits have been scaled for the maximum opamp output of 1. The input stages have been chosen as single–input as mentioned above in iii). The sampling frequency is high enough to make the distortion negligible. The response of the circuits is shown in Fig.4.5a,b. It can be seen that a zero at half the sampling frequency is lost for single–input type circuits. The following indices are used as global measures of system sensitivity and dynamic range respectively

$$s(\omega) = \left\{ \sum_i \left[\frac{c_i}{|H(\omega)|} \frac{\partial |H(\omega)|}{\partial c_i} \right]^2 \right\}^{1/2} \qquad (4.11a)$$

$$d(\omega) = \left\{ \prod_m |H_m(j\omega)| \right\}^{1/M} \qquad (4.11b)$$

where $\{c_i\}$ and $\{H_m\}$ are the sets of capacitances and opamp output voltage, respectively, and M is the number of opamps. Plots of $s(\omega)$ and $d(\omega)$ of the filters can be compared with a biquad circuit in Fig.4.6a,b, where $d(\omega)$ has been converted into dB, i.e., 20log(d). It can be observed that the ladder simulations have lower sensitivity than the biquad circuit. Notice that circuits obtained from the left matrix decomposition exhibit high sensitivity near 0Hz. The biquad appears to have the best dynamic range for this particular example. Left decomposition circuits have considerably smaller capacitance spread than right decomposition ones and biquads.

C_1	0.3465	C_2	0.1580	L_2	0.2484
C_3	0.6119	C_4	0.0596	L_4	0.3006
C_5	0.4836			L_5	4.0362
Gin	1.0000	G_L	0.8802		

Sampling frequency	100	KHz
Lower passband edge	300	Hz
Upper passband edge	3400	Hz
Passband ripple	< 0.2	dB
Lower stopband edge	10	Hz
Lower stopband att.>	30	dB
Upper stopband edge	5000	Hz
Upper stopband att. >	45	dB

Table 4.1 Design data for the prototype ladder

	Left-LUD	Left-Direct(IA)	Right-LUD	Right-Direct(BI)
C_1	1.000	1.000	3.147	3.147
C_2	9.174	9.174	9.392	9.392
C_3	1.000	1.000	1.000	1.000
C_4	3.620	3.620	9.821	9.821
C_5	1.615	1.615	3.387	1.615
C_6	1.266	1.266	1.266	1.266
C_7	4.445	3.435	3.435	3.435
C_8	1.375	1.375	4.044	4.044
C_9	3.736	3.736	2.391	5.433
C_{10}	21.697	25.451	22.474	22.474
C_{11}	4.632	5.433	1.690	3.736
C_{12}	21.169	22.474	11.201	25.451
C_{13}	1.573	1.573	2.935	1.000
C_{14}	1.000	1.000	1.000	1.573
C_{15}	1.612	1.000	2.074	1.473
C_{16}	1.000	1.000	1.000	1.000
C_{17}	1.000	1.000	1.000	2.137
C_{18}	8.326	9.325	9.953	7.070
C_{19}	1.000	1.265	1.000	1.000
C_{20}	4.804	5.475	51.232	10.686
C_{21}	3.907	3.907	1.252	1.252
C_{22}	4.999	4.999	1.407	1.000
C_{23}	3.120	3.120	1.000	1.000
total	111.199	117.373	150.109	123.014
spread	21.697	25.451	51.232	25.451

Table 4.2 Design data for various SC ladder simulations

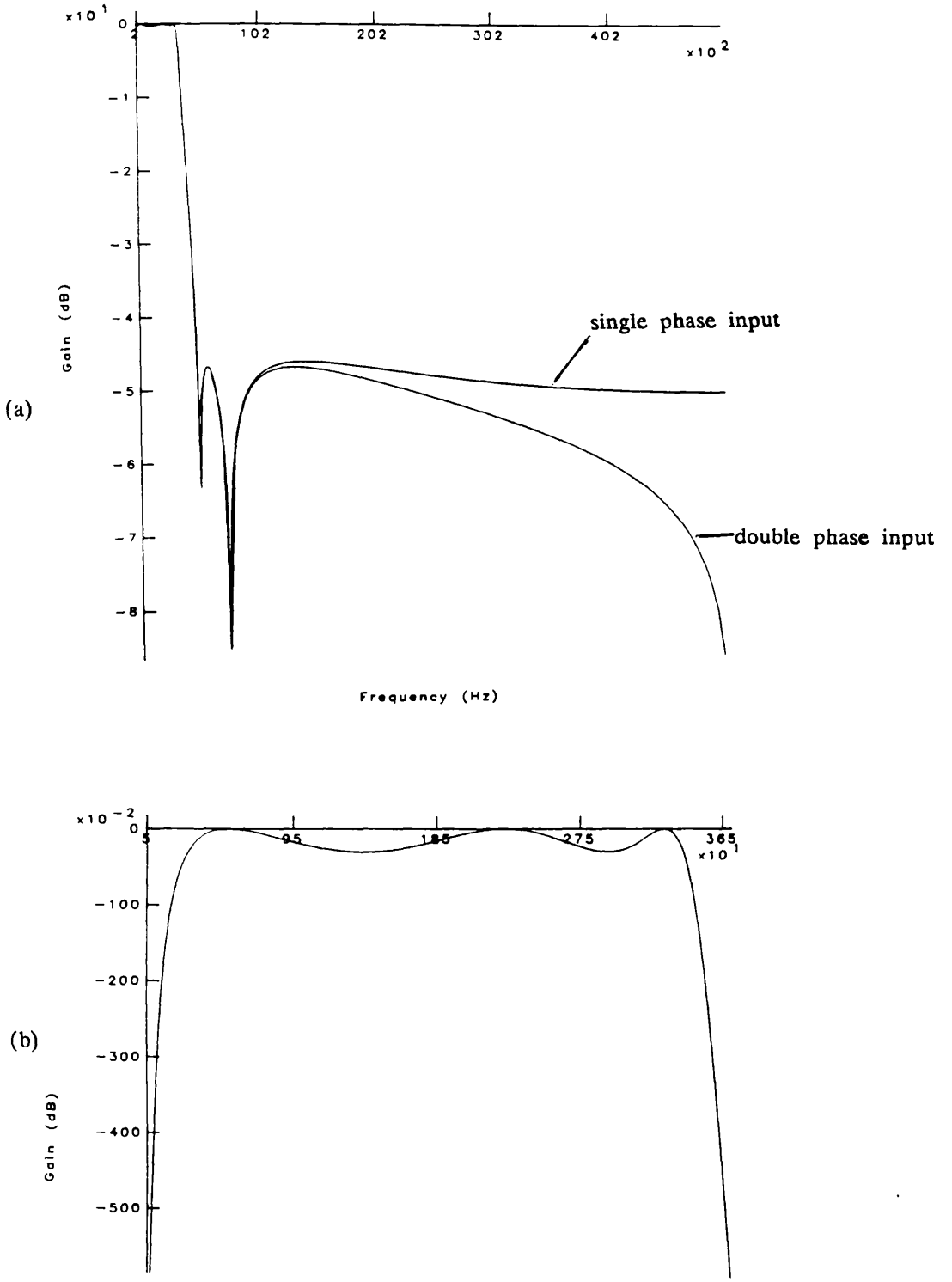


Fig.4.5 A 6th order bandpass function

(a) Overall response

(b) Passband response

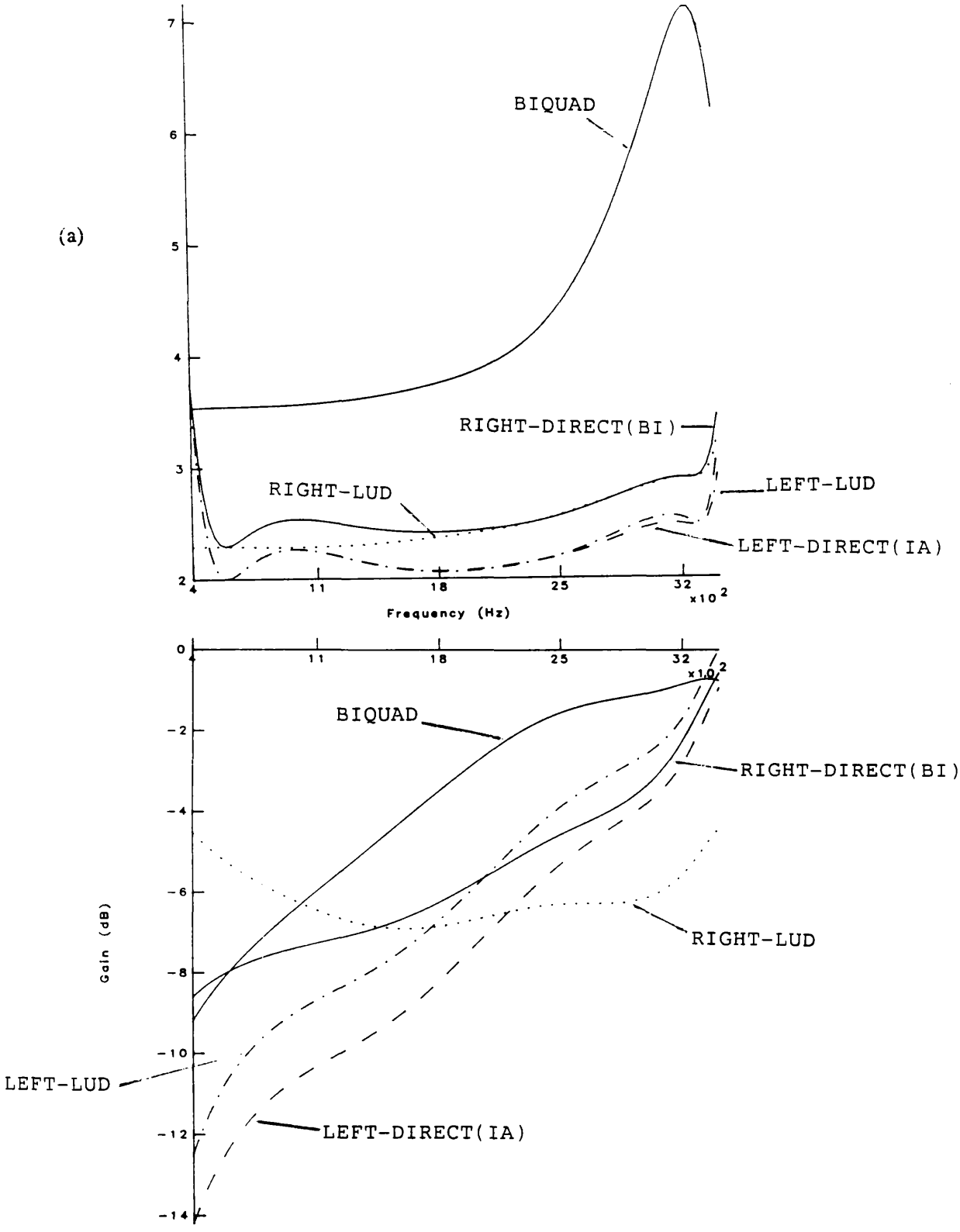


Fig.4.6 Comparison of system performance

(a) Sensitivity

(b) Dynamic range

4.3.3) UL−LU and LU−UL SC ladders

The UL−LU and LU−UL design can also be applied to SC circuits. The principle is the same as that for RC circuits, apart from some consideration for the termination stages to get correct arrangement of switching phases. Eq.(4.7) can be rearranged as

$$\left(\frac{1}{\Psi} A + \Phi B + zD_1 + D_n \right) V = (1+z)J' \qquad (4.12a)$$

$$A=2/TC+T/2\Gamma-G_1+G_n \quad B=2T\Gamma \quad D_1=2G_1 \quad D_n=2G_n \qquad (4.12b)$$

or

$$\left(\frac{1}{\Phi} A + \Psi B + z^{-1}D_1 + D_n \right) V = (1+z^{-1})J \qquad (4.12c)$$

$$A=2/TC+T/2\Gamma+G_1-G_n \quad B=2T\Gamma \quad D_1=2G_1 \quad D_n=2G_n \qquad (4.12d)$$

Formulae for UL−LU ladder design

Let

$$A = U_a L_a \qquad (4.13a)$$

$$B = L_b U_b \qquad (4.13b)$$

Define

$$W_a = \Psi^{-1} (L_a V + U_a^{-1} J) \qquad (4.13c)$$

$$W_b = U_b V \qquad (4.13d)$$

$$G_1 = \mathrm{diag}[g_{11}, 0, \ldots, 0] \qquad (4.13e)$$

$$G_n = \text{diag}[\ 0,\ldots,0,\ g_{nn}\ ] \tag{4.13f}$$

$$D_{1s} = 2\ G_1\ L_a^{-1} \tag{4.13g}$$

$$D_{ns} = 2\ G_n\ U_b^{-1} \tag{4.13h}$$

The upper triangular matrix U_{as} and lower triangular matrix L_{bs} are defined to satisfy the identity

$$U_{as}\ L_a = L_{bs}\ U_b \tag{4.13i}$$

Also let

$$J' = -(1+D_{1s}A^{-1})J \tag{4.13j}$$

Then (4.11a) can be linearised as

$$\begin{cases} U_a\ W_a = -[(\Phi L_b+D_{ns})W_b+\Phi D_{1s}W_a] - (2+D_{1s}U_a^{-1})J & (4.14a) \\ L_{bs}\ W_b = \Psi\ U_{bs}\ W_a - U_{as}U_a^{-1}J & (4.14b) \end{cases}$$

The output is w_{bn}.

Formulae for UL–LU ladder design

Let

$$A = L_a\ U_a \tag{4.15a}$$

$$B = U_b\ L_b \tag{4.15b}$$

Define

$$W_a = U_a\ V \tag{4.15c}$$

$$W_b = \Psi\ L_b\ V - 2U_b^{-1}J \tag{4.15d}$$

$$G_1 = \mathrm{diag}[\, g_{11},\ 0,\ldots,0\ ] \tag{4.15e}$$

$$G_n = \mathrm{diag}[\, 0,\ldots,0,\ g_{nn}\ ] \tag{4.15f}$$

$$D_{1s} = 2\, G_1\, L_b^{-1} \tag{4.15g}$$

$$D_{ns} = 2\, G_n\, U_a^{-1} \tag{4.15h}$$

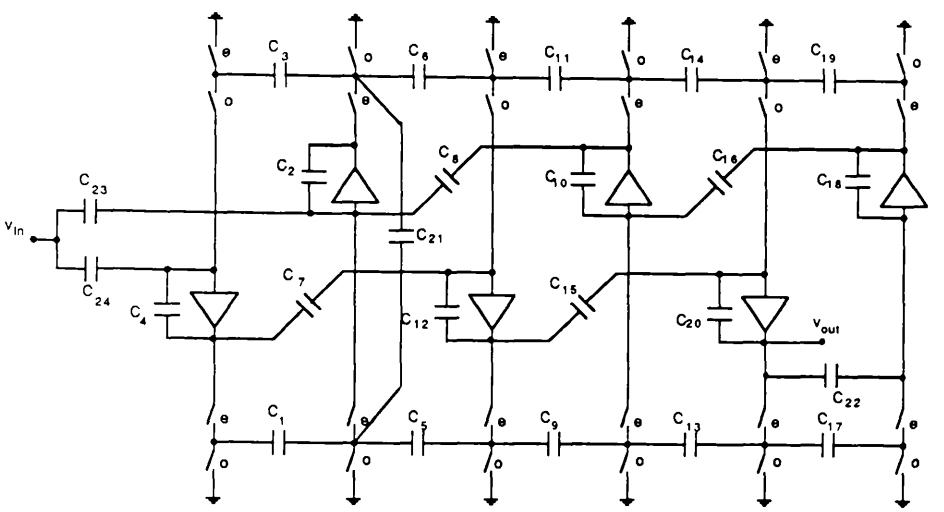
The lower triangular matrix L_{as} and upper triangular matrix U_{bs} are defined to satisfy the identity

$$L_{as}\, U_a = U_{bs}\, L_b \tag{4.15i}$$

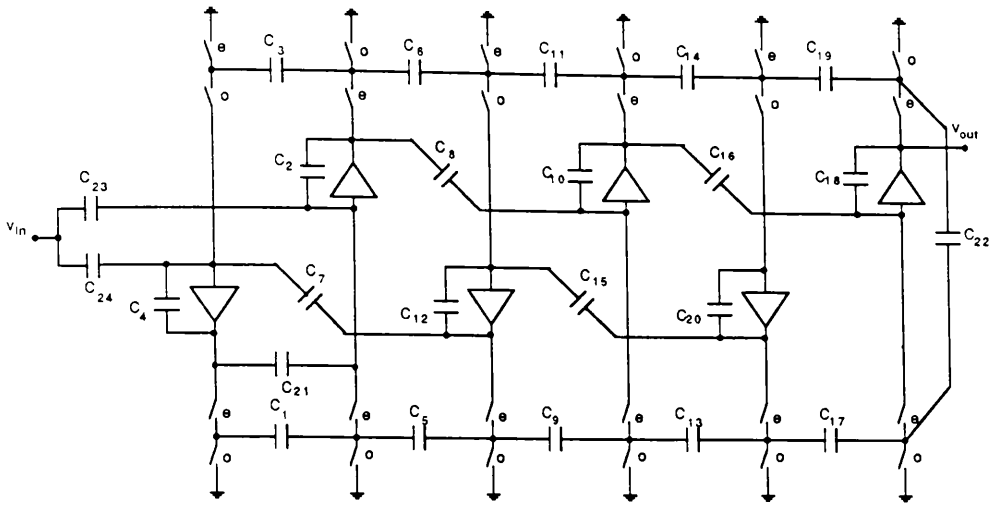
Then (4.11c) can be linearised as

$$\begin{cases} L_a\ W_a = -[(\Phi U_b + D_{1s}) W_b + \Phi D_{ns} W_a] - (1+2D_{1s}U_b^{-1})J & (4.16a) \\ U_{bs}\ W_b = \Psi\, L_{as}\, W_a - 2U_{bs}U_b^{-1}J & (4.16b) \end{cases}$$

The output is w_{an}. Two examples of UL−LU and LU−UL circuits are shown in Fig.4.7.



(a)



(b)

Fig.4.7 (a) A UL−LU SC ladder and (b) A LU−UL SC ladder

4.3.4) Canonical discrete ladders

Canonical SC ladders can be designed in the same manner as that for active−RC circuits. Suppose that a change of parity of the numerator of the transfer function has been applied as Section 3.5.2. Start from the modified prototype (3.25) and perform the bilinear transformation

$$\left[\frac{2}{T}\frac{1-z^{-1}}{1+z^{-1}} C + \frac{T}{2}\frac{1+z^{-1}}{1-z^{-1}} \Gamma + G \right] V = \frac{2}{T}\frac{1-z^{-1}}{1+z^{-1}} J + \frac{T}{2}\frac{1+z^{-1}}{1-z^{-1}} \omega_i{}^2 J \qquad (4.17a)$$

The system can be rearranged as

$$\left(\frac{1}{\Psi} A + \Phi B + D \right) V = (1+ \omega_i{}^2)\frac{1}{\Psi} J + 4\Phi\omega_i{}^2 J \qquad (4.17b)$$

or

$$\left(\frac{1}{\Phi} A + \Psi B + D \right) V = (1+ \omega_i^2)\frac{1}{\Phi} J + 4\Psi\omega_i^2 J \qquad (4.17c)$$

where **A**, **B** and **D** are defined in the same way as in (4.8). The above equations can be linearised respectively as

Left Matrix Decomposition

$$A_l W = -(\Phi B + G) V - \Phi 4\omega_i 2(-J) \qquad (4.18a)$$

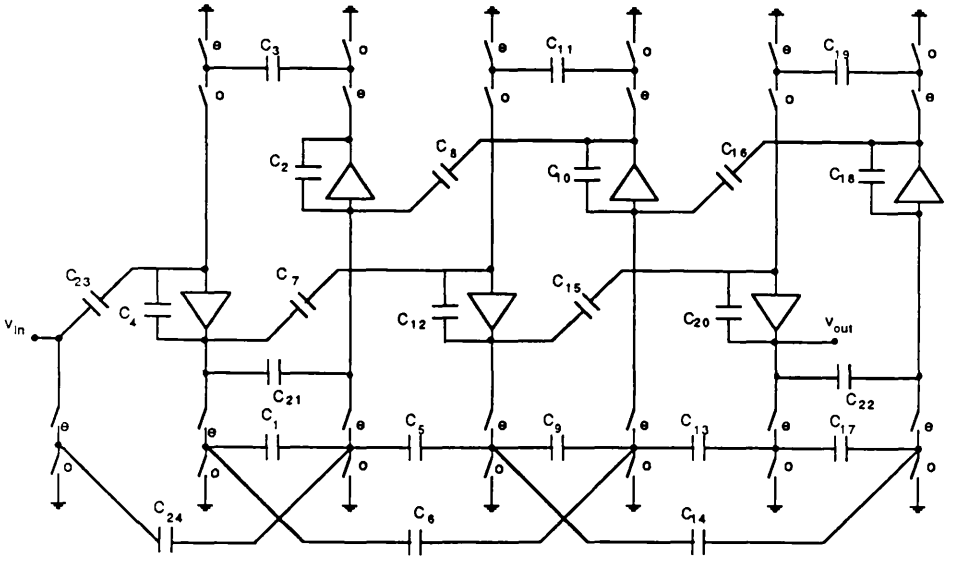
$$A_r V = \Psi W - A_l^{-1}(\omega_i^2 + 1)(-J) \qquad (4.18b)$$

Right Matrix Decomposition

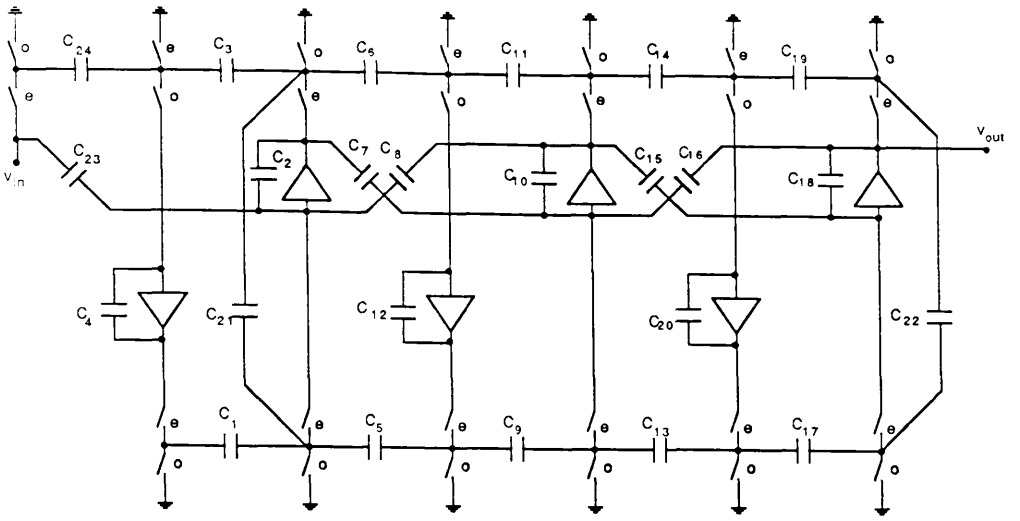
$$AV = -\Phi (B_l W + GV) - (\omega_i^2 + 1)(-J) \qquad (4.19a)$$

$$W = \Psi (B_r V + 4\omega_i^2 B_l^{-1})(-J) \qquad (4.19b)$$

Some examples of these canonical circuits by UL decompositions are shown in Fig.4.8.



(a)



(b)

Fig.4.8 Canonical Bilinear– LDI SC ladders

(a) Left– ULD type circuit

(b) Right– ULD type circuit

4.4 MODIFICATION OF BILINEAR DISCRETE LADDERS

In some cases matrix **A** in (4.8) has more non– zero entries than its counterpart matrix in (4.3), costing more circuit elements in realisation. This happens when there are inductance branches without corresponding parallel capacitance branches in the prototype and consequently **A** is less sparse than **C** after adding the non– zero entries of $(T/2)\Gamma$ to the zero entries of $(2/T)\mathbf{C}$. The pure inductance branches are normally used to realise poles at infinity. Since the entries in $(T/2)\Gamma$ are usually much smaller than those in $(2/T)\mathbf{C}$, addition of $(T/2)\Gamma$ to $(2/T)\mathbf{C}$ also causes an uneven distribution of values in **A** and results in a large capacitance spread in the SC implementation.

The difficulty can be overcome by placing a negative capacitor, C_i, in parallel with the purely inductive branch, L_i, of value

$$C_i = -\frac{T^2}{4}\frac{1}{L_i} \qquad (4.20)$$

Then from (4.8) the contributions of C_i and L_i will cancel each other. This reduces both the number of capacitors and spread of capacitance values. The resonant frequency of the pole due to C_i and L_i is given by

$$s_r^2 = \frac{-1}{L_i C_i} = \frac{4}{T^2} = (\pm 2f_s)^2 \qquad (4.21)$$

where f_s is the sampling frequency. If L_i is a series inductance branch in a ladder, s_r will become a pole of the transfer function. The response error thus caused can be eliminated in the approximation procedure, by replacing poles at infinity by ones at $-2f_s$ on the real axis. The negative capacitance required can then be incorporated in the synthesis of the passive ladder prototype [117]. The low-sensitivity properties are not influenced by the introduction of negative elements (Section 2.4).

4.5 HIGH ORDER DISCRETE FILTER DESIGN

In *left-LUD* design, the matrix **A** is decomposed into LU triangular form,

$$\mathbf{A} = \mathbf{L_a L_a}^T \qquad (4.22)$$

The separation of the non-zero off-diagonal entries to $\mathbf{L_a}$ and $\mathbf{L_a}^T$ remove the delay-free loops common to leapfrog and coupled-biquad simulations.

The main circuit features influencing opamp settling times for SC realisation are now the long unswitched chains opamps and capacitors along which signals will be delayed. The problem is not specific to *left-LUD* design and exists together with delay-free loops in other circuits.

Exactly the same problem is reflected in digital realisations as the long chain of series multiplication operations without interruption by delays. These operations must be performed in a sequential order and so prevent the use of parallel processing techniques.

The above problems arise when matrix **A** has successive non-zero

off− diagonal entries. They can be avoided for low order design (with matrix orders less than or equal to 3) by application of the inverse matrix method introduced in Section 3.6.2.

For high order SC filters, the inductor and negative capacitor pairs introduced in Section 4.6 can be used to cancel the off− diagonal non− zero entries in **A** and therefore break the long chains. A combination of negative elements and the inverse matrix decomposition is useful, provided differential integrators are available. Real zeros can be introduced, to make **A** a block diagonal matrix with second or third order diagonal blocks. Each of the blocks can be realised by the inverse matrix method with the shortest unswitched chains. High order filters which are particularly sensitive to non− ideal factors like finite opamp GB or on− resistance of switches [33,34] will benefit from this technique.

Example 4.2:

A 20th order bandpass ladder, Fig.4.9, is simulated by the left− LUD circuit, Fig.4.10. Notice this schematic is drawn in a different way from those used earlier. The structure is very regular and the long unswitched capacitor op− amp chains have been broken by introducing two negative elements into the prototype. The response of the circuit is shown in Figs.11a,b. The component values for the circuit are listed in Table 4.2.

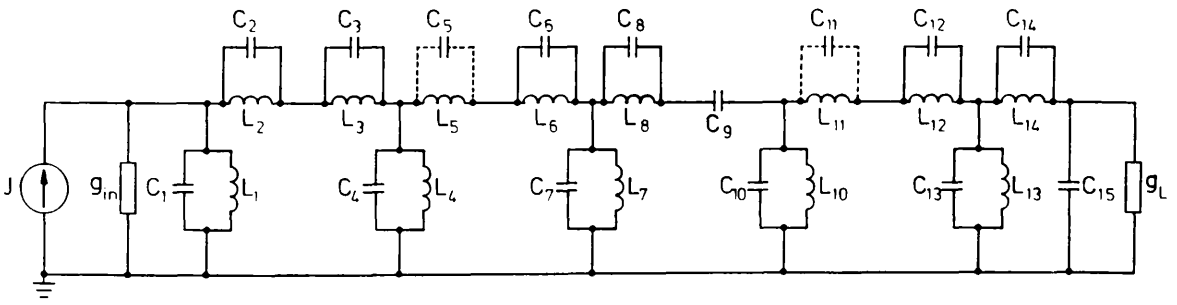


Fig.4.9 A 20th order ladder prototype

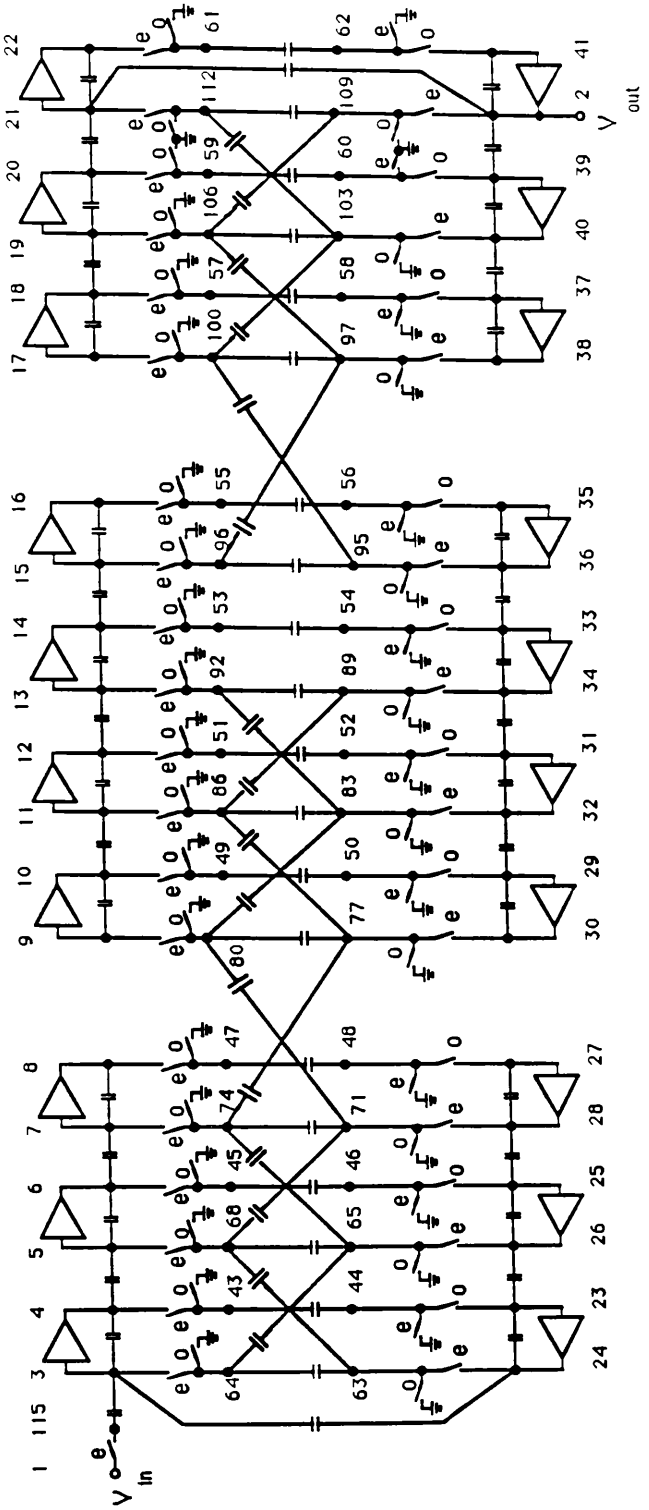


Fig.4.10 A 20th order left– LUD SC ladder

Normalised data for the RLC ladder

Gin	1.0	GL	0.51020				
C1	2.4200	L1	0.39346	C2	9.1911	L2	0.084942
C3	7.9789	L3	0.16361	C4	8.5633	L4	0.11936
C5	-0.001237	L5	2.5595	C6	1.4699	L6	0.99020
C7	10.453	L7	0.09341	C8	3.2603	L8	0.23531
C9	0.59787			C10	10.308	L10	0.095873
C11	-0.0016599	L11	1.9075	C12	3.1240	L12	0.42852
C13	7.6061	L13	0.14009	C14	3.04204	L14	0.23821
C15	0.51578						

lower passband edge	0.9075	upper passband edge	1.1065
lower stopband edge	0.877	upper stopband edge	1.132
passband ripple	< 0.03dB		
lower stopband atten.	> 95dB	upper stopband atten.	> 85dB

Component values for the SC ladder

NODE1	NODE2	VALUE	NODE1	NODE2	VALUE	NODE1	NODE2	VALUE	NODE1	NODE2	VALUE
4	3	24.38	4	5	10.37	6	5	9.095	6	7	40.92
8	7	39.09	10	9	47.51	10	11	6.576	12	11	25.31
12	13	4.401	14	13	5.049	14	15	4.493	16	15	43.78
18	17	46.54	18	19	7.795	20	19	14.39	20	21	4.113
22	21	2.712	24	23	16.32	26	23	18.05	26	25	28.15
28	25	18.62	28	27	30.77	30	29	28.71	32	29	9.335
32	31	22.63	34	31	9.969	34	33	34.52	36	33	3.243
36	35	31.09	38	37	32.58	40	37	15.40	40	39	28.45
2	39	6.541	2	41	30.91	43	44	1.000	45	46	1.000
47	48	1.000	49	50	1.000	51	52	1.000	53	54	1.000
55	56	1.000	57	58	1.000	59	60	1.000	61	62	1.000
63	64	3.764	65	64	4.341	63	68	1.670	65	68	3.558
71	68	1.000	65	74	6.805	71	74	13.62	77	74	1.000
71	80	1.000	77	80	10.02	83	80	2.349	77	86	1.000
83	86	5.139	89	86	2.533	83	92	1.000	89	92	1.852
95	96	10.65	97	96	1.000	95	100	1.000	97	100	10.70
103	100	4.128	97	106	1.463	103	106	4.049	109	106	1.000
103	112	1.243	109	112	1.000	24	3	2.993	2	21	1.383
115	3	1.000									

total capacitance	814 units	capacitance spread	47.5 units
capacitance unit	1 pF	clock frequency	800 kHz
number of capacitors	73	number of switches	81
number of opamps	20		
lower passband edge	10.1 kHz	upper passband edge	12.45 kHz
lower stopband edge	9.18 kHz	upper stopband edge	13.00 kHz

Table 4.3 Design data for a 20th order SC ladder

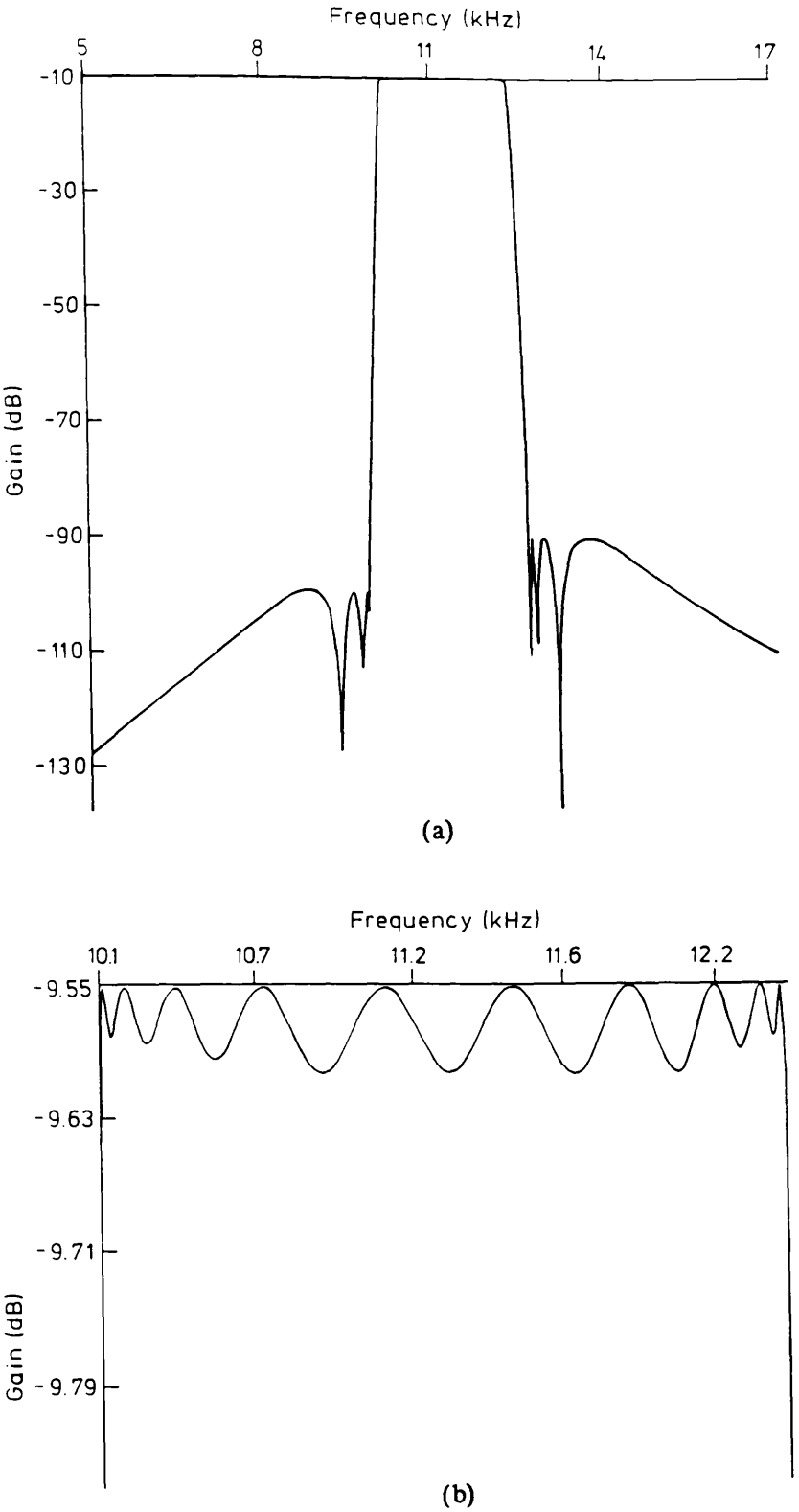


Fig.4.11 A 20th order bandpass function

(a) Overall response

(b) Passband response

4.6 DIGITAL BILINEAR–LDI LADDERS

4.6.1) Digital LU– LU ladders

Being without of delay free loops, the LUD approach is a strong candidate for digital filter design. The design procedures can be considered to be identical to those for left– LUD, UL– LU and LU– UL type SC circuits by using digital circuit realisations of Ψ and Φ given in Fig.4.12. However as digital circuit implementation is very flexible, there is some variation between circuit structures.

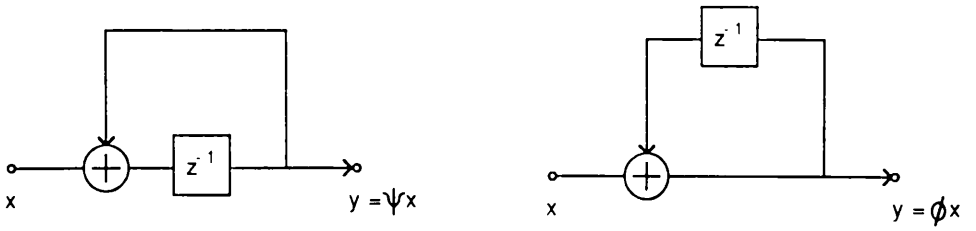


Fig.4.12 A pair of digital integrators

Multiplication is the most costly operation in digital implementation. It is desirable to minimise the number of multiplications and the number of multiplier coefficients. This can be done by inserting scaling matrices in the decomposition procedures which are applied to both left and right matrices.

As matrix **A** in (4.3) is always symmetric for passive networks, its LU decomposition can be expressed in a symmetric form

$$A = L_a \, D_a \, L_a^T \tag{4.23}$$

where D_a is a diagonal matrix, appropriately chosen to set every diagonal element of L_a to unity. Seperate L_a into diagonal and off– diagonal terms

$$L_a = I + L_{aoffd} \tag{4.24}$$

Also let **B** be LU factorised into

$$B = L_b \, D_b \, L_b^T \tag{4.25}$$

Then the so-called LU-LU type system follows

$$W = -(\Phi L_b D_b L_b^T + G) V - L_{aoffd} W + (1+z^{-1}) J \qquad (4.26a)$$

$$V = - L_{aoffd}^T V + \Psi D_a^{-1} W \qquad (4.26b)$$

Example 4.3:

The following example illustrates the design procedures for a standard and a scaled LUD digital circuit. For the passive network, Fig.4.13a, (3.1) becomes

$$\left\{ s \begin{bmatrix} 3.62 & 0.171 & & \\ 0.171 & 6.57 & 0.802 & \\ & 0.802 & 6.71 & 0.577 \\ & & 0.577 & 3.66 \end{bmatrix} + s^{-1} \begin{bmatrix} 0.242 & 0.242 & & \\ 0.242 & 0.503 & 0.261 & \\ & 0.261 & 0.535 & 0.273 \\ & & 0.273 & 0.273 \end{bmatrix} + \right.$$

$$\left. + \begin{bmatrix} 1 & & & \\ & 0 & & \\ & & 0 & \\ & & & 1 \end{bmatrix} \right\} V = \begin{bmatrix} J_{in} \\ 0 \\ 0 \\ 0 \end{bmatrix} \qquad (4.27)$$

where $V = [v_1, -v_2, v_3, -v_4]^T$. Let T=2 for simplicity. Perform the bilinear transformation $s = 2(1-z^{-1})/T(1+z^{-1})$ and follow the procedure from (4.8) and (4.26) using a LU decomposition. The relevant matrices are

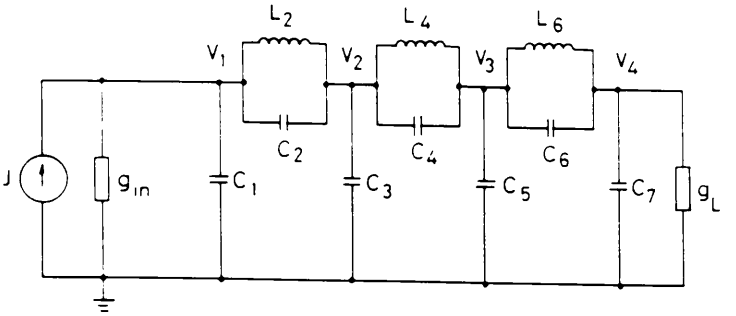
$$A = \begin{bmatrix} 1 & & & \\ 0.085 & 1 & & \\ & 0.151 & 1 & \\ & & 0.121 & 1 \end{bmatrix} \begin{bmatrix} 4.86 & & & \\ & 7.04 & & \\ & & 7.08 & \\ & & & 4.83 \end{bmatrix} \begin{bmatrix} 1 & 0.085 & & \\ & 1 & 0.151 & \\ & & 1 & 0.121 \\ & & & 1 \end{bmatrix}$$

(4.28a)

$$B = 4\Gamma = \begin{bmatrix} 1 & & & \\ 1 & 1 & & \\ & 1 & 1 & \\ & & & 1 \end{bmatrix} \begin{bmatrix} 0.968 & & & \\ & 1.06 & & \\ & & 1.09 & \end{bmatrix} \begin{bmatrix} 1 & 1 & & \\ & 1 & 1 & \\ & & 1 & 1 \end{bmatrix} \qquad (4.28b)$$

$$D = 2G = \begin{bmatrix} 2 & & & \\ & 0 & & \\ & & 0 & \\ & & & 2 \end{bmatrix} \qquad (4.28c)$$

The standard LU-LU realisation can now be drawn, Fig.4.14.



$g_{in} = 1S$ $g_L = 1S$
$c_1 = 3.450F$ $c_2 = 0.1717F$ $L_2 = 4.137H$
$c_3 = 5.601F$ $c_4 = 0.8016F$ $L_4 = 3.828H$
$c_5 = 5.328F$ $c_6 = 0.5722F$ $L_6 = 3.659H$
$c_7 = 3.082F$

Fig.4.13 A 7th order ladder prototype

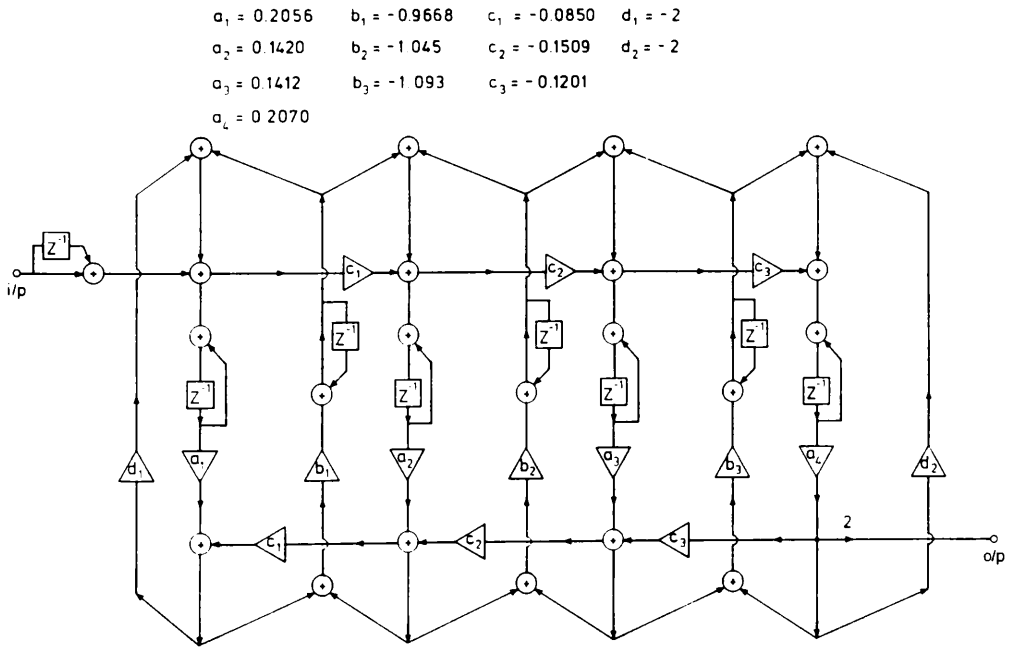


Fig.4.14 A digital LU– LU ladder

The digital realisation in Fig.4.14 has a canonical number of distinct multiplication coefficients, which equals the number of components in the prototype. The number of multiplications is not canonical since the entries of matrix $\mathbf{L}_{aoffd}$ is used twice for multiplication in (4.26). This will reduce the operation speed in sequential processors. However for implementation on array processors this is no longer a major problem as now the speed is mainly influenced by the degree of parallelism. Indeed the bottleneck for parallel processing is now the series multiplication chain along the horizontal line in Fig.4.14 as they *must* be processed serially in the direction of signal flow. The series multiplication chain problem bears an interesting relationship to the capacitor– opamp chain problem mentioned in Section 4.6, as they are both caused by the non– zero off– diagonal entries in the left hand side matrix.

4.6.2) Scaling technique to increase parallelism

The operation speed along the series multiplication chain in digital circuits can be increased by scaling all non– zero elements in $\mathbf{L}_a$ to their nearest powers of 2. The operation required to multiply a number by 2^{-k} is simply to shift it by k bits. It is also possible to scale all non– zero entries in $\mathbf{L}_a$ to ±1's, but this results in a very large coefficient spread. The scaling procedure can be performed in terms of matrix transformations. Let $\mathbf{S}$ be a diagonal constant matrix, pre– and post– multiply the matrices in equation (4.8) by $\mathbf{S}$. Let

$$\mathbf{A}_S = \mathbf{S}\,\mathbf{A}\,\mathbf{S} \qquad \mathbf{B}_S = \mathbf{S}\,\mathbf{B}\,\mathbf{S} \qquad \mathbf{D}_S = \mathbf{S}\,\mathbf{D}\,\mathbf{S}$$

$$\mathbf{V}_S = \mathbf{S}^{-1}\,\mathbf{V} \qquad \mathbf{J}_S = \mathbf{S}\,\mathbf{J} \tag{4.29}$$

A new system is obtained with a transfer function differing from that of system (4.8) only by a constant.

$$\left(\frac{1}{\Psi}\,\mathbf{A}_S + \Phi\mathbf{B}_S + \mathbf{D}_S \right) \mathbf{V}_S = (1+z)\mathbf{J}_S \tag{4.30}$$

Scaling is carried out so that $\mathbf{A}_S$ will decompose into

$$\mathbf{A}_S = \mathbf{L}_{as}\mathbf{D}_{as}\mathbf{L}_{as}^T \tag{4.31}$$

where every diagonal element of L_{as} is 1 and also the upper–diagonal elements are powers of 2. It can be verified that this procedure is possible provided A_S is tri–diagonal, which is always the case for a ladder structure.

Example 4.4:

To produce a scaled realisation, continue from Example 4.3 by choosing the scaling matrix S,

$$S = \text{diag}\,[0.603,\ 0.444,\ 0.735,\ 0.765] \tag{4.32}$$

Then for (4.29–4.31)

$$A_S = SAS = U_S D_S U_S^T = \begin{bmatrix} 1 & & & \\ 2^{-4} & 1 & & \\ & 2^{-2} & 1 & \\ & & 2^{-3} & 1 \end{bmatrix} \begin{bmatrix} 1.77 & & & \\ & 1.39 & & \\ & & 3.82 & \\ & & & 2.82 \end{bmatrix} \begin{bmatrix} 1 & 2^{-4} & & \\ & 1 & 2^{-2} & \\ & & 1 & 2^{-3} \\ & & & 1 \end{bmatrix}$$

$$B_S = SBS = \begin{bmatrix} 0.603 & & & \\ & 0.444 & & \\ & & 0.735 & \\ & & & 0.765 \end{bmatrix} \begin{bmatrix} 1 & & & \\ 1 & 1 & & \\ & 1 & 1 & \\ & & 1 & \end{bmatrix} \begin{bmatrix} 0.968 & & & \\ & 1.06 & & \\ & & 1.09 & \end{bmatrix} \begin{bmatrix} 1 & 1 & & \\ & 1 & 1 & \\ & & 1 & 1 \end{bmatrix} \begin{bmatrix} 0.603 & & & \\ & 0.444 & & \\ & & 0.735 & \\ & & & 0.765 \end{bmatrix}$$

$$G_S = SDS = \begin{bmatrix} 0.603 & & & \\ & 0.444 & & \\ & & 0.735 & \\ & & & 0.765 \end{bmatrix} \begin{bmatrix} 2 & & & \\ & 0 & & \\ & & 0 & \\ & & & 2 \end{bmatrix} \begin{bmatrix} 0.603 & & & \\ & 0.444 & & \\ & & 0.735 & \\ & & & 0.765 \end{bmatrix}$$

(4.33)

The scaled realisation by topological decomposition of B_S shown in Fig.4.15 follows.

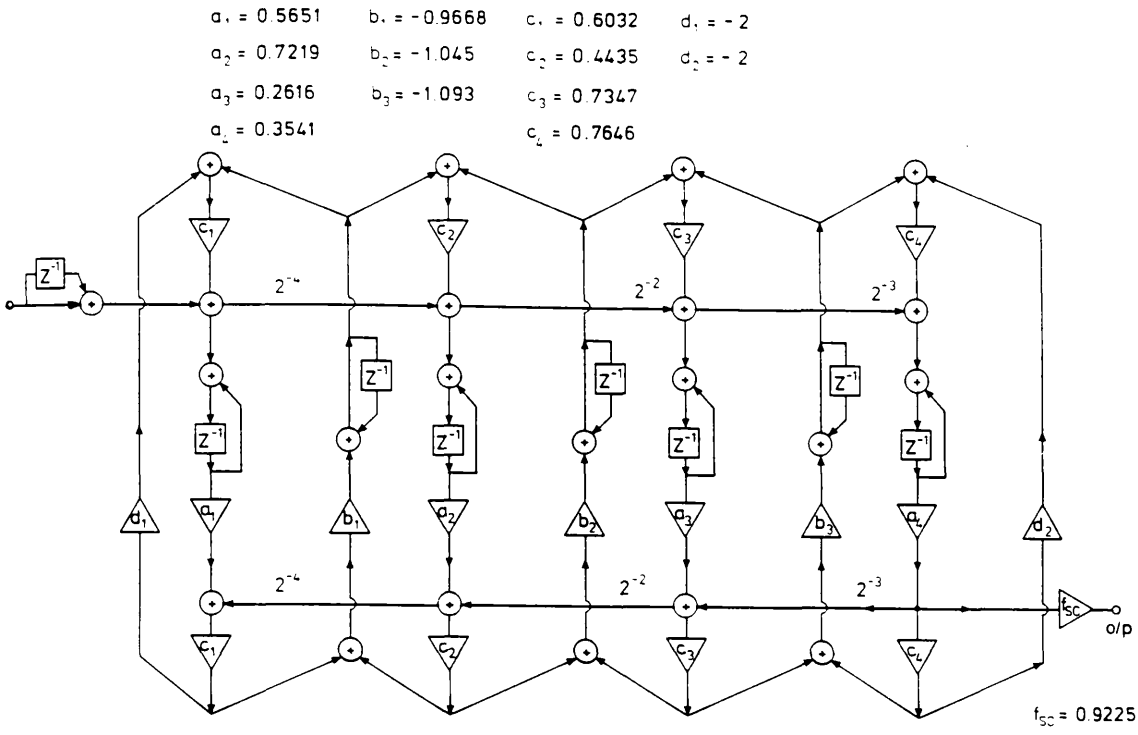


Fig.4.15 A scaled digital LU− LU ladder

Example 4.5:

To illustrate the influence of coefficience quantisation, a wave, a LU− LU and a biquad digital filter are designed with the same frequency response shown in Fig.4.16. LU− LU and wave design still use the same RLC circuit in Fig.4.12 as the prototype but sampling frequency is changed to 32000Hz. It is assumed that floating point storage of coefficients is used. All the coefficients are truncated to the nearest smaller number.

The detailed passband response for 8 bits implementation given in Fig.4.17 shows a quite serious overall distortion for the biquad, whereas all other responses are almost ideal. When the wordlength is reduced to 4 bits, the overall filter response for wave and LUD derived typies are retained with reasonable accuracy while the biquad response variation is dramatic, Fig.4.18.

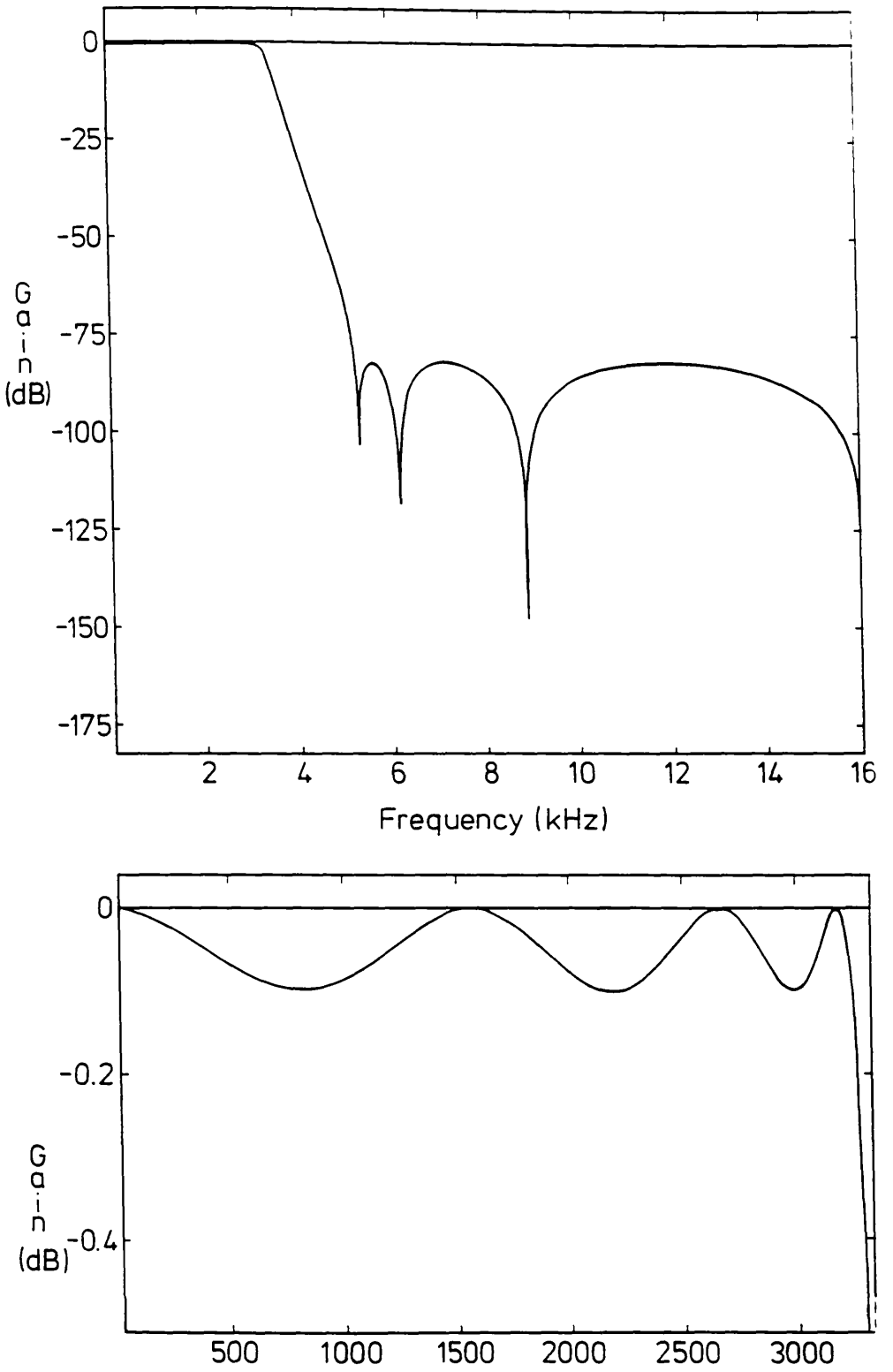


Fig.4.16 A 7th order lowpass function

(a) Overall response

(b) Passband response

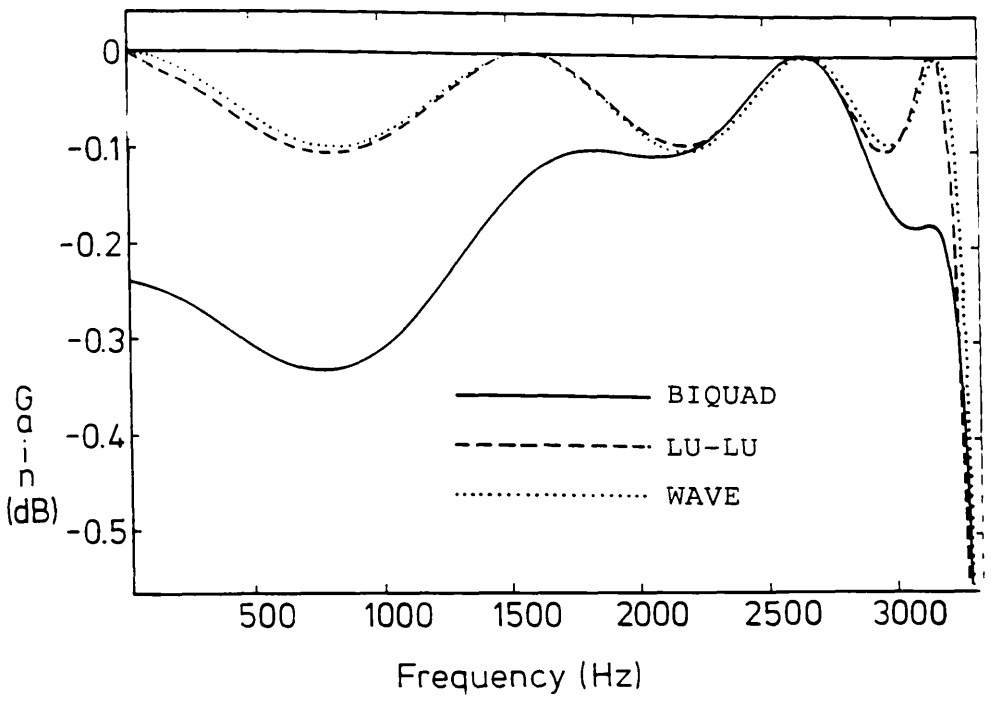


Fig.4.17 Passband responses with 8– bit digital realisation

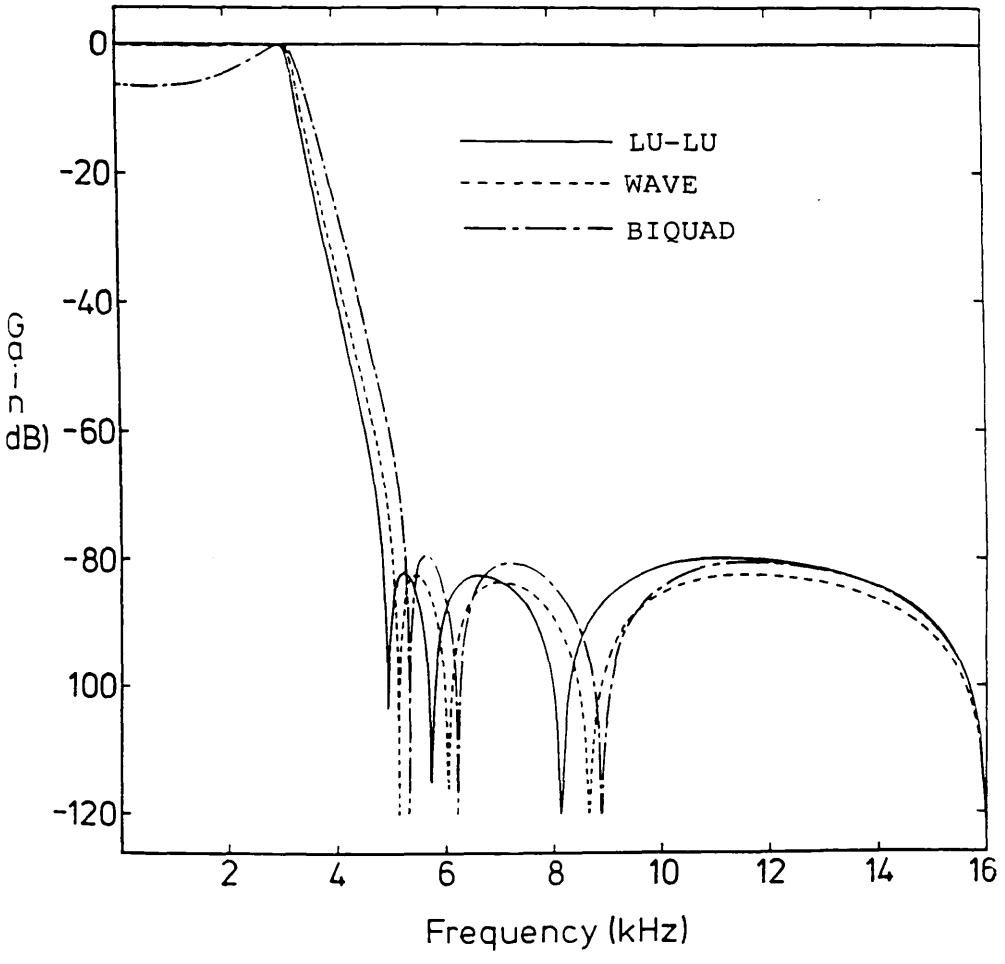


Fig.4.18 Overall responses with 4– bit digital realisation

4.7 STATISTICAL STUDIES

A number of discrete ladder structures have been covered in this chapter, including both existing and novel ones. Properly selecting a suitable structure for a particular specification is very important in practical design. It is difficult to set up a general rule for this purpose. Some observations have been made for SC designs from our experience as follows.

For most SC networks, such as modem or codec filters, specifications are of lowpass or bandpass types. For lowpass designs the Right–LUD method (which is identical to the leapfrog one [51] in the lowpass case) appears the best candidate since it can provide a canonical solution with low spread and low sensitivity. It is more complicated to reach a decision about bandpass designs as the performances of all kinds of circuits vary dramatically according to the relative bandwidth. This can be seen from some statistical studies.

As the passband behaviour is of most intrest to filter designers, define two indices for system sensitivity and dynamic range, which are the average measures of $s(\omega)$ and $d(\omega)$, defined by (4.11), in the passband

$$S = \frac{1}{\text{width of passband}} \int_{\text{passband}} s(\omega)\,d\omega \qquad (4.34a)$$

$$D = \frac{1}{\text{width of passband}} \int_{\text{passband}} d(\omega)\,d\omega \qquad (4.34b)$$

Normally the chip area required for fabrication of a SC filter is measured by

$$T_C = \sum_{\text{all capacitors}} c_i \qquad (4.34c)$$

but to reflect the influence of capacitance spread the following index will also be used

$$C = \left[\sum_{\text{all capacitors}} c_i^2 \right]^{1/2} \qquad (4.34d)$$

A overall performance index of an SC filter can be defined by

$$P = \frac{C\,S}{D} \qquad (4.34e)$$

For these indices, it is desirable to have lower S, T_c, C and P (the lower limit is 0). The maximum opamp output will always be assumed to have been scaled to 1, so that D will always be a positive number less than 1. It is desirable to have D close to 1, which means that all the opamps have equal output swing in the passband.

For a bandpass filter the relative bandwidth is defined by (let ω^+ and ω^- be the upper and lower edge frequency respectively),

$$RBW = (\omega^+ - \omega^-)/\omega_m \qquad \omega_m = (\omega^+\omega^-)^{1/2} \qquad (4.35)$$

It is known that RBW has a great influence on the system performance. For 6th order elliptic designs, let the passband ripple be fixed as 0.1dB, stopband attenuation 50 dB and f_m/f_s ratio 25 ($2\pi f_m = \omega_m$, f_s is the sampling frequency). Computer simulations of S, T_c, D and P are performed against relative bandwidth. The sweeped results are shown in Fig.4.19– 4.22. A similar study has been carried out for 10th order designs, Fig.4.23– 4.26. From these results it can be seen that the left– decomposition designs have very good total capacitance property in the narrow band range but that the biquad method takes over at around RBW= 1. For the sensitivity index S all the ladder designs are much better than the biquad method over the whole range. The dynamic range index D of the biquad method is discountinuous at some points. This may be due to the fact that E– type and F– type biquads are selected according to Q– factor and discontinuity of internal nodal voltages may take place when the design is switched from E– type to F– type or vice versa. Another reason is that the pairing of biquadratic sections is carried out to achieve minimum total capacitance, which does not take into consideration voltage levels.

Comparing the overall performance indices indicates that the left– LUD

method is the best candidate for narrow band design and the biquad method is best for wide band design. It is found that for wide band designs the most significant factor causing the deterioration of all designs is the lower band finite zeroes, which approach zero when RBW increases. Realisations of these zeroes require large capacitance spread. The deterioration process can be slowed down if the lower band finite zeroes are replaced at the origin. A 8th order sweep is carried out with the form of transfer function shown in Fig.4.27, where three zeroes are placed at origin. The fixed parameter are $f_m/f_s = 25$, passband ripple$= 0.1$, (passband width)/(stopband width)$= 1.15$. The results are shown in Fig.4.28$-$4.31 and in this case the left$-$LUD appears to have best performance in every respect.

Another two less common cases are bandstop and highpass designs. For bandstop design the cascade biquads method is still the best candidate. Although it is not clear why ladders cannot provide a good solution (even by the twintor circuit discussed in Chapter 5). It seems that it is even not necessary to search for a better solution other than cascade biquads circuits, they are just good enough regarding sensitivity, spread and dynamic range. This is probably due to the fact that the transfer function of a section of biquad is naturally a notch type function. For highpass design the biquad and leapfrog (with modulators discussed in Chapter 5) methods are recommended. It seems that other ladder methods can also be employed for highpass designs with some modifications but this requires further investigation.

4.8 SUMMARY

In this chapter, matrix methods have been extended to SC and digital filter design. The basic principle is the same as for the continuous domain systems. Techniques have been developed to meet some special requirements for discrete systems, such as efficient realisation of exact s$-$to$-$z mapped systems and to increase the parallelism in the circuit structures.

Since SC circuits are fully integrated and cannot be tuned after fabrication, it is particularily important to design circuits with low sensitivity to errors in the element values. For this reason, ladder structures have found wide industrial application. Detailed comparison have been made between different types of designs and the advantages of adopting ladder structures for high quality systems have been demonstrated.

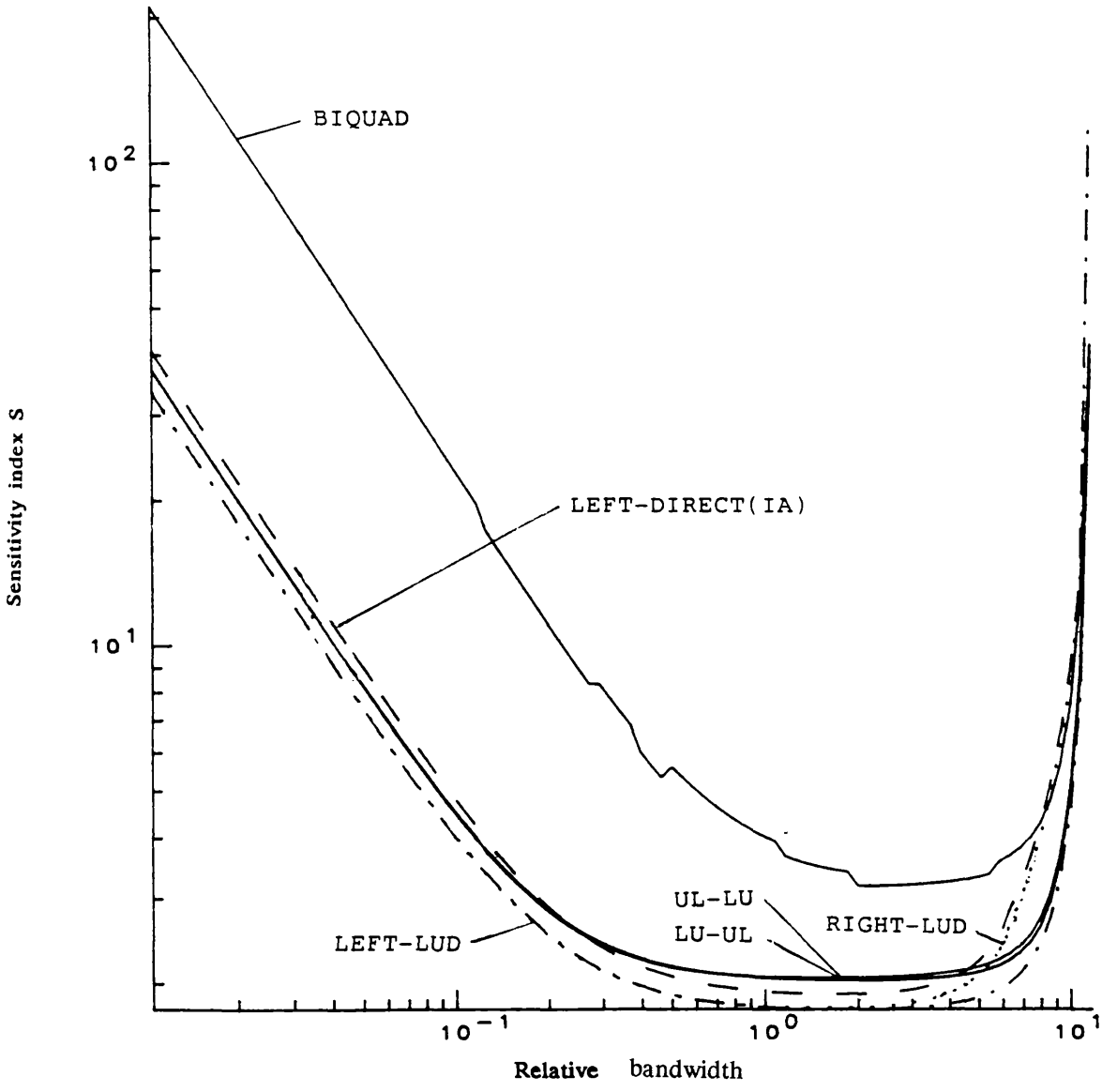


Fig.4.19 Sensitivity index for 6th order elliptic designs

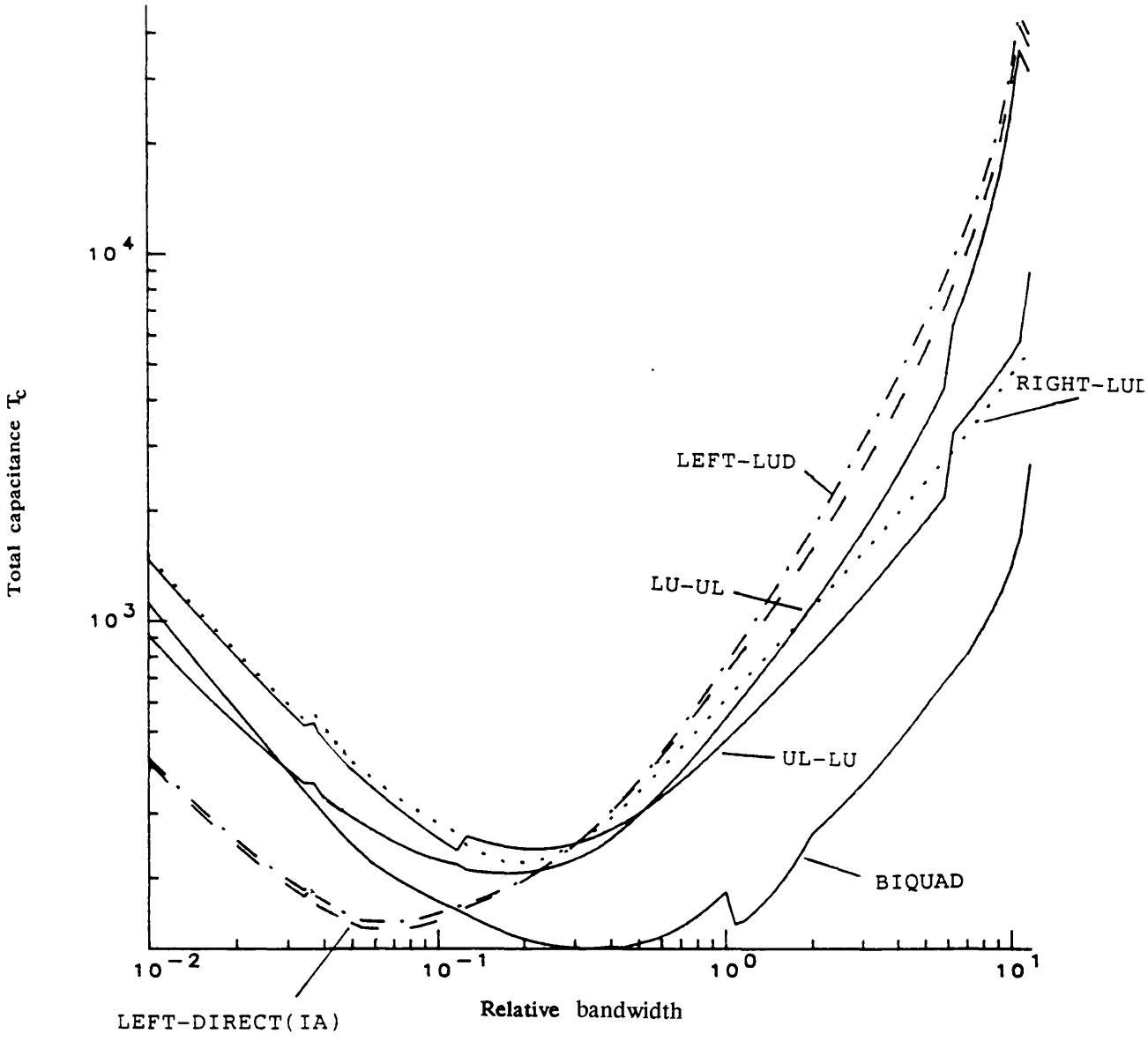


Fig.4.20 Total capacitance for 6th order elliptic designs

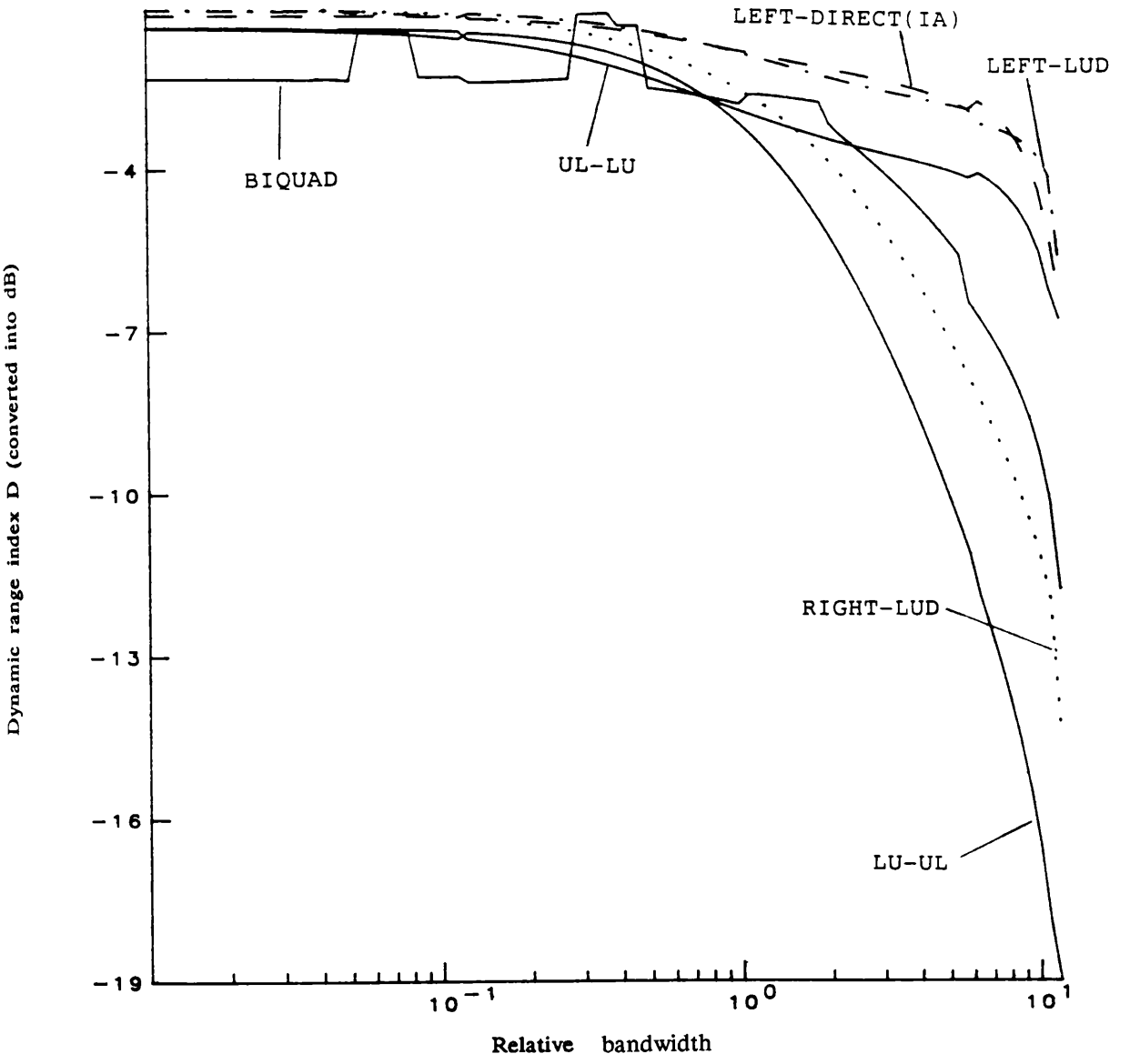


Fig.4.21 Dynamic range index for 6th order elliptic designs

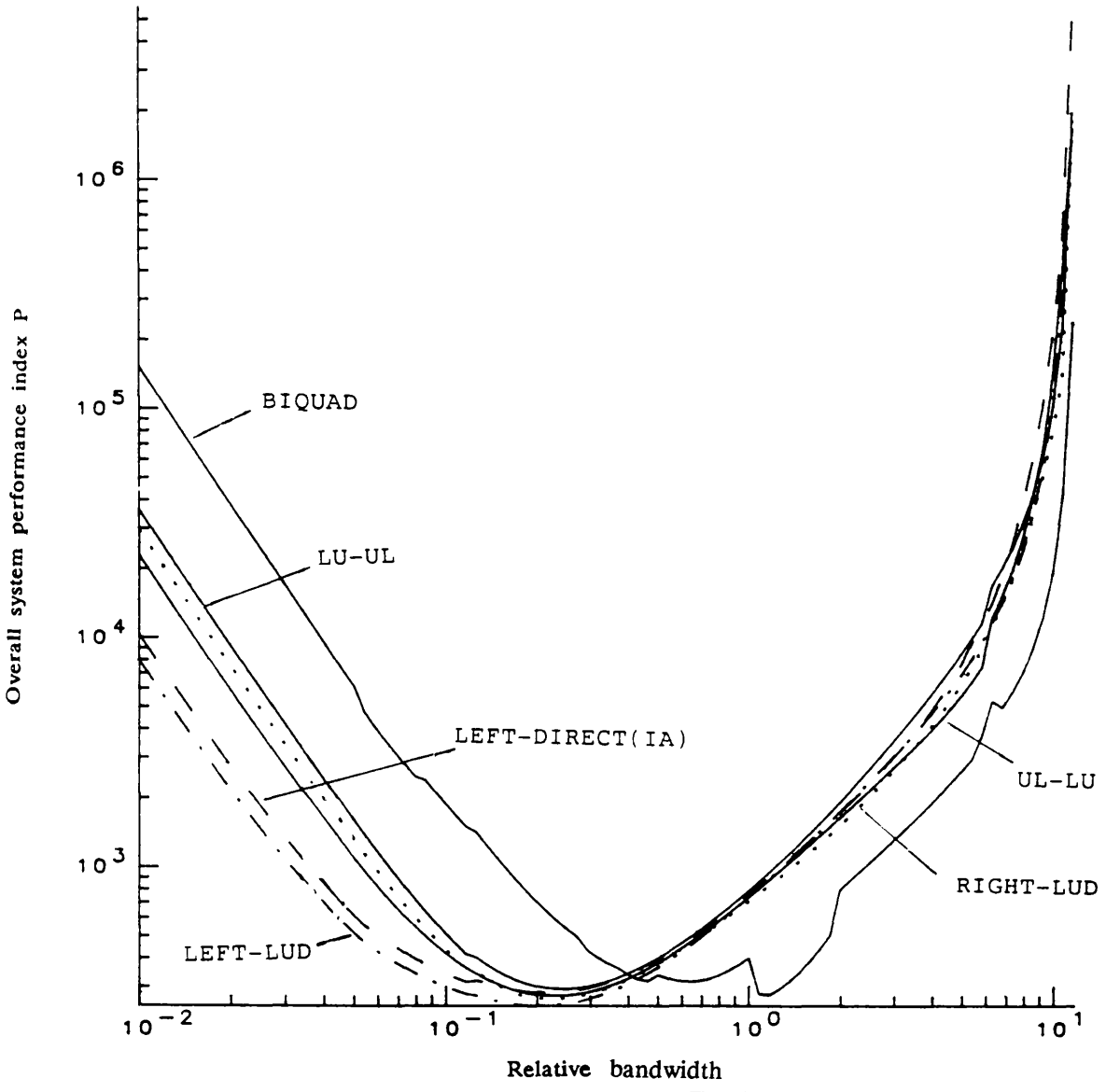


Fig.4.22 Overall performance index for 6th order elliptic designs

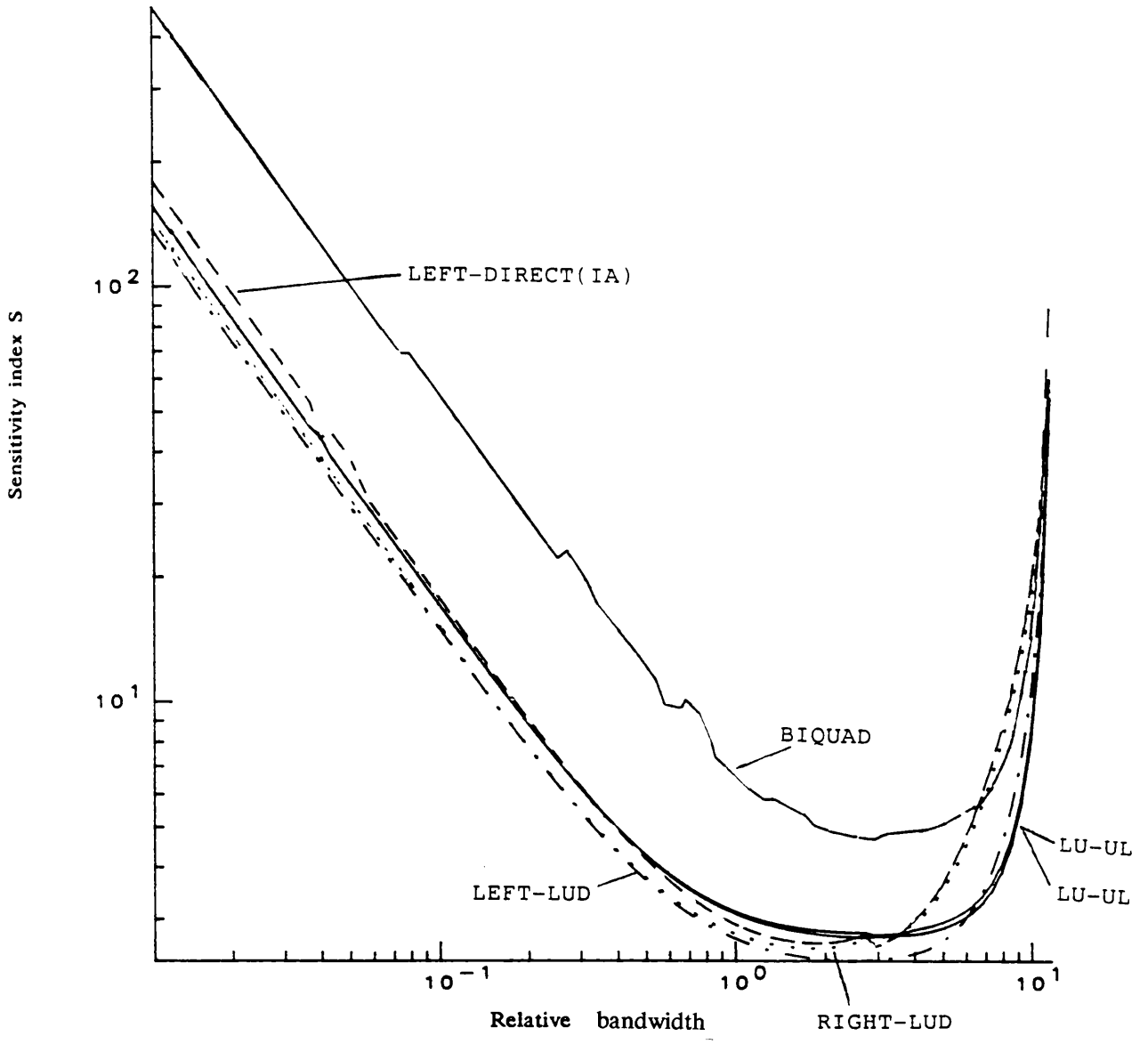


Fig.4.23 Sensitivity index for 10th order elliptic designs

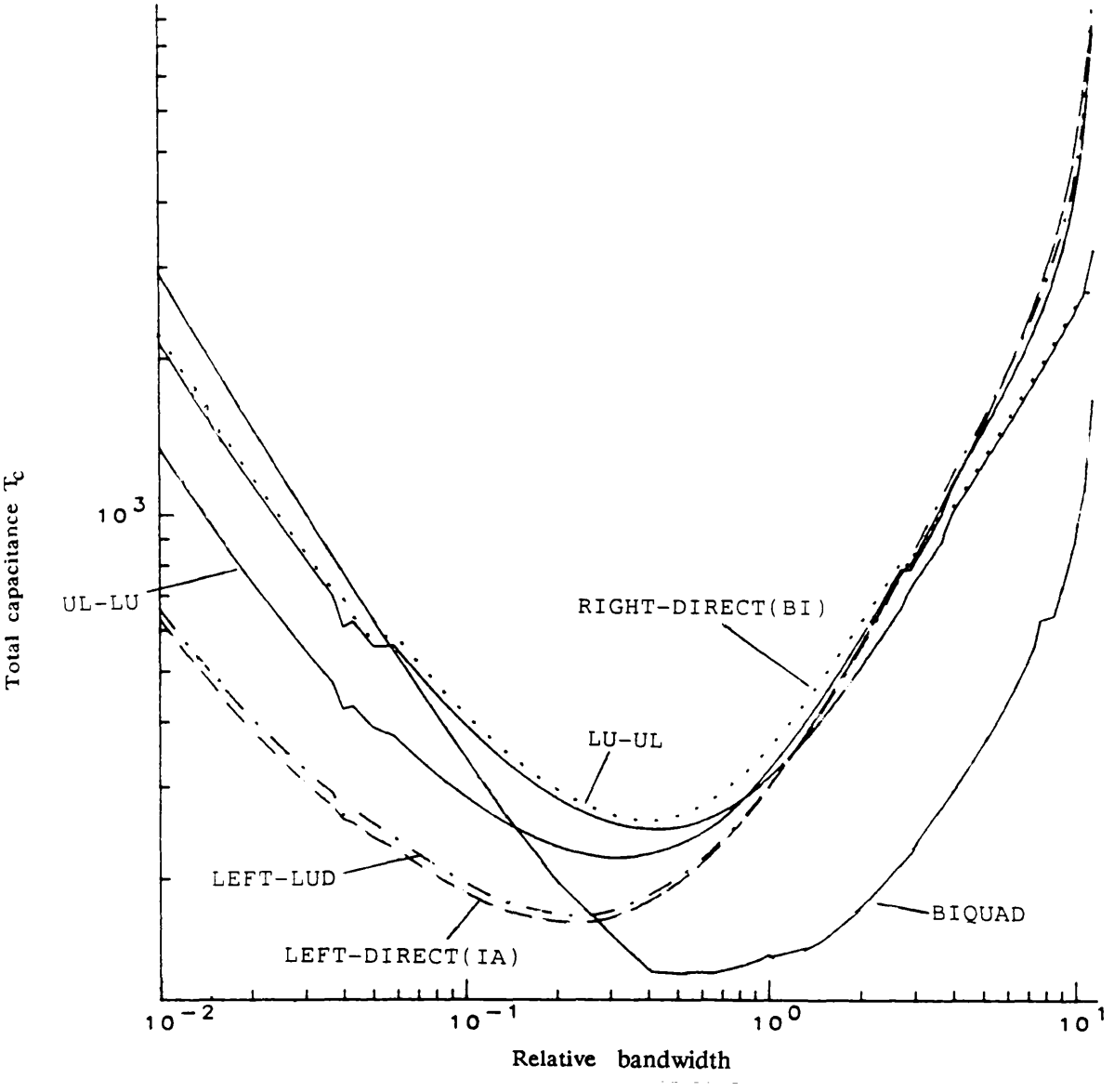


Fig.4.24 Total capacitance for 10th order elliptic designs

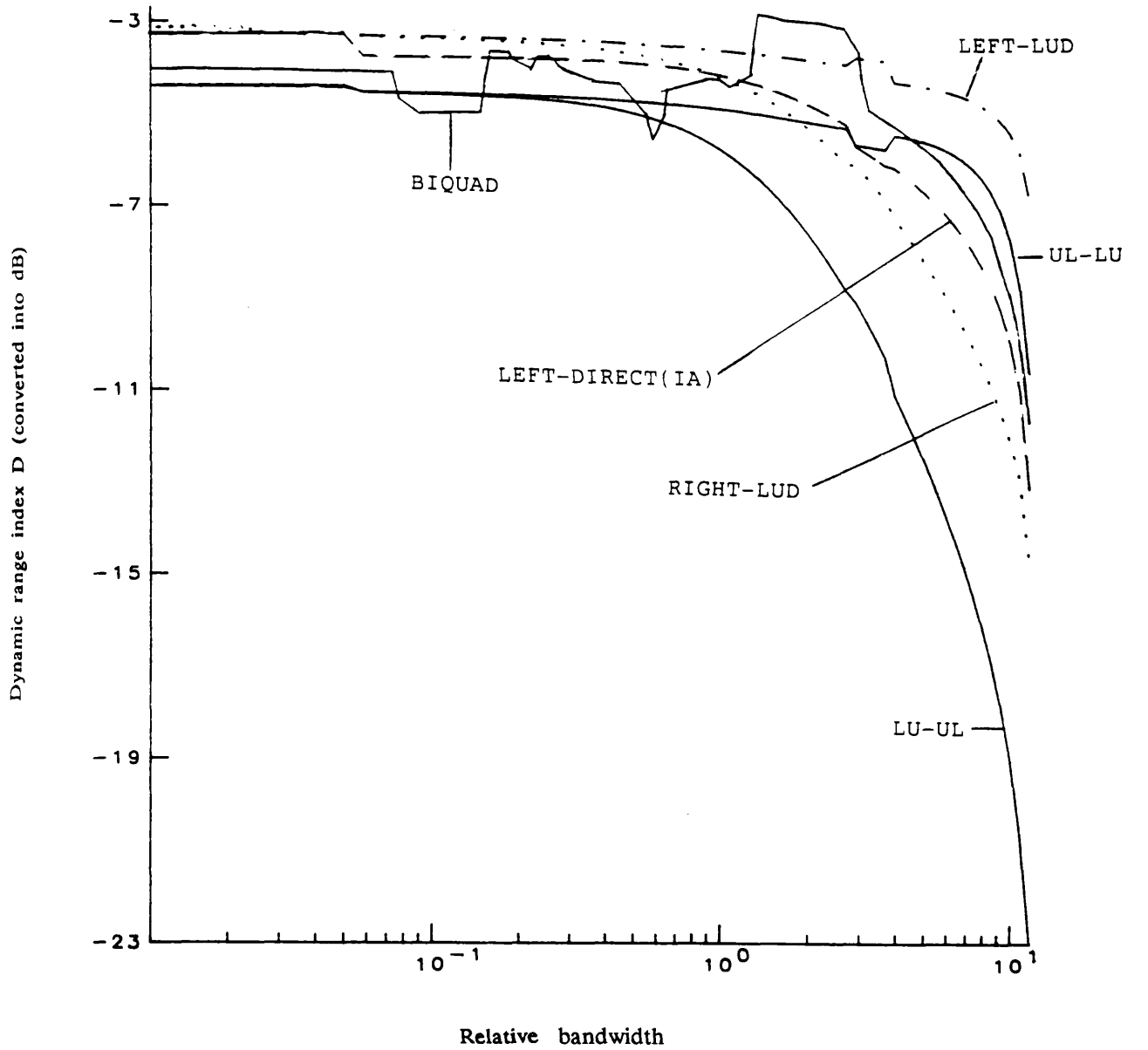


Fig.4.25 Dynamic range index for 10th order elliptic designs

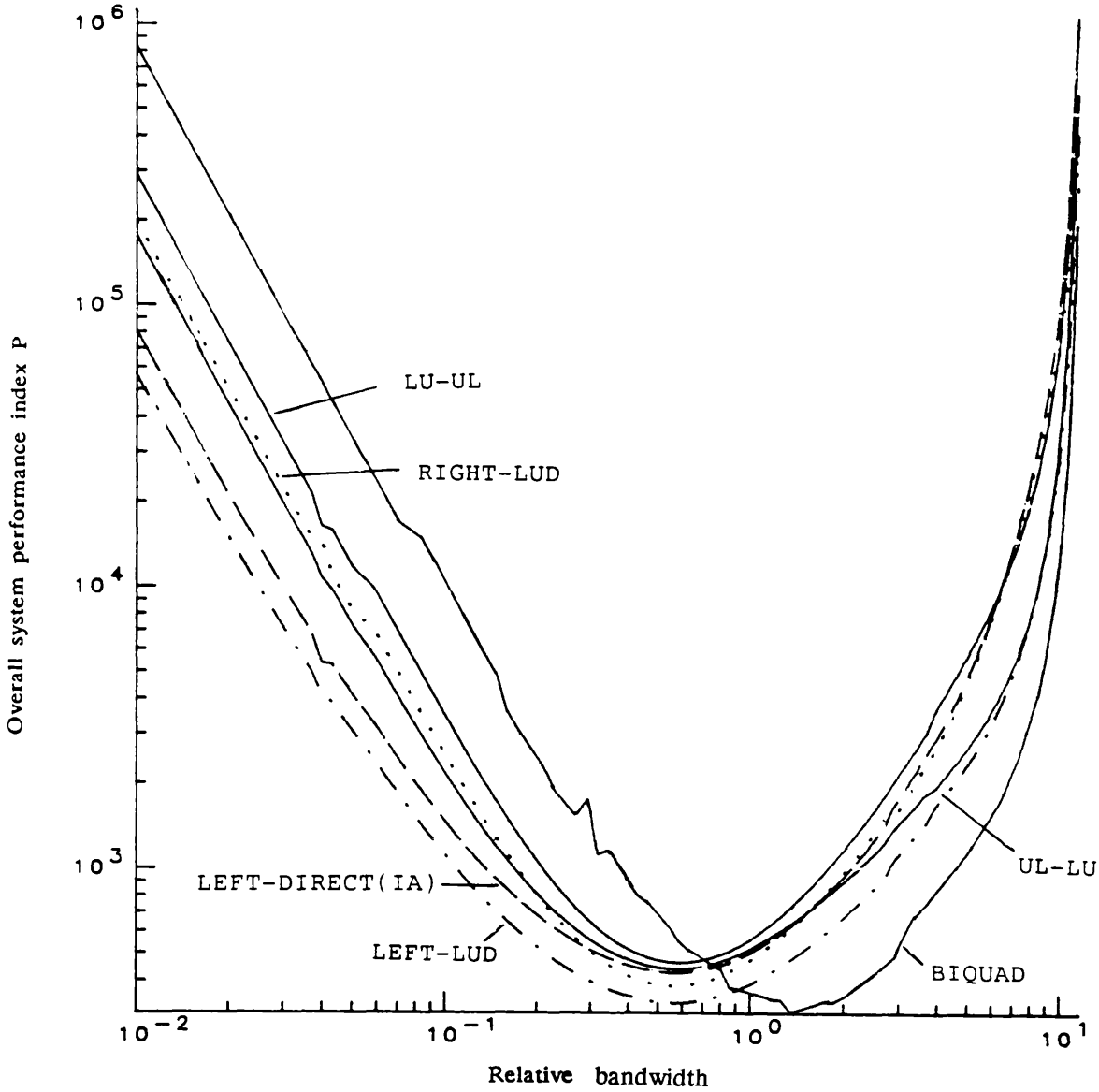


Fig.4.26 Overall performance index for 10th order elliptic designs

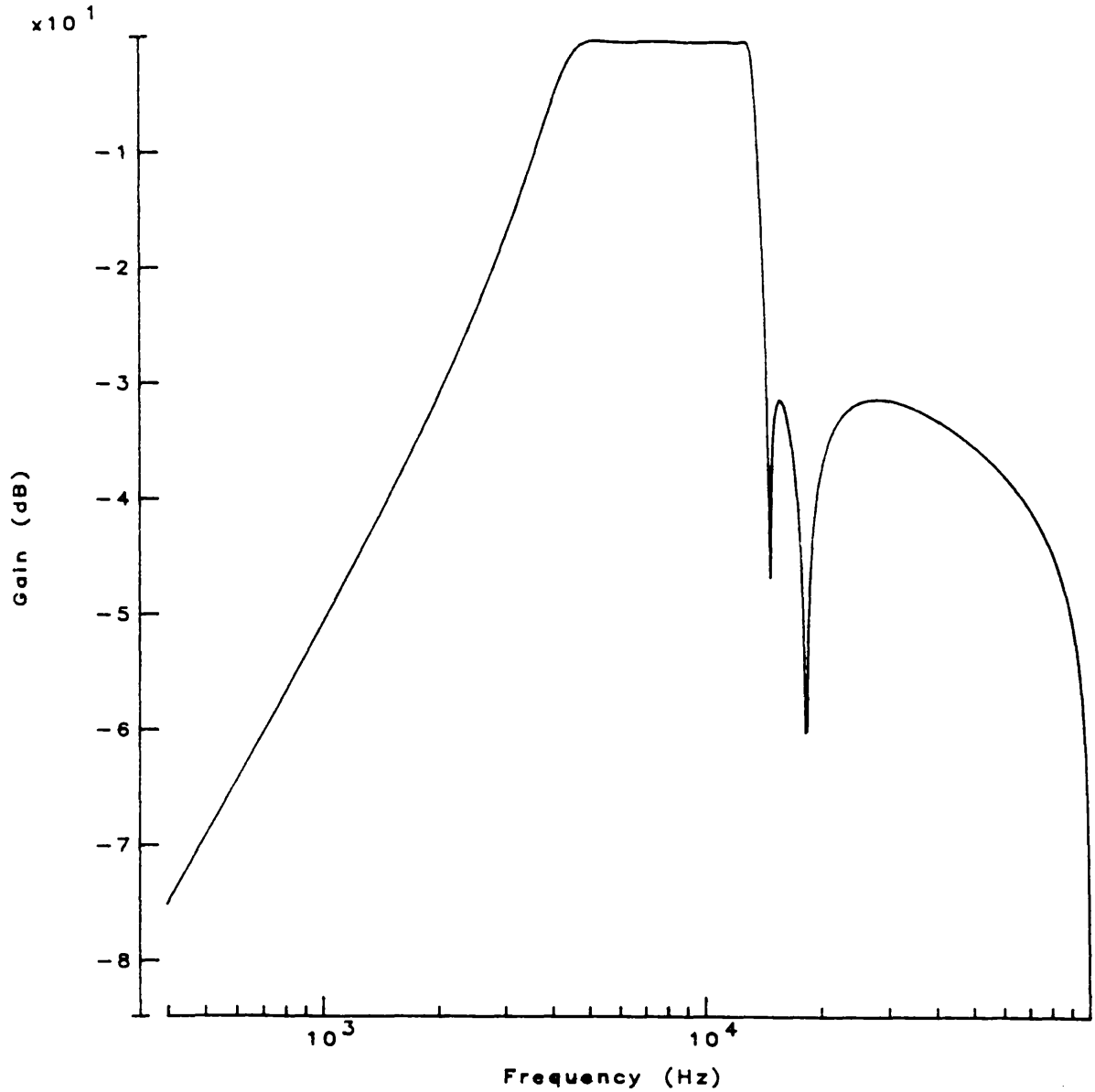


Fig.4.27 A 8th order bandpass function with three zeroes at origin

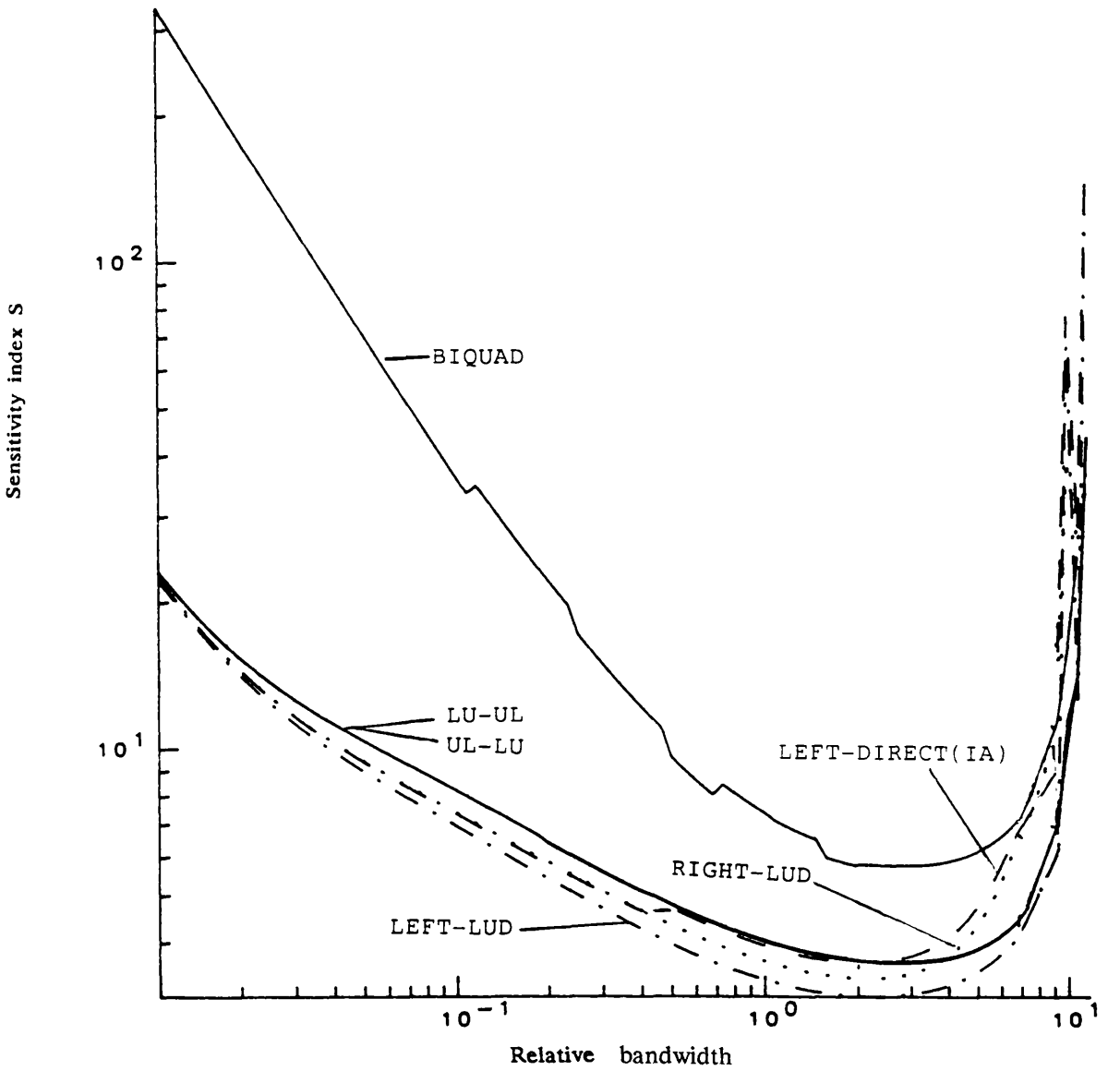


Fig.4.28 Sensitivity index for 8th order designs

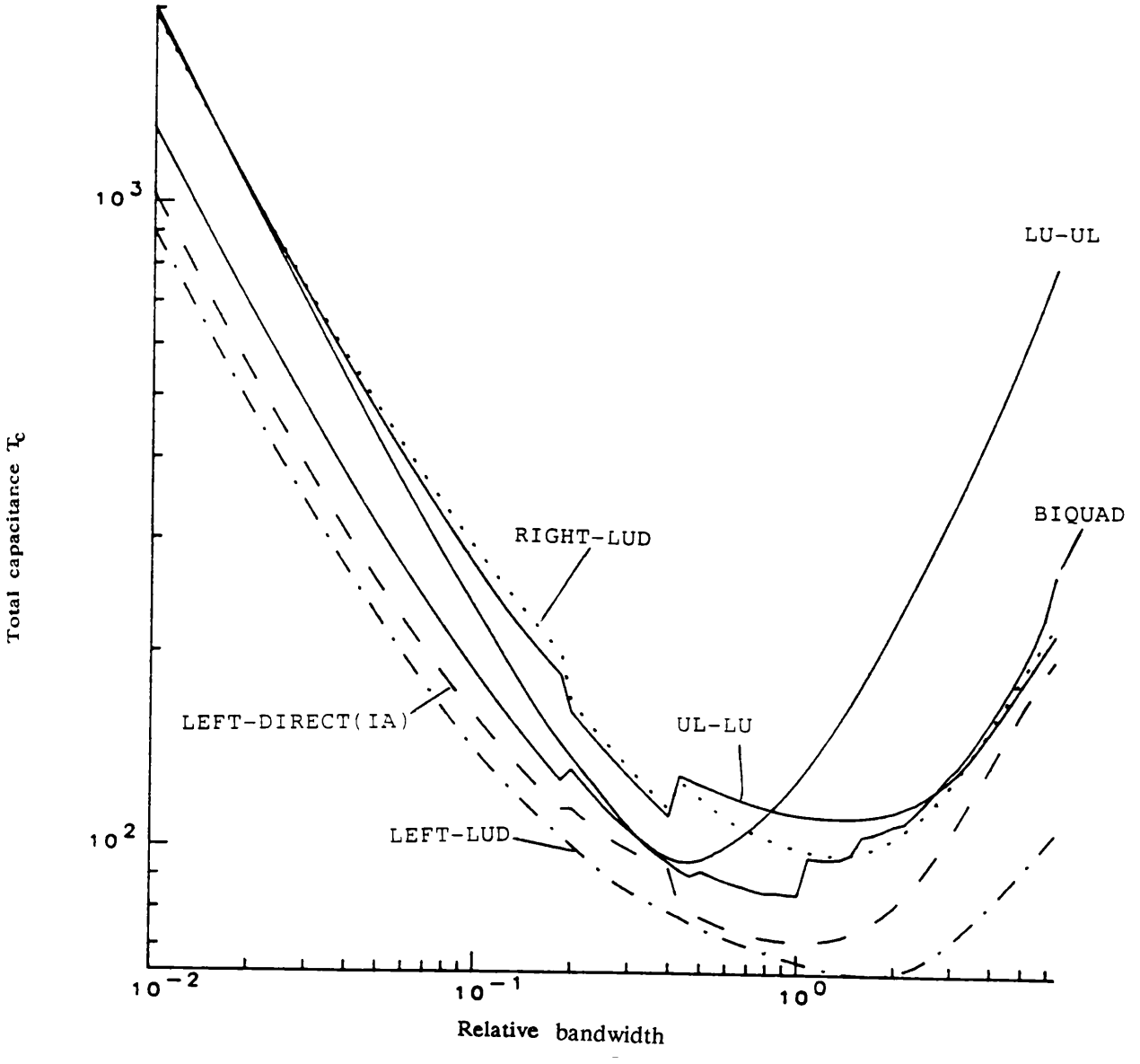


Fig.4.29 Total capacitance for 8th order designs

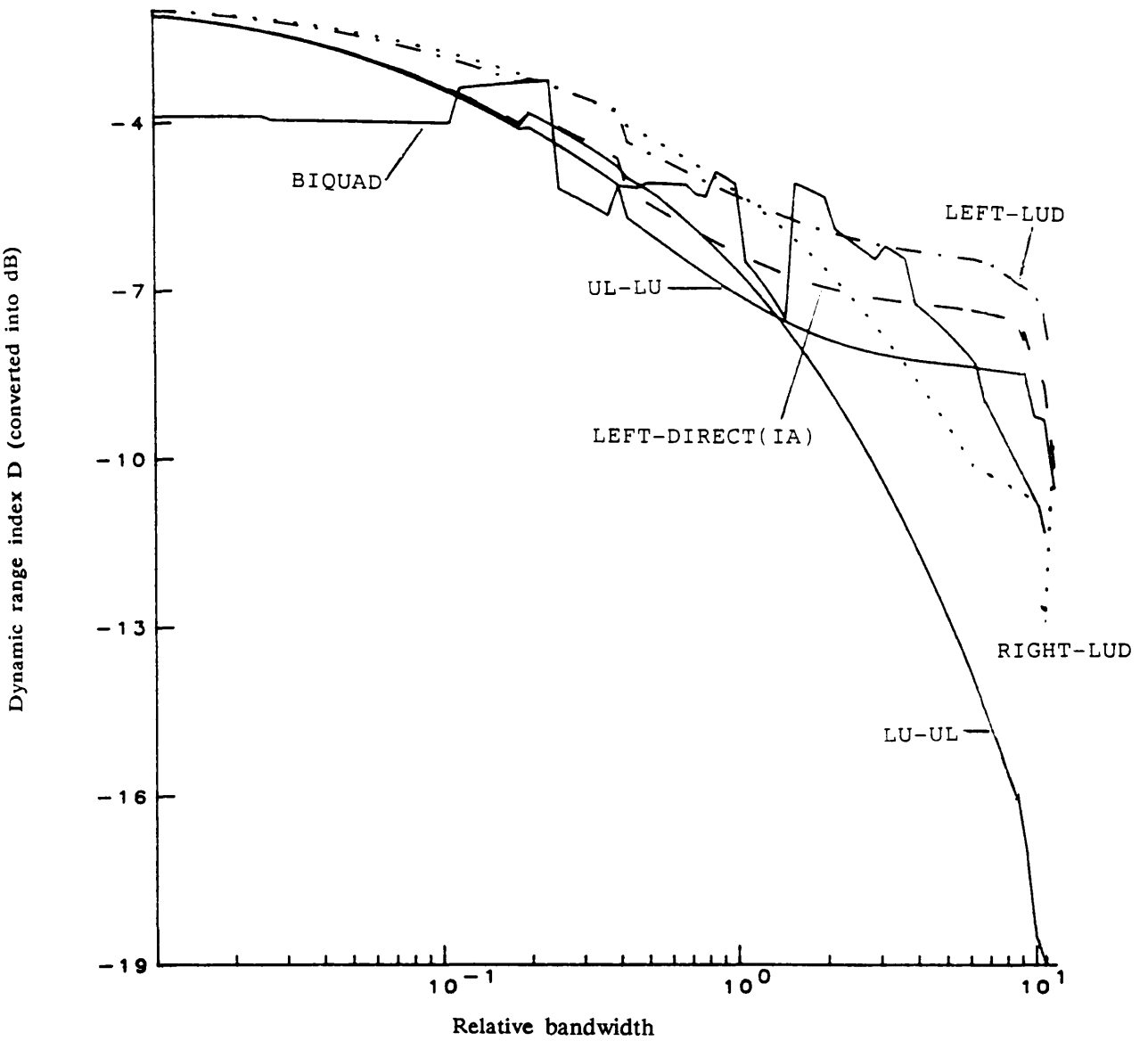


Fig.4.30 Dynamic range index for 8th order designs

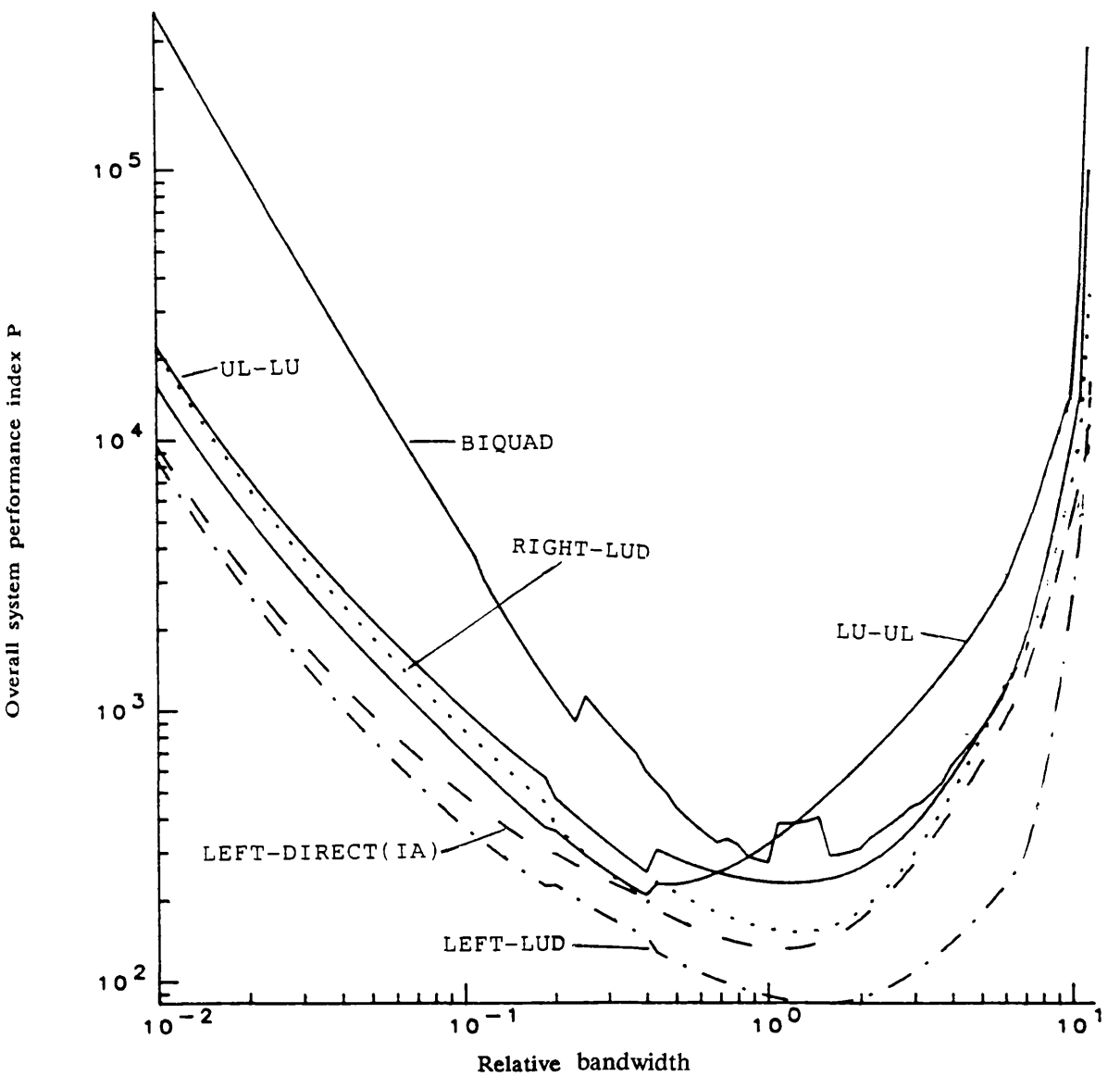


Fig.4.31 Overall performance index for 8th order designs

CHAPTER 5

FREQUENCY TRANSFORMATION METHODS FOR DISCRETE LADDER DESIGN

5.1 INTRODUCTION

The standard bilinear–LDI methods introduced in Chapter 4 for discrete ladder design can be applied directly to lowpass and band–pass but not to high–pass and band–stop designs. The difficulty is that for these latter cases the transfer function is not of zero value at $z=-1$ (corresponding to $s = \infty$ in continuous domain). However the input fuctions of (4.8a) and (4.8c) reach zero at $z=-1$. This implies that the transfer function from $(1+z)J$ or $(1+z^{-1})J$ to the output must be infinite at $z=-1$ to facilitate cancellation, which inevitably results in an unstable system. This problem can be avoided by canonical design in Section 4.3.4 or by the frequency transformation method discussed in this chapter.

The basic idea of frequency transformation methods is to replace the standard LDI operator pairs by a set of operator pairs which are adapted to the type of the filter specifications. The input stage can then be made to realise a transmission zero in the stopband, so that no stability problem will arise.

For digital realisation these transformation methods also have the advantage of preserving the circuit structure; a useful property for programmable applications. In bandpass and bandstop cases the cost of additions in a transformed realisation is lower than that in a direct realisation and when the ratio between sampling and centre frequencies is selectable the cost of multiplications can also be greatly reduced.

A new type of second order building–block called a twintor (TWinned INTegratOR) is introduced for realising bandstop SC operators. The circuit uses two signal channels to directly realise the basic bandstop operators without term cancellations, and also reduces the required opamp operation speed. Either single–input or differential–input integrators are allowed, giving flexibility for fabrication.

Based on the transformation of a lowpass function into other types of functions, the following discussion is restricted to the realisations of systems with geometrically symmetric frequency response.

5.2 FREQUENCY TRANSFORMATION METHODS FOR DIGITAL LADDER DESIGN

Again starting from a normalised lowpass reference passive ladder with nodal description

$$(s C + s^{-1} \Gamma + G) V = J \qquad (5.1)$$

It is well known [2] that in the continuous time domain a lowpass function can be transformed into a bandpass, bandstop or a highpass function by frequency transformations, Fig.5.1. It will be shown in this chapter that these transformations can be used to derive a family of operators for different applications.

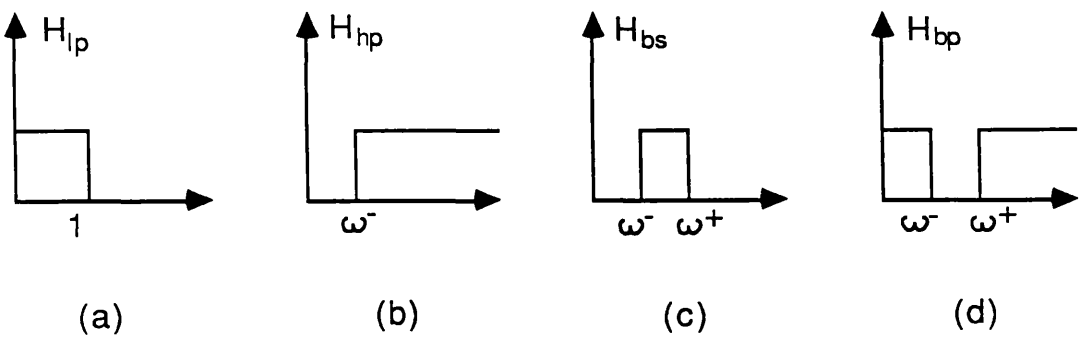


Fig.5.1 Illustration of frequency transformations

(a) A lowpass reference function

(b) A highpass function

(c) A bandstop function

(d) A bandpass function

5.2.1) Lowpass to highpass transformation

In the continuous time domain lowpass to highpass transformation is carried out by

$$s \longrightarrow \frac{\omega^-}{s} \tag{5.2}$$

where ω^- is the lower passband edge. After bilinear transformation, it can be seen that substitution of the reference system (5.1) according to the relationship

$$s \longrightarrow \frac{2}{\omega^- T} \frac{1-z^{-1}}{1+z^{-1}} \tag{5.3}$$

will transform the lowpass reference into the desired highpass system. Compared with the denormalised lowpass system obtained from (5.1) according to (ω^+ is the upper passband edge)

$$s \longrightarrow \frac{\omega^+ T}{2} \frac{1+z^{-1}}{1-z^{-1}} \tag{5.4}$$

It can be seen that apart from a scaling factor, the highpass system can be derived from a lowpass one by simply substituting $z^{-1} \rightarrow -z^{-1}$. Equivalently, highpass systems can be obtained by substituting the standard LDI operators in a lowpass one by a pair of highpass operators, Table 5.1,

$$\Phi_{hp} = 1/(1+z^{-1}) \tag{5.5a}$$

$$\Psi_{hp} = -z^{-1}/(1+z^{-1}) \tag{5.5b}$$

and substituting the input stage in the lowpass system, $1+z^{-1}$, by $1-z^{-1}$. A notch is shifted to the origin and the instability problem is avoided.

An alternative approach to realising $z^{-1} \rightarrow -z^{-1}$ can be derived by using the modulation method [59]. If a time domain series f(n) is modulated to given $f^*(n)$ according to

$$f^*(n) = \begin{cases} f(n) & n \text{ even} \quad (5.6a) \\ -f(n) & n \text{ odd} \quad (5.6b) \end{cases}$$

then their z– transformations are related by

$$Z^*(z) = Z\{ f^*(n) \} = \sum_{n}^{\infty} (-1)^n f(n) z^{-n} = Z\{ f(n) \}\Big|_{z \to -z} = Z(-z)$$

(5.7)

The modulation function of (5,6) can be realised by the circuit shown in Fig.5.2a with two switches and an inverter. If modulators are inserted in both input and output ends of a lowpass filter, Fig.5.2b, the output of the first modulator is $V_{in}(-z)$ and the output of the second modulator is $H(-z)V_{in}(z)$. Hence a highpass function is obtained.

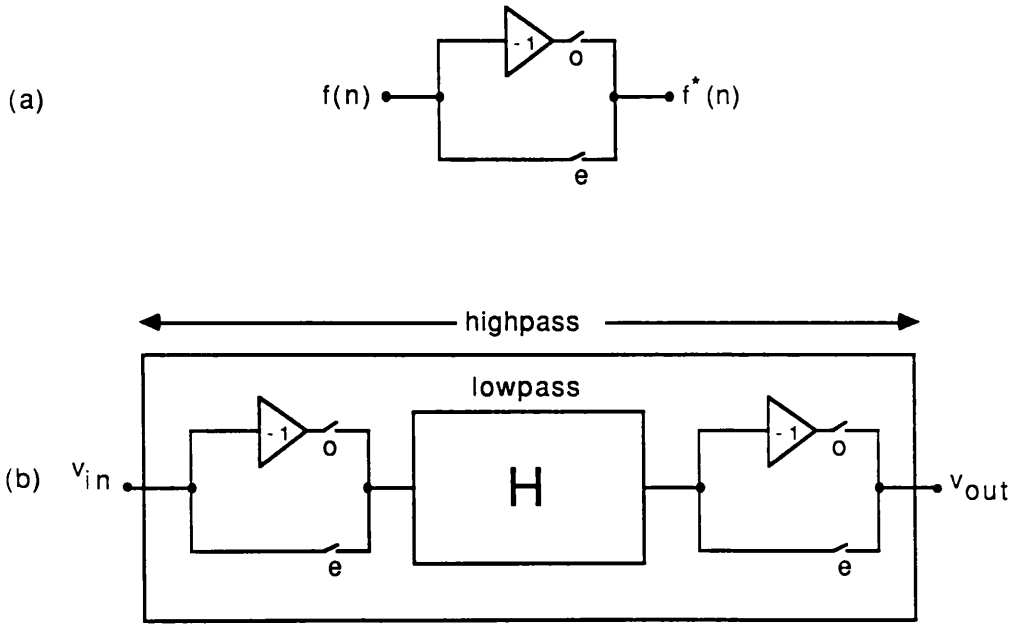


Fig.5.2 Modulator and highpass digital filter realisation

(a) A modulator

(b) Highpass digital filter realisation using a lowpass system and two modulators

5.2.2) Lowpass to bandstop transformation

In the continuous time domain a symmetric bandstop function can be derived from a normalised lowpass one by transformation [2],

$$s \longrightarrow a^{-1} \left(\frac{s}{\omega_m} + \frac{\omega_m}{s} \right)^{-1} \qquad (5.8a)$$

$$\text{with} \qquad a = \frac{\omega_m}{\omega^+ - \omega^-} \qquad \omega_m = \sqrt{\omega^+ \omega^-} \qquad (5.8b)$$

Substitute (5.8) into (5.1) and perform the bilinear transformtion $s = 2(1-z^{-1})/T(1+z^{-1})$,

$$\left\{ a^{-1} \left(\frac{2}{\omega_m T} \frac{1-z^{-1}}{1+z^{-1}} + \frac{\omega_m T}{2} \frac{1+z^{-1}}{1-z^{-1}} \right)^{-1} C + a \left(\frac{2}{\omega_m T} \frac{1-z^{-1}}{1+z^{-1}} + \frac{\omega_m T}{2} \frac{1+z^{-1}}{1-z^{-1}} \right) \Gamma + G \right\} V = J \qquad (5.9)$$

Multiply through (5.9) by the coefficient of Γ and rearrange to give

$$\left(\Psi_{bs}^{-1} A + \Phi_{bs} B + D \right) = \left(\Psi^{-1} + 2 \right) J \qquad (5.10a)$$

or

$$\left(\Phi_{bs}^{-1} A + \Psi_{bs} B + D \right) = \left(-\Phi^{-1} + 2 \right) J \qquad (5.10b)$$

$$\Phi_{bs} = (1-\beta z^{-1})/(1-z^{-2}) \qquad (5.11a)$$

$$\Psi_{bs} = (z^{-2}-\beta z^{-1})/(1-z^{-2}) \qquad (5.11b)$$

$$A = \alpha^{-1} C + \alpha \Gamma \pm G \qquad (5.11c)$$

$$B = 4 \alpha \Gamma \qquad (5.11d)$$

$$D = 2 G \qquad (5.11e)$$

$$\mu = \omega_m T/2 \qquad (5.11f)$$

$$\alpha = a (\mu^{-1} + \mu) \qquad (5.11g)$$

$$\beta = (\mu^{-1} - \mu)/(\mu^{-1} + \mu) \qquad (5.11h)$$

where the sign of **G** in (5.11c) is positive for (5.10a) and negative for (5.10b). Both the equations in (5.10) have the same appearance as those in (4.8) and so they can be realised in the same way, with only Φ and Ψ replaced by Φ_{bs} and Ψ_{bs}. The digital realisations of Φ_{bs} and Ψ_{bs} are given in Table 5.1. A bandstop LU−LU design based on (5.10a) is shown in Fig.5.3, where $\Theta_{bs} = -\Phi_{bs}^{-1} + 2$, using the 5th order RLC ladder of Fig.3.7 as the prototype. It can be verified that the zeros of Θ_{bs} now lie exactly in the middle of stopband and the instability problem mentioned above is thus avoided. The design data is given in Table.5.2. Notice that in this example the system (5.10a) has been scaled by 0.5 to set the termination entries in **D** to 1, saving two multipliers. The passband ranges are from 0 to 3000 Hz and from 4000 to 16000 Hz. The sampling frequency is 32000 Hz. The frequency response is shown in Fig.5.4.

5.2.3) Lowpass to bandpass transformation

Similarly a symmetric bandpass function can be derived from a normalised lowpass one by transformation [2],

$$s \longrightarrow a \left(\frac{s}{\omega_m} + \frac{\omega_m}{s} \right) \qquad (5.12a)$$

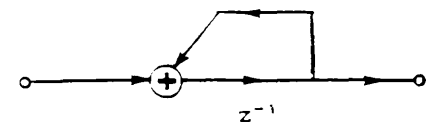
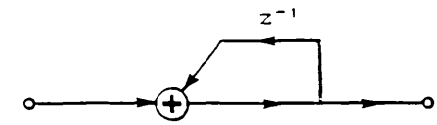
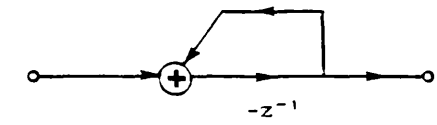
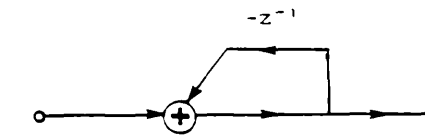
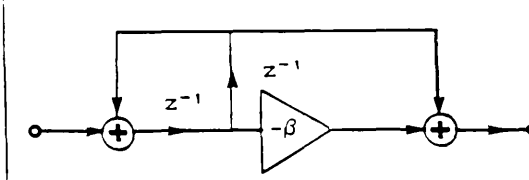
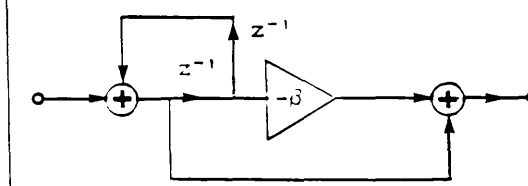
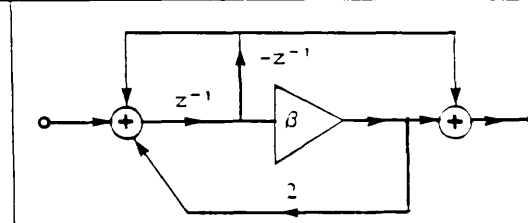
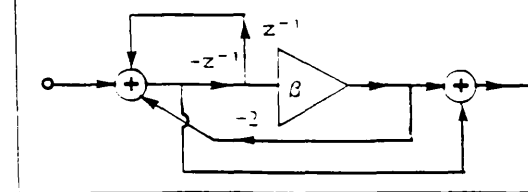
standard and lowpass	$\frac{z^{-1}}{1-z^{-1}}$	φ	
	$\frac{1}{1-z^{-1}}$	Φ	
highpass	$\frac{-z^{-1}}{1+z^{-1}}$	φ_{hp}	
	$\frac{1}{1+z^{-1}}$	Φ_{hp}	
bandstop	$\frac{z^{-2}-\beta z^{-1}}{1-z^{-2}}$	φ_{bs}	
	$\frac{1-\beta z^{-1}}{1-z^{-2}}$	Φ_{bs}	
bandpass	$\frac{\beta z^{-1}-z^{-2}}{1-2\beta z^{-1}+z^{-2}}$	φ_{bp}	
	$\frac{1-\beta z^{-1}}{1-2\beta z^{-1}+z^{-2}}$	Φ_{bp}	

Table 5.1 Various types of frequency operators

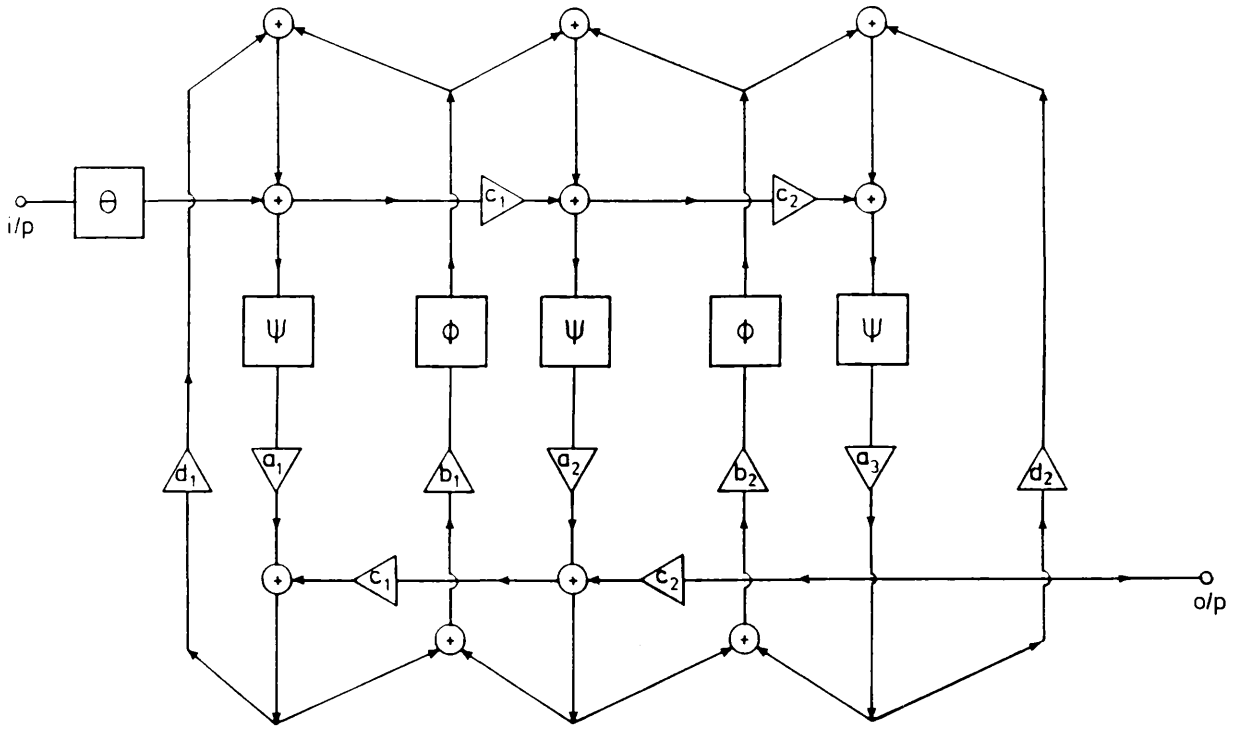


Fig.5.3 A LU–LU digital realisation

Reference Ladder (normalised values)		
g_i = 1	g_L = 1	
C_1 = 1.05298	L_2 = 1.24796	C_2 = 0.11789
C_3 = 1.69738	L_4 = 1.02002	C_4 = 0.33388
C_5 = 0.88240		
Digital simulation		
a_1 = 0.21618	a_2 = 0.17976	a_3 = 0.94811
b_1 = 16.2715	b_2 = 19.908	
c_1 = 0.88070	c_2 = 0.89761	
d_1 = 1	d_2 = 1	β = 0.77675

Table 5.2 Parameters for the bandstop filter

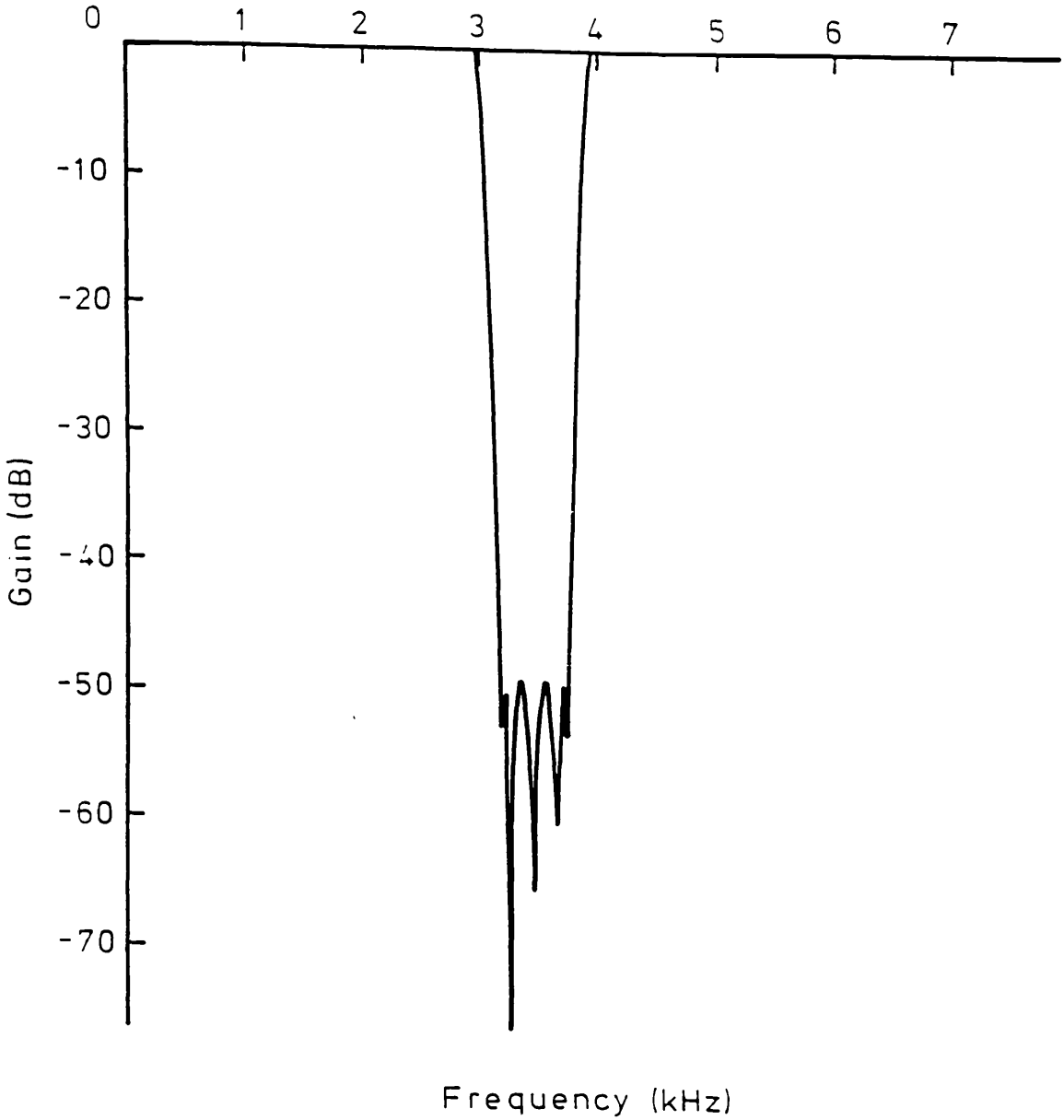


Fig.5.4 A 10th order elliptic bandstop response

$$\text{with} \qquad a = \frac{\omega_m}{\omega^+ - \omega^-} \qquad \omega_m = \sqrt{\omega^+\omega^-} \tag{5.12b}$$

Substitute (5.12) into (5.1) and perform the bilinear transformation $s = 2(1-z^{-1})/T(1+z^{-1})$,

$$\left\{ a\left(\frac{2}{\omega_m T}\,\frac{1-z^{-1}}{1+z^{-1}} + \frac{\omega_m T}{2}\,\frac{1+z^{-1}}{1-z^{-1}}\right) C + a^{-1}\left(\frac{2}{\omega_m T}\,\frac{1-z^{-1}}{1+z^{-1}} + \frac{\omega_m T}{2}\,\frac{1+z^{-1}}{1-z^{-1}}\right)^{-1}\Gamma + G \right\} V = J \tag{5.13}$$

(5.13) can be again written as

$$\left(\Psi_{bp}^{-1} A + \Phi_{bp} B + D \right) = (\Psi^{-1}+2)\, J \tag{5.14a}$$

or

$$\left(\Phi_{bp}^{-1} A + \Psi_{bp} B + D \right) = (-\Phi^{-1}+2)\, J \tag{5.14b}$$

$$\Phi_{bp} = (1-\beta z^{-1})/(1-2\beta z^{-1}+z^{-2}) \tag{5.15a}$$

$$\Psi_{bp} = (\beta z^{-1}-z^{-2})/(1-2\beta z^{-1}+z^{-2}) \tag{5.15b}$$

$$A = \alpha\, C + \alpha^{-1}\, \Gamma \pm G \tag{5.15c}$$

$$B = 4\, \alpha^{-1}\, \Gamma \tag{5.15d}$$

$$D = 2\, G \tag{5.15e}$$

$$\mu = \omega_m T/2 \qquad (5.15f)$$

$$\alpha = a\ (\ \mu^{-1} + \mu\ ) \qquad (5.15g)$$

$$\beta = (\mu^{-1} - \mu)/(\mu^{-1} + \mu) \qquad (5.15h)$$

where the sign of G in (5.15c) is positive for (5.14a) and negative for (5.14b). Again (5.14) can be realised by the same scheme, Fig.5.3 with Φ and Ψ replaced by Φ_{bp} and Ψ_{bp}, Table 5.1. It can even be verified that in this approach the number of additions is much smaller than required in the direct simulation of a bandpass prototype.

5.2.4) Discussions

It is interesting to note some common properties shared by the block operators given in the Table 5.1: (a) $\Phi_* - \Psi_* = 1$, (b) the poles of Φ_* and Ψ_* are on the unit circle and at the middle of passband, (c) the zeros of the input stages are in the middle of the stopband on the unit circle; where "$*$" applies to all four types.

If it is possible to adjust the product of ω_m and T, β may be scaled to a special number to faciliate easy multiplication. For example, if β is set to $0.75 = 2^{-2} + 2^{-3}$, then it requires only two shifts and one addition to multiply a signal by β. As β is repeately used , considerable saving of hardware cost and operation time can be gained.

5.3 FREQUENCY TRANSFORMATION METHODS FOR SC DESIGN

The SC realisations of frequency transformed circuit follow the same principle as outlined in the last section for digital ones. The realisation of different SC operators requires more careful consideration since SC circuits are not as flexible as digital ones, being constrained to be stray–capacitance insensitive.

5.3.1) Lowpass to highpass transformation

The highpass operators given in (5.5) can be realised by SC differentiators. However they are stray sensitive and produce a high level of noise. A more efficient method is to use modulators as mentioned above, requiring two inverters at both input and output stages.

5.3.2) Lowpass to bandstop transformation

The frequency dependent operators Ψ and Φ given by (5.11) can certainly be realised by SC biquads [39]. However, notice that for the special form of the denominators of Φ and Ψ, where z^{-1} term is missing, undesirable term cancellations must be used. An interesting alternative is using a new TWINTOR second order strays–insensitive biquad scheme, Fig.5.5a.

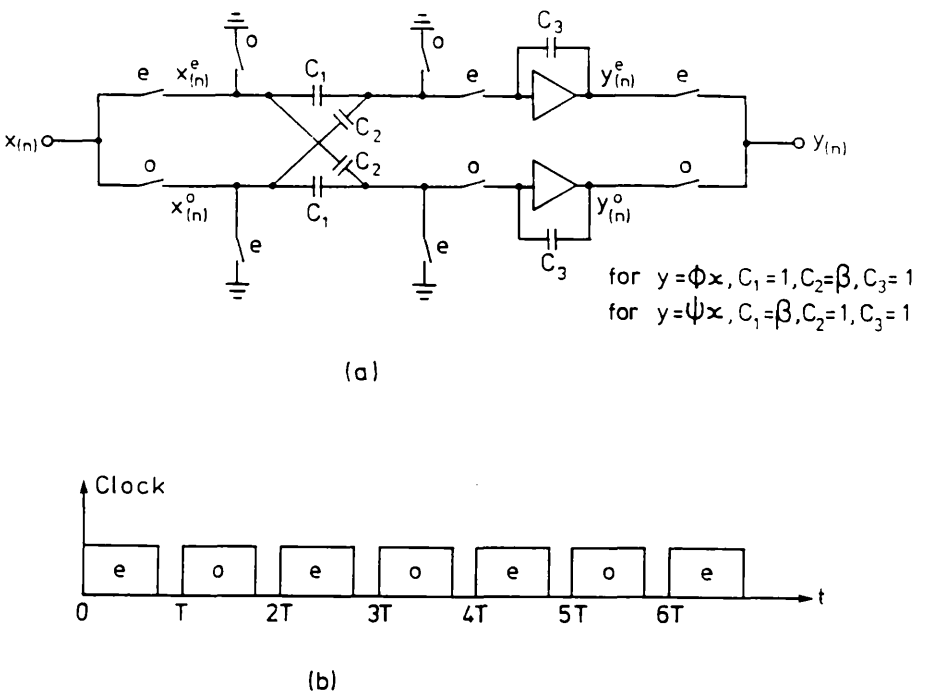


Fig.5.5 (a) A twintor circuit realising Φ and (b) Clock waveform

In a twintor each opamp is operated only in every other period, T. The charge relations for the circuit of Fig.5.5a are

$$C_3[y^e(n)-y^e(n-2)] = -C_1x^e(n) + C_2x^o(n-1) \qquad \text{when n even} \qquad (5.16a)$$

$$C_3[y^o(n)-y^o(n-2)] = -C_1x^o(n) + C_2x^e(n-1) \qquad \text{when n odd} \qquad (5.16b)$$

Therefore the overall transfer function is given by

$$Y(z) = \frac{1}{C_3} \frac{C_2z^{-1}-C_1}{1-z^{-2}} X(z) \qquad (5.17)$$

Notice that the denominator $(1-z^{-2})$ is exactly realised without term cancellation. It can be seen from Fig.5.5b that now the clock period is 2T compared to T in a conventional LDI integrator SC circuit. This means that the operation speed for the whole circuit, determined by sampling frequency, can be doubled without requiring an increase in opamp speed.

By selecting suitable capacitance values $-\Phi$ can be directly implemented. When twintors are connected together to form a ladder structure, some simplifications are possible by separating signals into two channels, Fig.5.6. The first equivalence in Fig.5.6 is obvious. For the second equivalence, notice that a sampling signal of an even (odd) channel opamp output in a odd (even) period is actually the signal held from the previous period, therefore a delay factor, z^{-1}, is realised. Notice that besides different selection of C_1 and C_2, Ψ can be realised as $z^{-1}(-\Phi)$ and so the cross coupling will precisely give Ψ. A number of switches are also saved by this two channel technique.

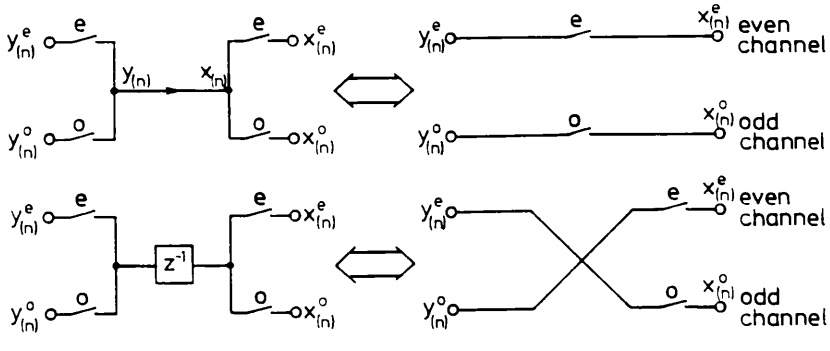


Fig.5.6 Two channel equivalent connection of twintors

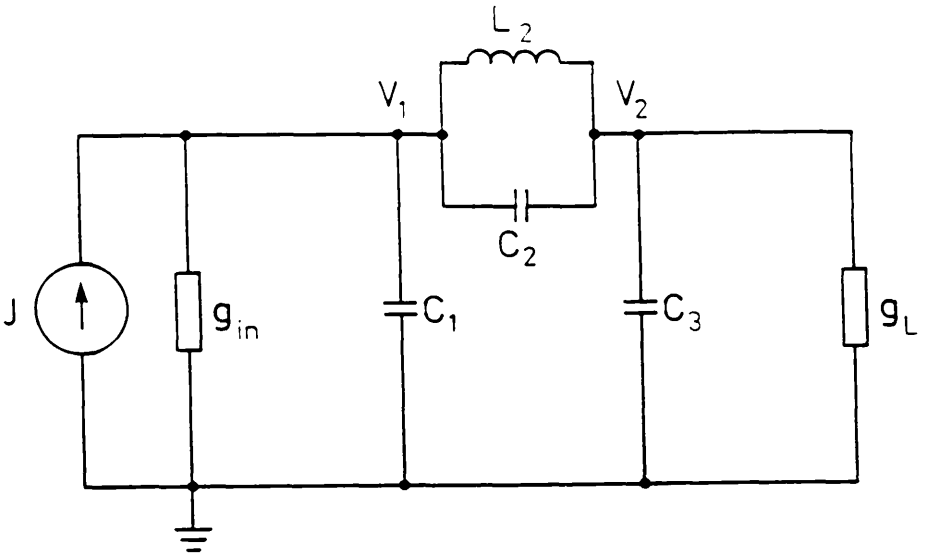


Fig.5.7 A 3th order lowpass RLC ladder

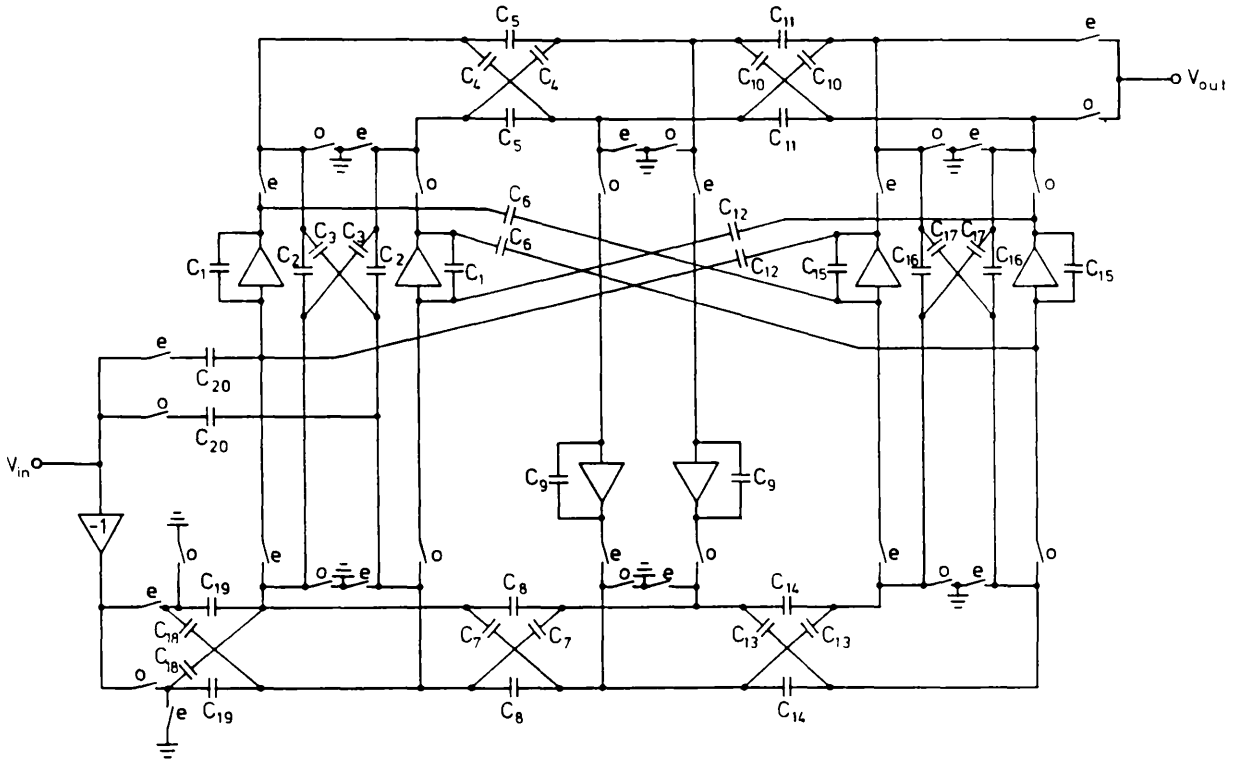


Fig.5.8 A 6th order bandstop SC bi−channel filter design

Specifications for the Bandstop SC Filter

lower passband edge		4.5 kHz	upper passband edge		5.5 kHz
lower stopband edge		3.5 kHz	upper stopband edge		6.5 kHz
passband ripple	<	0.1 dB	stopband attenuation	>	26 dB
sampling frequency		100 kHz			

Normalized Data for the Lowpass SC Ladder Reference Filter

G1 = GL = 1 C1 0.91646 L2 0.96995 C2 0.17046 C3 0.91646

Component Values for the Bandstop SC Filter

C1	14.79097	C2	1.414525	C3	1.398662	C4	1.614900	C5	1.633215
C6	15.64070	C7	37.44417	C8	37.86882	C9	1.000000	C10	1.141830
C11	1.154780	C12	10.93656	C13	37.86304	C14	38.29245	C15	10.57509
C16	1.011341	C17	1.000000	C18	1.977572	C19	2.000000	C20	1.000000

number of capacitors	40	number of switches	30
number of op amps	6	total capacitance	439.51
capacitance spread	38.29		

Table 5.3 Design data for the 6th SC bandstop filter

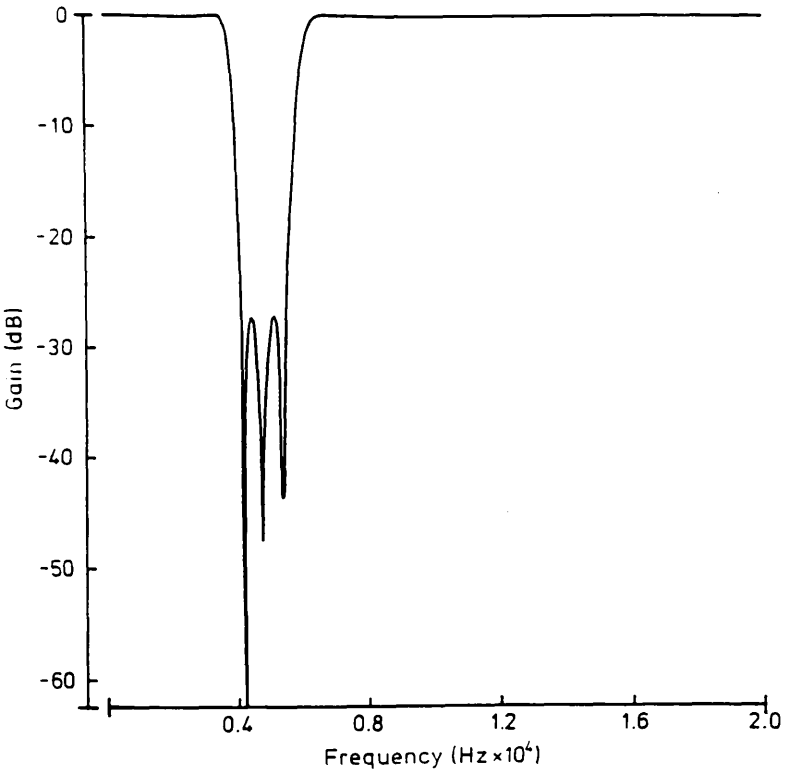


Fig.5.9 Computed response of the 6th order SC bandstop filter

An overall 6th order bi−channel bandstop SC ladder is shown in Fig.5.8 with the lowpass RLC ladder of Fig.5.7 as reference prototype. The specifications and the component values are listed in Table 5.3. The simulated response of the SC bandstop ladder is shown in Fig.5.9.

Finally it is necessary to indicate that although the twintor SC circuits have some theoretical attraction, such as the reduction in the switching rate, some preliminary studies show that their sensitivity behaviour is surprisingly poor. It is still not clear why this should happen despite their being based on ladder simulations. It should also be pointed out that the biquad method can provide perfect solution for most bandstop type designs, as the transfer function of a section of biquad is naturally a notch type function. The most difficult type of filtering for the biquad method is bandpass functions, and it has been shown in Chapter 4 that the ladder type circuits discussed in this thesis can be used to solve this problem very efficiently.

5.3.3) Lowpass to bandpass transformation

Although the lowpass to bandpass transformation is also applicable by using SC biquads to realise the bandpass operators no advantages are observed over standard design methods.

5.4 SUMMARY

Frequency transformation methods have been introduced in this chapter for non−lowpass type discrete filter design. The instability problem encountered in bilinear−LDI type highpass and bandstop filters can be avoided and for digital implementation some notable saving of hardware cost can also be gained in many cases.

A new strays−free SC circuit scheme has been proposed for bandstop SC ladder design. A major feature of the new circuit is that the clock period required is 2T so that the circuit can operate at a higher speed without extra demands on opamp performance. However it has also been indicated that the poor sensitivity of such circuit remains a unsolved problem.

CHAPTER 6

ACTIVE AND DIGITAL ALLPASS LADDER DESIGN

6.1 INTRODUCTION

Until now our discussion has been limited to the design of filters with amplitude characteristics. Commonly in communication systems, group delay characteristics are implemented by allpass networks, which are primarily designed to provide phase characteristics without interference with an existing amplitude response. However, in practical realisations the amplitude response will inevitably be influenced by component variations. It is important therefore to utilise circuit implementations having low amplitude sensitivity characteristics. Because allpass functions are non–minimum phase by definition, low–sensitivity ladder based design remains an open problem. Cascaded biquad sections are typical in both analogue and digital realisations instead and such topologies are highly sensitive to component deviations, especially in high–Q cases [1,36].

A novel method for allpass digital filter design has been proposed in [93,94]. The allpass transfer function is decomposed into two terms: a constant and a function realisable as the driving point impedance of a passive network, which is in turn simulated by a digital circuit. The resulting system is structurally allpass, that is, wordlength truncation will not introduce any distortion into the amplitude response. The above principle is employed in this chapter to develop a family of active–RLC, active–RC and SC filters.

The matrix methods covered in the previous chapters will still be followed. It will be shown that allpass ladders can again be derived by left and right decompositions. The opamps can be made canonical in number for RC and SC implementations if the allpass equaliser and the amplitude filter are considered together. Structurally allpass properties are proved for all realisations. The new configurations are also very suitable for parallel digital circuit implementations.

Major emphasis will be placed on SC circuit realisations. Design examples are given and comparisons are made between the different ladder based structures and with cascade biquads. It will be demonstrated that sensitivities of the amplitude responses of ladder systems are much lower than those of the cascade biquad structures and sensitivities of the delay responses are similar for all realisations. Low capacitance spreads are also observed for ladder based methods.

6.2 CONTINUOUS DOMAIN ALLPASS LADDERS

An allpass function in the s− domain has the following form,

$$H_a(s) = k \frac{P(-s)}{P(s)} \qquad (6.1)$$

where P(s) is a Hurwitz polynomial of order n. For convenience let the constant $k = -1$ if n is even and $k = 1$ if n is odd.

6.2.1) Active RLC allpass ladder synthesis

Separate P(s) into even and odd parts, [93]

$$P(s) = EvP(s) + OdP(s) \qquad (6.2)$$

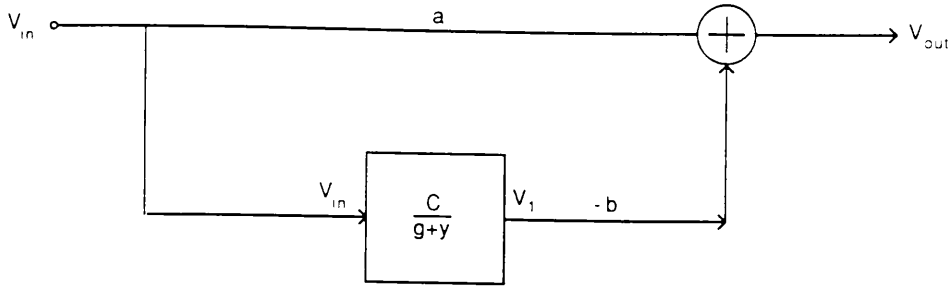
Define

$$Y(s) = \begin{cases} \dfrac{EvP(s)}{OdP(s)} & \text{if n even} \qquad (6.3a) \\ \\ \dfrac{OdP(s)}{EvP(s)} & \text{if n odd} \qquad (6.3b) \end{cases}$$

Substitute (6.2) and (6.3) into (6.1) and make the rearrangement,

$$H_a(s) = \frac{1 - Y(s)}{1 + Y(s)} = 1 - \frac{2}{1 + Y(s)} \qquad (6.4)$$

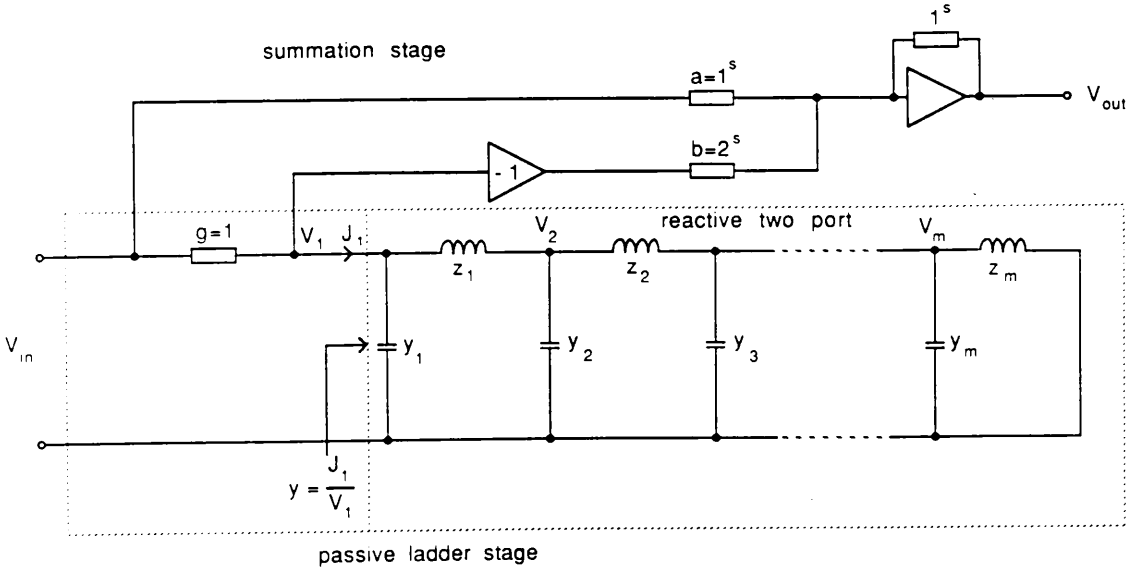
A signal flow graph (SFG) is given in Fig.6.1 to realise (6.4) where the transfer function 1 + Y(s) can be synthesised by a singly terminated LC ladder. It is well known that if P(s) = EvP(s) + OdP(s) is Hurwitz then Y(s) = EvP(s)/OdP(s) can be expanded in continued fraction form as (suppose n is even, i.e., n = 2m)



For s-domain a = c = g = 1 b = 2

For z-domain a = c = g = 1 b = 1 + z

Fig.6.1 Realisation of allpass function



$z_i = \Phi^{-1} L_i$ $y_i = \Psi^{-1} C_i$

For s-domain $\Phi^{-1} = \Psi^{-1} = s$

For z-domain $\Phi^{-1} = 1 - z^{-1}$ $\Psi^{-1} = z - 1$

Fig.6.2 Active– RLC allpass circuit

$$Y(s) = sC_1 + \cfrac{1}{sL_1 + \cfrac{1}{sC_2 + \cfrac{1}{sL_2 + \ddots \; sC_m + \cfrac{1}{sL_m}}}} \qquad (6.5)$$

with all $\{L_i\}$ and $\{C_i\}$ positive. If n is odd (i.e. $n = 2m + 1$) then the only difference is that (6.5) will terminate with sC_{m+1}. Eq. (6.5) provides a basis for a ladder realisation in Fig.6.2 where the summing amplifier is also included.

Traditionally, passive allpass filters are realised as cascaded lattice–derived bridged–T structures. Two major disadvantages are associated with this method; first the amplitude response is sensitive to all of the components and second the circuits are not canonical, requiring approximately 2.5n reactance elements in implementation. For the scheme shown in Fig.6.2 the amplitude response is completely insensitive to the deviation in the reactance elements (Section 6.4) and only n reactance elements are required. The summing amplifier and several resistors are an extra cost.

6.2.2) Active RC ladder design

The passive ladder network part of Fig.6.2 can be simulated by active RC circuits. The nodal admittance matrix equation for the passive ladder subnetwork is:

$$\left(sC + \frac{1}{s}\Gamma + G \right) V = J \qquad (6.6)$$

The matrix decomposition method for active RC network design described in Chapter 3 can be readily applied here. (6.6) can be written in the left–LUD form, (because all the capacitors in Fig.6.2 are connected to ground, C is simply diagonal and no real decomposition of C is necessary)

$$\begin{cases} W = -\left(s^{-1}\Gamma + G\right)V + J & (6.7a) \\ V = s^{-1} C^{-1} W & (6.7b) \end{cases}$$

or, after LU decomposition $\Gamma = \Gamma_r \Gamma_l$ the right-LUD form,

$$\begin{cases} (C+s^{-1}G)V = s^{-1}(-\Gamma_r W + J) & (6.8a) \\ W = s^{-1}\Gamma_l V & (6.8b) \end{cases}$$

Both (6.7) and (6.8) are linearised with respect to s^{-1} so that they can be realised directly by active-RC circuits. For a 6^{th} order circuit, the signal flow graphs (SFG's) of Figs.6.3a and 6.4a and the simulation circuits Figs.6.3b and 6.4b (incorporating the summation stages) can be obtained. Inversion in the output stage is incorporated in the simulation part. Other types of decompositions are also possible but they will not be discussed here.

The summing amplifier employed in the output stage in Fig.6.3b and 6.4b need not be realised explicitly in delay equalised filter systems. Provided that the allpass filter is succeeded by an amplitude filter stage, the virtual ground of the input integrator of the amplitude stage can be directly connected to P_V to realise the summation function. Thus realisations with canonical number of opamps are possible.

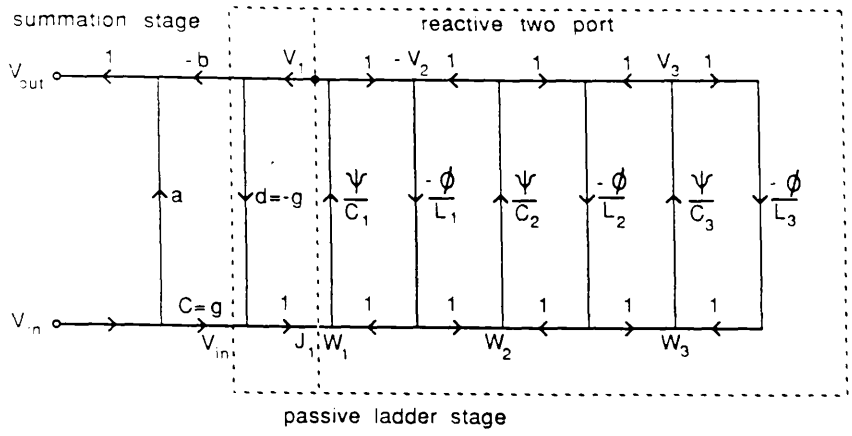
6.3 DISCRETE DOMAIN ALLPASS LADDERS

There are several approaches to the derivation of all-pass ladders in the z-domain. In particular it has been found most efficient to use the so-called bilinear-LDI method as it is both exact in frequency response and efficient in terms of implementation cost. Such a structure could be derived by the technique of Section 4.4 which places real-zeros in the ladder prototype to introduce the cancellation of capacitors after bilinear transformation. However a more straightforward derivation is presented here utilising a continued fraction expansion for z-domain transfer functions [92].

An allpass function in z-domain has the following form

$$H_a(z) = k \frac{z^n P(z^{-1})}{P(z)} \qquad (6.9)$$

where P(z) has poles inside the unit circle, n is the order of P(z) and $k = \pm 1$.



For s-domain $\Phi = \Psi = s^{-1}$ $\quad b = 2 \quad a = g = 1$

For z-domain $\Phi = 1/(1-z)^{-1} \quad \Psi = z^{-1}/(1 - z^{-1})$

$b = b_1 + b_2 z^{-1} \quad a = z^{-1} \quad b_1 = b_2 = g = 1$

Fig.6.3 (a) A left–LUD type SFG for allpass realisation

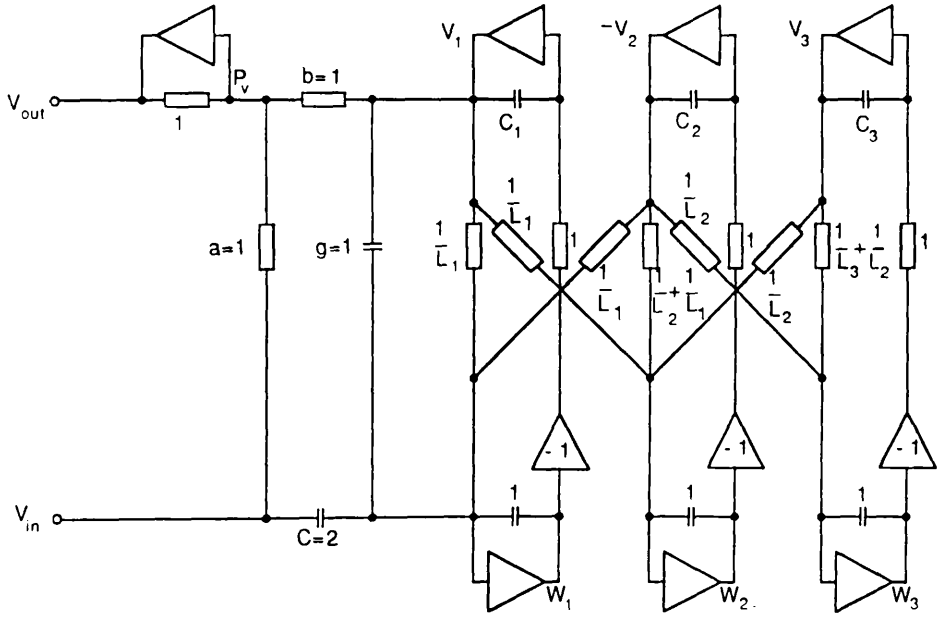
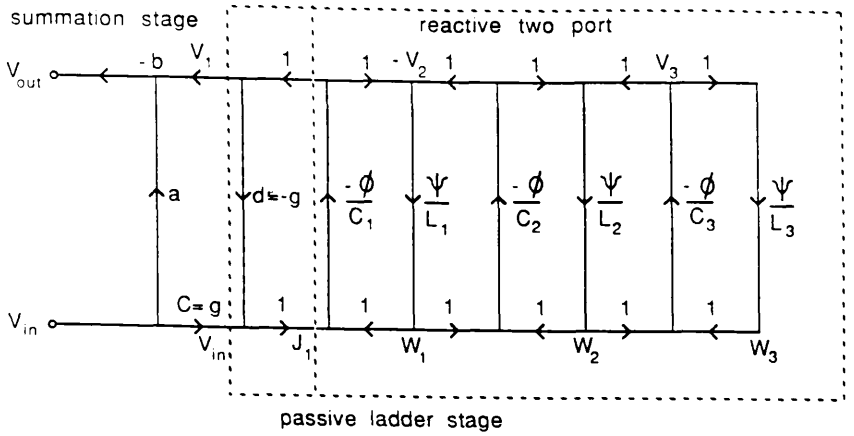


Fig.6.3 (b) A left–LUD type active–RC allpass filter
(elements in μF and μS)



For s-domain $\Phi = \Psi = s^{-1}$ $\quad b = 2 \quad a = g = 1$

For z-domain $\Phi = 1/(1-z)^{-1}$ $\quad \Psi = z^{-1}/(1 - z^{-1})$

$b = b_1 + b_2 z^{-1} \quad a = z^{-1} \quad b_1 = b_2 = g = 1$

Fig.6.4 (a) A right– LUD type SFG for allpass realisation

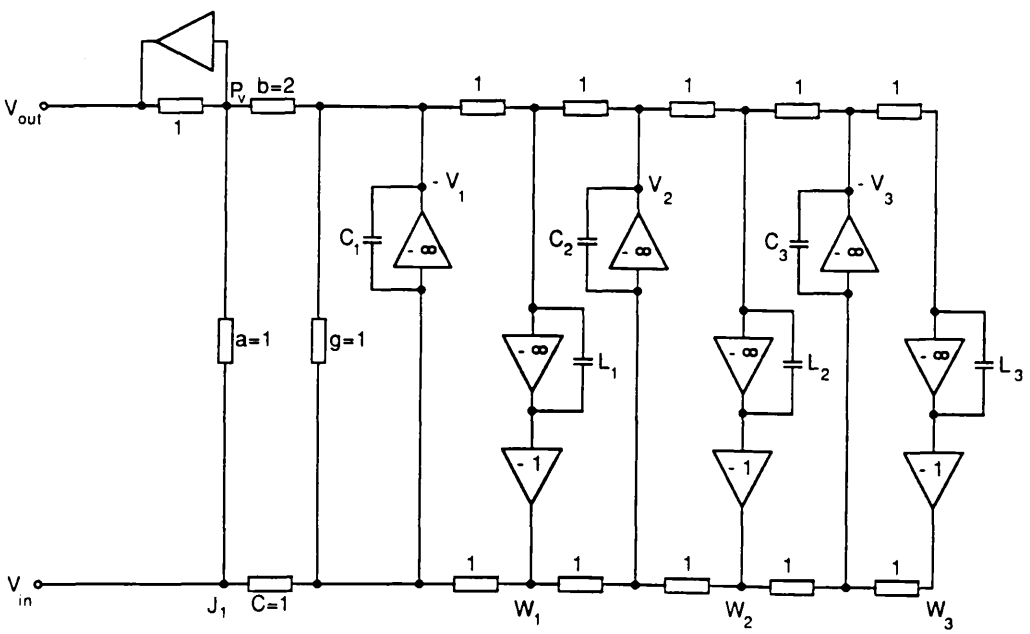


Fig.6.4 (b) A right– LUD type active– RC allpass filter (elements in μF and μS)

6.3.1) Left− LUD method for SC and digital ladder design

Suppose n is even, n = 2m and k = −1. Rearrange (6.9) to get

$$H_a(z) = -\frac{z^nP(z^{-1})}{P(z)} = 1 - \cfrac{1+z}{1 + \cfrac{zP(z)+z^nP(z^{-1})}{P(z)-z^nP(z^{-1})}} = 1 - \frac{1+z}{1+Y(z)} \qquad (6.10a)$$

Suppose n is odd, n = 2m + 1 and k = 1

$$H_a(z) = \frac{z^nP(z^{-1})}{P(z)} = 1 - \cfrac{1+z}{1 + \cfrac{zP(z)-z^nP(z^{-1})}{P(z)+z^nP(z^{-1})}} = 1 - \frac{1+z}{1+Y(z)} \qquad (6.10b)$$

To avoid the non− causal term z in (6.10) the transfer function is modified to

$$z^{-1}H_a(z) = z^{-1} - \frac{1+z^{-1}}{1+Y(z)} \qquad (6.11)$$

which introduces only a single extra delay. The continued fraction expansion of (6.10) can be achieved in terms of Ψ^{-1} and Φ^{-1} defined in (4.1) alternately, [92]

$$Y(z) = \Psi^{-1}C_1 + \cfrac{1}{\Phi^{-1}L_1 + \cfrac{1}{\Psi^{-1}C_2 + \cfrac{1}{\Phi^{-1}L_2 + \ddots \Psi^{-1}C_m + \cfrac{1}{\Phi^{-1}L_m}}}} \qquad (6.12)$$

For n odd (6.12) will terminate with a $\Psi^{-1}C_{m+1}$ term. Positive values of $\{C_i\}$ and $\{L_i\}$ are guaranteed [92]. By analogy with (6.5) it can be seen that a ladder simulation is appropriate. The passive ladder part in Fig.6.2 can again be used to realise (6.12) by a 'passive network', with admittance $y_i = \Psi^{-1}C_1$ and impedance $z_i = \Phi^{-1}L_i$. Although physically unrealisable, it can be used as prototype for SC and digital simulations. A nodal description can be set up for the ladder section of Fig.6.2 in terms of Ψ and Φ,

$$\left(\frac{1}{\Psi}C + \Phi\Gamma + G \right) V = J \qquad (6.13)$$

Left– LUD SC and digital circuit can be obtained by rewriting (6.13)

$$\begin{cases} W = -(\Phi\Gamma + G)V + J & (6.14a) \\ V = \Psi C^{-1} W & (6.14b) \end{cases}$$

This can be again represented by SFG, Fig.6.3a including the output stage, suitable for digital implementation. The corresponding SC circuit can be obtained by replacing the branches in the SFG by SC elements, Fig.6.5. The single z^{-1} of equation (6.10c) has been realised by a rearrangement of switching in the sample– and– hold and other input/output circuitry. The sampled input from an even phase is transferred to the output summing amplifier in the subsequent odd phase. The unit delay is realised when the output is sampled in the even phase of the next clock period.

Left– LUD type SC circuits will always require an even number of opamps, which is canonical for even order cases but not for odd cases.

6.3.2) Right– LUD method for SC and digital ladder design

Using (6.13) directly to derive the right– LUD type circuit causes difficulty in realising the termination terms. Instead, it is easy to verify the equivalence between (6.13) and the following system,

$$\left(\frac{1}{\Phi} C' + \Psi \Gamma + G \right) V = z^{-1}J \qquad (6.15)$$

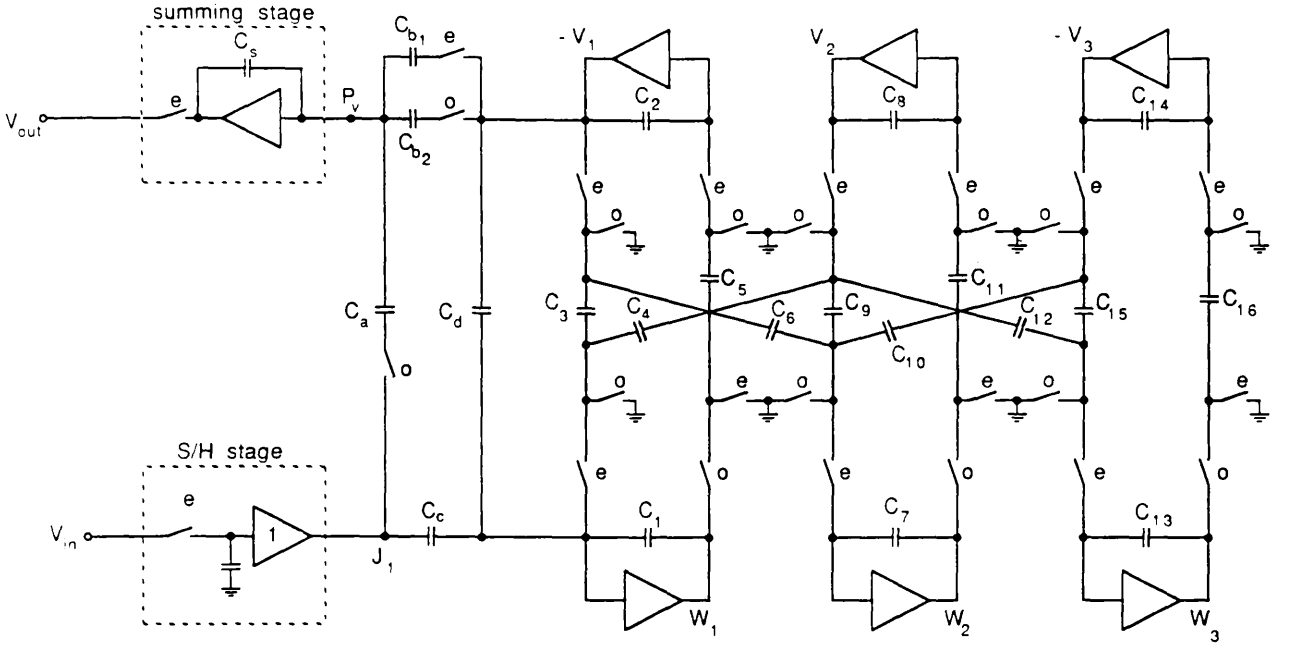


Fig.6.5 A left– LUD type SC allpass filter

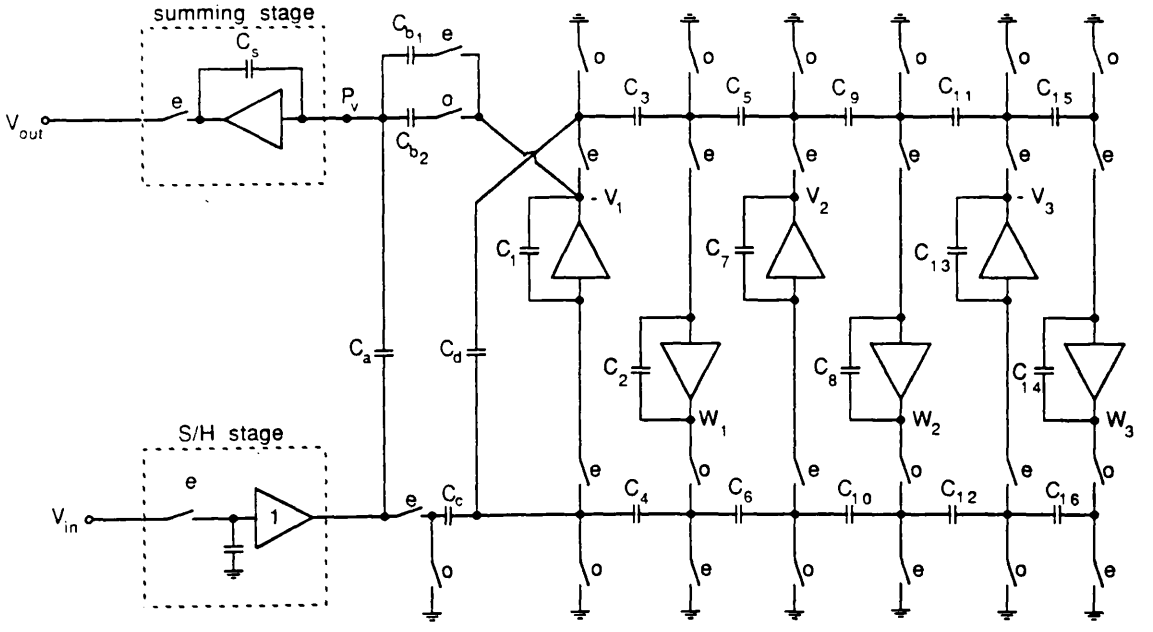


Fig.6.6 A right– LUD type SC allpass filter

where

$$C' = C - G \tag{6.16}$$

The right matrix decomposition structure can be derived by rewriting (6.15) as

$$\begin{cases} (C' + \Phi G)V = \Phi(-\Gamma_r W + z^{-1}J) & (6.17a) \\ W = \Psi \Gamma_l \quad V & (6.17b) \end{cases}$$

The SFG in Fig.6.4a can again be used to represent (6.17) and an illustration of SC replacement is given in Fig.6.6. The z^{-1} factor in (6.17a) cancels the non-casual factor of $1+z$ in (6.10).

Notice the circuit in Fig.6.6 is in principle very similar to the digital LDI ladder realisation presented in [94].

Right-LUD SC simulation can always realise a circuit with canonical number of opamps provided the amplitude and allpass stages are considered together. However for narrow band SC design right-LUD will result in a larger total capacitance than an Left-LUD design.

From Fig.6.4a it is seen that there is a delay-free-loop at the termination stage: $v_1 \rightarrow -g \rightarrow J_1 \rightarrow \Phi/c_1 \rightarrow v_1$. For digital realisation this can be eliminated by the equivalent circuit transformation shown in Fig.6.7. The resulting circuit is highly parallel and requires only a canonical number of multipliers for digital implementation. The number of additions required is also relatively small (roughly 2n).

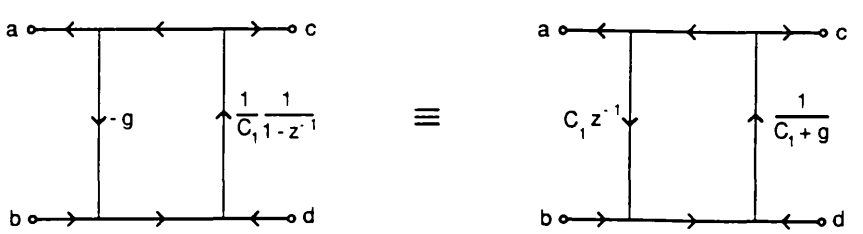


Fig.6.7 A network transformation to eliminate the delay-free-loops

6.4 SENSITIVITY ESTIMATIONS

In the fabrication process, nonideal factors will inevitably lead to a deviation in system parameters. In the digital case, the nonideal factor would be the truncation of multiplier coefficients to finite wordlength which will only have an affect on $\{C_i\}$ and $\{L_i\}$. For analogue cases, inaccuracies in the values of $\{C_i\}$, $\{L_i\}$ and all the unity valued elements Figs.6.2– 6.6 would affect the sensitivity.

It will be proved that the amplitude response of the structures introduced in this section, unlike their biquad counterparts, are completely insensitive with respect to the deviation of most element values and are bounded for a few terminating elements. The transfer functions of Figs.6.2– 6.6 have the form

$$\frac{V_{out}}{V_{in}} = H_a = \pm \left[a - \frac{bc\ v_1/J_1}{1 + d\ v_1/J_1} \right] \qquad (6.18)$$

for Figs.6.2, 6.3b, 6.4b $a= c= d= 1$, $b= 2$ and for Fig.6.5, 6.6 $b= b_1+ b_2z^{-1}$, $a= b_1= b_2= c= d= 1$.

Remark: *For the circuits in Fig.6.2– 6.6 if* ***a, b*** (or b_1 and b_2), ***and c are fixed then*** $|H_a|=1$ ***regardless*** of ***all the other parameters, even the unity valued elements.***

Proof: In the s– domain (Fig.6.2, 6.3b and 6.4b) equation (6.18) becomes

$$\left| H_a \right| = \left| \frac{1 - v_1/J_1}{1 + v_1/J_1} \right| \qquad (6.19)$$

It is easily seen that $|H_a|=1$ if v_1/J_1 is imaginary.

For the circuit in Fig.6.2, v_1/J_1 is certainly imaginary, being the admittance of a reactive network.

For the circuit in Fig.6.3b, apply Mason's formula [96] to derive v_1/J_1,

$$\frac{v_1}{J_1} = \frac{1}{\Delta} \sum_{\text{all forward paths}} (g_k \Delta_k) \qquad (6.20)$$

with

$$\Delta = 1 - \sum_m P_{m1} + \sum_m P_{m2} - \sum_m P_{m3} + \ldots\ldots \qquad (6.21)$$

where g_k is the product of edge weights for kth forward path.

P_{mr} is the product of loop transmissions for the mth set of vertex−disjoint feedback loops.

Δ_k is the value of Δ for the part of the graph having no vertices in common with the kth forward path.

Every loop in the subnetwork of the reactive two port in Fig.6.3a involves exactly one Ψ term and one Φ term. In the s−domain, $\Psi\Phi = (j\omega)^{-2} = -\omega^{-2}$ and therefore $P_{mr} = \Pi(\Psi/C_i)(-\Phi/L_j)$ will be real , so will all Δ and $\{\Delta_k\}$. There is only one forward path from J_1 to v_1, $g_1 = \Psi/C_1 = j\omega/C_1$, hence from (20) v_1/J_1 is imaginary and $|H_a|=1$. Notice that this imaginary property is solely structural and is not influenced by deviation of any parameter. A similar proof can be applied to the circuit of Fig.6.4b.

For the z−domain circuit in Fig.6.5, note that all Δ and $\{\Delta_k\}$ are again real as

$$\Psi\Phi = \frac{z^{-1}}{(1-z^{-1})^2} = -\sin^{-2}\left(\frac{\omega T}{2}\right) \qquad \text{for } z=e^{j\omega T} \qquad (6.22)$$

Since only one forward path is $g_1 = \Psi/C_1$, from (20) v_1/J_1 will have the form of $v_1/J_1 = \alpha\Psi$ with α real. Hence the following identities are derived,

$$\left| H_a \right| = \left| 1 - \frac{1+z}{1+J_1/v_1} \right| = \left| \frac{-1+\frac{1-z}{1+z}+2\frac{J_1/v_1}{1+z}}{1+\frac{1-z}{1+z}+2\frac{J_1/v_1}{1+z}} \right| = \left| \frac{-1+(1+\frac{2}{\alpha})\frac{1-z}{1+z}}{1+(1+\frac{1}{\alpha})\frac{1-z}{1+z}} \right| \qquad (6.23)$$

As $(1-z)/(1+z) = j\tan(\omega T/2)$ is imaginary for $z = e^{j\omega T}$, it is seen that $|H_a| = 1$. A similar result can be proved for the circuit in Fig.6.6.

The sensitivity fomulae for the remaining elements in the circuits in Fig.6.3b,4b can be derived as (since $Y(j\omega) = J_1/v_1$ is a pure imaginary number)

$$-1 \leqslant \frac{a}{|H_a|}\frac{\partial|H_a|}{\partial a} = \pm\frac{1 - |Y(j\omega)|^2}{1 + |Y(j\omega)|^2} \leqslant 1 \qquad (6.24a)$$

$$-2 \leqslant \frac{b}{|H_a|}\frac{\partial|H_a|}{\partial b} = \frac{c}{|H_a|}\frac{\partial|H_a|}{\partial c} = \frac{\pm 2}{1 + |Y(j\omega)|^2} \leqslant 2 \qquad (6.24b)$$

$$-2 \leqslant \frac{d}{|H_a|}\frac{\partial|H_a|}{\partial d} = \frac{\pm 2}{1 + |Y(j\omega)|^2} \leqslant 2 \qquad (6.24c)$$

Similar formulas can be derived for the circuits in Fig.6.5 and 6.6.

6.5 EXAMPLES AND COMPARISONS

As an example, a 6th order allpass SC filter is designed to achieve an equi-ripple correction of the delay distortion caused by a 6th order SC bandpass filter. The design data given in Table 6.1 relates to the two ladder based equaliser structures, left-LUD and right-LUD Fig.6.5 and 6.6. Each of these circuits can be followed by the amplitude stage in Fig.6.8 (drawn in a different way from Fig.4.2a), designed as a 6th order elliptic left-LUD type SC circuit, Table 6.2. All the circuits have been scaled for maximum dynamic range. The P_V point of either circuit in Figs.6.5 and 6.6 can be directly connected to the input of the circuit in Fig.6.8. The amplitude and delay responses are shown in Figs.6.9a, b.

The following formula is used to measure the overall system sensitivity

$$S = \left\{ \sum_i \left[\frac{c_i}{|H|}\frac{\partial|H|}{\partial c_i} \right]^2 \right\}^{1/2} \qquad (6.25)$$

The system delay sensitivity can be defined in the same way. For comparison two cascade biquad SC circuits are designed for the delay equalisation stage, using biquad Topologies 1 and 2 of [36] respectively. The resulting design parameters are listed in Table 6.3. As in [36], Topology 1 has quite a small spread but very high sensitivity, while Topology 2 has an improved sensitivity at the cost of high spread, Fig.6.10. Other biquad topologies [36] show some trade–off of sensitivity and spread between these two extremes. However it is seen that ladder based structures demonstrate the significant advantage of both low sensitivity and low capacitance spread.

The amplitude sensitivities for ladder circuits, Fig.6.5,6.6, are mainly determined by five parameters, i.e., a = C_a/C_s, b_1 = C_{b1}/C_s, b_2 = C_{b2}/C_s, c = C_c/C_1 and d = C_d/C_1. Provided these ratios are carefully controlled, good allpass properties can be expected.

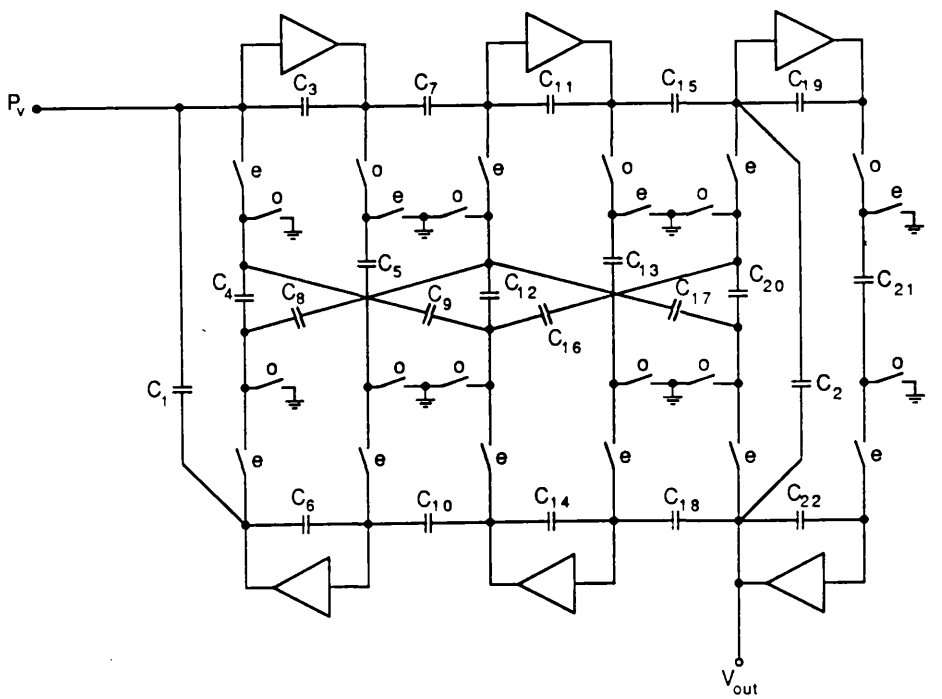


Fig.6.8 A 6th order left–LUD SC elliptic LUD filter

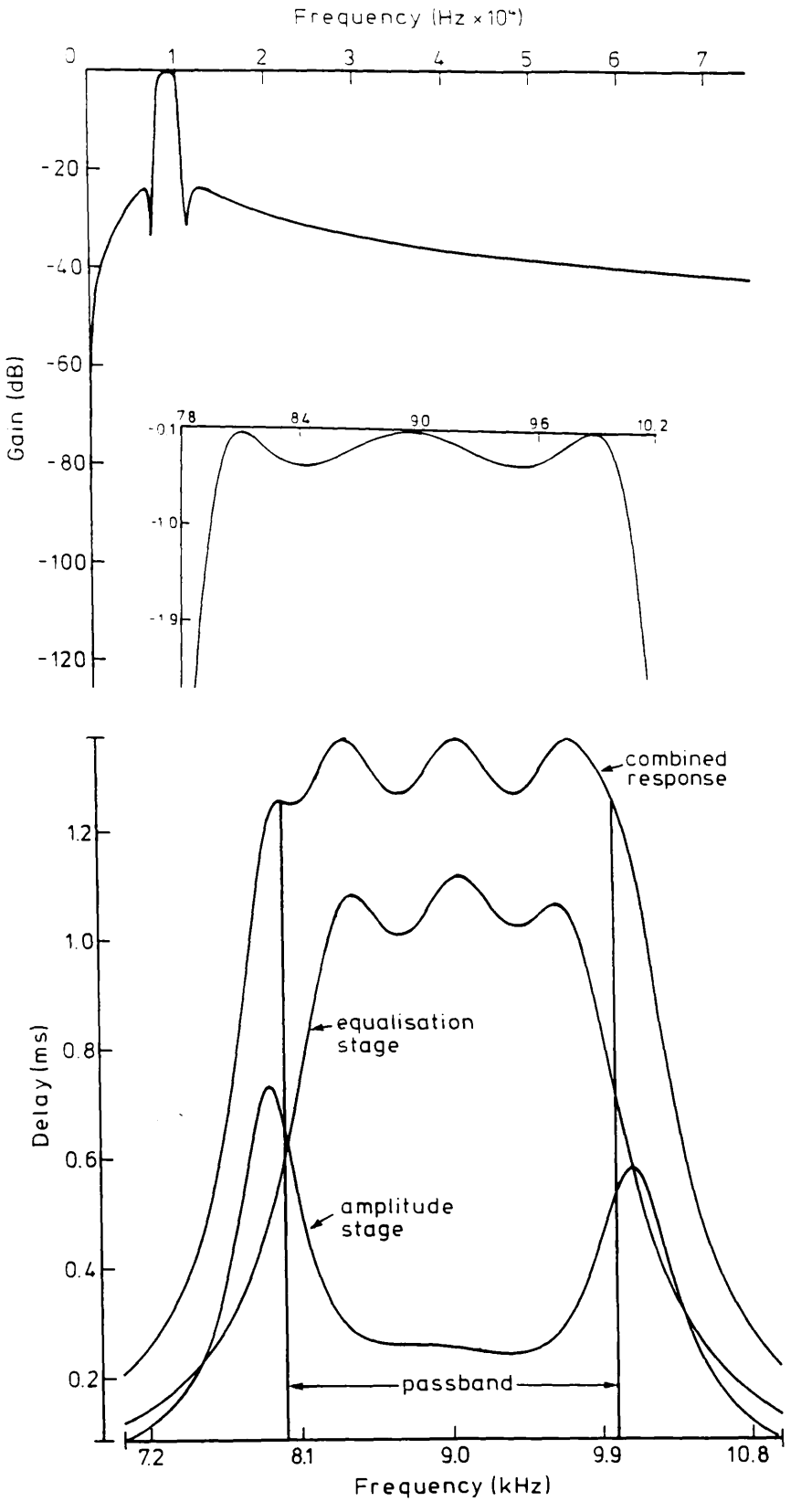


Fig.6.9 Amplitude and delay response of the 6th order SC LUD filter

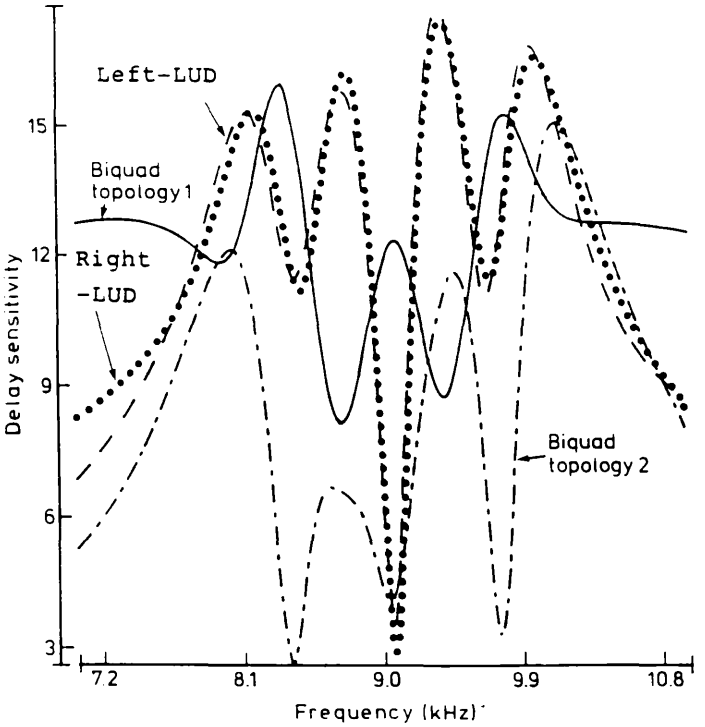


Fig.610b Delay sensitivities of equalisers

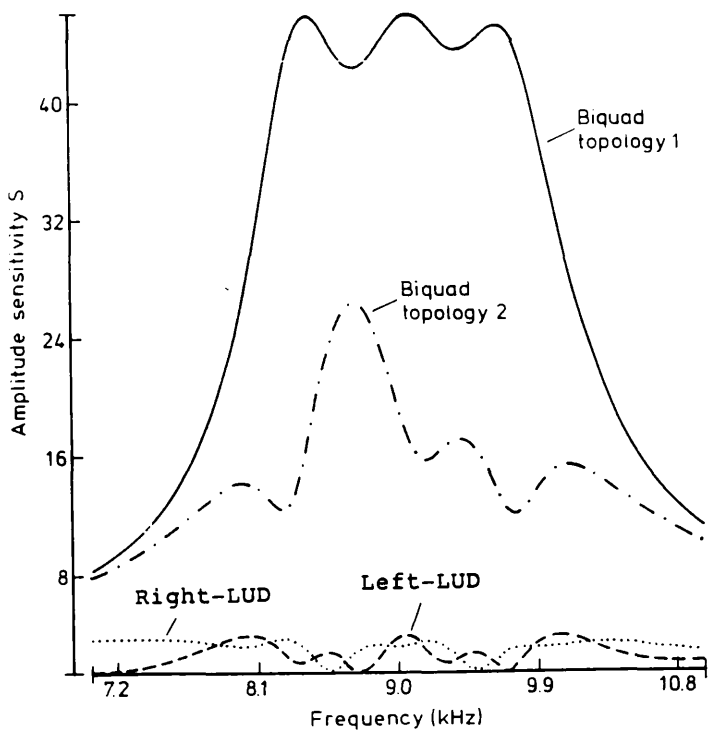


Fig.610a Amplitude sensitivities of equalisers

Specification for delay equaliser					
lower equalisation edge 8000Hz			upper equalisation edge 10000Hz		
approximation type equi-ripple			in-band ripple < 0.00014sec		
filter order 6			sample frequency 150000Hz		
Poles of normalised allpass transfer function in s-domain					
- 0.0518242 + j1.01293			- 0.0518242 - j1.01293		
- 0.0482866 + j1.08983			- 0.0482866 - j1.08983		
- 0.0458278 + j0.93370			- 0.0458278 - j0.93370		
Component values for the Left-LUD SC ladder					
Ca 1.000	Cb1 1.023	Cb2 1.023	Cc 2.333	Cd 2.386	
C1 9.903	C2 2.380	C3 3.273	C4 1.000	C5 1.000	C6 1.011
C7 24.22	C8 2.478	C9 8.660	C10 1.000	C11 1.000	C12 1.000
C13 29.29	C14 2.651	C15 10.99			
total capacitance		109 units	capacitance spread		29 units
number of switches		27	number of capacitors		21
number of opamps		6			
Component values for the Right-LUD SC ladder					
Ca 1.015	Cb1 1.000	Cb2 1.000	Cc 1.015	Cd 1.000	
C1 8.878	C2 9.546	C3 3.289	C4 3.982	C5 1.000	C6 1.000
C7 20.34	C8 22.19	C9 8.305	C10 7.565	C11 1.000	C12 1.000
C13 29.21	C14 2.660	C15 1.000			
total capacitance		138 units	capacitance spread		29 units
number of switches		28	number of capacitors		21
number of opamps		6			

Table 6.1 Design data for SC delay equalisers

Specification for amplitude filter			
lower passband edge	8000Hz	upper passband edge	10000Hz
lower stopband edge	7200Hz	upper stopband edge	10800Hz
passband ripple	< 0.3dB	stopband attenuation	> 25dB
approximation type	elliptic	filter order	6
sampling frequency	150000		

Component values for the Left-LUD SC ladder					
C1 1.000	C2 1.000	C3 10.83	C4 2.769	C5 1.000	C6 2.182
C7 5.041	C8 1.000	C9 1.335	C10 1.356	C11 10.76	C12 4.055
C13 1.794	C14 3.733	C15 5.873	C16 2.573	C17 1.263	C18 1.000
C19 7.265	C20 3.285	C21 1.000	C22 2.430		

total capacitance	74 units	capacitance spread	10 units
number of switched	25	number of capacitors	22
number of opamps	6		

Table 6.2 Design data for a 6th order bandpass SC filter

	Left-LUD	Right-LUD	Biquad top. 1	Biquad top. 2
total capacitance	109 units	138 units	102 units	311 units
capacitance spread	29 units	29 units	26 units	62 units
number of opamps	6	6	6	6
number of switches	27	28	32	32
number of capacitors	21	21	24	24

The S/H and summation stages are excluded

Table 6.3 Comparison of various SC delay equaliser

6.6 CONCLUSIONS

A systematic approach has been proposed for active and digital allpass ladder design, which demonstrates very low amplitude sensitivity as well as other advantages, such as high parallelism for digital realisation and low capacitance spread for SC realisation. It is shown that the ladder structures can be implemented with a canonical number of multipliers for digital circuits or with a canonical number of opamps for analogue circuits.

CHAPTER 7

SOFTWARE PACKAGE AND FABRICATED CIRCUITS

7.1 INTRODUCTION

The previous chapters have proposed theories and procedures for high–quality ladder filter design. In this chapter we examine some practical implications of the research work.

The first is the development of a useful CAD tool for integrated filter design. The systematic and regular features of the matrix methods have been harnessed in a comprehensive silicon compiler system, PANDDA, together with a variety of other sophisticated approximation and prototype synthesis algorithms.

The second, which is the ultimate aim of the research, is to produce integrated filters with improved performance. This is demonstrated by two commercially fabricated telecommunication LUD filters. The specifications of both circuits are known to be difficult for existing design methods and have formed part of the motivation for this research work. The test results of a biquad filter designed by the author is also included as an additional example.

7.2 PANDDA; A PROGRAM FOR ADVANCED NETWORK DESIGN: DIGITAL AND ANALOGUE

The PANDDA software package has been developed by the author with cooperation with R.K. Henderson during this research. Its distinguishing features are summarised as follows. A full report covering all the other stages can be found in [117].

Specification

Either parameters of a classical approximation or a piece–wise linear tolerance boundary can be selected for the specification of attenuation and group delay.

Filter options include network structure (biquad, LUD or direct decompositions, leapfrog etc.), circuit implementation (switched–capacitor, active–RC, digital), non–ideal circuit parameters (unit capacitance, switch resistances, op–amp parameters, wordlength) and scaling directives.

Approximation and Prototype Design

The task of approximation is to set up a transfer function which meets the amplitude and group delay specifications. To avoid unnecessarily complex circuits this function should be of minimum order. The best known classical approximations can be obtained; Butterworth, Chebyshev, inverse Chebyshev and elliptic.

Specialised amplitude responses can also be designed. The transfer functions can be asymmetric and the order of tangency of certain extreme points (touch points) of the amplitude response to attenuation boundaries can be specified. In this way a wide class of transfer functions lying between conventional equiripple and maximally-flat types may be designed. High order touch points may be used to smooth the amplitude function near the band-edge to reduce the delay peaking, and improve sensitivity.

The designer has the freedom to specify the sequence of passbands and stopbands and the distribution of touch points in each. The attenuation function in each band is specified by a pair of piece-wise linear boundaries through which a linear-phase FIR, IIR or continuous time transfer function will be fitted. Unusual transfer functions can be designed. Approximation of allpass transfer functions can also be performed to equalise the group delay of the amplitude function.

Having designed a suitable transfer function, a prototype for succeeding filter design must be calculated. This takes the form of either a normalised doubly-terminated LC ladder or a transfer function in factorised form.

Design of passive ladder networks is accomplished by an extension of an iterative design method due to Orchard [15] in conjunction with a simplified insertion-loss synthesis [2,105] program. Features of the iterative algorithm are very good accuracy and the ability to design high order networks (up to 100th). The conventional synthesis program is used to set up the structure and provide initial component values for the iterative part.

Filter realisation

The filter realisation stage of the program must take a prototype filter and convert it into a realiseable network description. The general approximation capability above means that these functions can take a wide variety of different forms. For easy conceptual use, it is important to guarantee that all these transfer functions can be realised by a regular, stable, canonic network in a variety of network topologies. This can be achieved by the matrix methods developed in previous chapters. An additional advantage is that they are highly suitable for implementation of computer software. The matrix methods form the core of the filter realisation section of PANDDA.

The design stage is divided into three steps.

Step 1) the prototype passed from the previous stage, which may be a passive ladder or a set of the poles and zeros of the transfer function, is pre– processed and, if it is a ladder design, symmetric matrix polynomial in terms of (3.4) is formulated by a stamp method [95].

Step 2) the prototype system is linearised into a set of matrix equations according to the selection of structure options by manipulations presented from Chapter 3 to Chapter 6. As the sparsity of the matrix system is known at this step, a quick computation of internal voltage level for scaling and sensitivity analysis is achieved.

Step 3) the matrix system is expanded into a internal network description. A library of basic bullding– blocks, e.g. Miller integrator in active– RC, LDI integrator SC and delay element in digital, is established. All the matrices are traversed and the netlist is produced according the types of building– blocks and the inter– connections of the non– zero entries.

The above procedures greatly ease the complexity of the software. As it can be seen that the first step and the third step are independent of the particular circuit structure to be realised (apart from reading a pole– zero file or reading a ladder prototype file) so that the algorithms for these two steps are very straightforward. Only at the second step have the design types to be taken into consideration, but this only involves the setting up of a few matrices which is carried out either by well known LU decomposition algorithm or by some direct manipulation.

7.3 TEST RESULTS OF FABRICATED SC LADDER CIRCUITS

Three SC circuits designed by the author have been fabricated. The practical results presented in this section are provided by courtesy of Wolfson Microelectronics Ltd., Edinburgh.

Design 1:

The first circuit is a 6th order bandpass Butterworth type filter, its ideal transfer function has been plotted in Fig.7.1. Its relative bandwidth (defined in Section 4.7) RBW= 0.0625 indicating that the passband is quite narrow. According to the stastistical studies provided in Section 4.7, left− LUD is the best candidate for this specification. The design data is listed in Fig.7.2 (in SCNAP format [71]). In Fig.7.3 the measured reponses are given. A circuit layout is shown in Fig.7.4.

Design 2:

The second circuit is a 8th order wide bandpass filter with relative bandwidth RBW= 2.85. In this case, realisation of an elliptic function by any of the structures would result in a very large capacitance spread and an asymmetric type transfer function similar to one shown in Fig.4.28 has to be used. For this particular case the discussion of Section 4.7 indicates that the left− LUD type circuit behaves much better than any other type of circuit hence it is selected for the final design.

A difficult problem for this design is that the numerator of the transfer function is an even polynomial (unlike that of Fig.4.28). At the stage when this filter was designed, the canonical design method of Section 4.3.4 had not yet been discovered so that a canonical solution could not be found for ladder simulations. Fortunately the numerator contains two zeros located at the origin. The transfer function is thus partitioned into a biquadratic function with a single s numerator term and a 6th order rational function with an odd numerator polynomial. The biquadratic function is formed by selecting a pair of the lowest− Q poles, which eases the sensitivity problem. The 6th order function is realised by the left− LUD method, and the cascaded circuit results in a relatively small spread and small sensitivity.

The ideal response (solid line) and the measured response of a test chip (dotted line) are given in Fig.7.5 and 7.6. Notice that in practice a pair of transmission zeros was moved to 2fs to break up the un−switched capacitor−opamp chain. The layout of a test chip is shown in Fig.7.7.

Due to the fact that the specification is extremely difficult, with very wide bandwidth, it can be seen that the template at the passband edges has been violated by the measured response. This was found to have been caused by the truncation of capacitance values to finite precision. By carefully selecting the truncation or the rounding of capacitance values, this problem can be avoided and this will be done for a revised version of the design. This serves to emphasise the importance of sensitivity problem in practical integrated filter design.

Design 3:

An additional example of a biquad design is shown in Figs.7.8−7.9 (ideal response in solid line and measured response in dotted line) and Fig.7.10 (circuit layout). The specification is of an unusual downward sloping shape. As the maximum power transmission is attained only at one point (lower passband edge), the argument of low sensitivity of ladder circuits is no longer valid. Also ladder and biquad designs result in nearly the same total capacitance. For this reason the biquad design was finally selected. This example also demonstrates that the application of ladder circuits is not completely universal.

7.4. SUMMARY

A new program for filter design has been introduced. Several advanced facilities which remove traditional design limitations have been illustrated.

Some test results of SC chips are presented. The left−LUD method has been succesfully applied to the design of practical circuits known to present difficulties for existing methods. The value of the research developed in this thesis has thus been illustrated in a real engineering environment.

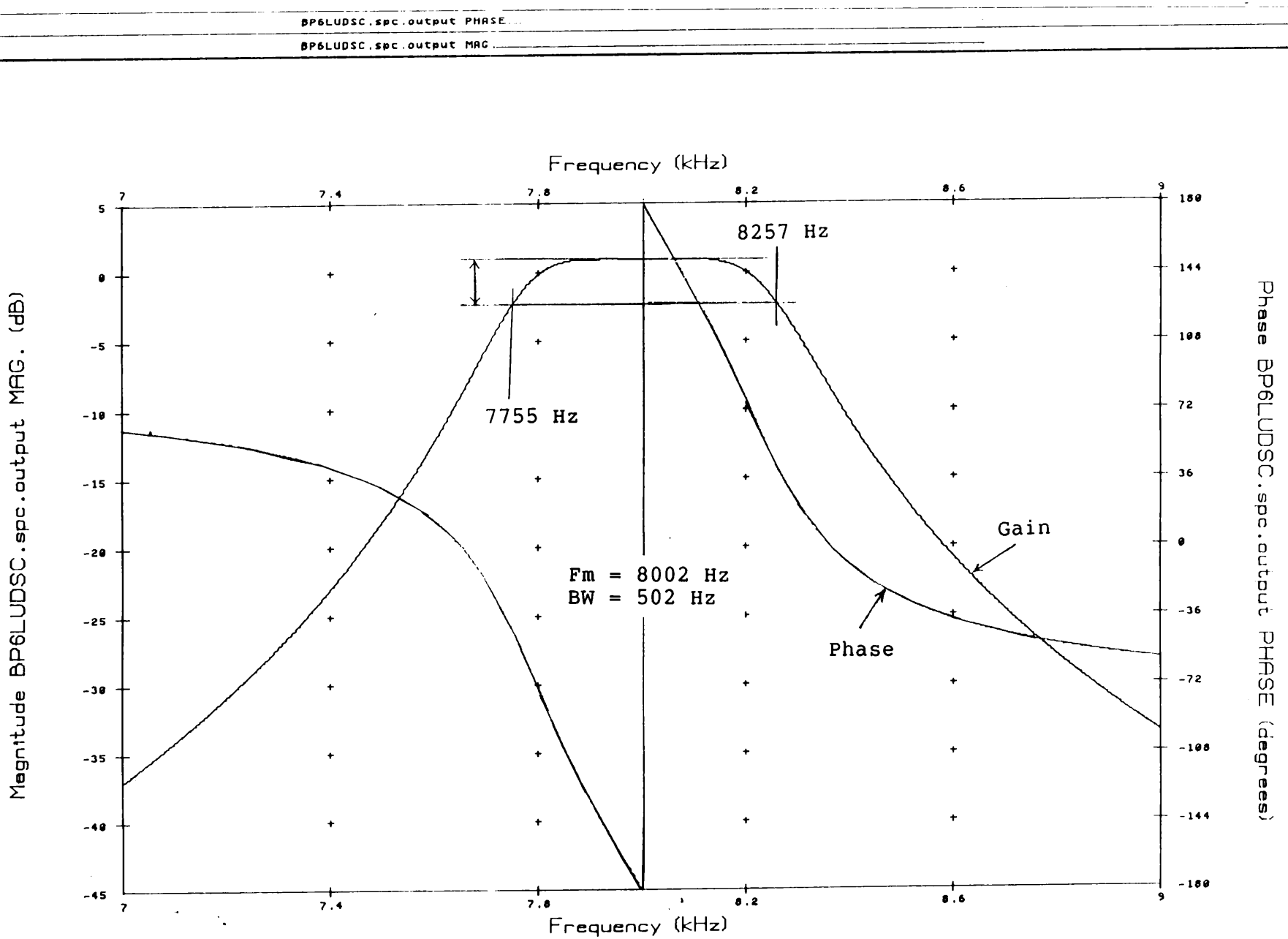


Fig.7.1 An ideal 6th order bandpass transfer function

```
! Total capacitance = 329.7711units
! Capacitance spread = 96.24657units
! Average capacitor = 17.35637units
! Number of capacitors = 19
! Number of switches = 25
! Number of op-amps = 6


analyze
  ideal freq 7700.000 8300.000 lin 201
  output 2
end

timing
  def
    T = 0.2427184E-05
  end
  even T (0 0.0) (1 1.0) (2 1.0)
  odd T (0 1.0) (1 0.0) (2 0.0)
end

subckt opamp 1 2 3 4 (gain, BW)
  vcvs 1 2 3 4 gain
end

circuit
vs 1 0 ac 1.000000 0.0
opamp 0 3 4 0 (0.1000000E+08, 1000000.)
opamp 0 5 6 0 (0.1000000E+08, 1000000.)
opamp 0 7 8 0 (0.1000000E+08, 1000000.)
opamp 0 9 10 0 (0.1000000E+08, 1000000.)
opamp 0 11 12 0 (0.1000000E+08, 1000000.)
opamp 0 13 2 0 (0.1000000E+08, 1000000.)
c 4 3 93.55485
c 6 5 96.24657
c 6 7 1.145088
c 8 7 16.26420
c 10 9 3.985315
c 12 11 37.33633
c 2 11 1.000000
c 2 13 4.065341
c 15 16 1.000000
c 17 18 9.030050
c 19 20 1.000000
c 21 22 21.96506
c 23 22 1.000000
c 21 26 1.000000
c 23 26 23.57698
c 29 30 3.887713
c 10 3 5.640317
c 2 7 1.000000
c 31 3 7.073258
s 4 15 even
s 15 0 odd
s 16 9 odd
s 16 0 even
s 6 17 even
s 17 0 odd
s 18 11 odd
s 18 0 even
s 8 19 even
s 19 0 odd
s 20 13 odd
s 20 0 even
s 10 21 even
s 21 0 odd
s 22 3 even
s 22 0 odd
s 12 23 even
s 23 0 odd
s 26 5 even
s 26 0 odd
s 2 29 even
s 29 0 odd
s 30 7 even
s 30 0 odd
s 1 31 even
end
```

Fig.7.2 Netlist of a 6th order SC ladder design (in SCNAP format)

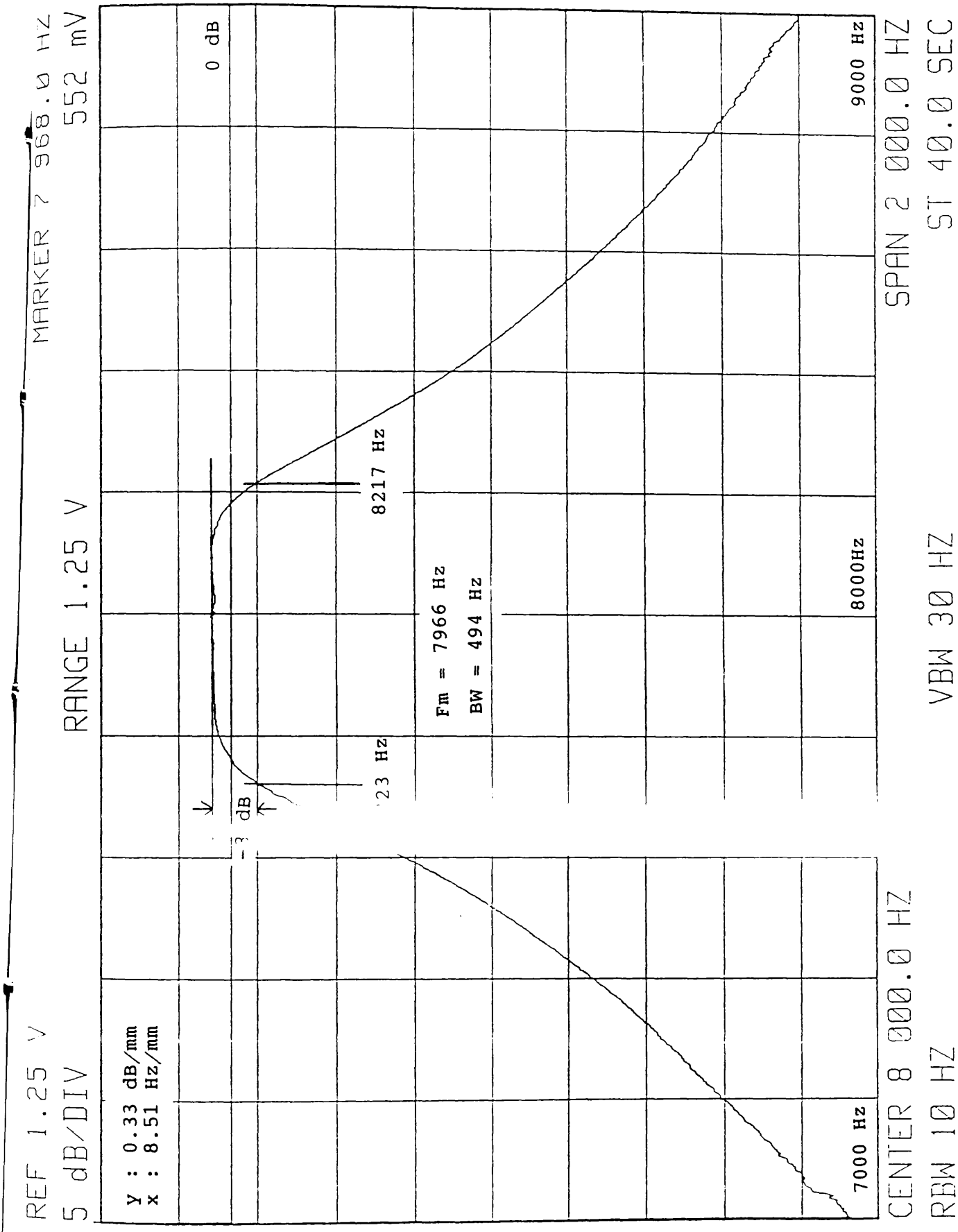


Fig.7.3 Measured response of a 6th order LUD SC ladder

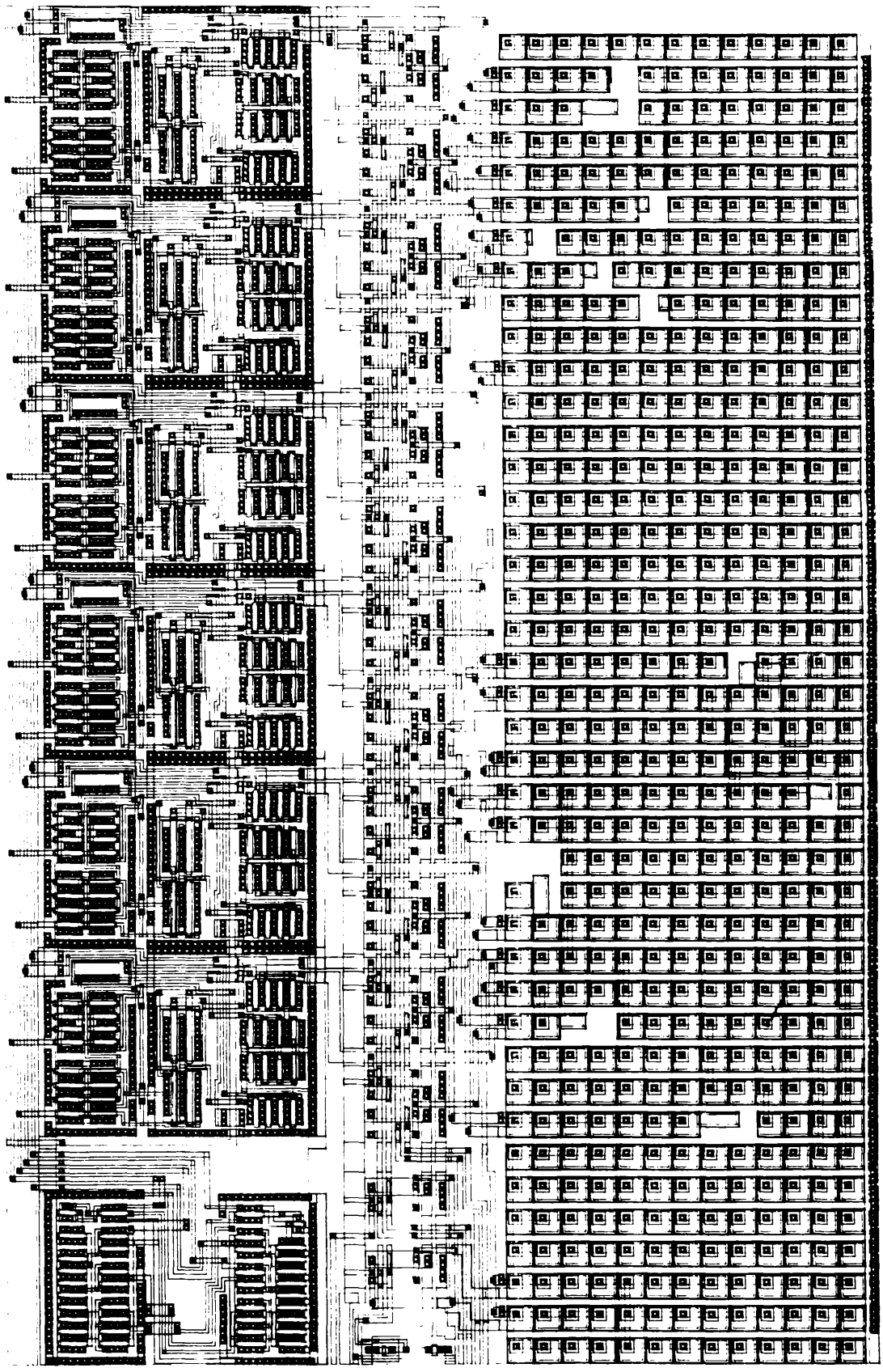


Fig.7.4 Layout of a 6th order LUD SC ladder

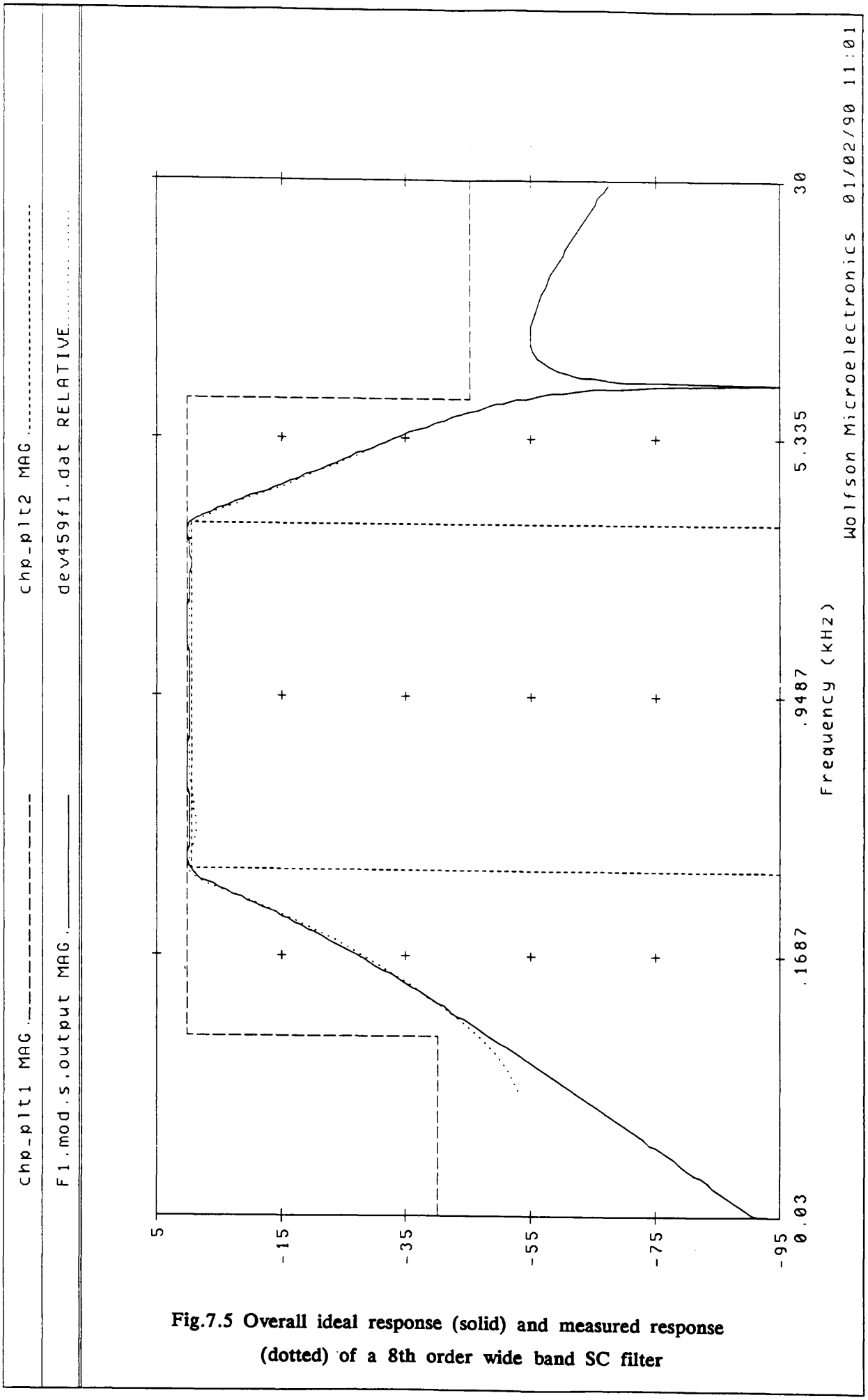


Fig.7.5 Overall ideal response (solid) and measured response (dotted) of a 8th order wide band SC filter

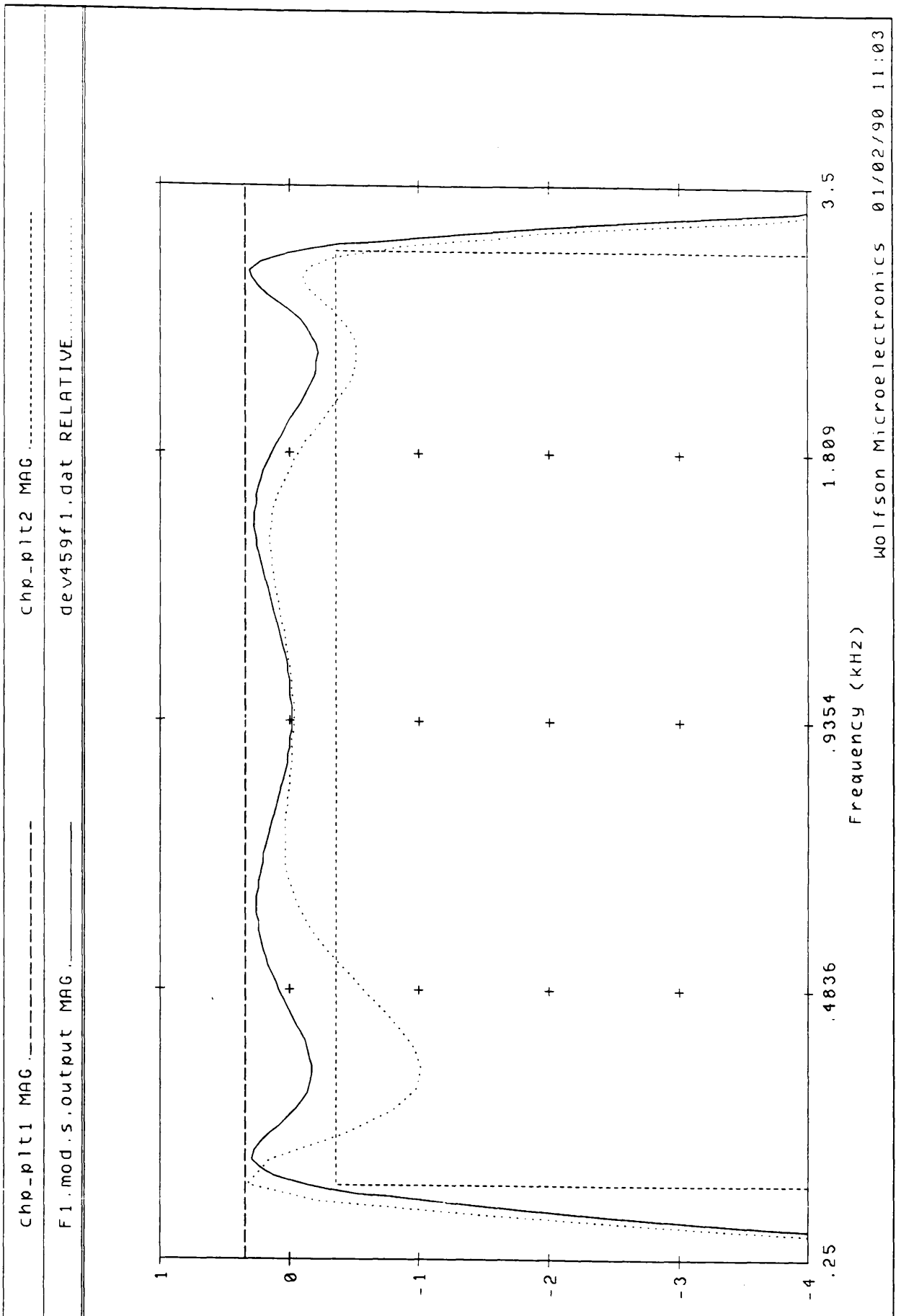


Fig.7.6 Ideal passband response (solid) and measured passband response (dotted) of a 8th order wide band SC filter

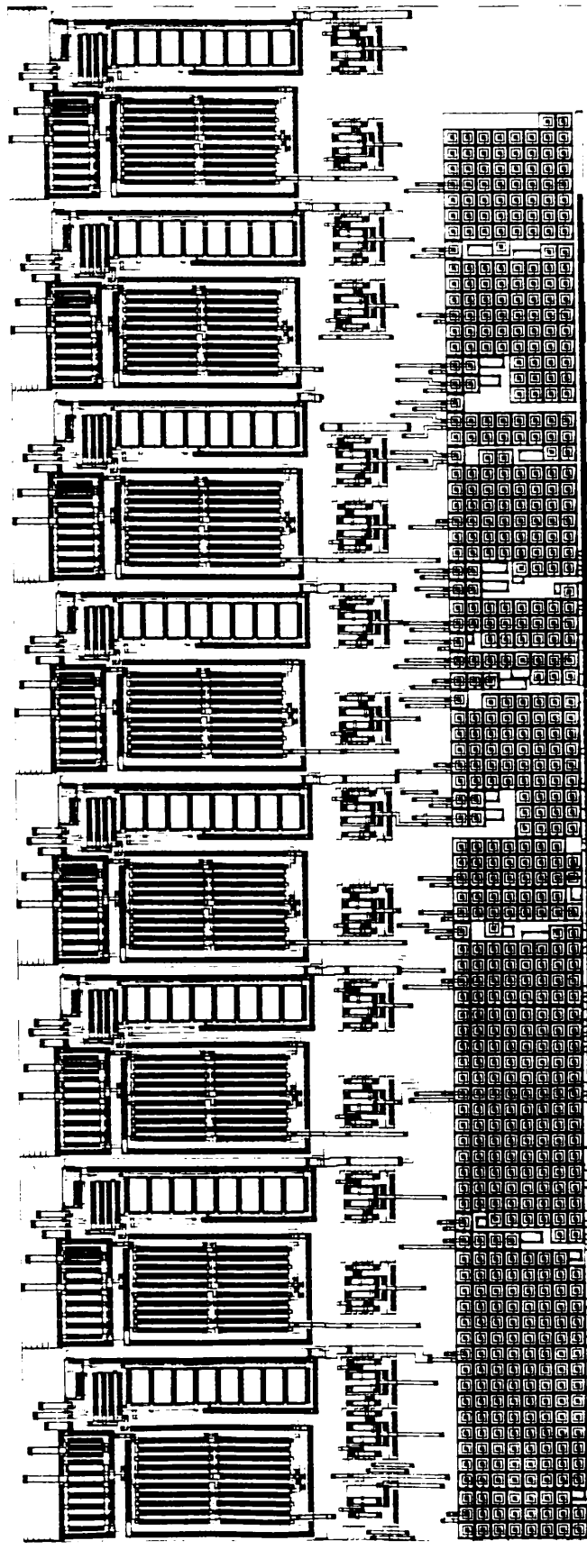


Fig.7.7 Circuit layout of a 8th order mixed LUD– biquad SC filter

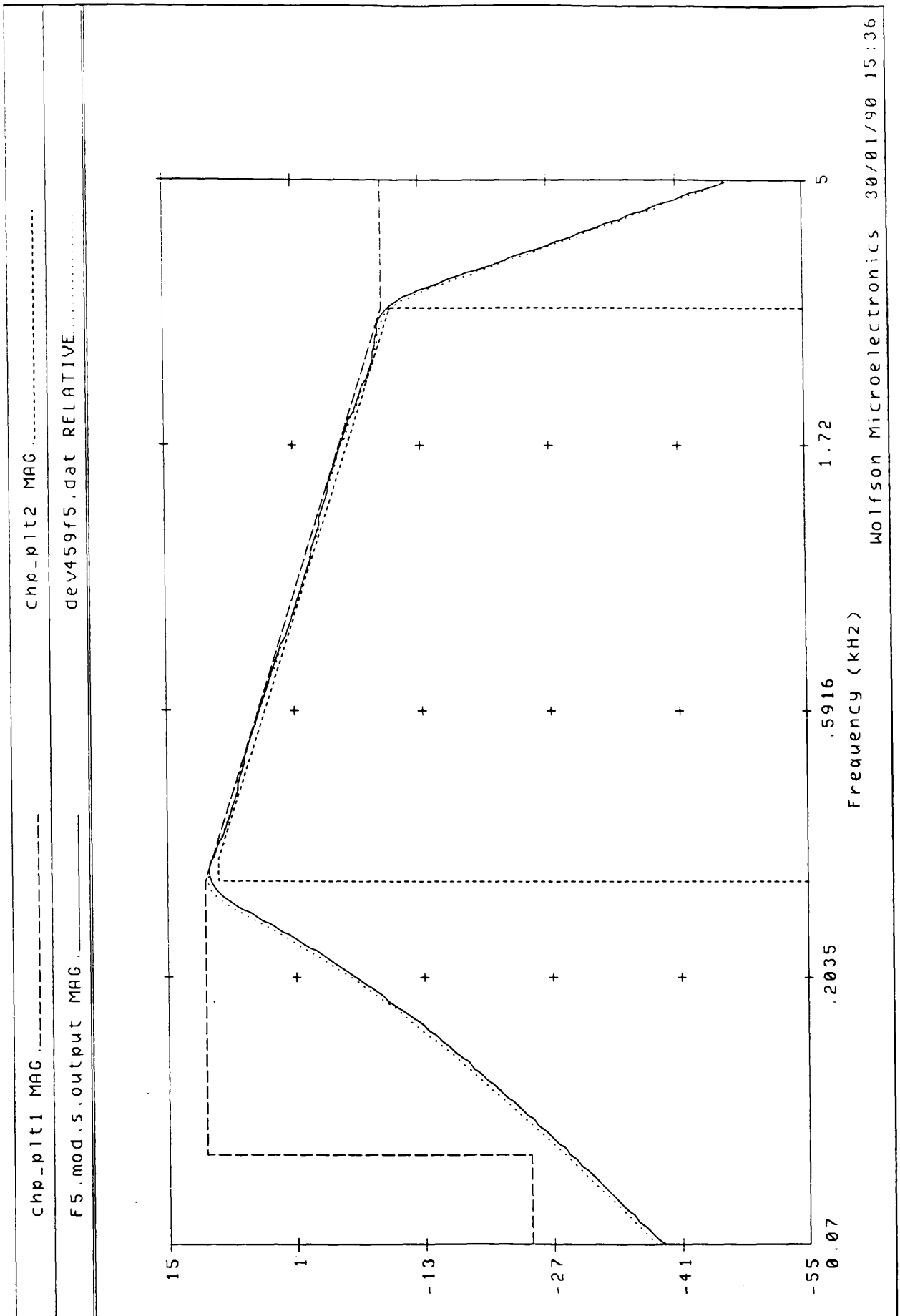


Fig.7.8 Overall ideal response (solid) and measured response (dotted) of a 8th order sloping shape SC filter

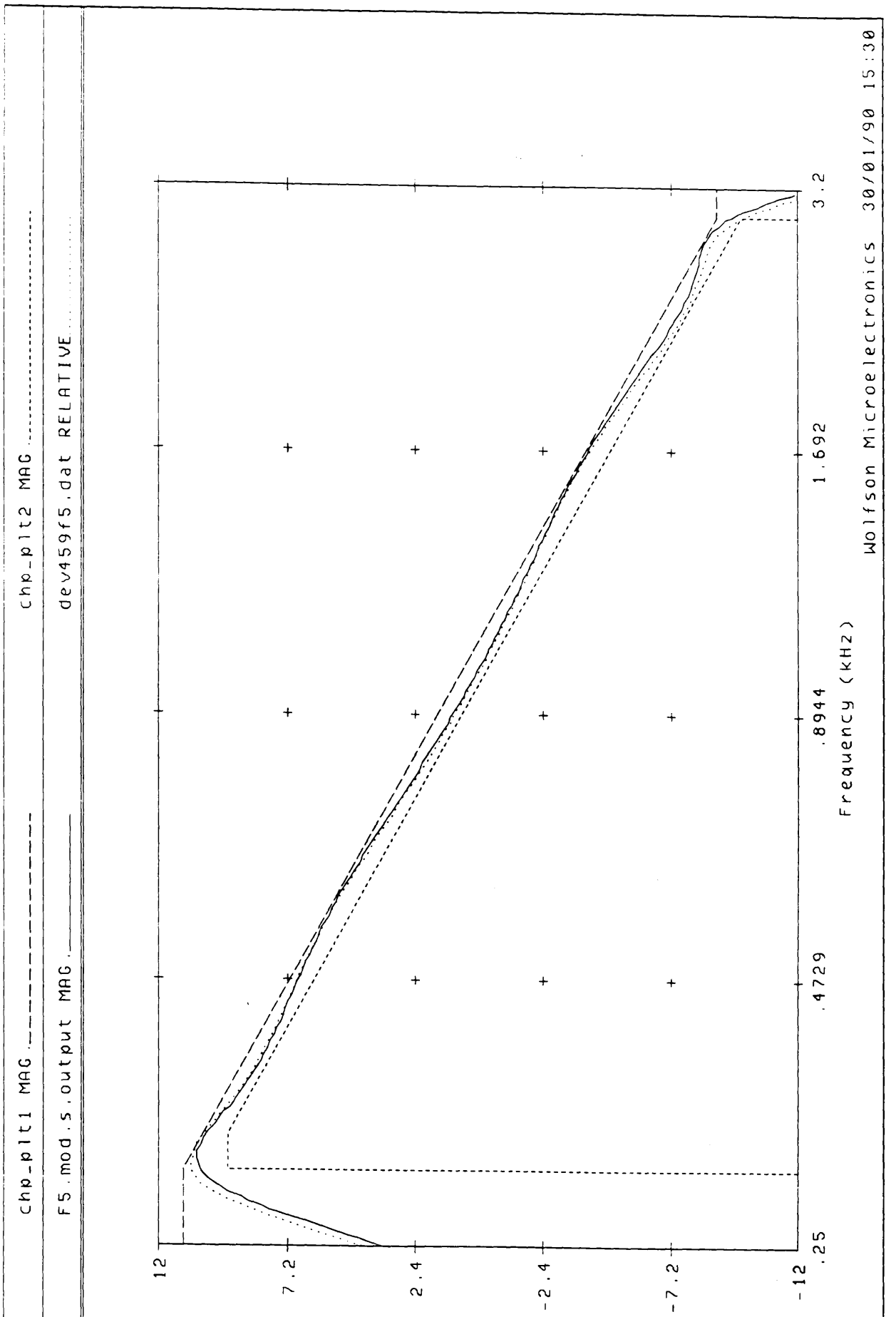
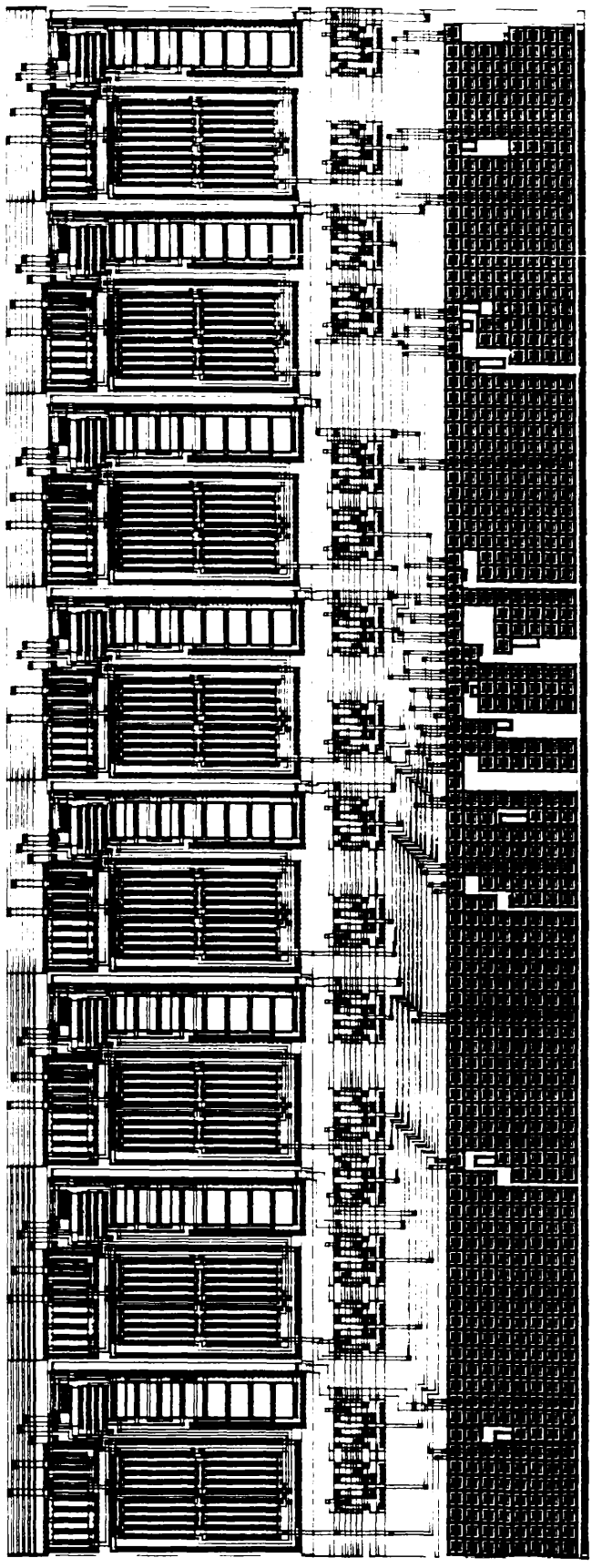


Fig.7.9 Ideal passband response (solid) and measured passband response (dotted) of a 8th order sloping shape SC filter



OWNER: rob FILE: robf5.plt SCALE 156:1 REF: SCRATCH DATE: Jan 12 15:47 Copyright (c) WM 1987

Fig.7.10 Circuit layout of a 8th order biquad SC filter

CHAPTER 8

CONCLUSIONS AND SUGGESTIONS FOR POSSIBLE FURTHER WORK

8.1 DISCUSSION OF THE RESULTS

8.2 SUGGESTIONS FOR POSSIBLE FURTHER WORK

8.1 DISCUSSION OF THE RESULTS

Ladder networks have long been known as the best choice for high performance filter design, whether they are implemented by passive, active or digital circuits. However, various factors have detracted from the success of integrated ladder filters; they have a complicated design procedure, the filter structures can be irregular and can have certain undesirable properties such as the delay– free– loops and large capacitance spread for SC circuits.

The objective of this work was to establish a unified theory and methodology for high performance integrated filter design. A new mathematical framework has been employed which introduces matrix methods into the field of filter synthesis. Matrix methods are already central to control system design, and so it is natural to expect that they can be readily applied to filter networks which are, after all, only typical examples of linear systems. Indeed the application of matrix principles from network analysis to network synthesis has yielded a considerably more profound understanding of the properties of ladder structures. A detailed theoretical study of such filters has been undertaken with a view to developing filter structures with improved performance. The success of this work has been proven by test results of commercially fabricated SC circuits. The main accomplishments are summarised below.

After a general introduction in Chapter 1, a theoretical investigation was presented for symmetric matrix polynomial system (SMPS) in Chapter 2, which is a mathematical generalisation of passive circuits, in particular passive ladders. Definitions and criteria were advanced for the simulation of ladders by canonic integrated circuits. The sensitivity and noise behaviour of the SMPSs was assessed by examining their boundedness and pseudopassivity properties. Although the theories are mainly applicable to the case of systems which undergo symmetric deviations of their element values, formulae are also developed for the asymmetric case. However, a rigorous assessment of the distortion caused by the latter effect is still lacking. The low sensitivity and low noise properties of the circuit structures developed in this work were mainly confirmed by computer simulations. Nevertheless, this theoretical study has still many practical implications, such as the assurance that if that stability is maintained, negative elements will not introduce any special sensitivity or noise problems into the systems. This has been proved to be an important statement for later work on simplified circuit structures.

In Chapter 3 a detailed description of the matrix design procedures for active– RC circuits was undertaken. It was shown that ladder type active– RC circuits can be divided into two major families, derived by either left or right matrix decompositions. Combined left and right decomposition methods were also explored. Well– known leapfrog circuits belong to the right decomposition derived structures and coupled– biquads to the left ones. Moreover LU decomposition drawn from numerical methods can be used for more efficient design. A family of very regular structures has been developed for canonical design, which can be applied to nearly all practically used transfer functions. Some special techniques, such as inverse matrix or hybrid matrix methods have also been briefly discussed.

The matrix methods were extended to the SC and digital circuit designs in Chapter 4. A procedure to convert a bilinearly transformed system into a bilinear– LDI type description has been presented, which has the advantages of exact frequency reponse and simpler circuits in both SC and digital realisations. The discussion of matrix design methods was then straightforward by replacing the s^{-1} operators in the active– RC case by a pair of LDI operators. This fact also clearly illustrates the flexibility and conciseness of matrix methods. The property of structural parallelism is important for high performance digital and SC circuits. In the latter it can be interpreted by the presence capacitance– opamp chains which slows the operation of the circuit. A number of techniques were introduced to enhance the parallelism, such as by placing real zeros on the real axis or using matrix scaling. Some statistical results have been presented to provide a full picture of the behaviour of various SC circuit structures. It is shown that in many circumstances ladder type circuits have much better performance than biquad ones. In particular, left– LUD method has demonstrated some very attractive properties for bandpass filter designs.

In Chapter 5 frequency transformation methods were discussed. It was shown that the concept of LDI operators could be generalised into a whole family of operators suitable for different types of filtering. These various operators can be easily implemented by digital circuits, reducing the number of addition and multiplication operations. For SC realisation the frequency transformation methods are found to be efficient in highpass and bandstop type design. A novel second order building– block, the so– called twintor, has been proposed to realise bandstop type operators. In a twintor circuit the switches are operated at the same rate as the sampling frequency (while in an ordinary SC circuit with LDI operators switches are operated at twice the rate of the sampling frequency),

which eases the requirements on opamps as well as other elements such as switches.

Allpass filter design for delay equalisation was considered in Chapter 6. Allpass filters have been traditionally realised as cascade biquads but their high amplitude sensitivity for the high–Q case is a commonly known problem. Based on a decomposition technique for allpass functions, some novel allpass ladder structures have been developed. The main body of an allpass ladder has exactly the same structure as that of a typical ladder filter, apart from being derived from a singly–terminated prototype. Some additional components are required at the input/output stages and it was proved that the amplitude response of the whole allpass ladder is sensitive only to these components and no others. It was further proved that even for these input/output components the relative sensitivity is small and bounded. In SC design the capacitance spreads were shown to be low for ladder type designs.

As described in Chapter 7, a computer software package, PANDDA, has been developed in tandem with this research work. PANDDA incorporates many state–of–the–art filter design techniques and algorithms. In particular, the matrix methods for filter realisation form the core of the package. It was shown that a wide variety of circuits can be handled efficiently in matrix form on computers. Various manipulations of circuit structures, essential to achieve optimal dynamic range, sensitivity and component spread, become very simple and regular by the matrix techniques. The software has been successfully used in integrated filter design, some of which have been fabricated. The measured results have been shown.

8.2 SUGGESTIONS FOR POSSIBLE FURTHER WORK

With respect to the theoretical investigation of the symmetric matrix polynomial system (SMPS), it would be of interest to investigate the following problems,

1. As has been proven in the Chapter 2, amplitude distortion caused by symmetric deviations will reach zero value at the maximum signal transmission points and it can be expected it will kept small in the whole passband where ρ is small. Although, a concise formula has been developed to assess the effect asymmetric deviations, no definite conclusion is reached to assert that the resulting

distortion will be small for a SMPS. Nevertheless many examples in Chapter 4 indicate that the amplitude sensitivity of an SMPS is really low, even in the asymmetric case. However a more rigorous reasoning is required to confirm when and why this low sensitivity property can be achieved.

2. In Chapter 2 a wave variable based procedure is given to develop limit cycle free digital realisations. It is known that wave type digital ladders are more complicated than LDI ones. Although there is no proof that a LDI based structure can be made free from limit cycles, some observations suggest that wave and LDI ladders have nearly the same noise behaviour. The LUD methods presented in this research greatly simplify and regularise the design procedure of 'exact' LDI ladders. It would seem interesting to, either by theoretical induction or by experiments, examine the noise behaviour caused by signal quantisations. This remains a future work to complete the research on LUD type digital filters.

With respect to matrix methods for integrated filter design, two possible directions for further research are suggested,

3. Non– minimum phase systems may lead to efficient design for combined amplitude– group delay specifications. It has been indicated that some 30% of the components can be saved if the amplitude and all– pass parts in a whole system are merged by employing non– minimum phase functions. All the circuit structures, apart from allpass ladders, derived in this work are based on the simulation of terminated reactance prototypes and the zeros are restricted to be on the imaginary axis. However, it has also been shown that, in the derivation of all– pass ladders, non– minimum phase functions can also be realised by adding a single feedthrough branch directly from the input to the output. This technique could be generalised to construct a multi– input system, removing the constraint of imaginary axis zeros. However, the prototype synthesis procedure must be generalised to produce prototypes realising arbitrary numerators.

4. The combined left– and right– decomposition methods have already been shown to be possible for ladder design. It is observed that the right LU and UL decomposition method has good sensitivity properties at low frequency but that the left LU and UL decomposition methods behave better at higher frequency. This suggests that a combination of right and left LUD methods would possibly inherit the best qualities of the two. However this not the case as shown by the statistical results in Chapter 4. It seems that this is caused by the large

capacitance spread of F− type damping (capacitor C_{21} in Fig.4.7a and C_{22} in Fig.4.7b) at termination stages. If some technique can be discovered to allow both E− type damping (or possible both F− type damping) without extra cost of compononts, it is expected that total capacitance and sensitivity can be further improved.

With respect to frequency transformation methods some further topics on twintor type circuits are of interest,

5. Twintor type circuits offer a reduction in the switch speed which may find application in high− speed signal prcessing. In a twintor section the output signal is sampled alternately between two opamps. This in fact follows the same principle as some polyphase digital networks which have found wide application in reduction of the operation speed in digital circuits. It is expected that the principle of twintor circuits can be generalised and may find application in non− bandstop type filter design. Also the high sensitivity problem of twintor circuits remains to be explained and solved.

With respect to allpass ladder filter design there is a direct application as outlined below,

6. It is known that some amplitude transfer functions can be expressed as the summation of two all− pass functions [91]. This has led to an interesting category of digital filter structures, often referred to as wave− lattice structures because each subnetwork is normally realised by wave digital building blocks. However wave type realisation is not efficient in active− RC or SC implementations. The advent of LDI type allpass ladders provides a very promising means for active− RC and SC lattice circuit realisation.

With respect to the development of computer aided integrated circuit design the following possible research work is indicated

7. In its present state, PANDDA is already a useful tool for an analogue filter designer with a certain level of experience. The digital filter synthesis part of PANDDA still remain to be developed. It is expected that matrix principles can be also used to incorporate LDI, wave and lattice type digital ladders and provide fast algorithm partition and analysis. Recent developments on GaAs SC filters have also brought many interesting topics into research [31,41]. Improvement of PANDDA to handle the many special problems met in GaAs circuit design, such

as low opamp gain and high switch resistance would make it very helpful for the research in this field. Also with some further improvements to the of user–interface and graphical facilities, it could be made much more user–friendly. The present software is arranged as a set of programs which handle the major computational steps in filter design. It relies on the skill of the designer to apply its capabilities most appropriately. However, this knowledge could be built into a more sophisticated expert system which could make recommendations about the best design approach, enabling the designer to reach a quick decision without specialised ability.

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