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DC-DC and AC-DC Converters Based on Three-Phase DC-DC Topologies

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Abstract

Power electronics is the field of electrical engineering that uses power semiconductor devices along with passive elements such as inductors, capacitor and transistors to convert electrical power that can be generated by a source to a form that is suitable for user loads. The main focus of this thesis is on the development of new DC-DC and AC-DC topologies that are based on three-phase DC-DC converters. Three-phase DC-DC converters take an input DC voltage, convert it into a high-frequency AC voltage that is then stepped up or down, then rectify and filter this voltage to produce an output DC voltage. They are implemented with a high-frequency three-phase transformer in their topology rather than a single-phase transformer. These converters are very attractive over other topologies that have a single-phase transformer in their topologies for several reasons. First, just one three-phase DC-DC converter can be used instead of using three DC-DC converters in parallel for particular applications; this advantage is especially attractive for higher power applications. In addition, by using three-phase DC-DC converters, the ripple of the source current is significantly reduced and that means less filtering is needed. Moreover, the components of the converter will have less current stress because current is split among three-phases.

In this thesis, new DC-DC and AC-DC converters that are based on three-phase DC-DC topology are proposed. The proposed converters use fewer active switches than other previously proposed converters of similar type, thus resulting in lower cost and simpler operation. For each of the proposed converters, its steady-state characteristics are determined by mathematical analysis and procedure for the design of key converter components is developed. The feasibility of each proposed converter has been confirmed with results that have been obtained from experimental prototypes. For one of the proposed converters, a comparison between the operation of one of the proposed converters operating with traditional silicon devices (Si) and that with the converter operating with new silicon-carbide devices (SiC) was made to examine its performance with both types of devices.

Keywords: DC-DC power conversion, renewable energy systems, AC-DC conversion, ZVS, single-stage converters

Summary for Lay Audience

Power electronics has a significant impact in a wide spectrum of electrical applications, from personal electrical devices such as cellphones and laptops to large industrial applications such as renewable energy and automotive applications. In general, power electronics is the field of electrical engineering that uses power semiconductor devices along with passive elements such as inductors, capacitor and transistors to convert electrical power that can be generated by a source to a form that is suitable for user loads. The input source can be utility voltage, a battery, solar panels, fuel cells, electric generators, etc. The load can be a motor, telecommunications equipment, medical equipment, a battery, etc. There are four basic types of power converters: -AC-DC, DC-DC, DC-AC and AC-AC- depending on whether the source is AC or DC and whether the load is AC or DC.

The main focus of this thesis is on the development of new DC-DC and AC-DC topologies that are based on three-phase DC-DC converters. These converters are very attractive over other topologies that have a single-phase transformer in their topologies for several reasons because the converter components have less stress, their input and output currents can be closer to being ideally DC, and they are less expensive to implement than three separate DC-DC converters. In this thesis, new DC-DC and AC-DC converters that are based on three-phase DC-DC topology are proposed. For each of the proposed converters, its steady-state characteristics are determined by mathematical analysis and procedure for the design of key converter components is developed. The feasibility of each proposed converter has been confirmed with results that have been obtained from experimental prototypes.

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Acronyms

AC :	Alternate Current
AVG:	Average Value
CCM:	Continuous Current Mode
DC:	Direct Current
DCM:	Discontinuous Current Mode
EMI:	Electro Magnetic Interference
GaN:	Gallium Nitride
PF:	Pwer Factor
PFC:	Power Factor Correction
PWM:	Pulse Width Modulation
RMS:	Root Mean Square
Si:	Silicon
SiC:	Silicon-Carbide
THD:	Total Harmonic Distortion
ZCS:	Zero Current Switching
ZVS:	Zero Voltage Switching

Abbreviations

C_o	Output Capacitor
C_c	Clamping Capacitor
D	Duty Cycle
D_f	Flyback Duty Cycle
D_x	Diode x
D_{cx}	Clamping Diode x
D_{ax}	Auxiliary Diode x
f_s	Switching Frequency of Main Switches
f_{sf}	Switching Frequency of Fyback Switch
G	Gain
i_{DCx}	Current Through Clamping Diode x
I_{in}	Input Current
I_{Lm}	Magnetizing Current
I_o	Output Current
I_{px}	Current through the Primary of Main Transformer in Phase x
$I_{S,avg}$	Switch Average Current

$I_{S,pk}$	Switch Peak Current
$I_{S,rms}$	Switch RMS Current
L_{in}	Input Inductance
L_x	Inductor x
L_{kx}	Leakage Inductor x
L_m	Magnetizing Inductor
L_o	Output Inductor
N, n	Transformer Turns Ration
P_{in}	Input Power
P_o	Output Power
P_{fb}	Flyback Power Rating
$R_{ds\text{-}on}$	Resistance Between Drain-Source in MOSFET when Switch is ON
R_o	Output Resistive Load
S_x	Switch x
t	Time
V_{in}	Input Voltage
V_o	Output Voltage
$\overline{V_o}$	Voltage Across Primary Side of Main Transformer

V_c, V_{Cc}	Voltage Across Cc
V_{Cmin}	Minimum Voltage Across Cc
V_{Cmax}	Maximum Voltage Across Cc
Z_o, Z_1	Characteristic Impedance
Δ_{iL}	Inductor Current Ripple
Δv_o	Output Voltage Ripple

Chapter 1

1 Introduction

1.1 Introduction

Power electronics is the field of electrical engineering that is concerned with the use of power semiconductor devices to convert electrical power from the form that can be used by a source to the form needed by a load. The input source can be utility voltage, a battery, solar panels, fuel cells, electric generators, etc. The load can be a motor, telecommunications equipment, medical equipment, a battery, etc. Power semiconductor devices are implemented along with passive elements such as inductors, capacitor and transistors in power converters. Although all these elements can be arranged in many ways, in many different converter structures called topologies. There are four basic types of power converters: - AC-DC, DC-DC, DC-AC and AC-AC - depending on whether the source is AC or DC and whether the load is AC or DC.

The focus of this thesis is on three-phase DC-DC converters. Although there is no phase associated with DC sources and loads, the term ‘three-phase DC-DC’ comes from the fact that DC-DC power conversion is typically done by performing DC-AC conversion first then AC-DC conversion. Such an approach is needed if a DC input voltage is to be stepped up or stepped down. As this cannot be done directly with a transformer (unlike AC), what is needed is an intermediate AC voltage produced from the DC source that can be stepped up or down by a transformer then rectified to produce the desired DC voltage. This AC voltage can be single-phase or three-phase and thus fed to a single-phase or three-phase transformer. What the term “three-phase DC-DC” really means is a DC-DC converter that has a three-phase transformer in its topology. It should be noted that the three-phase AC voltage that is applied to the transformer does not have a frequency of 60 Hz, but has a much higher frequency, in the tens of kHz, so that voltage can be stepped up or down using a much smaller transformer.

Three-phase DC-DC converters are attractive because they have several advantageous features over conventional DC-DC converter that have a single-phase transformer in their

topologies. One advantage is that instead of using three DC-DC converters in parallel for particular applications, just one three-phase DC-DC converter can be used; this advantage is particularly attractive for higher power applications. Another advantage is that the input current ripple can be significantly reduced. Current ripple is the AC component that appears on a DC waveform and is a source of power losses that can reduce power conversion efficiency. By using three-phase DC-DC converters, the ripple current of each individual phase can be reduced considerably so that the overall current coming out of the DC source has lower ripple and less thus filtering is needed. A third advantage is that the current stresses on converter components are lower than those found in single-phase DC-DC converters as current is split among three phases.

Three-phase DC-DC converters are attractive for higher power applications. Other applications where three-phase DC-DC converters are attractive are renewable energy applications such as solar power conversion and fuel-cell power converters. Renewable energy sources such as solar cells and fuel cells tend to produce low output DC voltages. The current coming out of these sources can be considerable even for power conversion applications of a few hundred watts because their voltages are low and thus whatever converter is used to convert the low input DC voltage to a higher more practical DC voltage must be able to handle this high current. Since three-phase DC-DC converters are better than conventional DC-DC converters in this regard, therefore they are more suitable for certain renewable energy applications.

In this chapter, basic power electronic concepts that are related to the work performed for this thesis are explained and a literature review of relevant previous work that is related to the thesis topic is performed. The objectives of the thesis are then stated and the chapter concludes with an outline of this thesis.

1.2 Fundamental Concepts

In this section of the thesis, several fundamental power electronic concepts that are related to the thesis are presented.

1.2.1 DC-DC Boost Converters

DC-DC converters may either have a transformer in their topologies, in which case they are isolated converters, or they may not, in which case they are non-isolated converters. If it is needed for a DC voltage to be stepped up and a non-isolated converter can be used, then one way of doing so is the conventional DC-DC boost converter shown in Figure 1.1. As can be seen in Figure 1.1, the converter consists of an input inductor L_{in}, a switch S_w, a diode D and an output capacitor C_o. The load represented by R_o in the figure.

The boost converter works as follows: The converter operates in periodic manner when it is in steady-state. Switch S_w can be on or off during a switching cycle. When switch S_w is on, the input voltage V_{in} is placed across the input inductor L_{in} and the current through it rises. While this is happening, diode D does not conduct current as it is reverse biased and output capacitor C_o supplies power to the load. When the switch is off, diode D conducts the full input inductor current and the capacitor is charged. While this is happening, L_{in} has negative voltage across it as the output voltage is greater than the input voltage and thus the input current falls. If the current falls to zero during the time that the switch is off, then the converter is considered to be operating in discontinuous current mode (DCM).

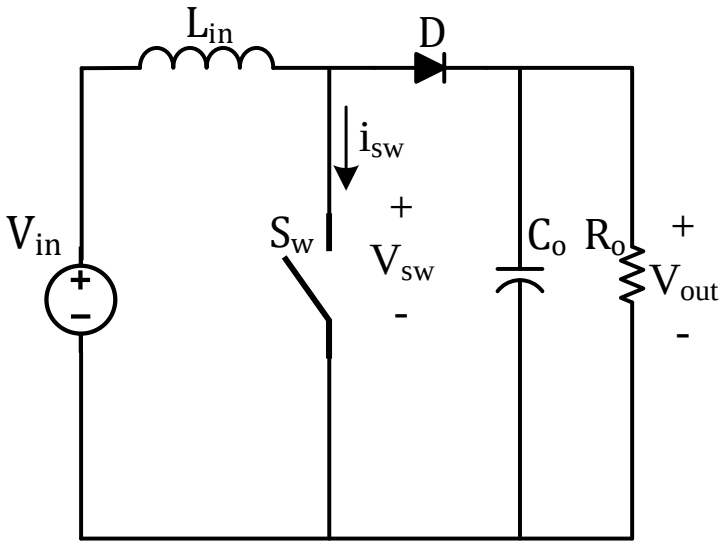


Figure 1.1: DC-DC boost converter

If the current does not fall to zero, then the converter is considered to be operating in continuous current mode (CCM). Current rises again when the switch is turned on at the start of the next switching cycle.

1.2.2 Switching Losses

Ideal power electronic converters are 100% efficient and do not dissipate power while they are performing power conversion. In reality, however, power converters operate with certain power losses, some of these being switching losses. Switching losses in power converters occur whenever a converter switch, such as the switch in the boost converter shown in Figure 1.1, is turned on or off. During a switching transition, there is an overlap between the voltage across the switch and the current flowing through it and it is this overlap of voltage and current that creates the losses as shown in Figure 1.2. These switching losses can be reduced if either the switch voltage or the switch current is made to be zero at the time of the transition. As a result, converter efficiency can be increased if converter switches are operated with either zero-voltage switching (ZVS) or zero-current switching (ZCS). ZVS and ZCS are considered to be forms of soft-switching in the power electronics literature.

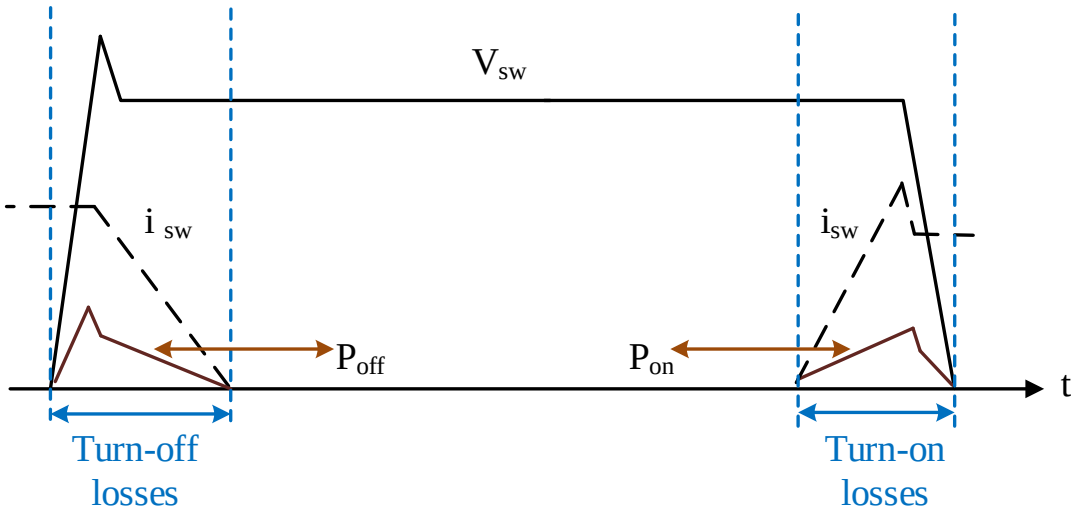


Figure 1.2: Loss of power during hard switching

There are various methods of implementing ZVS or ZCS in power converters. Many of these methods use an auxiliary circuit of some kind, usually connected parallel to the main converter switch(es), that either forces the voltage across the converter switches to zero before they are turned on or diverts the current away from the converter switches before they are turned off. A ZVS turn-off of a switch can be implemented by simply adding a small capacitor across it (or by using the device's output capacitance if it is sufficient) as the capacitor slows down the rate of voltage rise when it is turned off, which reduces the overlap of switch voltage and current and thus reducing switching losses. A ZCS turn-on of a switch can be implemented by adding a small inductor in series with it as the inductor slows down the rate of current rise when it is turned on, which reduces the overlap of switch voltage and current. The auxiliary circuit is activated before a switch is turned on for ZVS or before a switch is turned off for ZCS.

1.2.3 Isolated Single-Phase DC-DC Full-Bridge Converters

DC-DC power conversion can be performed with converters that are more sophisticated than simple converters like the boost converter shown in Figure 1.1. Examples of such converters are isolated DC-DC converters that contain a transformer in their topologies. There are several types of these converters; this section will focus on full-bridge converters having a single-phase power transformer.

Full-bridge converters have four main switches in their topologies and are used in higher power applications (> 400 W). There are two types of single-phase DC full-bridge converters: voltage-fed converters [1] and current-fed converters [2]. Voltage-fed converters have a DC input that is a voltage source of some kind (a source or a bulk capacitor) that supplies power to the four-switch full-bridge; current-fed converters have a current source of some kind (i.e. a bulk inductor). The basic structure of both converters is shown in Figure 1.3.

The voltage-fed converter shown in Figure 1.3(a) consists of four switches $S_{1\text{-}4}$, a transformer with turns ratio n, a diode bridge rectifier at the secondary side of the transformer and an output filter that is made up of components L_o and C_o.

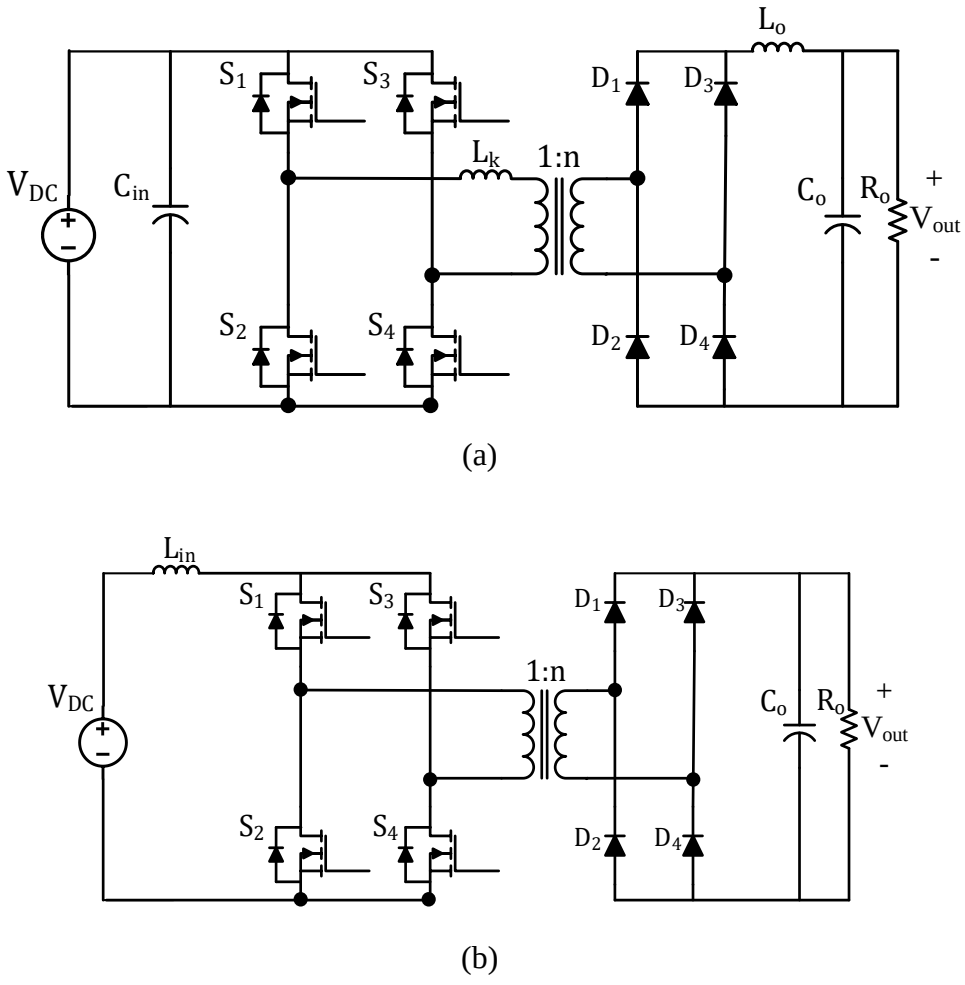


Figure 1.3: Types of DC-DC full-bridge converter (a) A full-bridge voltage-fed DC-DC converter (figure reproduced from [1]). (b) Full bridge current-fed boost dc-dc converter [2]

The way this converter works is as follows: The four main converter switches are turned on and off in a way that produces an AC square voltage across the primary of the transformer. This AC voltage can be stepped down or up (typically down) by the transformer and then rectified by the diode bridge. The output of the diode bridge is fed to a low pass filter that reduces AC harmonics so that a DC output voltage is produced.

The current-fed full-bridge converter shown in Figure 1.3(b) has a topology that is similar to the voltage-fed converter in Figure 1.3(a) except that the output has just a capacitor C_o

as the output filter instead of an inductive-capacitive LC filter. This is because the converter in Figure 1.3(b) is an isolated version of the boost converter shown in Figure 1.1; just as the boost converter has a capacitive output filter, so too does the current-fed converter in Figure 1.3(b). The converter is the dual of the voltage-fed converter and operates in a similar manner. Instead of an AC square wave voltage being fed to the transformer primary, an AC square wave current is fed instead.

The main difference between the two converters is that the current-fed converter can have short-circuit states that are analogous to the turning on of the switch in a boost converter (which makes the input inductor current rise) while the voltage-fed converter cannot have such short circuit states, which would be destructive; instead it has open-circuit states that place zero voltage across the transformer primary.

Full-bridge converters can be operated with auxiliary circuits that can help the four main converter switches operate with soft-switching. Due to the nature of their topologies, auxiliary circuits are needed more for current-fed than for voltage-fed full-bridge converters. This is mainly because the input inductor of a current-fed full-bridge converter sees inductance in the form of the primary transformer. Since one inductance cannot interface with another inductance if they are carrying different currents, there needs to be some path for the current difference to flow through. An auxiliary circuit connected to the converter can provide such a path.

Examples of current-fed full-bridge converters with auxiliary circuits are shown in Figure 1.4. Figure 1.4(a) shows a full-bridge converter with an auxiliary circuit that allows the main switches to operate with ZVS [3] while Figure 1.4(b) shows a full-bridge converter with an auxiliary circuit that allows the main switches to operate with ZCS [4]. As explained in Section 1.2.2, an auxiliary circuit is activated just before certain key switching transitions to ensure soft-switching operation.

1.3 Literature Review

Since the focus of this thesis is on three-phase DC-DC converters, a literature review of previously proposed converters of this type is performed in this section. As with the

single-phase isolated DC-DC converters discussed in the previous section, there are voltage-fed and current-fed converters. The literature review will cover both types of three-phase DC-DC converter.

1.3.1 Three-phase DC-DC voltage-fed converters

The first three-phase DC-DC converter was proposed by Prasad et al. in [5]; the converter is shown in Figure 1.5. This converter consists of six switches, a three-phase transformer a three-phase diode bridge rectifier connected to the transformer secondary and an output LC filter.

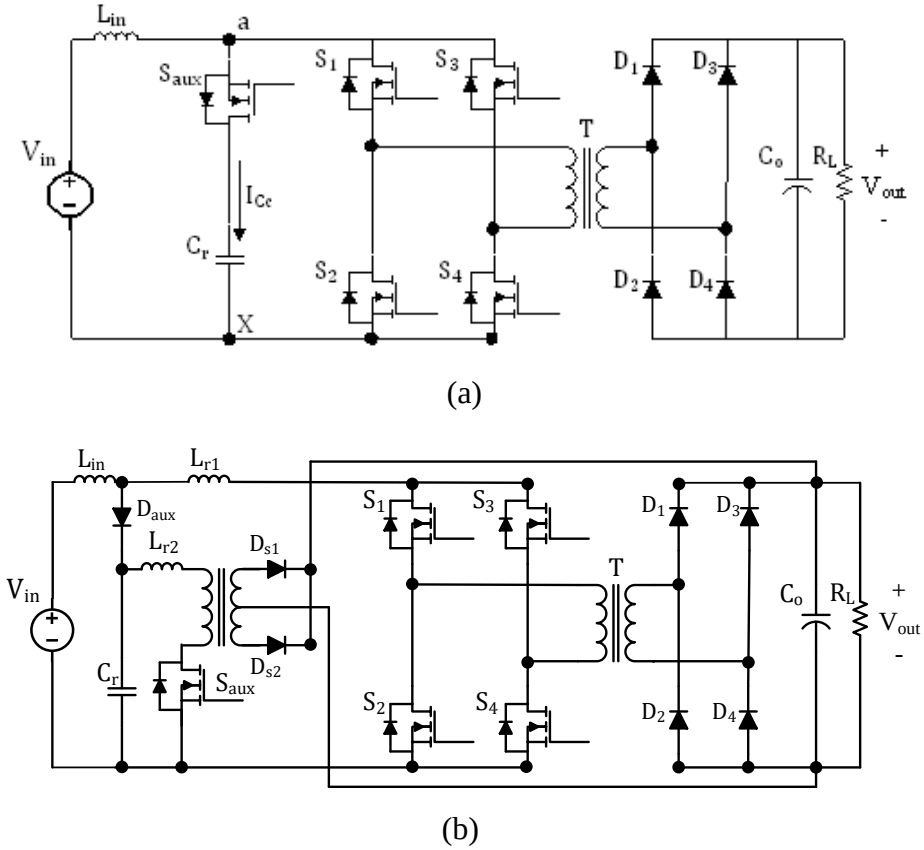


Figure 1.4: Example current-fed DC-DC full-bridge converters, (a) ZVS current-fed full bridge converter [3] (b) ZCS current-fed full-bridge converter [4]

The basic operating principle of this converter is very similar to that of the isolated voltage-fed DC-DC converter discussed in Section 1.2.3 as AC square wave voltages are impressed across the three-phase of the transformer, which are then rectified by the diode bridge then filtered by the LC filter to produce a DC output voltage. The three AC square wave voltages are identical, and each voltage is phase-shifted by 120^{o} with respect to the other AC voltages. The shape and phase of each voltage is achieved by the appropriate turning on and off of the converter switches.

Almost work on the topic of three-phase DC-DC converters has been done by researchers, the literature on the topic is not as vast as what can be found for other types of DC-DC converters such as the forward or flyback converters. The main obstacle is the transformer as more research is needed to improve their design (e.g. implementing all the transformer magnetics on a single core to reduce size) before three-phase DC-DC converters can be widely used in industry. Nonetheless, three-phase DC-DC converters have tremendous potential and research continues to be done on this type of topology.

This particular converter is attractive for a number of reasons compared to using multiple single-phase DC-DC converters as discussed in the Introduction: lower cost, less current ripple and lower component stresses. Most three-phase DC-DC converters are based on this particular topology [6]–[13]. The converter, however, does have a couple of drawbacks. One of these is that the number of semiconductor components in its topology is still considerable. As a result, converters like the one shown in Figure 1.6 [9] have been proposed. This converter is implemented with a secondary rectifier that consists of three diodes and three inductors instead of six diodes. One benefit of doing so, other that reducing the number of diodes in the converter, is that current flowing out of each phase of the transformer secondary flows through only one diode instead of two. Since there are power losses associated with semiconductor devices conducting current, some improvement in converter efficiency can be achieved by using fewer diodes and reducing conduction losses. Although the converter shown in Figure 1.6 may have fewer conduction losses, it still may have significant switching losses.

Another drawback of the converter introduced in [5] is that its switches produce switching losses whenever they are turned on and off; due to this drawback so-called soft-switching resonant converters have been proposed in the literature [7], [8], [12].

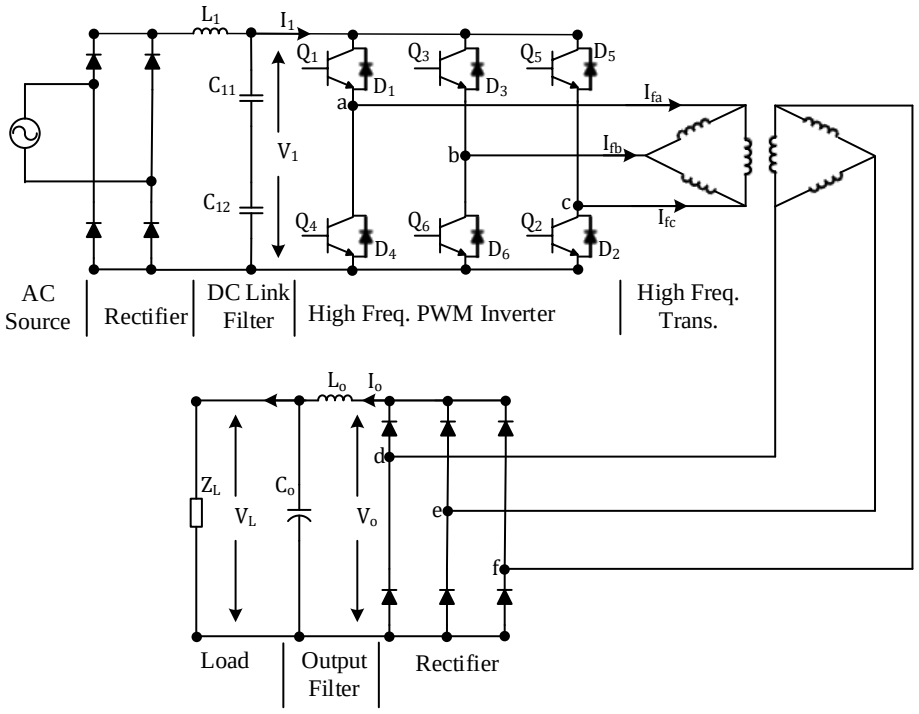


Figure 1.5: Three phase high frequency DC-DC converter proposed in [5]

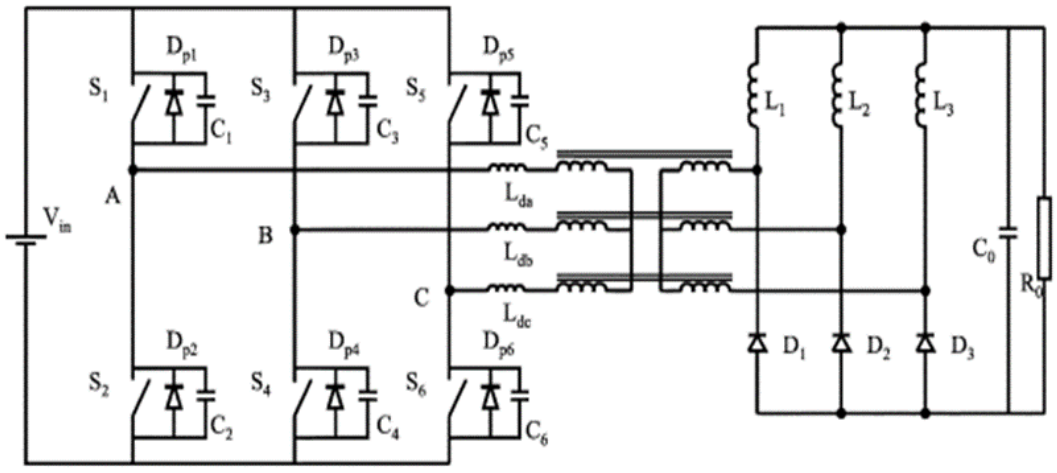


Figure 1.6: Three phase ZVS dc-dc converter with the Hybridge rectifier [9]

Resonant converters use reactive components such as inductors and capacitors as part of passive circuit resonant networks to shape their transformer primary current so that it is sinusoidal. In the case of ZVS resonant converters, the resonant networks are designed so that the primary current lags the primary voltage. This ensures that current is injected in the anti-parallel diode that is part of any active power semiconductor device, along with the switch. This injected current clamps the voltage across a converter switch to near zero voltage so that the switch can be turned on with ZVS and thus with fewer switching losses.

An example of a three-phase resonant DC-DC converter is shown in Figure 1.7. It can be seen that a resonant network has been added to the original three-phase converter shown in Figure 1.5. Although the resonant network helps the converter switches operate with ZVS, the resonant components themselves may be bulky and thus increase converter size and weight.

More recent research such as in [9], [11], [13] has allowed voltage-fed three-phase DC-DC converters to be operated with ZVS without the use of resonant circuits. This has been achieved due to an improved understanding of how these circuits work and the development of new methods for the turning on and off of the converter switches. For even higher power applications, more sophisticated and complex three-phase DC-DC converters can be implemented with more devices. An example of one such converter is the converter shown in Figure 1.8 [10]. It can be seen that this converter has twelve switches instead of six. The switches in this converter conduct less current than do the switches in more conventional six switch topologies. Moreover, as there are more switches, there is more flexibility in how they are turned on and off so that ripple current flowing in the converter can be reduced. For especially high-power applications, this is beneficial as ripple current can be considerable. In addition to lower current ripple, the soft-switching operation of the converter switches can be achieved. This converter, however, is not used for lower power applications due to cost.

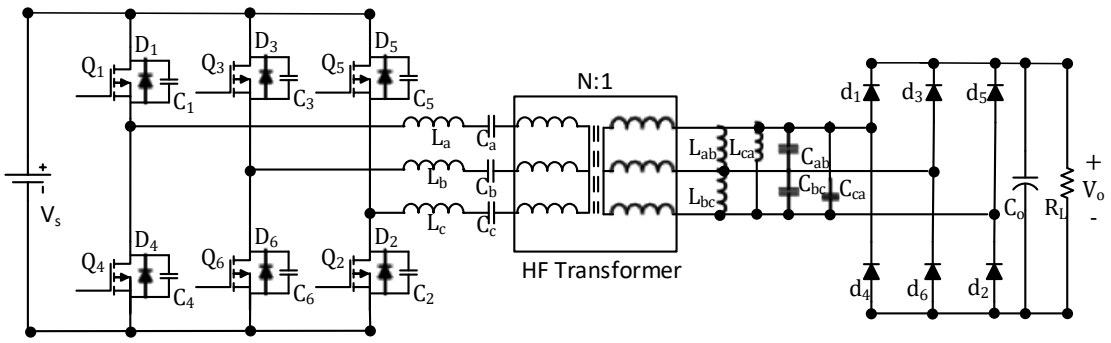


Figure 1.7: Three phase DC-DC resonant converter [12]

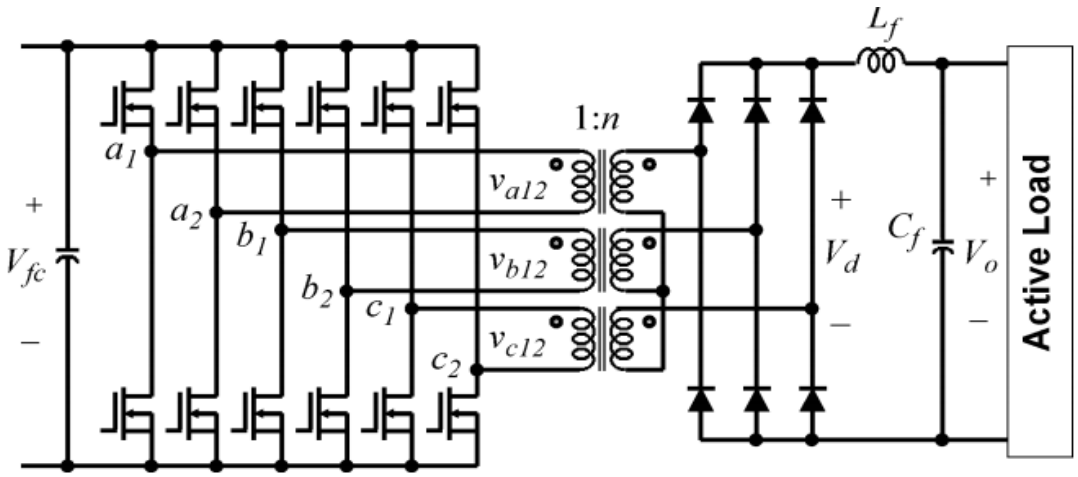


Figure 1.8: Six-leg three phase high power DC-DC converter [10]

1.3.2 Three-Phase DC-DC Current-Fed Converters

Current-fed converters are the other type of three-phase DC-DC converter. These converters are preferable for applications where the output voltage needs to be higher than the input voltage, as they are like the boost converter described in Section 2.1, and for applications where the input current is high as current can be distributed among the three-phases in a way that reduced input current ripple.

In 2005 a three-phase current-fed DC-DC converter was proposed by Oliveira and Barbi in [14] and is shown in Figure 1.9. It consists of three switches, three inductors, a three-phase high frequency transformer, a three-phase diode bridge rectifier and an output capacitor that acts as a filter. The secondary output section of the converter is similar to

that of the single-phase current-fed DC-DC converters discussed in Section 1.2.3 except that a three-phase diode bridge is used instead of a single-phase bridge. The primary section has three inductors each carrying about the same amount of current, but the ripple in each current is 120^o out of phase with the ripple in the other currents so that the use of a bulky input inductor is avoided. The converter switches are operated in a way that ensures square wave AC currents are fed to the three-phase transformer; the input inductor currents rise and fall during any particular switching cycle.

A passive circuit consisting of diodes D_{s1}-D_{s3} and resistor R_s and C_s is added to the converter to suppress or "snub" and voltage spikes that may appear across the switches when they are turned off. What the passive snubber circuit does is that it provides a path for current to flow through when a switch is turned off, thus avoid a situation when inductive current is forced through a switch, which can be destructive.

The main drawback of the converter shown in Figure 1.9 is that its switches do not operate with soft-switching. A number of soft-switching three-phase current-fed DC-DC converters have been proposed [15]–[22] with one of the earliest being the converter shown in Figure 1.10. This converter is essentially the three-phase version of the single-phase isolated current-fed DC-DC converter shown in Figure 1.3(b). It can be seen that it consists of six primary switches with an auxiliary circuit consisting of switch S_c and capacitor C_c connected across them in parallel. The converter can operate with ZVS due to the auxiliary circuit, but it has only one phase and thus one input inductor instead of three. This inductor must be very bulky in order to reduce ripple current and this converter is more suited to higher power applications with relatively lower input current.

A way of combining the most attractive features of the converters shown in Figure 1.9 and Figure 1.10 is the converter shown in Figure 1.11. This converter has three main power switches and three inductors like the converter in Figure 1.9, but with an auxiliary circuit that can help its main switches operate with ZVS. The converter operates in the same way as the converter shown in Figure 1.9 except that the auxiliary circuit is activated whenever one of the main switches is about to be turned on. The auxiliary circuit consists of three active switches of lower power rating than the main switches and

a capacitor. Since the converter has three phases, an auxiliary switch is needed for each phase unlike the converter shown in Figure 1.10, which has only one input phase and thus requires only one auxiliary switch. The converter, however, must still be implemented with six active switches.

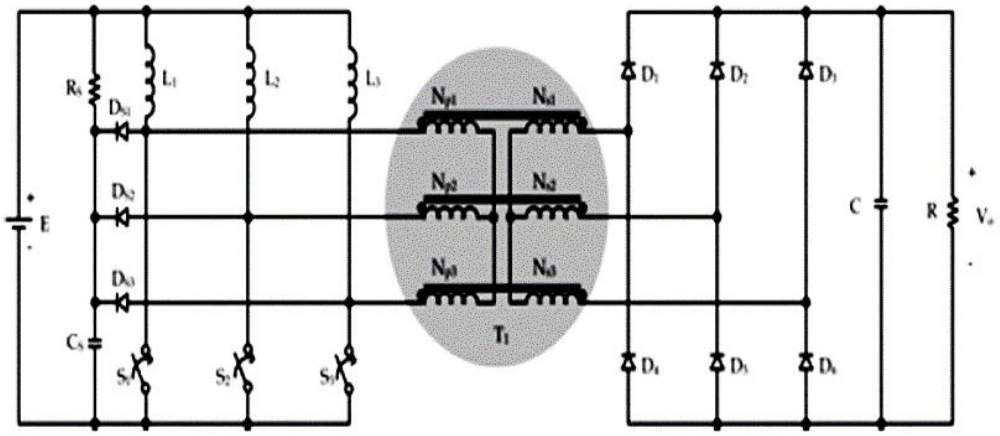


Figure 1.9: Three-phase current-fed DC/DC converter produced from [14]

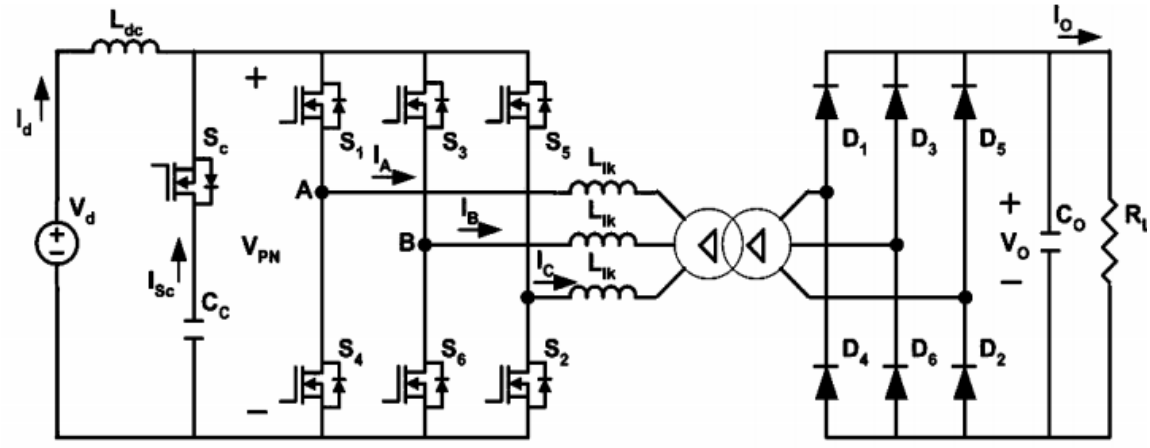


Figure 1.10: Three-phase current-fed DC/DC converter with single input inductor and active clamp [16]

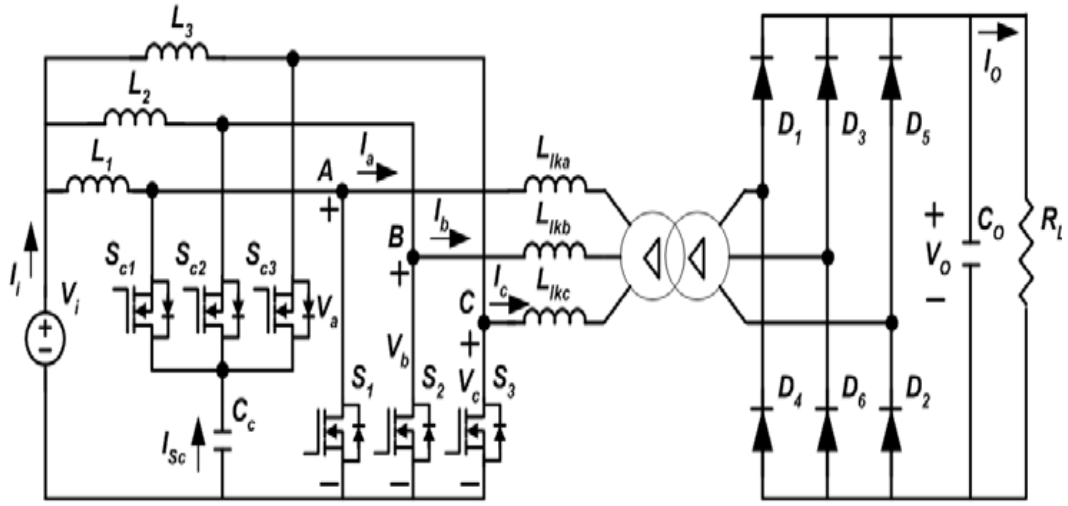


Figure 1.11: Three-phase current-fed DC/DC converter with three input inductors and auxiliary circuit produced from [15]

1.3.3 AC-DC Converters

AC-DC power conversion typically involves the use of two power converters: an AC-DC front-end converter followed by a back-end DC-DC converter[23]–[28]. The AC-DC converter is usually some sort of boost converter that is implemented with power factor correction (PFC) to satisfy regulatory agency requirements on harmonic content. While the AC-DC converter is converting AC utility grid voltage to a DC voltage, it is also shaping the input current so that it is sinusoidal and in phase with the input voltage. The DC-DC converter is usually some sort of flyback or forward converter for lower power applications, some sort of half-bridge converter for medium power applications, and some sort of full-bridge converter for higher power applications. The DC-DC converter converts the output of the front-end converter into the desired output voltage.

Although two-stage power conversion is popular, it can also be expensive as it requires two separate converters with two separate controllers to be implemented. The cost becomes even higher if additional switches are needed. For example, the interleaving of AC-DC boost converters is popular as a means of reducing input current ripple [29]–[35], but its benefits come at the cost of more boost converter switches and diodes as shown in Figure 1.12. Similarly, three-phase DC-DC converters that use three-phase transformers

in their topologies can produce lower output current at higher harmonic frequencies, but such topologies generally need to be implemented with six switches, instead of the typical four switches used in conventional full-bridge topologies as presented in Section 1.3.1 [5]–[13]. An example of a two-stage converter with the AC-DC section implemented with a three interleaved boost converter and the DC-DC section implemented with a three-phase DC-DC bridge converter is shown in Figure 1.13.

Due to the cost and size of two-stage AC-DC converters, single-stage converters – converters that use just one power converter to convert AC input voltage into DC output voltage – have been proposed by power electronics researchers (i.e.[36]–[40], [41]–[45], [46]–[53]. Such converters can be synthesized by combining an AC-DC front-end converter with a DC-DC back end converter, then eliminating redundant components. In addition to having fewer power components, single-stage AC-DC converters are typically implemented with just a single controller to regulate the output voltage instead of two controllers, one for each of the two converter stages, thus further decreasing cost. Although many lower power flyback and forward-based AC-DC single-stage converters have been proposed, considerably fewer higher power AC-DC single stage converter have been. The higher power AC-DC single stage converters that have been proposed have at least one of the following drawbacks:

- The input current in the converter is discontinuous and has high current peaks; this can lead to higher component stresses and more EMI noise. The reason why the converter must operate with discontinuous input current is that the converter operates with just a single controller and with a fixed duty cycle over the entire AC input line period as the converter is simultaneously performing DC-DC conversion. Since the AC input current is not controlled, it must be made to be discontinuous so that it becomes a train of triangular pulses with their amplitudes following the shape of the sinusoidal input voltage [36], [38], [39], [42], [44], [47], [48].

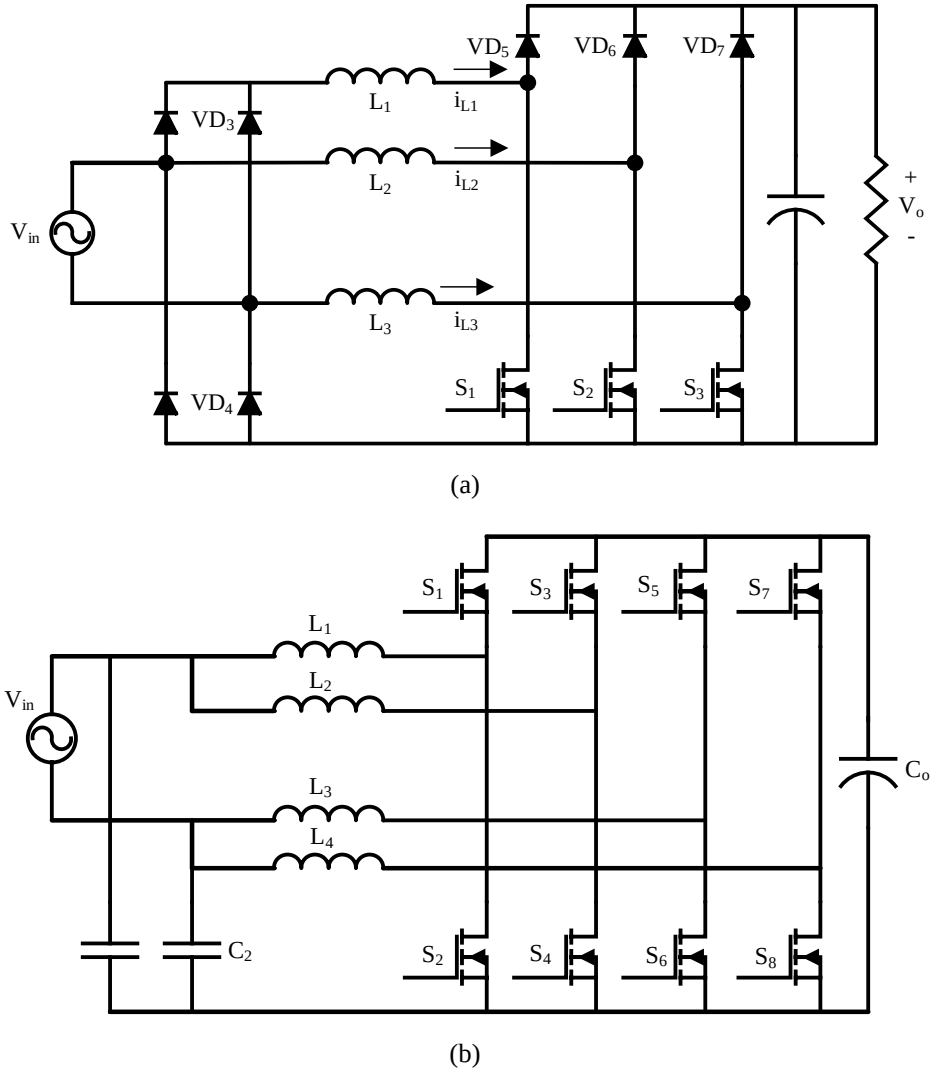


Figure 1.12: (a) Hybrid interleaved parallel AC-DC boost converter [35] **(b) Differential interleaved AC-DC boost converter** [36]

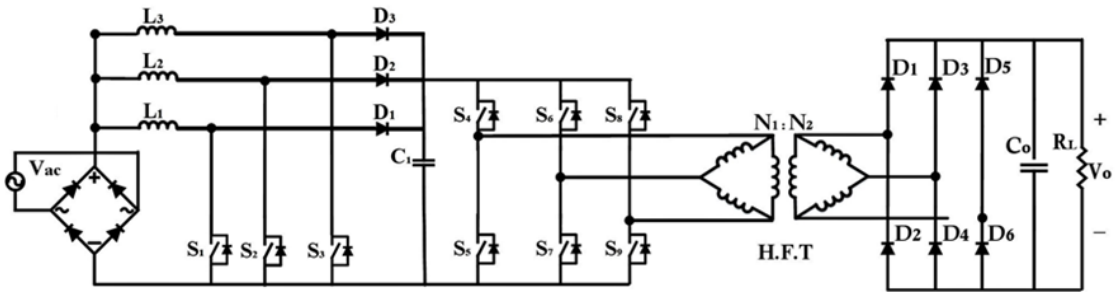


Figure 1.13: Two-stage AC-DC converter with three-phase input interleaving

- The converter switches do not operate with zero-voltage switching (ZVS) and thus have switching losses that can lower their efficiency. Moreover, the suppression of voltage spikes caused by the interaction of transformer leakage inductance and switch output capacitance is an issue in some converters and sophisticated snubber circuits are needed to suppress them [36], [44], [48]–[51].

- Although the converter has fewer components that a two-stage converter, it remains expensive and bulky [38], [39], [42], [46].

- They are implemented with three separate ac–dc single-stage modules, which increase cost and introduce issues related to the synchronization of all three modules [52].

- Sophisticated or non-standard methods must be used to control the converter. For example, resonant converters that need that need to be controlled using variable switching frequency control methods [37], [43], [53].

1.3.4. High Gain DC-DC Converter

There are a number of applications that require power converters that can convert a low DC source voltage into a much higher DC output voltage. A common application where such power conversion is needed is for renewable energy systems such as the one shown in Figure 1.14.

In this system, input DC voltage is provided either by solar panels or fuel cells. The voltage obtained from such renewable power source is typically very low (< 50V) and needs to be stepped up considerably in order to feed downstream converters and loads. In the system diagram shown in Figure 1.14, inverters that interface with the grid, DC loads or DC-DC converters are supplied by a high DC voltage bus that was stepped up from the low voltage DC source by some sort of boost converter.

The boost converter is typically either a single-switch PWM boost converter or a full-bridge converter [54]–[61]. Although these converters have an input inductor that can

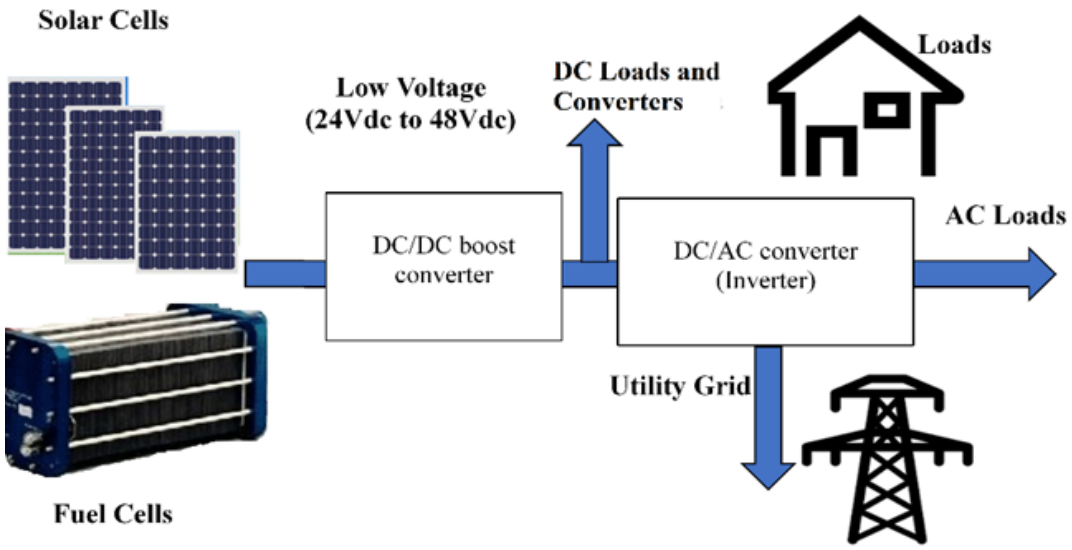


Figure 1.14: Block diagram of a renewable energy system

smooth out input current, considerable input current ripple can still be produced unless an extremely large input filter inductor is used. The ripple can create problems for the DC sources, especially those like batteries, PV cells and fuel cells that have issues with lifetime.

Another issue is that although single-switch PWM boost converters and current-fed full-bridge boost converters can boost input DC voltage, their gains are not sufficiently high for renewable energy applications such as what is shown in Figure 1.14. As a result, many high gain DC-DC converters have been proposed in the literature[62], [63], [72], [64]–[71]. These converters achieve high gain by cascading a boost converter so that they are quadratic converters, using coupled inductors, or using voltage multiplier cells. an example of these converters is shown in Figure 1.15. These converters, however, have at least one of the following problems:

- Their topologies have high conduction losses because current is forced to flow through a number of components in series in order to achieve high voltage gain.
- Their switches are subjected to high voltage spikes unless additional components are added to the circuit to suppress these spikes.

- Their components are subjected to high voltage and/or high current peak stresses.
- Input and output current ripple still remain an issue.

Three-phase DC-DC boost converters with input phases coming out of the DC source have less input current and output voltage ripple as the equivalent converter frequency is three times more than the switching frequency and their switches conduct less current than does the switch in a conventional PWM boost converter.

Current ripple is an important consideration for batteries as exposure to high current ripple can reduce their lifetime. Although they have less current ripple and are suitable for higher power applications due to their multi-switch topologies, little research has been done on increasing the gain of three-phase DC-DC converters and only a few high-gain three-phase DC-DC converters have been proposed [22], [73]–[76]. An example of these converters is shown in Figure 1.16. Although these converters address the issue of high current ripple, they still have some of the above-mentioned drawbacks.

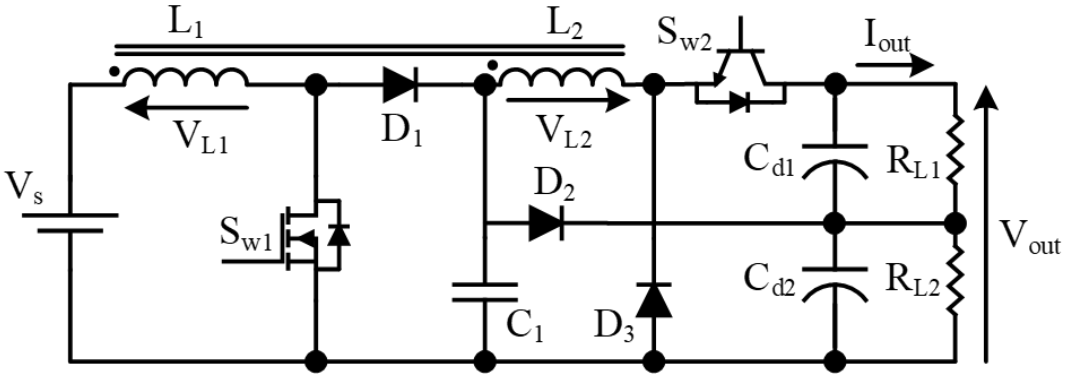


Figure 1.15: Coupled inductor-assisted two quadrant high frequency PWM chopper type DC-DC converter [62]

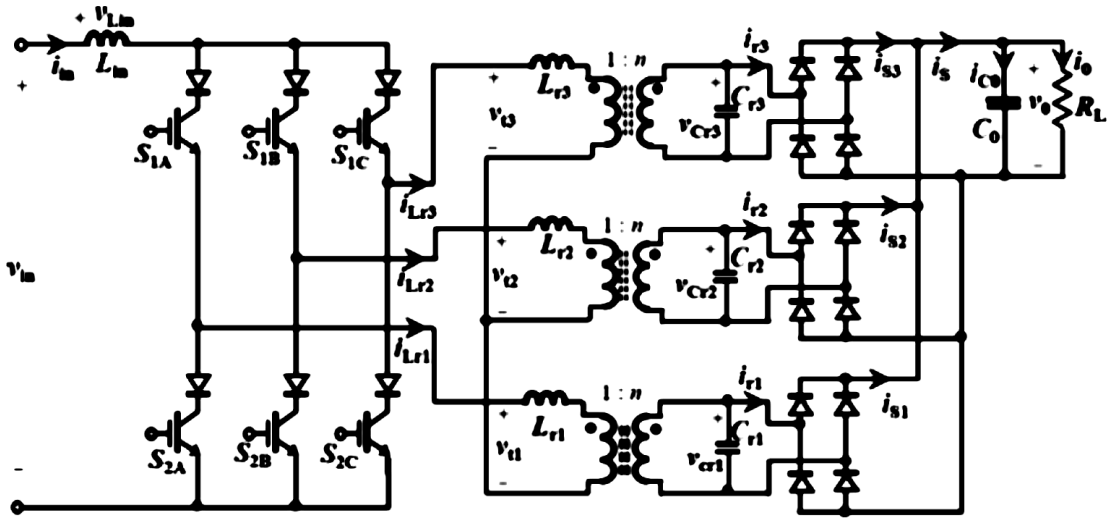


Figure 1.16: High-gain three-phase DC-DC reproduced from [22]

1.1 Thesis Objectives

The main objective of this thesis is to propose new DC-DC and AC-DC converters that are based on three-phase DC-DC technology and that use fewer active switching devices than comparable existing converters. These converters include:

- A new three-phase DC-DC converter with input interleaving and transformer isolations.
- A new single-phase, single-stage AC-DC converter with input current interleaving and transformer isolation that uses a three-phase DC-DC converter in its topology.
- A new non-isolated three-phase DC-DC converter with high output voltage gain that can boost small DC input voltages to much larger ones that can then be used to feed other converters such as DC-AC inverters.

Other objectives of this thesis include:

- The steady-state characterization of these converters so that a design procedure for these converters can be established.

- A comparison between the operation of the isolated three-phase DC-DC converter operating with traditional silicon devices (Si) and new silicon-carbide devices to determine how much better converter efficiency can be achieved. SiC devices are said to offer better performance than Si devices but are less readily available and more expensive.

For this work, the primary emphasis has been placed on the reduction on the number of switches that a converter is implemented with as this generally leads to a reduction in converter cost and size. It should be noted that it is not only the number of switches that are reduced, but also the amount of gate drive circuitry, the amount of sensing circuitry for the switches, the number of controllers and their complexity, and the cost and size of prototype space as well.

1.5 Thesis Outline

The outline of this thesis is as follows:

In Chapter 2, a new three-phase DC-DC converter is presented. This converter requires fewer active switches than converters of the same type, has input current interleaving, inherent switch voltage clamping, and an auxiliary circuit that does not interfere with the operation of the main part of the circuit. In this chapter, the general operation of the converter is described as well as the most significant modes of operation that it goes through during a typical switching cycle. Equations for each mode of operation are derived and then used to establish a design procedure that can be used to select key converter components. The design procedure is demonstrated with an example and used to design an experimental converter prototype.

In Chapter 3, experimental results obtained from a prototype of the converter that was introduced in Chapter 2 are presented. Key experimental waveforms are shown as well as efficiency results. These efficiency results are compared to those obtained of a representative active-clamp type three-phase DC-DC converter operating with conventional silicon (Si) semiconductor devices. Further comparisons are made between

experimental prototypes that were built with silicon-carbide (SiC) devices and conclusions related to converter performance with SiC devices vs Si devices are made.

In Chapter 4, a new single-phase AC-DC converter with three-phase transformer isolation is introduced. The advantages of this converter are that it has an interleaved input current, it has lower component current stresses and less output ripple than AC-DC converters with single-phase transformer isolation. In this chapter, the general operation of the converter is described and the most significant modes of operation that the converter goes through during a typical switching cycle are explained. Equations for each mode of operation are derived and then used to establish a design procedure that can be used to select key converter components. The design procedure is demonstrated with an example and used to design an experimental converter prototype. Results obtained from an experimental prototype of the proposed AC-DC converter are shown and conclusions are presented.

In Chapter 5, a new three-phase DC-DC converter with high output voltage / input voltage gain is introduced. The proposed high gain converter has high output gain, only three active switches, reduced switch voltage stress, an interleaved input for low input current ripple, and inherent voltage snubbing of the switches. In this chapter, the general operation of the converter is described and the most significant modes of operation that the converter goes through during a typical switching cycle is explained. Equations for each mode of operation are derived and then used to establish a design procedure that can be used to select key converter components. The design procedure is demonstrated with an example and used to design an experimental converter prototype. Results obtained from an experimental prototype of the proposed high-gain DC-DC converter are shown, and conclusions are presented.

In Chapter 6, the contents of the thesis are summarized, the main conclusion and contributions of the thesis are stated, and suggestions for future work are presented.

Chapter 2

2 A Novel Three-Phase DC/DC PWM Isolated Boost Converter

A new three-phase DC-DC PWM boost converter that is suitable for use in renewable energy applications is proposed in this chapter. The number of active switches in the proposed circuit is less than that of other previously proposed converters of the same type, resulting in lower cost and simpler operation. The chapter discusses the operation of the converter, presents a procedure for its design, and demonstrates the procedure with an example.

2.1 Converter Operation and Analysis

The proposed three-phase boost converter is shown in Figure 2.1. It is a three-interleaved boost converter that consists of three input inductors (L_1-L_3) and three main switches (S_1-S_3). The converter is connected to the output (high voltage side) through three single-phase transformers whose primaries and secondaries are both connected in delta configuration, a three-phase diode bridge rectifier at the transformer secondary, and an output capacitive filter C_o. The converter is also connected to a flyback snubber through a clamping capacitor C_c and clamping diodes (D_{c1} - D_{c3}). The output of the flyback snubber is connected to the high voltage side of the converter. The proposed converter operates as follows: Whenever one of the main switches is turned on, the current through the main inductor that is connected to its drain rises and this inductor stores energy. Whenever one of the main switches is turned off, the current through the inductor that is connected to it starts to fall. The drain voltage of the switch becomes equal to the voltage across clamping capacitor C_c. If the three main transformers have the same gating signals, but shafted 120^o with respect to each other, then a three-phase voltage can be produced across the three-phase transformer; this voltage can be rectified and fed to the output.

A flyback converter is connected to the interleaved boost converter to discharge capacitor C_c so that its voltage does not become excessive. Energy stored in C_c is fed to the output instead of being dissipated through a snubber resistor.

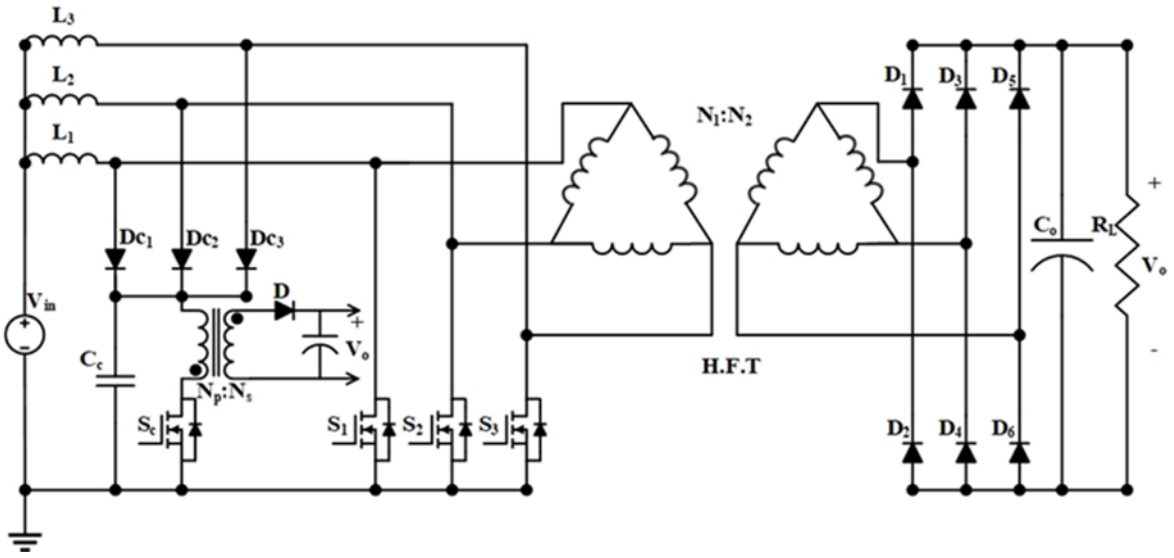


Figure 2.1: Proposed three-phase DC-DC PWM boost converter with flyback snubber

The level of the voltage across C_c depends on how often and for how long switch S_c is on, with the voltage across C_c being lower as S_c is on more frequently and for longer time.

The modes of operation during a third of a steady-state switching cycle are explained in this section. Typical converter waveforms are shown in Figure 2.2 and circuit diagrams for each mode are shown in Figure 2.3. The following assumptions have been made in this section:

- The converter components are ideal
- The input inductors (L_1, L_2 and L_3) are large enough to keep the current through them continuous over a switching period.
- Switch S_1 was on before $t = t_0$ and that it is conducting the full input current before the start of Mode 1 of operation.

Mode 1 [$t_0 < t < t_1$]: At $t = t_0$, switch S_2 is turned on and current from the transformer is transferred to switch S_2. This current transfer is gradual because of the transformer primary leakage inductance.

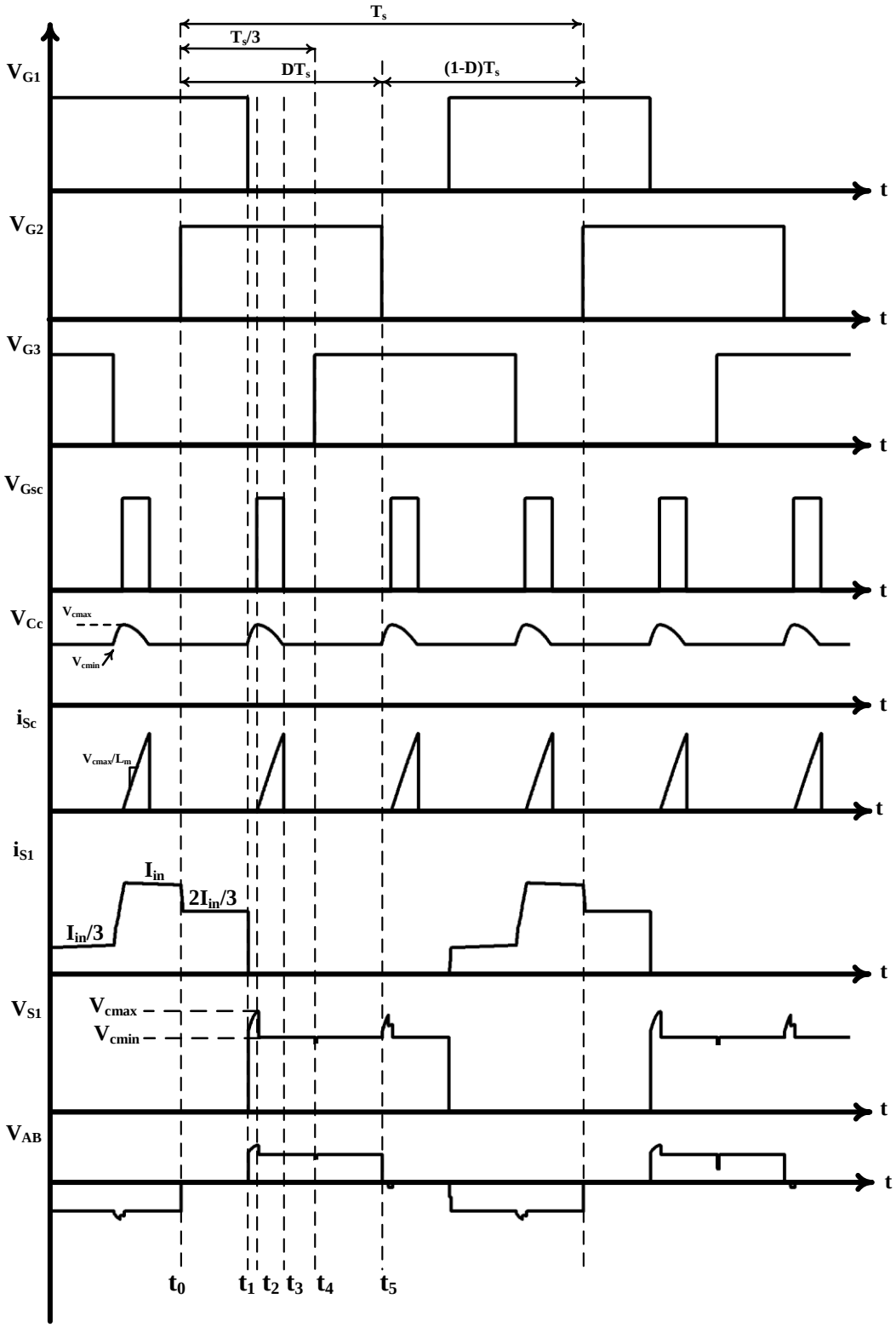


Figure 2.2: Typical converter waveforms at D=0.5

The current through S_2 increases as the current through S_1 decreases. Switches S_1 and S_2 are on, and S_3 is off during this mode. Energy is transferred through the three-phase transformer through the windings that have voltage impressed across them. Diodes D_2 and D_5 conduct current in the secondary.

Mode 2 [$t_1 < t < t_2$]: At $t = t_1$, S_1 is turned off and the currents in diodes D_{c1} and D_{c3}, i_{Dc1} and i_{Dc3}, flow into the clamping capacitor. During this mode, the current through main switch S_2 increases as do currents i_{p1} and i_{p3}. At the converter's secondary side, diode D_1 starts to conduct and diodes D_2 and D_5 continue to conduct. Figure 2.4 shows the equivalent circuit of mode 2 reflected to primary side using Δ-Δ three-transformer configuration.

At the end of this mode, switch S_2 carries all input current, the current i_{Dc1} (t_2) (= i_{L1} (t_2) - i_{p1} (t_2)) drops to zero, and the voltage across the clamping capacitor reaches its peak value. This value can be determined using the following three steps:

- First, the current through the clamping capacitor is expressed as

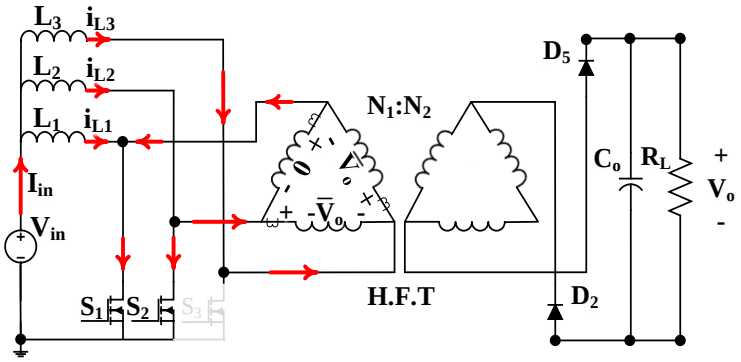
$$i_c(t) = C_c \frac{dv_c(t)}{dt} = i_{Dc1}(t) + i_{Dc3}(t) \tag{2.1}$$

where,

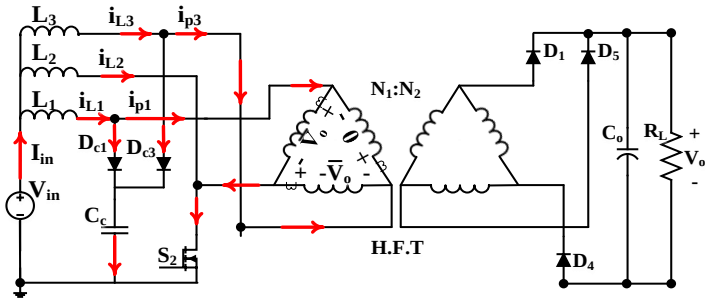
$$i_{Dc1}(t) = I_{L1} - i_{p1}(t)$$

and,

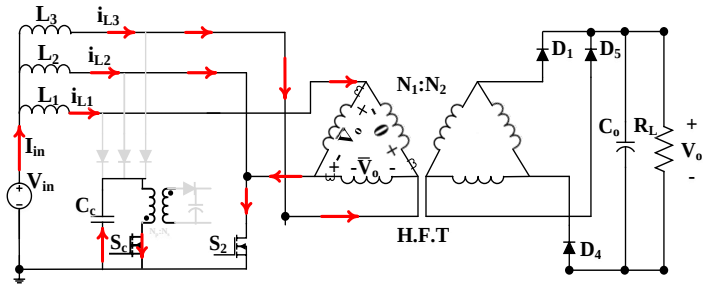
$$i_{Dc3}(t) = I_{L3} - i_{p3}(t) \tag{2.2}$$



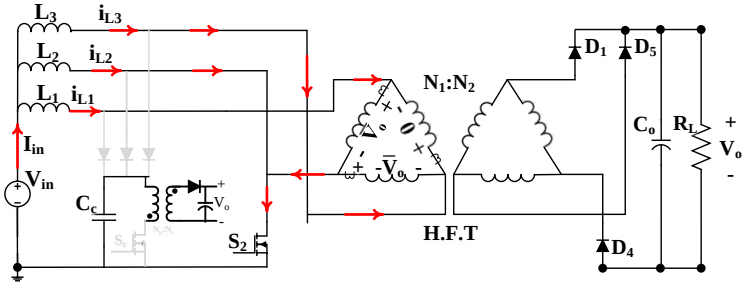
Mode 1



Mode 2



Mode 3



Mode 4

Figure 2.3: Modes of operation

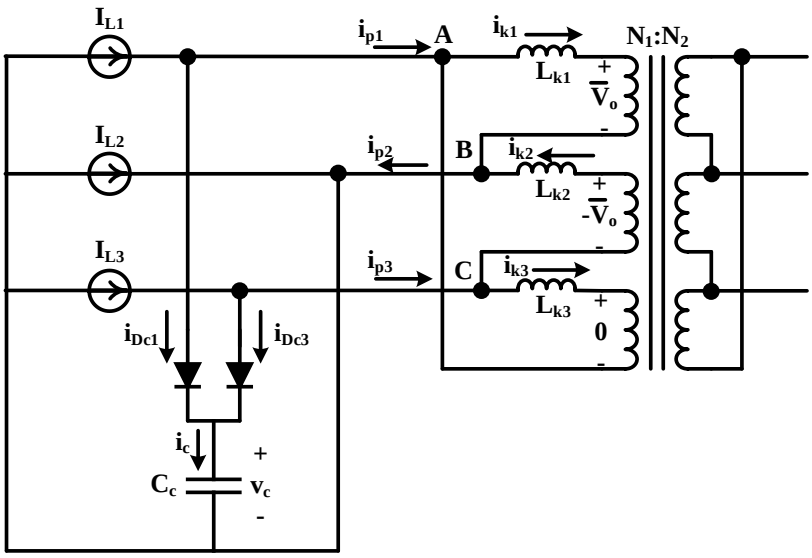


Figure 2.4: Equivalent circuit of mode 2 using Δ-Δ three-transformer configuration

where,

I_{L1} and I_{L3} are the input inductor currents of phase A and C respectively in steady state operation,

i_{Dc1} and i_{Dc3} are the current that flow through the clamping diodes D_{c1} and D_{c3} respectively,

i_{p1} and i_{p3} are the currents that follow through the primary transformer in phase A and C respectively as shown in Figure 2.4, and they can be obtained from (2.3) and (2.4)

$$i_{p1}(t) = i_{k1(t)} - i_{k3}(t) \tag{2.3}$$

$$i_{p3}(t) = i_{k2(t)} + i_{k3}(t) \tag{2.4}$$

where, i_{k1}, i_{k2}, and i_{k3} are the currents of the leakage inductances of the three-phase transformer.

By substituting (2.2), (2.3), and (2.4) in (2.1), the following first order differential equation will be obtained

$$I_{L_1} + I_{L_3} = C_c \frac{dv_c(t)}{dt} + i_{k_1}(t) + i_{k_2}(t) \tag{2.5}$$

- Second, by derivative (2.5), it becomes

$$C_c \frac{d^2 v_c(t)}{dt^2} + \frac{di_{k1}(t)}{dt} + \frac{di_{k2}(t)}{dt} = 0 \tag{2.6}$$

where i_{k1} and i_{k2} can be obtained from Figure 2.4 as following

$$L_{k_1} \frac{di_{k_1}}{dt} = v_c(t) - \overline{V_o} \tag{2.7}$$

$$L_{k_2} \frac{di_{k_2}}{dt} = v_c(t) - \overline{V_o} \tag{2.8}$$

- Third, By substituting (2.7) and (2.8) in (2.6) and the initial value of v_c is defined as $V_c(0) = V_{c_{min}}$ and the initial value of the current through the clamping capacitor is $\frac{I_{in}}{2}$, the voltage across and the current through the clamping capacitor are obtained as

$$v_c(t) = V_{c_{min}} \cos(\omega_o t) + \overline{V_o}\left(1 - \cos(\omega_o t)\right) + \frac{I_{in}}{2} Z_o \sin(\omega_o t) \tag{2.9}$$

$$i_c(t) = \frac{I_{in}}{2} \cos \omega_0 t - \frac{V_{cmin} - \overline{V_o}}{Z_0} \sin \omega_0 t \tag{2.10}$$

where,

$\overline{V_o} = \frac{V_o}{n}$: primary voltage across the main transformer where V_o is the output voltage of the converter and n is the turn ratio of the main transformer $\left(n = \frac{N2}{N1}\right)$,

$$\omega_o = \sqrt{\frac{1}{L_k C_c}} \tag{2.11}$$

and,

$$Z_o = \sqrt{\frac{L_k}{C_c}}, \quad \frac{1}{L_k} = \frac{1}{L_{k_1}} + \frac{1}{L_{k_2}} \tag{2.12}$$

At the end of this mode, $i_c(t) = 0 \; and \; v_c(t) = V_{c_{max}}$. By substituting these values in (2.10) the duration of this mode can be determined, according to,

$$t_2 - t_1 = \frac{1}{\omega_o} \tan^{-1}\left(\frac{I_{in}}{2} \frac{Z_o}{V_{c_{min}} - \overline{V_o}}\right) \tag{2.13}$$

The peak voltage across voltage across the capacitor at the end of this mode, which also the peak voltage across the switches, becomes

$$V_{c_{max}} = V_{c_{min}} \cos \omega_0 (t_2 - t_1) + \bar{V_o}\big(1 - \cos\omega_0 (t_2 - t_1)\big) + \frac{I_{in}}{2} Z_o \sin \omega_0 (t_2 - t_1) \quad (2.14)$$

where,

$$\omega_o = \frac{1}{C_C Z_o} = \frac{1}{\sqrt{L_k C_c}} \quad (2.15)$$

Since the duration time of this mode is the quarter of the resonant cycle between the equivalent leakage inductance of the transformer, L_k, and the clamping capacitor, C_c, (i.e. $t_2 - t_1 = \frac{\pi}{2}\sqrt{L_k C_c}$). By substituting in (2.14), the maximum voltage across the clamping capacitor can be obtained as

$$V_{c_{max}} = \bar{V_o} + \frac{I_{in}}{2} Z_o \quad (2.16)$$

Mode 3 [$t_2 < t < t_3$]: At $t = t_2$, clamping diode D_{c1} stops conducting and capacitor C_c starts discharging. Switches S_1 and S_3 remain off and switch S_2 stays on during this mode. Power is transferred to the output through D_1, D_4 and D_5. The flyback transformer also starts to store energy in this mode. Figure 2.3 (Mode 3) shows the equivalent circuit of this mode with switch S_c turned on. It should be noted that S_c can be turned on and off at any time during the switching period to discharge C_c. At the end of this mode the voltage

across the clamping capacitor is V_{cmin}. The voltage across clamping capacitor and the current through flyback switch can be expressed according to the following equations:

$$L_m \frac{di_{L_m}(t)}{dt} - v_c(t) = 0 \tag{2.17}$$

$$i_c(t) = i_{L_m}(t) = -C_c \frac{dv_c(t)}{dt} \tag{2.18}$$

where,

L_m: magnetizing inductor of flyback transformer

$i_c(t)$: the current through the clamping capacitor

$i_{L_m}(t)$: the current through the magnetizing inductor of the flyback transformer

If the initial value of $v_c(t)$ is defined as $v_c(t) = V_{c_{max}}$ and the initial value of the current through the clamping capacitor is zero, the voltage across the capacitor and the current through it can be expressed as

$$V_c(t) = V_{cmax} \cos \omega_1 t \tag{2.19}$$

$$i_c(t) = i_{L_m}(t) = \frac{V_{c_{max}}}{Z_1} \sin \omega_1 t \tag{2.20}$$

where

$$\omega_1 = \frac{1}{\sqrt{L_m C_c}} \tag{2.21}$$

and

$$Z_1 = \sqrt{\frac{L_m}{C_c}} \tag{2.22}$$

At the end of this mode, the voltage across the clamping capacitor is regulated to desired value V_{cmin}, which is just slightly higher than the primary voltage of the main transformer, ($V_{C_{min}} \approx \overline{V_o}$), where $\overline{V_o}$ is the primary voltage across the main transformer. By substituting in (2.19), the duration of this mode (t_3-t_2) can be expressed as

$$t_3 - t_2 = \frac{1}{\omega_1} \cos^{-1}\left(\frac{V_{c_{min}}}{V_{c_{max}}}\right) \tag{2.23}$$

By using (2.16)

$$t_3 - t_2 = C_c Z_1 \cos^{-1}\left(\frac{\overline{V_o}}{\overline{V_o} + \frac{I_{in}}{2} Z_o}\right) \tag{2.24}$$

where

$$\omega_1 = \frac{1}{C_c Z_1} \tag{2.25}$$

The duration of this mode determines how much the auxillary switch will be turned on, thus the duty cycle for the flyback converter can be determined to be

$$D_f = \frac{t_3 - t_2}{T_{sf}} = (t_3 - t_2) f_{sf} = f_{sf}\, C_c Z_1 cos^{-1}\left(\frac{\overline{V_o}}{\overline{V_o} + \frac{I_{in}}{2} Z_o}\right) \tag{2.26}$$

Mode 4 [$t_3 < t < t_4$]: At $t = t_3$, the flyback switch is turned off. The energy stored in the flyback transformer is transferred to the output. Note that the main switches have the same on/off state as in the previous mode and that this mode has been included to show how the circuit operates when switch S_c is turned off. This mode can happen at any time during the switching period.

Mode 5 [$t_4 < t < t_5$]: At $t = t_4$, S_3 is turned on and the next third of a switching cycle starts. The converter operates as it does in Mode 1, but with S_2 and S_3 on instead of S_1 and S_2. A circuit diagram for Mode 5 is not shown in Figure 2.3 as this mode is the same as Mode 1.

2.2 Duty Cycle Range

The converter can be operated with PWM with the gating signals of the three main switches - S_1, S_2, S_3 - being identical but phase-shifted by 120^o with respect to each other. There are three distinct ranges of duty that the converter can operate with:

- *Range 1 [$0 < D < 0.33$]:* In this range, there is either a single main switch on or none at all. The converter should only be operated in this range under light load conditions when the current is low as some of the phase currents will not have a path to flow through the main switches, but must flow through capacitor C_c, thus charging it up and increasing its voltage. As a result, either the voltage across this capacitor will increase, thus increasing the voltage stress of the converter switches, or the auxiliary switch must be activated more frequently and/or be on for a longer duration to discharge the capacitor, thus increasing the stress on the auxiliary switch S_c.

- *Range 2 [$0.33 < D < 0.66$]:* In this range, there is always at least one main switch on at any given instant and there may be two main switches on. As a result, there will always be a path for current in each phase to flow through at any time during a switching cycle.

- *Range 3 [$0.66 < D < 1$]:* In this range, either two main switches or all three main switches are on at any given time. The converter operates in the same manner as it

does when the converter operates with a duty cycle between 0.33 and 0.66, but there is a fundamental difference between Range II and Range III operation. If the converter is operated with D > 0.66, then there will be intervals of time when no energy transfer from input to output will take place. For example, if all three main switches are on at the same time, then each converter phase has the same voltage so that all three line-to-line voltages are zero and the voltages across all transformer windings is zero. With the duration of such zero energy-transfer intervals increasing as D is increased above D = 0.66, the gain of the converter may actually decrease instead of increase, as is the case with most PWM converters. It is therefore recommended that the converter not be operated in Range III and that the maximum duty cycle be restricted to D = 0.66.

2.3 Converter Features

The proposed converter has the following features:

- An increased power rating with respect to a conventional single-phase boost converter due to the use of a three phase DC-DC converter topology instead of a single phase one.

- The current stresses of the main converter switches can be reduced significantly, which enables the use of lower rated devices.

- The size of the input DC inductors and the output filter can be reduced as the effective switching frequency is increased.

- Unlike a number of previously propose three-phase converters, only four converter switches are required as opposed to six or seven switches.

- A large snubber capacitor can be placed across the main converter switches and energy from this snubber capacitor can be transferred to the output instead of being dissipated through a resistor.

- The converter can be operated at higher switching frequencies than some other previously proposed three switch DC-DC converters. This is because the auxiliary flyback converter does not directly interfere with the operation of the main converter unlike the auxiliary circuits in other converters. In many other converters, such as those based on active-clamp technology for example, time for the operation of the auxiliary circuit must be included in the switching period.

2.4 Design Procedure and Example for the Power Stage of the Proposed Converter

The proposed converter has two parts: the first part is a three-phase interleaved current-fed converter and the second part is an auxiliary circuit which consist of clamping components and flyback converter. The design of the power stage of the proposed converter is discussed in this section and demonstrated with an example of the selection of certain key parameters. The design of the auxiliary flyback converter section will be discussed and demonstrated in the next section of the thesis. It should be noted that the design procedures of both converter sections are iterative as the parameters in each section are interrelated and dependent on one another. It will generally take several iterations before a satisfactory design can be achieved and this process may need to be continued in the design of a final experimental prototype. The example shown in this section and continued in the next section can be considered to be the final iteration of a design process.

Since electrical components like capacitors are only commercially available with certain standard values (i.e. 22 nF, 33 nF, etc.) and parasitic elements such as parasitic inductances can only be accurately determined after a preliminary prototype has been constructed, the design procedure can only narrow down a suitable range of values and cannot be used for an “optimized” design. This narrowing process can be done by the previous iterations, by examining parameters such as voltage stress, peak current stress, rms current stress, etc, then eliminating possible sets of component values if their parametric values are inappropriately high (which would result in the need for more expensive components to handle the stress) or low (which would represent an underutilization of the component and additional stress on other converter components).

The converter is designed according to the following specifications: input voltage V_{in} = 48 V, output voltage V_o = 360 V, output power P_o = 1.5 kW, and switching frequency f_s = 50 kHz. The leakage inductance of the main transformer is assumed to be 1 μH based on previous design iterations. The targeted efficiency in this example is assumed to be at least 90% based on previous iterations. For this work, what was done was to build a prototype using preliminary iterations to get some idea about the converter's performance, then make appropriate adjustments for following iterations. What is shown in this example, as well as for other similar design examples in this thesis is the final iteration.

2.4.1 Maximum input current

The maximum input current of the proposed converter, its DC value, can be determined by

$$I_{in} = \frac{P_o}{\eta V_{in}} \tag{2.27}$$

Since P_o=1.5 kW, V_{in}=48V and a minimum efficiency of 90% is assumed, therefore, the maximum input current $I_{in(max)}$=34.72A.

2.4.2 Input-output voltage gain

The input-output voltage gain of the converter for both CCM and DCM modes can be expressed as follows:

$$G_{CCM} = \frac{V_o}{V_{in}} = \frac{n}{(1-D)} \tag{2.28}$$

$$G_{DCM} = \frac{V_o}{V_{in}} = n + \frac{3D^2 V_{in}}{2 I_o L f_s} \tag{2.29}$$

It is assumed for now that the converter will operate in CCM under typical load conditions and operate in DCM only under light-load conditions. With this being the case, the voltage gain is therefore

$$G = \frac{V_o}{V_{in}} = \frac{360}{48} = 7.5 \tag{2.30}$$

2.4.3 Duty cycle and main transformer turns ratio

Since it is assumed that the converter operates in CCM with a duty cycle D > 0.33 under heavy-load conditions (as explained in Section 2.2) and the voltage gain was previously determined to be 7.5, the turns ratio can be limited to be less than 5, according to (2.28), which has been plotted in Figure 2.5 for CCM operation.. There is, however, a trade-off between the turns ratio and the duty cycle that must be considered in the design. Although smaller duty cycle means lower voltage stress across the switches, it results in

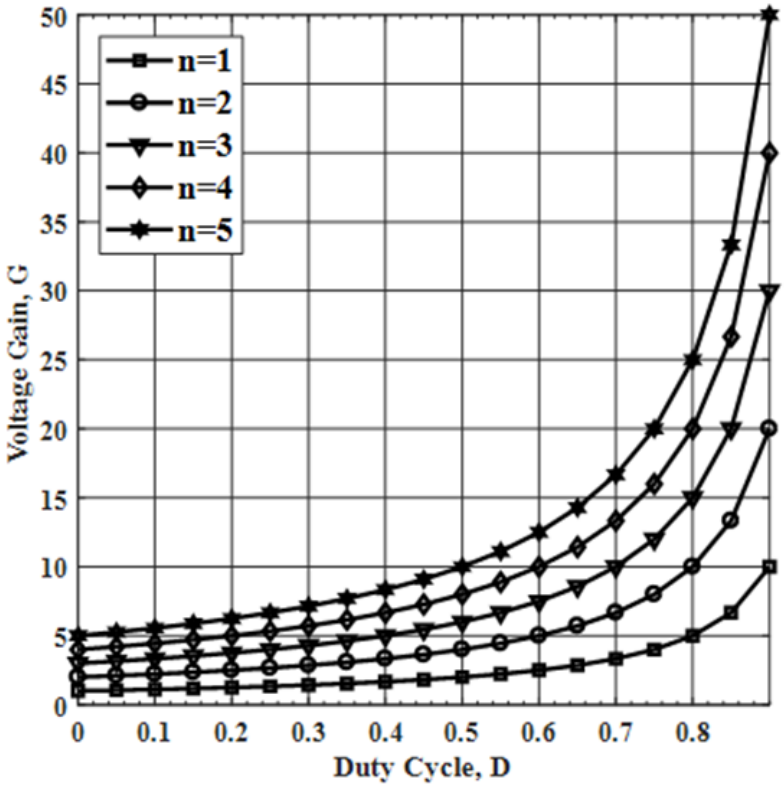


Figure 2.5: Voltage gain with duty cycle according to the variation of transformer turns ratio, n under CCM

higher turns ratio. This increases the amount of current circulating in the primary circulation current and thus conduction losses as well. The turns ratio of the main transformer should be chosen to minimize the voltage stress across the main switches, which can be approximated to be the voltage across the primary of the main transformer, $\overline{V_o} = \frac{V_o}{n}$.

Figure 2.6 shows a graph of the voltage across the primary of the main transformer with different values of turns ratio. It can be seen that a lower turns ratio causes more voltage to appear across the primary; as a result, the peak voltage rating of the main switches will need to be increased. According to the graph in Figure 2.6, the range of the turns ratio is between 1 and 5 and the primary voltage is between 70 V to 350V.

In this design example, the proposed converter is operated in Range 2 [0.33 < D < 0.66]. by using D_{max}=0.6 and the voltage gain G=7.5, which results n=3 according to (2.28) and Figure 2.5. From graph in Figure 2.6, the primary voltage of the main transformer is 120V.

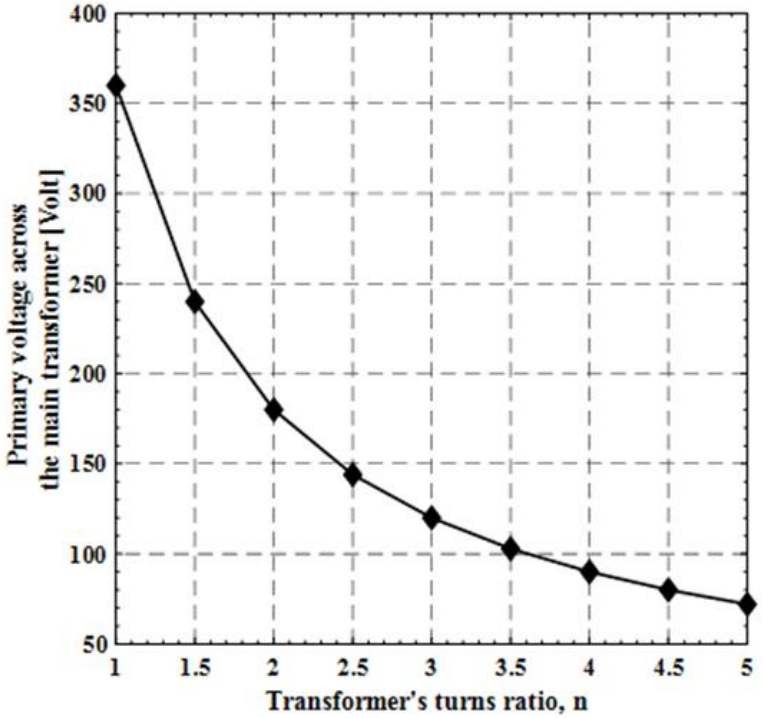


Figure 2.6: Primary voltage across the main transformer with turns ratio,n

2.4.4 Determine the value of input boost inductor

The minimum input inductor value that will guarantee the converter operates in CCM can be calculated by

$$L_{min} = \frac{3R_L D(1-D)^2}{2n^2 f_s} \tag{2.31}$$

By using, D=0.6, n=3 and f_s=50 kHz, it results V_o=360V, $R_L = \frac{(360)^2}{1500} = 86.4\ \Omega$ and the minimum value of the input inductor for each phase can be determined to be 27.65 µH.

Since the converter is a boost converter operating in CCM, the value of each input inductor ($L_1 = L_2 = L_3$) can be expressed as

$$L = \frac{V_{in} D}{\Delta i_L f_s} \tag{2.32}$$

where Δi_L is the peak-to-peak current ripple for each input inductor. If a ripple of Δi_L=2A is considered in this example, then each input inductor should have a value of 288 µH.

2.4.5 Determine the value of output capacitor

The magnitude of the output voltage ripple, Δv_o, can be determined by

$$\Delta v_o = \frac{V_o(2-3D)(D-\frac{1}{3})}{3R_L f_s C_o (1-D)} \tag{2.33}$$

If a ripple of Δv_o=10 *mV, R_L=86.4 Ω, D=0.6, f_s=50kHz and V_o=360V* are considered, the output capacitor C_o can then be determined to be C_o=370.37µF.

2.4.6 Current stress in the main switches

At some point during a switching period, any of the main switches may need to conduct the full current through the inductor that it is connected to. The peak current in any of the main switches is equal to the input current plus the peak current ripple. The peak switch current is therefore

$$I_{S_{pk}} = I_{in} = 34.72 \text{ A}$$

The average current through each main switch when the converter is operating at full-load is

$$I_{s_{avg}} = \frac{1}{T}\int_0^T i_s(t)dt = \left(\frac{I_{in}}{3}\right) \tag{2.34}$$

It can be seen that the average current for any of the main switches is a third of the input current. Using the maximum input current value determined previously, the average current through one of the main switches is $I_{s_{avg}} = 11.57$ A.

The rms current of each main switch can be determined by

$$I_{s_{rms}} = \sqrt{\frac{1}{T}\int_0^T i_s^2(t)dt} = \frac{I_{in}}{3\sqrt{3}}\sqrt{13 - 12D} \tag{2.35}$$

It can be seen that the rms current through each main switch depends on the input current and the duty cycle D. By increasing the input current, the rms value will increase, but this value can be reduced by increasing D. In this design, the rms current through each main switch is $I_{s_{rms}} = 16.09\ A$.

2.5 Design Procedure and Example for the Auxiliary Circuit Stage

The auxiliary circuit of the proposed converter consists of clamping diodes D_{c1}-D_{c3}, clamping capacitor C_c and flyback converter. In this section, the design of the auxiliary stage of the proposed will be discussed and demonstrated with an example of the selection of certain key parameters. Like the design procedure for the main circuit converter components, the procedure presented in this section is iterative and it will generally take several iterations before a satisfactory design is achieved. The example shown below can be considered to be the final iteration of a design process.

Figure 2.7 shows a simple flowchart of a computer program that determines whether the proposed converter is functioning under steady-state conditions. Once this has been

determined, suitable characteristic curves that can be used for design purposes can be generated.

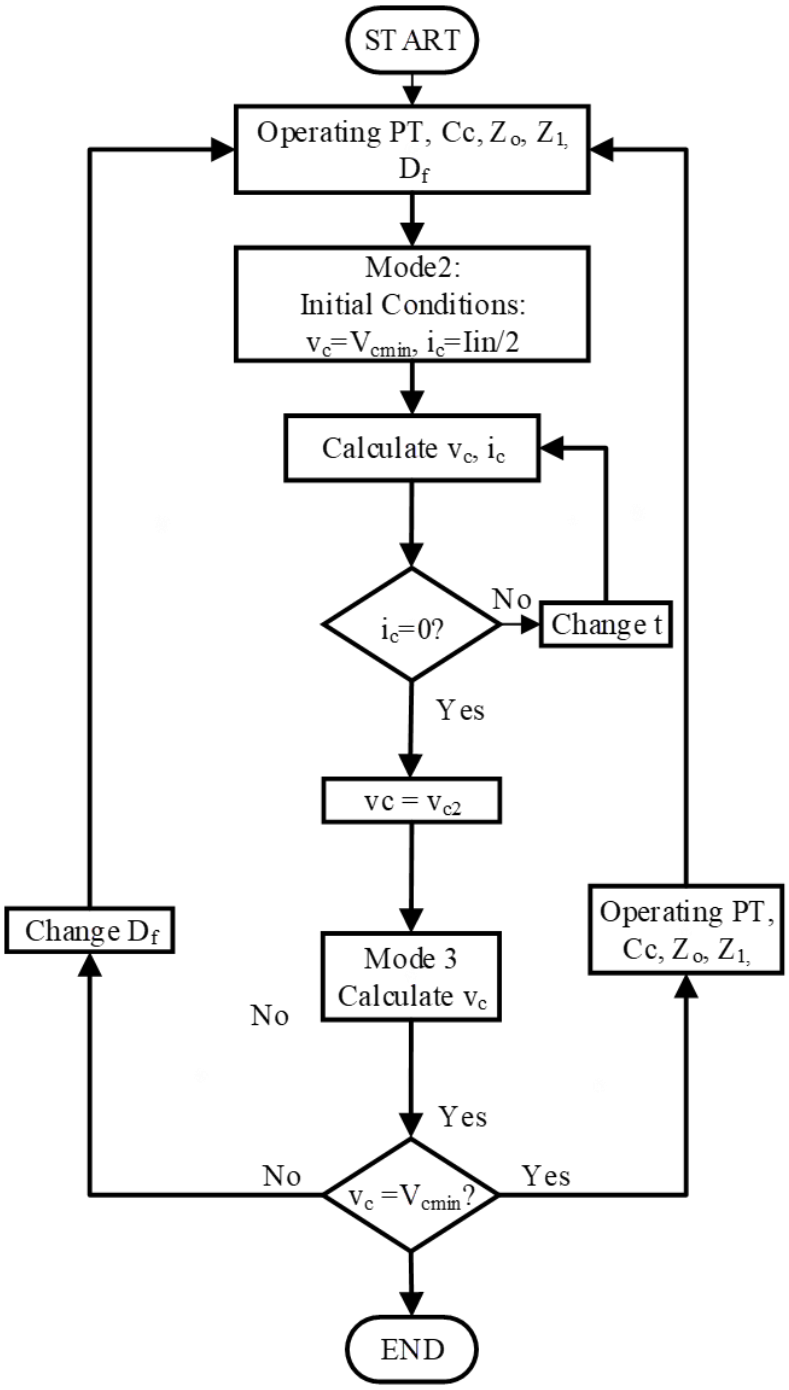


Figure 2.7: Flowchart of program to determine if converter is operating under steady-state conditions

2.5.1 Power Rating for the flyback snubber

The flyback converter allows the clamping capacitor to be discharged so that the voltage across it does not become excessive. The snubber circuit switch (S_c) is turned on soon after whenever any of the main switches is turned off. The flyback snubber can be independently controlled to regulate the minimum value of the clamping capacitor, V_{cmin}, to a desired value, which is just slightly higher than the voltage across the primary of the main transformer. The power rating of this circuit is determined by

$$P_{fb} = \frac{1}{2} C_c \left(V_{C_{max}}^2 - V_{C_{min}}^2\right) f_{sf} \tag{2.36}$$

where V_{cmax} is a maximum voltage across C_c, V_{cmin} is the minimum voltage across C_c, which is equal to the voltage across the primary of the main transformer, $\overline{V_o}$ and f_{sf} is the switching frequency of the flyback snubber. By using $V_{c_{max}} = \overline{V_o} + \frac{I_{in}}{2} Z_o$, $V_{c_{min}} = \overline{V_o}$, and $Z_o = \sqrt{\frac{L_k}{C_c}}$ then substituting in to (2.36), the power rating of the flyback converter becomes

$$P_{fb} = \frac{1}{2} \frac{L_k}{Z_0^2} \left(I_{in} \overline{V_o} Z_0 + \left(\frac{I_{in} Z_o}{2} \right)^2 \right) f_{sf} \tag{2.37}$$

The power rating curve of the flyback converter with different values of characteristic impedance Z_o and leakage inductance L_k is plotted from (2.37) in Figure 2.8.

The value of $\overline{V_o}$ was set to 120V is Section 2.4.3 and the switching frequency of the flyback converter is selected to be f_{sf} =150 kHz for this example (i.e. the flyback converter will operate three times during one period of the power converter).

It can be seen that higher Z_o decreases the rating of the flyback snubber because less current will flow through it. The power rating will decrease significantly with lower main transformer leakage inductance L_k because less energy will be trapped by L_k.

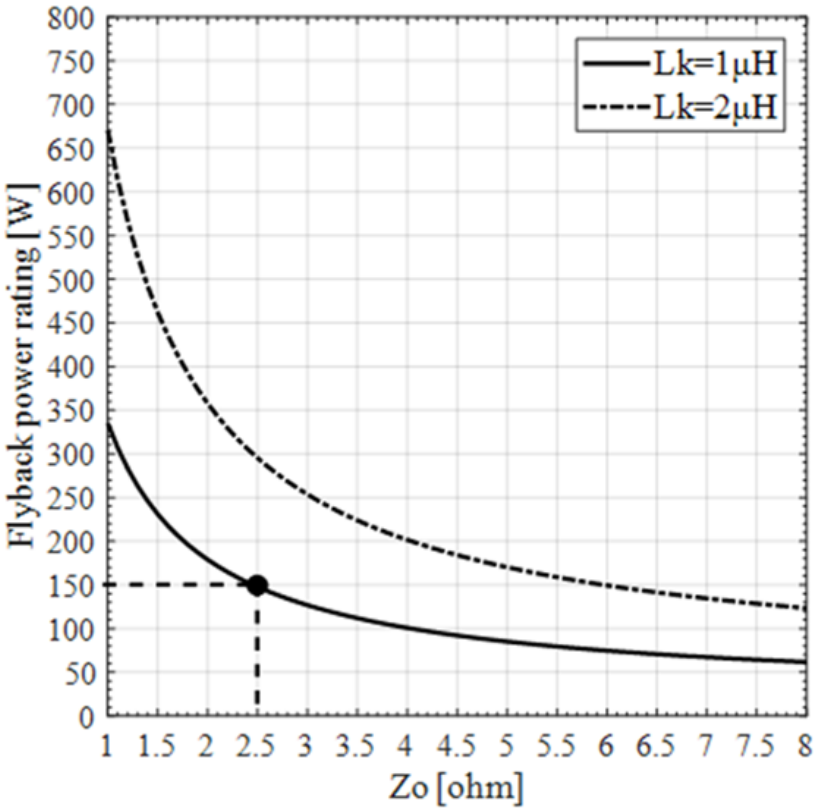


Figure 2.8: Flyback power rating with different values of Z_o for different values of L_k, P_o = 1.5KW and V_o=360V

In this design example, the power rating of the auxiliary flyback converter section is chosen to be 10% of the load (i.e. 150 W). Since the leakage inductance was assumed to be 1 μH based on previous iterations, the value of the characteristic impedance is therefore Z_0=2.5Ω, from Figure 2.8.

2.5.2 Peak voltage across the clamping capacitor

In Mode 2, whenever one of the main switches, S_1-S_3, is turned off, the voltage across them builds up, due to the resonance between the equivalent leakage inductance of the main transformer and clamping capacitor C_c. At the end of this mode, the voltage across a main switch that turned off reaches its peak voltage, which is the same as the voltage across the clamping capacitor. By reducing the clamping capacitor voltage, the excess voltage across the main switches will be reduced.

Figure 2.9 shows a graph of the peak voltage across clamping capacitor for different values of Z_o using (2.16). From the graph in Figure 2.9, it can be seen that a larger impedance Z_o means that there will be more voltage across C_c and thus more voltage stress across the main switches of the converter energy. If a smaller impedance is chosen, then the result will be less peak voltage, but the flyback converter section will have a higher power rating, as shown in Figure 2.8 in the previous section.

For this design, a value of Z_o= 2.5 Ω was chosen in the previous section, which resulted in a 150 W flyback power rating. This, in turn, will result in 164 V being placed across the clamping capacitor under full-load conditions, according to Figure 2.9. It should be noted that this voltage is the maximum voltage stress across the main switches.

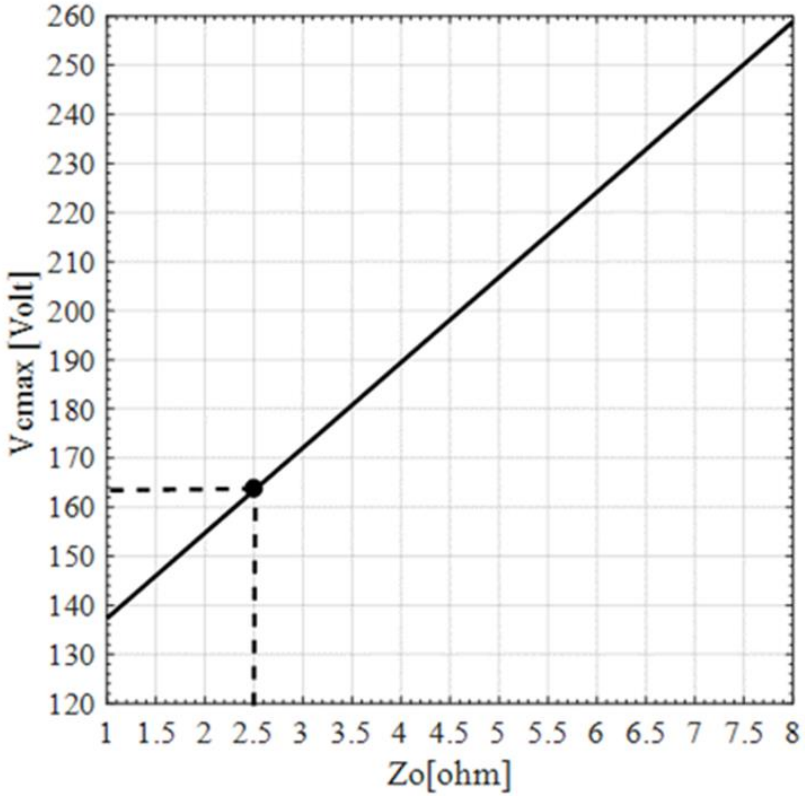


Figure 2.9 : Maximum voltage across the clamping capacitor with different values of Z_o, P_o = 1.5KW and V_o=360V

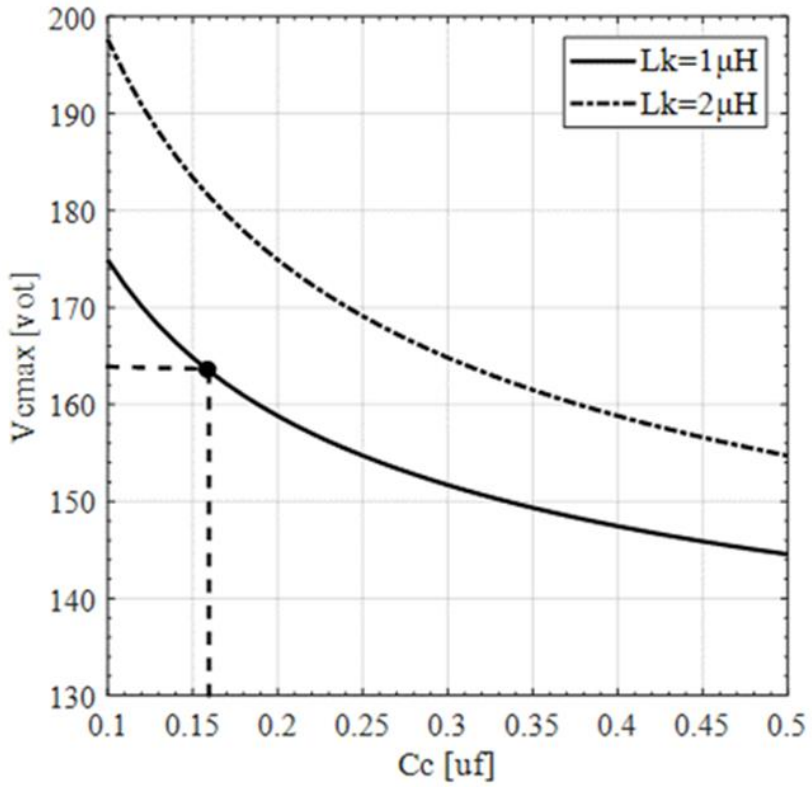


Figure 2.10: Variation of the maximum voltage across the clamping capacitor with different values of C_c and L_k

The value of the voltage across C_c is dependent on Z_o using (2.16) (where $Z_o = \sqrt{\frac{L_k}{C_c}}$), thus it is impacted by changing L_k and C_c.

Figure 2.10 shows the peak voltage across the clamping capacitor for different values of C_c and L_k. From this graph, the value of clamping capacitor can be determined. by using V_{cmax} = 164 V from Figure 2.10; this results in C_c=160 nF.

2.5.3 Voltage stress across flyback switch and flyback transformer turns ratio

The rated voltage of the flyback switch should be close to the rated voltage of the main switches. The voltage stress across the flyback switch can be expressed by:

$$V_{sc} = V_{cmin} + \frac{V_o}{N} \tag{2.38}$$

where, V_{cmin} is the minimum voltage across the clamping capacitor, $N=N_s/N_p$ is the turns ratio of the flyback transformer (N_s, N_p are the primary and secondary turns respectively) and V_o is the output voltage of the converter. It is clear that the voltage stress across the calming switch strongly depends on the turns ratio of the flyback transformer. Figure 2.11 shows the relationship between the flyback transformer turns ratio and the voltage across its switch when V_{cmin} is 120V and V_o is 360V. It can be seen that more turns ratio means less voltage stress across the flyback switch however more turns ratio means larger transformer size. It is a trade-off between the voltage rating of the flyback switch and the size of the flyback transformer. It should be noted that the rating voltage of the flyback switch must be as close as the rating voltage of the main switch (i.e. V_{cmax} =164 V). In this design the maximum voltage across the flyback's switch is chosen to be 180V. From Figure 2.11 the turns ratio N will be 6.

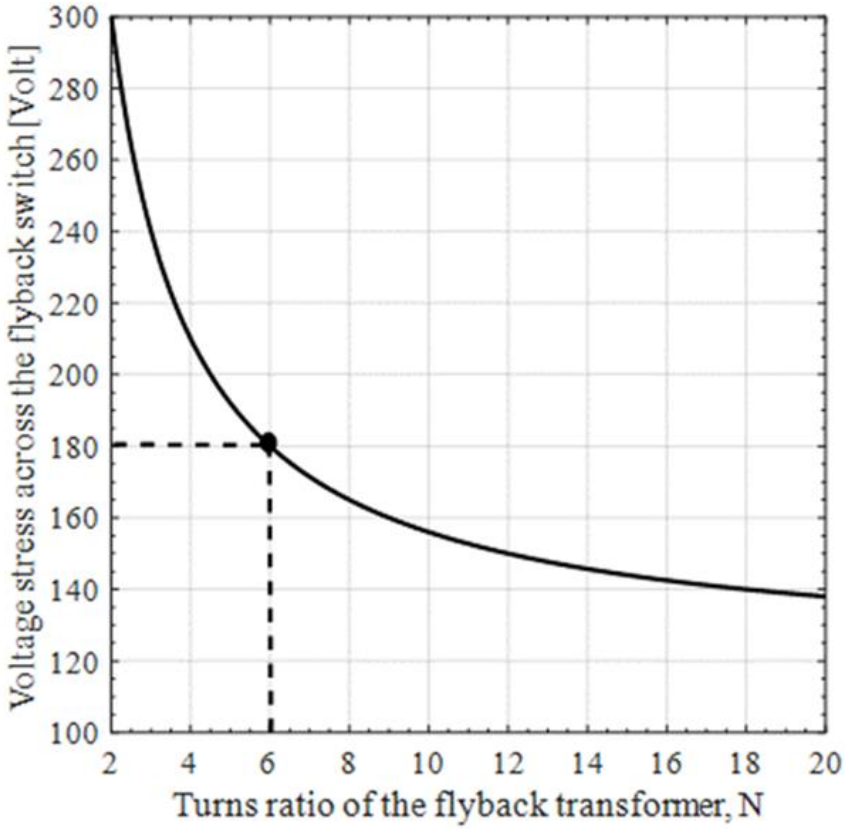


Figure 2.11: Flyback switch's voltage stress with flyback transformer turns ratio, N

2.5.4 Determine the duty cycle D_f and the characteristic impedance Z_1 of the flyback converter

In Mode 3, the flyback converter switch is turned on after the clamping capacitor reaches its maximum value and it transfers all the energy that stored on the clamping capacitor to the output through the flyback transformer. The duty cycle of the flyback converter switch is determined by the duration of Mode 3 as shown in (2.26). The duty cycle of the flyback converter switch depends on the characteristic impedances Z_0 and Z_1 as shown in Figure 2.12. It can be seen that higher Z_1 results in more duty cycle being needed (i.e. more time needed to transfer the capacitor energy to the flyback transformer), but this will result in more conduction losses. Thus, D_f and Z_1 should be chosen as small as possible. The duty cycle of the flyback converter switch, D_f, is determined by (2.39) as follows:

$$\frac{V_o}{V_{C_{max}}} = \frac{D_f}{(1 - D_f)}\left(\frac{N_s}{N_p}\right) \tag{2.39}$$

By using V_o=360 V, V_{cmax}=164 V, and (N_s/N_p) = 6 from previous sections, the duty cycle of the flyback converter switch becomes D_f=0.27. By using Z_o=2.5Ω from Figure 2.12, this results in Z_1=15Ω.

2.5.5 Maximum current in the clamping switch

At the end of Mode 3, when the flyback converter switch S_c is turned off, the current through this switch will be at its peak value. The value of the peak current can be determined by (2.20) and (2.23) as follows:

$$i_{Sc}(pk) = \frac{V_{c_{max}}}{Z_1}\sin\left(cos^{-1}\frac{\overline{V_o}}{V_{c_{max}}}\right) \tag{2.40}$$

It should be noted that the maximum current through the flyback switch depends on the peak clamping voltage, which depends on Z_o, and the characteristic impedance Z_1. Figure 2.13 shows the peak current in the flyback switch for different values of Z_1 and Z_o. It can be seen that higher Z_1 results in lower current stress on the flyback switch, but this means that the switch must be on longer (have a higher D_f) to transfer the energy to the output,

as shown in Figure 2.12. Z_o =2.5Ω and Z_1=15 Ω are chosen for this design, which results in a maximum current is 7.9A, according to Figure 2.13.

2.5.6 Average and RMS currents in the flyback converter switch

The average current in the flyback converter switch can be calculated by

$$I_{sc}(avg) = \frac{1}{T_{sf}} \int_{t_2}^{t_3} i_{sc}(t)dt = \frac{1}{T_{sf}} \left(\frac{I_{sc}(pk)(t_3 - t_2)}{2} \right) = \frac{I_{sc}(pk)D_f}{2} \qquad (2.41)$$

The rms value can be calculated by

$$I_{sc}(rms) = \sqrt{\frac{1}{T_{sf}} \int_{t_2}^{t_3} i_{sc}^2(t)dt} = \sqrt{\frac{1}{T_{sf}} \left(\frac{I_{sc}^2(pk)(t_3 - t_2)}{3} \right)}$$

$$= I_{sc}(pk) \sqrt{\frac{D_f}{3}} \qquad (2.42)$$

By using $V_{c_{max}} = 164$ V, $C_c = 160nf$, $f_{fb} = 150kHz$, $Z_1 = 15\Omega$, D_f=0.27, and Figure 2.13, this will result in $I_{sc}(avg)$ = 0.7856A and $I_{sc}(rms)$ = 1.55A.

2.6 Conclusion

Three-phase DC-DC converters are an attractive option for applications where a low DC input voltage needs to be converted into a much higher DC output voltage. For example, many renewable energy power systems require DC-DC converters that can convert the DC voltages produced by solar panels or fuel cells into much higher DC voltages that are then fed to grid-interfacing inverters. A new three-phase DC-DC converter was presented in this chapter. The outstanding features of the proposed converter include:

- a reduced number of switches compared with other three-phase DC-DC converters, which results in lower cost and size;

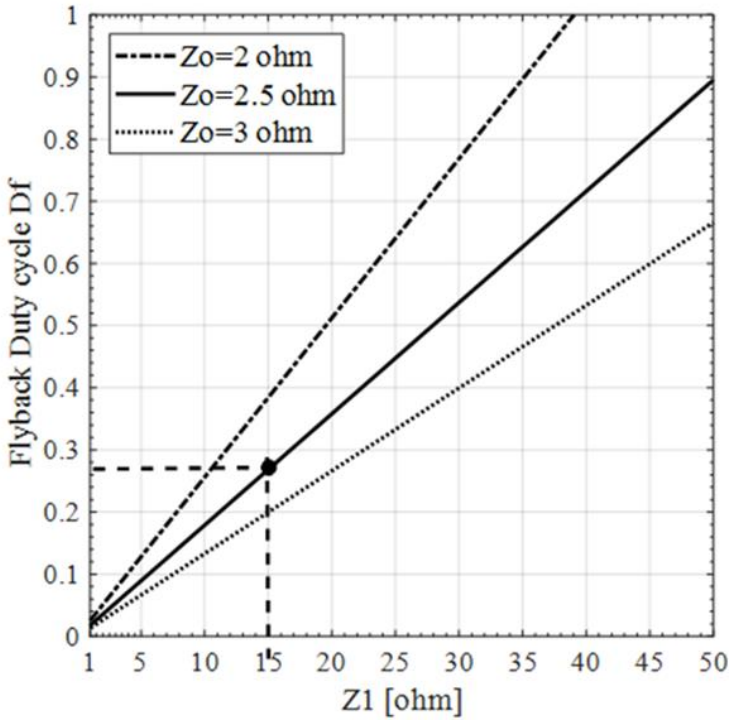


Figure 2.12: Flyback duty cycle for different values of Z_0 and Z_1

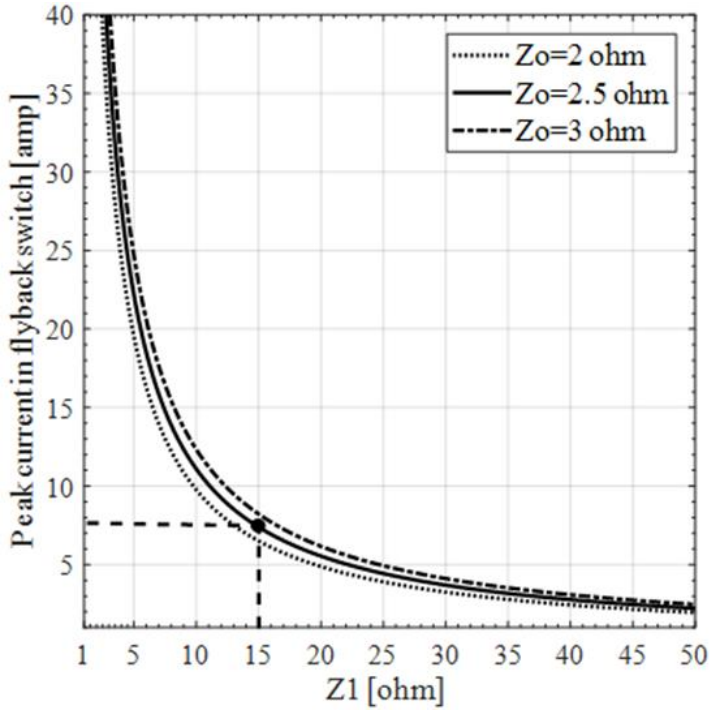


Figure 2.13: The clamping switch's current for different values of characteristic impedances Z_1 and Z_0

- a snubber that can clamp voltage spikes when any of the main switches is turned off and that does not dissipate energy through a snubber resistor;

- a flyback snubber circuit that can be operated independently of the main power circuit so that it does not interfere with its operation; this allows the converter to be operated with higher switching frequency.

In this chapter, the operation of the converter was explained, and its features and design were discussed.

Chapter 3

3 Experimental Results of a Proposed Three-phase DC-DC converter

In this section, the experimental results of the proposed topology will be shown and described to confirm the operation of the proposed converter. The performance of the proposed converter is compared to that of a popular three-phase DC-DC boost converter that was first proposed in [15]. This comparison is done with traditional silicon (Si) devices and newer silicon carbide (SiC) devices. It should be noted that wide bandgap SiC and GaN devices represent the future when it comes to semiconductor technology, but traditional silicon (Si) devices continue to be used as they are considerably cheaper and more available.

3.1 Experimental results

A prototype of the proposed converter was implemented and tested to confirm the converter's feasibility with the following specifications: V_{in} = 48V (nominal value), output voltage V_o = 360V, output power P_o =1.5kW and switching frequency f_s = 50 kHz; more details of the converter's specifications and key parameters that have been calculated and designed in the previous section are shown in Table I. A switching frequency of 50 kHz has been used for this work as it has been in several other previously published papers. 50 kHz is a frequency that is sufficiently high to reduce the size of magnetic elements and filter capacitors, but sufficiently low to minimize the effects of noise and parasitics on the operation of the converter.

Figure 3.1 shows typical waveforms for the power stage of the proposed converter. The gating signals for the main switches (S_1−S_3) of the proposed converter is shown in Figure 3.1(a). It can be seen that these signals are phase-shifted by 120^o by each other. Figure 3.1(b) shows the voltage and current waveforms for one of the main switches. It can be seen that the level of the current waveform is changed when the switch is on. The change of the current amplitude is due to turning on or off of the other main switches. Figure 3.1(c) shows the voltage waveform across one primary of the main the main transformer. It can be seen that the waveform has zero voltage regions due to two of the main switches

being on. When just one of the main switches is on and the other two are off, the voltage across the primary is positive or negative. The voltage level depends on the difference between the voltage applied on each phase of the transformer.

Table I: Specifications and key parameters the proposed prototypes

Main switches S_1-S_3	(Si): FDL 100N50F
Clamping switch S_c	(Si): FDL 100N50F
Clamping diodes D_{c1}-D_{c3}	ETL0806
Three-phase output bridge rectifier	U1560
Leakage inductances L_{k1}-L_{k3}	2μH
Clamping capacitor	150nf
Output capacitor C_o	500μf
Main transformer turns ratio (N_2/N_1)	3
Flyback transformer turns ratio (N_s/N_p)	6
Input boost inductors L_1-L_3	280μH
Duty cycle of power converter, D	0.6
Duty cycle of flyback converter	0.27
Peak current of each main switch, I_{spk}	34.72A
Average current of each main switch, $I_{s,avge}$	11.57A
RMS current of each main switch, I_{sRMS}	16.09A
Average current of clamping switch I_{scavg}	0.785A
RMS current of clamping switch I_{scRMS}	1.55A
Maximum voltage of clamping capacitor V_{cmax}	164V
Minimum voltage of clamping capacitor V_{cmin}	120V
Flyback power rating	150W

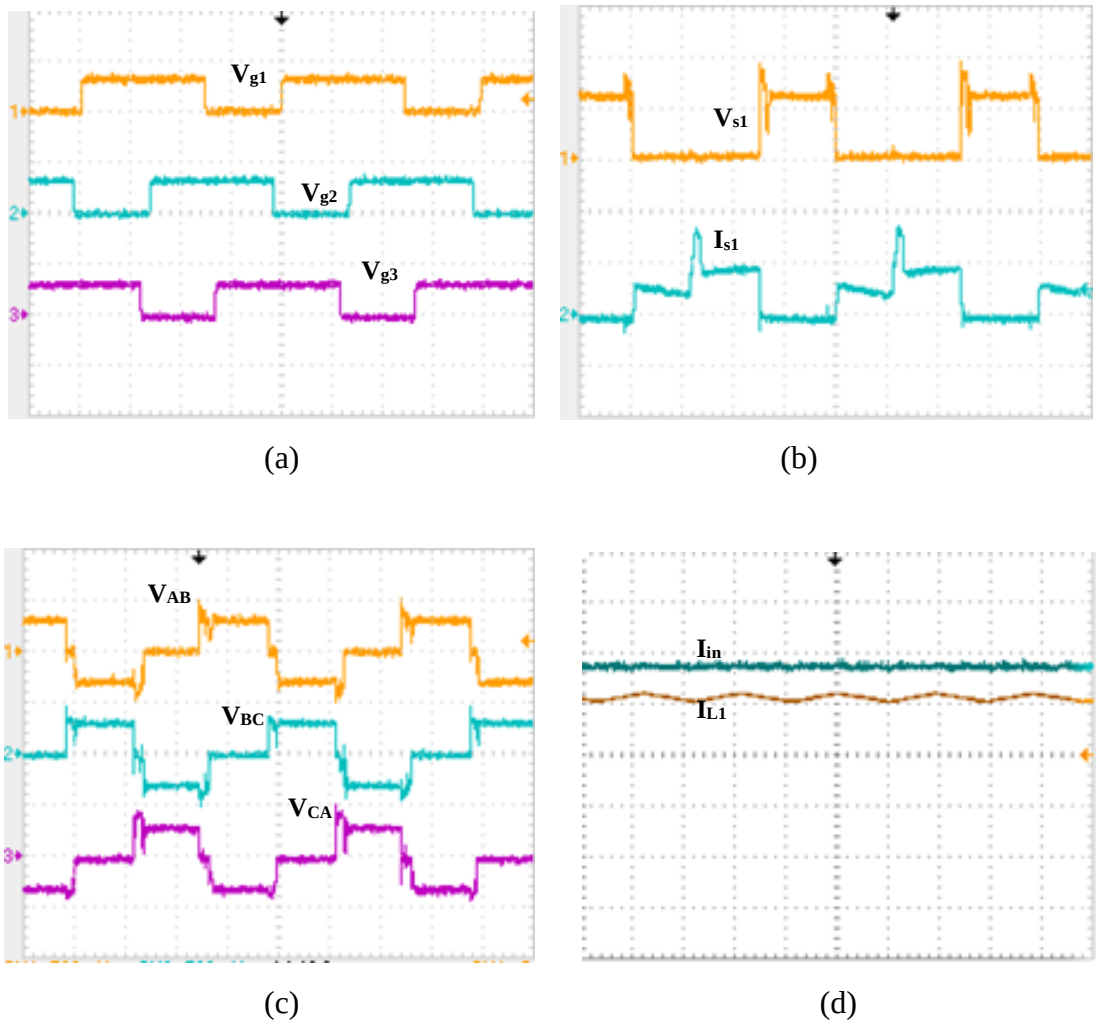
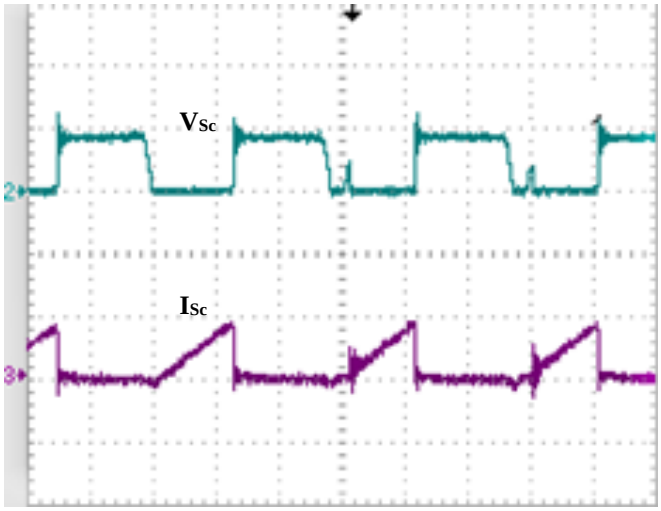
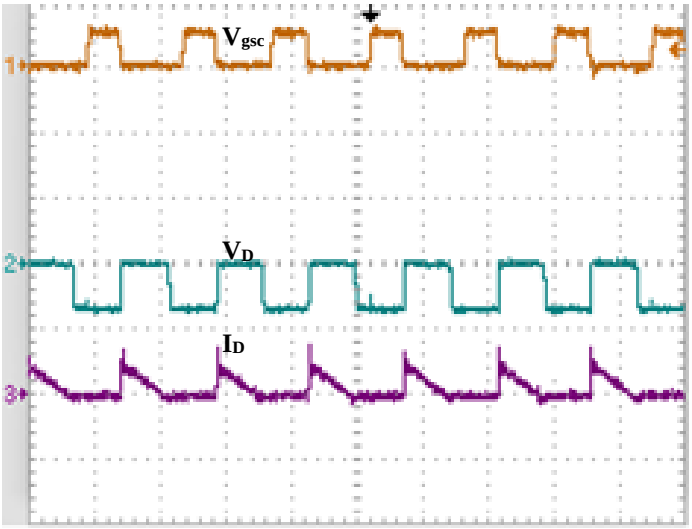


Figure 3.1: Typical converter waveforms at maximum Load at D=0.6: (a) Gating signals of main switches (V : 20V/div., t : 5µs/div., (b) The voltage across the main switch and the current through it (V : 100V/div, I : 20A/div., t : 5µs/div.,), (c) Primary voltage waveforms across the transformer (V : 200V/div., t : 5µs/div..), (d) The input current and the current through one of the boost inductors (I_{in}: 20A/div., I_{L1}: 10A/div., t : 10µs/div.).



(a)



(b)

Figure 3.2: Flyback snubber circuit waveforms: (a) the voltage across the flyback switch and the current through it (V: 200V/div., I : 10A/div., t : 2.5µs/div), (b) gating signal and output diode voltage and current for flyback snubber (V g : 50V/div., V_D : 1000V/div., I_D : 2A/div., t : 5µs/div

Figure 3.1(d) shows the input current of the DC source and the current the current through one of the main inductors. Since an interleaved topology is used in the proposed converter, the ripple of the input current is reduced significantly compared to the current that through in one of the input inductors.

Figure 3.2 shows the waveforms for the flyback snubber circuit. It can be seen that the current of the flyback switch is rising when the flyback switch is turned on as shown in Figure 3.2(a) and there is no current flow through the output side as shown in Figure 3.2(b). Energy is thus stored in the magnetizing inductor of the flyback transformer. When the flyback switch is turned off, the output diode of the flyback snubber conducts as shown in Figure 3.2(b); thus, energy is released to the high voltage side of the converter.

3.2 Comparison and discussion

Based on the experimental and on simulation and investigative work performed on the proposed converter and on the converter that proposed on [15], a comparison of the three three-phase DC-DC converters discussed in this section can be made. In this section, a brief description of each converter is presented, and their features are stated. In addition, the comparison results will be presented and discussed using different types of semiconductor devices.

3.2.1 Three-Phase DC-DC Boost Converter with Three-Switch Active Clamp

The converter that will be used to compare the performance and characteristics of the proposed three-phase DC-DC converter (see Figure 3.3) is shown in Figure 3.3. This converter consists of three main switches, S_1-S_3, three input inductors L_1-L_3, a three-phase high-frequency transformer, a three-phase full-bridge rectifier with diodes D_1-D_6, and an output filter capacitor C_o. It also has a three-phase active-clamp auxiliary circuit that consists of switches S_{c1}-S_{c3} and clamp capacitor C_c.

This converter is essentially a set of three interleaved DC-DC boost converter combined with a three-phase transformer. The basic operation depends on the following PWM strategy:

- The main switches (S_1-S_3) are operated with gating signals phase shifted by 120˚ with respect to each other.

- Two of the main switches (S_1-S_3) are turned on and one is turned off; thus, two of the input inductors share energy from input DC source and the energy is transferred to the output from the other inductor through one phase of the transformer.

- One of the main switches that was on is turned off and the voltage across it is clamped to the voltage across the clamping capacitor C_c due to the interaction between the leakage inductance of the transformer and the clamping capacitor. During that switch S_c can be turned on with ZVS, which results in fewer switching losses.

- Switch S_c is turned off before the other main switch is turned on. The output capacitor of the main switch is discharged, and its body diode will conduct. Thus, this main switch can be turned on with ZVS (which results in fewer switching losses) and the next third of the cycle will begin.

Details about the operation of this converter can be found in [15].

3.2.2 Comparison results

In this section, a comparison between the two converters is made based on the comparison of the two converters made based on efficiency, cost, simplicity, switching frequency. In order to verify the performance and make comparison between the converters, two prototypes were implemented experimentally and the efficiency of the two converters were measured for different output loads. V_{in} = 48V (nominal value), output voltage V_o = 360V, output power P_o =1.5kW and switching frequency f_s = 50 kHz; more details are shown in table II.

Figures 3.5 to 3.9 show the efficiency comparison of the two converters using Si devices and SiC devices.

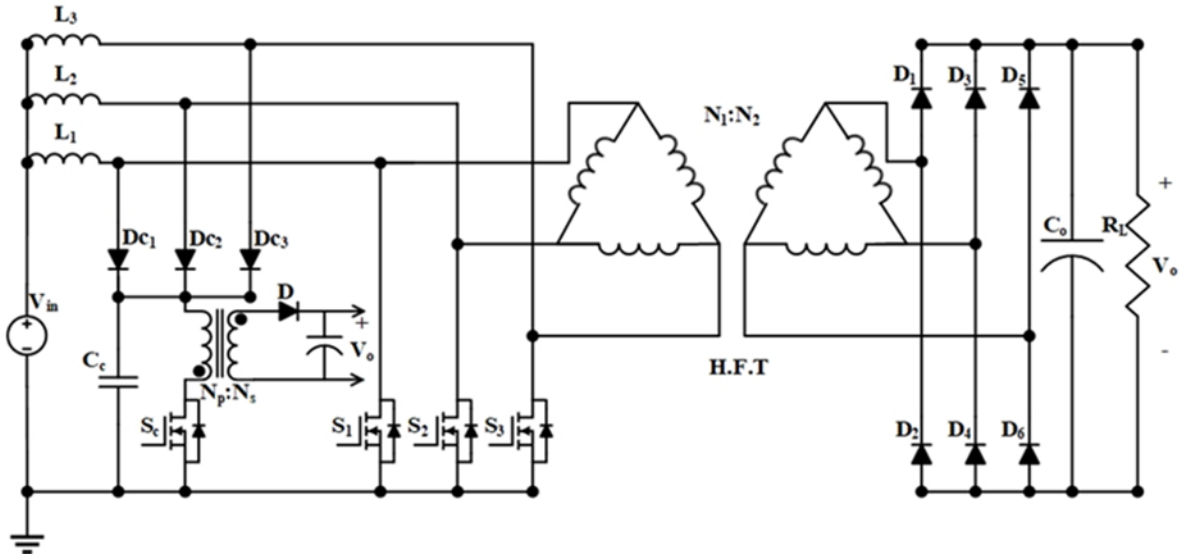


Figure 3.3: Proposed three-phase DC-DC converter

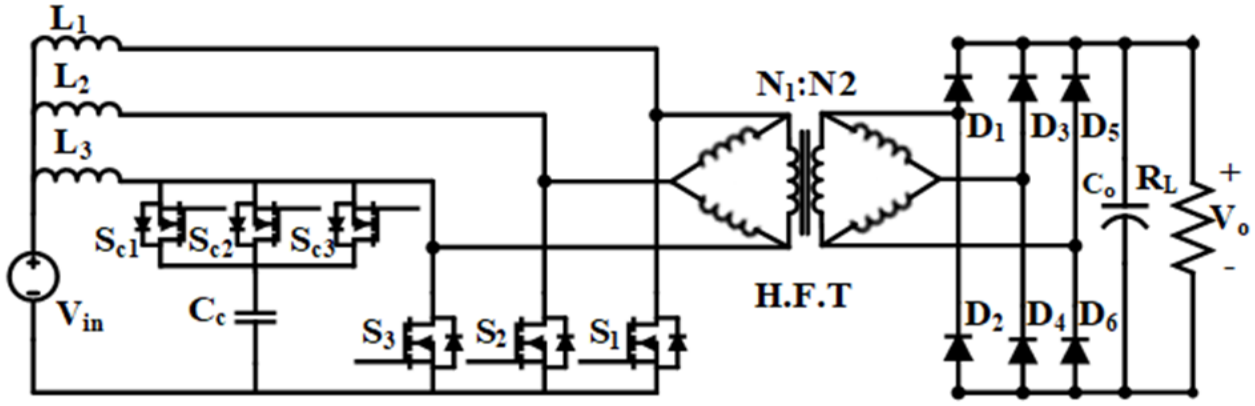


Figure 3.4: Three-phase interleaved DC-DC converter with active clamp that proposed in [15]

Table II: Specifications of the proposed converter and the three-phase with active clamp

Component	Proposed converter	Converter in [15]
Main switches S_1-S_3	(Si): FDL 100N50F	(Si): FDL 100N50F
	(SiC): SCT3060	(SiC): SCT3060
Clamping switches S_{c1}-S_{c3}	----------	(Si): FDL 100N50F
	----------	(SiC): SCT3060
Clamping switch S_c	(Si): FDL 100N50F	----------
	(SiC): SCT3060	----------
Clamping diodes D_{c1}-D_{c3}	ETL0806	----------
Three-phase output bridge rectifier	U1560	U1560
Leakage inductances L_{k1}-L_{k3}	2μH	3.5μH
Clamping capacitor	10 μf	160 nf
Main transformer turns ratio (N_2/N_1)	3	3
Flyback transformer turns ratio (N_s/N_p)	6	----------
Input boost inductors L_1-L_3	280μH	280μH

Figure 3.5 shows the efficiency of the proposed converter. It can be seen that the maximum efficiency of the proposed converter achieved under half load condition (≈94%). When the converter is operating under full load condition, more conduction losses will result and the efficiency becomes 92%. It should be noted that although the proposed converter is a single-stage converter, its efficiency is comparable to a two-stage converter that processes power twice during its power conversion process, but it is much less expensive.

Comparison efficiency curves between the proposed converter and the three-phase with active clamp using Si devices is shown in Figure 3.6. It can be seen that, under heavy load condition, the proposed converter is less efficient than the converter with active clamp that is because the advantages of ZVS. In contrast, under light load of operation, both of the converters work without ZVS, thus the proposed converter is more efficient. However, the efficiency of the proposed converter is less by ≈1.5% of the more sophisticated and more expensive three-phase with active clamp converter for a load range of 1.5kW.

Figure 3.7 illustrates comparison efficiency curves for the proposed converter using Si and SiC devices. It can be seen that the efficiency is significantly improved when SiC MOSFETs are used. The efficiency improvement by changing the Si MOSFETs devices SiC MOSFETs is about 3% at light load and 1% at heavy load of operation. As it can be noted from this measuring data that the efficiency is dramatically improved at light load because Si devices have more switching losses that SiC devices. By increasing the output load, the devices will carry more current and that will cause more conduction losses. As a result, the efficiency of SiC devices will be slightly reduced.

A comparison efficiency curves of the three-phase converter with active clamp by using Si and SiC devices are shown in Figure 3.8. it can be seen that the effect ZVS topology has neglected effect on the converter by changing Si devices with SiC devices. The only impact that can be observed is when the converter operates at low output power. This is because the converter will operate with no ZVS and SiC devices become more efficient than Si devices.

Figure 3.9 shows the comparison efficiency curves between the proposed converter is compared with three-phase DC-DC converter with active clamp using SiC devices. It can be seen that the proposed converter has the same efficiency of the converter with active clamp during most of the load operation. In addition, the proposed converter is higher efficient at light load of operation and that is because both of the converters operate with no ZVS and more conduction losses are present in the converter with active clamp circuit as it has more switches. The proposed converter, however, has slightly less efficiency

than the other converter at heavy loads because the proposed converter has switching losses whereas the active clamp converter works with ZVS. In short, the efficiency of the proposed converter significantly improved by using SiC devices compared with the converter with active clamp. This is because the proposed converter has fewer active switches and the other converter lose the ZVS benefits by using SiC devices.

Based on the experimental work performed on the proposed converter and on simulation and investigative work performed on the other converters, a comparison of the three three-phase DC-DC converters discussed in this chapter can be made. Such a comparison is presented in Table III.

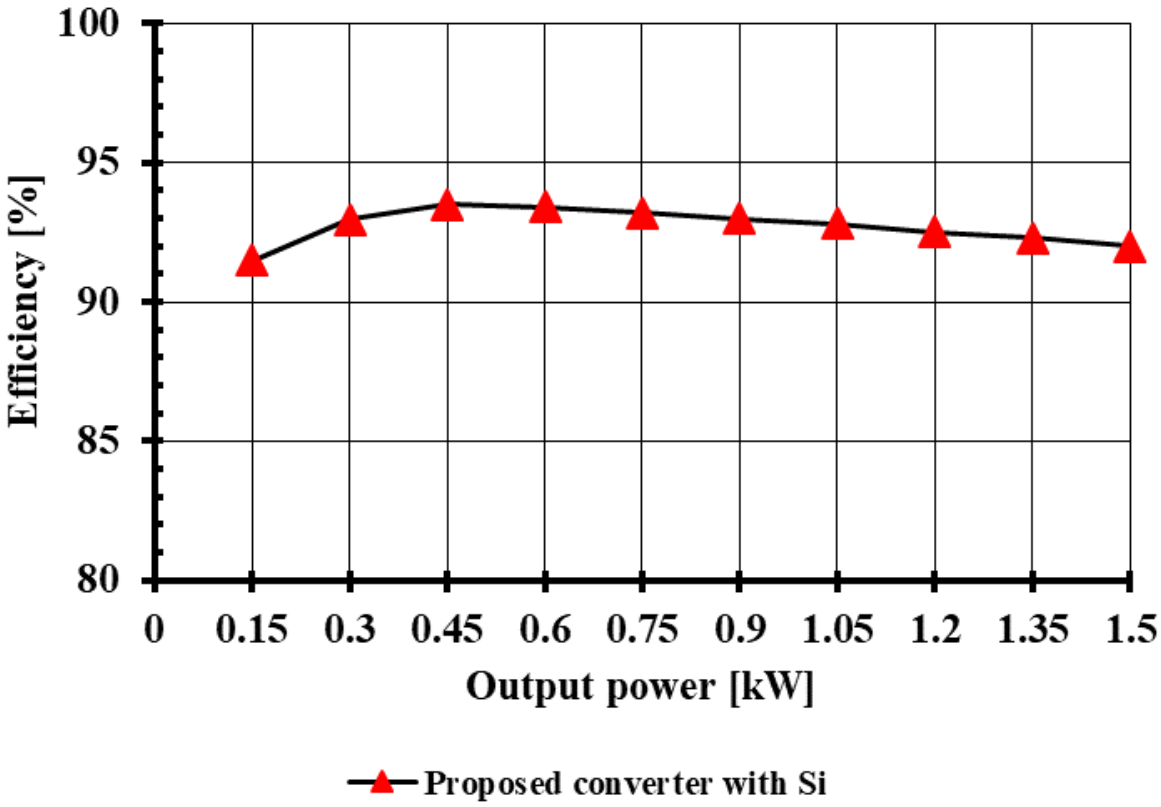


Figure 3.5: Efficiency curves of the proposed converter using Si devices

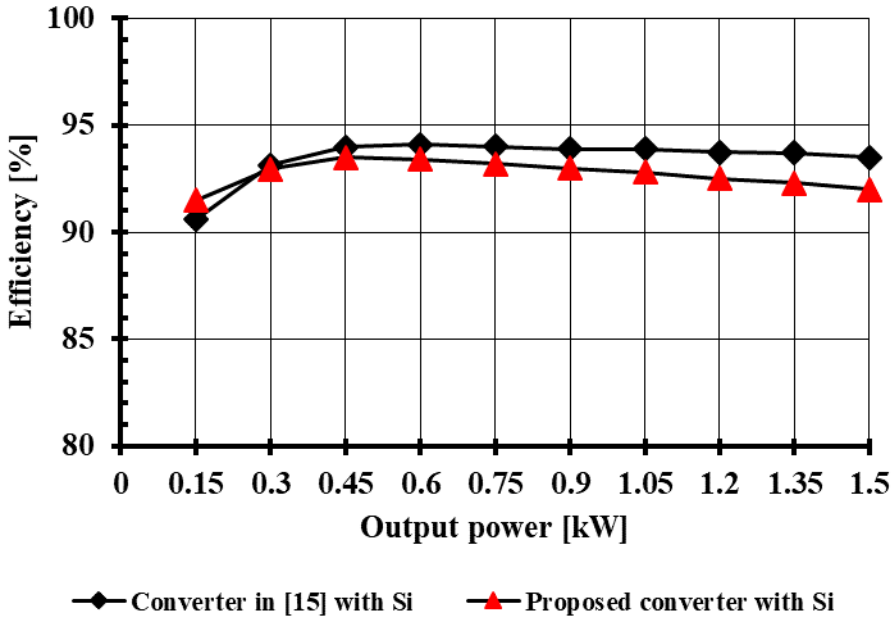


Figure 3.6: Efficiency curves of the proposed converter and converter in [15] using Si devices

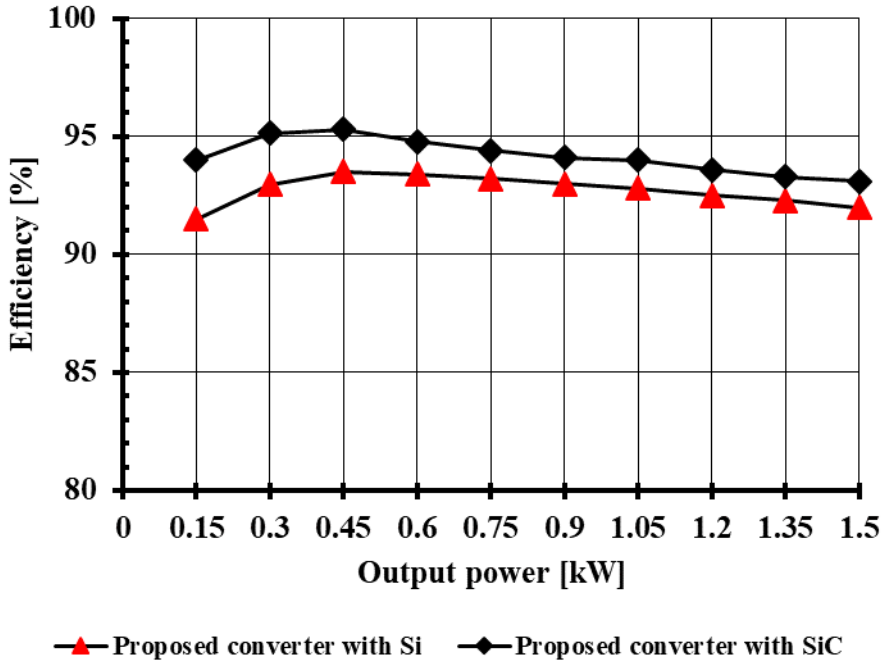


Figure 3.7: Efficiency curves of the proposed converter using Si and SiC devices

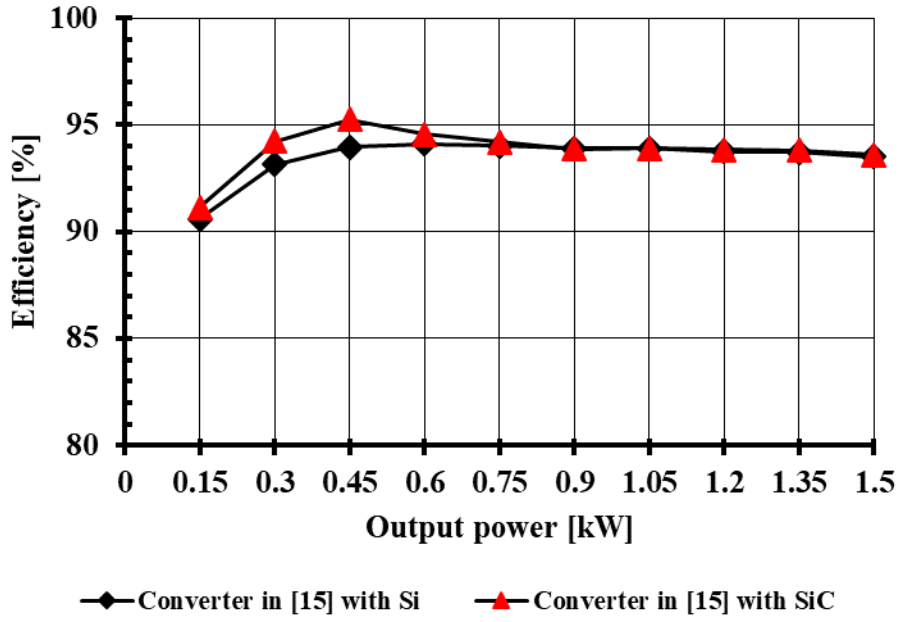


Figure 3.8: Efficiency curves of the converter in [15] using Si and SiC devices

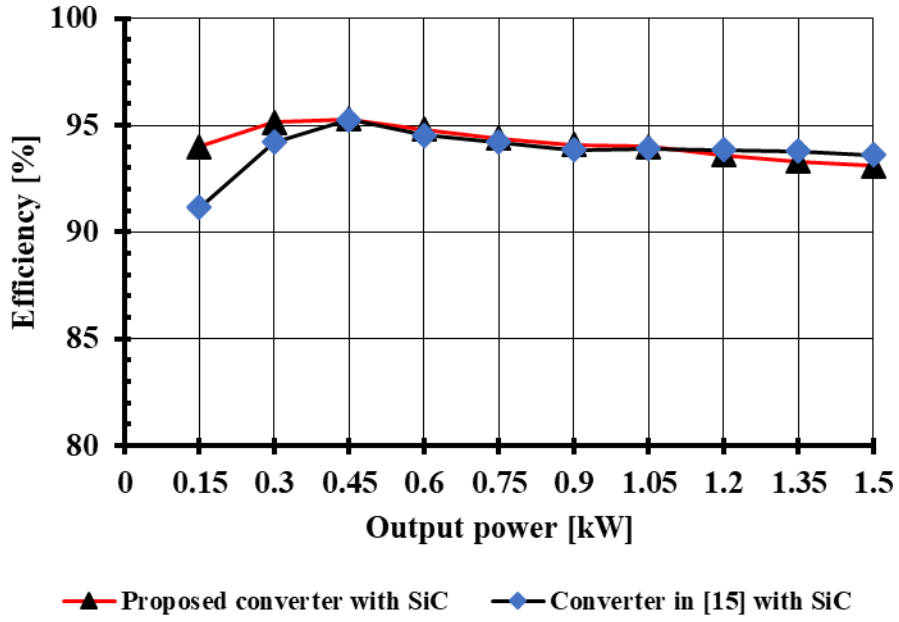


Figure 3.9: Efficiency curves of the proposed converter and converter in [15] using SiC devices

Table III: Comparison of the two three-phase DC-DC converters

Topology	**Converter with active clamp [15]**	**Proposed converter**
Cost & Simplicity	Converter requires 3 main switches, 3 active clamp switches, and 3 floating gate drive circuits.	Converter requires 3 main switches and an active clamp switch with some passive components. Converter requires no floating gate circuits.
Efficiency	Converter can operate with ZVS due to the presence of the active clamp in the converter. Converter has higher efficiency at higher loads than proposed converter as it operates with ZVS, but has lower efficiency at lighter loads as it loses ZVS capability.	Converter cannot operate with ZVS and is thus the least efficient of the three converters. The difference in efficiency is insignificant for lighter loads as none of the converters operates with ZVS, but becomes more significant for heavier loads.
Switching Frequency	The switching frequency of the converter is limited by the operation of the active clamp circuit as it must be turned on 3 times within a switching cycle. The operation of the active clamp is not independent of the operation of the main converter switches.	The operation of the flyback snubber is independent of the operation of the main converter switches.

3.3 Conclusion

Experimental results obtained from a prototype of the proposed converter that was introduced in Chapter 2 were presented. Key experimental waveforms were shown as well as efficiency results. These efficiency results were compared to those obtained of a representative active-clamp type three-phase DC-DC converter operating with conventional silicon (Si) semiconductor devices. Further comparisons were made between experimental prototypes that were built with silicon-carbide (SiC) devices that are said to offer better performance than Si devices, but are less readily available and more expensive. Based on the experimental work presented in this chapters, conclusions related to the efficiency of the proposed converter vs that of the active-clamp converter and the efficiency of Si-based converters vs SiC based converters were made.

The proposed converter is less efficient than the active-clamp converter when operating with heavy loads. This is because the active-clamp converter switches can turn on with ZVS, but the switches in the proposed converter cannot. Since the switches in the

proposed converter do not turn on with ZVS, they have turn-on switching losses that the switches in the active-clamp converter do not have so that the proposed converter operates with less efficiency. This difference in converter efficiency is somewhat offset by the fact that the proposed converter has only four switches while the active-clamp converter has six switches so that the proposed converter has fewer turn-off switching losses.

The efficiency of the proposed converter implemented with newer silicon-carbide (SiC) devices that have fewer switching losses was to compared to the efficiency of the same converter implemented with traditional, lower cost silicon (Si) devices that have more switching losses than SiC devices. A similar comparison was done for the active-clamp converter. It was found that the difference in efficiency between the two implementations of the proposed converter was about 2% while the difference between the two implementations of active-clamp converter was insignificant except for some light loads. The reason for this is that SiC devices help reduce switching losses. The active clamp converter operates with ZVS with heavy loads and thus has no switching losses while the proposed converter does not operate with ZVS. As a result, implementing the proposed converter with SiC devices result in a decrease in such losses and an increase in efficiency while there are few, if any, switching losses that the SiC devices can reduce for the active clamp converter. The use of more expensive SiC devices can be justified in converters that operate without ZVS. There is less justification for their use in converters that are already operating with ZVS.

Chapter 4

4 A Single-Phase ZVS AC-DC Boost Converter with Interleaved Input

AC-DC power conversion is typically done using two separate converters, but this can be expensive. Single-stage converters using a single converter have therefore been proposed to reduce cost, but they have several drawbacks, including an input current that is discontinuous with high current peaks. A new single-phase, single-stage AC-DC converter with interleaved input is proposed in this chapter. The converter's operation is explained and analyzed, and a design procedure is presented. Results obtained from an experimental prototype of the proposed converters are also presented in the chapter.

4.1 Converter Operation

The proposed single-stage converter in Figure 4.1 has been synthesized by combining an AC-DC interleaved boost converter with a DC-DC three-phase converter. It has three main switches, S_1–S_3, a diode bridge, three boost inductors, L_1-L_3, a transformer, an output bridge rectifier and an output capacitor C_o. A clamping network made up of switches, S_{c1} - S_{c3} and capacitor C_c is connected to the converter's main switches.

The main converter switches have identical gating signals that are shifted 120^o with respect to each other. The input current is generally continuous even though each input inductor current is discontinuous because of interleaving. While the input AC-DC section

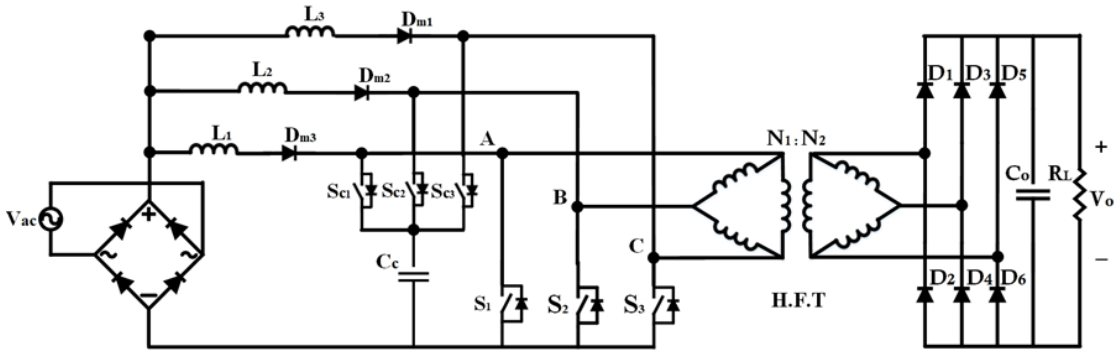


Figure 4.1: Proposed interleaved AC-DC single-stage converter

is working, voltage is impressed across the primary of each phase of the transformer. This voltage is rectified and fed to the output through the output diode bridge.

A three-phase active clamp clamps any overvoltage spikes that might appear due to the interaction of the transformer's leakage inductance and the output capacitances of the main switches. The clamping circuit operates like any active clamp used in lower power DC-DC converters. A converter switch can be made to turn on with ZVS by using energy in the clamping capacitor that is transferred to the transformer by the turning on of an active clamp switch that is connected to the same phase. When this particular active clamp switch is turned off, the energy that was released is used to discharge the switch's output capacitance so that it can be turned on with ZVS eventually.

It should be noted that unlike the topology that was presented in Chapter 2, the switches in this topology are exposed to higher voltages and thus will have higher turn-on switching losses; it must be implemented with some sort of ZVS method. Since the topology in Chapter 2 cannot operate with ZVS, its switching losses would be high it was modified to operates as an off-line AC-DC converter. As a result, the proposed topology is more suitable for this application.

The modes of operation during a third of a steady-state switching cycle are explained in this section. Typical converter waveforms are shown in Figure 4.2 and circuit diagrams for each mode are shown in Figure 4.3. The modes of operation are as follows:

Mode 1 [$t_0 < t < t_1$]: Switches S_1, S_2 and S_{c3} are on before this mode begins. This mode starts at $t=t_0$ with the turning off of S_1. The boost inductor current of phase A charges the parasitic capacitor of switch S_1. When the voltage across S_1 reaches the clamp capacitor voltage V_{Cc}, the body diode of S_{c1} starts conducting and the voltage across switch S_1 is clamped to the voltage across C_c, V_{Cc}. Transformer primary voltage V_{AB} becomes equal to V_{Cc}. and transformer primary voltage V_{CA} becomes zero. Transformer secondary voltage V_{ab} becomes zero, V_{ca} becomes V_o and V_{bc} does not change so that the reflected voltages of phases ab, bc and ca across the transformer's primary are zero, $-\overline{V_o}$ and $\overline{V_o}$ respectively. While this is happening, the transformer primary current of phase A, I_a, is increasing as its slope depends on V_{Cc} and the phase C current, I_c, decreases as its slope is

determined by the reflected voltage $\overline{V_o}$. Energy transfer to the output is done through the transformer's phase C and D_2, D_4 and D_5. Some time (t_0-t_1) is needed to clamp the voltage across the main switch, to prevent any overvoltage spike that may be caused by the presence of leakage inductance from appearing.

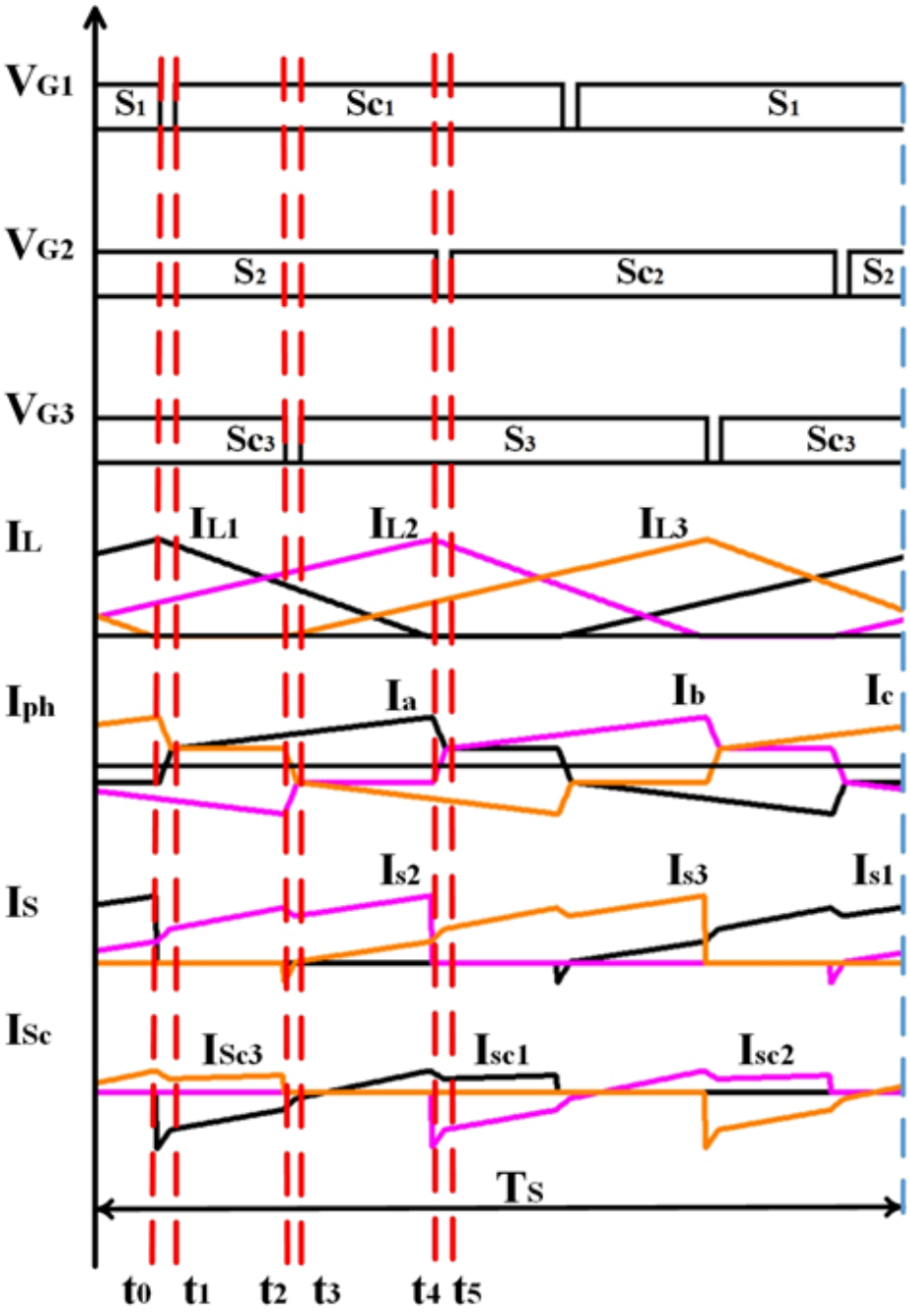


Figure 4.2: Typical converter waveforms

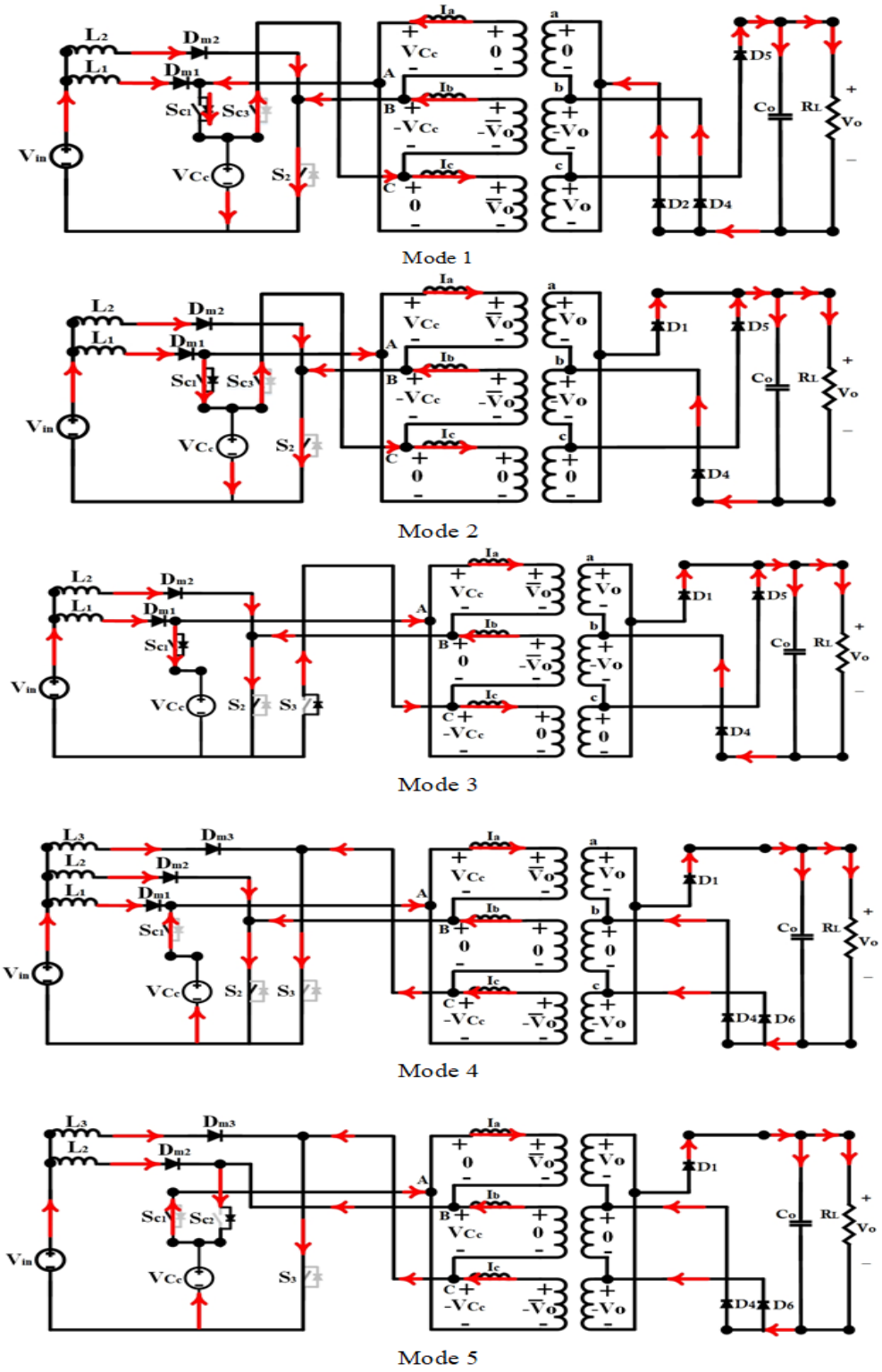


Figure 4.3: Modes of operation

The current through the primary transformer's phase A, which flows through leakage inductance L_k can be expressed as

$$i_a(t) = \frac{V_{C_c}}{L_k} t + i_a(t_0) \tag{4.1}$$

The duration for this mode can be expressed as

$$t_1 - t_0 = \frac{i_a(t_1) - i_a(t_0)}{\left(\frac{V_{C_c}}{L_k}\right)} \tag{4.2}$$

Mode 2 [$t_1 < t < t_2$]: When this mode begins, the current through the transformer's phase C current, I_c, becomes constant, its phase A current, I_a, continues to increase, and its phase B current, I_b, continues to decrease. Energy is transferred to the output through diode D_1. Secondary voltage V_{ab}, changes from zero to V_o and is reflected to the primary as $\overline{V_o}$. Secondary voltage V_{ca}, changes from V_o to zero and the reflected voltage across the primary becomes zero. Clamping switch S_{c1} can be turned on with ZVS sometime during this mode as current flows through its body diode. The transformer's phase A current, I_a, is increased as its slope is dependent on the difference between V_{Cc} and the reflected voltage $\overline{V_o}$.

Mode 3 [$t_2 < t < t_3$]: Switch S_{c3} is turned off at $t=t_2$ to start this mode. The transformer's phase C current, I_c, begins to decrease while that of phase B, I_b, starts increasing. The parasitic output capacitor of S_{c3} starts to discharge during this mode and interacts with the leakage inductances of the transformer. The body diode of S_3 starts to conduct after this capacitor is fully discharged, and S_3 can be turned on with ZVS sometime soon afterwards. Voltages V_{BC} becomes zero and V_{CA} becomes $-V_{Cc}$ during this mode.

Mode 4 [$t_3 < t < t_4$]: At the beginning of this mode, switch S_3 can be turned on with ZVS. The transformer primary current of phase B, I_b, is greater than that of phase C, I_c, so that output diode D_5 stops conducting and D_6 begins conducting. Consequently, the reflected voltages across the primary from secondary voltages, V_{bc} and V_{ca}, become zero and $-\overline{V_o}$ respectively. The transformer primary current phase A, I_a, continues to increase and that of phase C, I_c, continues to decrease as their slope is determined by the difference between $\overline{V_o}$ and V_c. The transformer's phase B current, I_b, becomes constant. At the end of this mode, current I_a, reaches its maximum value.

Mode 5 [$t_4 < t < t_5$]: Main switch S_2 is turned off at $t = t_4$ and the next third of a switching cycle starts. The converter operates as in Mode 1 during this mode except switch S_{c1} is turned on and the body diode of S_{c2} conducts instead of S_{c3} being turned on and the body diode of S_{c1} conducting. Energy is transferred to the output through output diodes D_1, D_4 and D_6.

4.2 Converter Features

The proposed single-phase AC-DC single-stage converter has the following features:

- Single-stage AC-DC power conversion can be done by using just six converter switches: three main power switches and three active clamp switches.
- The converter switches can operate with ZVS
- Voltage spikes that would otherwise appear due to the interaction of transformer leakage inductance and switch output capacitance are easily clamped due to the presence of clamping capacitor C_c.
- The input current is continuous as the converter’s input section consists of three interleaved boost modules.
- The operation of the converter is simple as it can be operated like an interleaved boost converter.
- No sophisticated or non-standard methods of control are required.

4.3 Steady State Analysis

The significant parameter that must be derived from an analysis of the proposed converter is the clamping capacitor voltage V_{cc} (i.e. The storage-capacitor voltage), because it is only than other parameters such as input current and duty cycle can be determined. Since the proposed converter is a single stage AC-DC converter, the voltage across the capacitor can be derived by noting that an energy equilibrium must be exist for clamping capacitor C_c when the converter is in steady-state operation.

Since there are various possible combinations of output input modes, V_{cc} cannot be determined by an equation with a closed-loop solution; but must instead be determined using a computer program.

The following assumptions are made for the steady state analysis:

- All semiconductor devises are ideal.
- dead times between switching transitions are neglected in the analysis as these times are very short compared to power transfer mode.
- The switching frequency is much higher than the power line frequency, and thus the input ac voltage can be considered constant during the switching cycle.
- The input inductor currents are discontinues and they operate under discontinuous conduction mode, DCM.
- The voltage across the clamping capacitor is constant as V_{cc}.
- The magnetizing inductors of the transformers are very large, and their effect are negligible.
- Since the three interleaved converters are theoretically identical, only the analysis of one phase will be shown.

For an operating point with given an input voltage, output voltage, switching frequency, input inductor, leakage inductor, transformer turns ratio, and output power, the voltage across the clamping capacitor can be determined as follows:

1) Assume a duty cycle as an initial "guess" (ex. 0.5)

2) Calculate the minimum value of the clamping voltage that guarantees the input inductor current operates on discontinuous mode.

This value is calculated by applying volt-second balance in the inductor current in steady state and then find the relation between clamping voltage and input ac voltage as

$$\frac{V_{cc}}{|v_{in,k}|} = \frac{D + \Delta_{s,k}}{\Delta_{s,k}} \tag{4.3}$$

where $|v_{in,k}|$ is the rectified AC supply voltage during switching cycle interval k, D is the duty cycle of and it is represented when one of the main switches is turned on, and $\Delta_{s,k}$ is the duration when the input inductor current becomes zero during switching cycle interval k.

In order to make sure that the input inductor current is discontinuous, $\Delta_{s,k}$ must satisfy the expression $\Delta_{s,k}$ <1-D at any interval k and load conditions. Using (4.3), the minimum value of clamping voltage is obtained as

$$V_{cc,min} = \frac{|v_{in,k}|}{(1 - D_{max})} \tag{4.4}$$

3) Determined the voltage across the clamping capacitor:

The voltage across the clamping capacitor is derived by applying voltage-sec balance on the leakage inductance current of the transformer and by consider that the sum of the average leakage inductor current of three phases is equal to the average load current referenced at the primary as in (4.5) and (4.6).

It should be noted that the proposed converter has three different regions of operation, and the current through the leakage inductance depends on which region the converter is operated.

$$\frac{3(1-D)^2 T_s}{L_{Lk}}\left(\frac{nV_{Cc}}{V_o}-1\right)V_{Cc} = n\frac{V_o}{R_L} \qquad for\ D > 0.3 \tag{4.5}$$

$$\frac{3D^2 T_s}{L_{Lk}}\left(\frac{nV_{Cc}}{V_o}-1\right)V_{Cc} = n\frac{V_o}{R_L} \qquad for\ D \leq 0.3 \tag{4.6}$$

From (4.5) and (4.6), the voltage across the clamping capacitor is obtained as

$$V_{Cc} = \frac{1}{2n}\left(V_o + \sqrt{V_o^2 + \frac{4P_o n^2 L_{Lk} f_s}{3D_c^2}}\right) \tag{4.7}$$

where, D_c is equal to (1-D) for D>0.3 and is equal to D for D≤ 0.3, n is the main transformer turns ratio ($n=N_2/N_1$), P_o is the output power, and f_s is the switching frequency, and L_{Lk} is the leakage inductance of one phase of the transformer ($L_{Lk}=L_{Lk1}=L_{Lk2}=L_{Lk3}$).

If V_{cc} that determined in this step more than the minimum value in step 2 then go to the next step, otherwise change the value of the duty cycle.

4) with known V_{cc}, the average current that flows out of the clamping capacitor through the leakage inductance of the transformer during a half-line cycle is obtained as

$$I_{A(avg)} = \left(V_{cc} - \frac{V_o}{n}\right)\frac{D_c^2}{L_{Lk}f_s} \tag{4.8}$$

5) Determine the average current that is fed from the input to during a half-line cycle using (4.9)

$$I_{L_{in1}(avg)} = 2f_{in}\sum_{k=0}^{m}\int_{t^*}^{t_k}[I^*_{in1,k} - \frac{V_{C_c} - |v_{in,k}|}{L_{in}}(t - t^*)]dt \tag{4.9}$$

where $m=(f_s/2f_{in})$, f_s is switching frequency, f_{in} is the line frequency, L_{in} is the input inductor for one phase ($L_{in}=L_1=L_2=L_3$), and $I^*_{in1,k}$ is the peak current of one input inductor during a switching cycle k, just when switch S_1 (or any of other main switches S_2, S_3) is turned off at time $t= t^*=t_0$ (Figure 4.2).

6) If (8) and (9) are equals, then the converter is operating under steady-state conditions and the value of V_{cc} that has been calculated is valid. If not, the procedure must be repeated for different value of D. if $I_{Lin(avg)}>I_{A(avge)}$, repate with a smaller value of D; if $I_{Lin(avge)}<I_{A(avge)}$ then repeat with a larger value of D.

4.4 Converter Characteristics

The procedure that described in Section 4.3 can be repeated to determine the voltage across the clamping capacitor V_{cc} or any other parameters for other operating points. So, graphs for steady state characteristics curves can be generated for design purposes. It is observed that from (4.7), (4.8) and (4.9) the operating characteristics of the converter at

any given input and output voltage are dependent on three key parameters: transformer turns ratio, input inductance L_{in} and leakage inductance $L_{Lk.}$ The following steady state characteristics can be determined:

1) Figure 4.4 shows the effect of transformer turns ratio ($n=N_2/N_1$) on the clamping capacitor with different load conditions and all other parameters keep constant. It is clear that the clamping capacitor voltage remains constant regardless what the load is. It is significantly dependent on the ratio of the transformer

2) As the input voltage increase, the clamping voltage increases also to maintain the energy balancing of the clamping capacitor as shown in Figure 4.5.

3) Figure 4.6 shows the effect on the input inductor on the clamping voltage. It is clear that the clamping voltage keeps constant under all load conditions. That is because the input current is discontinuous. By changing the input inductance, it is clear that there is no significant effect of the input inductor on the clamping voltage value.

4) By increasing the leakage inductance of the transformer, the clamping voltage is slightly increased. when the leakage inductance increases means more voltage will appear across it. This results more voltage will apply across the clamping voltage as shown in Figure 4.7.

4.5 Design Procedure and Example

The proposed converter is a single-phase, single-stage AC-DC converter with three interleaved boost converter that is connected to an isolated high frequency transformer and this section named as power stage. The power stage of the converter is connected to an active clamp circuit that contents of three switches and clamping capacitor.

The design of the proposed converter is discussed in this section and demonstrated with an example of the selection of certain key parameters.

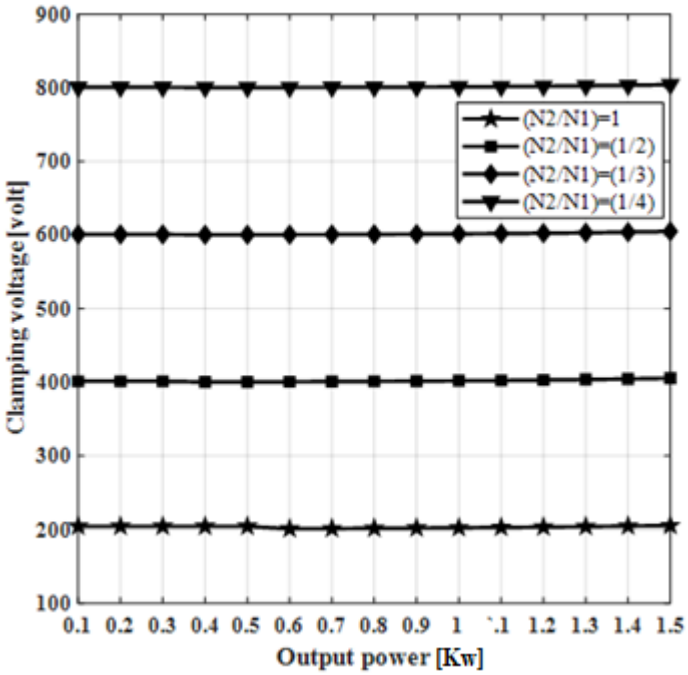


Figure 4.4: Effect of transformer ratio value n on clamping voltage (V_{in}=90 V_{rms}, V_o=200V, f_s=50KHz, L_1=100µH, L_{k1}=10µH)

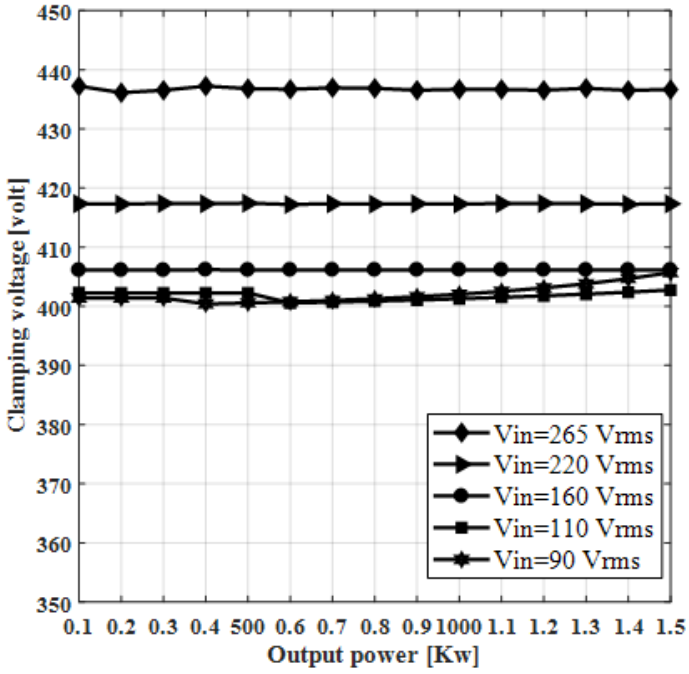


Figure 4.5: Effect of input voltage on clamping voltage (n=0.5, V_o=200V, f_s=50KHz, L_1=100µH, L_{k1}=10µH)

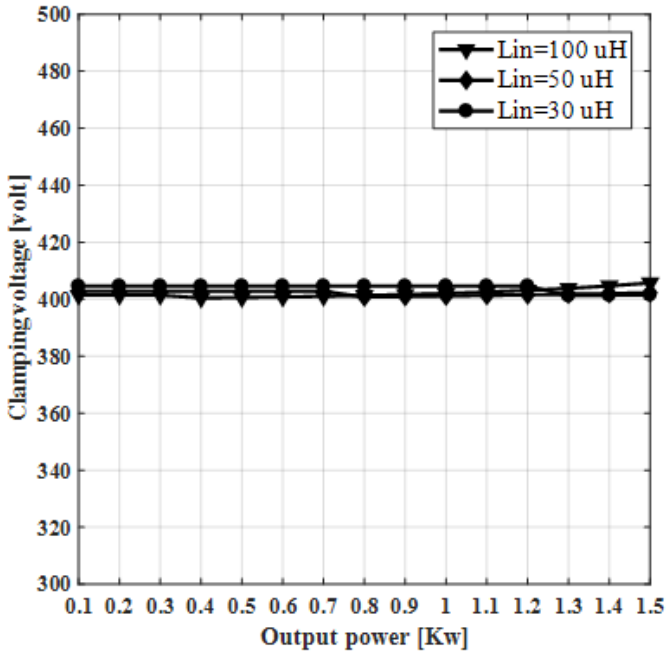


Figure 4.6: Effect of input inductor on clamping voltage (Vin=90 Vrms, n=0.5, V_o=200V, f_s=50KHz, L_{k1}=10µH)

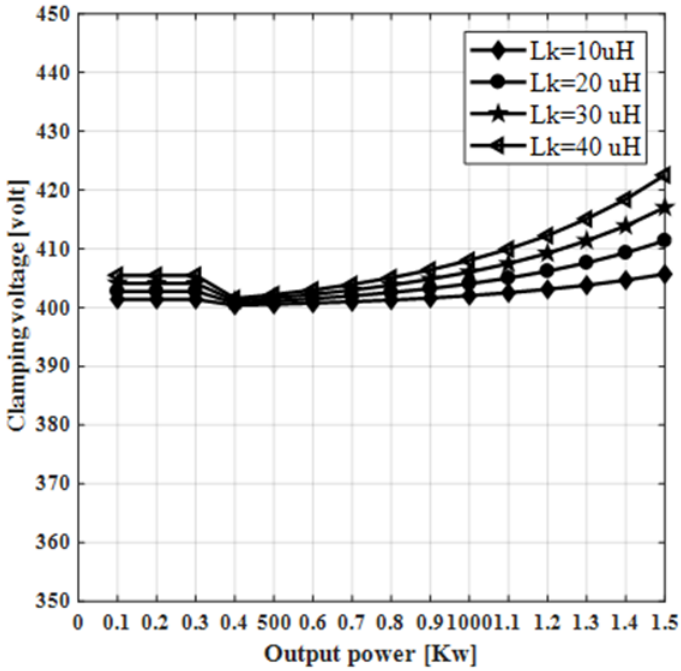


Figure 4.7: Effect of leakage inductor on clamping voltage (Vin=90 Vrms, n=0.5, V_o=200V, f_s=50KHz, L_{in}=100µH)

The converter is designed according to the following specifications: input voltage V_{in} = 90-265 V_{rms}, output voltage V_o = 200 V_{dc}, output power P_o = 1.5 kW, and switching frequency f_s = 50 kHz. The targeted efficiency in this example is assumed to be at least 93% based on previous iterations, similar to what was described in Section 2.4.

In this section of the thesis, several key considerations will take in account when designing the proposed converter. It should be noted that the design procedure is iterative and only the last iteration is shown here.

4.5.1 Main transformer turns ratio, n

The main key parameter to design the converter is the turns ratio of the main transformer, $n=(N_2/N_1)$ because it affects the amount of reflected load current that is available at the transformer primary to discharge the clamp capacitor. Figure 4.4 shows an example of the effect on the transformer turns ration on the clamping voltage. If the turns ration is low, less reflected load current will be available to discharge the clamping capacitor. This can result an extremely high voltage across the clamping capacitor. On the other hand, more turns ratio means more reflected output current and less clamping voltage; however more circulating current and more conduction losses will be created. It is clear that, a trade off between low and high values of n; therefore, selecting the value of n must be considered. However, selecting n cannot be achieved by a simple equation; a computer program that described in previews section is used to examine the value of n for different values of L_{in} and L_k that allow the converter to work under discontinuous current mod and under two most extreme line and load conditions: high line voltage, light load, and low line voltage, full load.

For this particular design example, several graphs of characteristic curves are generated for different values of n and based on these graphs, a value of n=0.5 is selected as appropriate value.

From Figure 4.5, it is clear that the value of the clamping voltage is 400 V at minimum input voltage V_{in}=90 V_{rms} input voltage. By increasing the input voltage for the same

value of turns ratio n, the clamping voltage will be increased to be less than 440 V at maximum input voltage V_{in}=265 V_{rm}.

4.5.2 Determine the Value of Duty Cycle

The proposed converter can operate with three distinct ranges of duty: Range 1 [0 < D < 0.33], Range 2 [0.33 < D < 0.66], and Range 3 [0.66 < D < 1]. Each one differs from other by the number of switches on at the same time.

The maximum of the duty cycle is determined by (4.4). The maximum duty cycle is 0.68 by considered minimum input voltage is V_{in}=90 V_{rms} to achieve a clamping voltage 400 V.

4.5.3 Maximum Input Inductor Value

The input inductor should be small enough to ensure that the current through each input inductor is fully discontinuous under all operating conditions, but not too small to avoid an excessively high peak current.

The value of each input inductor is determined by consider that the average input power is equal to the output power and this can be done using a computer program with the following equations.

The average input power during half line cycle is expressed as

$$P_{in} = \frac{1}{f_{sn}} \sum_{k=0}^{f_{sn}-1} \left|v_{in,k}\right|.(3 * I_{Lin1,k}) \tag{4.10}$$

where, $f_{sn}=f_s/(2*f_{in})$, f_s is the switching frequency, f_{in} is the line frequency, $|v_{in,k}|$ is the rectified AC supply voltage during switching cycle interval k, $I_{in,k}$ is the average current through one of the input inductors during switching cycle interval k.

$I_{Lin1,k}$ during switching cycle interval k is expressed as

$$I_{Lin1,k} = \frac{1}{T_s}\int_0^{T_s} i_{in,k}(t)dt \tag{4.11}$$

$$I_{Lin1,k} = \frac{1}{T_s}\left[\int_0^{DT_s} \frac{|v_{in,k}|}{L_{in}} t\, dt + \int_{DT_s}^{(\Delta_{s,k}+D)T_s} \left(I_{L_1 pk} - \frac{V_{C_c} - |v_{in,k}|}{L_{in}} t\right) dt\right] \tag{4.12}$$

Thus,

$$I_{L_{in1},k} = \frac{D^2}{2f_s L_{in}}\left[\left(\frac{|v_{in,k}|}{1 - \frac{|v_{in,k}|}{v_{Cc}}}\right)\right] \tag{4.13}$$

By substituting 4.13 into 4.10, the input power is expressed as

$$P_{in} = \frac{3D^2}{2f_s L_{in}} \cdot \frac{1}{f_{sn}} \sum_{k=0}^{f_{sn}-1} \left[\left(\frac{|v_{in,k}|^2}{1 - \frac{|v_{in,k}|}{v_{Cc}}}\right)\right] \tag{4.14}$$

where,

$$|v_{in,k}| = v_{in,rms}\sqrt{2}\left|sin(\frac{2\pi k}{f_{sn}})\right| \tag{4.15}$$

By assuming that P_{in} =P_o, the following equation can be derived to determine the value of the input inductor for each phase:

$$L_{in} = \frac{3D^2}{2f_s P_o} \cdot \frac{1}{f_{sn}} \sum_{k=0}^{f_{sn}-1} \left[\left(\frac{\left|v_{in,k}\right|^2}{1 - \frac{\left|v_{in,k}\right|}{v_{Cc}}} \right) \right] \tag{4.16}$$

The worst case to be considered in this design example when the converter operates with minimum input voltage and maximum load. By using v_{in}=90 V_{rms}, Po=1500w, V_{cc}=400V and D=D_{max}=0.68, the input inductor value for each phase L_{in} at the boundry condition is determine using computer program as 103 μH. L_{in}=100 μH is used.

4.5.4 Clamp Capacitor (C_c)

The value of clamping capacitor C_c is chosen such that one-half cycle of the resonant period between the clamping capacitor C_c and the leakage inductance L_{Lk} should eceed the maximum turn-off time of the main switches. This value is obtained as following:

$$(1 - D_{min})T_s > \pi \sqrt{L_{keq} C_c} \tag{4.17}$$

$$C_c > \frac{(1 - D_{min})^2}{\pi^2 L_{keq}} T_s^2 \tag{4.18}$$

where, C_c is the clamping capacitor, D_{min} is the minimum duty cycle, and L_{keq} is the equivalent leakage inductance that will interact with the clamping capacitor.

4.5.5 ZVS Turn on Range

An important consideration in the design of the converter is that all its switches should be able to turn on with ZVS over as wide a load range as possible. ZVS for the clamping switches S_{c1}-S_{c3} can be achieved for the whole load range because there will always be sufficient current flowing through their body diodes and this current is independent of any load considerations. On the other hand, the main switches, S_1-S_3, may not operate with ZVS under light-load conditions as there will not be sufficient current to discharge their output capacitances.

It is necessary to derive the timing between the turn-off of one of the clamping switches S_{c1}-S_{c3} and the turn-on of one of the main switches S_1-S_3 as the voltage across the parasitic output capacitor for any of the main switches must reach its minimum before it will be turned on. At the beginning of Mode 3, and before the clamping diode of the main switch is conducting, the output capacitor across the main switch (S_3 in this case) starts to discharge until it becomes zero. The time needed for Mode 3 to ensure ZVS operation should be determined so that it is not longer than a quarter of the resonant period between the leakage inductance of the transformer and the parasitic capacitors of the switches and it can be expressed as

$$t_3 - t_2 > \frac{\pi}{2}\sqrt{C_t L_{keq}} \tag{4.19}$$

where, C_t: parasitic capacitor across the main switches S_1-S_3.

L_k: the equivalent leakage inductance of the main transformer

4.6 Experimental Results

An experimental prototype was built to confirm the feasibility of the proposed converters. The specifications were: Input voltage V_{in}= 110 V_{rms}, output voltage V_{out}= 200 V, maximum power P_o= 1.5 kW and frequency f_{sw}=50 kHz. The parameters values were L_1=

$L_2 = L_3 = 100$ µH and a transformer turns ratio of n = (1/2). 6R190P6 devices were used for the switches and U1560 devices were used for the diodes. Figure 4.8 shows experimental results for the case when $V_{in} = 110\ V_{rms}$.

Input AC voltage and current waveforms are shown in Figure 4.8 (a). The input current is sinusoidal and in phase with the input voltage. Figure 4.8 (b) shows two input boost inductor currents I_{L1} and I_{L2}, which are discontinuous, and phase shifted 120˚. Voltage and current waveforms for one of the main switches are shown Figure 4.8 (c). The switch voltage is clamped to the voltage across the clamping capacitor, V_{Cc}, when it is turned off and the switch has a ZVS turn-on. The voltages across two of the three-phase transformer primary windings are shown in Figure 4.8. It can be seen that the primary voltage waveforms are square with zero voltage intervals and they are shifted 120˚ with respect to each other.

The quality of input current in the proposed converter is verified by compared its harmonics with the EN 61000-3-2 standard in Figure 4.9 for $120V_{ac}$ and $240V_{ac}$. It can be seen that the converter's harmonics are below the harmonic levels that are specified by the EN 61000-3-2 standard.

Another important factor that is useful to show the quality of the input current is power factor (PF). The converter power factor is shown in Figure 4.10 for the entire load at $120V_{ac}$ input. It can be seen that the power factor is greater then 0.99 at full-load operation. At light-load conditions, the power factor becomes slightly worse because harmonic currents become more dominant as the fundamental AC input current component is reduced.

Figure 4.11 shows the efficiency curve for the proposed converter with different output power. It can be seen that the maximum power of the converter is 94% from half to full load of operation. The efficiency is reduced significantly when the load is reduced then

half load (40% of the full load and less) that is because there is not enough current to achieve ZVS at light-load operation so that more switching losses are present.

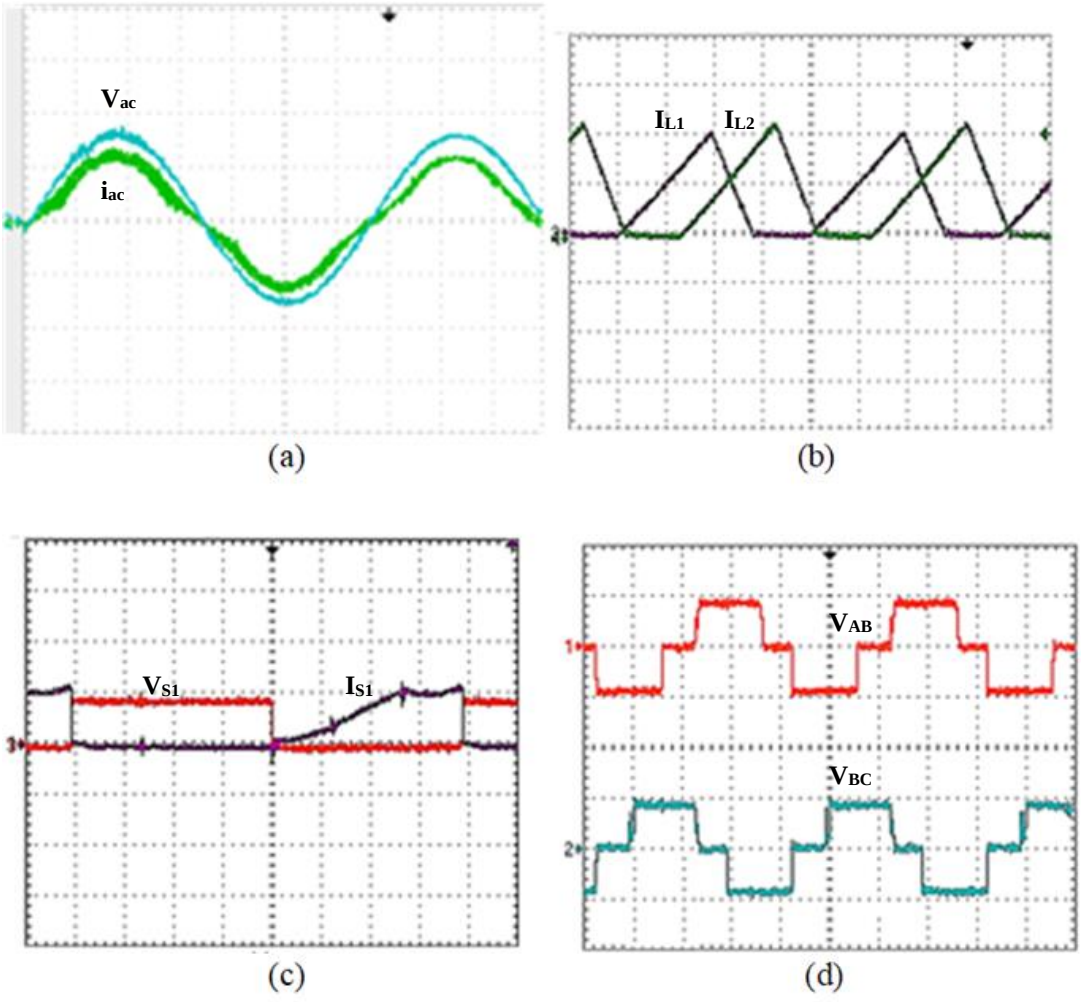


Figure 4.8: Typical converter's waveforms: (a) input ac voltage and current (V:100V/div, I:20A/div, t:5ms/div), (b) current through two of boost inductors (I:10A/div, t:5us/div), (c) the voltage across one of the main switch and the current through it (V:500V/div, I:20A/div, t:5us/div), (d) primary voltage waveform across two phases of the transformer (V:500V/div., t:5µs /div)

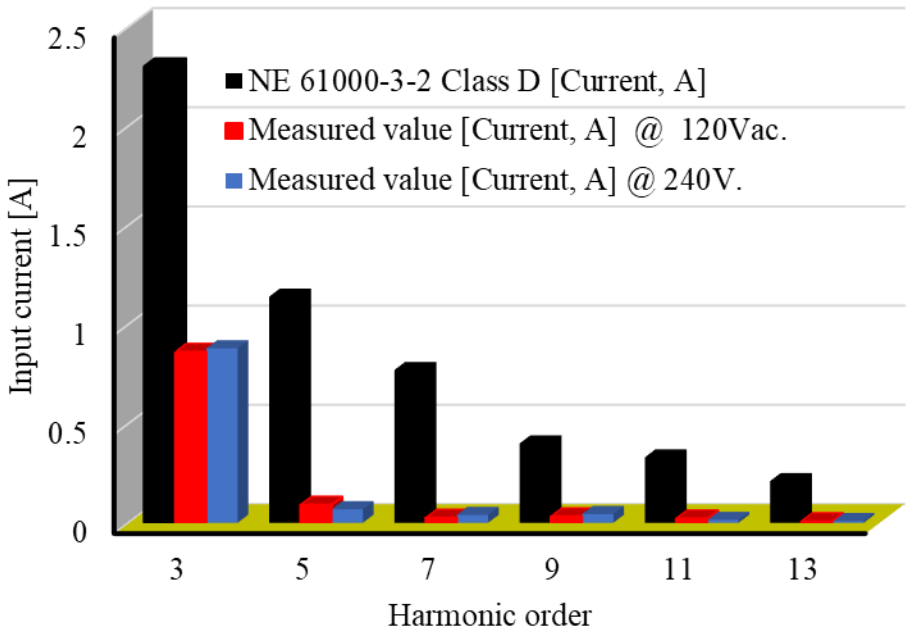


Figure 4.9: Input current harmonics at V_{in} =120 V_{rms} and V_{in}=240V_{rms} compared with EN61000-3-2 standard at full load operation

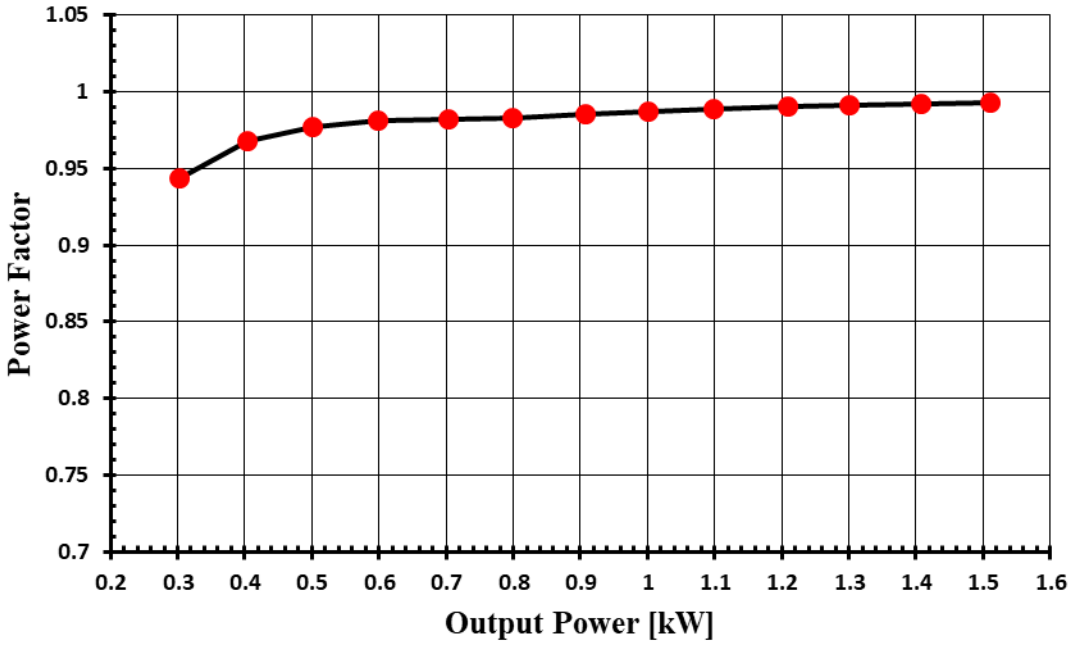


Figure 4.10: PFC of the proposed converter

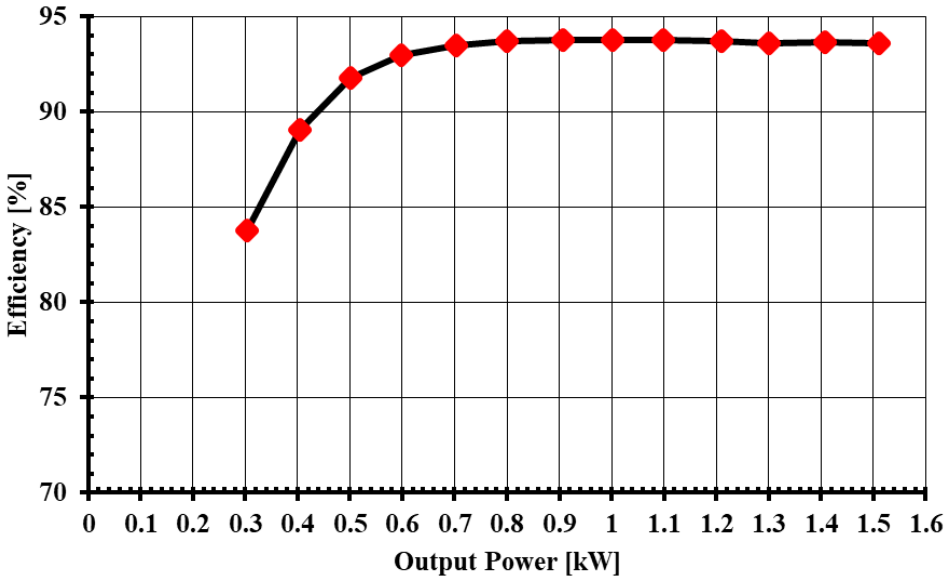


Figure 4.11: Efficiency of the proposed converter

4.7 Conclusion

A new interleaved AC-DC single-stage converter is proposed in this chapter. The proposed converter can do single-stage AC-DC power conversion with just three main power switches and three active clamp switches. All these switches can operate with ZVS and voltage spikes that would otherwise appear due to the interaction of transformer leakage inductance and switch output capacitance are easily clamped due to the presence of clamping capacitor C_c. The input current is continuous as the converter's input section consists of three interleaved boost modules. The operation of the converter is simple as it can be operated like an interleaved boost converter. No sophisticated or non-standard methods of control are required.

The converter's general operation and its modes of operation were explained in this chapter. Its steady-state characteristics were analyzed and used to develop a design procedure. Results obtained from an experimental prototype that confirmed the feasibility of the proposed converter were presented in the chapter.

Chapter 5

5 A Novel High-Gain Three-Phase DC-DC PWM Boost Converter

A new high-gain three-phase DC-DC boost converter that can be used in applications where a high output DC bus voltage must be produced from a low DC source voltage is proposed in this chapter. The proposed converter has high voltage gain, low input current ripple, and inherent switch voltage clamping. In the chapter, the operation of the converter is explained in detail, its features are discussed and guidelines for its design are given. Experimental results obtained from a converter prototype are presented to confirm the converter's feasibility.

5.1 Converter Operation and Analysis

The proposed converter is shown in Figure 5.1. It consists of three main switches, S_1–S_3, a three-phase transformer, whose primary and secondary are both connected in delta configuration, a three-phase diode bridge rectifier at the transformer secondary and an output capacitive filter C_1. The main switches of the converter are connected to the output through diodes D_{a1}, D_{a2}, and D_{a3} and these diodes are connected to the high side voltage through capacitor C_2.

The converter works as follows: Whenever a switch is turned on, the current in the inductor connected to its drain rises. Whenever a switch is turned off, its drain voltage is clamped to the voltage across C_2 as the inductor current flows to the output through D_{a1}, D_{a2} or D_{a3} and falls. Energy is transferred to C_1 while the converter is operating, whenever a primary voltage appears across one of the transformer primary windings. For example, this can happen when switch S_2 is on and switch S_1 is off with the current in L_1 flowing in D_{a1}. In this case, the voltage across the AB primary winding is V_{C2}. If the gating signals of the three main switches are such that they are the same but shifted 120^o with respect to each other, then ripple reduction will occur due to interleaving.

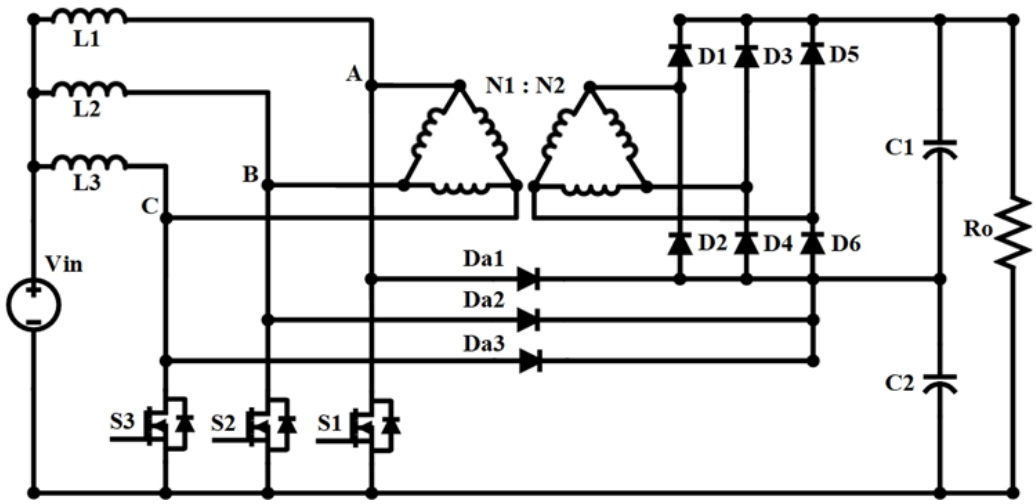


Figure 5.1: Proposed high-gain three-phase DC-DC PWM boost converter.

The modes of operation during a third of a steady-state switching cycle are explained in this section. Typical converter waveforms and circuit diagrams for each mode are shown in Figure 5.2 and Figure 5.3 respectively. For these diagrams, all converter components are ideal and it is assumed that the input inductors (L_1, L_2 and L_3) are large enough to keep the current through them continuous over a switching period. It is assumed that switch S_1 was on before $t = t_0$ and that it is conducting the full input current before the start of Mode 1 of operation.

Mode 1 [$t_0 < t < t_1$]: Switch S_2 is turned on at the beginning of this mode. The current through S_2 is gradually increased due the leakage inductance of the primary of the transformer. The current through switch S_2 increases, whereas the current through switch S_1 decreases. In this mode, Switches S_1 and S_2 are turned on, whereas switch S_3 is turned off. Energy is transferred through the three-phase transformer through the windings that have voltage impressed across them. Secondary current flows through diodes D_2, D_4 and D_5.

During this mode the current through switches S_1-S_3 can be obtained as following:

$$I_{s1} = I_1 + I_A \tag{5.1}$$

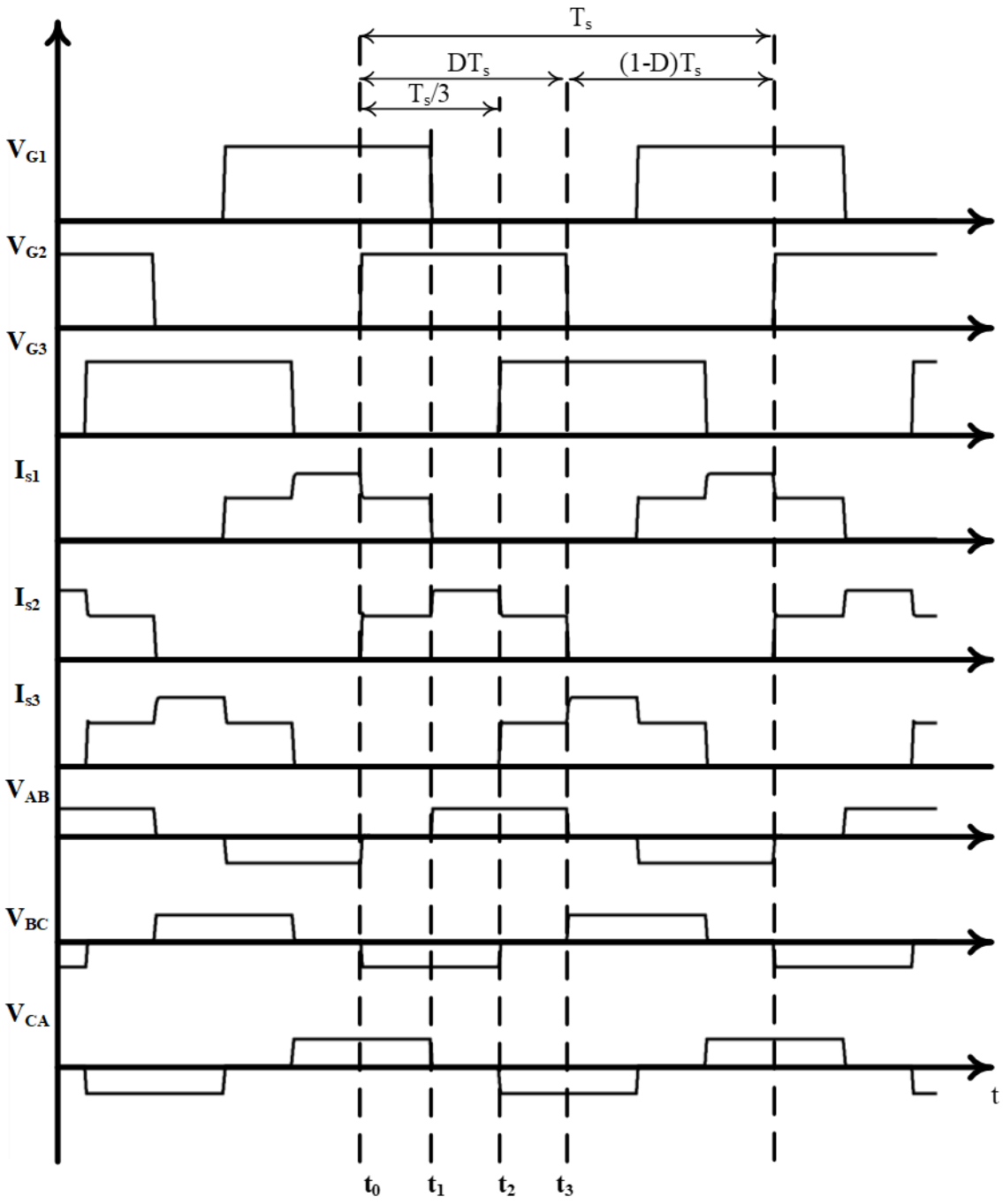
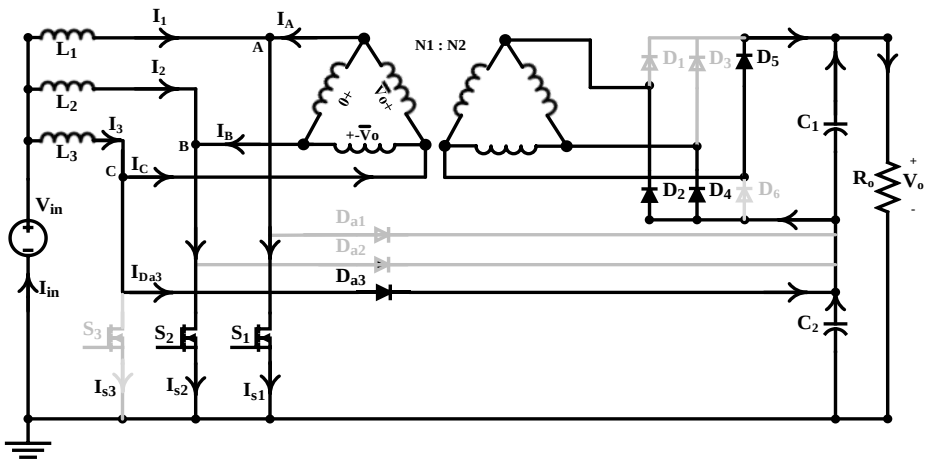
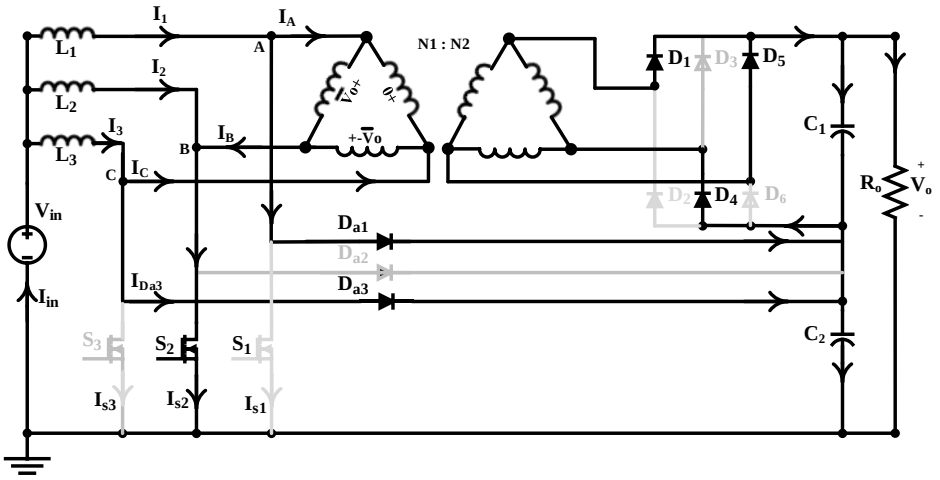


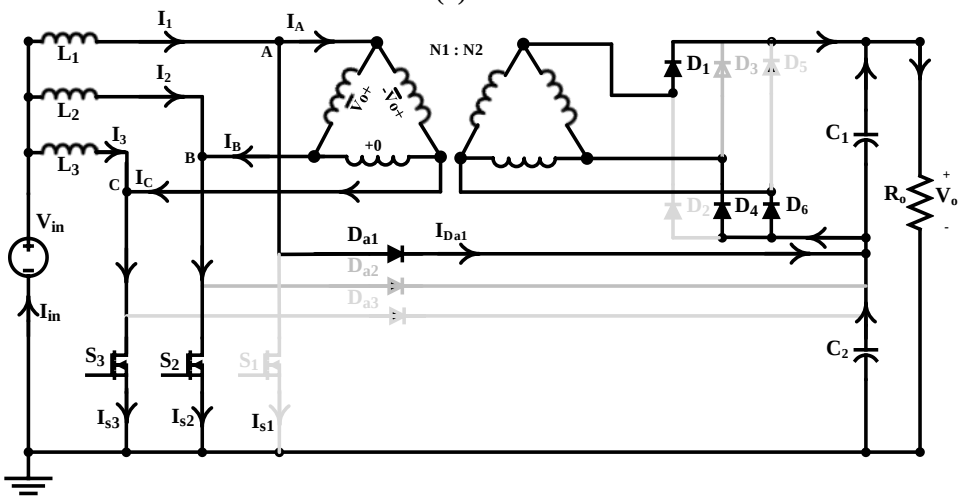
Figure 5.2: Typical converter waveforms



(a) Mode 1



(b) Mode 2



(c) Mode 3

Figure 5.3: Converter modes of operation

$$I_{s2} = I_2 + I_B \tag{5.2}$$

$$I_{s3} = I_3 - I_C - I_{Da3} = 0 \tag{5.3}$$

where, I_1, I_2 and I_3 are the currents of the input inductors L_1, L_2, and L_3 respectively,

I_A, I_B, and I_C are the currents of phase A, B, and C respectively, and

I_{Da3} is the current through the auxiliary diode D_{a3} and it is equal to the half of the current through input inductor L_3, i.e. $I_{Da3}=I_3/2$.

Since, L_1, L_2, and L_3 have same values, they will share the input current equally, i.e. $I_1=I_2=I_3=I_{in}/3$.

The voltage across phases A and B, V_{AB}, is zero as shown in Figure 5.3(a) because both of switches S_1 and S_2 is turned on and that results currents I_A and I_B will be same and circulating. Thus, the current that goes through S_1 is the same current that will goes through S_2, i.e. $I_{s1}=I_{s2}$.

By taking summation of (5.1), (5.2) and (5.3), the following equation will be yield

$$I_{s1} + I_{s2} + I_{s3} = I_1 + I_2 + I_3 + I_A + I_B - I_C - I_{Da3} \tag{5.4}$$

where, $I_{s1}=I_{s2}$, $I_{s3}=0$, $I_1=I_2=I_3=I_{in}/3$, $I_{Da3}=I_3/2=I_{in}/6$,

and $I_A+I_B=I_C$ because of the balancing of three phase transformer.

Thus, the currents through S_1 -S_3 are obtained by (5.5)

$$I_{s1} = I_{s2} = \frac{5I_{in}}{12} \; and \; I_{s3} = 0 \tag{5.5}$$

Mode 2 [$t_1 < t < t_2$]: At the beginning of this mode, Switch S_1 is turned off and the diodes D_{a1} and D_{a3} start to conduct; current flows to output through them. During this mode, energy is transferred to the output through the three-phase transformer as well as through the diodes D_{a1} and D_{a3}. In the secondary of the transformer D_1 starts to conduct whereas D_2 starts to disconnect. In this mode, the voltage across capacitor C_2 reaches to the level of the voltage across the transformer's primary and this voltage is applied across switch S_1.

During this mode the current through switches S_1-S_3 can be obtained as following:

$$I_{s1} = 0 = I_1 - I_{A-}I_{Da1} \tag{5.6}$$

$$I_{s2} = I_2 + I_B \tag{5.7}$$

$$I_{s3} = I_3 - I_C - I_{Da3} = 0 \tag{5.8}$$

where, I_{Da1} is the current through the auxiliary diode D_{a1} and it is equal to the half of the current through input inductor L_1, i.e. $I_{Da1}=I_1/2=I_{in}/6$, and

I_{Da3} is the current through the auxiliary diode D_{a3} and it is equal to the half of the current through input inductor L_3, i.e. $I_{Da3}=I_3/2=I_{in}/6$.

The voltage across phases C and A, V_{CA}, is zero as shown in Figure 5.3(b) because both of switches S_1 and S_3 is turned off and that results currents I_A and I_C will be same.

By taking summation of (5.6), (5.7) and (5.8), the following equation will be yield

$$I_{s1} + I_{s2} + I_{s3} = I_1 + I_2 + I_3 - I_A + I_B - I_C - I_{Da1} - I_{Da3} \quad (5.9)$$

where, $I_{s1}=I_{s3}=0$, $I_1=I_2=I_3=I_{in}/3$, $I_{Da1}=I_{in}/6$, $I_{Da2}=I_{in}/6$, and $I_A+I_C=I_B$ because of the balancing of three phase transformer.

Thus, the currents through S_1 -S_3 are obtained by (5.10)

$$I_{s1} = I_{s3} = 0 \; and \; I_{s2} = \frac{2}{3} I_{in} \quad (5.10)$$

Mode 3 [$t_2 < t < t_3$]: At the beginning of this mode, switch S_3 is turned on and the next one-third switching cycle begins. The converter operates in the same manner as in Mode1 except that switches S_2 and S_3 are turned on instead of switches S_1 and S_2. In this mode, energy is transferred to the output through three-phase transformer and diodes D_1, D_4 and D_6.

During this mode the current through switches S_1-S_3 can be obtained as following by using same analysis in mode 1:

$$I_{s2} = I_{s3} = \frac{5I_{in}}{12} \; and \; I_{s1} = 0 \quad (5.11)$$

5.2 Converter Features

The features of the proposed converter are discussed in detail in this section. The converter has the following features:

5.2.1 Current ripple reduction

As discussed in the Introduction, conventional single-phase high gain DC-DC converters have issues with current ripple and a bulky input inductor is needed to reduce it. Moreover, the same holds true for the output if the converter is operated with heavy loads. Current ripple is not an issue with the proposed converter as it is a three-phase DC-DC converter. It has an interleaved three-phase input, which reduces input current ripple. It also has reduced output current ripple as it is three times the switching frequency and thus easier to filter. This allows two smaller capacitors to be used instead of one big output capacitor.

5.2.2 High output gain

The proposed converter can be made to operate with high voltage gain because it has two separate mechanisms by which voltage can be stepped up. The first mechanism is the three-phase transformer section, the second is the non-isolated boost converter section. Each section can step up voltage by itself. In the case of the three-phase transformer, it is just a matter of adjusting the turns ratio of the transformer. In the case of the boost converter, it is just a matter of increasing the converter duty cycle.

A net increase in gain can be achieved by stacking the output of the two sections one on top of the other. This is different than many other high gain converters, which have only one mechanism for increasing gain and only one output.

5.2.3 Single-stage power processing

Many high gain converters use multiple cascaded cells to increase their gain. These cells can be based on additional active converters or passive voltage multiplier cells.

> Cascaded high gain converters use multiple converters to increase gain. In these converters, the output of one converter is fed to the input of another converter so that gain is increased. Sometimes, redundant elements in these converters can be removed to reduced cost. So-called quadratic converters, which are converters whose gain depends on the square of the duty cycle rather than the duty cycle itself, are just such converters.

Although the use of cascaded converters and quadratic converters has been established in the literature, these converters are rarely used except in low power applications. This is mainly because current must flow through numerous circuit elements so that conduction losses become significant. Such converters therefore cannot be used in renewable energy applications because of the high current that converter components must conduct.

The same issue arises when the use of passive voltage multiplier cells is considered. Passive voltage multiplier cells take the voltage of one cell then feed it to the input of another cell, which then feeds another cell until the last cell. Many of these multiplier cells are based on capacitors that are stacked one on top of the other. This can work if the current through the cells is low and in fact it is common to use such cells at the secondary output of high gain converters where the output voltage is already high, and the output current is low to provide an additional increase in gain. If such cells are considered in renewable energy applications, then they should not be exposed to high current.

In the proposed converter, power is processed by only one converter: power is either process by the three-phase transformer section or by the non-isolated boost section. As a result, current flows through only one converter instead of multiple converters and thus significant increases in conduction losses are avoided.

5.2.4 Inherent snubber circuit

In many high gain converters, the presence of voltage spikes due to parasitic elements is a concern; this is especially true for coupled inductor high gain converters. In such converters, the use of coupled inductors means that the converter switches are not clamped to any voltage and any difference in the current of the coupled inductors will try to force its way through the switches when they are turned off. As a result, such converters cannot operate unless additional snubbers are needed.

These snubbers can either be passive snubbers or active snubbers. Passive snubbers tend to dissipate energy or involve the addition of numerous components. Active snubbers

involve the use of additional active switches thus increasing the cost and complexity of the converter.

The proposed converter has an inherent snubber circuit and thus does not require that sophisticated clamping or dissipative passive snubber circuits be added to it. When a converter switch is turned off, the voltage across the switch is naturally clamped to the voltage across output capacitor C_2, which is a bulk capacitor.

5.2.5 Reduced peak switch voltage stress

Due to the high gain of high voltage gain converters, the switches of some previously proposed converters are exposed to high peak voltage stresses. This is because the high output DC voltage appears directly across the switch. High gain converters where the switches are not directly exposed to the output voltage have numerous circuit elements between them and the output. This, however, results in increased conduction losses as current must flow through these series elements.

In the proposed converter, peak switch voltage stress is not excessive. It is in fact less than the output voltage as the maximum voltage that appears across any converter switch is the voltage across C_2. This allows lower voltage rated semiconductor devices with lower values of on-state resistance R_{DSon} to be used as the converter switches.

5.3 Design Considerations

Several key considerations should be taken into account when designing the proposed converter. Some of these considerations are discussed in this section.

5.3.1 Input-output voltage gain

The proposed converter can be divided into two stages with the output voltage being the sum of the voltage across each stage. The first stage works as a three-phase interleaved boost converter with three-phase high frequency transformer. Assuming that the transformer leakage inductance is negligible, and the converter operates under continuous conduction mode (CCM).

The voltage gain of the first section can be described by the following equation

$$\frac{V_{C1}}{V_{in}} = \frac{n}{1-D} \tag{5.12}$$

where, V_{C1} is the voltage across C_1, V_{in} is the input voltage, n is the transformer turns ratio $n = \frac{N_2}{N_1}$, and D is the converter duty cycle.

The second stage (auxiliary circuit) works as a conventional interleaved boost converter. the output to input ratio in this section can be expressed as

$$\frac{V_{C2}}{V_{in}} = \frac{1}{1-D} \tag{5.13}$$

where V_{C2} is the voltage across C_2

The overall voltage gain, G, of the proposed converter can be derived as following

$$G = \frac{V_o}{V_{in}} = \frac{n+1}{1-D} \tag{5.14}$$

From (5.14), the overall voltage gain depends on the transformer's turns ratio and the duty ratio of the converter. The gain of the proposed converter increases whether the transformer's turns ration or the duty cycle is increased as shown in Figure 5.4. There is, however, a trade-off between the turns ratio and the duty cycle. Although smaller duty cycle means lower voltage stress across the switches, it results in higher turns ratio, which increases the amount of current circulating in the primary circulation current, thus increasing conduction losses.

5.3.2 Transformer turns ratio, n

The transformer's turns ratio should be chosen to minimize the voltage stress across the converter semiconductors devices. The voltage stress across the main switches is the voltage across the output capacitor, V_{C2}. It should be noted that V_{C2} can be calculated using (5.13) or it can be also approximated to be the voltage across the primary transformer ($V_{C2} = V_{pri} = \frac{V_{in}}{1-D}$). Thus, the output voltage across C_1 is calculated as

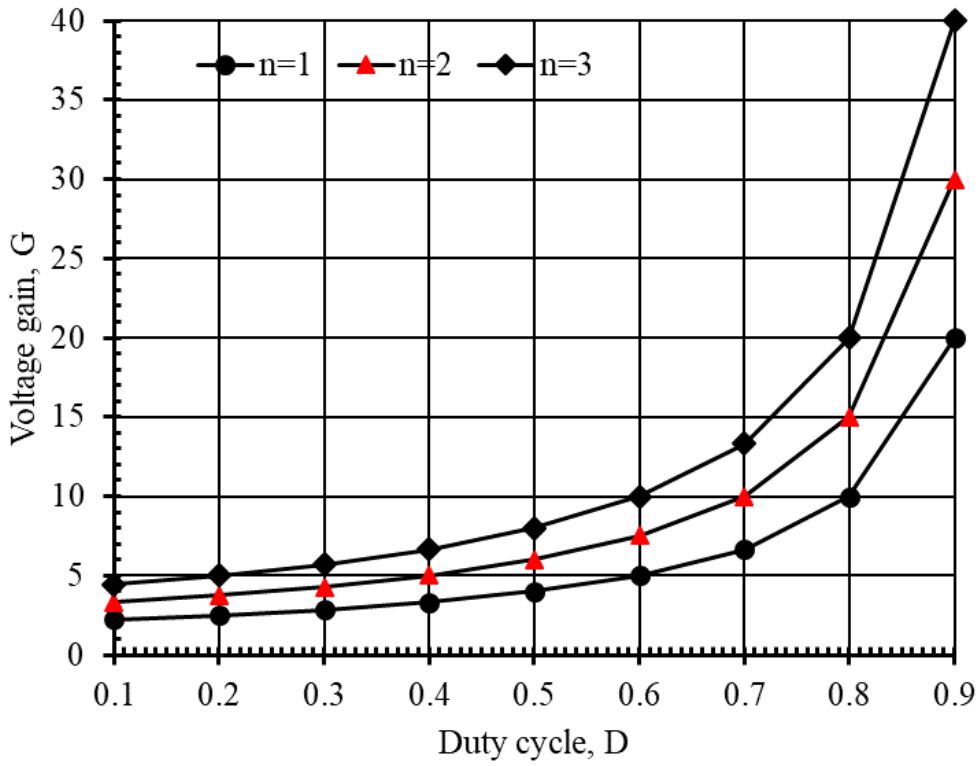


Figure 5.4: Voltage gain according to duty cycle with different values of transformer turns ratio, n under CCM

$V_{C1} = nV_{C2}$. For constant duty cycle D, increasing the turns ratio will result in more voltage appearing across capacitor C_1 while the voltage across the primary does not change (i.e. the voltage stress across the switches does not increase). Higher voltage stress across the output bridge diodes, however, will appear.

The transformer's turns ratio also has a significant effect on the distribution of the output voltages (V_{C1}:V_{C2}). This ratio can be determined by using (5.12) and (5.13), (i.e. the ratio V_{C1}/V_{C2}=n). Figure 5.5 shows the impact of transformer turns ratio on the output voltage destitution of the converter. It can be seen that higher turns ratio means more voltage across capacitor C_1 and more energy transferred to the output through the transformer, but more energy results in more losses and higher rating for the transformer. On the other hand, lower turns ratio means higher voltage across C_2 and more components stresses. The turns ratio of the transformer therefore should be chosen as a compromise between the transformer size and the stress of the converter components.

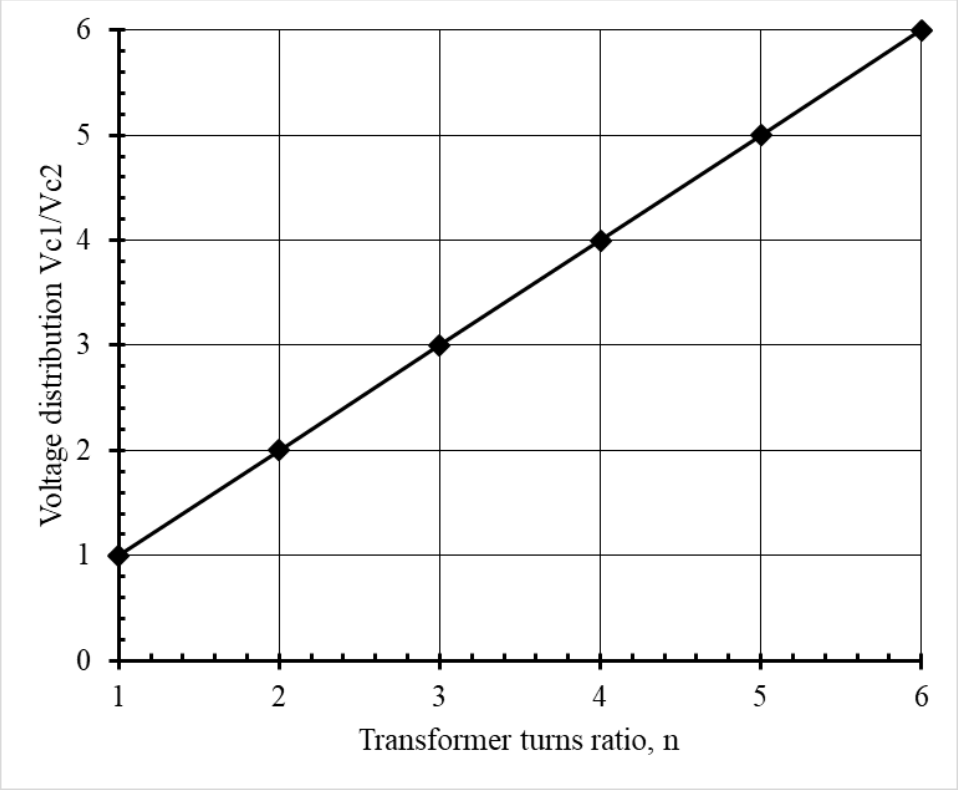


Figure 5.5: output voltages distribution according to the variation of transformer turns ratio, n

5.4 Design Procedure and Example of the Proposed Converter

The proposed converter has two three-phase DC-DC converters stages, the first stage is a three-phase interleaved boost converter with three-phase high frequency transformer and the second stage is conventional interleaved boost converter. Both of the converters are connected to the same input source through three interleaved boost inductors. The design of the proposed converter is discussed in this section and demonstrated with an example of the selection of certain key parameters. It should be noted that the design procedures of both converter sections are iterative as the parameters in each section are interrelated and dependent on one another. It will generally take several iterations before a satisfactory design can be achieved and this process may need to be continued in the design of a final experimental prototype. The example shown in this section can be considered to be the final iteration of a design process.

The converter is designed according to the following specifications: input voltage 18V-30V, output voltage V_o= 200 V, output power P_o= 500 W and switching frequency f_{sw}=50 kHz. The targeted efficiency in this example is assumed to be at least 90% based on previous iterations, similar to what was described in Section 2. 4.

5.4.1 Peak input current

The peak input current of the proposed converter can be calculated from the following equation

$$I_{in,pk} = I_{in,avg} + \frac{\Delta i_{in}}{2} \tag{5.15}$$

where, Δi_{in} is the ripple of the input current and $I_{in,avg}$ is the average input current.

The input average current can be calculated as

$$I_{in,avg} = \frac{P_o}{\eta V_{in,min}} \tag{5.16}$$

where P_o is the output power, $V_{in,min}$ is the minimum input voltage, and η is the converter's efficiency.

By using Δi_{in}=0.5A, P_o=500W, $V_{in,min}$=18V and the efficiency is 90% is assumed, by substituting in to (5.15) and (5.16) therefore, the peak input current $I_{in,pk}$=31.11A.

5.4.2 Input-output voltage gain

It is assumed that the converter operates in continuous conduction mode (CCM) and the maximum input-output voltage gain of the proposed converter in this design example can be calculated by using (5.14) as following:

$$G = \frac{V_o}{V_{in,min}} = \frac{200}{18} = 11.11 \tag{5.17}$$

5.4.3 Determine the value of the duty cycle, D and transformer turns ratio, n

It is assumed that the converter operates in CCM with a duty cycle 0.33< D <0.66 because the input current ripple and output voltage ripple are reduced significantly in this region as shown in [77], [78]. Thus, the maximum value of the duty cycle is D_{max}=0.66. It should be noted that the maximum duty cycle happens when the input voltage is minimum (i.e. $V_{in,min}$=18V).

Since the voltage gain was previously determined in section 5.4.2 to be 11.11, the turns ratio can be calculated according to (5.14), which has been plotted in Figure 5.4 for CCM operation. Thus, the turns ratio is n=2.77. In addition, the minimum duty cycle can be calculated at maximum input voltage $V_{in,max}$=30V by using (5.14) and it becomes D_{min}=0.43.

In this design example, the proposed converter is operated in range 2 [0.33 < D < 0.66]. by using n=3, V_{in}=18V and the output voltage gain G=11.11, which results D_{max}=0.64 and D_{min}=0.4 according to (5.14) and Figure 5.4.

5.4.4 Determine the value of input boost inductor

Since the proposed converter is a three-phase interleaved boost converter, the input current ripple at CCM is the sum of each conductor current, and the input inductor can be calculated as

$$L = \frac{V_{in,min}}{\Delta i_{in} f_s}\left(\frac{2-3D_{max}}{1-D_{max}}\right)(D_{max} - \frac{1}{3}) \qquad (5.18)$$

where, $L=L_1=L_2=L_3$ is the input inductor for each phase, f_s is the switching frequency, D_{max} is the maximum duty cycle, $V_{in,max}$ is the maximum input voltage and Δi_{in} is the input current ripple. Equation (5.18) has been derived based on the work on [78] for 0.33<D<0.66.

In this design example, $V_{in,min}$=18V, D_{max}=0.6, f_s=50kHz, Δi_{in}=0.5A, this results the input inductor value for each phase is L= 160µH. In this example L_1=200µH.

5.4.5 Voltage stress across switches S_1-S_3

The voltage tress of the main switches S_1-S_3 is the voltage across capacitor C_2. This voltage is calculated using (5.19)

$$V_s = V_{C2} = \frac{V_{in}}{1 - D} \tag{5.19}$$

where, V_s is the voltage stress across one of the main switches, $V_s=V_{s1}=V_{s2}=V_{s3}$, V_{in} is the input voltage and D is the duty cycle. Figure 5.6 shows the impact of duty cycle for different values of input voltages. It is can be seen that more duty cycle results more voltage stress across the switches. On the other hands, less duty cycle means less voltage stress, however less gain will results as shown in Figure 5.4 in Section 5.3.1.

Since the duty cycle of the proposed converter has been chosen to be between 0.33 and 0.66 (i.e. 0.33<D<0.66), the maximum stress will be 88.23V as shown in Figure 5.6.

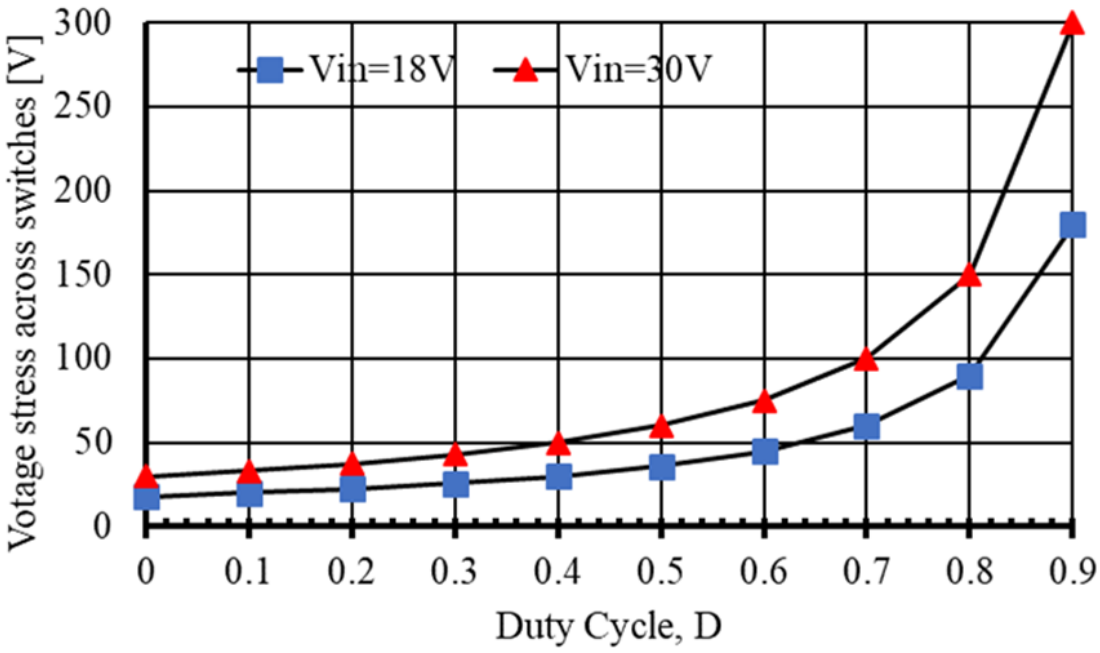


Figure 5.6: Switches voltage stress with duty cycle, D, for different values of input voltage, V_{in}

5.4.6 Current stress on switches S_1-S_3

Since the converter operates in Range II (0.33<D<0.66), the peak current in any of the main switches will happen when just one switch is turned on. For example, the current through S_2 in mode 2 (see Figure 5.3(b)) using (5.10). Using $I_{in,pk}$= 31.11 A, which calculated from Section 5.4.1, The peak switch current therefore is

$$I_{S_{pk}} = \frac{2}{3} I_{in,pk} = 20.74A$$

The average current through each main switch when the converter is operating at full-load can be determined as

$$I_{s_{avg}} = \frac{1}{T_s}\int_0^T i_s(t)dt = \frac{1}{T_s}\left[\int_{t_0}^{t_1} \frac{5}{12} I_{in}.\,dt + \int_{t_1}^{t_2} \frac{2}{3} I_{in}.\,dt + \int_{t_2}^{t_3} \frac{5}{12} I_{in}.\,dt\right]$$

$$\begin{aligned} I_{s_{avg}} &= \frac{1}{T_s}\left[\frac{5}{12} I_{in}(t_1 - t_0) + \frac{2}{3} I_{in}(t_2 - t_1) + \frac{5}{12} I_{in}(t_3 - t_2)\right. \\ &\left. = \left(\frac{I_{in}}{6}\right)(1 + D)\right] \end{aligned} \tag{5.20}$$

where, (t_1-t_0), (t_2-t_1) and (t_3-t_2) are the time duration of modes 1, 2, and 3 respectively. These durations are calculated as follows:

$$(t_1 - t_0) = (t_3 - t_2) = \left(D - \frac{1}{3}\right) T_s \; and \; (t_2 - t_1) = \left(\frac{2}{3} - D\right) T_s \tag{5.21}$$

By substituting (5.21) in to (5.20), the average current for each switch can be calculated by (5.22).

$$I_{s_{avg}} = \left(\frac{I_{in}}{6}\right)(1 + D) \tag{5.22}$$

Using the maximum input current value determined previously $I_{s,pk}$=20.74 A and duty cycle D=0.6, the average current through one of the main switches is $I_{s_{avg}} = 5.53$ A.

5.5 Experimental Results

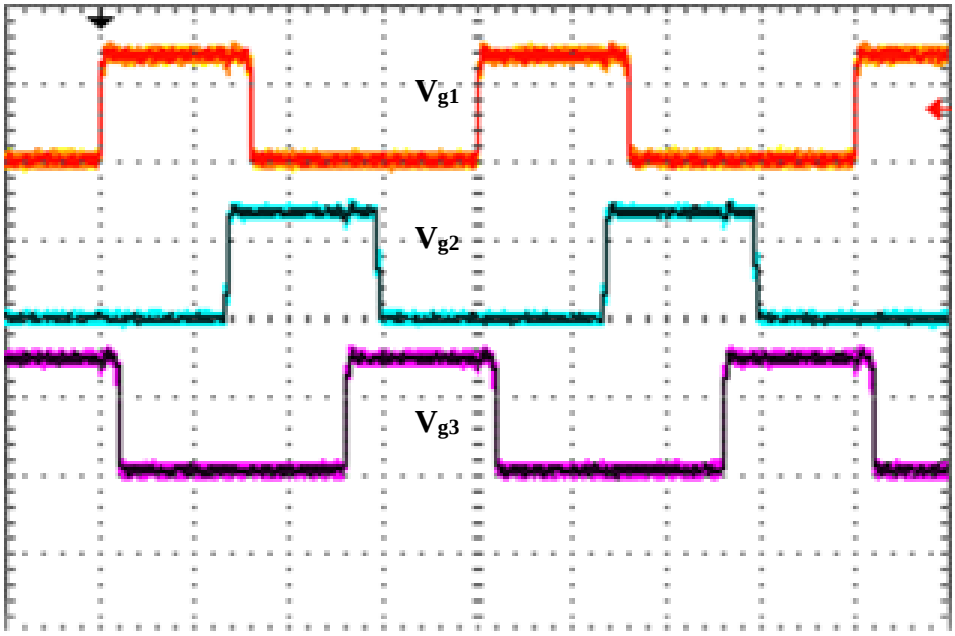
A prototype of the proposed converter was built according to the following specifications: Input voltage V_{in}= 18V-30V, output voltage V_o= 200 V, output power P_o= 500 W and switching frequency f_{sw}=50 kHz. The prototype was implemented with L_1= L_2 = L_3 = 200 µH and a transformer turns ratio of n = 3. IRFB 4227 devices were used for the switches and ETL 0806 devices were used for the diodes. Typical experimental waveforms obtained with V_{in} = 30 V are shown in Figure 5.7.

Figure 5.7(a) shows gating signals of the converter's main switches, which are identical but shifted by 120˚ with respect to each other. Voltage and current waveforms for one of the main switches are shown in Figure 5.7(b). It can be seen that the switch voltage is clamped and that it is clamped to a voltage that is less than the output voltage.

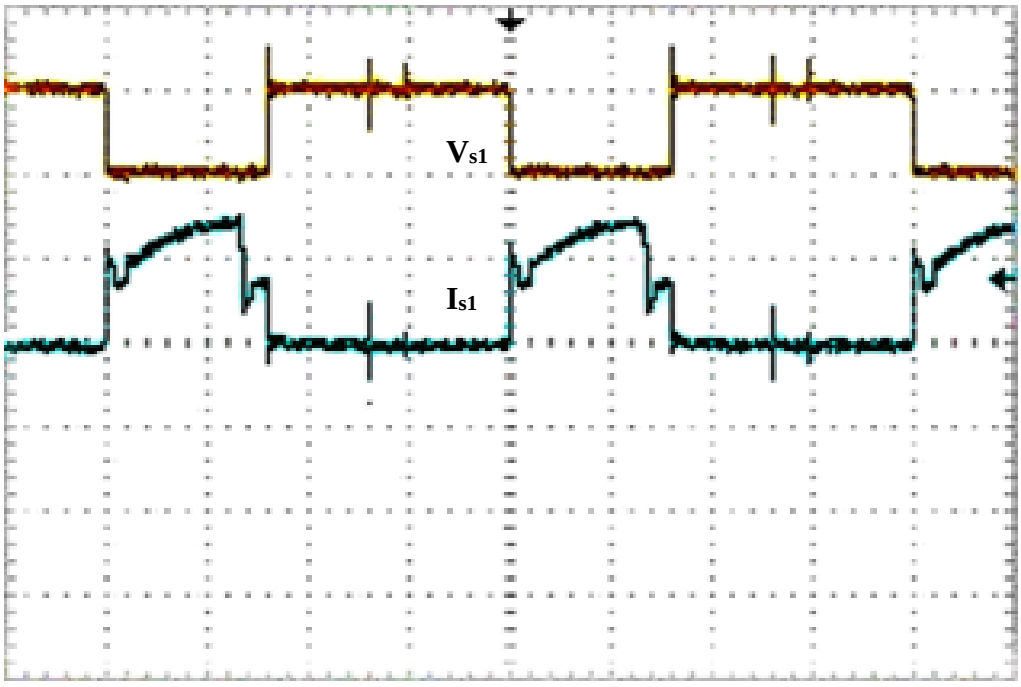
Figure 5.7(c) shows gating signals for two main switches and a voltage across one of the three-phase transformer primaries. The primary voltage waveform is a square waveform with some zero voltage intervals and that it is not symmetrical. The symmetry or asymmetry of the voltage is dependent on the switch states of the switches.

Figure 5.7(d) shows the currents for two of the boost inductors I_{L1} and I_{L2} and Figure 5.7(e) shows the current of one of the boost inductors and the input current I_{in} flowing out of the DC source. The inductor currents have some ripple and the input current has little due to interleaving.

Figure 5.8 shows the efficiency of the proposed converter. It can be seen that the maximum efficiency of the proposed converter achieved under half load condition (≈94%). When the converter is operating under full load condition, more conduction losses will result, and the efficiency becomes 90%.



(a)



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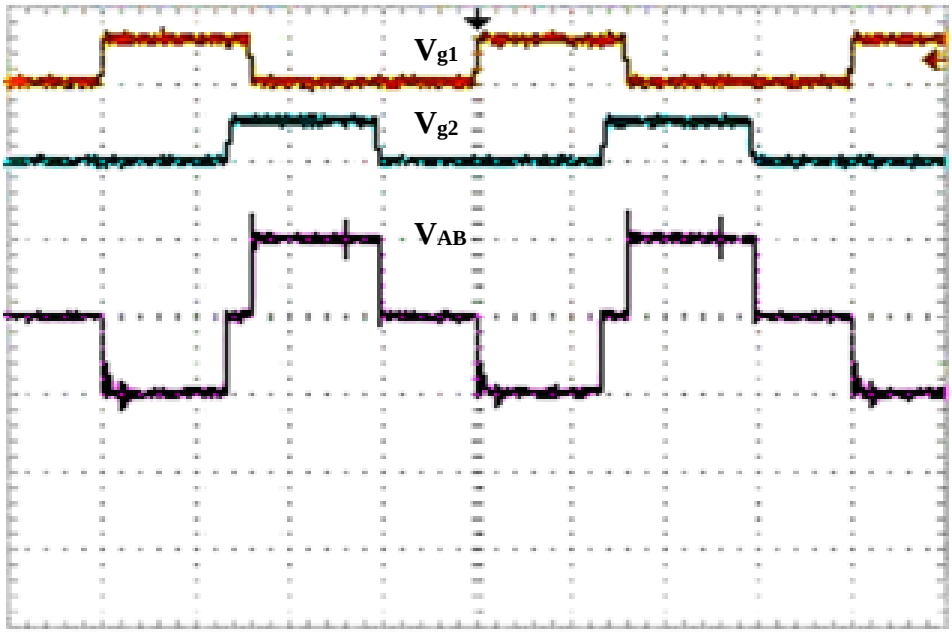

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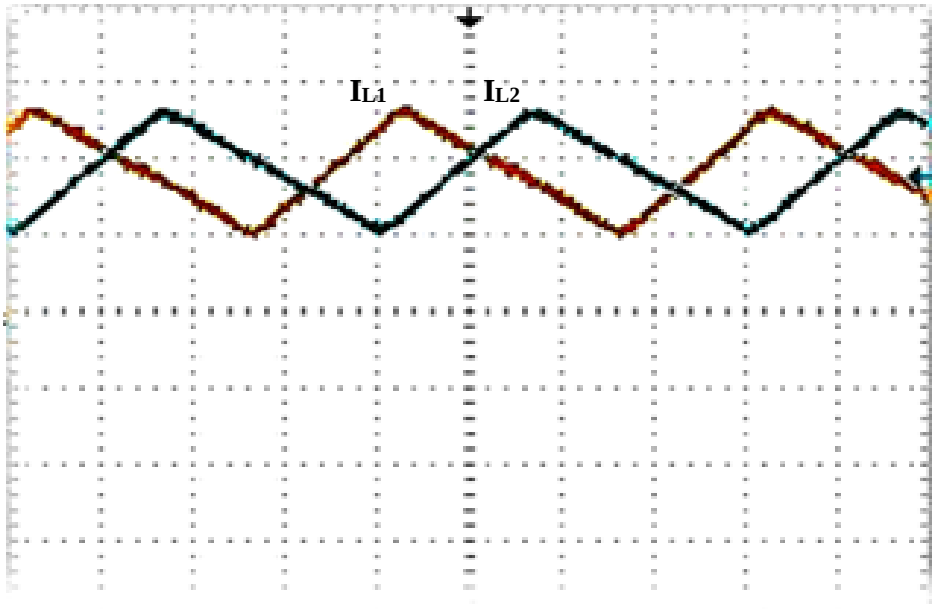
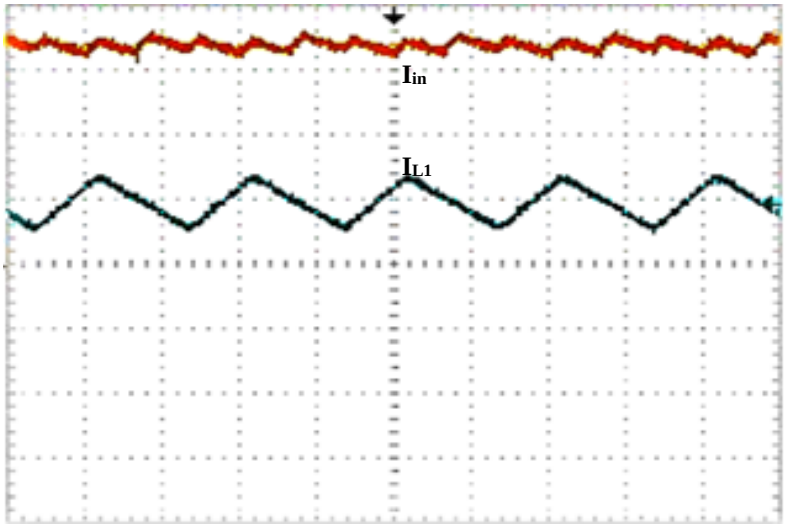


(d)



(e)

Figure 5.7: Experimental results: (a) Gating signal waveforms (V:20V/div., t:5µs/div.), (b) Voltage and current for the main switch (V: 50V/div., I: 5A/div., t: 5µs/div), (c) Gating signal waveforms for two main switches and primary voltage waveform across the transformer (Vg: 50V/div., Vt: 50V/div., t: 5µs/div, (d) Current through two main inductors (I: 1A/div, t: 5µs/div.), (e) Input current and main inductor current waveform (I_{in}: 2A/div., I_L: 2A/div, t: 10µs/div.)

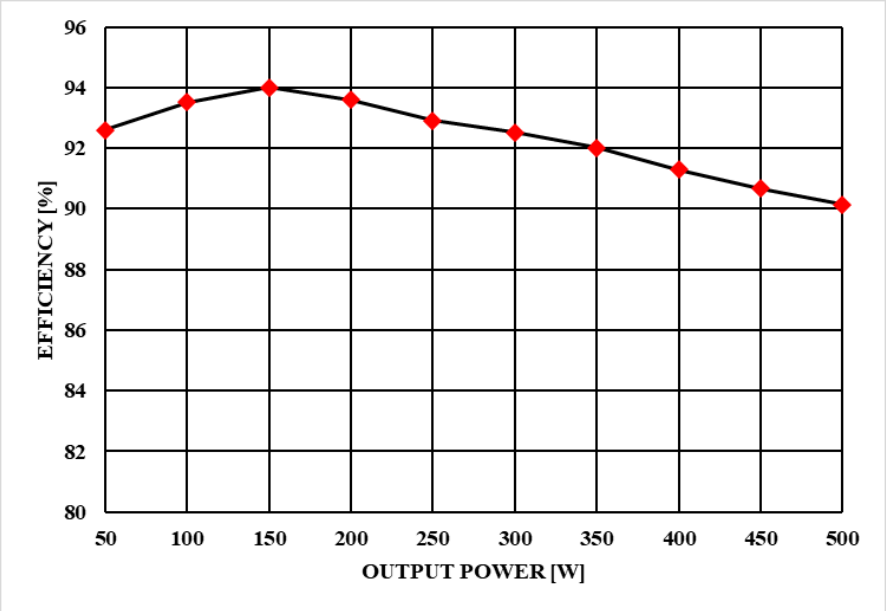


Figure 5.8: Efficiency curve of the proposed converter

5.6 Conclusion

A new high-gain three-phase DC-DC converter is proposed in this chapter. It has an input current with low ripple, high gain due to a stacking structure), lower conduction losses due to fewer components in the path of current and the fact that power is only processed once (either by the boost converter or the three-phase transformer), a simple and inherent clamping mechanism (no additional clamping snubbers need to be added to the circuit), and lower voltage and/or current stresses on the components (i.e. the peak voltage stress is clamped to V_{C2} and not V_o).

In this chapter, the operation of the converter was explained in detail, its features were discussed and some guidelines for its design were given. The converter's feasibility was confirmed with results obtained from an experimental prototype.

Chapter 6

6 Summary and Conclusion

6.1 Summary

The focus of this thesis has been on power converters that are based on three-phase DC-DC converters that have a three-phase transformer in their topology. The typical conversion process of these DC-DC converters is to convert an input DC source voltage into three-phase high-frequency AC voltage, feed this three-phase AC voltage to a three-phase transformer, which steps the voltage up or down, then rectify this voltage and filter the result so that a desired three-phase DC output voltage can be obtained.

Three-phase DC-DC converters are attractive because they have several advantageous features over conventional DC-DC converter that have a single-phase transformer in their topologies. These include lower cost for higher power applications as one converter can be used instead of three lower power converters in parallel, less input current ripple in some three-phase DC-DC topologies than that found in conventional DC-DC converters due to inherent interleaving, less output current ripple that is lower and at higher frequency than that produced by conventional DC-DC converters, and less current stresses on converter components as current is split among three phases. Three-phase DC-DC converters are thus attractive for higher power applications.

Other applications where three-phase DC-DC converters are attractive are renewable energy applications such as solar power conversion and fuel-cell power converters. Renewable energy sources such as solar cells and fuel cells tend to produce low output DC voltages. The current coming out of these sources can be considerable even for power conversion applications of a few hundred watts because their voltages are low and thus whatever converter is used to convert the low input DC voltage to a higher more practical DC voltage must be able to handle this high current. Since three-phase DC-DC converters are better than conventional DC-DC converters in this regard, therefore they are more suitable for certain renewable energy applications.

The contents of this thesis can be summarized as follows:

In Chapter 1, basic power electronic concepts that are related to the work performed for this thesis were explained and a literature review of relevant previous work was performed. The objectives of the thesis were stated and the outline of this thesis was presented.

In Chapter 2, a new three-phase DC-DC converter was presented. This converter requires fewer active switches than converters of the same type, has input current interleaving, inherent switch voltage clamping, and an auxiliary circuit that does not interfere with the operation of the main part of the circuit. In this chapter, the general operation of the converter was described as well as the most significant modes of operation that it goes through during a typical switching cycle. Equations for each mode of operation were derived and then used to establish a design procedure that can be used to select key converter components. The design procedure was demonstrated with an example and used to design an experimental converter prototype.

In Chapter 3, experimental results obtained from a prototype of the converter that was introduced in Chapter 2 were presented. Key experimental waveforms were shown as well as efficiency results. These efficiency results were compared to those obtained of a representative active-clamp type three-phase DC-DC converter operating with conventional silicon (Si) semiconductor devices. Further comparisons were made between experimental prototypes that were built with silicon-carbide (SiC) devices that are said to offer better performance than Si devices, but are less readily available and more expensive. Based on the experimental work presented in this chapters, conclusions related to the efficiency of the proposed converter vs that of the active-clamp converter and the efficiency of Si-based converters vs SiC based converters were made.

In Chapter 4, a new single-phase AC-DC converter with three-phase transformer isolation was introduced. The advantages of this converter are that it has an interleaved input current, it has lower component current stresses and less output ripple than AC-DC converters with single-phase transformer isolation. Moreover, it can be implemented with fewer active switches than conventional two-stage approaches that require an additional converter. In this chapter, the general operation of the converter was described and the most significant modes of operation that the converter goes through during a typical switching cycle were

explained. Equations for each mode of operation were derived and then used to establish a design procedure that can be used to select key converter components. The design procedure was demonstrated with an example and used to design an experimental converter prototype. Result obtained from an experimental prototype of the proposed AC-DC converter were shown and conclusions were presented.

In Chapter 5, a new three-phase DC-DC converter with high output voltage / input voltage gain was introduced. High gain converters have become popular in recent years due to their use in renewable energy source systems as they can take low-level DC voltages from solar panels or fuel cells and convert them to higher-level DC voltages that can be used to feed DC-AC inverters that can be connected to the grid. The proposed high gain converter has high output gain, only three active switches, reduced switch voltage stress, an interleaved input for low input current ripple, and inherent voltage snubbing of the switches. In this chapter, the general operation of the converter was described and the most significant modes of operation that the converter goes through during a typical switching cycle were explained. Equations for each mode of operation were derived and then used to establish a design procedure that can be used to select key converter components. The design procedure was demonstrated with an example and used to design an experimental converter prototype. Results obtained from an experimental prototype of the proposed high-gain DC-DC converter were shown and conclusions were presented.

In this chapter, the contents of the thesis are summarized, the main conclusion and contributions of the thesis are stated, and suggestions for future work are presented.

6.2 Conclusions

The following conclusions can be made based on the work that has been done for this thesis:

- It is possible to perform three-phase DC-DC conversion with just four active switches. This results in the elimination of at least 2-3 active switches and their associated gate drive circuits that previously proposed converters have in their topologies, thus reducing cost.

- The efficiency of the proposed three-phase four-switch DC-DC converter is almost the same as that of the more sophisticated and more expensive three-phase active clamp converter for a load range of up to 1.5kW.
- The prototypes that were implemented with silicon carbide (SiC) devices were only slightly more efficient than those implemented with conventional silicon (Si) devices. This was because the prototypes were operated with low input voltages and high input currents so that conductions losses were the most dominant losses; these were unaffected by the type of switching device that was used. Switching losses, which are affected by the type of device used, were not as significant as conduction losses. The fact that prototypes with SiC devices were only slightly more efficient than those Si devices is significant because it is generally assumed by power electronics that replacing Si devices with SiC devices will automatically improve converter efficiency significantly. While this may be the case for many converters, it is not the case for the DC-DC converters that were examined in this thesis.
- The difference in efficiency between the two converters narrowed when SiC devices were used. This was because SiC devices impact switching losses. There was little change in the efficiency of the active clamp converter because the converter switches already operate with ZVS except for light loads so switching losses are already eliminated. In the case of the proposed three-phase four-switch DC-DC converter, SiC devices can help reduce switching losses as the switches in these converters do not operate with ZVS and thus the gap in efficiency between the two converters can be narrowed.
- The AC-DC converter proposed in this thesis is actually a single-stage converter with a DC clamp capacitor that has a voltage across it that is determined by the converter's parameters and operating conditions. As it is a single-stage converter that can perform AC-DC power conversion with just one converter instead of two, it shares some of the characteristics of such converters. One such characteristic is that the voltage across the clamp capacitor is independent of load if the input inductor currents are discontinuous and the current in the magnetizing inductances of the three-phase transformer are discontinuous. This characteristic is significant

along with the interleaved converter input as the input current can be made continuous and the clamp capacitor voltage can avoid being excessive, which is something that cannot be achieved with a standard boost-type single-stage converter.

- The proposed high-gain DC-DC high-gain converter has an inherent snubber circuit, which results in the voltage across the switches being naturally clamped to the voltage across output capacitor $C_{2.}$ This means the voltage rating of the active switches does not depend on output voltage and is therefore lower than that found in other high-gain converters.

6.3 Contributions

The contributions to the power electronics literature of the work done for this thesis are as follows:

- A new three-phase DC-DC converter that uses just four active switches was proposed in this thesis. This converter uses fewer active devices than other previously proposed three-phase DC-DC converters that typically require six or seven active switches. Moreover, the proposed converter has input current interleaving that can reduce input current ripple, which makes it suitable for renewable energy applications where it is desired that such ripple is low.
- A comparative study between a three-phase DC-DC converter with Si devices and one with SiC devices was made. This comparison showed that SiC devices may result in only marginal efficiency improvement over Si devices for some converter topologies. This result is unexpected as it has been commonly accepted by the power electronics community that converters with SiC devices have much greater efficiencies than those with Si devices.
- A new AC-DC single-stage converter that has three-module phase interleaving and transformer isolation was proposed. Such a converter uses fewer active devices than the conventional two-stage approach, which may require as many as nine active switches.
- A new three-phase DC-DC converter with high output voltage gain was proposed. This converter can produce a high output voltage from a low input DC voltage,

which makes it especially suitable for renewable energy application just as though for solar energy systems where the DC voltage obtained from solar panels is low. The proposed converter has just three active switches, reduced switch voltage stress, and inherent voltage snubbing to prevent switch overvoltage spikes from appearing across the switches.

- A full analysis of the key steady-state characteristics of all the new converters that have been presented in this thesis was made and a design procedure for the selection of the most significant components of each converter was developed and presented. This will help other engineers implement the converters proposed in this thesis.

6.4 Suggested and Future Work

The following suggestions for future work are made in this section:

- An investigation of how the three-phase DC-DC converters have been proposed in this thesis can be implemented in renewable energy systems can be made. The objective in this case would be to examine how these converters would work as part of a system as opposed to working independently.
- The three-phase DC-DC converter proposed in Chapter 2 has an auxiliary circuit that does not interfere with the operation of the main circuit, unlike many previously proposed converters of the same type. As a result, it can operate with higher switching frequencies. Future work can involve an investigation of how the proposed converter operates with SiC devices at high switching frequencies.

References

[1] A. Averberg and A. Mertens, “Analysis of a voltage-fed full bridge DC-DC converter in fuel cell systems,” in *IEEE PESC*, 2007, pp. 286–292.

[2] V. Vaisanen, T. Riipinen, and P. Silventounen, “Effects of switching asymmetry on an isolated full-Bbridge boost converter,” *IEEE Trans. power Electron.*, vol. 25, no. 8, pp. 2033–2044, 2010.

[3] V. Yakushev, V. Meleshin, and S. Fraidlin, “Full-bridge isolated current fed converter with active clamp,” in *IEEE APEC*, 1999, pp. 560–566.

[4] A. Mousavi, P. Das, G. Moschopoulos, and S. Member, “A Comparative study of a new ZCS DC – DC full-bridge boost converter with a ZVS active-clamp converter,” *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1347–1358, 2012.

[5] A. R. Prasad, P. D. Ziogas, and S. Manias, “Analysis and design of a three-phase Off-Line dc-dc converter with high-frequency isolation,” *IEEE Trans. Ind. Appl.*, vol. 28, no. 4, pp. 824–832, 1992.

[6] W. A. A. De Doncker and D. M. Divan, “A Three-phase soft-switched high-power-density dc/dc converter for high-power applications,” *IEEE Trans. Ind. Appl.*, vol. 27, no. 1, pp. 63–73, 1991.

[7] R. L. Zheng, “Analysis and design of a three-phase LCC-type resonant converter,” in *IEEE PESC*, 1998, vol. 34, no. 2.

[8] J. Jacobs, A. Averberg, and R. De Doncker, “A novel three-phase DC/DC converter for high-power applications,” in *IEEE APEC*, 2004, pp. 1861–1867.

[9] D. S. Oliveira and I. Barbi, “A three-phase ZVS PWM DC / DC converter with asymmetrical duty cycle associated with a three-phase version of the hybridge rectifier,” *IEEE Trans. power Electron.*, vol. 20, no. 2, pp. 354–360, 2005.

[10] T. H. Converter, C. Liu, A. Ridenour, J. J. Lai, and S. Member, “Modeling and control of a novel six-leg low voltage fuel cell applications,” *IEEE Trans. power Electron.*, vol. 21, no. 5, pp. 1292–1300, 2006.

[11] H. Kim, C. Yoon, and S. Choi, “A three-phase zero-voltage and zero-current applications,” *IEEE Trans. power Electron.*, vol. 25, no. 2, pp. 391–398, 2010.

[12] M. Almardy and A. K. S. Bhat, “A comparison of three-phase high- frequency transformer isolated LCC and LCL-type DC-DC resonant converter topologies,” in *IEEE ICPE-ECCE*, 2015, vol. 1, pp. 1513–1520.

[13] W. Y. Δ. C. Transformer, K. Jin, and C. Liu, “A novel PWM high voltage conversion ratio bidirectional three-phase DC/DC converter with Y-Δ connected transformer,” *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 81–88, 2016.

[14] S. V. G. Oliveira and I. Barbi, “A three-phase step-up DC-DC converter with a three-phase high frequency transformer,” in *IEEE ISIE*, 2005, vol. 2, pp. 571–576.

[15] H. Cha, J. Choi, and B. Han, “A new three-phase interleaved isolated boost converter with active clamp for fuel cells,” in *IEEE PESC*, 2008, pp. 1271–1276.

[16] H. Cha, J. Choi, and P. N. Enjeti, “A three-phase current-fed DC / DC converter energy sources,” *IEEE Trans. power Electron.*, vol. 23, no. 6, pp. 2784–2793, 2008.

[17] Y. Song *et al.*, “A current-fed three-phase half-bridge DC-DC converter with active clamping,” in *IEEE ECCE*, 2009, pp. 1362–1366.

[18] H. Cha, J. Choi, W. Kim, and V. Blasko, “A new Bi-directional three-phase interleaved isolated converter with active clamp,” in *IEEE APEC*, 2009, pp. 1766–1772.

[19] J. Choi, H. Cha, and B. Han, “A three-phase interleaved DC – DC converter with active clamp for fuel cells,” *IEEE Trans. Power Electron.*, vol. 25, no. 8, pp. 2115–2123, 2010.

[20] S. Vidal, G. Oliveira, and I. Barbi, “A three-phase step-up DC – DC converter with a three-phase high-frequency transformer for DC renewable power source applications,” *IEEE Trans. Ind. Electron.*, vol. 58, no. 8, pp. 3567–3580, 2011.

[21] S. Lee, J. Park, S. Choi, and S. Member, “A three-phase current-fed push – pull DC – DC converter with active clamp for fuel cell applications,” *IEEE Trans. Power Electron.*, vol. 26, no. 8, pp. 2266–2277, 2011.

[22] K. Modepalli, A. Mohammadpour, and T. Li, “Three-phase current-fed isolated DC – DC converter,” *IEEE Trans. Ind. Appl.*, vol. 53, no. 1, pp. 242–250, 2017.

[23] S. Manias, P. D. Ziogas, and G. Olivier, “An AC-to-DC converter with improved input power factor and high power density,” *IEEE Trans. Ind. Appl.*, vol. IA-22, no. 6, pp. 1073–1081, 1986.

[24] A. Fernadez, A. Ferreres, P. Villegas, J. Sebastian, and L. Alvarez, “Size comparison between a half bridge converter with an AICS and a two-stage boost converter operating in a narrow input voltage range,” in *IEEE PESC*, 2001, pp. 1793–1798.

[25] B. Singh, B. N. Singh, A. Chandra, K. Al-haddad, and A. Pandey, “A review of single-phase improved power quality AC – DC converters,” *IEEE Trans. Ind. Electron.*, vol. 50, no. 5, pp. 962–981, 2003.

[26] C. Shin-young, L. II-Oun, P. Jeong-eon, and M. Gun-woo, “Two-stage configuration for 60W universal-line AC-DC adapter,” in *IEEE IECON*, 2012, pp. 1445–1450.

[27] J. Park, J. Kim, B. Lee, and G. Moon, “Design on topologies for high efficiency two-Stage AC-DC converter,” in *IEEE ECCE*, 2012, vol. 1, pp. 257–262.

[28] Z. Guo, X. Ren, Y. Wu, L. Bai, Z. Zhang, and Q. Chen, “Optimum harmonics injection to minimize bus capacitance of CRM boost PFC conveters meeting EN61000-3-2 class D limits,” in *IEEE APEC*, 2018, pp. 2009–2014.

[29] T. Nussbaumer, K. Raggl, J. W. Kolar, and S. Member, “Design guidelines for interleaved single-phase boost PFC circuits,” *IEEE Trans. Ind. Electron.*, vol. 56, no. 7, pp. 2559–2573, 2009.

[30] M. Pahlevaninezhad, P. Das, J. Drobnik, G. Moschopoulos, P. K. Jain, and A. Bakhshai, “A nonlinear optimal control approach based on the control-lyapunov function for an AC / DC converter used in electric vehicles,” *IEEE Trans. Ind. Informatics*, vol. 8, no. 3, pp. 596–614, 2012.

[31] D. S. Gautam *et al.*, “An automotive onboard 3 . 3-kW battery charger for PHEV application,” *IEEE Trans. Veh. Technol.*, vol. 61, no. 8, pp. 3466–3474, 2012.

[32] J. Lee and H. Chae, “6 . 6-kW onboard charger design using DCM PFC converter with harmonic modulation technique and two-stage DC / DC converter,” *IEEE Trans. Ind. Electron.*, vol. 61, no. 3, pp. 1243–1252, 2014.

[33] A. K. Panda, P. R. Mohanty, T. Penthia, and N. Patnaik, “Dual output interleaved PFC for alleviating mutual interference between loads during transients,” in *IEEE UPCON*, 2016, pp. 289–294.

[34] J. Hu, W. Xiao, B. Zhang, and D. Qiu, “A single phase hybrid interleaved parallel boost PFC converter,” in *IEEE ECCE*, 2018, pp. 2855–2859.

[35] A. Tausif, H. Jung, and S. Choi, “Single-stage isolated electrolytic capacitor-less EV onboard charger with power decoupling,” *CPSS Trans. Power Electron. Appl.*, vol. 4, no. 1, pp. 30–39, 2019.

[36] R. Erickson, M. Madigan, and S. Singer, “Design of a simple high-power factor rectifier based on the flyback converter,” in *IEEE APEC*, 1990, pp. 792–801.

[37] M. J. Schutten, R. L. Steigenvald, and M. H. Kheraluwala, “Characteristics of load resonant converters operated in a high-power factor mode,” *IEEE Trans. POWER Electron.*, vol. 7, no. 2, 1992.

[38] P. K. Jain, J. R. Espinoza, and N. A. Ismail, “A Single-stage zero-voltage zero-current-switched extended load power range,” *IEEE Trans. Ind. Electron.*, vol. 46, no. 2, pp. 261–270, 1999.

[39] J. Zhang, F. C. Lee, and M. M. Jovanovit, “A novel interleaved discontinuous-current-mode single-stage power-factor- correction technique with universal-line input,” in *IEEE PESC*, 2001, pp. 1007–1012.

[40] A. K. S. Bhat and R. Venkatraman, “A soft-switched full-bridge single-stage AC-to-DC harmonic distortion,” *IEEE Trans. Ind. Electron.*, vol. 52, no. 4, pp. 1109–1116, 2005.

[41] U. Kamnarn and V. Chunkag, “Analysis and design of a modular Tthree-phase AC-to-DC converter using CUK rectifier module with nearly unity power factor and fast dynamic response,” *IEEE Trans. POWER Electron.*, vol. 24, no. 8, pp. 2000–2012, 2009.

[42] P. Das, S. Li, and G. Moschopoulos, “An improved AC – DC single-stage full-bridge converter with reduced DC bus voltage,” *IEEE Trans. Ind. Electron.*, vol. 56, no. 12, pp. 4882–4893, 2009.

[43] J. Zhang, D. D. Lu, and T. Sun, “Flyback-based single-stage power-factor-correction scheme with time-multiplexing control,” *IEEE Trans. Ind. Electron.*, vol. 57, no. 3, pp. 1041–1049, 2010.

[44] H. Ma, Y. Ji, and Y. Xu, “Design and analysis of single-stage power factor correction converter with a feedback winding,” *IEEE Trans. POWER Electron.*, vol. 25, no. 6, pp. 1460–1470, 2010.

[45] H. S. Ribeiro and B. V. Borges, “New optimized full-bridge single-stage ac / dc converters,” *IEEE Trans. Ind. Electron.*, vol. 58, no. 6, pp. 2397–2409, 2011.

[46] H. Cheng, Y. Hsieh, and C. Lin, “A novel single-stage high-power-factor AC/DC converter featuring high circuit efficiency,” *IEEE Trans. Ind. Electron.*, vol. 58, no. 2, pp. 524–532, 2011.

[47] J. Kwon, W. Choi, and B. Kwon, “Single-stage quasi-resonant flyback converter for a cost-effective PDP sustain power module,” *IEEE Trans. Ind. Electron.*, vol. 58, no. 6, pp. 2372–2377, 2011.

[48] S. Moon, G. Koo, and G. Moon, “A new control method of interleaved single-stage flyback AC – DC converter for outdoor LED lighting systems,” *IEEE Trans. Power Electron.*, vol. 28, no. 8, pp. 4051–4062, 2013.

[49] K. Mandal, S. Banerjee, and C. Chakraborty, “Symmetry-breaking bifurcation in series-parallel load resonant dc-dc converters,” *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 60, no. 3, pp. 778–787, 2013.

[50] M. Narimani and G. Moschopoulos, “A new single-phase single-stage three-level power-factor-correction AC – DC converter with phase-shift modulation,” *IEEE Trans. Ind. Electron.*, vol. 60, no. 9, pp. 3731–3735, 2013.

[51] M. Narimani, S. Member, G. Moschopoulos, and S. Member, “A three-level integrated AC – DC converter,” *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1813–1820, 2014.

[52] R. Saasaa, W. Eberle, and M. Agamy, “A single-stage interleaved LLC PFC converter,” in *IEEE ECCE*, 2016, pp. 1–6.

[53] I. Castro, K. Martin, A. Vazquez, M. Arias, D. G. Lamar, and J. Sebastian, “An AC – DC PFC single-stage dual inductor lighting applications,” *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 6, no. 1, pp. 255–266, 2018.

[54] C. Tseng and C. Chen, “A passive lossless snubber cell for nonisolated PWM DC/DC converters,” *IEEE Trans. Ind. Electron.*, vol. 45, no. 4, pp. 593–601, 1998.

[55] V. Yakushev, V. Meleshin, and S. Fraidlin, “Full-bridge isolated current fed converter with active clamp,” in *IEEE APEC*, 1999, pp. 560–566.

[56] T. Kim, H. Kim, and H. Ahn, “An improved ZVT PWM boost converter,” in *IEEE PESC*, 2000, pp. 615–619.

[57] H. Bodur and A. F. Bakan, “A new ZVT-PWM DC – DC converter,” *IEEE Trans. Power Electron.*, vol. 17, no. 1, pp. 40–47, 2002.

[58] P. Applications and D. North, “A novel soft-commutating isolated boost full-bridge ZVS DC-DC converters for bi-direcional high power applications,” in *IEEE PESC*, 2004, pp. 2141–2146.

[59] A. Averberg, K. R. Meyer, and A. Mertens, “Current-fed full bridge converter for

fuel cell systems," in *IEEE PESC*, 2008, pp. 866–872.

[60] A. Mousavi, P. Das, G. Moschopoulos, and S. Member, "A comparative study of a new ZCS DC – DC full-bridge boost converter With a ZVS active-clamp converter," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1347–1358, 2012.

[61] B. Ak, "An improved ZVT – ZCT PWM DC – DC boost converter with increased efficiency," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1919–1926, 2014.

[62] C. Y. Inaba, Y. Konishi, M. Nakamura, and M. Nakaoka, "High frequency PWM boost chopper-fed DC-DC converters with coupled-inductors," in *IEEE CIEP*, 2002, pp. 134–138.

[63] W. Li, J. Liu, J. Wu, X. He, and S. Member, "Design and analysis of isolated ZVT boost converters for high-efficiency and high-step-up applications," *IEEE Trans. power Electron.*, vol. 22, no. 6, pp. 2363–2374, 2007.

[64] H. Do, "A soft-switching DC / DC converter with high," *IEEE Trans. Power Electron.*, vol. 25, no. 5, pp. 1193–1200, 2010.

[65] H. Do, "A zero-voltage-switching DC – DC converter with high voltage gain," *IEEE Trans. Power Electron.*, vol. 26, no. 5, pp. 1578–1586, 2011.

[66] M. Garg and R. K. Singh, "Coupled inductor boost converter with enhanced ESR filter capacitor for DC microgrid applications," in *ICIT*, pp. 963–968.

[67] G. Wu and X. Ruan, "Non-isolated high step-up converter adopting coupled inductor," in *IEEE IECON*, pp. 3506–3510.

[68] H. E. Mohamed and A. A. Fardoun, "High gain DC-DC converter for PV applications," in *IEEE MWSCAS*, pp. 1–4.

[69] V. Anand, K. Prabhala, P. Fajri, and ....., "A DC – DC converter with high voltage gain and two input boost stages," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 4206–4215, 2016.

[70] M. Muhammad, M. Armstrong, and M. A. Elgendy, "Analysis and implementation of high-gain non-isolated DC – DC boost converter," *IET Power Electron.*, vol. 10, no. 11, pp. 1241–1249, 2017.

[71] M. Eydi, S. H. Hosseini, and R. Ghazi, "A new high gain DC-DC boost converter with continuous input and output currents," in *IEEE PEDSTC*, pp. 224–229.

[72] S. Lee and H. Do, "Quadratic boost DC – DC converter with high voltage gain and reduced voltage stresses," *IEEE Trans. Power Electron.*, vol. 34, no. 3, pp. 2397–2404, 2019.

[73] C. Yoon, J. Kim, S. Choi, and S. Member, "Multiphase DC – DC converters using a boost-half-bridge cell for high-voltage and high-power applications," *IEEE Trans. Power Electron.*, vol. 26, no. 2, pp. 381–388, 2011.

[74] G. C. Silveira, F. L. Tofoli, L. Daniel, S. Bezerra, and R. P. Torrico-bascopé, "A nonisolated DC – DC boost converter with high voltage gain and balanced output voltage," *IEEE Trans. Ind. Electron.*, vol. 61, no. 12, pp. 6739–6746, 2014.

[75] K. Modepalli, R. Suryadevara, and L. Parsa, "High-frequency isolated DC-DC

converter for offshore wind energy systems," in *IEEE ECCE*, 2016, pp. 1–6.

[76] F. Liu, Y. Chen, X. Chen, and A. A. Tptl, "Comprehensive analysis of three-phase three-level LC -type resonant DC / DC converter with variable frequency control — series resonant converter," *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5122–5131, 2017.

[77] G. Choe, J. Kim, H. Kang, and B. Lee, "An optimal design methodology of an interleaved boost converter for fuel cell applications," *J. Electr. Eng. Technol.*, vol. 5, no. 2, 2010.

[78] G. Ram, C. Mouli, S. Member, and J. H. Schijffelen, "Design and comparison of a 10-kW interleaved boost converter for PV application using Si and SiC devices," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 5, no. 2, pp. 610–623, 2017.

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3. R. Rasoulinezhad, A. Abosnina and G. Moschopoulos, "An interleaved AC-DC ZCS-PWM boost rectifier," *INTELEC*, Oct. 2018, pp. 1-7.

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7. R. Rasoulinezhad, A. Abosnina and G. Moschopoulos, "A novel AC-DC interleaved ZCS-PWM boost converter," *IEEE APEC*, March 2018, pp. 716-722.

8. A. A. Abosnina and G. Moschopoulos, "A novel high-gain three-phase DC-DC PWM boost converter," *IEEE APEC*, March 2018, pp. 1533-1539.

9. A. A. Abosnina and G. Moschopoulos, "A novel three-phase bidirectional DC-DC converter for UPS applications," *IEEE APEC*, March 2018, pp. 1506-1513.

10. A. A. Abosnina and G. Moschopoulos, "A novel three-phase DC-DC PWM isolated boost converter," *IEEE INTELEC*, Oct. 2017, pp. 464-470.

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12. A. A. Abosnina and G. Moschopoulos, "Three-phase DC-DC PWM boost converter for renewable energy applications," *IEEE ECCE*, Oct. 2017, pp. 447-454.

13. A. Alganidi, A. Abosnina and G. Moschopoulos, "A novel high gain DC-DC full-bridge converter for low voltage renewable energy applications," *IEEE CCECE*, April 2017, pp. 1-4.