Universidad de Antioquia

Power Electronic Converters Design and Control Based on Non-linear Dynamical Models with Verified Controllability via Set Theory in Control

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A thesis submitted in fulfilment of the requirements
for the degree of Master of Engineering

in the

Grupo de Investigación en el Manejo Eficiente de la Energía (GIMEL)
Department of Electrical Engineering

December 2015

UNIVERSIDAD DE ANTIOQUIA

Abstract

Faculty of Engineering
Department of Electrical Engineering

Master of Engineering

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In this work a design procedure of Power Electronic Converters (PECs) is proposed, which is based on system knowledge and systems theory. The proposed design procedure is composed by 4 stages and 10 steps and allows to obtain all PEC parameters and its control structure such that established system operating requirements are satisfied. In this proposed design procedure, system controllability is tested based on set theory in control. The main achievement of this design procedure is to allow the PEC design taking into account its inherent dynamical nature and with verified controllability, but without fixing any control structure. The proposed design procedure is applied to a Boost DC-DC converter as illustrative example to show its applicability. Then, proposed procedure design is applied to a case of study: a Three-Leg Split-Capacitor Shunt Active Power Filter is successfully designed.

Keywords: Power Electronic Converters, Design Procedure, Dynamical Modeling, Set Theory in Control, Controllability, Controller Design, DC-DC converter, Voltage Source Inverter.

Acknowledgements

En primer lugar, quiero dar mis mas sinceros agradecimientos a mi tutor, Profesor Nicolás Muñoz, por permiterme trabajar con él, por poner a mi disposición todos los recursos que estuvieron a su alcance para llevar a cabo este trabajo, por su constante orientación y disposición.

Agredezco a todos mis compañeros del Grupo de Investigación en Manejo Eficiente de la Energía GIMEL por brindarme un espacio propicio de trabajo, en especial, quiero agradecer a Cristian, fueron muchos los espacios de conversación que tuvimos que me motivaron a seguir adelante, a Leo y a Daniel, sin su apoyo, disposición y dedicación tal vez esta tesis no hubiera encontrado su punto final. También quiero agradecer a los integrantes del Semillero de Electrónica de Potencia por el interés mostrado en mi trabajo y por los espacios compartidos, fueron de gran aprendizaje.

Agradezco infinitamente a la Profesora Lina Gómez, gran parte de mi formación como investigador la debo a ella. Le agradezco especialmente su amistad incondicional y su disposición infita para orientarme.

Agradezco infinitamente a mis padres, ellos me lo han dado todo, es de ellos cada uno de mis logros.

Agradezco infinitamente a mi Karen por su paciencia y amor, fue ella en la que siempre encontré un motivo para seguir adelante, fueron sus palabras y los momentos compartidos los que no me permitieron desfallecer.

Finalmente, quiero expresar mi gratitud con la Universidad de Antioquia, fue el apoyo económico a través de la beca de Estudiante Instructor lo que hizo posible llevar a cabo mis estudios de Maestría.

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Abbreviations

APF	**A**ctive **P**ower **F**ilters
AM	**A**veraged **M**odel
CCM	**C**ontinuous **C**onduction **M**ode
CI	**C**ontrollability **I**ndex
CMC	**C**urrent **M**ode **C**ontrol
DSP	**D**igital **S**ignal **P**rocessor
DCM	**D**iscontinuous **C**onduction **M**ode
ESR	**E**quivalent **S**eries **R**esistence
FPGA	**F**ield **P**rogrammable **G**ate **A**rrays
FLFB	**F**our-**L**eg **F**our-**B**ridge
FLSC	**F**our-**L**eg **S**plit-**C**apacitor
ID	**I**ntegrated **D**esign
LHP	**L**eft **H**alf **P**lane
LTI	**L**inear **T**ime **I**nvariant
PHC	**P**erfect **H**armonic **C**ancellation
PV	**P**hoto**v**oltaic
PCC	**P**oint of **C**ommon **C**oupling
PEC	**P**ower **E**lectronic **C**onverter
PE	**P**ower **E**lectronics
PWM	**P**ulse-**W**idth **M**odulation
RHP	**R**ight **H**alf **P**lane
SPCD	**S**imultaneously **P**rocess and **C**ontrol **D**esign
TLSC	**T**hree-**L**eg **S**plit-**C**apacitor
THD	**T**otal **H**armonic **D**istortion
ULSS	**U**ltra-**L**arge-**S**cale **S**ystems

UPF	**U**nit **P**ower **F**actor
VLSI	**V**ery-**L**arge-**S**cale **I**ntegration
VOC	**V**oltage **O**riented **C**ontrol
VSI	**V**oltage **S**ource **I**nverter

To my K.A. with her patience and love.

Chapter 1

Introduction

Today, almost all the technologies that require power conversion utilize Power Electronics (PE) technology [1]. This work explores design procedures for Power Electronic Converters (PECs). Particularly those design procedures that take into account both system design and its control. The above due to the fact that the achievable PEC dynamic performance is an inherent system property and that design procedures based only on both economic criteria and steady-state assumptions can lead to difficulty to control PECs, exhibiting poor dynamic performance and unexpected behavior against both disturbance and uncertainties [2].

1.1 Motivation

PECs are used to control power conversion from one or more AC or DC sources to one or more AC or DC loads, sometimes with bidirectional capabilities. In most PE systems, this power conversion is accomplished with two functional modules called control and power stages. PE systems handle power transfer from input to output, or vice versa, and it is constituted of power semiconductor devices acting as switches, plus passive elements such as capacitors and/or inductors. Semiconductor devices such as MOSFET or IGBT are the most commonly switching technology used in PE systems applications. Because the use of this switching technology, PE systems can operate in a range from few watts up to GW, with a frequency range from $100Hz$ up to $100kHz$ or more, depending on the power handled.

The advent of microelectronics and computer control made it possible to apply modern control theory to PE systems and, at the same time, it made possible very complex PE systems functions. Therefore, PE systems field became interdisciplinary. At high power

level, PE systems deal with static and rotating equipment for generation, transmission, and distribution handling large amount of power [3]. For consumer electronic applications, PE systems are important for information processing employing microprocessors, including microcontrollers, Digital Signal Processors (DSP), and Field Programmable Gate Arrays (FPGA) [4]. In the control field, PE systems deal with stability and closed-loop requirements of dynamical performance due to feedback loops [5]. Finally, with the development of Very Large Scale Integration (VLSI) and Ultra-Large-Scale Systems (ULSS), advanced control systems could be used to develop new PE systems topologies [6].

The development of devices and equipment able to efficiently power convert from AC to DC, DC to DC, DC to AC, and AC to AC, along with electrical and control engineering improvement, resulted in a wide spread of PE systems in a large spectrum of applications.

1.2 Literature Review

PECs design is an engineering process that, in general, is carried out in a sequential form as follow: *(a)* PEC structure is selected, then *(b)* passive elements are established such that both cost and losses are minimized, and finally *(c)* PEC control structure is designed such that PEC dynamical performance is optimized. Some works that present this design procedure are [7], [8], [9] [10], and [11]. However, this sequential schema disregards dynamical nature of the system in stages *(a)* and *(b)* and properties such as controllability are not tested. Thus, the designed PEC can be difficult to control, can exhibit a poor dynamical performance and/or an unexpected behavior against both disturbance and uncertainties [2].

In PECs field only few works that take into account the integration of system design and control have been carried out [12], [13], and [2]. In [12], the integrated design and control of a Buck DC-DC converter is investigated. The paper presents dynamical performance optimization of the converter, resulting in a linear state feedback controller synthesized based on covariance control theory. Authors in [13] investigate how to maximize the dynamical performance of a Buck-Boost DC-DC converter using an integrated design and control approach. As the considered Buck-Boost DC-DC converter has nonlinear dynamics, a linearized averaged model is considered to simplify the problem. As controller, a PID is selected. Averaged model parameters and controller parameters to be tuned are state variables dependent, thus a nonlinear optimization problem is obtained. Several Buck-Boost DC-DC converter reference trajectories are taken as reference to measure the converter dynamical performance using a quadratic function cost. These

reference trajectories are including in the function cost to be optimized. Sequential quadratic programming is then used to solve the nonlinear optimization problem.

The two approaches presented by [12] and [13] fix the control structure. They provide optimal parameters for fixed control structure, but they do not, in general, provide the optimal controller. A reason is that selected control structure is linear and it can-not deal with the actuator limitations that are predominant is switched systems. Another reason that avoids finding out the optimal controller is the necessity to test iteratively all possible control structures to find the optimal one.

Authors in [2] tackle the gap between methods that optimally design circuit parameters with a non-optimal controller and optimal control methods. The scope of this work is to optimally design circuit parameters for control purpose that give a performance close to the limits of the circuit, but without imposing any control structure. The considered design objectives are dynamical performance and energy efficiency. In this work is proposed a simultaneous optimization of the circuit parameters and control input using a variable substitution technique and a decomposition of the general min-max problem into two simple min-max problems. The first min-max optimization problem yield the optimal sequence of state for the worse case load, which is unique, one of the sought circuit parameter and an auxiliary control input which embeds the effect of the other disturbances. These results are used in a second min-max optimization problem to obtain real optimal control input and remaining circuit parameters.

In contrast, the integration of system design and control is a mature field of research in chemical engineering known as Integrated Process Design and Control or simply Integrated Design (ID) [14]. Although, in mechatronics field some works that integrate the system design and control has been carried out [15], [16]. The ID conception produces significant economic benefits as well as the improvement of system dynamical performance regarding the important relation between its cost and its controllability [14].

The different possibilities of the integration of design and control are evidenced in the recent literature reviews that have been published in the chemical engineering field [17], [18], [19], [20], [21], and [14]. Authors in [17] remarks on efforts made in the ID and control fields and is made a classification of methods in four categories, as follows: *(a)* process characterization and controllability, *(b)* methods of integrated process design and control, *(c)* plantwide interactions of design and control, and *(c)* extensions of the integrated process design and control.

The following works [18], [19], [20], [21], and [14] concentrate on the optimization-based and simultaneous design and control methodologies. Authors in [18] distinguish two categories into the optimization problem formulation: *(a)* methods that attempt to

design economical optimal processes that can operate in an efficient dynamic mode within an envelope around the nominal operating point and *(b)* methods that consider a single economics-based performance index, while representing system operation and specifications with dynamic rather than steady-state models.

Authors in [19] adopt a classification based on the way the dynamic behavior and its impact on the cost are quantified as follows: *(a)* controllability index-based approach, *(b)* dynamic optimization-based approach, and *(c)* robust model-based approach.

Authors in [20] present a review that separates the controllability-indicators-based methodologies from optimization-based methodologies. However, the main focuses of this work are optimization-based simultaneous design and control formulations and solving strategies, which they classify in: *(a)* controllability-index based optimization, *(b)* mixed integer dynamic optimization, *(c)* robust-based approach, *(d)* embedded control optimization, and *(e)* black-box optimization.

Author in [21] presents a thematic review of the relevant research into integration of process design and control as a starting point and exploration map for the researches in the field. Sharifzadeh's work is organized in three parts: *(a)* first part discusses incentives and barriers for ID and presents the industrial perspective about the subject. *(b)* Second part provides the research review in the field, where two categories of methods are identified as follow: *(1)* methods that have a sequential approach in which the process is designed first, and then the design of its control system is decided; and *(2)*, recognizing interactions between process design and control, methods that integrate process design and control. *(c)* Third part provides summary and discussions of the reviewed methods and suggests future research activities.

Authors in [14] present a classification considering the most important contributions from wide-ranging developments related to the integration of process and control design presented in literature. The classification is based on: *(a)* projecting design methods and *(b)* integrated-optimization design methods. The classification includes aspects as: *(a)* scope of the problem formulation, *(b)* methods to evaluate controllability and other related system properties, *(c)* introduction of advanced control strategies, *(d)* uncertainties and disturbance treatment, and *(e)* optimization problem type and methods to solve it.

From the literature review in the chemical engineering field, methods based on state controllability are selected as candidates to apply in PECs design process, since these methods: *(a)* take into account system dynamical behavior from initial stages of design process; *(b)* are, in general, based on phenomenological model of the system; *(c)* do

not require, in general, the system model linearization ; and *(d)* do not fix the control structure, although system controllability is assured.

Work presented in [22] is a contribution where the design process is carried out to ensure local controllability of input affine nonlinear systems. They consider different process aspects such as: *(a)* available degrees of freedom for control, *(b)* controllability matrix rank (in the sense of Kalman), *(c)* system inversibility, *(d)* range of available control actions, and *(e)* existence of a linear reachable trajectory. These aspects are examined to address problems such as misleading interactions between inputs and states, wrong selection of manipulated variables or final control elements and physical restrictions of the states, which preclude the assurance of practical controllability. The procedure design uses the phenomenological model of the system, established manipulated variables and best input-output variables paring to control. Finally, the control system is designed to suit the optimal plant, knowing that its controllability is assured at the desired operating point.

An extension of work presented in [22] is found in work presented in [23] where a methodology is proposed to verify the controllability of coupled systems based on the accessibility distribution computation and controllable/non-controllable states decomposition.

In work presented in [24], the Hankel matrix is proposed as controllability measure to establish a criterion for ID methodology. In [25] the state-space practical controllability analysis is used as a pre-feasibility step to impose certain restrictions in the integrated design of a sulfitation tower by integrated-optimization methods. The controllability analysis used is composed of following analysis: *(a)* control degrees of freedom, *(b)* rank of the nonlinear controllability matrix, *(c)* determinant of the associated matrix with the forced response, and *(d)* suitability of the forced input with admissible control inputs.

Authors in [26] propose the redesign for a wastewater treatment plant based on the results of the nonlinear state controllability analysis. The set theory in control is used to test the system controllability including both inputs and disturbance boundaries. In work presented in [27] a comparison between differential geometry and set theoretical methods in control based on randomized algorithms to test the nonlinear state controllability is presented. Authors conclude that both methods are equivalent to verify if the system is controllable or not.

Authors in [28] present a detailed methodology description to assess non-linear state controllability in the ID framework. This approach is named by the author Simultaneously Process and Control Design (SPCD). The controllability verification method employed in [28] is based on the differential geometry.

Finally, authors in [29] propose a (SPCD) methodology where the state controllability is tested based on set theory in control. This approach, unlike [28] approach, allows to quantify system controllability, not only establishes if the system is controllable or not. Robust reachable and controllable sets are computed to verify the robust reversible set existence, which is a sufficient condition to verify system local controllability. Then, a Controllability Index (CI) is proposed to quantify the system controllability based on both robust controllable and reversible sest sizes.

In conclusion, the set theory in control is an alternative framework to solve the system controllability problem. Based on the set theory in control, the controllability problem refers to determine the state-space subset that can be reached from the admissible control signals set such that states restrictions are satisfied. The advantages of to analyze the system controllability via set theory in control are: *(a)* the inclusion of inputs and states restrictions in controllability analysis; *(b)* the system need not be input-affine; and *(c)* it is possible to verify the *"robust"* controllability. Moreover, recent works [30], [29], [31] have shown that from obtained results of controllability analysis via set theory in control, it is possible to carry out an optimization process in order to maximize the system controllability.

In PECs field, set theory in control has been used as method to verify the PEC design [32], [33] and to integrate reliability into the design of fault-tolerant power electronics systems [34]. Authors in [32] introduce a technique to obtain the hybrid automaton for representing the behavior of PECs and to perform analysis procedures over the circuit automaton to help the systems designers during the specification, development and design phases. Moreover, a systematic procedure to obtain a new controller to the converter is implemented. The modeling process can treat refinement requirements of the semiconductor devices of the circuits and also it is possible to model and analyze PEC with time varying sources. As verification method, the reachability method is implemented by a direct search in the state-space of the system, without information loss from the system behavior. The verification procedure receives both reachable set and properties specifications as input to test whether desired properties are valid or not.

Authors in [34] introduce a methodology to analyze the behavior of fault-tolerant PE systems in the presence of component faults. Rather than using a qualitative description of system functionality, authors use a state-space representation of dynamics based on averaging and linearization. The methodology takes into account the uncertainty associated to the converter uncontrolled inputs such as input voltage variations. The model assumes that uncertainty of uncontrollable inputs is unknown but bounded. Then, using techniques developed in the context of reachability analysis of Linear Time Invariant

(LTI) systems, the uncertainty in the uncontrollable inputs is propagated to the converter state variables, which also become uncertain. Authors conclude that in not-faulty condition, assuming that the converter is properly designed, converter state variables remain within a region of space-state defined by performance requirements. In contrast, in the presence of a component fault, the uncertainty in the uncontrolled inputs are propagated differently to converter state variables, which might result in the state variables being outside the region of the state-space defined by performance requirements. The overall converter reliability is then computed to include the probability in which the converter will meet the performance requirements into the formulation of a Markov reliability model.

Authors in [35] returning into the work developed in [34], where the reachability problem is formulated in terms of the linearized converter averaged model without including converter switching effects and the proposed solution to the reachability problem relied on the computation of a bounding ellipsoid, which does not provide an exact solution. Authors solve these problem as follow: *(a)* formulating the reachability problem in terms of the converter large-signal model; and *(b)* providing a method to compute the exact solution to the reachability problem rather than providing an upper bound. Methods used by authors to solve reachability problem provide an exact solution using ellipsoidal calculus. Algorithms for addressing the verification of both open-loop and closed-loop controlled PE systems are provided.

Authors in [36] extend the work presented in [35] by: *(a)* providing a precise formulation of the reachability problem in DC-DC converters; *(b)* tailoring ellipsoidal-based reachability tools to cases when the input space is defined by a symmetric polytope; *(c)* providing a more detailed analysis of open-loop and closed-loop controlled buck and boost converters; *(d)* providing a detailed comparison of the computational performance of the proposed method with simulation-based Monte Carlo methods; and *(e)* providing a method to address parametric uncertainty. According to authors, technique employed to solve reachability problem provides a computationally tractable solution to the large-signal behavior verification problem for PE systems. This method can substantially reduce the computational burden of existing time-domain simulation-based large-signal behavior verification methods, which rely on performing a large number of simulations in order to capture the behavior of the system for all possible operating conditions. Finally, the analytically tractable solutions provided by the proposed method also give further insight into the influence of design parameters and control techniques on the overall system performance.

Finally, author in [33] present two methods for performing design verification of PECs: *(a)* first method can be used to compute the set of reachable states from an initial set

of states with non-deterministic parameters. *(b)* Second method uses model checking to verify circuits that can naturally be modeled as timed automata. Authors test method *(a)* on a buck converter in an open-loop configuration. Method *(a)* is automatic and uses the hybrid systems reachability analysis tool SpaceEx. Authors test method *(b)* on an open-loop multilevel converter used to convert several DC inputs to one AC output. Method *(b)* is also automatic and uses the timed automata model checker Uppaal. Finally, authors mention that in contrast to simulation or testing based approaches (standard Monte Carlo analysis), methods presented in their work perform the verification for all runs of the circuits and all possible component parameter variations. The main authors contribution is to show that some analog circuits can be naturally modeled as timed automata.

1.3 Literature Review Conclusions

Following conclusions are derived after literature review: *(a)* in PECs field, only few works that include the system dynamical inherent nature are carried out, and works carried out have following limitations: *(1)* control structure is fixed and/or *(2)* design process implies sophisticated optimization stages. *(b)* Integrated design and control is a mature field in chemical engineering and, despite that most of the developed methodologies include any optimization stage, well-founded analysis such as controllability analysis can be applied as preliminary step before applying any optimization method to process design. *(c)* State controllability analysis are preferred over input-output controllability analysis due to the fact that state controllability analysis, in general, are based on system phenomenological models and they allow to have a complete knowledge of internal system evolution. *(d)* Within state controllability analysis, such analysis based on set theory in control are highlighted due to the fact that not only test if the system is controllable or not but also quantify the system controllability. *(e)* Set theory in control has been used as method to verify the PEC design and to integrate reliability into the design of fault-tolerant power electronics systems, but it is not used as method to verify system controllability as preliminary step before applying any optimization method to PEC design.

1.4 Research Problem

There has been few works which include the PEC dynamical inherent nature. Those works carried out have the following limitations: *(1)* control structure is fixed and/or *(2)* design process implies sophisticated optimization stages. Additionally, none design

process include the controllability analysis as preliminary step before applying some optimization method to PEC design. Therefore, the research question that conducts this work is:

> ***How to formulate a systematic design procedure for designing a Power Electronic Converter including the inherent system dynamical behavior, with verified controllability, but without fix the control structure?***

Chapter 2

General Framework

In this chapter the basis of: *(a)* PECs modeling issues, *(b)* system controllability, and *(c)* PECs control issues are introduced. Both large-signal and small-signal models of PECs are discussed. Basis of system controllability in both linear and nonlinear cases are introduced. The procedure to verify the system controllability via Lie Brackets is presented. An Monte Carlo based algorithm to compute an approximation of reachable and controllable sets is given as well as to compute an approximation of their robust version. A Controllability Index CI is presented to quantify the system controllability based on both reachable and reversible sets. Finally, issues about control theory applied to PECs application are discussed and definitions of PI/PID controllers are given.

2.1 Modeling Issues

Modeling and simulation of PE systems are essential steps that enable design verifications and control of numerous electrical energy systems including modern electric grid and its components, distributed energy resources, as well as electrical systems of ships, aircraft, vehicles, industrial automation, among others [37]. With the development of modern simulation tools, the detailed models of power-electronic components and modules (where the switching of all diodes and transistors is taken into account) may be readily implemented using a number of commercially available digital programs and/or simulators such as MatLab, PSIM, LabView, etc.

According to work presented in [38], it is possible to obtain the switched model of any Power Electronic Converter (PEC) and its bilinear form by two methods: *(a)* listing all its possible configurations and finding a general structure which leads to bilinear form, or *(b)* applying the method to emphasize the variables that exhibits switched-time evolution.

In this work, the method *(a)* is adopted for PECs modelling due to the fact that the method is based on PEC circuital analysis [39].

2.1.1 Large-Signal Models

A generic PEC is described as dynamical system as in equation (2.1).

$$\frac{dx(t)}{dt} = A_i x(t) + B_i e(t); \qquad t_i \leq t \leq t_{i+1} \tag{2.1}$$

with

$$\sum_{i=1}^{N} (t_i - t_{i-1}) = T$$

Where T is switched time, N is number of possible configurations, t_i are different time points defining the switching between N configurations, A_i and B_i are $n \times n$ state matrix an $n \times p$ input matrix respectively, corresponding to i configuration, $x(t)$ is $n - length$ state vector and $e(t)$ is $p - length$ vector of independent sources of the system.

A more compact form to represent a generic PEC is given by the equation (2.2).

$$\frac{dx(t)}{dt} = \sum_{i=1}^{N} \left(A_i x(t) + B_i e(t)\right) h_i \tag{2.2}$$

Where h_i are respective validation functions associated to each i configuration. h_i functions take values of 1 or 0 depending on whether their respective configurations are activated or not.

Derived by the equation (2.1), it is possible to obtain a suitable structure called bilinear form. Bilinear form provides a more compact representation of PEC switched model, while showing the control inputs explicitly [38]. Instead of using h_i functions, it is possible to condensate the information in a single unified model which is fed with p binary functions. p binary functions are denoted by u_k, usually named switching functions. The number p is determined as the small integer satisfying the relation $2p >= N$.

Bilinear form of the switched model is expressed by general equation given by (2.3).

$$\frac{dx(t)}{dt} = Ax(t) + \sum_{k=1}^{P} \left(B_k x(t) + b_k\right) U_k + e(t) \tag{2.3}$$

Where, for every k from 1 to p, $B_k \in R^{nxn}$, $b_k \in R^{1xn}$ and $e \in R^{1xn}$. The products between state variables and control inputs give the bilinear feature of the model.

The switched model, in its general or bilinear form, describes the so-called high frequency dynamics of the system and its suitable, e.g., to design non-linear control laws like sliding-mode control [40], [41], [42], [43].

The Averaged Model (AM), derived from the general form, focuses on capturing the low-frequency behavior of PECs neglecting high-frequency variations due to circuit switching [39]. AM can be obtained through application of the averaging method and it is suitable, e.g., to design linear control laws such as traditional PI/PID control. Applying the averaging method, it is possible to transform the original discontinuous model into a continuous invariant model that provides the best representation of the macroscopic PEC behavior [37].

The state of switches can be represented by the switching functions u_k as in Figure (2.1). When the switch is closed, output $S = E.u$ is equal to input source E. Otherwise, S is equal to 0.

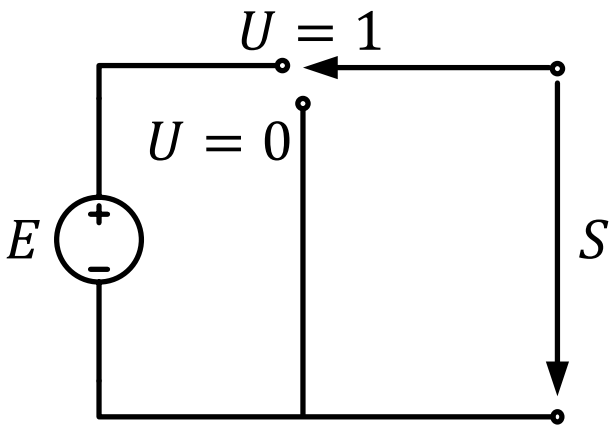

FIGURE 2.1: On-off switch

Without employing any simplification its average value is given by the equation (2.4).

$$S = E \cdot U \Longrightarrow \langle S \rangle_o = \langle E \cdot U \rangle_o \tag{2.4}$$

When equation (2.4) is developed, two cases can occur:

1. E is a constant value and it is obtained an exact relation given by (2.5).

$$\langle S\rangle_o = \langle E\rangle_o\langle U\rangle_o = E\langle U\rangle_o \tag{2.5}$$

2. E is a variable, S is given by an approximation from equation (2.6).

$$\langle S\rangle_o = \langle E\rangle_o\langle U\rangle_o \tag{2.6}$$

Equations (2.5) and (2.6) are justified if one of E or u is close to its average value (the small-ripple assumption). If E is supposed constant, E takes its average value.

In order to obtain an AM that separates u_k from the passive elements (L, C, R), the following properties can be used: *(a)* Preservation of circuit configurations by replacing the variables with their averages: the derivative of the average is the average of derivative (Equation (2.7)), implying that the relations between currents and voltages are the same as those linking their averages, i.e., for an inductor L: $v_L(t) = L\frac{di_L}{dt}$.

Due to R, L ,and C remains unchanged after circuit averaging operation, property *(b)* is defined as follows: *(b)* Replacement of the products of variables by the products of average, which means that the configuration of passive circuit remains unchanged by averaging.

$$\frac{d}{dt}\langle f(t)\rangle_o(t) = \langle\frac{d}{dt}f(t)\rangle_o(t) \tag{2.7}$$

Analytical approach to obtain PEC AM is as follow: *(1)* Starting from the bilinear form (Eq. (2.3)), *(2)* applying the averaged operator (Eq. (2.4)), and *(3)* approximating the average of product by the product of average, where the matrices A, B_k, and b_k are invariant. Considering topological equations (2.2), AM of PECs is given by the equation (2.8).

$$\frac{d}{dt}\langle x(t)\rangle_o = A\langle x(t)\rangle_o + \sum_{k=1}^{P}\left(B_k\langle x(t)\rangle_o + b_k\right)d_k + e \tag{2.8}$$

Where $d_k = \langle u_k\rangle_0$ is the duty radio of the switching function u_k for each k from 1 to p.

Models given by equations (2.1)-(2.8) are called large-signal models (usually nonlinear for PECs) since they are valid for the entire definition PEC operation range.

2.1.2 Small-Signal Models

General continuous nonlinear system given by equations in (2.9) is considered for deducing small-signal PEC model.

$$\begin{aligned} \frac{dx}{dt} &= f\left(x\left(t\right), u\left(t\right)\right) \\ y &= h\left(x(t), u(t)\right) \end{aligned} \tag{2.9}$$

Where x, u, and y are state, input, and output vectors, respectively.

By zeroing the derivatives, it is possible to obtain the steady-state input-output characteristic, i.e., the locus of the system equilibrium point, denoted with the subscript e and represented by a generally nonlinear curve in the input-output plane given by the equation (2.10).

$$Y_e = g\left(U_e\right) \tag{2.10}$$

Now the small variations established in response to input u_e ($\tilde{x} = x - x_e$, $\tilde{u} = u - u_e$, and $\tilde{y} = y - y_e$) around a given equilibrium point y_e are considered. Thus, the linearized system around a specified equilibrium point is given by equations in (2.11).

$$\begin{aligned} \tilde{\dot{x}} &= A\tilde{x} + B\tilde{u} \\ \tilde{y} &= C\tilde{x} + D\tilde{u} \end{aligned} \tag{2.11}$$

With

$$\begin{aligned} A &= \left(\frac{\partial f\left(x,u\right)}{\partial x}\right)_{x_e,u_e} & B &= \left(\frac{\partial f\left(x,u\right)}{\partial u}\right)_{x_e,u_e} \\ C &= \left(\frac{\partial h\left(x,u\right)}{\partial x}\right)_{x_e,u_e} & D &= \left(\frac{\partial h\left(x,u\right)}{\partial u}\right)_{x_e,u_e} \end{aligned} \tag{2.12}$$

In the case of bilinear systems, some simplifications are made: *(a)* to neglect the products of variations corresponding to higher than second order terms in the Taylor series expansion and *(b)* to simplify terms corresponding to $x = 0$.

After simplifications, the resulting model is described by the same matrices as those corresponding to the linearized model represented by equations in (2.11), i.e., those given by equations in (2.12).

The small-signal model may also be expressed in the frequency domain, i.e., as transfer functions, which can be computed based upon the matrices given by equations in (2.12). Equation (2.13) is a common realization that relates state-space model with system transfer functions.

$$G(s) = \frac{1}{det(sI - A)} C\left[adj(sI - A)\right] B + D \tag{2.13}$$

In this work, the switched model is adopted as starting point to derive average and small-signal models because it is a tool that emphasizes on the presence of external control action. In its bilinear form this model can be directly used for simulation and control design purposes. Furthermore, the switched model offers a starting point to obtain other types of models such as averaged or reduced-order, which are useful to represent low-frequency dynamics in the system neglecting high-frequency dynamics and to deduce frequency-domain models of the system [37].

2.2 Controllability

Due to the existence of unmanipulated inputs (system disturbances), PECs need an additional system known as controller. Some of the controller functions are disturbance rejection, output regulation, and both high efficiency and safe PEC operation.

To implement a control structure, it is needed that inputs have an impact over outputs, i.e., the system must be controllable. The controllability is the system's property that describes the interaction between inputs and state variables. Hence, the controllability is the first property that must be verified during or after system design. The controllability can be interpreted as the existence and uniqueness theory extension of differential equations to the formalization of family solutions of forced differential equations that represent a system control and its possible behaviors [44].

Since 1960 Kalman presented his work *"On the general theory of control systems"*, the rank of controllability matrix is evaluated to test this property in linear systems represented by a state-space model. Even, this test have been applied in PE system field [45], [46], [47], [48] to verify the system controllability.

In non-linear case, state controllability verification requires to incorporate the accessibility concept. Although, both global and local controllability as well as global and local accessibility are differentiated [44]. To test the controllability in non-linear systems case, some tools have been employed such as Lie brackets method [27], [28] and set theory in control [44], [29], [49].

Rank controllability matrix evaluation and Lie brackets method only verify if the system is controllable or not. In the other hand, controllability analysis via set theory allows the system controllability verification and quantification [50], [51], [29]. Authors in work presented by [27] show that controllability analysis via set theory and via differential geometry (Lie brackets) are equivalent.

In this subsection, basic controllability concepts and conditions are introduced as well as algorithms to verify the system controllability. First, the controllability fundamentals of linear systems are presented. Then, the controllability concepts, conditions, and algorithms to verify this property in nonlinear systems are presented. It is important to remark that in the nonlinear system case, the controllability verification is possible only about an equilibrium point. Nonlinear systems can have multiples equilibrium points, then if a nonlinear system is controllable about an equilibrium point, not necessarily is completely controllable.

2.2.1 Linear Systems Controllability

To study the linear systems controllability, the Linear Time Invariant (LTI) system given by the equation (2.14) must be considered.

$$\begin{aligned} \dot{x}(t) &= Ax(t) + Bu(t) \\ y(t) &= Cx(t) + Du(t) \end{aligned} \tag{2.14}$$

where $x(t)$, $y(t)$, and $u(t)$ are vectors valued functions, and A, B, C, and D are matrices. The derivative $\dot{x}(t)$ is the vector formed from derivatives of each scalar entry in $x(t)$. The variable $t \geq 0$ is *time* and the function $u(t)$ is referred to as the system *input*. The functions $x(t)$ and $y(t)$ are called *state* and *output* of the system, respectively, and depend on the input.

The dimensions of vectors are:

$$x(t) \in R^n, u(t) \in R^m, and \quad y(t) \in R^p \tag{2.15}$$

Thus A is an $n \times n$ matrix, B is an $n \times m$ matrix, C is an $p \times n$ matrix, and D is an $p \times m$ matrix.

Definition 2.1. Controllability [52]: A state x of a plant is said to be *"controllable"* if there exists a control signal $u(t)$ defined over a finite interval $0 \leq t \leq t_1$ such that $\Phi(t_1; x, 0) = 0$. In general, the time t_1 will depend on x. If every state is controllable, the plant is said to be *"completely controllable"*

Where the function Φ is defined by Kalman as a transition function that represents the system evolution from initial state $x_0(t_0 = 0)$ to final state $x(t_1) = \Phi(t_1; x(t_0), t_0)$. If the final state $x(t_1) = 0$ is a equilibrium state, then this state is controllable.

Remarks

- The linear systems controllability is a global property, since the only equilibrium of a linear system is the origin.
- In Kalman's definition, the input u is not bounded, thus u can takes values in the rage $(-\infty, \infty)$.
- In Kalman's definition, the controllability is a system *quality*. Each system state is controllable or not. Therefore, a intermediate possibility is not considered in this definition, thus, a controllability quantification is impossible.

In order to verify the controllability in linear systems, the controllability matrix is defined.

Definition 2.2. Controllability matrix: The matrix $W \in R^{n \times nm}$ defined as $W = \begin{bmatrix} B & AB & \dots & A^{n-1}B \end{bmatrix}$ is known as the controllability matrix.

Once the controllability matrix is defined, the theorem that allows to verify the system controllability is given.

Theorem 2.3. ***The rank condition****: The LTI system given by the equation (2.14) is controllable if only if* $Rank(W) = n$.

An important issue of the controllability matrix is that only involve matrices A and B of the LTI model given by the equation (2.14). This because the controllability property only relates the input variables with system states.

Next, the rank condition interpretation is given. In order to facilitate the understanding of this condition, the discrete time linear system given by the equation (2.16) is considered.

$$x(k+1) \quad = \quad Ax(k) + Bu(k) \tag{2.16}$$

Interpretation of the controllability matrix rank condition. The controllability matrix appears from recursively solution of the system given by the equation (2.16). The recursively solution of the system given by the equation (2.16) is given by the equation (2.17).

$$x(k) \quad = \quad A^k x(0) + WU, \quad with \quad U = \begin{bmatrix} u(k-1) & u(k-2) & \dots & u(1) & u(0) \end{bmatrix}^T \tag{2.17}$$

Assuming that the control action U is unknown, to reach the origin is needed to solve the linear system given by the equation (2.18).

$$WU \quad = \quad -A^k x(0) \tag{2.18}$$

The linear system given by the equation (2.18) has a single solution if $Rank(W) = n$. If $Rank(W) < n$, only some system states can be reached. The reached states are those that belong to the linear combination of the column vector of W.

Other highlighted definition is the *reachability*.

Definition 2.4. Reachability [44]: A linear system is reachable if for all $x_1, x_2 \in R^n$ exist a control action u such that the system can be driven from the initial state x_1 to the final state x_2 in a finite time t.

Remarks

- The reachability is the ability of a linear system reaches any final state from a initial state. In the other hand, the controllability is the ability of a linear system reaches the origin from an initial state. The controllability also can be interpreted as the ability of a linear system reaches an state, where this state is a equilibrium point of the forced system.
- In the LTI system, controllability and reachability coincide.

2.2.2 Nonlinear Systems Controllability

Equations (2.19) and (2.20) must be considered in order to introduce accessibility and controllability concepts of nonlinear systems.

$$\sum : \dot{x}(t) \quad = \quad f(x(t), u(t)) \tag{2.19}$$

$$\sum_{aff} : \dot{x}(t) \quad = \quad f(x(t)) + \sum_{i=1}^{m} u_i g_i(x(t)) \tag{2.20}$$

Where, $x(t) \in X$ is the *state* of the system, with X an open subset on R^n or a manifold M of dimension n. $u(t) \in U$ are *inputs* or *control actions*, with U a subset of R^m. The function f is real analytic and $u(\cdot)$ are measurable and bounded, i.e., $\max |u| < \infty$. $\phi(t, x, u)$ is a system transition function, where $\phi(t, x, w) = z$ means that, from $x(0) = x$, the system evolve to $x(t) = z$ using as control signal $w : [0, t] \to U$.

Reachability and controllability are not equivalent concepts in the nonlinear system case. Moreover, reachability is a weaker property than controllability [53], also called weak controllability or accessibility.

Definition 2.5. Reachability in time T [44]: It is said that z is reached from x in time T or, equivalently, that x is controllable to z in time T, if exist a control signal $w : [0, t] \to U$ such that $\phi(T, x, w) = z$.

Definition 2.6. Reachability [44]: It is said that z is reaches from x or, equivalently, that x is controllable to z if exist $T \geq 0$ and a control signal $w : [0, t] \to U$ such that $\phi(T, x, w) = z$.

The notation $x \underset{T}{\to} z$ will be used if z is reaches from x in time T (Definition 2.5). The notation $x \to z$ will be used if z is reached from x (Definition 2.6).

An interpretation of nonlinear systems reachability can be found in [44, pp. 33-36].

Definition 2.7. Local reachability [44]: The system given by the equation (2.19) is locally reachable about the point $x_1 \in X$ if exist a vicinity V of x_1 such that the system can reaches any state x_2 in a finite time and with admissible control actions.

Definition 2.8. Local controllability [44]: The system given by the equation (2.19) is locally controllable in x_o if for each vicinity U of x_o, $\mathcal{R}_U(x_o)$ also is a vicinity of x_o.

Definition 2.9. Controllability [44]: The system given by the equation (2.19) is (completely) controllable in time T, if for each $x, z \in X$ states it holds that $x \underset{T}{\rightarrow} z$. Likewise, it is just (completely) controllable if for each $x, z \in X$ it holds that $x \rightarrow z$.

Additional related controllability concepts are reachable and controllable sets, which are defined as follow:

Definition 2.10. Reachable set [53]: The *reachable set* from x in time T is

$$\mathcal{R}^T(x) = \{z \in X | x \underset{T}{\rightarrow} z\} \tag{2.21}$$

The *reachable set* from x is

$$\mathcal{R}(x) = \{z \in X | x \rightarrow z\} = \bigcup_{T \geq 0} \mathcal{R}^T(x) \tag{2.22}$$

if $\mathcal{S}$ is a subset of X, also it can be defined

$$\mathcal{R}^T(\mathcal{S}) = \bigcup_{x \in \mathcal{S}} \mathcal{R}^T(x) \tag{2.23}$$

$$\mathcal{R}(\mathcal{S}) = \bigcup_{x \in \mathcal{S}} \mathcal{R}(x) \tag{2.24}$$

for the sets reachable from the subset $\mathcal{S}$.

Definition 2.11. Controllable set [53]: The *controllable set* to x in time T is

$$\mathcal{C}^T(x) = \{z \in X | x \underset{T}{\rightarrow} z\} \tag{2.25}$$

The *controllable set* to x is

$$\mathcal{C}(x) = \{z \in X | x \rightarrow z\} = \bigcup_{T \geq 0} \mathcal{C}^T(x) \tag{2.26}$$

if $\mathcal{S}$ is a subset of X, also it can be defined

$$\mathcal{C}^T(\mathcal{S}) = \bigcup_{x \in \mathcal{S}} \mathcal{C}^T(x) \tag{2.27}$$

$$\mathcal{C}(\mathcal{S}) = \bigcup_{x \in \mathcal{S}} \mathcal{C}(x) \tag{2.28}$$

for the sets controllable to the subset $\mathcal{S}$.

Definition 2.12. Controllability [44]: The system given by the equation (2.19) is (completely) controllable to x if $\mathcal{C}(x) = X$. The system given by the equation (2.19) is (completely) reachable from x if $\mathcal{R} = X$.

Remark: Definition 2.12 establishes that the (completely) controllability implies that a system can go from any state to the all state-space. However, verify when a nonlinear system is controllable still is an open research problem [44].

Exist tests that establish *necessary conditions*, *but insufficient*, to verify the system controllability. A test is the rank condition of the Lie brackets [53]. Lie brackets allow to verify when a system is reachable. However, reachability is a weaker property than controllability. Figure (2.2) shows differences between reachability and controllability for a bi-dimensional system. Figure (2.2a) shows an unreachable system; the system only can be driven in one direction in the state-space. Figure (2.2b) shows an reachable system; the system can be driven in a subspace of the state-space. Figure (2.2c) shows an controllable system; the system can be driven in any state-space direction.

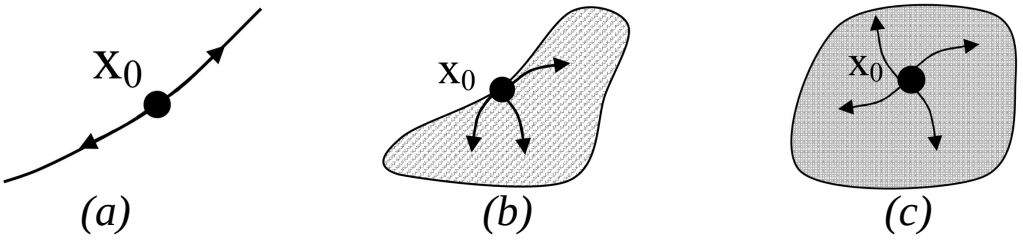

FIGURE 2.2: *(a)* unreachable, *(b)* reachable, and *(c)* controllable.

The Lie brackets give a framework that allows to verify the accessibility in the nonlinear systems case. The Lie brackets are a linear combination of the vector fields obtained from the nonlinear system mathematical model. Lie brackets allow to study interconnections among dynamical systems in a independent coordinate system.

The nonlinear control system given by the equation (2.19) can be seen as a family of dynamical systems (vector fields) parameterized by a parameter called control $f_u = f(\cdot, u)$ that defines a vector fields family as $\mathcal{F} = \{f_u\}_{u \in U}$. In this way, the basic properties of the dynamical systems given by the equation (2.19) depend on the interconnections among these systems associated with the different controls.

Next, the necessary definitions of Lie algebra and brackets are given in order to indicate the rank Lie brackets condition to verify the system accessibility.

If $f = (f_1, \ldots, f_n)' : \mathcal{O} \to R^n$ is a continuously differentiable map or a *smooth* vector field (infinitely differentiable) defined on some open subset $\mathcal{O} \subseteq R^n$. The set of all (smooth) vector fields on a given $\mathcal{O} \subseteq R_n$ is denoted by $\mathbb{V}(\mathcal{O})$.

Definition 2.13. Lie bracket [44]: The *Lie bracket* of $f, g \in \mathbb{V}(\mathcal{O})$ is another vector field on X defined as follows

$$[f, g] \quad = \quad \frac{\partial g}{\partial x}(x) f(x) - \frac{\partial f}{\partial x}(x) g(x) \tag{2.29}$$

where $\dfrac{\partial f}{\partial x}$ and $\dfrac{\partial g}{\partial x}$ denote the Jacobi matrices of f and g, respectively.

Definition 2.14. Lie Algebra [53]: A *Lie algebra* (of vector fields on $\mathcal{O}$) is a linear subspace $S \subseteq \mathbb{V}(\mathcal{O})$ that is closed under the Lie bracket operation, that is, $[f, g] \in S$ whenever f and g are in S.

A Lie algebra associated with the system $\sum$ (see equation (2.19)) is the smaller linear space of vector fields in X. This linear space contain the family $\mathcal{F}$ and is closed under the Lie bracket, that is

$$f_1, f_2 \in \mathcal{L} \Rightarrow [f_1, f_2] \in \mathcal{L} \tag{2.30}$$

For any subset $\mathcal{A} \subseteq \mathbb{V}(\mathcal{O})$, it is defined $\mathcal{A}_{LA}$, the *Lie algebra generated by* $\mathcal{A}$, as the intersection of all the Lie algebras of vector fields which contain $\mathcal{A}$. (The set of all such algebras is nonempty, since it includes $\mathbb{V}(\mathcal{O})$). An intersection of any family of Lie algebras is also a Lie algebra; thus, $\mathcal{A}_{LA}$ = smallest Lie algebra of vector fields which contains $\mathcal{A}$.

From the system given by the equation (2.19), the set of vector fields given by the equation (2.31) is assigned.

$$\mathcal{A} \quad = \quad \{f_u = f(\cdot, u), u \in U\} \tag{2.31}$$

Definition 2.15. Accessibility Lie Algebra [44]: The Lie algebra of the vector fields $\mathcal{A}_{LA}$ is called *accessibility Lie algebra* of the system $\sum$. The rank accessibility condition in x_o is satisfied if $\mathcal{A}(x_o) = R^n$.

Theorem 2.16. ***nonlinear systems reachability [54]:*** *The system given by the equation (2.19) is reachable if only if the rank accessibility condition is satisfied.*

In the input-affine systems (see equation (2.20)), it is possible to compute the accessibility Lie algebra as in the Lemma 2.17.

Lemma 2.17. *For a system given by the equation (2.20),* $\mathcal{A}_{LA} = \{f, g_1, \ldots, g_m\}$.

If the system is reversible, reachability is a necessary and sufficient controllability condition [53, Corollary 4.3.12, p. 159].

It is possible to stablish a direct connection between rank accessibility condition and reachable and controllable sets.

Theorem 2.18. ***[53]:*** *Assuming that the accessibility rank condition holds at* x_o*. Then, for each neighborhood* $\mathcal{V}$ *of* x_o*, and each* $T > 0$*,*

$$\text{int}\mathcal{R}_{\mathcal{V}}^{\leq T}(x_o) \neq \emptyset \tag{2.32}$$

and

$$\text{int}\mathcal{C}_{\mathcal{V}}^{\leq T}(x_o) \neq \emptyset \tag{2.33}$$

In particular, $\mathcal{R}(x_o)$ *and* $\mathcal{C}(x_o)$ *have nonempty interiors.*

From Theorem 2.18, it follows that if the rank accessibility condition is satisfied in x_o, exist a neighborhood $\mathcal{V}_{\mathcal{R}}$ of full dimension about x_o such that the system can reach. Additionally, exist a neighborhood $\mathcal{V}_{\mathcal{C}}$ of full dimension such that the system can reach to x_o. Not necessarily $\mathcal{V}_{\mathcal{R}} = \mathcal{V}_{\mathcal{C}}$.

Definition 2.19. Reversibility [53]: A system is *weakly reversible* if $\rightarrow$ is an equivalent relation, and *strongly reversible* if for each x_o and each $w \in \mathcal{L}_U^{\infty}(0, T)$ admissible for x_o, there is some $v \in \mathcal{L}_U^{\infty}(0, T)$ which is admissible for $z_o = \phi(T, 0, x_o, w)$ and is such that $\phi(t, 0, x_o, w) = \phi(T - t, 0, z_o, v)$ for all $t \in [0, T]$

That is, weakly reversible means that $z_o \in \mathcal{R}(x_o)$ if only if $x_o \in \mathcal{R}(z_o)$, and strongly reversible means that the same path that takes the system from x_o to z_o can be traveled backward. Strong reversibility implies weak reversibility, but not conversely.

Proposition 2.20. ***[53]:*** *Assuming that the accessibility rank condition holds at* x_o*. If the system given by the equation (2.19) is weakly reversible, then*

$$x_o \in \text{int}\left(\mathcal{R}(x_o) \bigcap \mathcal{C}(x_o)\right) \tag{2.34}$$

Moreover, if it is strongly reversible, then

$$x_o \in \text{int}\left(\mathcal{R}_{\mathcal{V}}^{\leq T}(x_o) \bigcap \mathcal{CV}^{\leq T}(x_o)\right) \tag{2.35}$$

for every neighborhood $\mathcal{V}$ *of* x_o *and every* $T < 0$.

Corollary 2.21. *[53]: For a weakly reversible system, if the accessibility rank condition hold at every state* $x \in X$ *is connected, then the system is* completely controllable.

Conditions to verify the input-affine system controllability are full established with Definition 2.19, proposition 2.20, and corollary 2.21.

2.2.3 Set Theory in Control

The set theory in control is an alternative framework to solve the controllability problem. Based on the set theory in control, the controllability problem refers to determine the state-space subset that can be reached from the admissible control signals set such that states restrictions are satisfied. The advantages of to analyze the system controllability via set theory in control are: *(a)* the inclusion of inputs and states restrictions in controllability analysis; *(b)* the system need not be input-affine; and *(c)* it is possible to verify the *"robust"* controllability. Moreover, recent works [30], [29], [31] have shown that from obtained results of controllability analysis via set theory in control, it is possible to carry out an optimization process in order to maximize the system controllability.

The controllability framework from the set theory in control is the same as the nonlinear controllability. Therefore, the system given by the equation (2.19) is considered in this section to verify the system controllability via set theory in control. Function transition, reversibility and both reachable and controllable sets concepts also are considered.

From an initial state, it is possible to know all states that can be reached for the system in a time t if the function transition ϕ is evaluated in each control signal. Next, a functional space is defined for the control signals.

Definition 2.22. Control signals space [27]: Given a time interval $[\sigma, \tau)$ and a subset $U \subseteq R^m$, the *control signals space* $U^{[\sigma,\tau)}$ is defined for all admissible function in the form $w : [\sigma, \tau) \to U$

Then, it is possible to redefine both reachable and controllable sets as follow.

Definition 2.23. Reachable set in time t**:** Taking $t = \tau - \sigma$, the *reachable set* can defined as follow:

$$\mathcal{R}^t(x_o) \quad = \quad \{z | \phi_{w_i}(t; x_o, 0) = z\} \quad \forall w_i \in U^{[\sigma,\tau)} \tag{2.36}$$

Definition 2.24. Controllable set in time t: Taking $t = \tau - \sigma$, the *controllable set* can be defined as follow:

$$\mathcal{C}^t(x_o) \quad = \quad \{z|\phi_{w_i}(t;z,0) = x_o\} \quad \forall w_i \in U^{[\sigma,\tau)} \tag{2.37}$$

Figure (2.3) shows an interpretation of both reachable and controllable sets. Only a few paths are depicted, however, bot reachable and controllable set are the result of infinite paths.

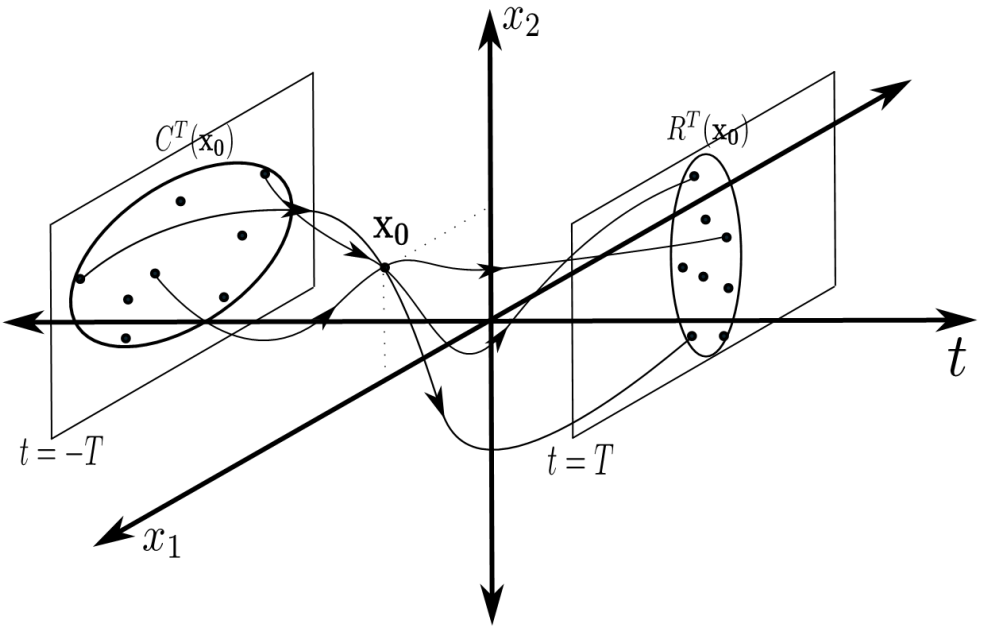

FIGURE 2.3: Reachable and controllable set in time $t = T$.

Definitions of reachable and controllable sets can be extended to a subset of initial conditions $\Omega_o \in X$ as follow.

Definition 2.25. Reachable set from Ω_o in time t: Given the subset $\Omega_o \in X$, the *reachable set from Ω_o in time t* can be defined as follow:

$$\mathcal{R}^t(\Omega_o) \quad = \quad \{z|\phi_{w_i}(t;\Omega_o,0) = z\} \quad \forall w_i \in U^{[\sigma,\tau)} \tag{2.38}$$

Definition 2.26. Controllable set to Ω_o in time t: Given the subset $\Omega_o \in X$, the *controllable set to Ω_o in time t* can be defined as follow:

$$\mathcal{C}^t(\Omega_o) \quad = \quad \{z|\phi_{w_i}(t;z,0)=\Omega_o\} \quad \forall w_i \in U^{[\sigma,\tau)} \tag{2.39}$$

The reversible set $\tau^t(\Omega_t)$ can be defined based on weakly controllability and both reachable and controllable sets definitions as follow.

Definition 2.27. Reversible set in time t: Given the subset $\Omega_t \in X$, The *reversible set from Ω_t to Ω_t in time t* can be defined as follow:

$$\tau^t(\Omega_t) \quad = \quad \{\Omega_t|\phi_{w_i}(t;\Omega_t,0)=\Omega_t\} \quad \forall w_i \in U^{[\sigma,\tau)} \tag{2.40}$$

The *reversible set from Ω_t to Ω_t in time t* can be defined also as follow:

$$\tau^t(\Omega_t) \quad = \quad \{\Omega_t|\phi_{w_i}(t;\Omega_t,0)\subseteq\mathcal{R}^t(\Omega_t)\wedge\phi_{w_i}(t;\Omega_t,0)\subseteq\mathcal{C}^t(\Omega_t)\} \quad \forall w_i \in U^{[\sigma,\tau)} \tag{2.41}$$

or equivalently

$$\tau^t(\Omega_t) \quad = \quad \mathcal{R}^t(\Omega_t)\bigcap\mathcal{C}^t(\Omega_t) \tag{2.42}$$

Remarks: Based on definitions (2.25) - (2.27), $\mathcal{R}^t$ is the set composed of all state-space vectors that can be reached by the dynamical system evolution under effects of admissible control signals in a time t. $\mathcal{C}^t$ is the set composed of all state-space vectors that are inside Ω_t, which is the result of the system dynamical evolution under effects of admissible control signals in a time t. Finally, τ^t is the set composed of all state-space vectors for which, under effects of any admissible control signal, the system can evolve from an initial state x_0 to final state x_t and return in a finite time t.

To analyze the state controllability in nonlinear systems via set theory, it is enough that $\text{int}(\tau^t(\Omega_t)) \neq \emptyset$. Since, a nonlinear system is controllable if: *a.* the system satisfies the rank condition and *b.* is, although, weakly reversible [49]. First condition leads to verify the dimension of Lie algebra associated to the system. However, the Lie algebra associated to the system indicates the dimension of either reachable or controllable sets, i.e, $\text{int}\left(\mathcal{R}^t(\Omega_t)\right) \neq \emptyset$ or $\text{int}\left(\mathcal{C}^t(\Omega_t)\right) \neq \emptyset$. Furthermore, the system is reversible if $\Omega_t \in \tau(\Omega_t)$ [27].

Up to this point, only control signals have been considered as those that determine the dynamical control system evolution. However, it is well know that a control system is susceptible to disturbances. Disturbances can be seen as unmanipulated system inputs and included to determine dynamical control system evolution as in the equation (2.43).

$$\sum : \dot{x}(t) = f(x(t), u(t), d(t)) \tag{2.43}$$

Where $d(t) \in D$ is the vector of unmanipulated system inputs.

Kerrigan in his Doctoral Thesis [55] defined the robust reachable and controllable sets version. In these robust version, disturbances are included. The disturbances inclusion is an issue not considered in the framework of controllability verification through Lie brackets. Robust reachable and controllable sets reflect the *"real"* system space-state. Therefore, it is possible to verify the *robust system controllability* via the set theory in control.

Next, robust reachable and controllable sets definitions are given.

Definition 2.28. Robust reachable set $\tilde{\mathcal{R}}^t(\Omega_o)$ in time t: Given set Ω_o, the *robust reachable set* $\tilde{\mathcal{R}}^t(\Omega_o)$ *in time* t is the set of states $x \in X$ for which exists admissible control inputs $u \in U$ and bounded system disturbances $d \in D$ such that the system evolves to Ω_t from Ω_o, with $t < \infty$. Formal definition is given by the equation (2.44).

$$\tilde{\mathcal{R}}^t(\Omega_o) = \{x \in X | \exists x_o \in \Omega_o, u \in U, d \in D : x_t \in \Omega_t\} \tag{2.44}$$

Definition 2.29. Robust controllable set $\tilde{\mathcal{C}}^t(\Omega_o)$ in time t: Given set Ω_o, the *robust controllable set* $\tilde{\mathcal{C}}^t(\Omega_o)$ *in time* t is set of states $x \in X$ for which exists admissible control inputs $u \in U$ and bounded system disturbances $d \in D$ such that the system evolves from Ω_t to Ω_o, with $t < \infty$. Formal definition is given by the equation (2.45).

$$\tilde{\mathcal{C}}^t(\Omega_o) = \{x \in X | \exists x \in \Omega_t, u \in U, d \in D : x(0) \in \Omega_0\} \tag{2.45}$$

The robust reversible set $\tilde{\tau}^t$ from Ω_t to Ω_t in time t can be defines based on definitions (2.28) and (2.29), as follow:

Definition 2.30. Robust reversible set $\tilde{\tau}^t(\Omega_t)$ in time t: Given set Ω_t, the *robust reversible set* $\tilde{\tau}(\Omega_t)$ *from* Ω_t *to* Ω_t *in time* t is the set of states $x \in X$ for which exists admissible control inputs $u \in U$ and bounded system disturbances $d \in D$ such that the system evolves from Ω_t to Ω_t. Formal definition is given by the equation (2.46).

$$\tilde{\tau}^t(\Omega_t) = \left\{ x \in X | x \in \tilde{\mathcal{R}}^t(\Omega_t) \wedge x \in \tilde{\mathcal{C}}^t(\Omega_t) \right\} \tag{2.46}$$

or equivalent by the equation (2.47).

$$\tilde{\tau}^t(\Omega_t) = \tilde{\mathcal{R}}^t(\Omega_t) \bigcap \tilde{\mathcal{C}}^t(\Omega_\tau) \tag{2.47}$$

To analyze the robust state controllability via set theory, it is enough that $\text{int}(\tilde{\tau}_t(\Omega_t)) \neq \emptyset$.

It is important to remark that in the nonlinear systems case, only local controllability is verified via Lie algebra as well as via set theory in control. The controllability verification via Lie algebra theory requires the computation of Lie brackets to evaluate the rank accessibility condition for an input-affine system, where accessibility is a weakly property than controllability. The controllability verification via Set theory in control requires the computation of reachable, controllable, and reversible sets, where system controllability is guaranteed if either $\text{int}(\tau_t(\Omega_t)) \neq \emptyset$ or $\text{int}(\tilde{\tau}_t(\Omega_t)) \neq \emptyset$. Furthermore, the system need not be input-affine and disturbances can be included.

Gómez in her Doctoral Thesis [44] presented an Monte Carlo based algorithm to compute an approximation of both reachable and controllable sets. This algorithm was extended by Alzate in his Master Thesis [30] for robust reachable and controllable sets case. Moreover, author by [30] presented an Controllability Index (CI) for not only verify but also quantify the system controllability. The Monte Carlo based algorithm and CI presented by [30] are presented.

Algorithm (1) can be employed to compute an approximation of $\mathcal{R}^t$, $\mathcal{C}^t$, and τ^t as well as $\tilde{\mathcal{R}}^t(\Omega_t)$, $\tilde{\mathcal{C}}^t(\Omega_t)$, and $\tilde{\tau}^t(\Omega_t)$ to test local system controllability. Algorithm (1) is based on randomized algorithms. Randomized algorithms have proved to be a good solution to transform intractable control problems into polynomial complexity problems dependent on system complexity and computer equipment [56].

Once reachable, controllable, and reversible sets have been computed, it is possible to extract valuable information from these sets. For example, it is possible to compute the size of these sets and to determine their form. The sets size can be useful to quantify the system controllability about systems operating point as in the work presented by [30].

A Controllability Index (CI) is needed to quantify the system controllability. Alzate in his Master Thesis [30] summarizes controllability indexes available in the literature and their limitations. Alzate also recall that these controllability indexes are not based

Algorithm 1: Controllability verification algorithm

Input: $x_o, f, t, x_{min}, x_{max}, u_{min}, u_{max}, d_{min}, d_{max}, \epsilon, \delta$

Output: $\mathcal{R}^t(\Omega_t)$, $\mathcal{C}^t(\Omega_t)$, and $\tau^t(\Omega_t)$ or $\tilde{\mathcal{R}}^t(\Omega_t)$, $\tilde{\mathcal{C}}^t(\Omega_t)$, and $\tilde{\tau}(\Omega_t)$

1 Given an operating point x_0, significance (δ), maximum permissible error ϵ, constraints for X, and a set of constraints for both U and D.

2 To Determine the sample size using the Chernoff bound given by the equation (2.48):

$$N > \frac{1}{2\epsilon^2} log \frac{2}{\delta} \tag{2.48}$$

3 To obtain N samples for $u_i \sim Uniform(U)$ and $d_i \sim Uniform(D)$, for $i = 1, 2, \ldots, N$.

4 **if** $d_{min} = d_{max}$ **then**

5 Reachable set $\mathcal{R}^t(\Omega_t)$ in time t is the system solution $\dot{x}(t) = f(x, u)$ for each $u_i(t) \in U$ with $t = \sigma - \tau$. Controllable set $\mathcal{C}^t(\Omega_t)$ in time t is the system solution $\dot{x}(t) = -f(x, u)$ for each $u_i(t) \in U$ with $t = \sigma - \tau$.

6 Reversible set $\tau^t(\Omega_t)$ in time t is the intersection between $\mathcal{R}^t(\Omega_t)$ and $\mathcal{C}^t(\Omega_t)$.

7 **else**

8 Robust reachable set $\tilde{\mathcal{R}}^t(\Omega_t)$ in time t is the system solution $\dot{x} = f(x, u_i, d_i)$ for each u_i, d_i with $t = \sigma - \tau$. Robust controllable set $\tilde{\mathcal{C}}^t(\Omega_t)$ i time t is the system solution $\dot{x} = -f(x, u_i, d_i)$ for each u_i, d_i with $t = \sigma - \tau$.

9 Robust reversible set $\tilde{\tau}^t(\Omega_t)$ in time t is the intersection between $\tilde{R}_\tau(\Omega_0)$ and $\tilde{C}_0(\Omega_\tau)$, i.e., $\tilde{\tau}(\Omega_t) = \tilde{R}_\tau(\Omega_0) \cap \tilde{C}_0(\Omega_\tau)$.

10 **end**

in the set theory control. Furthermore, he emphasizes that a CI must be incorporate the system dynamical nature and restrictions of states and inputs. Based in these facts, Alzate proposes the CI given by the equation (2.49).

$$CI = \frac{\eta_{\tilde{\tau}^t(\Omega_t)}}{\eta_{\tilde{\mathcal{R}}^t(\Omega_t)}} \tag{2.49}$$

where $\eta_{\tilde{\tau}^t(\Omega_t)}$ and $\eta_{\tilde{\mathcal{R}}^t(\Omega_t)}$ are reversible and reachable sets hypervolumes, respectively.

Definition 2.31. Hypervolume of Ω_o, $\eta_{T_t}(\Omega_o)$ [30]: The *hypervolume of* $\Omega_o \in R^n$ is the integral of the subset hypervolume $T_t(\Omega_o) \subseteq \Omega_o$, i.e.,

$$\eta_{T_t(\Omega_o)} = \int_{T_t(\Omega_0)} 1 dx \tag{2.50}$$

An approximation of $\eta_{T_t(\Omega_o)}$ can be obtained by a disjunct partition of the admissible sate-space X. Thereby, any state-space point only belongs to a partition. These partitions can be of an arbitrary size. However, it is suggested that X is partitioned in c partitions $\mathcal{B}_b$ in each label, where b is a vectorial index of dimension n that indicates the position of each X partition. In this way, c^n partitions of X will be created.

Once X is partitioned, a membership function $I_\Omega(b)$ is applied over the set $T_t(\Omega_o)$. $I_\Omega(b)$ is defined as follow:

Definition 2.32. Ω membership function in the partition b, $I_\Omega(b)$: *Ω membership function in the partition b, $I_\Omega(b)$*, is a function that is equal to 1 if exist at least a $x \in \mathcal{B}_b$ such that $x \in \Omega$. Where b is a vectorial index of dimension n that indicates the position of a X partition. With $b_a = 1, \ldots, b$ and $a = 1, \ldots, n$. Otherwise, $I_\Omega(b)$ is equal to zero.

$$I_\Omega(b) = \begin{cases} 1 & if x \in \mathcal{B}_b : x \in \Omega \\ 0 & otherwise. \end{cases} \tag{2.51}$$

Figure (2.4) shows an example of the $I_\Omega(b)$ evaluation for a set $T_t(\Omega)$ in each partition $\mathcal{B}_b$ of a discretized X.

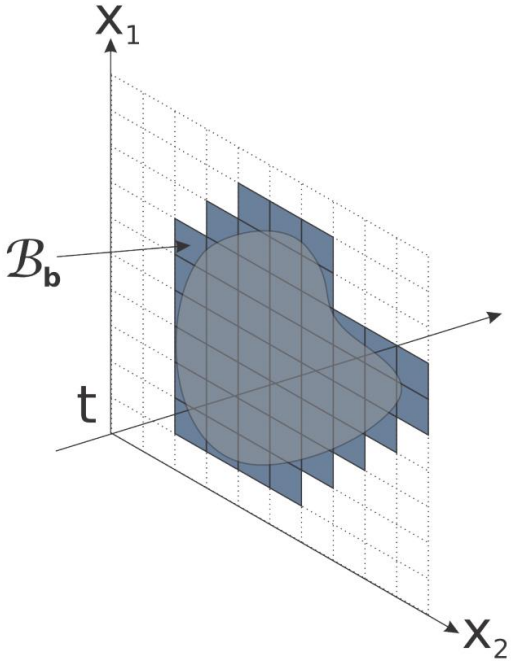

FIGURE 2.4: Admissible state-space discretization and $I_\Omega(b)$ membership function evaluation.

Then, an approximation of $\eta_{T_t(\Omega)}$ is given by the equation (2.52).

$$\eta_{T_t(\Omega_o)} \approx \sum_{b_1=1}^{b} \cdots \sum_{b_n=1}^{b} \{I_{T_i(\Omega_o)}\} \eta_{\mathcal{B}_b} \tag{2.52}$$

where

$$\eta_{\mathcal{B}_b} = \prod_{a=1}^{n} \left\{ \frac{\max(x_a) - \min(x_a)}{c} \right\} \tag{2.53}$$

The CI given by the equation (2.49) indicates the relation between sizes of $\tilde{\tau}^t(\Omega_t)$ and $\tilde{\mathcal{R}}^t(\Omega_t)$. CI quantifies the fraction of state-space which is possible reach and return to operating point x_o. CI can take values in the range $[0, 1]$. Where $CI = 0$ if $int(\tilde{\tau}^t(\Omega_t)) = \emptyset$ and $CI = 1$ if $\eta_{T_{\tilde{\tau}^t(\Omega_t)}} = \eta_{T_{\tilde{\mathcal{R}}^t(\Omega_t)}}$, i.e., if the sizes of $\tilde{\mathcal{R}}^t(\Omega_t)$ and $\tilde{\tau}^t(\Omega_t)$ are equal. Is is important to remark that $\max(CI) = 1$ due to the fact that $\tau^t(\Omega_t) \leq \mathcal{R}^t(\Omega_t)$ or $\tilde{\tau}^t(\Omega_t) \leq \tilde{\mathcal{R}}^t(\Omega_t)$.

Figure (2.5) is a graphic representation for CI cases. From Figure (2.5a) is seen that reachable and controllable sets are intersected, however $CI < 1$ because exist a state-space region that the system reaches, but can not to return to x_o with admissible control actions. In the other hand, from Figure (2.5b) is seen that reachable and controllable sets are superimposed, then $CI = 1$ because the system can go from any state in $\mathcal{R}^t(\Omega_o)$ and return to x_o with admissible control actions.

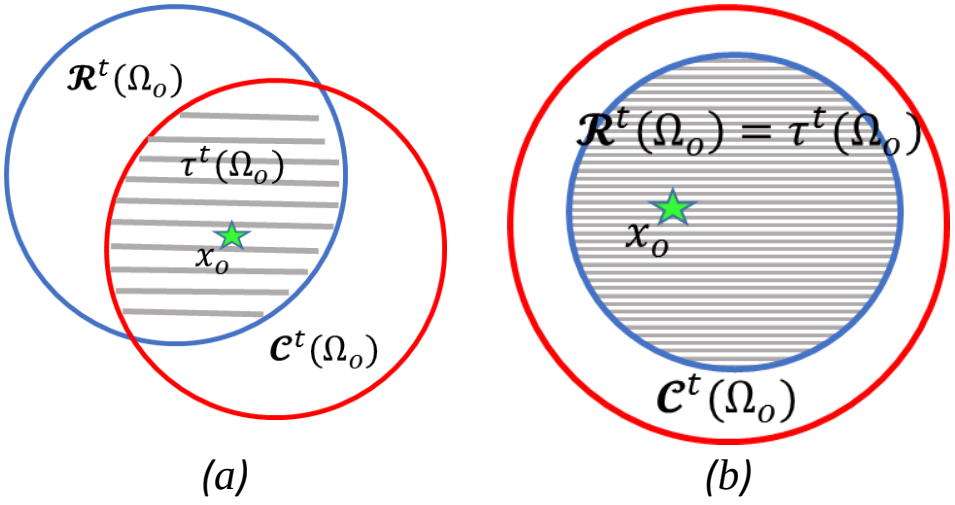

FIGURE 2.5: Different system controllability cases.

From results of system controllability obtained via set theory in control, it is possible to carry out stability system analysis and performance control evaluation [55], [29]. These analysis are out of scope of this work. However, it is important to highlight that any system stability region will be inside of $\tilde{\mathcal{R}}^t(\Omega_t)$. Moreover, this stability region can be known and included in controller restrictions as in the work presented by [55].

2.3 Control Issues

A PEC is a variable-structure system with fast nonlinear dynamics that are potentially subject to significant noise disturbances because of modulated control signals. Systems with these characteristics are a challenge from the control perspective and a large number of control structures have been explored [57].

PEC control specifications are quite diversified, e.g., a DC-DC converter operating in switch-mode power supply feeding a certain variable load may need duty ratio adjustments in order to assure a constant output voltage for the entire operating range (voltage regulation) [58]. In contrast, a grid-tie inverter fed by a renewable energy system must supply a desired AC current to the grid such that certain power transfer requirement is satisfied, thus the inverter behaves as current source [58]. On the other hand, Active Power Filters (APF) must provide the necessary current-voltage in order to cancel out undesired harmonic content produced by polluting loads, all by maintaining the grid-load power balance [59]. Generally speaking, PEC control structure is designed to impose low-frequency behavior of the system and to satisfy operating requirements [60].

The so-called standard control structures employ simple but robust invariant PI/PID controllers that are tuned taking into account PEC transfer functions. These controllers generate a continuous control signal (duty ratio), which needs a modulation strategy such as Pulse-Width Modulation (PWM) or carrier-based PWM as the case may be (DC-DC, DC-AC or AC-DC converter).

In the DC-DC converters case, Current-Mode Control (CMC) is a robust control scheme that has been successfully tested, widely accepted, and commonly implemented with conventional linear PI controllers [61]. Basically, it is a multiloop approach in cascade configuration. The inner loop senses either switch current or inductor current for feedback purposes, and uses a proportional-integral compensator to add damping and to provide protection against line and load disturbance. The outer loop senses output voltage and uses proportional-integral compensator to drive output voltage towards a desired setpoint value.

Other option in DC-DC converters case is the so-called voltage-mode control, which employs a single loop that senses output voltage for feedback. However, the main drawback of this control strategy is that in DC-DC converters with boost capabilities the duty-ratio-to-output-voltage transfer function can contain a Right Half Plane (RHP) zeros. These RHP zeros seriously limit the closed loop system performance [61].

In DC-AC or AC-DC converters, Voltage Oriented Control (VOC) is a robust control scheme that has been successfully tested, widely accepted, and commonly implemented

with conventional linear PI controllers [62], [63]. VOC is based on coordinate transformation between stationary *abc* and synchronous rotating $dq0$ reference frame. It guarantees fast transient response and high closed-loop performance. Due to the fact that the VOC uses internal current control loops, final closed-loop system performance is depended on applied current control techniques. The conventional VOC structure uses synchronous current control in rotating $dq0$ reference-frame. Thanks to the $dq0$ transformation the control values are DC quantities. As current controller, the PI controllers are used.

Another important issue in DC-AC or AC-DC converters is methods for extraction of inefficient and harmonic load currents and determination of converter reference currents. Indeed, accuracy and speed of the converter response are related to this point. The methods of reference current generation are categorized in two main fields: *(a)* time-domain and *(b)* frequency-domain methods. Time-domain methods such as $dq0$ transformation, $p-q$ transformation, symmetrical components transformation, etc., are based on the measurements and transformation of three-phase quantities. The main advantage of these time-domain reference generation methods is the fast response obtained. On the other side, frequency-domain methods such as Fourier transformation provide accurate individual and multiple harmonic load current detection, but it is not instantaneous reference generation methods. Furthermore, the closed-loop performance can be limited [64].

To conclude, whichever control structure is selected, PI controller is employed due to the fact that it is a simple but robust controller that can be tuned based on system transfer functions derived of system phenomenological-based mathematical model or derived of system empirical-based model.

A PID controller is composed of: *(a)* a proportional mode P that provides to the controller an output proportional to the error; *(b)* an integral mode I that produces a signal proportional to the integral of the error. The integration time T_i is the time that must elapse before the integral action reaches the magnitude of P. and *(c)* a derivative mode D. A controller takes a time before perceiving a change, the derivative action anticipates this change in the controlled variable. The frequency-domain control policy of an ideal PID controller is given by the equation (2.54).

$$C_{PID}(S) = K_p \left[1 + \frac{1}{T_i s} + T_d s\right] E(s) \tag{2.54}$$

Where K_p is proportional gain, T_i is integrating time, T_d is derivative time, and $E(s)$ is the error between measured output and its desired value.

There are different methods for tuning PID controllers, such as root locus techniques, loop-shaping methods or tuning rules [65]. However, regardless of the tuning method, the main interest is the trade-off between performance and robustness. Performance refers to how much faster controller response to a disturbance or setpoint change. On the other hand, robustness refers to how stable is the closed-loop system once that controller is designed and it is subjected to disturbances. Assuming that the closed-loop system has all its poles in RHP, stability refers to how much and which type of modeling uncertainties are supported by closed-loop system before it becomes unstable, i.e., its output increases or decreases indefinitely [66].

Based on this interpretation about robustness, a new concept appears: relative stability. Measures of the relative stability are known as robustness measures. Thereby, if a controller is designed such that any robustness measure is satisfied, this controller is a robust controller. A particular case is a PID robust controller.

Robustness measures are divided in two: *(a)* gain margin and phase margin, and *(b)* sensitivity function.

2.3.1 Gain Margin and Phase Margin

Assuming that the system transfer function is $G(s)$ and that PI controller transfer function is $C(s)$, thus direct-loop transfer function in the frequency-domain is $H(j\omega) = C(j\omega)G(j\omega)$. Margin gain A_m and phase gain ϕ_m are defined in equations (2.55) and (2.56), respectively.

$$A_m = \frac{1}{|C(j\omega_p)G(j\omega_p)|} \tag{2.55}$$

$$\phi_m = arg\,|C(j\omega_g)G(j\omega_g)| + \pi \tag{2.56}$$

Where ω_p and ω_g are given by equations (2.57) and (2.58), respectively.

$$|C(j\omega_p)G(j\omega_p)| = 1 \tag{2.57}$$

$$arg\,|C(j\omega_g)G(j\omega_g)| = -\pi \tag{2.58}$$

A_m as robustness measure indicates that if any error was carried out during modeling process and the system model is wrong, the system static gain can increase a factor A_m before the system become unstable. Typical values for the gain margin are $2 \leq A_m \geq 5$.

ϕ_m as robustness measure indicates that any error was carried out during modeling process and the systems model is wrong, the system delay can increase ϕ_m deg, at ω_g, before the system become unstable. Typical values for the phase margin are $30^o \leq \phi \geq 60^o$.

2.3.2 Sensitivity Function

The sensitivity function is given by the equation (2.59).

$$S(s) = \frac{1}{1 + C(s)G(s)} \tag{2.59}$$

The sensitivity function is the basis to establish the robustness measure in PID controllers design process. System uncertainty can be cumulative, this means that to nominal system model $G_o(s)$ is added an uncertainty model $\Delta G(s)$, such that the system model is $G(s) = G_o(s) + \Delta G(s)$. $S(s)$ is directly affected by $\Delta G(s)$. Therefore, the controller must be designed such that $S(s)$ has a small magnitude within frequencies range where $\Delta G(s)$ has some impact.

From $S(s)$, the robustness index M_s given by the equation (2.60) is derived.

$$M_s = \max_{\omega} |S(j\omega)| = \frac{1}{\min_{\omega} |1 + C(j\omega)G(j\omega)|} \tag{2.60}$$

Typical values for M_s are $1.4 \leq M_s \geq 2$.

It is possible proof that a value of M_s can assure, simultaneously, boundaries for A_m and ϕ_m given by equations (2.61) and (2.62), respectively. Thus, M_s is more general robustness measure.

$$A_m = \frac{M_s}{M_s - 1} \tag{2.61}$$

$$\phi_m = 2 \arcsin\left(\frac{1}{M_s}\right) \tag{2.62}$$

Where $M_s = 2$ corresponds to $A_m \geq 2$ and $\phi_m \geq 29^o$, and $M_s = 1,4$ corresponds to $A_m \geq 3.5$ and $\phi_m \geq 41^o$.

Chapter 3

Design Procedure of Power Electronic Converters

In this chapter a PECs design procedure is proposed. The proposed design procedure is based on system knowledge and systems theory. The proposed design procedure is composed of 4 stages and 10 steps. The design procedure is presented in a sequential form, however, it is not strictly necessary to follow this sequence. Moreover, once the system model is obtained, any order to system design can be adopted. This proposed design procedure allows to obtain all PEC parameters and its control structure such that established operating requirements are satisfied. In this proposed design procedure, system controllability is tested based on set theory in control. The main achievement of this design procedure is to allow the PEC design taking into account its inherent dynamical nature and with verified controllability, but without fixing any control structure. The proposed procedure design employs linear as well as nonlinear tools to analyze the system. However, the control structure can be linear or nonlinear.

3.1 Proposed Design Procedure

The proposed design procedure is detailed in table 3.1.

TABLE 3.1: Proposed Design Procedure of Power Electronic Converters

Stage	Step*	Analysis tool	Required model	Result
Dynamical modeling	1. To Set both system structure and desired operating requirements.	Knowledge of the problem to be solved.		The system structure and a set of operating requirements.
	2. To apply conservative laws to the system.	Kirchhoff's circuit laws.		A set of nonlinear coupled differential equations.
	3. To obtain a suitable structure for the system phenomenological-based model.	Systems theory.	Phenomenological-based model.	Switched model in its general or bilinear form.
	4. To apply the average operator.	Fourier transform.	Switched model.	Continuous-time averaged model.
	5. To apply the Taylor series expansion.	Taylor series theory.	Continuous-time averaged model.	Small-signal model or linearized state-space model.
	6. To apply a state-space to transfer functions realization.	Systems theory.	Small-signal model or linearized state-space model.	System transfer functions (frequency-domain model).
Passive elements design	7. To apply inductor volt-second and capacitor charge balance principles.	Energy conservation law.	Continuous-time averaged model.	Steady-state model.
	8. To apply circuital laws.	Energy conservation law and Ohm's law.	Steady-state model.	Expressions for efficiency, power electronic converter operation mode, and passive elements boundaries.
Design controllability verification	9. To apply state controllability analysis based on set theory in control.	Set theory in control.	Continuous-time averaged model.	Reachable, controllable, and reversible sets.
Control structure design	10. To apply control theory.	Control theory.	Whichever switched model, averaged model and/or small-signal model.	A control structure that guarantee system operating requirements.

* Several steps can contain several sub-steps. However, additional sub-steps are according to the application case.

3.2 Observations About The Proposed Design Procedure

Concerning to the system structure, DC-DC, DC-AC, and AC-DC are some structures for the system. All of these structures have different objectives and they are selected according to the need. Currents and voltages waveforms, currents and voltages THD, power factor, power quality, harmonic cancellation, efficiency, operation mode, among others, are typical system desired operating requirements.

Concerning to the passive elements design, there is not a consensus regarding to the design method. However, the main interest in this stage is to find expressions for system efficiency and power electronic converter operation mode such that passive elements boundaries are derived from these expressions. Efficiency analysis states how well energy is used to measure the ratio between power input and power output. When a converter is implemented to use current-unidirectional and/or voltage-unidirectional switches, one or more new modes of operation known as Discontinuous Conduction Modes (DCM) can occur. DCM is commonly observed in DC-DC converters and rectifiers (AC/DC converters). DCM can also occur in inverters or in other converters containing two-quadrant switches. The key to design power electronic converters keeping both electric requirements and dynamical performance is to select suitable values for inductors and capacitors such that constraints like maximum physical admissible currents and voltages, converter efficiency, and Continuous Conduction Mode (CCM) are satisfied.

Concerning to the design controllability-oriented verification method, set theory in control is adopted due to the fact that controllability verification throughout this method not only allows to verify this system property, but also to quantify it. Moreover, controllability verification method based on set theory in control is equivalent with state-controllability verification method based on differential geometry. Results from controllability analysis via set theory in control can be used to system re-design such that system controllability is maximized.

Concerning to the control structure design, control paradigm and associated design methods chosen to solve PECs control problem depend on complex factors that include converter role, desired closed-loop dynamics, operating range, safety issues, control input limitations and so on. In the relevant literature, a wide plethora of control structures that have been employed to solve PEC control problem can be found. Linear as well as nonlinear control structures, each of them with their advantages and limitations.

Furthermore, the controller design task can differ in each case and a particular structure o method is not proposed here.

Chapter 4

Illustrative example: Boost DC-DC converter

In this chapter, design procedure presented in chapter 3 is applied to a Boost DC-DC converter in order to show its applicability. System requirements are established. Both large- and small-signal models are developed for the Boost DC-DC converter. Large-signal models are obtained in general and bilinear form. Small-signal models are obtained in time and frequency domains in order to have a ready-to-use model for control purposes. Passive elements boundaries are established based on system knowledge, then some simulations are carried out to evaluate their impact in the dynamical system performance. The design controllability-oriented verification method is applied to designed Boost DC-DC converter and it is concluded that the designed converter is 92.41% locally controllable about its operating point. Finally, a Current-Mode Control (CMC) structure is designed for the Boost DC-DC converter and it is implemented in PSIM. A satisfactory closed-loop dynamical system performance is obtained.

4.1 Introduction

Technological developments in the power electronics field have increased the use of DC-DC converters in a large variety of applications, from the simplest ones (power supply for mobile phones or laptops [67]) to more demanding ones (applications in the aeronautics field [68], [69], automobiles industry [70], [71], [72], telecommunications [73], [74], renewable energy field [75], [76]). DC-DC converters are used to provide the power supply for electronic circuits such as microcontrollers. Therefore their main role is to adjust voltage level, providing a regulated output voltage based on a supply voltage that can

vary. For these reasons, DC-DC converters represent an interesting and active research domain [77].

A Boost DC-DC converter, operating in Continuous Conduction Mode (CCM) [78], is considered in this chapter since is one of the basic DC-DC converter topology.

Design procedure presented in chapter 3 is applied to a Boost DC-DC converter in order to show its applicability.

4.2 Dynamical Modelling

The firs stage in proposed design procedure of PECs is dynamical modeling. This stage is composed by steps 1 - 6 divided in three subsections. Where, system operating requirements are established and both large- and small-signal models are derived. The stage aim is to obtain both design- and control-oriented models. This section is composed of following subsections: *(1)* system operating requirements, *(2)* large-signal models, and *(3)* small-signal models.

4.2.1 System Operating Requirements

The first step in proposed design procedure of PEC is establishment of the system operating requirements. In PECs, the typical requirements are: input voltage range, output voltage range, output power range, output current range, operating frequency, output ripple and efficiency. Unless otherwise noted, continuous operating mode is assumed.

The set of operating requirements are specified in table 4.1.

Steps 2-6 in the proposed design procedure are concerning to develop a system mathematical dynamical model. For Boost DC-DC converter system showed in Figure (4.1), two types of mathematical models are derived in order to represent both high frequency (large-signal models) and low-frequency (small-signal models) behaviors.

4.2.2 Large-Signal Models

The Boost DC-DC converter operating in CCM can take two configurations as showed in Figure (4.1): configurations (a) and (b) correspond to switch H being turned on $h_1 = 1$ and turned off $h_2 = 1$, respectively. Therefore, switching function u can be defined as follow: $u = h_1 = 1 - h_2$.

TABLE 4.1: Boost DC-DC converter operating requirements

Requirement	**Values**		
	Min	**Typ**	**Max**
Input voltage range	30V	35V	40V
Output voltage range	50V	70V	95V
Output power range	0W	100W	300W
Output current range	0A	2A	8A (At 50V)
Operating frequency		100kHz	
Output current ripple	1%	5%	10%
Output voltage ripple	0.1%	0.5%	1%
Steady-State efficiency	90%	95%	98%
Load	25Ω	50Ω	100Ω

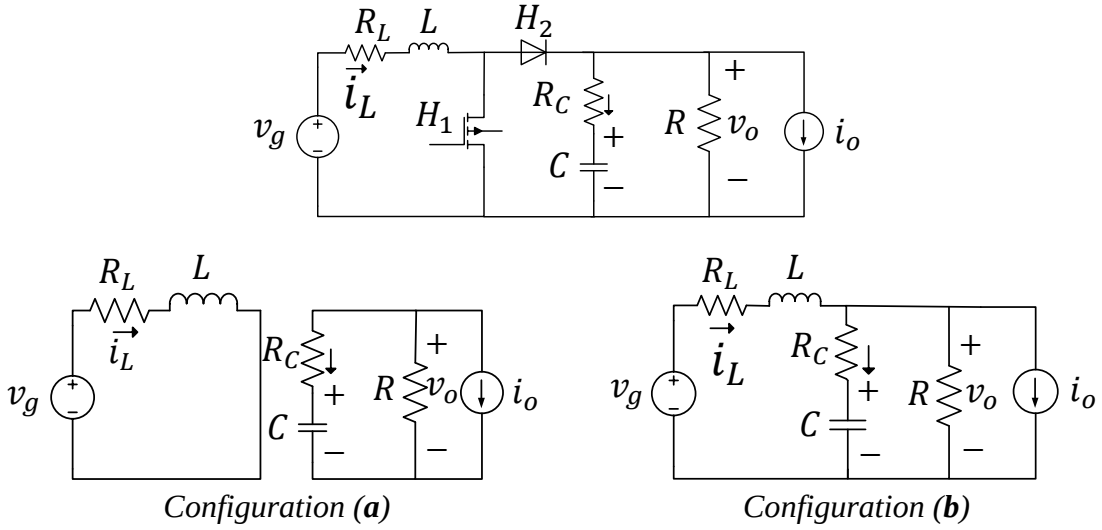

FIGURE 4.1: Nonideal DC-DC Boost converter circuital diagram

State variables (inductor current i_L and capacitor voltage v_c) are defined to represent energy variation of the system. The complete set of equations for the two configurations showed in Figure (4.1) are given by equations (4.1)-(4.5). The system inputs are switching function u, DC input voltage source v_g, and current source i_o; while the system output is the output voltage v_o.

Configuration (a):

$$v_L = L\frac{di_L}{dt} = v_g - R_L i_L \tag{4.1}$$

$$i_C = C\frac{dv_C}{dt} = \left(\frac{1}{1+\alpha_C}\right)\left(-\frac{v_C}{R} - i_o\right) \tag{4.2}$$

where

$$\alpha_C = \frac{R_C}{R}$$

Configuration (b):

$$v_L = L\frac{di_L}{dt} = v_g - R_L i_L - R_C i_C - v_C \tag{4.3}$$

$$v_L = L\frac{di_L}{dt} = v_g - R_L i_L - \phi_C\left(-\frac{v_C}{R} - i_o + i_L\right) \tag{4.4}$$

$$i_C = C\frac{dv_C}{dt} = \left(\frac{1}{1+\alpha_C}\right)\left(-\frac{v_C}{R} - i_o + i_L\right) \tag{4.5}$$

where

$$\phi_C = \frac{R_C}{1+\alpha_C}$$

It is possible to re-write the above set of equations (4.1)-(4.5) under the equivalent switching form given by equations (4.6)-(4.7). Equations (4.6)-(4.7) represent the Boost DC-DC converter switching form.

$$L\frac{di_L}{dt} = (v_g - R_L i_L)\, h_1 + \left(v_g - R_L i_L - \phi_c\left(-\frac{v_c}{R} - i_o + i_L\right)\right) h_2 \tag{4.6}$$

$$C\frac{dv_c}{dt} = \left[\left(\frac{1}{1+\alpha_c}\right)\left(-\frac{v_c}{R} - i_o\right)\right] h_1 + \left[\left(\frac{1}{1+\alpha_c}\right)\left(-\frac{v_c}{R} - i_o - i_L\right)\right] h_2 \tag{4.7}$$

The Boost DC-DC converter bilinear form is given by the equation (4.8).

$$\begin{bmatrix} \dot{i}_L \\ \dot{v}_C \end{bmatrix} = \begin{bmatrix} -\dfrac{R_L - \phi_C}{L} & \dfrac{\phi_C}{RL} \\ \dfrac{1}{C}\left(\dfrac{1}{1+\alpha_C}\right) & -\dfrac{1}{R_C}\left(\dfrac{1}{1+\alpha_C}\right) \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} \dfrac{\phi_C}{L} & -\dfrac{\phi_C}{RL} \\ -\dfrac{1}{C}\left(\dfrac{1}{1+\alpha_C}\right) & 0 \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} -\phi_C i_o \\ 0 \end{bmatrix} u + \begin{bmatrix} v_g + \phi_C i_o \\ -\left(\dfrac{1}{1+\alpha_c}\right) i_o \end{bmatrix} \tag{4.8}$$

The Boost DC-DC converter average model is given by the equation (4.9).

$$\begin{bmatrix} \dot{\langle i_L \rangle}_o \\ \dot{\langle v_C \rangle}_0 \end{bmatrix} = \begin{bmatrix} -\dfrac{R_L - \phi_C}{L} & \dfrac{\phi_C}{RL} \\ \dfrac{1}{C}\left(\dfrac{1}{1+\alpha_C}\right) & -\dfrac{1}{RC}\left(\dfrac{1}{1+\alpha_C}\right) \end{bmatrix} \begin{bmatrix} \langle i_L \rangle_o \\ \langle v_C \rangle_o \end{bmatrix} + \begin{bmatrix} \dfrac{\phi_C}{L} & -\dfrac{\phi_C}{RL} \\ -\dfrac{1}{C}\left(\dfrac{1}{1+\alpha_C}\right) & 0 \end{bmatrix} \begin{bmatrix} \langle i_L \rangle_o \\ \langle v_C \rangle_o \end{bmatrix} + \begin{bmatrix} -\phi_C i_o \\ 0 \end{bmatrix} d + \begin{bmatrix} v_g + \phi_C i_o \\ -\left(\dfrac{1}{1+\alpha_C}\right) i_o \end{bmatrix} \tag{4.9}$$

Where $d = \langle u \rangle_0$ is the duty radio of the Boost DC-DC converter switching function u.

4.2.3 Small-Signal Models

Small-signal model derivation is carried out from large-signal Boost DC-DC converter model given by equations (4.11)-(4.12).

$$L\frac{di_L}{dt} = v_g - v_o(1-d) - R_L i_L \tag{4.10}$$

$$C\frac{dv_C}{dt} = i_L(1-d) - \frac{v_o}{R} \tag{4.11}$$

$$v_o = CR_C\frac{v_C}{dt} + v_C \tag{4.12}$$

Steady-state model is given by equations in (4.13). Capital letters indicate the steady-state average values, thus: V_g is the input voltage, V_o is the output voltage, I_L is the inductor current, and D is the duty cycle.

$$\begin{aligned} V_g - V_o(1-D) - R_L I_L &= 0 \\ I_L(1-D) - \frac{V_o}{R} &= 0 \\ V_o &= V_C \end{aligned} \tag{4.13}$$

Equations (4.11)-(4.12) are differentiated. Hence, the small-signal model is given by equations in (4.14). The variations in the system may be written around equilibrium point, where: $I_L = I_{Le} + \tilde{i_L}$, $V_C = V_{Ce} + \tilde{v_C}$, $V_g = V_{g_e} + \tilde{v_g}$, $D = D_e + \tilde{d}$, and $R = R_e + \tilde{R}$. Subscript e indicates the variables rated values.

$$\begin{aligned} L\dot{\tilde{i_L}} &= V_{g_e} + \tilde{v_g} - R_L\left(I_{L_e} + \tilde{i_L}\right) - \left(V_{C_e} - \tilde{v_C}\right)\left(1 - D_e - \tilde{d}\right) \\ C\dot{\tilde{v_C}} &= -\frac{\left(V_{C_e} + \tilde{v_C}\right)}{\left(R_e + \tilde{R}\right)} + \left(I_{L_e} + \tilde{i_L}\right)\left(1 + D_e - \tilde{d}\right) \\ V_{o_e} + \tilde{v_o} &= CR_C\dot{\tilde{v_C}} + V_{C_e} + \tilde{v_C} \end{aligned} \tag{4.14}$$

Where "$\tilde{\ }$" denotes the small variations around equilibrium point.

Replacing equations in (4.13) into equations in (4.14) and neglecting small variations, the Small-Signal model can be rewritten as equations in (4.15).

$$\begin{aligned} L\dot{\tilde{i_L}} &= \tilde{v_g} + V_{C_e}\tilde{d} - \tilde{v_C}(1-D_e) - R_L\tilde{i_L} \\ C\dot{\tilde{v_C}} &= -I_{L_e}\tilde{d} + \tilde{i_L}(1-D_e) - \frac{\tilde{v_C}}{R_e} - \tilde{i_s} \\ \tilde{v_o} &= CR_C\dot{\tilde{v_C}} + \tilde{v_C} \end{aligned} \tag{4.15}$$

Where the current load variations have been denoted by $\tilde{i}_s = -\dfrac{V_{Ce}\tilde{R}}{R_e^2}$.

Associated equivalent circuit diagram to (4.15) is given in Figure (4.2).

Figure (4.2) shows the influence in variations of all exogenous variables over system outputs. System outputs result from superposition of all inputs variables.

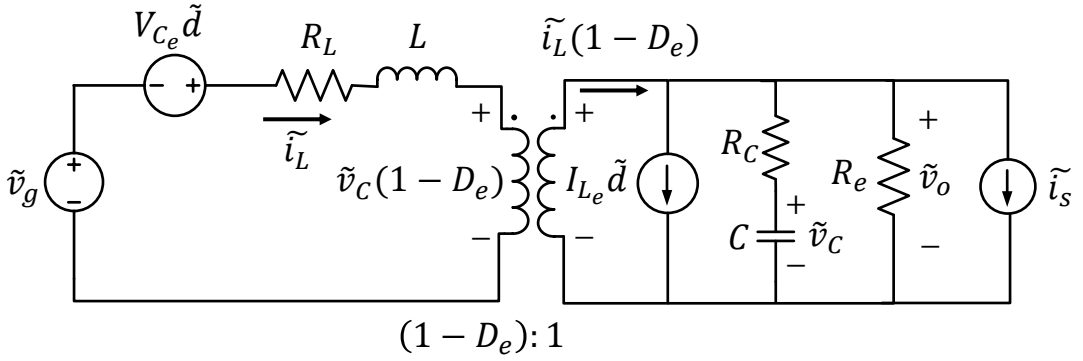

FIGURE 4.2: Small-signal model of the non-ideal Boost DC-DC circuit: equivalent diagram

The system inputs are: *(1)* duty ratio $\tilde{d}$, *(2)* DC voltage source $\tilde{v}_g$, and *(3)* current source $\tilde{i}_s$.

The system outputs are: *(1)* voltage $\tilde{v}_o$ and/or *(2)* inductor current $\tilde{i}_L$.

The output of the system is selected according to the control objective. In the Boost DC-DC converter case, commonly, the control objective is to regulate $\tilde{v}_o$ around a certain specified value.

The Boost DC-DC converter transfer functions are obtained based on equations (4.11)-(4.12) as follow: *(a)* replacing equation (4.12) into equation (4.11) and equation (4.12) to obtain the large-signal averaged model given by equations in (4.16), and *(b)* applying the state-space realization given by the equation (4.17). Two cases can occur: *(1)* output voltage v_o is selected as system output, then the small-signal averaged model is given by equations (4.19) and (4.20). *(2)* inductor current i_L is selected as system output, then, the small-signal averaged model is given by equations (4.19) and (4.21).

$$\begin{aligned} L\frac{di_L}{dt} &= v_g - (R_L + \phi_C(1-d))i_L + \left(\frac{\phi_C}{R} - 1\right)(1-d)v_C + \phi_C(1-d)i_o \\ C\frac{dv_C}{dt} &= \left(\frac{1}{1+\alpha_C}\right)\left((1-d)i_L - \frac{v_C}{R} - i_o\right) \end{aligned} \tag{4.16}$$

$$\begin{aligned} \dot{x} &= Ax + Bu \\ y &= Cx + Du \end{aligned} \tag{4.17}$$

where

$$\begin{aligned} A &= \left(\frac{\partial f\,(x,u)}{\partial x}\right)_{x_e,u_e} & B &= \left(\frac{\partial f\,(x,u)}{\partial u}\right)_{x_e,u_e} \\ C &= \left(\frac{\partial h\,(x,u)}{\partial x}\right)_{x_e,u_e} & D &= \left(\frac{\partial h\,(x,u)}{\partial u}\right)_{x_e,u_e} \end{aligned} \tag{4.18}$$

Subscript e of equations in (4.18) refers to both state variables and input variables in their rated values.

$$\begin{bmatrix} \dot{i_L} \\ \dot{v_C} \end{bmatrix} = \begin{bmatrix} -\dfrac{R_L+\phi_C}{L} & \dfrac{\left(\frac{\phi_C}{R}-1\right)(1-d)}{L} \\ \dfrac{(1-d)}{(1+\alpha_C)C} & -\dfrac{1}{RC(1+\alpha_C)} \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} \dfrac{\left(\phi_C I_L - V_C\left(\frac{\phi_C}{R}-1\right)-\phi_C I_o\right)}{L} & \dfrac{1}{L} & \dfrac{\phi_C(1-d)}{L} \\ -\dfrac{IL}{(1+\alpha_C)C} & 0 & -\dfrac{1}{(1+\alpha_C C)} \end{bmatrix} \begin{bmatrix} d \\ v_g \\ i_o \end{bmatrix} \tag{4.19}$$

With output voltage v_o as system output.

$$\begin{bmatrix} v_o \end{bmatrix} = \begin{bmatrix} \phi_C(1-D) & 1-\dfrac{\phi_C}{R} \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} -\phi_C I_L & 0 & -\phi_C \end{bmatrix} \begin{bmatrix} d \\ v_g \\ i_o \end{bmatrix} \tag{4.20}$$

With inductor current i_L as system output.

$$\begin{bmatrix} i_L \end{bmatrix} = \begin{bmatrix} 1 & 0 \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} d \\ v_g \\ i_o \end{bmatrix} \tag{4.21}$$

Equation (4.22) is the common realization that allows to relate the state-space model with the system transfer functions.

$$G(s) = \frac{1}{det(sI - A)} C\left[adj(sI - A)\right] B + D \tag{4.22}$$

Applying realization given by the equation (4.22) to equations in (4.19) and (4.20), transfer functions given by the equation (4.23) are obtained. Numerator of equation (4.23) has three components, one for each system input, i.e., d, v_g, and i_o, respectively.

$$G_{v_o}(s) = \frac{\begin{bmatrix} -(RLI_L s + \phi_C R I_o(1-D) + \phi_C(1-D)V_C - R(1-D)V_C + RR_L I_L) \\ (\phi_C C(1+\alpha_C)s + 1) \\ R(\phi_C C(1+\alpha_C)s + 1)(1-D) \\ R(\phi_C(1-D)^2 - \phi_C(1-D) - R_L)(\phi_C C(1+\alpha_C)s + 1) \end{bmatrix}}{\begin{bmatrix} (RLC(1+\alpha_C))s^2 + \phi_C RC(1-D)(1+\alpha_C)s - (\phi_C - R)(1-D)^2 \\ +\phi_C(1-D) + R_L \end{bmatrix}} \tag{4.23}$$

Applying realization given by the equation (4.22) to equations (4.19) and (4.21), transfer functions given by the equation (4.24) are obtained. Numerator has three components, one for each system input, i.e., d, v_g, and i_o, respectively.

$$G_{i_L}(s) = \frac{\begin{bmatrix} \left(\frac{1}{R}\right)(((\phi_C R^2 C I_L) - (\phi_C R^2 C I_o) - (\phi_C RCV_C) + (R^2 CV_C))(1+\alpha_C)s \\ -\phi_C R(1-D)I_L + R^2(1-D)I_L + \phi_C RI_L - \phi_C RI_o - (\phi_C - R)V_C) \\ RC(1+\alpha_C)s + 1 \\ \phi_C RC(1-D)(1+\alpha_C)s + R(1-D) \end{bmatrix}}{\begin{bmatrix} (RLC(1+\alpha_C))s^2 + \phi_C RC(1-D)(1+\alpha_C)s - (\phi_C - R)(1-D)^2 \\ +\phi_C(1-D) + R_L \end{bmatrix}} \tag{4.24}$$

Capital letters indicate the rated values of both states and inputs variables.

4.3 Passive elements design

The second stage in proposed design procedure of PECs is passive elements design, which is composed by steps 7 and 8. The aim of this stage is to find suitable values for passive

elements (inductor, capacitor, and resistors) such that system operating requirements are satisfied taking into account inherent dynamical system behavior. This section is composed of following subsections: *(1)* systems constraints, *(2)* passive elements selection, and *(3)* system frequency response verification.

4.3.1 System Constraints

Once the system model is obtained, following sub-steps are carried out to determine suitable passive elements (R, C, and L) boundaries which satisfy design requirements: *(1)* steady-state analysis, *(2)* current and voltage ripples analysis, *(3)* losses effect and efficiency analysis, *(4)* CCM analysis, and *(5)* zeros-based system dynamical analysis.

4.3.1.1 Steady-State Analysis

The first sub-step is the steady-state analysis. Steady-state analysis allows to obtain expressions for average rated values for both capacitor voltage v_C and inductor current i_L as a function of system inputs and parameters. The steady-state model is obtained by setting to zero model given by equations in (4.16). Thus, equations (4.25) and (4.26) are obtained.

$$I_L = \frac{V_C}{R\,(1-D)} \tag{4.25}$$

$$V_g = \left[\left(\frac{R_L + \phi_C\,(1-D)}{R\,(1-D)}\right) - \left(\frac{\phi_C}{R} - 1\right)(1-D)\right] V_o \tag{4.26}$$

Capital letters indicate the steady-state average values, thus: Vg is input voltage, Vo is output voltage, I_L is inductor current, and D is duty cycle.

Replacing equation (4.25) into equation (4.26), it is found that $V_o = V_C$. Therefore, the Equilibrium Conversion Ratio ($M(D)$) of the Boost DC-DC converter is given by the equation (4.27).

$$M(D) = \frac{V_o}{V_g} = \frac{(1-D)}{\left[1 - \frac{\phi_C}{R}\right](1-D)^2 + \frac{\phi_C}{R}(1-D) + \frac{R_L}{R}} \tag{4.27}$$

$M(D)$ indicates the Boost DC-DC converter elevation voltage factor in terms of D, R, R_L, and ϕ_C.

4.3.1.2 Currents and Voltages Ripple Analysis

The second sub-step is currents and voltages ripple analysis. The analysis is carried out to determine the constraint equations for a suitable choice of both L and C values.

Figure (4.3) shows typical inductor voltage V_L and i_L waveforms (linear-ripple approximation). Slope, with i_L increasing or decreasing, is deduced from the analysis of V_L at each subinterval of time taken into account. Typical values of current inductor ripple Δi_L lie under 10% of the full-load value of I_L [78]. i_L begins at initial value $i_L(0)$. During the first subinterval (DT_s), switch in position 1, i_L increases with the constant slope given by the equation (4.28). At time $t = DT_s$, the switch changes to position 2. i_L then decreases with the constant slope given by the equation (4.29). At time $t = T_s$, the switch changes back to position 1, and the process repeats (See Figure (4.1)).

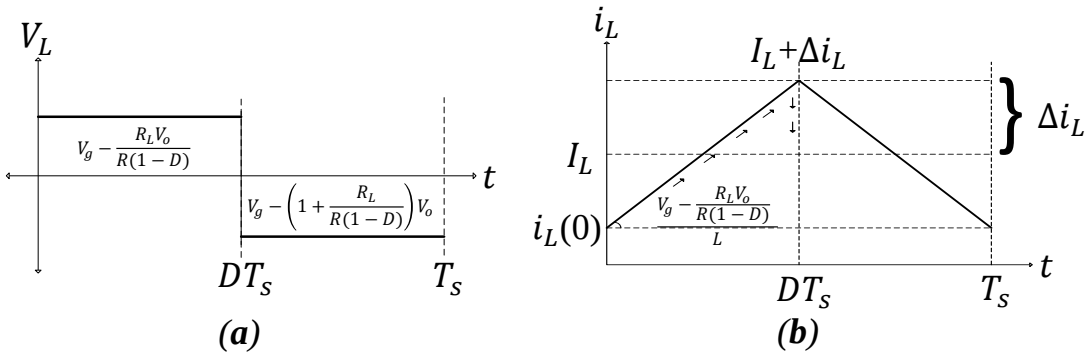

FIGURE 4.3: *a.* Typical inductor voltage waveform. *b.* Typical current inductor linear-ripple approximation.

$$L\frac{di_L}{dt} = V_g - \frac{R_L}{R\,(1-D)}V_o \tag{4.28}$$

$$L\frac{di_L}{dt} = V_g - \left(1 + \frac{R_L}{R\,(1-D)}\right)V_o \tag{4.29}$$

As illustrated in Figure (4.3b), the peak inductor current is equal to I_L plus the peak-to-average ripple Δi_L. This peak current flows through the inductor and the semiconductor devices that comprise the switch. The knowledge of the peak current is necessary when specifying the rating of the device.

The ripple magnitude can be calculated knowing both the slope of i_L and the length of the first subinterval (DT_s). The $i_L(t)$ waveform is symmetrical about I_L, hence, during DT_s, i_L increases by $2\Delta i_L$ (Since Δi_L is the peak ripple, the peak-to-peak ripple is

$2\Delta i_L$). Thus the change in current, $2\Delta i_L$, is equal to the slope (applied inductor voltage divided by L) times the length of DT_s (See equation (4.30)).

$$2\Delta i_L = \frac{V_g - \left(\frac{R_L}{R\,(1-D)}\right) V_o}{L} DT_s \tag{4.30}$$

Solution for Δi_L is given by (4.31).

$$\Delta i_L = \frac{V_g - \left(\frac{R_L}{R\,(1-D)}\right) V_o}{2L} DT_s \tag{4.31}$$

The inductor value can be chosen such that a desired Δi_L is attained. Solution of equation (4.31) for the inductance L is given by the equation (4.32).

$$L = \frac{V_g - \left(\frac{R_L}{R\,(1-D)}\right) V_o}{2\Delta i_L} DT_s \tag{4.32}$$

Likewise, capacitor voltage v_C waveform is depicted in Figure (4.4b) and an expression derived for the output voltage ripple peak magnitude Δv_C is obtained. Capacitor current waveform i_C is given in Figure (4.4a). Slope of the capacitor voltage waveform v_C, during DT_s, is given by the equation (4.33). The slope of the capacitor voltage waveform v_C, during the second subinterval $(1-D)T_s$, is given by the equation (4.34).

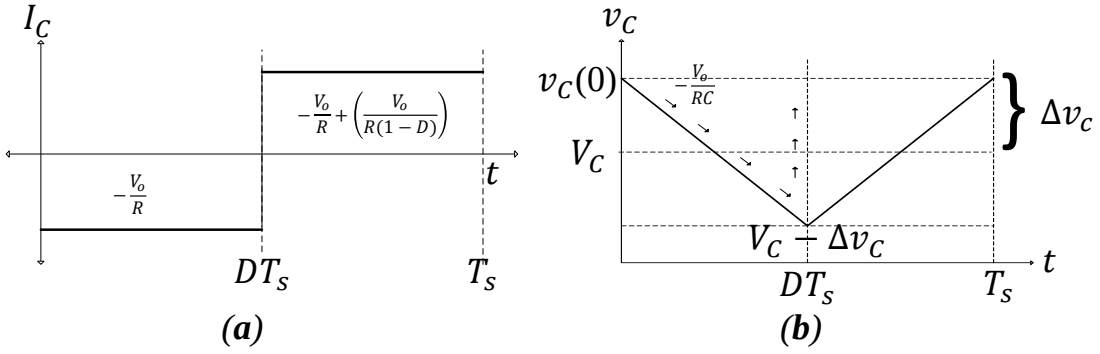

FIGURE 4.4: *a.* Typical capacitor current waveform. *b.* Typical capacitor voltage waveform.

$$C\frac{dv_C}{dt} = -\frac{V_o}{R} \tag{4.33}$$

$$C\frac{dv_C}{dt} = \left(\frac{1}{R\,(1-D)} - \frac{1}{R}\right) V_o \tag{4.34}$$

The change in v_C, $-2\Delta v_C$, during DT_s, is equal to the slope multiplied by DT_s (See equation (4.35)).

$$2\Delta v_C = \frac{\left(\frac{1}{1+\alpha_V}\right)\left(I_o - \frac{V_o}{R}\right)}{C} DT_s = \frac{v_o}{RC} DT_s \tag{4.35}$$

Solution for Δv_C is given by the equation (4.36).

$$\Delta v_C = \frac{\left(\frac{1}{1+\alpha_c}\right)\left(I_o - \frac{V_o}{R}\right)}{2C} DT_s = \frac{V_o}{2RC} DT_s \tag{4.36}$$

Equation (4.36) can be used to select capacitor value C to obtain a given Δv_C. Solution of equation (4.36) for the capacitor C is given by the equation (4.37).

$$C = \frac{\left(\frac{1}{1+\alpha_C}\right)\left(I_o - \frac{V_o}{R}\right)}{2\Delta v_C} DT_s = \frac{V_o}{2R\Delta v_C} DT_s \tag{4.37}$$

4.3.1.3 Losses Effect and Efficiency Analysis

The third sub-step is losses effect and efficiency analysis. The DC transformer is used to model ideal functions performed by a DC-DC converter. This model correctly represents the relations between DC voltages and currents of the converter. The model can be refined by including losses, such as semiconductor forward voltage drop and on-resistances, inductor core and copper losses, among others. The resulting model can be directly solved to find voltages, currents, losses and efficiency in the non-ideal Boost DC-DC converter.

Equations (4.38) and (4.39) are obtained setting to zero equation (4.16).

$$\langle v_L \rangle_o = V_g - \left(R_L - \phi_C\,(1-D)\right) I_L - \underbrace{\left[1 - \frac{\phi_C}{R}\right] V_C\,(1-D)}_{V_d} \tag{4.38}$$

$$\langle i_C \rangle_o = -\left(\frac{1}{1+\alpha_C}\right)\frac{V_C}{R} + \underbrace{\left(\frac{1}{1+\alpha_C}\right) I_L\,(1-D)}_{I_d} \tag{4.39}$$

where

$$\left[1 - \frac{\phi_C}{R}\right] = \left(\frac{1}{1+\alpha_C}\right)$$

The first task is to build a circuital model based on equations(4.38) and (4.39) which describes the DC behavior of the Boost DC-DC converter with inductor and capacitor losses. This is carried out by constructing a circuit of which Kirchoff loop and node equation are identical to equations (4.38) and (4.39).

Equation (4.38) describes the average inductor voltage during subintervals DT_s and $(1-D)T_s$. It also has the same form as a loop equation. Equation (4.38) describes the DC components of the voltages around a loop containing the inductor L, with loop current equal to the DC inductor current I_L.

Therefore a circuit containing a loop with current I_L, corresponding to equation (4.38), is built in Figure (4.5a). The first term in equation (4.38) is input voltage V_g. The second term is a voltage drop of value $R_L - \phi_C(1-D)I_L$, which is proportional to current I_L in the loop. The third term is a voltage $V_d = \left(\frac{1}{1+\alpha_C}\right) V_C(1-D)$, dependent on the converter output voltage due to the fact that in steady-state $V_C = V_o$.

Equation (4.39) sets that the sum of two DC currents is equal to $\langle i_C \rangle_o$. Equation (4.39) has the same form as a node equation. Equation (4.39) describes the DC components of currents flowing into a node connected to the capacitor C. The DC capacitor voltage is $V_C = V_o$ in steady-state.

Therefore a circuit containing a node connected to the capacitor is built in Figure (4.5b), of which the node equation satisfies equation (4.39). The first term in equation (4.39) is a current magnitude $\left(\frac{1}{1+\alpha_C}\right)\frac{V_o}{R}$, proportional to the DC capacitor voltage V_C in steady-state. The second term is a current $I_d = \left(\frac{1}{1+\alpha_C}\right) I_L(1-D)$, dependent on DC inductor current I_L. This term can be modeled using a dependent current source as shown in Figure (4.5b). The polarity of the source is chosen to satisfy equation (4.39).

The second task is to combine the circuits of Figures (4.5a) and (4.5b) into the circuit in Figure (4.6a). This circuit can be further simplified by acknowledging that dependent voltage and current sources constitute an ideal DC transformer. V_d depends on V_C. Likewise, I_d depends on I_L. In each case, the coefficient is $\left(\frac{1}{1+\alpha_C}\right)(1-D)$. Hence, the fact that the voltage source appears on the primary rather than the secondary side

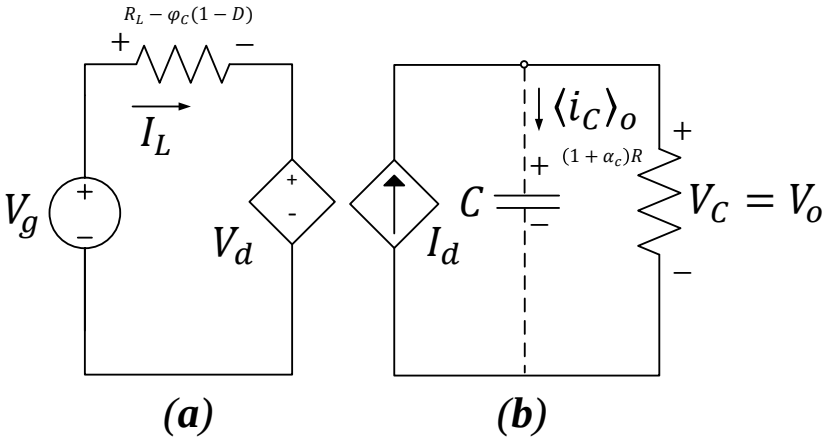

FIGURE 4.5: Sources depended equivalent circuit diagram of the Boost DC-DC Converter

is owing to the symmetry of the transformer. Therefore, there is an equivalent DC transformer, with turns ratio $\left(\frac{1}{1+\alpha_C}\right)(1-D) : 1$, that represents the non-ideal Boost DC-DC converter. Substitution of the ideal DC transformer model for the dependent sources yields the equivalent circuit of Figure (4.6b).

The main importance of the equivalent circuit model in Figure (4.6) is that it allows to compute converter efficiency η. Figure (4.6) predicts that the convert input power is given by the equation (4.40). The load current is equal to the current in the secondary of the ideal DC transformer I_d. Hence the model predicts that the converter output power is given by the equation (4.41).

$$P_{in} = V_g I_g = V_g \left(\frac{V_C}{\left(\frac{1}{1+\alpha_C}\right)\left(\frac{1}{1+\alpha_C}\right)(1-D)} \right) \tag{4.40}$$

$$P_{out} = V_o I_o = V_o \left(\frac{V_C}{\left(\frac{1}{1+\alpha_C}\right)\frac{1}{R}} \right) \tag{4.41}$$

Therefore, η is given by the equation (4.42).

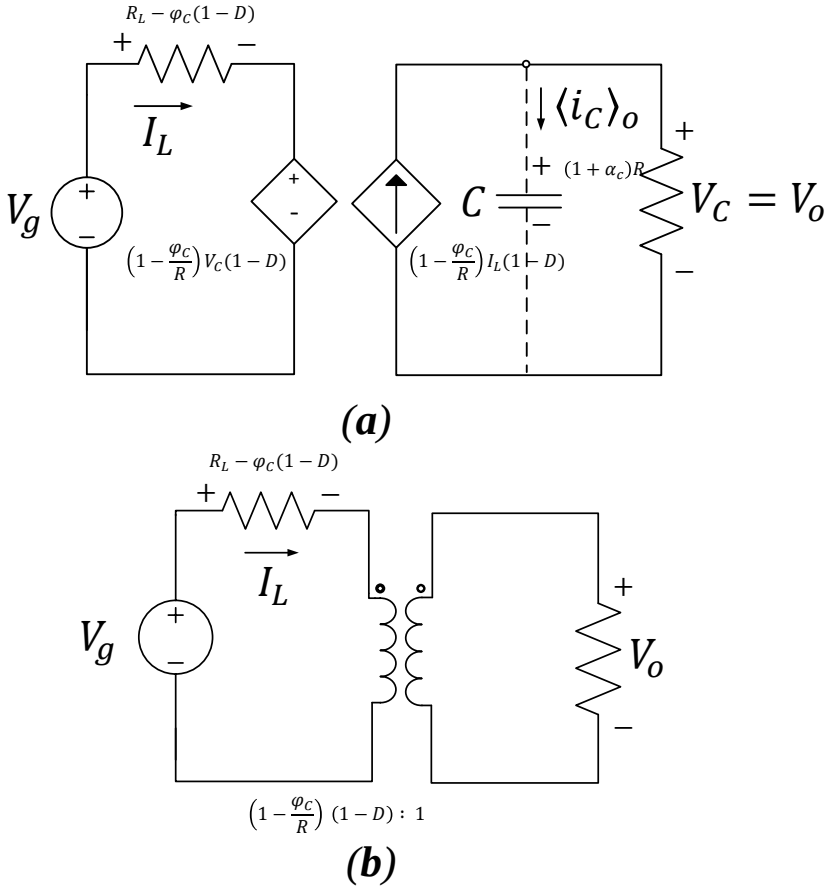

FIGURE 4.6: *a.* Sources depended equivalent circuit diagram of the Boost DC-DC Converter. *b.* Ideal DC transformer model of the Boost DC-DC converter.

$$\eta = \frac{P_{out}}{P_{in}} = M(D)\left(\frac{\dfrac{V_C}{\left(\dfrac{1}{1+\alpha_C}\right)\dfrac{1}{R}}}{V_C\left(\dfrac{1}{1+\alpha_C}\right)^2\dfrac{1}{R}(1-D)}\right) \tag{4.42}$$

Eliminating V_C, equation (4.42) is simplified and η is given by the equation (4.43).

$$\eta = \left(\frac{1}{1+\alpha_C}\right)(1-D)\,M(D) \tag{4.43}$$

Some plots of equations (4.27) and (4.43) are shown in Figure (4.7) for several values of $\alpha_C = \frac{R_C}{R}$ and $\alpha_L = \frac{R_L}{R}$ ratios in order to see how much losses affect both $M(D)$ and η.

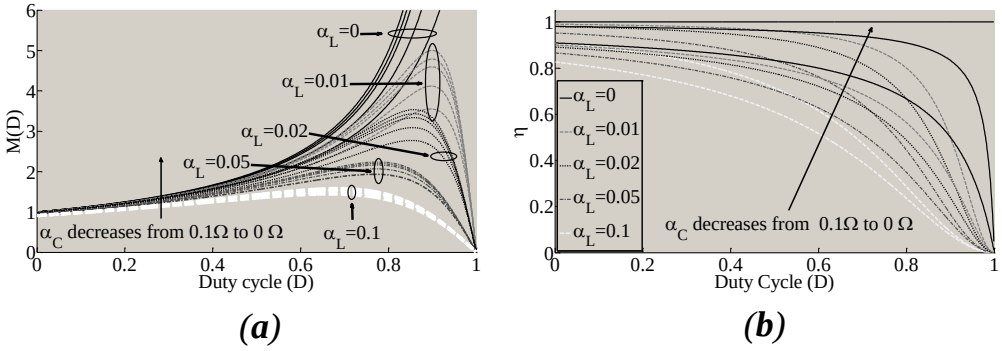

FIGURE 4.7: *(a)* the conversion ratio $M(D)$ v.s. the duty cycle D . *(b)* Efficiency η v.s. the duty cycle D

4.3.1.4 Continuous Conduction Mode (CCM) Analysis

The fourth sub-step is to assure that the PEC operates in CCM under any system condition. The CCM is suggested since Discontinuous Conduction Mode (DCM) causes larger voltage ripple [79], [80] and oscillations around the Maximum Power Point (MPP) [81]. Furthermore, the peak inductor current in DCM is higher than that in CCM with the same power level and current stress on the power switch is also higher [82].

By [78], the sufficient conditions for operation in the CCM and DCM are given by equations (4.44) and (4.45).

$$|I_L| > |\Delta i_L| \qquad for\ \ CCM \tag{4.44}$$

$$|I_L| < |\Delta i_L| \qquad for\ \ DCM \tag{4.45}$$

Where $|I_L|$ and $|\Delta i_L|$ are found assuming that the converter operates in CCM.

The DCM operation condition for the Boost DC-DC converter is given by the equation (4.46).

$$\frac{V_o}{R\,(1-D)} < \frac{R\,(1-D)\,V_g - V_o}{2LR(1-D)}DT_s \tag{4.46}$$

Simplifying equation (4.46) leads to equation (4.47).

$$D\left[\frac{(1-D)}{M\,(D)} - \frac{1}{R}\right] > \frac{2L}{RT_s} \tag{4.47}$$

Equation (4.47) can also be expressed as equation (4.48).

$$K\left(M\left(D\right),D\right) > K \tag{4.48}$$

where

$$K\left(M\left(D\right),D\right) = D\left[\frac{(1-D)}{M\left(D\right)} - \frac{1}{R}\right] \tag{4.49}$$

$$K = \frac{2L}{RT_s} \tag{4.50}$$

Dimensionless parameter K is a converter measure of the tendency to operate in the DCM [78]. Large values of K lead to CCM, while small values of K lead to the DCM for some values of (D). The critical value of K is the boundary between modes, $K_{crit}(M(D),D)$, and it is a function of D and R, R_C, R_L, i.e, load and equivalent resistances losses of passive elements C and L.

It is possible to prove that the function $K_{crit}(M(D),D)$ has a critical point given by the equation (4.51).

$$\begin{aligned} D &= \frac{1}{3}\left[\left(\alpha_L - \frac{1}{R}\right)\left(1+\frac{R_L}{R}\right) - 2\frac{R_C}{R} + 1\right] \\ &= \frac{1}{3}\left[-3\alpha_C + \alpha_C\alpha_L + \alpha_L\right] \end{aligned} \tag{4.51}$$

It is possible to prove that in critical point given by the equation (4.51), there is a maximum for the function, due to the fact that the second derivative of $K_{crit}(M(D),D)$ given by the equation (4.52) is always negative for $D \in [0,1]$.

$$\frac{d^2K\left(M\left(D\right),D\right)}{dD^2} = -\left(\frac{1}{1+\alpha_C}\right)(6D + 2\alpha_C) \tag{4.52}$$

From result given by equations (4.51) and (4.52), it is possible to set that the sufficient condition for always operate in CCM is given by the equation (4.53).

$$max\left(K\left(M\left(D\right),D\right)\right) < min\left(K\right) \tag{4.53}$$

where

$$min\,(K) = min\left(\frac{2L}{RT_s}\right)$$

Therefore, if a value for R was given in the system specifications, a condition for the maximum possible value of L is given by the equation (4.54) such that equation (4.53) is assured.

$$L > \frac{RT_s}{2} max(K(M(D), D)) \tag{4.54}$$

Some plots of equations (4.49) and (4.50), for several values of R and L, are shown in Figure (4.8). Figure (4.8) shows how variations of R and L affect both $K_{crit}(M(D), D)$ and K functions, and which are the critical values for R and L,

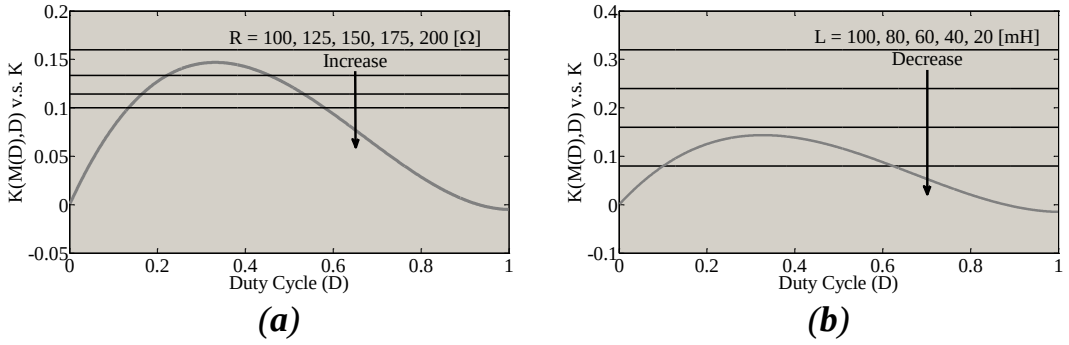

FIGURE 4.8: *(a)* $K(M(D), D)$ v.s. K varying R . *(b)* $K(M(D), D)$ v.s. K varying L

4.3.1.5 Zeros-Based Dynamical System Analysis

The fifth and last sub-step is to evaluate the PEC zeros location. Zeros location set some dynamical properties, such as overshoot or undershoot (non-minimum phase behavior), and damping.

The poles do not depend on either system inputs or outputs. However, the poles determine whether if system is stable or unstable, as well as its natural frequency. Moreover, every pole generates a natural mode in the system response. In contrast, system zeros are determined by the selected system inputs and outputs. Zeros location is related to the system performance limitations, additional overshoot in unit step response, and undershoot magnitude due to the system non-minimum phase behavior associated with Right Half Plane (RHP) zeros (unstable zeros)[83].

Due to the fact that zeros modify the system natural modes, PEC design procedure takes into account the zeros location such that the system dynamical properties such as both large currents and voltages overshoots, or both sharp currents or voltages undershoots are avoided. Large currents or voltage overshoots can cause converter failures. Otherwise, sharp currents or voltages undershoots are undesired behavior when classical control structures are employed due to tracking limitations with feedback systems [84], [85]. Accordingly, zeros location analysis objective is to find suitable values for R, C, and L such that RHP zeros are avoided or that their impact are minimized.

In Boost DC-DC converter applications, d is chosen as control input, while $\tilde{v}_g$ and $\tilde{i}_o$ are considered disturbances. Thus, d variations effect is of primary interest over system output. Then, the duty-ratio-to-voltage-output transfer function G_{vd} and the duty-ratio-to-inductor-current transfer function $G_{i_L d}$ are studied, i.e., characteristics of equations (4.23) and (4.24) are studied.

by the equation (4.23), zeros of G_{vd} are given by equations (4.55) and (4.56).

$$s_1 = -\frac{1}{R_C C} \tag{4.55}$$

$$s_2 = \frac{1}{L}\left[\frac{[(\phi_C - R)V_C - \phi_C R I_o]}{I_L R}(1-D) + R_L\right] \tag{4.56}$$

Zero given by the equation (4.55) is negative because it depends on circuit parameters, all of which are positive. However, zero given by the equation (4.56) is positive because it depends on circuit parameters, V_C, and I_L, all of which are positive. Also, in steady-state current source I_o is equal to zero. Zero given by the equation (4.56) is then placed in the RHP of Laplace domain, which mean that if $\tilde{v}_o$ is selected as system output, the system could have a non-minimum phase behavior.

Non-minimum phase behavior is a well-known result derived of the Boost DC-DC converter study [86]. To avoid this system behavior a cascade control structure has been proposed [86], [61]. With this control structure, the non-minimum phase behavior is avoided since both $G_{i_L d}$ and inductor-current-to-output-voltage $G_{v_o i_{L_{REF}}}$ transfer functions have a minimum phase behavior as will be shown.

by the equation (4.24), zero of the duty-ratio-to-inductor-current transfer function $G(s)_{i_L d}$ is given by the equation (4.57).

$$s = -\frac{1}{RC}\left(\frac{1}{1+\alpha_C}\right)\left[\frac{(R-\phi_C)RI_L(1-D)}{\phi_C R I_L - \phi_C R I_o + (R-\phi_C)V_C} + 1\right] \tag{4.57}$$

Zero given by the equation (4.57) is negative because it depends on circuit parameters, all of which are positive and, in steady-state, I_o is equal to zero. This zero is then placed in the Left Half Plane (LHP) of Laplace domain, which means that the system has a minimum phase behavior.

4.3.2 Passive Elements Selection

R, C, and L values are to be set taking into account both *system operating requirements* (table 4.1) and *system constraints*.

According to the *currents and voltages ripple analysis*, if $max(\Delta i_L) \leq 10\%$ and $max(\Delta v_o) \leq 1\%$ are desired, equations (4.58) and (4.59) must be assured.

$$max(\Delta i_L) \geq \frac{max(V_g) - \left(\frac{R_L}{max(R)(1-D)} min(V_o)\right)}{2L} DT_s \tag{4.58}$$

$$max(\Delta v_o) \geq \frac{max(V_o)}{2min(R)C} \tag{4.59}$$

Solution of equations (4.58) and (4.59) for C and L is given by equations (4.60) and (4.61), respectively.

$$L \geq \frac{max(V_g) - \left(\frac{R_L}{max(R)(1-D)} min(V_o)\right)}{2max(\Delta i_L)} DT_s \tag{4.60}$$

$$C \geq \frac{max(V_o)}{2min(R)max(\Delta v_o)} \tag{4.61}$$

Both equations (4.60) and (4.61) give a minimum boundary for values of L and C.

According to the *losses effect and efficiency analysis*, the worst condition for the Boost DC-DC convert is when $V_g = V_{g_{min}} = 30V$ and $V_o = V_{o_{max}} = 95V$, because $M(D) = M_{max}(D) \approx 3.17$. To assure that in the worst case $\eta \geq 90\%$, losses ratios must be $\alpha_C < 0.05$ and $\alpha_L < 0.05$ when $R = R_{max} = 100\Omega$ (See Figure (4.9)).

According to the *continuous conduction mode (CCM) analysis*, to always operate in CCM given R, equation (4.62) must be assured.

$$L > \frac{RT_s}{2} max(K(M(D), D)) \tag{4.62}$$

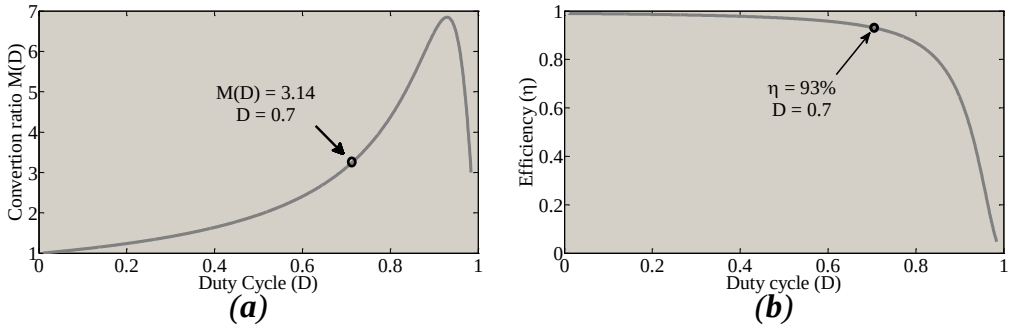

FIGURE 4.9: *(a)* Conversion ratio $M(D)$. *(b)* Efficiency η.

Equation (4.62) also gives a minimum boundary for L value. Then, both equations (4.60) and (4.62) must be evaluated and the maximum value, for minimum boundary L value, must be selected. Therefore, in order to fulfil *system operating requirements* $C \geq 14.120\mu F$ and $L \geq 326.34\mu H$.

According to the *zeros-based dynamical system analysis*, minimum possible value for C causes maximum *overshoot* in v_o. While a minimum possible value for L causes maximum *overshoot* in i_L. Moreover, minimum C and L values give minimum system *setting time*.

In contrast, large values for C cause high *overshoots* for i_L. While large values for L cause high system *setting time*.

In order to establish maximum possible values for C and L, two additional designed requirements are given: *(a)* maximum duty-ratio-to-output-voltage overshoot $O.S._{G_{vd}}$ and *(b)* maximum duty-ratio-to-inductor-current overshoot $O.S._{G_{i_L d}}$.

With minimum values of C and L, $O.S._{G_{vd}} = 57.3427\%$, $O.S._{G_{i_L d}} = 190.0448\%$, $ts = 2.3ms$ (See Figure (4.10)). Some simulations were carried out based on equations (4.24) and (4.23) to evaluate the effect of large values for both C and L in system performance (See Figure (4.11)).

From Figure (4.11), any effect over system performance is achieved if the values of both C and L are increased simultaneously. However, if either C or L values are increased both $O.S._{G_{vd}}$ and $O.S._{G_{i_L d}}$ are decreased. Nevertheless, larger values of L have a major impact that larger values of C.

By Figure (4.11), $L = 1mH$ and $C = 15\mu F$ are selected, since with these values $O.S._{G_{vd}} \approx 52\%$ and $O.S._{G_{i_L d}} \approx 100\%$, i.e., $O.S._{G_{i_L d}}$ is reduced approximately 90%. Further, $ts = 3.4ms$, i.e., the system setting time is increased $1.1ms$.

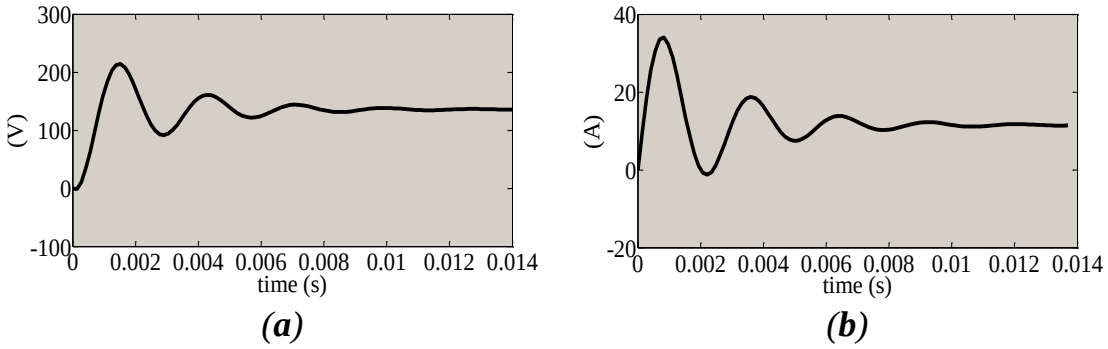

FIGURE 4.10: *(a)* G_{vd} Step system response. *(b)* Gi_Ld Step system response.

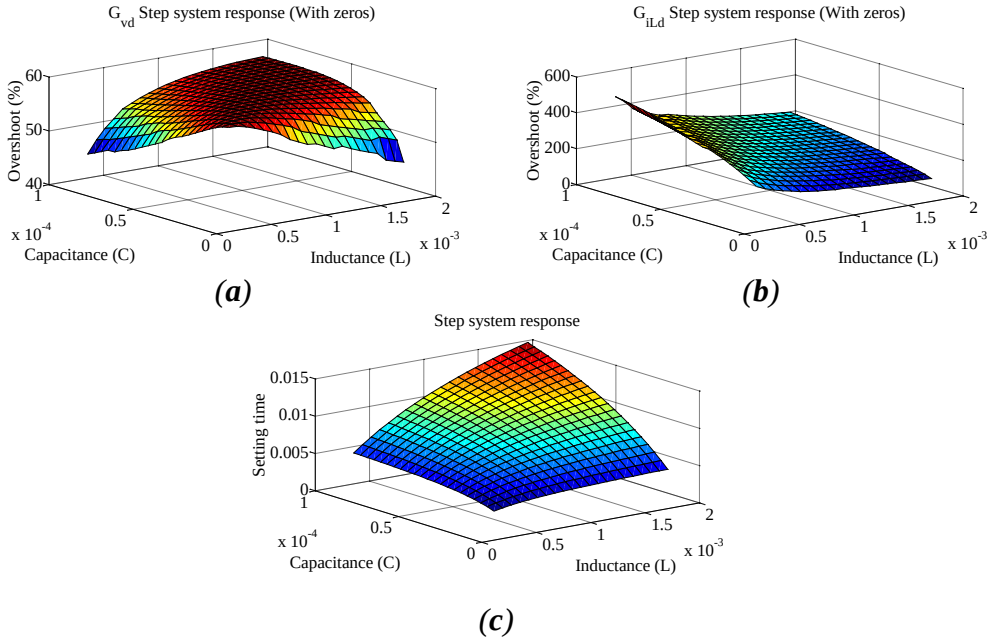

FIGURE 4.11: *(a)* G_{vd} Step system response varying C and L: overshoot with zeros. *(b)* G_{i_Ld} Step system response varying C and L: overshoot with zeros. *c* Step system response varying C and L: setting time.

4.3.3 System Frequency Response Verification

This step is not considered in proposed design procedure of PECs, but in order to validate the designed Boost DC-DC converter via simulation, frequency response of both mathematical model and PSIM circuital implementation are contrasted. The Boost DC-DC converter was parameterized with $L = 1mH$, $C = 15\mu F$, $v_g = 35$, $v_o = 70$, $i_o = 0$,

$R_L = 0.3\Omega$, $R_C = 0.17\Omega$, $R = 50\Omega$. Then, the equilibrium point has been found by solving equations (4.27), (4.25), and (4.26), then $I_L = 2.8812A$ and $D = 0.5141$.

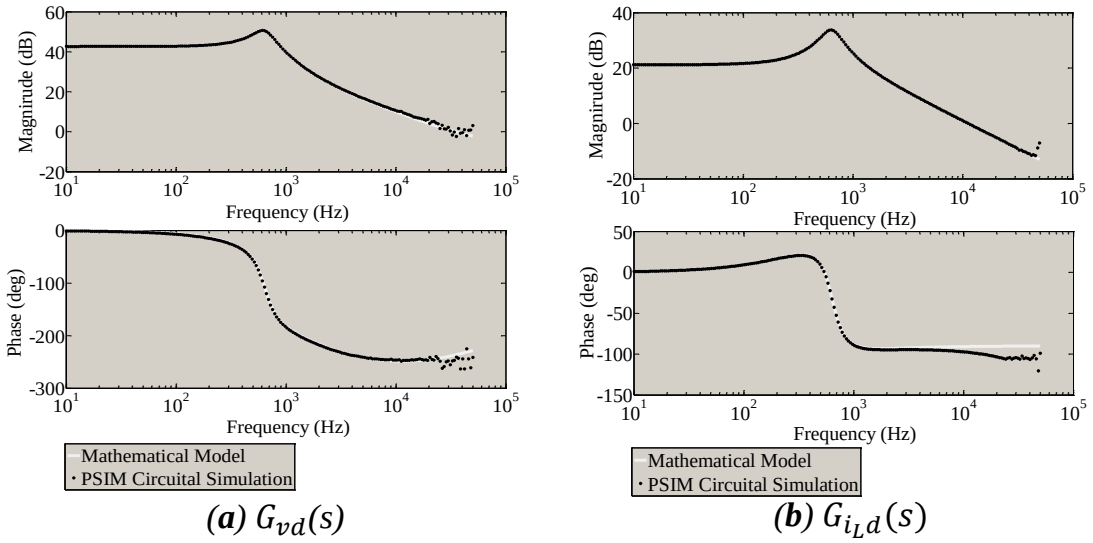

FIGURE 4.12: *(a)* G_{vd} Bode diagram. *(b)* G_{i_Ld} Bode diagram.

Figures (4.12) present the Boost DC-DC converter Bode diagrams of the mathematical model given by (4.23, 4.24) and PSIM circuital implementation. Frequency response of the Boost DC-DC converter PSIM circuital implementation coincides with the Boost DC-DC mathematical model. The Boost DC-DC converter of the PSIM circuital implementation is satisfactorily reproduced by the Boost DC-DC converter mathematical model given by equations (4.23 and 4.24).

4.4 Controllability Verification of the Designed Boost DC-DC Converter

The third stage in proposed design procedure of PECs is controllability verification of the Designed Boost DC-DC Converter, which is composed by step 9. Then, algorithm (1) is applied to test the local controllability of the designed Boost DC-DC converter. Two states (v_C and i_L) were defined for the Boost DC-DC converter. From the point of view of the set theory in control, the Boost DC-DC converter with two states is a convenient system to analyze since the state-space dimension of the systems is $X \in R^2$. This allows to compute two dimensional robust reachable, controllable, and reversible sets of the system.

The nonlinear dynamical model given by equations in (4.16) is taken as nonlinear dynamical model of the Boost DC-DC converter in order to compute the robust reachable $\tilde{\mathcal{R}}^t(\Omega_t)$ and the robust controllable $\tilde{\mathcal{C}}^t(\Omega_t)$ sets. Previously, the nonlinear dynamical model given by equations in (4.16) is normalized in order to improve the numerical stability to compute the sets. The following boundaries for states and inputs were taken: $v_C \in [50V, 95V]$, $i_L \in [0.2A, 15A]$, $d \in [0.01, 0.89]$, $v_g \in [30V.40V]$, and $i_o \in [-1A, 1A]$. The sample size was $N = 100000$ accordingly with Chernoff bound given be equation (2.48).

Figure (4.13) shows normalized operating point $x_e = [0.4444, 0.1812]$, normalized robust reachable set $\tilde{\mathcal{R}}^t(\Omega_t)$ from x_e in $t = 3.5ms$, and normalized robust controllable set $\tilde{\mathcal{C}}^t(\Omega_t)$ to x_e in $t = 3.5ms$ for the Boost DC-DC converter. From Figure (4.13), $\tilde{\mathcal{R}}^t(\Omega_t)$ is nearly superimposed over $\tilde{\mathcal{C}}^t(\Omega_t)$ then the robust reversible set $\tilde{\tau}^t(\Omega_t)$ exist, i.e., is not empty. Furthermore, the system is locally controllable around the x_e and $CI = 0.9241$, i.e., based on CI (2.49) the designed Boost DC-DC converter is 92.41% controllable around the operating point.

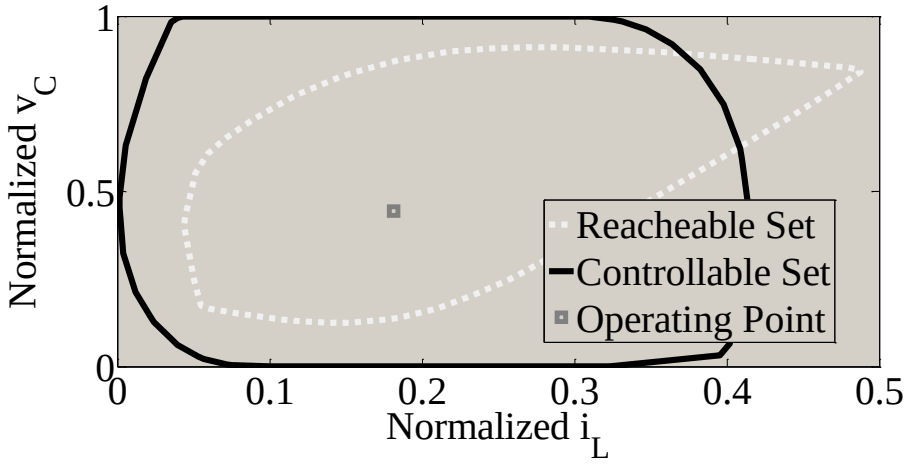

FIGURE 4.13: The Boost DC-DC converter sets.

4.5 Control Structure Design

The fourth stage in the proposed design procedure of PECs is control structure design, which is composed by step 10. In this section widely accepted Current-Mode Control (CMC) structure for Boost DC-DC converter is designed [61], [87]. The aim of this stage is to design a suitable control structure for designed Boost DC-DC converter such that control objective is achieved. This stage is composed of following subsections: *(1)*

control structure selection, *(2)* controllers tuning, *(3)* closed-loop system performance verification, and *(4)* system operating requirements verification.

4.5.1 Control Structure Selection

Generally speaking, converter control design is focused on imposing desired low-frequency behavior to the system by means of specified closed-loop requirements. In the Boost DC-DC converter operating in a switch-mode power supply, feeding a certain variable load, d needs adjustments in order to ensure a constant v_o for the entire operating range (voltage regulation). Besides, against any system disturbance, d value needs to be adjusted such that the system can be driven back to the operating point.

The Boost DC-DC converter contains a RHP zero in G_{vd}, i.e, the Boost DC-DC converter could have a non-minimum phase behavior. Non-minimum phase behavior is the reason why a CMC structure is needed. CMC structure employs cascaded loops. This cascaded structure allows the output voltage regulation while preserving the inductor current within specified safety limits. The outer control loop deals with voltage regulation imposing low-frequency dynamics and the inner loop concerns the faster current control. The voltage controller provides the setpoint of the inductor current, and this latter acts as the control input of the outer voltage loop.

In this work standard controllers are employed. Simple and robust classical invariant PI controllers that are tuned based on linearized Single-Input-Single-Output (SISO) averaged models of the Boost DC-DC converter given by equations (4.24, 4.23). These PI controllers generate a continuous control signal (duty ratio d), which needs a modulation so it may be applied to the power switching gates (PWM).

4.5.2 Controllers Tuning

The controller tuning task begins with a set of design specifications. The set of specifications are a group of goals for the behavior of the controlled system. Specifications are composed for both transient behavior (e.g. rise time, setting time, and maximum closed-loop system overshot) and stability margins (e.g., relative stability, gain margin, phase margin).

Time domain specifications are placed by the system performance specifications. The transient response of a regulated system is typically limited in terms of maximum deviation from the rated output value and setting time in response to a transient. The goal for the Boost DC-DC converter controller design presented is to control the output voltage v_o to within 2% of rated value (i.e. $68.6V$ to $71.4V$) in response to unit step

transients in both input voltage v_g and current source i_o. Also, the controller should be able to maintain the rated output voltage within the tolerances as the input varies over a range from $30V$ to $40V$, though this should be considered a steady-state, not transient, operating requirement. As a final specification, steady-state error in the output voltage v_o should be eliminated.

Due to the fact that the Boost DC-DC converter switching frequency is $100kHz$, inner loop bandwidth (i.e., current loop) must be smaller than $20kHz$ and outer loop bandwidth (i.e., voltage loop) must be smaller than $\frac{1}{5}$ inner loop bandwidth [88], i.e., smaller than $5kHz$. Additionally, a robustness index $M_s < 2$ is desired to establish a trade-off between control performance and robustness [66].

A PI controller, acting directly on d, has been designed to track the inductor current $i_{L_{REF}}$ since the $G_{i_L d}$ exhibits a minimum phase behavior. The inductor current PI controller was designed by means of the root-locus technique, adopting following design specifications: damping factor ζ equal to 0.707 and a $20kHz$ closed loop bandwidth. The designed PI controller transfer function $G_{C_{i_L}}(s)$ is given by the equation (4.63). These PI controller design specifications ensure: *(a)* zero steady-state error and a satisfactory reference tracking for frequencies below $20kHz$ observed on transfer function $T_{i_L i_{L_{REF}}}$ in Figure (4.14). *(b)* Effective disturbance rejection for both input voltage v_g and current source i_o variations observed on transfer functions $T_{i_L v_g}$ and $T_{i_L i_o}$ in Figure (4.14), respectively. *(c)* A $M_s = 1.2$.

$$G_{C_{i_L}}(s) = \frac{1.27s + 55218}{s} \tag{4.63}$$

Once the current control loop is closed, equivalent simplified representation of the Boost DC-DC converter showed in Figure (4.15) is derived. Large- and small-signal models of simplified Boost DC-DC converter are given by equations (4.64) and (4.65), respectively. Applying realization given by the equation(4.22), the transfer functions for the systems described by the equation (4.65) are given by the equation (4.67).

$$C\frac{dv_C}{dt} = \left(\frac{1}{1+\alpha_C}\right)\left(i_{L_{REF}}(1-D) - \frac{v_C}{R} - i_o\right) \tag{4.64}$$

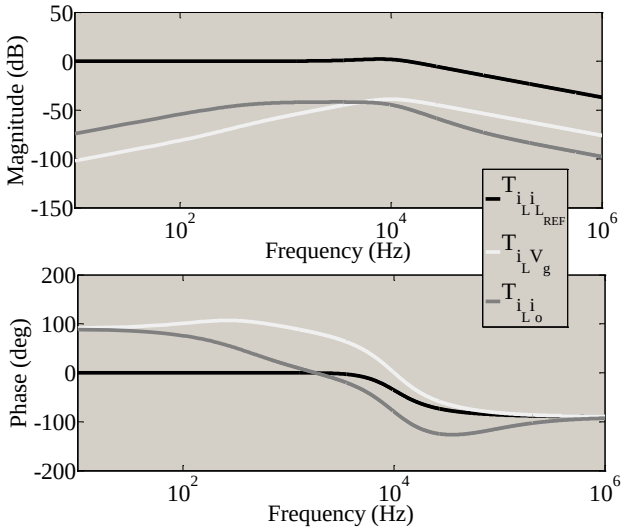

FIGURE 4.14: Inner current control loop transfer functions.

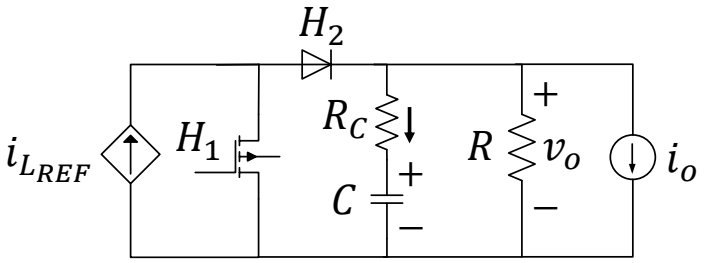

FIGURE 4.15: The equivalent simplified representation of the Boost DC-DC converter.

$$\begin{bmatrix} \dot{v_C} \end{bmatrix} = \begin{bmatrix} -\left(\frac{1}{1+\alpha_C}\right)\frac{1}{RC} \end{bmatrix} \begin{bmatrix} v_C \end{bmatrix} + \begin{bmatrix} \left(\frac{1}{1+\alpha_C}\right)\frac{(1-D)}{C} & -\left(\frac{1}{1+\alpha_C}\right)\frac{1}{C} \end{bmatrix} \begin{bmatrix} i_{L_{REF}} \\ i_o \end{bmatrix} \tag{4.65}$$

$$\begin{bmatrix} v_o \end{bmatrix} = \begin{bmatrix} \left(\frac{1}{1+\alpha_C}\right) \end{bmatrix} \begin{bmatrix} v_C \end{bmatrix} + \begin{bmatrix} \left(\frac{1}{1+\alpha_C}\right) R_C(1-D) & -\left(\frac{1}{1+\alpha_C}\right) R_C \end{bmatrix} \begin{bmatrix} i_{L_{REF}} \\ i_o \end{bmatrix} \tag{4.66}$$

$$G_{v_o}(s) = \frac{\begin{bmatrix}[(1+\alpha_C)RCR_Cs + R + R_C](1-D) \\ -(1+\alpha_C)RCR_Cs + R + R_C\end{bmatrix}}{(1+\alpha_C)\left[(1+\alpha_C)RCs + 1\right]} \tag{4.67}$$

A PI controller, that provides the setpoint of the inductor current control loop, has been designed to regulate v_o since the $G_{v_o i_{L_{REF}}}(s)$ transfer function exhibits a minimum phase behavior. The output voltage PI controller was designed by means of the root-locus technique, adopting following design specifications: damping factor ζ equal to 0.707 and a $5kHz$ closed loop bandwidth. The designed PI controller transfer function $G_{C_{v_o}}(s)$ is given by the equation (4.68). Above PI controller design conditions ensure: *a.* zero steady-state error observed on transfer function $T_{v_o v_{o_{REF}}}$ in Figure (4.16). *b.* Effective disturbance rejection for the current source i_o variations observed on transfer function $T_{v_o i_o}$ in Figure (4.16). *c.* A $M_s = 1.2$.

$$G_{C_{v_o}}(s) = \frac{0.07994s + 235.1}{s} \tag{4.68}$$

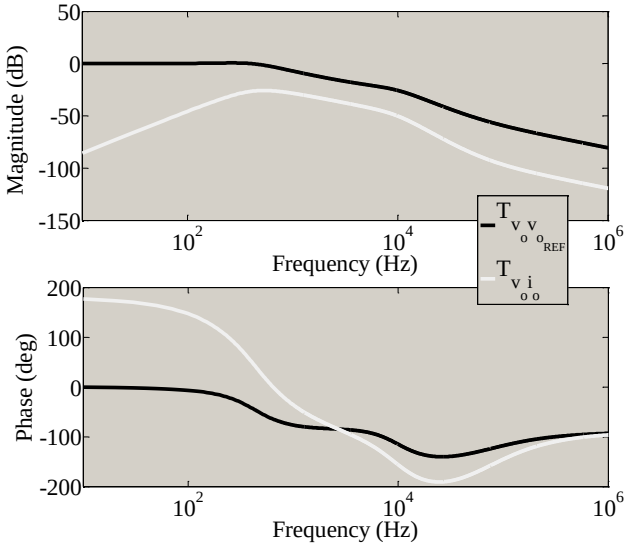

FIGURE 4.16: *Outer output voltage control loop transfer functions.*

4.5.3 Closed-Loop System Performance Verification

To assess the closed-loop system performance, the non-ideal designed Boost DC-DC converter with its control structure has been implemented in PSIM. Figure (4.17a) shows the closed-loop behavior at unit steps of i_o around the operating point corresponding

to the full load. Two current source i_o unit steps were applied to evaluate the control structure performance. First unit step was applied at $t = 10ms$ and for $10ms$, then the current source returns to its rated value $i_o = 0$. Second unit step was applied at $t = 30ms$ and for $10ms$, then the current source returns to its rated value $i_o = 0$. From Figure (4.17a) is observed a satisfactory tracking of $i_{L_{REF}}$ provided by the outer PI voltage controller and a satisfactory regulation of v_o to reject the load disturbances depicted as changes in i_o.

Figure (4.17b) shows the closed-loop behavior at unit steps of the input voltage v_g. Two v_g unit steps were applied to evaluate the control structure capabilities to regulate v_o and to evaluated the boost capabilities of the designed Boost DC-DC converter. Firs unit step was applied at $t = 10ms$ and for $10ms$. This first unit step was equal to $v_g = -5V$, i.e., the final value of the input voltage was $v_g = 30$ that corresponds with its lower boundary. Second unit step was applied at $t = 30ms$ and for $10ms$. This second unit step was equal to $v_g = +5V$, i.e., the final value of the input voltage was $v_g = 40V$ that corresponds with its upper boundary. From Figure (4.17b) is observed a satisfactory tracking of $i_{L_{REF}}$ provided by the outer PI voltage controller and a satisfactory regulation of the v_o to changes in v_g. It is important to remark that under the worst condition for input voltage v_g, the Boost DC-DC convert was able to keep the output voltage in its rated value.

Finally, Figure (4.17c) shows the closed-loop behavior at random unit steps of both i_o and v_g. This unit steps were applied such that the designed control structure performance could be evaluated against any random disturbance. From Figure (4.17c) is possible to see that the designed control structure has a satisfactory performance against multiple disturbances within specified design requirements for the Boost DC-DC converter in table 4.1.

4.5.4 System Operating Requirements Verification

Figure (4.18) shows: *(a)* P_{in}, P_{out}, and η and *(b)* i_L and v_o, when case c of Figure (4.17) is considered.

From Figure (4.18a) is seen that P_{out} never exceeds the maximum admissible output power and it is always less that P_{in}. It is also seen that the Boost DC-DC converter is never 100% efficient. Furthermore, from Figure (4.18a) is seen that only between $t = 0.01s$ and $t = 0.02s$ the efficiency is below 0.9. However, in this time interval v_g is equal to $20V$, i.e., in this time interval the Boost DC-DC converter operates in a not considered condition in table 4.1. Accordingly, the designed Boost DC-DC converter satisfies both power and efficiency requirements.

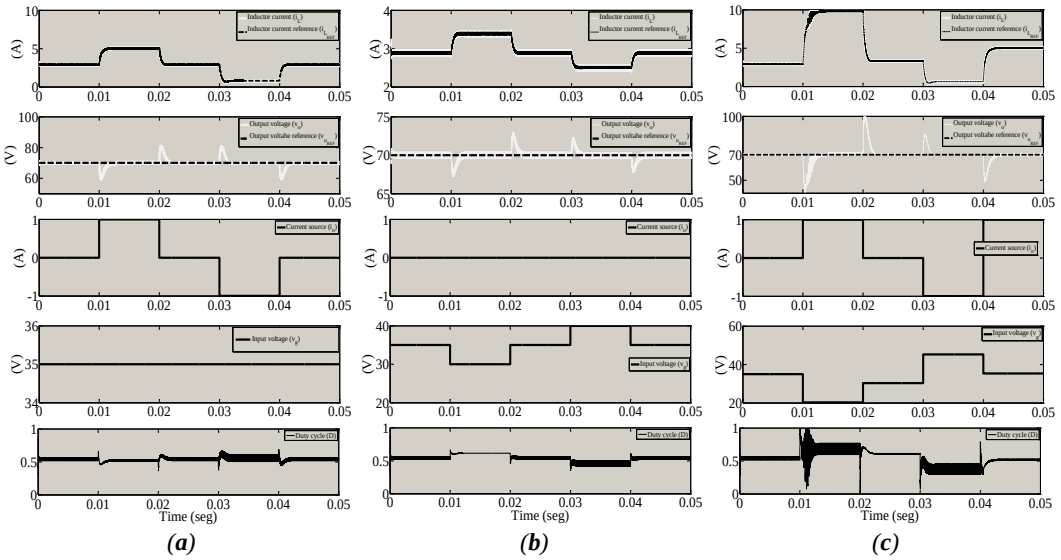

FIGURE 4.17: Closed-loop behavior at unit steps system disturbances.

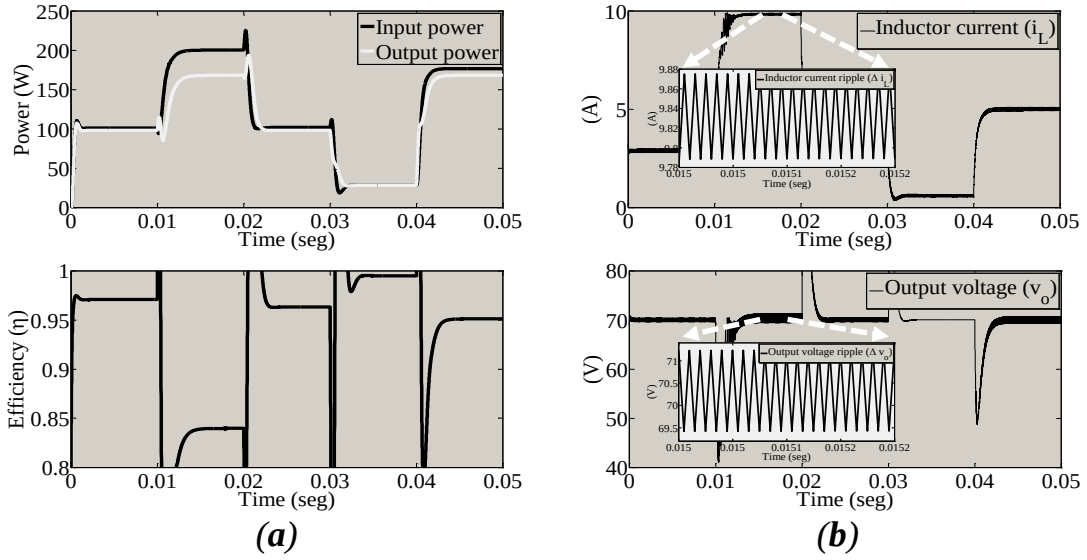

FIGURE 4.18: *(a)* Instantaneous Power and efficiency verification. *(b)* Ripples verification.

Figure (4.18b) shows i_L and v_o, a zoom was made for the worst simulated system condition. From Figure (4.18b) is seen that even in the worst i_L and v_o condition, ripples are below to 1%. Accordingly, the designed Boost DC-DC converter satisfies both i_L and v_o ripples condition.

In conclusion, Figure (4.18) shows that the Boost DC-DC converter system operating requirements given in table 4.1 are satisfied even in the worst simulated case (4.17c).

4.6 Conclusions

In this chapter a Boost DC-DC converter was designed applying the proposed design procedure presented in chapter 3. Both large- and small-signal models were derived and used to system design.

To determine suitable passive elements boundaries such that system operating requirements were assured, steady-state, currents and voltages ripple, losses effect and efficiency, CCM, and zero-based dynamical analysis were carried out. The steady-state analysis allowed to obtain an expression to the equilibrium conversion ratio $M(D)$ for an non-ideal Boost DC-DC converter when both inductor Equivalent Series Resistance (ESR) R_L and capacitor ESR R_C are considered. Currents and voltages ripple analysis allowed to find lower boundaries for L and C. Losses effect and efficiency analysis allowed to obtain an expression to the systems efficiency in function of the system parameters. This efficiency expression allowed to assure that in steady-state the efficiency of the designed system was always above 90%, even in the worst system condition case. The CCM analysis allowed to find lower boundaries to guarantee that the designed system operated in CCM mode, even in the worst systems condition case. Finally, the zeros-based dynamical system analysis allowed to select suitable L and C values such that the operating requirements were satisfied and both maximum current and maximum voltage overshoot were limited in order to avoid system failures.

Since the passive elements were selected, some simulations of both mathematical model and PSIM circuital implementation were carried out to verify the correspondence between both models. Later the design controllability verification was made, and both robust reachable and controllable sets were computed. The CI showed that the designed Boost DC-DC converter was 92.41% controllable around its operating point.

Finally, the CMC structure for the Boost DC-DC converter was designed and implemented in PSIM to verify the system closed-loop performance. Designed CMC structure allowed to fulfil the control objective and satisfied the operating requirements. To conclude, the proposed design procedure was successfully applied to design one of the basic DC-DC converter topology.

Chapter 5

Case of Study: Three-Leg Split-Capacitor Shunt Active Power Filter

In this chapter, design procedure presented in chapter 3 is applied to a Three-Leg Split-Capacitor Shunt Active Power Filter (TLSC SAPF). TLSC SAPF is a PEC able to mitigate problems related with inefficient load currents (reactive, harmonic, and unbalanced ones) in electric power quality improvement field. TLSC SAPF requirements are established such that designed converter is suitable for a medium-power electrical application. Both large- and small-signal models are derived and used for system design. Large-signal models are obtained in the general form. Small-signal models are obtained in both time and frequency domains to have ready-to-use models for control purposes. Steady-state, currents and voltage waveforms, losses effect and efficiency, and zeros-based dynamical system analysis are carried out to determine suitable passive elements boundaries such that system operating requirements are assured. Passive elements boundaries are established based on system knowledge, then some simulations are carried out to evaluate their impact in the dynamical systems performance. The design controllability-oriented verification method is applied to designed TLSC SAPF and it is concluded that designed converter is 67.72% locally controllable. Finally, a Voltage Oriented Control (VOC) structure is designed for TLSC SAPF and it is implemented in PSIM. A satisfactory closed-loop dynamical system performance is obtained.

5.1 Introduction

In three-phase four-wire power systems, the proliferation of inefficient loads causes reactive power demand, harmonic distortion and unbalanced voltages and currents, which cause an excessive current flowing through the neutral wire [89]. Furthermore, inefficient loads connection cause wire losses [90], [91], transformer losses [92], [93], and electric rotating machinery losses [94]. All of these problems result in economic losses for both the supplier and the consumer [95], [96], [97], [98].

The term Active Power Filter (APF) is a widely used terminology in electric power quality improvement field [99], [100]. The work presented by [101] reports two topologies for Shunt Active Power Filter (SAPC) called Four-Leg Full-Bridge (FLFB) topology and Three-Leg Split-Capacitor (TLSC) topology. They propose an alternative topology called Four-Leg Split-Capacitor (FLSC). According to the authors, FLFB topology offers a high easiness to control converter outputs thanks to its greater number of legs (4 legs). Nevertheless, to control FLFB SAPF topology is necessary advanced current control techniques to achieve suitable reference current tracking, such as space-vector modulation. TLSC SAPF topology has a smaller number of legs (3 legs) than FLFB topology and it allows to control each of these legs independently. Above control fact allows to use as modulation technique the well-know carrier-based Pulse-Width Modulation. However, TLSC SAPF drawback is that zero-sequence currents flowing through the DC-link. Zero-sequence currents give rise to a voltage unbalanced condition between capacitors, which is a undesirable effect when a precise SAPF control is required. Accordingly, authors propose an alternative topology as result of join FLFB and TLSC topologies. New topology is FLSC, which solves problems presented in above two topologies. In FLSC topology each leg work independently and zero-sequence currents can be regulated such that currents flowing through the DC-link are avoided. Although still in FLSC SAPF topology are necessary advanced current control techniques to achieve suitable reference current tracking.

The work presented by [59] presents a review of four control strategies (p-q method, $i_d - i_q$ method, unity power factor method, and Perfect Harmonic Cancellation (PHC) method) for the extraction of reference currents for a TLSC SAPF connected to a three-phase four-wire source that supplies a nonlinear load. A comparison of the methods is made by simulations and experimental validation under various load conditions and both ideal and distorted mains voltage conditions. Authors conclude that$p$-q strategy (maybe the most widely used) and the $i_d - iq$ strategy are the most sensitive to distortion and unbalanced in the voltages at the Point of Common Coupling (PCC). Authors also conclude that, although the objective of unity power factor method is to attain unity power factor and to minimize source current RMS values, with the power definitions

on IEEE Std. 1459 the goals are not achieved in the case of three-phase four-wire systems with zero-sequence components in the voltage. Finally, authors conclude that if it seeks compliance with harmonics standards, unbalanced elimination, and reactive power compensation, PHC method is the only strategy which is capable of correct action under any condition tested.

The work presented by [102] presents a comprehensive study on three-phase four-wire SAPF. TLSC SAPF, FLFB SAPF, and three H-bridge (3HB)-based SAPF topologies are compared. The performance of all three topologies, under an unbalanced non-linear load condition, is evaluated with a detailed Digital Signal Processor (DSP)-based experimental investigation. Steady-state as well as dynamical performance of APF are studied as compensator for current harmonics, reactive power, current unbalance and neutral current. Advantages and limitations offered by each of the topologies are also discussed. Authors report 41 significant publications on the three-phase four-wire SAPF over more than 100 critically studied. After experimental investigation of these three topologies, authors conclude that, under identical experimental environment and control strategy, all three topologies have given satisfactory results under both steady-state and dynamical performance conditions. Moreover, authors conclude that: *(a)* FLFB SAPF topology could be a better choice for superior performance in low-to-medium-power applications, whereas, *(b)* for the same applications with slight performance compromising the low cost TLSC SAPF topology would be appropriate. *(c)* the topological advantage makes 3HB SAPF topology a promising candidate for the high-voltage and medium-to-high-power applications.

In this chapter a TLSC SAPF is selected to apply the design procedure detailed in chapter 3 due to the fact that this topology satisfies the trade-off between simplicity and applicability in three-phase four-wire systems to electrical power quality improvement. Moreover, this PEC has been tested by others authors via simulation and experimental validated [103], [104], [105], [106], [107].

5.2 Dynamical Modeling

The firs stage in proposed design procedure of PECs is dynamical modeling. This stage is composed by steps 1 - 6 divided in 4 subsections. Where, both system structure and operating requirements are established and both large- and small-signal models are derived. The stage aim is to obtain both design- and control-oriented models. This section is composed of following subsections: *(1)* system structure selection, *(2)* system operating requirements, *(3)* large-signal models, and **(3)** small-signal models.

5.2.1 System Structure Selection

The first step in the proposed design procedure of PECs is the establishment of the system operating requirements. As it is shown in Figure (5.1), a single-phase Voltage Source Inverter (VSI) is a differential connection of two bidirectional Buck DC-DC converters ($F_1 - F_2$ and $F_3 - F_4$ as switches). If converter 1 produces an output voltage V_1 and converter 2 produces an output voltage V_2, then the VSI output voltage V_{inv} is given by the equation (5.1).

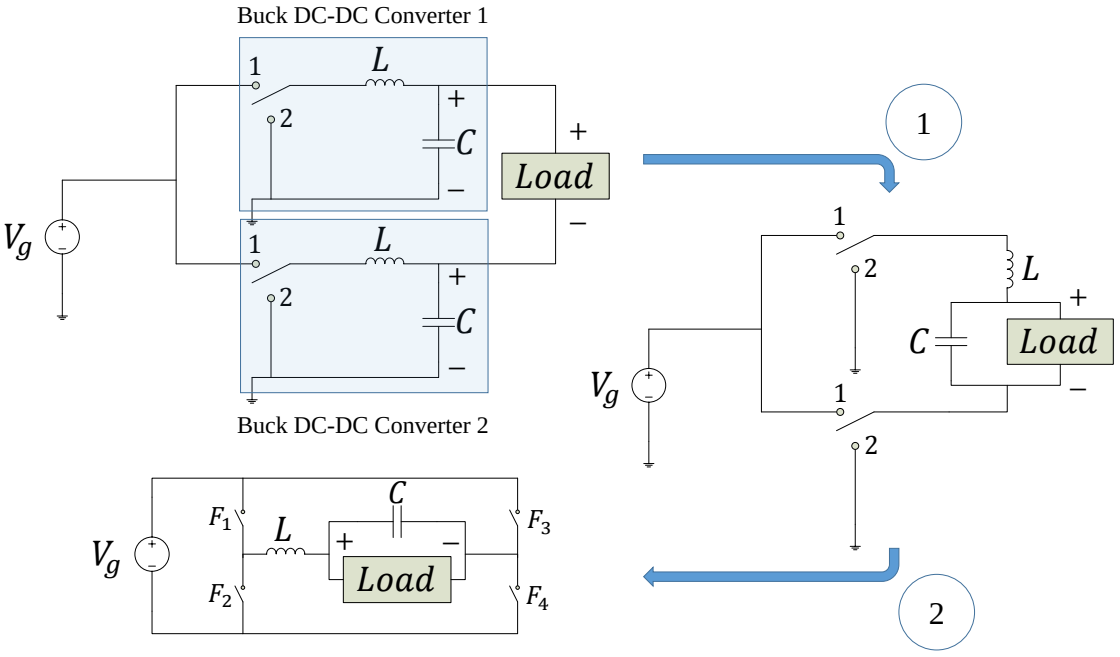

FIGURE 5.1: Derivation of Buck-converter-based VSI.

$$V_{inv} = V_1 - V_2 \tag{5.1}$$

Although V_1 and V_2 may both individually be positive, the VSI output voltage V_{inv} can be either positive or negative. Typically, if converter 1 is driven with duty cycle D, then the converter 2 is driven with its complement $(1 - D)$, such that when V_1 is positive, V_2 is negative, and vice versa. As it is known [78], ideal Buck DC-DC converter produces an output voltage $V_{out} = DV_g$, where D is duty cycle and V_g is input voltage. Accordingly, in a differential connection, converter 1 produces an output voltage $V_1 = DV_g$, while converter 2 produces an output voltage $V_2 = (1 - D)V_g$. Therefore, V_{inv} is given by the equation (5.2).

$$V_{inv} = (2D - 1)V_g \tag{5.2}$$

Equation (5.2) is plotted in Figure (5.2). It is seen that V_{inv} is positive for $D > 0.5$ and negative for $D < 0.5$. If D is varied sinusoidally about a quiescent operating point of 0.5, then V_{inv} will be sinusoidal without dc-offset.

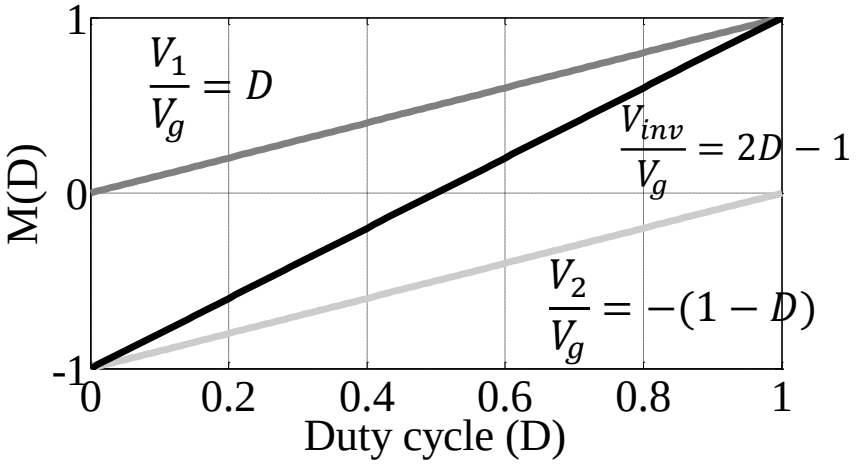

FIGURE 5.2: Steady-state characteristics under DC or low operating frequency of Buck-converter-based VSI.

The carrier-based Pulse Width Modulation (carrier-based PWM) is an option to sinusoidally variation D [108]. The carrier-based PWM is comprised of modulation signals and a carrier signal. The PWM signals are generated by comparing the modulation signals with a symmetrical triangular carrier signal. If bipolar triangular carrier signal ($-V_{tri}$ to V_{tri}) is used, the dc-offset in modulation signal V_{ref} is zero. The fundamental frequency of V_{ref} is VSI operating frequency f_s. The triangular carrier signal frequency establishes VSI switching frequency f_{sw}, which is significantly higher than f_s.

V_{inv} is composed of f_s as well as very high frequency components (due to modulation), which can be filtered using L or LCL filters [108]. After filtering high frequency components, the VSI can be connected to the grid in either shunt or series form, i.e., as current source [59], [64] or voltage source [109], respectively.

Polyphase VSI circuits can be derived by connecting more DC-DC converters in a differential form. As it is shown in Figure (5.3a), a three-phase load can be differentially connected across outputs of three bidirectional Buck DC-DC converters. If the three-phase load is balanced, neutral voltage V_n is equal to the average of three converters output voltage. If converters output voltage (V_1, V_2, and V_3) have the same dc-offset,

this dc-offset appears at neutral point n. Phase voltages V_{an}, V_{bn}, and V_{cn} are given by the equation (5.3).

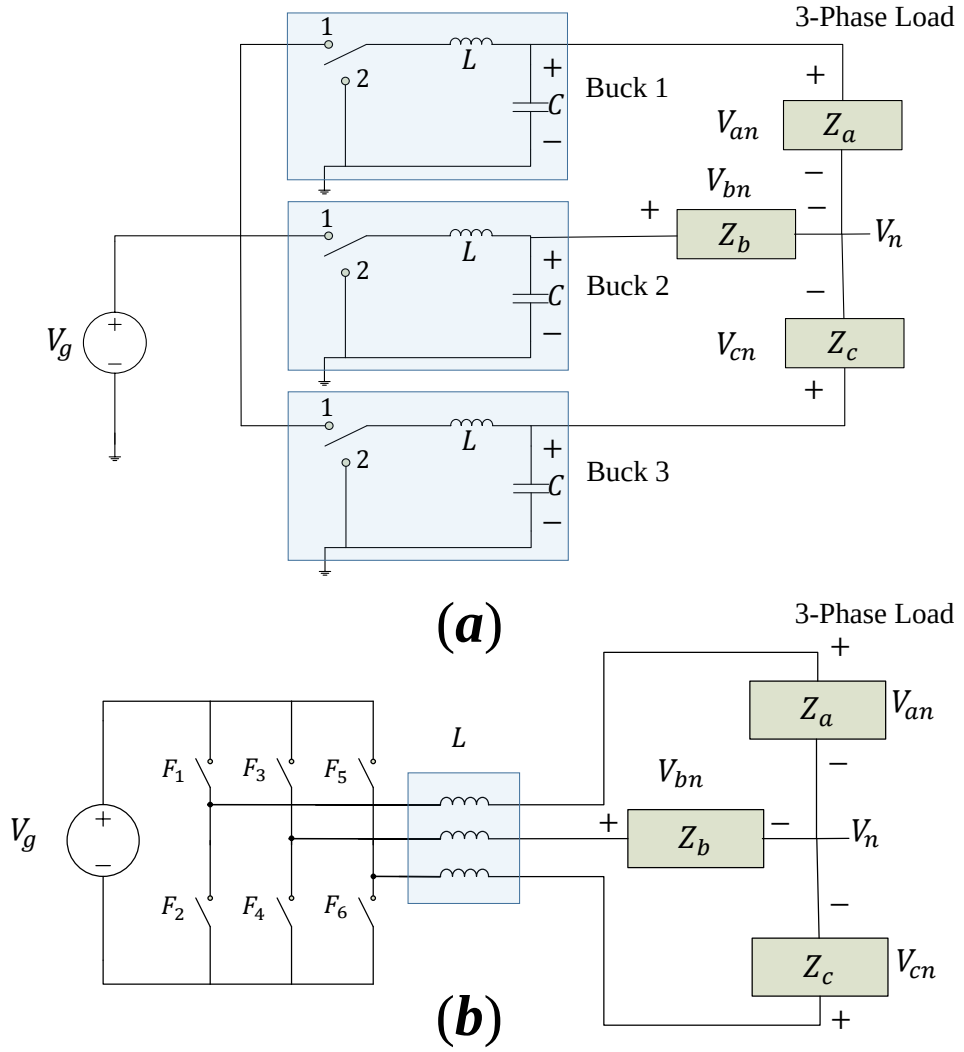

FIGURE 5.3: *(a)* Three-phase Buck-converter-based VSI. *(b)* Three-phase VSI.

$$\begin{aligned} V_{an} &= V_1 - V_n \\ V_{bn} &= V_2 - V_n \\ V_{cn} &= V_3 - V_n \end{aligned} \tag{5.3}$$

From equation (5.3), it is seen that the dc-offset is cancelled out and does not appear in V_{an}, V_{bn}, and V_{cn}.

For clarity, the circuit showed in Figure (5.3a) is re-drawn in Figure (5.3b). This converter is well-known as three-phase three-wire Buck-converter-based VSI or simply three-phase three-wire VSI [78]. Three-phase three-wire VSI is widely employed in both renewable energy [110] and power quality improvement [10] fields.

In a similar way, Boost-converter-based VSIs and Buck-boost-converter-based VSIs are also derived [111].

Three-phase three-wire VSI topology showed in Figure (5.3b) is suitable for three-phase three-wire systems working in balanced condition. Nevertheless, proliferation of non-linear loads causes harmonic distortion and both unbalanced voltages and currents in grids. Furthermore, three-phase four-wire systems are employed in order to have the possibility to generate zero sequence currents flowing through the neutral wire. Accordingly, for power quality improvement in three-phase four-wire systems a three-phase four-wire compensator is more suitable.

From circuit in Figure (5.3b), a three-phase four-wire VSI is built. A three-phase four-wire VSI is obtained if V_g is replaced by a split-capacitor DC-link and the neutral wire of the system is connected to the midpoint of the split-capacitor DC-link, such that system zero-sequence currents flow through it. Figure (5.4) shows a three-phase four-wire split-capacitor VSI in shunt connection to the grid through a coupling inductor L. The configuration showed in Figure (5.4) is known as Three-Leg Split-Capacitor Shunt Active Power Filter (TLSC SAPF).

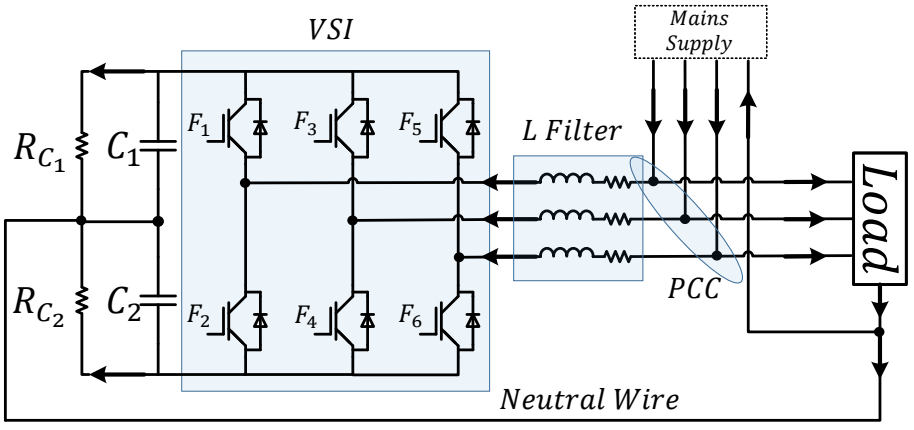

FIGURE 5.4: Three-phase four-wire split-capacitor VSI.

TLSC SAPF is able to solve the problem of reactive, harmonic and unbalanced currents, while mitigates the effect of neutral currents. Several works showing the TLSC SAPF effectiveness for power quality improvement have been carried out [103], [104], [105],

[106], [107]. In this work, the proposed design procedure presented in chapter 3 is applied to design a TLSC SAPF.

5.2.2 System Operating Requirements

Once that system structure is selected, system operating requirements must be established. Typical TLSC SAPF requirements are: input DC-link voltage range, rated grid voltage, both input and output electrical power capacity range, VSI switching frequency, fundamental operating grid frequency, maximum admissible Total Harmonic Distortion (THD) in both voltages and currents, and expected TLSC SAPF efficiency. The set of operating requirements are specified in Table (5.1).

TABLE 5.1: TLSC SAPF operating requirements.

Requirement	**Values**		
	Min	**Typ**	**Max**
Input DC-link voltage range	550V	600V	650V
Rated grid voltage (line-to-neutral rms)	119V	120V	121V
Input power range	0W	–	1.5kW
output power range	0W	–	1.5kW
VSI switching frequency		20kHz	
Rated grid frequency	49.9Hz	50Hz	50.1Hz
THD (voltage)	–	<5%	–
THD (current)	–	<5%	–
Load	100VA	–	1.5kVA
Steady-State TLSC SAPF efficiency	90%	95%	98%

THD constraint given in Table (5.1) is according with the IEEE Std. 519-2014 [112]. TLSC SAPF requirements given in Table (5.1) are requirements for a medium-power electrical application [113].

Steps 2-6 in the proposed design procedure are concerning to develop a system mathematical dynamical model. For TLSC SAPF system showed in Figure (5.4), two types of mathematical models are derived in order to represent both high frequency (large-signal models) and low-frequency (small-signal models) behaviors.

Dynamical modeling process is carried out in two sub-steps: *(a)* mathematical dynamical model of grid-isolated TLSC SAPF is deduced. Then, *(b)* mathematical dynamical model of grid-tied TLSC SAPF is deduced.

5.2.3 Large-Signal Models

Grid-tied TLSC SAPF circuital configuration showed in Figure (5.5) is composed of: *(a)* split-capacitor DC-link, *(b)* VSI, *(c)* coupling L filter, and *(d)* electrical power grid. TLSC SAPF showed in Figure (5.5) works as current source and it is able to reduce current-related system phenomena (current harmonics, unbalanced currents, and zero-sequence currents) due to inefficient loads.

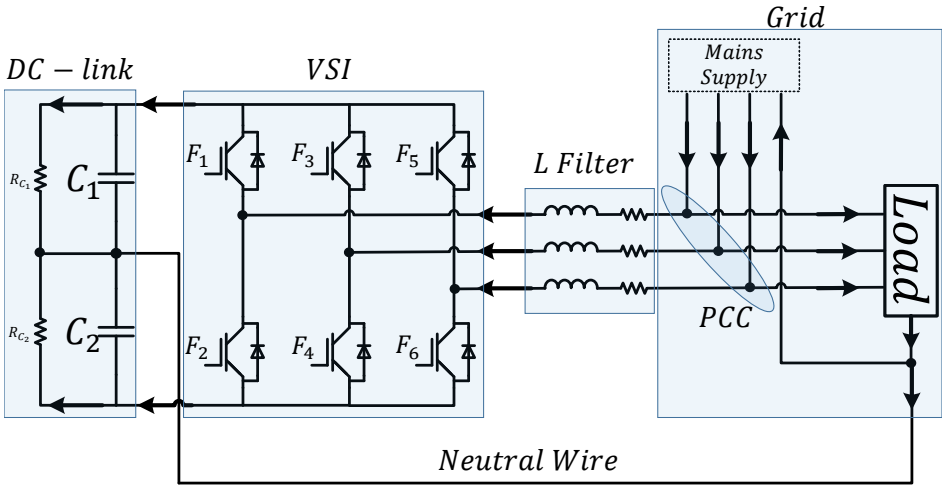

FIGURE 5.5: The grid-tied TLSC SAPF circuital configuration.

Grid-isolated TLSC SAPF circuital configuration is showed in Figure (5.6a) and its equivalent per phase TLSC SAPF circuital configuration is showed in Figure (5.6b). The circuit in Figure (5.6b) is divided in two sub-circuits: *(a)* VSI and *(b)* coupling L filter. Current Kirchhoff's law is applied to the sub-circuit *(a)*, thus voltage capacitor equations are given by equations (5.4) and (5.5).

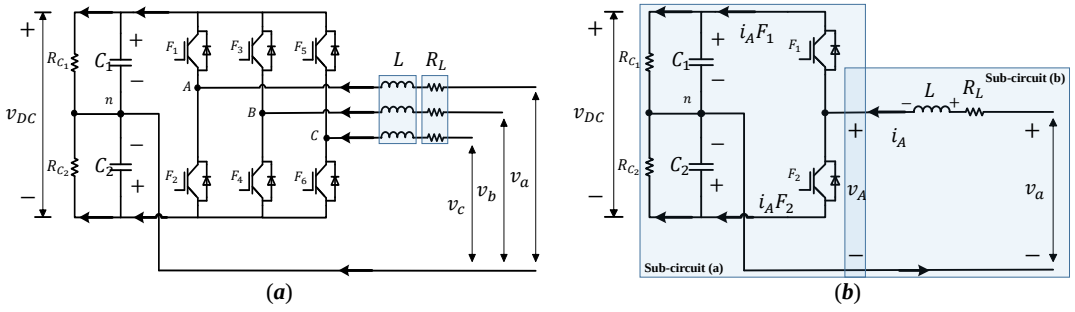

FIGURE 5.6: *(a)* The grid-isolated TLSC SAPF circuital configuration. *(b)* Per phase TLSC SAPF circuital configuration.

$$C_1 \frac{dv_{C_1}}{dt} = i_A F_1 - \frac{v_{C_1}}{R_{C_1}} \tag{5.4}$$

$$C_2 \frac{dv_{C_2}}{dt} = i_A F_2 - \frac{v_{C_2}}{R_{C_2}} \tag{5.5}$$

By superposition property, VSI output voltage v_A is given by the equation (5.6).

$$v_A = v_{C_1} F_1 + v_{C_2} F_2 \tag{5.6}$$

From Figure (5.6b), it is seen that v_A is the coupling variable between VSI and L filter, since v_A is simultaneously sub-circuit *(a)* output and sub-circuit *(b)* input. Voltage Kirchhoff's law is applied to the sub-circuit *(b)*, thus the inductor current equation is given by the equation (5.7).

$$L \frac{di_A}{dt} = -v_A - R_L i_A + v_a \tag{5.7}$$

Assuming that VSI switching is done such that the property given by the equation (5.8) is satisfied, i.e., switches F_1 and F_2 are complementary. The switching function u that indicates the leg state *on-off* is defined in equation (5.9).

$$F_1 + F_2 = 1 \tag{5.8}$$

$$u = \begin{cases} 1 & \text{si } F_1 = on \quad F_2 = off \\ -1 & \text{si } F_1 = off \quad F_2 = on \end{cases} \tag{5.9}$$

Additionally, both F_1 and F_2 are related with u. Then, u in terms of F_1 and u in terms of F_2 are given by equations (5.10) and (5.11), respectively.

$$u = 2F_1 - 1 \tag{5.10}$$

$$u = 1 - 2F_2 \tag{5.11}$$

Replacing equations (5.10) and (5.11) into equations (5.4)-(5.7) and coupling sub-circuits *(a)* and *(b)* in Figure (5.6b), the per phase TLSC SAPF dynamical model is given by equations in (5.12).

$$\begin{aligned} L\frac{di_A}{dt} &= -R_L i_A - \frac{v_{DC}}{2}u - \varepsilon_v + v_a \\ C\frac{dv_{DC}}{dt} &= i_A u - \frac{v_{DC}}{R_o} \\ 2C\frac{d\varepsilon_v}{dt} &= i_A - \frac{2\varepsilon_v}{R_o} \end{aligned} \tag{5.12}$$

Where, $v_{DC} = v_{C_1} - v_{C_2}$ is total DC-link voltage, $2\varepsilon_v = v_{C_1} + v_{C_2}$ is differential voltage between capacitors C_1 and C_2, $C_1 = C_2 = C$, and $R_{C_1} = R_{C_2} = R_o$.

Grid-tied TLSC SAPF dynamical model is derived from equation (5.12). From Figure (5.6a), it is seen that each TLSC SAPF leg is an independent sub-circuit. Thus, voltage Kirchhoff's law is applied to each phase of circuit in Figure (5.6a). Dynamical equations that represent phases a, b, and c are given by equations (5.13), (5.14), and (5.15), respectively.

$$L\frac{di_S^a}{dt} = -v_A - R_L i_S^a + v_{pcc}^a \tag{5.13}$$

$$L\frac{di_S^b}{dt} = -v_B - R_L i_S^b + v_{pcc}^b \tag{5.14}$$

$$L\frac{di_S^c}{dt} = -v_C - R_L i_S^c + v_{pcc}^c \tag{5.15}$$

From Figure (5.6a), it is seen that in the VSI DC side, the capacitor current is composed of the difference between sum of inductor currents per phase and current through parallel resistor R_o that represents the internal DC-link losses. Thus, current Kirchhoff's law is applied to the VSI in Figure (5.6a) and dynamical equations that represent both v_{DC} and ε_v are given by equations (5.16) and (5.17), respectively.

$$C\frac{dv_{DC}}{dt} = i_S^a u^a + i_S^b u^b + i_S^c u^c - \frac{v_{DC}}{R_o} \tag{5.16}$$

$$2C\frac{d\varepsilon_v}{dt} = i_S^a + i_S^b + i_S^c - 2\frac{\varepsilon_v}{R_o} \tag{5.17}$$

Grid-tied TLSC SAPF dynamical model is obtained by unification of equations (5.13)-(5.17) and is given by equations in (5.18).

$$\begin{aligned} L\frac{di_S^{abc}}{dt} &= -R_L i_S^{abc} - \frac{v_{DC}}{2}u^{abc} - \varepsilon_v + v_{pcc}^{abc} \\ C\frac{dv_{DC}}{dt} &= i_S^{abc}u^{abc^T} - \frac{v_{DC}}{R_o} \\ 2C\frac{d\varepsilon_v}{dt} &= i_S^{abc} - \frac{2\varepsilon_v}{R_o} \end{aligned} \tag{5.18}$$

Grid-tied TLSC SAPF dynamical model given by equations in (5.18) is a discontinuous-time model. A continuous-time model for TLSC SAPF must be obtained to facilitate the use of well-established classical control design methods for time-continuous systems.

In TLSC SAPF, average value of all variables (DC-side variables, AC-side variables, and switching functions) are time-dependent even in steady-state. Any periodical signal $f(t)$ may be written as the sum of simple waves mathematically represented by sines and cosines. Applying Fourier transform, the signal $f(t)$ is given by the equation (5.19).

$$f(t) = \frac{1}{T_s}\int_{t_0}^{t_0+T_s} f(\tau)d\tau + \sum_{h=1}^{h=\infty}\left[a_h\cos(h\omega_s t) + b_h\sin(h\omega_s t)\right] \tag{5.19}$$

Where h is $k-th$ harmonic component, $\omega_s = \dfrac{2\pi}{T_s}$, and constant coefficients (a_h, b_h) are given by equations (5.20) and (5.21).

$$a_h = \frac{2}{T_s}\int_{t_0}^{t_0+T_s} f(\tau)\cos(h\omega_s\tau)d\tau \tag{5.20}$$

$$b_h = \frac{2}{T_s}\int_{t_0}^{t_0+T_s} f(\tau)\sin(h\omega_s\tau)d\tau \tag{5.21}$$

Neglecting high frequency components of equation (5.19), the moving average value of $f(t)$ is given by the equation (5.22).

$$\langle f(t)\rangle_0 = \frac{1}{T_s}\int_{t_0}^{t_0+T_s} f(\tau)d\tau \tag{5.22}$$

Unlike the classical average of the signal $f(t)$, term $\langle f(t)\rangle_0$ given by the equation (5.22) is time-dependent due to the fact that the associated time window changes its position on the time axes. However, if signal $f(t)$ is periodic and reaches its steady-state regime, the moving average becomes identical with the classical average.

The fundamental property of the moving average is given by the equation (5.23); which is, time derivation of $\langle f(t)\rangle_0$ is the moving average of time derivation of $f(t)$.

$$\left\langle \frac{d}{dt} f(t) \right\rangle_0 = \frac{d}{dt}\langle f(t)\rangle_0 \tag{5.23}$$

Property given by the equation (5.23) is applied to equations in (5.18). Thus, TLSC SAPF Averaged Model (AM) is given by equations in (5.24).

$$\begin{aligned} L\frac{d}{dt}\langle i_S^{abc}\rangle_0 &= -R_L\langle i_S^{abc}\rangle_0 - \frac{\langle v_{DC}\rangle_0}{2}\langle u^{abc}\rangle_0 - \langle \varepsilon_v\rangle_0 + \langle v_{pcc}^{abc}\rangle_0 \\ C\frac{d}{dt}\langle v_{DC}\rangle_0 &= \langle i_S^{abc}\rangle_0\langle u^{abc^T}\rangle_0 - \frac{\langle v_{DC}\rangle_0}{R_o} \\ 2C\frac{d}{dt}\langle \varepsilon_v\rangle &= \langle i_S^{abc}\rangle_0 - \frac{2\langle \varepsilon_v\rangle_0}{R_o} \end{aligned} \tag{5.24}$$

TLSC SAPF AM given by equations in (5.24) has the following requirements to represent the system: *(a)* signals i_S^{abc}, u^{abc}, and v_{pcc}^{abc} must be sinusoids at the grid fundamental frequency f_s; *(b)* signals v_{DC} and ε_v reach a constant value in its steady-state regime; *(c)* switching frequency f_{sw} must be high enough that f_s. An estimate is that the system is represented by equations in (5.24) with an error $< 5\%$ if $f_{sw} > 50 f_s$ [114].

As a result, moving average $\langle u^{abc}\rangle_0$ of the switching function u^{abc} becomes in a continuous-time sinusoidal function that takes values in the range $[0, 1]$. Hence, TLSC SAPF AM given by equations in (5.24) is a continuous-time dynamical model.

Henceforth, for sake of simplicity, variables i_S^{abc}, u^{abc}, v_{pcc}^{abc}, v_{DC}, and ε_v will be refereed as moving average variables $\langle i_S^{abc}\rangle_0$, $\langle u^{abc}\rangle_0$, $\langle v_{pcc}^{abc}\rangle_0$, $\langle v_{DC}\rangle_0$, and $\langle \varepsilon_v\rangle_0$, respectively.

Steady-state solutions of the model given by equations in (5.24) are time-varying. It is well known that the dynamical analysis and control design methods for time-varying systems are more complex than time-invariant systems [115].

A sinusoidal AC variable is a rotating vector (phasor) with pulsation ω. dq transformation is applied to obtain active and reactive components of a three-phase phasor. dq components are obtained by projecting phasors on axes of a frame synchronously

rotating with ω. The active component (on abscissa axis) is denoted by subscript d, whereas the reactive component (on ordinate axis) is denoted by subscript q. In the grid unbalanced condition, $dq0$ transformation is applied to lead with grid zero sequence components. $dq0$ components are DC quantities in steady-state regime for system balanced condition. In unbalanced system condition, $dq0$ components are composed of a DC quantity and an oscillatory part with twice the grid frequency [116].

Transformation matrix from the three-phase stationary abc reference-frame to the synchronous $dq0$ rotating reference-frame is given by the equation (5.25). Where θ is synchronization signal lag.

$$T_{abc\to dq0} = \frac{2}{3}\begin{bmatrix} \sin(\omega t+\theta) & \sin\left(\omega t-\frac{2\pi}{3}+\theta\right) & \sin\left(\omega t-\frac{2\pi}{3}+\theta\right) \\ \cos(\omega t+\theta) & \cos\left(\omega t-\frac{2\pi}{3}+\theta\right) & \cos\left(\omega t-\frac{2\pi}{3}+\theta\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{5.25}$$

Two useful properties of $dq0$ transformation given by the equation (5.25) are given by equations (5.26) and (5.27).

$$[T_{abc\to dq0}]^{-1} = [T_{abc\to dq0}]^{T} \tag{5.26}$$

$$[T_{abc\to dq0}]\frac{d}{dt}[T_{abc\to dq0}]^{T} = \omega\begin{bmatrix} 0 & -1 & 0 \\ 1 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \tag{5.27}$$

Applying $dq0$ transformation given by the equation (5.25) to TLSC SAPF AM given by equations in (5.24), TLSC SAPF synchronous $dq0$ rotating reference-frame AM is given by equations in (5.28).

$$\begin{aligned} L\left[\begin{bmatrix} -\omega_{i_S}^{q} \\ \omega_{i_S}^{q} \\ 0 \end{bmatrix} + \frac{di_S^{dq0}}{dt}\right] &= -R_L i_S^{dq0} - \frac{v_{DC}}{2}u^{dq0} - \begin{bmatrix} 0 \\ 0 \\ \sqrt{3} \end{bmatrix}\varepsilon_v + v_{pcc}^{dq0} \\ C\frac{dv_{DC}}{dt} &= i_S^{dq0}u^{dq0^T} - \frac{v_{DC}}{R_o} \\ 2C\frac{d\varepsilon_v}{dt} &= \sqrt{3}i_S^0 - \frac{2\varepsilon_v}{R_o} \end{aligned} \tag{5.28}$$

Circuital realization of both TLSC SAPF AM given by equations in (5.24) and TLSC SAPF synchronous $dq0$ rotating reference-frame AM given by equations in (5.28) are showed in Figures (5.7) - (5.8), respectively.

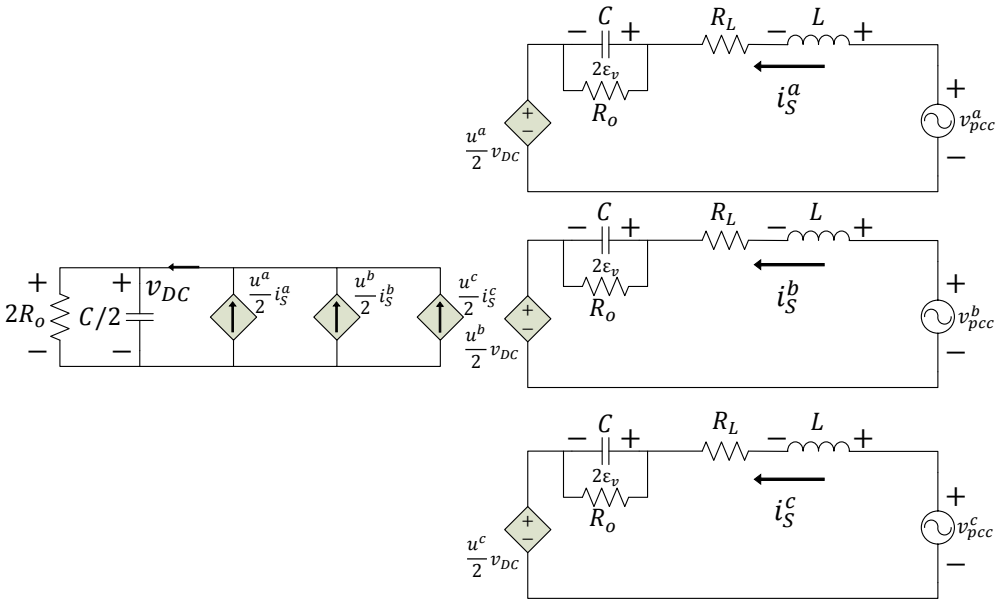

FIGURE 5.7: Circuital realization of the TLSC SAPF AM.

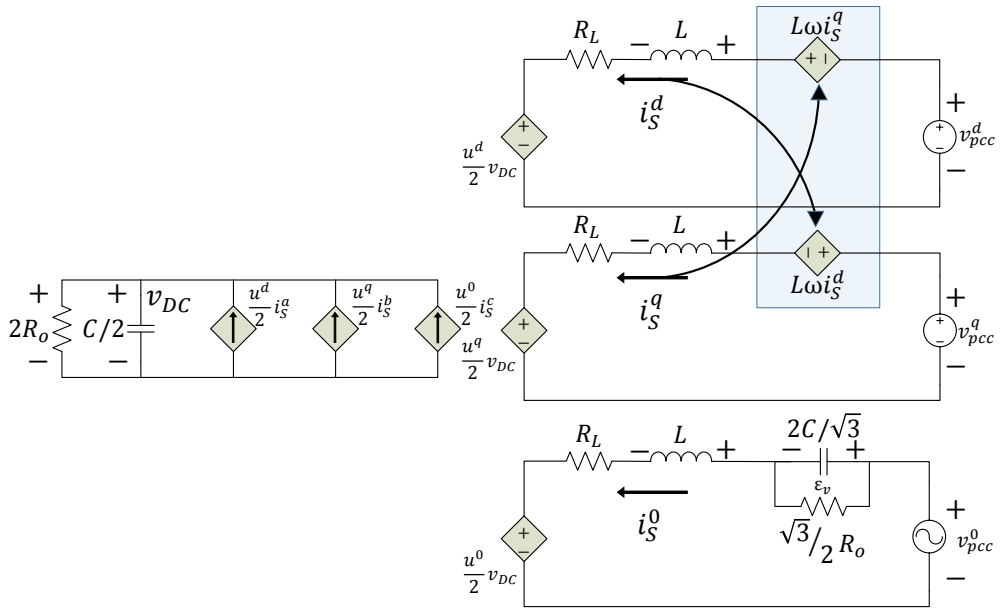

FIGURE 5.8: Circuital realization of the TLSC SAPF synchronous $dq0$ rotating reference-frame AM.

5.2.4 Small-Signal Models

TLSC SAPF small-signal synchronous $dq0$ rotating reference-frame AM is given by the equation (5.31) and it was obtained as follow: *(a)* taking the TLSC SAPF synchronous $dq0$ rotating reference-frame AM given by equations in (5.28) and *(b)* applying the state-space realization given by the equation (5.29). Where state variables are $x = \left[i_S^d, i_S^q, i_S^0, v_{DC}, \varepsilon_v\right]^T$; input variables are $u = \left[u^d, u^q, u^0, v_{pcc}^d, v_{pcc}^q, v_{pcc}^0\right]^T$; and output variables are $y = \left[i_S^d, i_S^q, i_S^0, v_{DC}, \varepsilon_v\right]^T$.

$$\begin{aligned} \dot{x} &= Ax + Bu \\ y &= Cx + Du \end{aligned} \tag{5.29}$$

where

$$\begin{aligned} A &= \left(\frac{\partial f\left(x,u\right)}{\partial x}\right)_{x_e,u_e} & B &= \left(\frac{\partial f\left(x,u\right)}{\partial u}\right)_{x_e,u_e} \\ C &= \left(\frac{\partial h\left(x,u\right)}{\partial x}\right)_{x_e,u_e} & D &= \left(\frac{\partial h\left(x,u\right)}{\partial u}\right)_{x_e,u_e} \end{aligned} \tag{5.30}$$

Subscript e in (5.30) refers to both state variables and input variables in their rated values.

$$\begin{bmatrix} \dot{i}_L^d \\ \dot{i}_L^q \\ \dot{i}_L^0 \\ \dot{v}_{DC} \\ \dot{\varepsilon}_v \end{bmatrix} = \begin{bmatrix} -\frac{R_L}{L} & \omega & 0 & -\frac{U^d}{2L} & 0 \\ -\omega & -\frac{R_L}{L} & 0 & -\frac{U^q}{2L} & 0 \\ 0 & 0 & -\frac{R_L}{L} & -\frac{U^0}{2L} & -\frac{\sqrt{3}}{L} \\ \frac{U^d}{C} & \frac{U^q}{C} & \frac{U^0}{C} & -\frac{1}{R_o C} & 0 \\ 0 & 0 & \frac{\sqrt{3}}{2C} & 0 & -\frac{1}{R_o C} \end{bmatrix} \begin{bmatrix} i_S^d \\ i_S^q \\ i_S^0 \\ v_{DC} \\ \varepsilon_v \end{bmatrix} + \begin{bmatrix} -\frac{V_{DC}}{2L} & 0 & 0 & \frac{1}{L} & 0 & 0 \\ 0 & -\frac{V_{DC}}{L} & 0 & 0 & \frac{1}{L} & 0 \\ 0 & 0 & -\frac{V_{DC}}{L} & 0 & 0 & \frac{1}{L} \\ \frac{I_S^d}{C} & \frac{I_S^q}{C} & \frac{I_S^0}{C} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} u^d \\ u^q \\ u^0 \\ v_{pcc}^d \\ v_{pcc}^q \\ v_{pcc}^0 \end{bmatrix} \tag{5.31}$$

Capital letters in equation (5.31) indicate the steady-state average values of both input and output variables.

In balanced system condition, system 0 components are zero, i.e., $v_{pcc}^0 = 0$, $i_S^0 = 0$, and $u^0 = 0$. Thus, coupling between dq and 0 components can be neglected. Therefore, TLSC SAPF small-signal synchronous $dq0$ rotating reference-frame AM given by the equation (5.31) is divided in: *(a)* TLSC SAPF small-signal synchronous dq rotating reference-frame AM given by the equation (5.32), and *(b)* TLSC SAPF small-signal synchronous 0 sequence rotating reference-frame AM given by the equation (5.33).

$$\begin{bmatrix} \dot{i}_L^d \\ \dot{i}_L^q \\ \dot{v}_{DC} \end{bmatrix} = \begin{bmatrix} -\frac{R_L}{L} & \omega & -\frac{U^d}{2L} \\ -\omega & -\frac{R_L}{L} & -\frac{U^q}{2L} \\ \frac{U^d}{C} & \frac{U^q}{C} & -\frac{1}{R_o C} \end{bmatrix} \begin{bmatrix} i_S^d \\ i_S^q \\ v_{DC} \end{bmatrix} + \begin{bmatrix} -\frac{V_{DC}}{2L} & 0 & \frac{1}{L} & 0 \\ 0 & -\frac{V_{DC}}{L} & 0 & \frac{1}{L} \\ \frac{I_S^d}{C} & \frac{I_S^q}{C} & 0 & 0 \end{bmatrix} \begin{bmatrix} u^d \\ u^q \\ v_{pcc}^d \\ v_{pcc}^q \end{bmatrix} \tag{5.32}$$

$$\begin{bmatrix} \dot{i}_L^0 \\ \dot{\varepsilon}_v \end{bmatrix} = \begin{bmatrix} -\frac{R_L}{L} & -\frac{\sqrt{3}}{L} \\ \frac{\sqrt{3}}{2C} & -\frac{1}{R_o C} \end{bmatrix} \begin{bmatrix} i_S^0 \\ \varepsilon_v \end{bmatrix} + \begin{bmatrix} -\frac{V_{DC}}{L} & \frac{1}{L} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} u^0 \\ v_{pcc}^0 \end{bmatrix} \tag{5.33}$$

Equation (5.34) is the common realization that allows to relate the state-space model with system transfer functions.

$$G(s) = \frac{1}{det(sI - A)} C \left[adj(sI - A) \right] B + D \tag{5.34}$$

Due to the fact that system outputs are system states, matrices C in models given by equations (5.32) and (5.33) are a 3×3 identity matrix and a 2×2 identity matrix, respectively. Matrices D in models given by equations (5.32) and (5.33) are a 4×3 matrix of zeros and a 2×2 matrix of zeros, respectively.

Applying realization given by the equation (5.29) to equation (5.32), transfer functions for TLSC SAPF small-signal synchronous dq rotating reference-frame AM are given by equations (5.35), (5.36), and (5.37) for i_S^d, i_S^q, and v_{DC}, respectively.

$$G_{i_S^d}(s) = \frac{\begin{bmatrix} \begin{bmatrix} -2CLR_oV_{DC}s^2 + (-2CR_oR_LV_{DC} - 2I_S^dLR_oU^d - 2LV_{DC})s \\ -2I_S^dLR_oU^q\omega - 2I_S^dR_oR_LU^d - R_o(U^q)^2V_{DC} - 2R_LV_{DC} \end{bmatrix} \\ \begin{bmatrix} (-2CLR_oV_{DC}\omega - 2I_S^qLR_oU^d)s - 2I_S^qLR_oU^q\omega \\ -2I_S^qR_oR_LU^d + R_oU^dU^qV_{DC} - 2L\omega V_{DC} \end{bmatrix} \\ 2(2CLR_os^2 + (2CR_oR_L + 2L)s + R_o(U^q)^2 + 2R_L) \\ 2(2CLR_o\omega s - R_oU^dU^q + 2\omega L) \end{bmatrix}}{\begin{bmatrix} 4CL^2R_os^3 + (8CLR_oR_L + 4L^2)s^2 + (4CL^2R_o\omega^2 + 4CR_oR_L^2 + 2LR_o(U^d)^2 \\ +2LR_o(U^q)^2 + 8LR_L)s + 4\omega^2L^2 + 2R_oR_L(U^d)^2 + 2R_oR_L(U^q)^2 + 4R_L^2 \end{bmatrix}} \tag{5.35}$$

$$G_{i_S^q}(s) = \frac{\begin{bmatrix} \begin{bmatrix} (2CLR_oV_{DC}\omega - 2I_S^dLR_oU^q)s + 2I_S^dLR_oU^d\omega - 2I_S^dR_oR_LU^q \\ +R_oU^dU^qV_{DC} + 2L\omega V_{DC} \end{bmatrix} \\ \begin{bmatrix} -2CLR_oV_{DC}s^2 + (-2CR_oR_LV_{DC} - 2I_S^qLR_oU^q - 2LV_{DC})s \\ +2I_S^qLR_oU^d\omega - 2I_S^qR_oR_LU^q - R_o(U^d)^2V_{DC} - 2R_LV_{DC} \end{bmatrix} \\ 2(-2CLR_o\omega s - R_oU^dU^q - 2\omega L) \\ 2(2CLR_os^2 + (2CR_oR_L + 2L)s + (U^d)^2R_o + 2R_L) \end{bmatrix}}{\begin{bmatrix} 4CL^2R_os^3 + (8CLR_oR_L + 4L^2)s^2 + (4CL^2R_o\omega^2 + 4CR_oR_L^2 + 2LR_o(U^d)^2 \\ +2LR_o(U^q)^2 + 8LR_L)s + 4\omega^2L^2 + 2R_oR_L(U^d)^2 + 2R_oR_L(U^q)^2 + 4R_L^2 \end{bmatrix}} \tag{5.36}$$

$$G_{v_{DC}}(s) = \frac{\begin{bmatrix} \begin{bmatrix} 2(2I_S^dL^2R_os^2 + (4I_S^dLR_L - LU^dV_{DC})R_os \\ +(2I_S^dL^2\omega^2 + LU^qV_{DC}\omega + 2I_S^dR_L^2 - R_LU^dV_{DC})R_o) \end{bmatrix} \\ \begin{bmatrix} 2(2I_S^qL^2R_os^2 + (4I_S^qLR_L - LU^qV_{DC})R_os \\ +(2I_S^qL^2\omega^2 - LU^dV_{DC}\omega + 2I_S^qR_L^2 - R_LU^qV_{DC})R_o) \end{bmatrix} \\ 2(2LR_oU^ds + (2(-LU^q\omega + R_LU^d))R_o) \\ 2(2LR_oU^qs + (2(\omega U^dL + R_LU^q)) * R_o) \end{bmatrix}}{\begin{bmatrix} 4CL^2R_os^3 + (8CLR_oR_L + 4L^2)s^2 + (4CL^2R_o\omega^2 + 4CR_oR_L^2 + 2LR_o(U^d)^2 \\ +2LR_o(U^q)^2 + 8LR_L)s + 4\omega^2L^2 + 2R_oR_L(U^d)^2 + 2R_oR_L(U^q)^2 + 4R_L^2 \end{bmatrix}} \tag{5.37}$$

Applying realization given by the equation (5.29) to equation (5.33), transfer functions for TLSC SAPF small-signal synchronous 0 sequence rotating reference-frame AM are given by equations (5.38) and (5.39) for i_S^0 and ε_v, respectively.

$$G_{i_S^0} = \frac{\begin{bmatrix} -CR_oV_{DC}s - V_{DC} \\ 2CR_os + 2 \end{bmatrix}}{2CLR_os^2 + (2CR_oR_L + 2L)s + 3R_o + 2R_L} \tag{5.38}$$

$$G_{\varepsilon_v} = \frac{\begin{bmatrix} \frac{\sqrt{3}}{2}V_{DC}R_o \\ \sqrt{3}R_o \end{bmatrix}}{2CLR_os^2 + (2CR_oR_L + 2L)s + 3R_o + 2R_L} \tag{5.39}$$

Capital letters in equations (5.35)-(5.39) indicate the rated values of both states and inputs variables.

5.3 Passive Elements Design

The second stage in proposed design procedure of PECs is passive elements design, which is composed by steps 7 and 8. The aim of this stage is to find suitable values for passive elements (inductor, capacitor, and resistors) such that system operating requirements are satisfied taking into account inherent dynamical system behavior. This section is composed of following subsections: *(1)* systems constraints, *(2)* passive elements selection, and *(3)* system frequency response verification.

5.3.1 System Constraints

Once that the system mathematical model is obtained, following sub-steps are carried out to determine suitable passive elements (C and L) boundaries which satisfy design requirements: *(1)* steady-state analysis, *(2)* currents and voltages waveforms analysis, *(3)* losses effect and efficiency analysis, and *(4)* zeros-based system dynamical analysis.

5.3.1.1 Steady-State Analysis

First sub-step is the steady-state analysis, which allows to obtain expressions for average rated values of dq model variables as function of known system inputs and parameters. Setting to zero model given by equations in (5.32), the steady-state model is given by equations (5.40)-(5.42).

$$I_S^d = \frac{1}{2R_L}\left[V_{pcc}^d \pm \sqrt{(V_{pcc}^d)^2 - 4R_L\left(R_L(I_S^q)^2 + \frac{V_{DC}^2}{2R_o}\right)}\right] \tag{5.40}$$

$$U^d = \frac{1}{I_S^d}\left(\frac{V_{DC}}{R_o} + \frac{2I_S^q}{V_{DC}}(L\omega I_S^d + R_L I_S^q)\right) \tag{5.41}$$

$$U^q = -\frac{2}{V_{DC}}(L\omega I_S^d + R_L I_S^q) \tag{5.42}$$

Capital letters indicate the steady-state average value, thus: V_{pcc}^d is direct component of the grid mains voltage, I_S^d is the TLSC SAPF direct current component, I_S^q is TLSC SAPF quadrature current component, U^d is modulation signal direct component, U^q is modulation signal quadrature component, and V_{DC} is DC-link voltage. I_S^d is necessary active current to keep the DC-link voltage level in its rated value and it is supplied by the grid mains supply.

The steady-state model given by equations (5.40)-(5.42) is an equation system composed of three-equations four-unknown variables. Further, equation (5.40) has two solutions.

TLSC SAPF function in this work is to supply the load inefficient currents while maintaining the DC-link voltage in its rated value. Accordingly, I_S^d must be equal to requested current to maintain DC-link level voltage and supply VSI internal losses. While I_S^q must be equal to requested load current due to the load inefficiencies.

i_S^q can be computed measuring system currents. Assuming that the system main supply only provides the fundamental positive-sequence active power (P_1^+) to the load, i.e., from the system main supply point of view, the load is fully efficient [105]. The required load current i_L^{abc} is given by the equation (5.43). Applying $dq0$ transformation given by the equation (5.25) to equation (5.43), i_L^{dq0} is given by equations (5.44) and (5.45) [116].

$$i_L^{abc} = \sqrt{2}\Re\left\{\tilde{I}_L^{abc}e^{j\omega t}\right\} = \sqrt{2}\Re\left\{A\tilde{I}_L^{120}e^{j\omega t}\right\} \tag{5.43}$$

Where $\tilde{I}_L^{abc}$ and $\tilde{I}_L^{120}$ are three-phase phasor vectors and A is the standard Fortescue sequence component decomposition.

$$i_L^{dq} = \sqrt{2}\tilde{I}_1 e^{-j(\theta-\omega t)} + \sqrt{2}\tilde{I}_2^* e^{-j(\theta+\omega t)} \tag{5.44}$$

$$i_L^0 = \Re\left\{\sqrt{2}\tilde{I}_0\right\} \tag{5.45}$$

Where $i_L^{dq} = i_L^d + j i_L^q = \Re\left\{i_L^{abc}\right\rangle + \Im\left\{i_L^{abc}\right\}$, and complex variables $\sqrt{2}\tilde{I}_1$, $\sqrt{2}\tilde{I}_2^*$, and $\sqrt{2}\tilde{I}_0$ are directly related to positive, negative, and zero sequence component phasors, respectively. In equation (5.44), $\sqrt{2}\tilde{I}_1$ correspond to i_L^{dq} in the synchronous dq rotating reference-frame ($T_{abc\to dq0}(\omega t)$), when only the positive sequence is present. Similarly, $\sqrt{2}\tilde{I}_2^*$ correspond to i_L^{dq} in the rotating reference-frame ($T_{abc\to dq0}(-\omega t)$), when only the negative sequence is present.

Accordingly with TLSC SAPF function, i_S^q is given by the equation (5.46).

$$i_S^q = -i_L^q = -\Im\left\{i_L^{abc}\right\} \tag{5.46}$$

In steady-state, $i_S^q = I_S^q$. Furthermore, with I_S^q given by the equation (5.46), equation system given by equations (5.40)-(5.42) has three-equations three-unknown variables, where $\min\left\{|I_S^d|\right\}$ must be selected.

5.3.1.2 Currents and Voltages waveform Analysis

The second sub-step is currents and voltages waveform analysis. The waveforms analysis is carried out to determine constraint equations for both L and C. Constraint equations must be suitable to choose L and C such that operating requirements are satisfied.

L Filter

This subsection is based on ideas in the work presented by [117]. Figure (5.9) shows i_S^a waveform corresponding to single-phase TLSC SAPF circuit showed in Figure (5.6b) due to F_1 and F_2 *on-off* switching, where I_L^a is the average value of i_S^a.

Points 1, 2, and 3 are defined over i_S^a curve. If F_1 is *on* and F_2 is *off* (subinterval 1 - 2), i_S^a increases linearly with the slope given by the equation (5.47). If F_1 is *off* and F_2 is *on* (subinterval 2 - 3), i_S^a decreases linearly with the slope given by the equation (5.48). F_1 and F_2 *on-off* switching process is cyclic along time.

$$\frac{di_S^{a^+}}{dt} = \frac{1}{L}\left(V_a - V_{C_1} - R_L I_S^a\right) \tag{5.47}$$

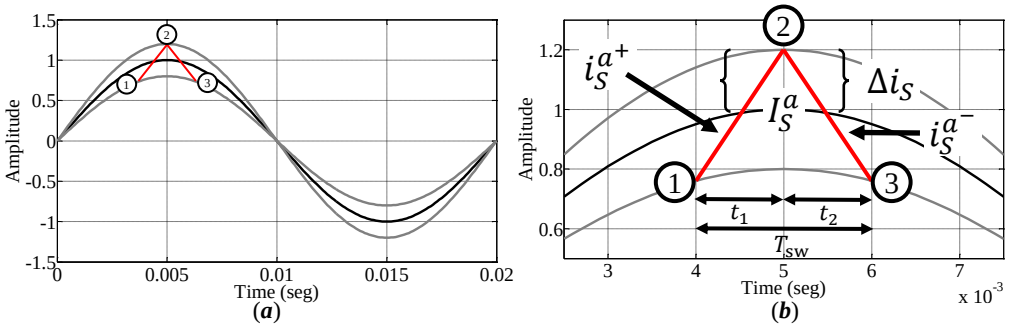

FIGURE 5.9: i_S^a and voltage inductor v_S^a waveforms corresponding to single-phase TLSC SAPF.

$$\frac{di_S^{a^-}}{dt} = \frac{1}{L}\left(V_a - V_{C_2} - R_L I_S^a\right) \tag{5.48}$$

In steady-state, condition given by the equation (5.49) is satisfied.

$$\frac{di_S^{a^+}}{dt} + \frac{di_S^{a^-}}{dt} = 0 \tag{5.49}$$

From Figure (5.9b) is seen that points 1, 2, and 3 are a triangle, where line equations (5.50) and (5.51) are satisfied.

$$\frac{di_S^{a^+}}{dt}t_1 - \frac{dI_S^a}{dt}t_1 = 2\Delta i_S^a \tag{5.50}$$

$$\frac{di_S^{a^-}}{dt}t_2 - \frac{dI_S^a}{dt}t_2 = -2\Delta i_S^a \tag{5.51}$$

Where Δi_S^a is distance between I_L^a and i_L^a peak magnitude, and t_1 and t_2 ($t_1 + t_2 = T_{sw}$) corresponding to subinterval 1 - 2 and subinterval 2 - 3, respectively.

Equations (5.50) and (5.51) are combined as follow: *(a)* equation (5.52) is equal to equation (5.50) plus equation (5.51), *(b)* equation (5.53) is equal to equation (5.50) less equation (5.51).

$$\frac{di_S^{a^+}}{dt}t_1 + \frac{di_S^{a^-}}{dt}t_2 - \frac{dI_S^a}{dt}T_{sw} = 0 \tag{5.52}$$

$$\frac{di_S^{a^+}}{dt}T_{sw} - \frac{dI_S^a}{dt}(t_1 - t_2) = 4\Delta i_S^a \tag{5.53}$$

Replacing equations (5.47) and (5.48) into equation (5.53), equation (5.54) is obtained.

$$(t_1 - t_2) = \frac{2L}{V_{DC}}\left[\frac{V_a - R_L I_S^a}{L} - \frac{dI_S^a}{dt}\right]T_{sw} \tag{5.54}$$

Replacing equations (5.47), (5.48), and (5.53) into equation (5.54), equation (5.55) is obtained.

$$\Delta i_S^a = \frac{V_{DC}}{8L}\left[1 - \frac{4L^2}{V_{DC}^2}\left(\frac{V_a - R_L I_S^a}{L} + \frac{dI_S^a}{dt}\right)^2\right]T_{sw} \tag{5.55}$$

The equation (5.55) can be solved for L getting a lower boundary for this parameter when the maximum admissible inductor current ripple $\max\{\Delta i_S^a\}$ is given.

DC-link Capacitor

Figure (5.10) shows both v_{DC_1} and v_{DC_2} waveforms for an unit step change in u^d. It is seen that v_{DC_1} and v_{DC_2} change their steady-state voltage value. Energy stored by capacitor C_1 is given by the equation (5.56) and energy variation is given by the equation (5.57).

$$w_{DC_1} = \frac{1}{2}C_1 v_{DC_1}^2 \tag{5.56}$$

$$\Delta w_{DC_1} = \frac{1}{2}C_1\left(v_{DC_{1_{ref}}}^2 - v_{DC_1}^2\right) \tag{5.57}$$

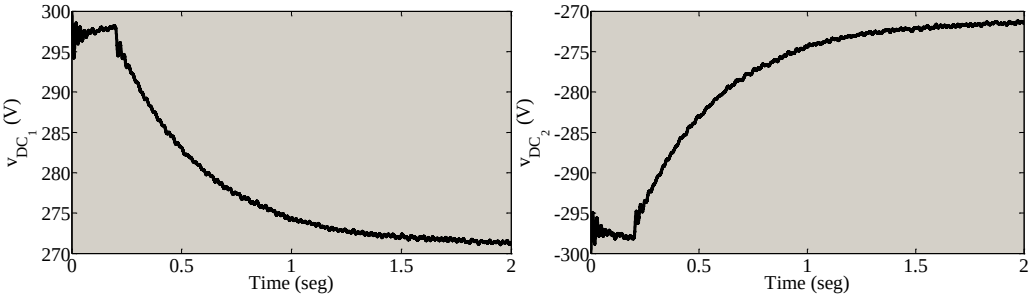

FIGURE 5.10: v_{DC_1} and v_{DC_2} waveforms for an unit step change in u^d.

Where $v_{DC_{1_{ref}}}$ is capacitor C_1 steady-state value. v_{DC_1} variation can be seen as $\alpha v_{DC_{1_{ref}}}$ and equation (5.57) can be rewritten as equation (5.58).

$$\Delta w_{DC_1} = \frac{1}{2} C_1 (1 - \alpha^2) v^2_{DC_{1_{ref}}} \tag{5.58}$$

An approximation for a DC-link power variation $\Delta P_{DC-link}$ is given by the equation (5.59).

$$\Delta P_{DC-link} \approx \frac{\Delta w}{\Delta t} \tag{5.59}$$

$\Delta P_{DC-link}$ can be taken as $k|\Delta S_{out}|$, where S_{out} is TLSC SAPF output power and k is the power factor supplied by TLSC SAPF to the load. Thus, the DC-link voltage variation can be limited if the selected capacitor satisfies condition given by the equation (5.60).

$$C = \frac{2NT_s k|\Delta S_{out}|}{(1 - \alpha^2) v^2_{DC_{ref}}} \tag{5.60}$$

Where N is number of cycles in which $v_{DC_{ref}}$ reaches v_{DC}.

5.3.1.3 Losses Effect and Efficiency Analysis

The third sub-step is losses effect and efficiency analysis. Figure (5.11a) shows the per phase TLSC SAPF circuital configuration and Figures (5.11b) - (5.11c) show the two per phase TLSC SAPF configurations due to switching of F_1 and F_2 *on-off*.

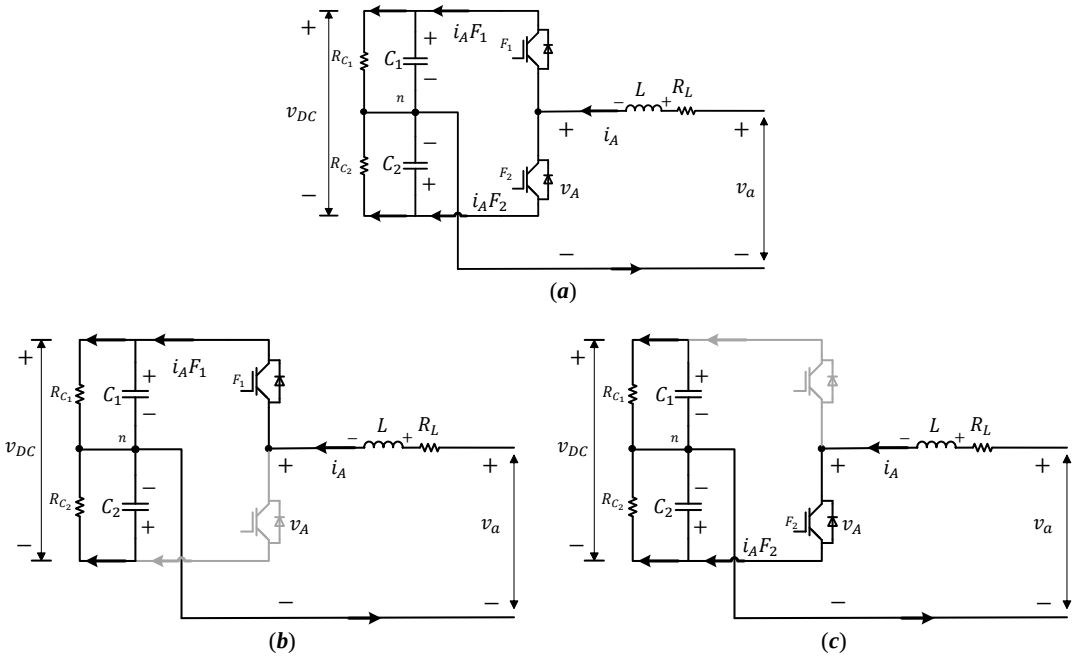

FIGURE 5.11: *(a)* The per phase TLSC SAPF circuital configuration. *(b)* $F_1 = on$, $F_2 = off$. *(c)* $F_1 = off$, $F_2 = on$.

Due to the fact that the TLSC SAPF is a differential connection of three Buck DC-DC converters, the per phase efficiency analysis can be carried out as efficiency analysis of the Buck DC-DC converter.

From Figure (5.11a) is seen that, the VSI output voltage v_A is given by the equation (5.61).

$$v_A = v_{C_1} D + v_{C_2}(1 - D) \tag{5.61}$$

Where D is the per phase TLSC SAPF duty cycle. If the total DC-link voltage is $v_{DC} = v_{C_1} - v_{C_2}$ and the differential voltage between capacitors C_1 and C_2 is $\varepsilon_v = v_{C_1} + v_{C_2}$, v_A as function of v_{DC} and ε_v is given by the equation (5.62).

$$v_A = \frac{v_{DC}}{2}(2D - 1) + \varepsilon_v \tag{5.62}$$

Equation (5.62) indicates that for the TLSC VSI, the maximum possible v_A value is half of the total DC-link voltage.

Taking into account the inductor Equivalent Series Resistance (ESR) R_L, TLSC SAPF Equilibrium Conversion Ratio $M(D)$ is given by the equation (5.63).

$$M(D) = \frac{V_a}{V_{DC}} = \left(\frac{1}{1 + \frac{R_L}{|Z_{load}|}} \right) \frac{(2D-1)}{2} \tag{5.63}$$

Where $|Z_{load}|$ is the load equivalent impedance.

From Figure (5.11a), per phase TLSC SAPF input power P_{in} and output power P_{out} are given by equations (5.64) and (5.66), respectively.

$$P_{in} = \frac{V_{DC}}{2} I_{DC} \tag{5.64}$$

$$\tag{5.65}$$

$$S_{out} = \frac{(V_a)^2}{Z_{load}} \tag{5.66}$$

Figure (5.12a) shows DC-link current i_{DC}. Two points were defined over i_{DC} curve. Figure (5.12b) is a zoom of the line between points 1 and 2 from Figure (5.12a). From Figure (5.12b), the line equation given by (5.67) is obtained.

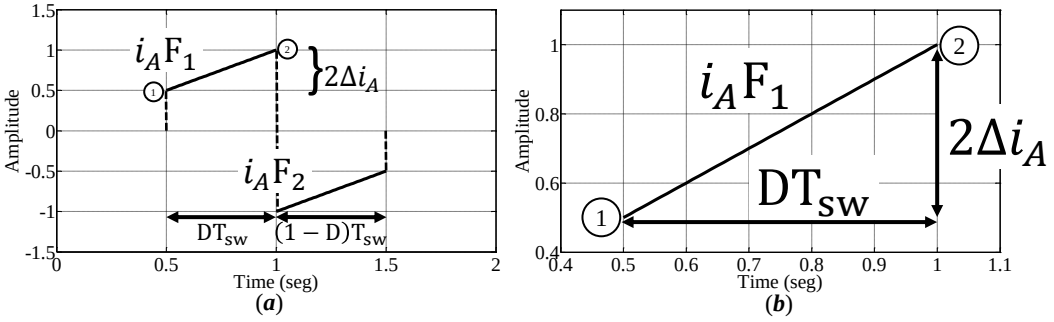

FIGURE 5.12: *(a)* the DC-link current i_{DC}. *(b)* the zoom of the line between points 1 and 2.

$$i_A = \frac{2\Delta i_A}{DT_{sw}} t + (I_A - \Delta i_A) \tag{5.67}$$

Average value of i_{DC_1} is given by the equation (5.68).

$$I_{DC_1} = \frac{1}{T_{sw}} \int_0^{DT_{sw}} i_A dt \tag{5.68}$$

Solving equation (5.68), equation (5.69) is obtained.

$$\begin{aligned} I_{DC_1} &= \frac{1}{T_{sw}} \left[\frac{\Delta i_A}{t_1} t^2 + (I_A - \Delta i_A)\, t \right]_0^{DT_{sw}} \\ &= I_A D \end{aligned} \tag{5.69}$$

Likewise, average value of i_{DC_2} is given by the equation (5.70).

$$I_{DC_2} = I_A(1 - D) \tag{5.70}$$

Furthermore, DC-link average current I_{DC} is given by the equation (5.71).

$$\begin{aligned} I_{DC} &= I_A(2D - 1) \\ &= \left| \frac{V_a}{Z_{load}} \right| (2D - 1) \end{aligned} \tag{5.71}$$

Replacing equation (5.71) into equation (5.64), the per phase TLSC SAPF efficiency is given by the equation (5.72).

$$\begin{aligned} \eta &= \frac{|S_{out}|}{P_{in}} \\ &= \frac{\left| \frac{(V_a)^2}{Z_{load}} \right|}{\frac{V_{DC}}{2} \left| \frac{V_a}{Z_{load}} \right| (2D - 1)} \\ &= \left(\frac{1}{1 + \frac{R_L}{|Z_{load}|}} \right) \end{aligned} \tag{5.72}$$

Equation (5.72) does not depend of D, this is the reason why D can be sinusoidally varied about quiescent operating point $D = 0.5$ without affecting converter efficiency.

Efficiency analysis carried out does not consider the conduction and semiconductors switching power losses. However, several works to estimate both conduction and switching power losses have been reported [118], [119], [120], [121]. Based on reported works, an alternative to include conduction and switching power losses is to add a series resistance with inductor ESR such that an equivalent power to power losses is consumed. Thus, equation (5.72) can be appropriately represent the per phase TLSC SAPF efficiency. If TLSC SAPF phases are composed of identical L filters, (5.72) is a good TLSC SAPF efficiency approximation.

Some plots of equations (5.63) and (5.72) are showed in Figure (5.13) for several values of $\alpha_L = \dfrac{R_L}{|Z_{load}|}$ ratio in order to see how losses affect both $M(D)$ and η.

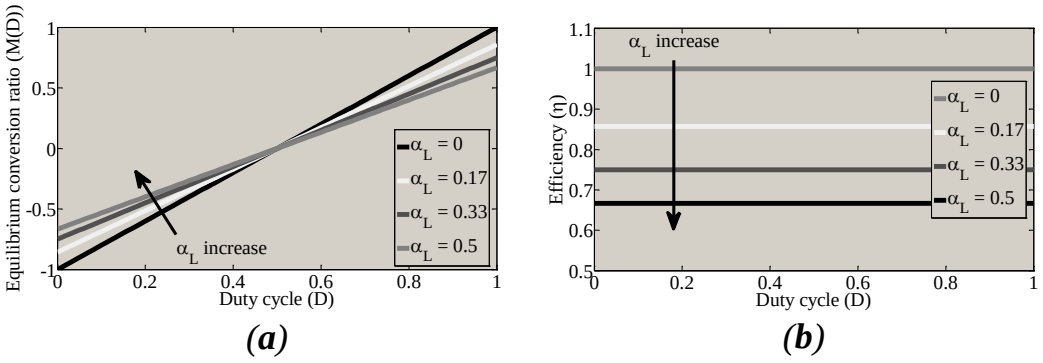

FIGURE 5.13: *(a)* The equilibrium conversion ratio ($M(D)$) v.s. the duty cycle D. *(b)* Efficiency η v.s. the duty cycle D.

5.3.1.4 Zeros-Based Dynamical System Analysis

The fourth and last sub-step is to evaluate the TLSC SAPF zeros location. Zeros location set some dynamical properties, such as overshoot, undershoot (non-minimum phase behavior), and damping.

System zeros are determined by selection of the system inputs and outputs. Zeros location is related to system performance limitations, additional overshoot in unit step response, and undershoot magnitude due to the system non-minimum phase behavior associated with Right Half Plane (RHP) zeros (unstable zeros)[83].

Due to the fact that zeros modify the system natural modes, PEC design procedure must take into account the zeros location such that system dynamical properties as both large

currents and voltages overshoots, or both sharp currents or voltages undershoots are avoided. Large currents or voltage overshoots can cause converter failures. Otherwise, sharp currents or voltages undershoots are undesired behavior when classical control structures are employed due to tracking limitations with feedback systems [84], [85]. Accordingly, zeros location analysis objective is to find values for passive elements such that RHP zeros are avoided or that their impact are minimized.

In TLSC SAPF application, u^d, u^q, and u^0 are control inputs; v_{pcc}^d, v_{pcc}^q, and v_{pcc}^0 are disturbances; and i_S^d, i_S^q, and i_S^0 are system outputs. Thus, u^d, u^q, and u^0 variations effect is of primary importance over i_S^d, i_S^q, and i_S^0. Hence, the $dq0$-switching-functions-to-$dq0$-inductor-currents transfer functions $G_{i_S^d}$, $G_{i_S^q}$, and $G_{i_S^0}$ are studied, i.e., characteristics of [Eqs. 36, 37, and 39] are studied.

by the equation (5.35), the numerator of $G_{i_S^d u^d}$ is given by the equation (5.73).

$$num(G_{i_S^d u^d}) = \begin{bmatrix} -2CLR_oV_{DC}s^2 + (-2CR_oR_LV_{DC} - 2I_S^dLR_oU^d - 2LV_{DC})s \\ -2I_S^dLR_oU^q\omega - 2I_S^dR_oR_LU^d - R_o(U^q)^2V_{DC} - 2R_LV_{DC} \end{bmatrix} \tag{5.73}$$

If equation (5.73) is solved for s, equation (5.74) is obtained.

$$s = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a} \tag{5.74}$$

Where

$$\begin{aligned} a &= -2CLR_oV_{DC} \\ b &= -2CR_oR_LV_{DC} - 2I_S^dLR_oU^d - 2LV_{DC} \\ c &= -2I_S^dLR_oU^q\omega - 2I_S^dR_oR_LU^d - R_o(U^q)^2V_{DC} - 2R_LV_{DC} \end{aligned}$$

Equation (5.74) has two solutions that are expected to be a pair of negative numbers (imaginary conjugate or not) due to the fact that buck-based converters exhibit a minimum phase behavior. If equation (5.75) is satisfied, solutions of equation (5.74) are negative complex conjugate numbers.

$$\begin{aligned} -4CI_S^dL^2R_o^2U^qV_{DC}\omega + C^2R_o^2R_L^2V_{DC}^2 - 2CI_S^dLR_o^2R_LU^dV_{DC} - 2CLR_o^2(U^q)^2V_{DC}^2 \\ +(I_S^d)^2L^2R_o^2(U^d)^2 - 2CLR_oR_LV_{DC}^2 + 2I_S^dL^2R_oU^dV_{DC} + L^2V_{DC}^2 \quad < \quad 0 \end{aligned} \tag{5.75}$$

by the equation (5.35), the numerator of $G_{i_S^d u^q}$ is given by the equation (5.76).

$$num(G_{i_S^d u^q}) \quad = \quad \begin{bmatrix} (-2CLR_oV_{DC}\omega - 2I_S^qLR_oU^d)s - 2I_S^qLR_oU^q\omega \\ -2I_S^qR_oR_LU^d + R_oU^dU^qV_{DC} - 2L\omega V_{DC} \end{bmatrix} \tag{5.76}$$

If equation (5.76) is solved for s, equation (5.77) is obtained.

$$s \quad = \quad -\frac{1}{2}\left[\frac{2I_S^qLR_oU^q\omega + 2I_S^qR_oR_LU^d - R_oU^dU^qV_{DC} + 2LV_{DC}\omega}{LR_o(CV_{DC}\omega + I_S^qU^d)}\right] \tag{5.77}$$

by the equation (5.36), the numerator of $G_{i_S^q u^d}$ is given by the equation (5.78).

$$num(G_{i_S^q u^d}) \quad = \quad \begin{bmatrix} (2CLR_oV_{DC}\omega - 2I_S^dLR_oU^q)s + 2I_S^dLR_oU^d\omega - 2I_S^dR_oR_LU^q \\ +R_oU^dU^qV_{DC} + 2L\omega V_{DC} \end{bmatrix} \tag{5.78}$$

If equation (5.78) is solved for s, equation (5.79) is obtained.

$$s \quad = \quad -\frac{1}{2}\left[\frac{2I_S^dLR_oU^d\omega + 2I_S^dR_oR_LU^q - R_oU^dU^qV_{DC} + 2LV_{DC}\omega}{LR_o(CV_{DC}\omega + I_S^dU^q)}\right] \tag{5.79}$$

by the equation (5.36), the numerator of $G_{i_S^q u^q}$ is given by the equation (5.80).

$$num(G_{i_S^q u^q}) \quad = \quad \begin{bmatrix} -2CLR_oV_{DC}s^2 + (-2CR_oR_LV_{DC} - 2I_S^qLR_oU^q - 2LV_{DC})s \\ +2I_S^qLR_oU^d\omega - 2I_S^qR_oR_LU^q - R_o(U^d)^2V_{DC} - 2R_LV_{DC} \end{bmatrix} \tag{5.80}$$

If equation (5.80) is solved for s, equation (5.81) is obtained.

$$s = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a} \tag{5.81}$$

Where

$$\begin{aligned} a &= -2CLR_oV_{DC} \\ b &= -2CR_oR_LV_{DC} - 2I_S^qLR_oU^q - 2LV_{DC} \\ c &= -2I_S^qLR_oU^d\omega - 2I_S^qR_oR_LU^q - R_o(U^d)^2V_{DC} - 2R_LV_{DC} \end{aligned}$$

Equation (5.81) has two solutions that are expected to be a pair of negative numbers (imaginary or not) due to the fact that buck-based converters exhibit a minimum phase behavior. If equation (5.82) is satisfied, solutions of equation (5.81) are negative complex conjugate numbers.

$$\begin{aligned} -4CI_S^qL^2R_o^2U^dV_{DC}\omega + C^2R_o^2R_L^2V_{DC}^2 - 2CI_S^qLR_o^2R_LU^qV_{DC} - 2CLR_o^2(U^d)^2V_{DC}^2 \\ +(I_S^q)^2L^2R_o^2(U^q)^2 - 2CLR_oR_LV_{DC}^2 + 2I_S^qL^2R_oU^dV_{DC} + L^2V_{DC}^2 < 0 \end{aligned} \tag{5.82}$$

by the equation (5.38), the numerator of $G_{i_S^0u^0}$ is given by the equation (5.83).

$$num(G_{i_S^0u^0}) = [-CR_oV_{DC}s - V_{DC}] \tag{5.83}$$

If equation (5.83) is solved for s, equation (5.84) is obtained.

$$s = -\frac{1}{CR_o} \tag{5.84}$$

Zero given by the equation (5.84) is positive because C and R_o are positive.

5.3.2 Passive Elements Selection

L and C values are to set taking into account both *system operating requirements* (Table 5.1) and *system constraints*.

According to the *voltages and currents waveform analysis*, $\max(\Delta i_S^{abc})$ can be limited. The worst condition for Δi_S^{abc} occurs when $\max(|I_S^{abc}|) = \dfrac{\max(|V_{pcc}^{abc}|)}{\min(|Z_{load}|)}$. If $I_S^{abc} = \max(|I_S^{abc}|)$ and $\dfrac{dI_S^{abc}}{dt} = 0$, equation (5.55) is simplified as equation (5.85).

$$\Delta i_S^{abc} = \frac{V_{DC}}{8L}\left[1 - 4\left(\frac{V_{pcc}^{abc} - R_L I_S^{abc}}{V_{DC}}\right)^2\right] T_{sw} \tag{5.85}$$

Solving equation (5.85) for L, equation (5.86) is obtained.

$$L = \frac{V_{DC}}{8\Delta i_S^{abc}}\left[1 - 4\left(\frac{V_{pcc}^{abc} - R_L I_S^{abc}}{V_{DC}}\right)^2\right] T_{sw} \tag{5.86}$$

If $\Delta i_S^{abc} < 2\%$ is desired even for $\max(|I_S^{abc}|)$, L must be selected such that equation (5.87) is satisfied.

$$L > \frac{V_{DC}}{8(0.02\max(|I_S^{abc}|))}\left[1 - 4\left(\frac{V_{pcc}^{abc} - R_L \max(|I_S^{abc}|)}{V_{DC}}\right)^2\right] T_{sw} \tag{5.87}$$

The TLSC SAPF worst condition is when the output power S_{out} is equal to $1.5kVA$ ($I_S^{abc} = 12.5A$). Furthermore, minimum inductor value $L_{\min}$ must satisfied $L_{\min} > 7.8736mH$.

According to the *voltages and currents waveform analysis*, $\Delta P_{DC-link}$ can be limited. It is known that the grid and capacitors C_1 and C_2 exchange energy at twice the grid frequency. Furthermore, v_{DC_1} and v_{DC_2} have a fluctuation around their rated values at $100Hz$. Assuming that the DC-link power variation is constrained to $\Delta P_{DC-link} < 300W$ in $t = \dfrac{1}{400}$ for $f_s = 50Hz$ and $\alpha = 0.9933$, thus, from equation (5.60) the minimum capacitor value $C_{\min}$ must satisfy $C_{\min} > 1194.7\mu F$.

According to the *losses effect and efficiency analysis*, if an efficiency $\eta > 95\%$ is desired, the losses ratio must satisfy $\alpha_L < 0.05$ in steady-state. If an efficiency $\eta > 90\%$ is desired in the TLSC SAPF worst condition, the losses ratio must satisfy $\alpha_L < 0.1$.

According to the *zeros-based dynamical system analysis*, from equations (5.73)-(5.83) $G_{i_S^d u^d}$, $G_{i_S^d u^q}$, $G_{i_S^q u^d}$, $G_{i_S^q u^q}$, and $G_{i_S^0 u^0}$ zeros are given in the table 5.2, respectively.

TABLE 5.2: Zeros values.

Transfer function	**Zeros** $[radseg^{-1}]$	
	s_1	s_2
$G_{i_S^d u^d}$	-2.3978	-99.7987
$G_{i_S^d u^q}$	-4.7527	
$G_{i_S^q u^d}$	0.3929	
$G_{i_S^q u^q}$	-50,4017 + 120,8493i	-50,4017 - 120,8493i
$G_{i_S^0 u^0}$	-1	

Figure (5.14) shows $G_{i_S^d u^d}$, $G_{i_S^d u^q}$, $G_{i_S^q u^d}$, $G_{i_S^q u^q}$, and $G_{i_S^0 u^0}$ step response for C_{min} and L_{min} values.

From Figure (5.14) is seen that $G_{i_S^d u^d}$, $G_{i_S^d u^q}$, $G_{i_S^q u^q}$, and $G_{i_S^0 u^0}$ are inverse response systems that exhibit a minimum phase behavior with large overshoot due to the fact that zeros are placed in the Left Half Plane (LHP). Otherwise, $G_{i_S^q u^d}$ is an inverse response system with the zero located in the RHP. $G_{i_S^q u^d}$ exhibits a non-minimum phase behavior with a large undershoot as is shown in Figure (5.14c).

Some simulations for several C and L values are carried out in order to see how these parameters affect the system dynamic response. Figure (5.15) shows maximum overshoot of the system step response due to the different C and L combinations. Figure (5.16) show both dq (See Figure (5.16a)) and zero-sequence (See Figure (5.16b)) system setting time due to the different C and L combinations, respectively.

From Figures (5.15) and (5.16) are seen that, in general, variations in L have a significant impact on maximum overshoot and setting time. Otherwise, variations in C have, in general, a subtle impact on maximum overshoot and setting time. For L and C values considered in these simulations: *(a)* in the $G_{i_S^d u^d}$ case, both small and large L values in combination with large C values cause larger overshoots. In contrast, large L values in combination with small C values are associated with smaller overshoots. *(b)* In the $G_{i_S^d u^q}$ case, the greatest impact over maximum overshoots is associated with L variations. Small L values cause larger overshoots, while large L values are associated with smaller overshoots in combination of any C value. *(c)* In the $G_{i_S^q u^d}$ case, small L values in combination with some C values cause maximum overshoots around $3 \times 10^5\%$, this overshoot magnitude is considered dangerous because it can cause system failures.

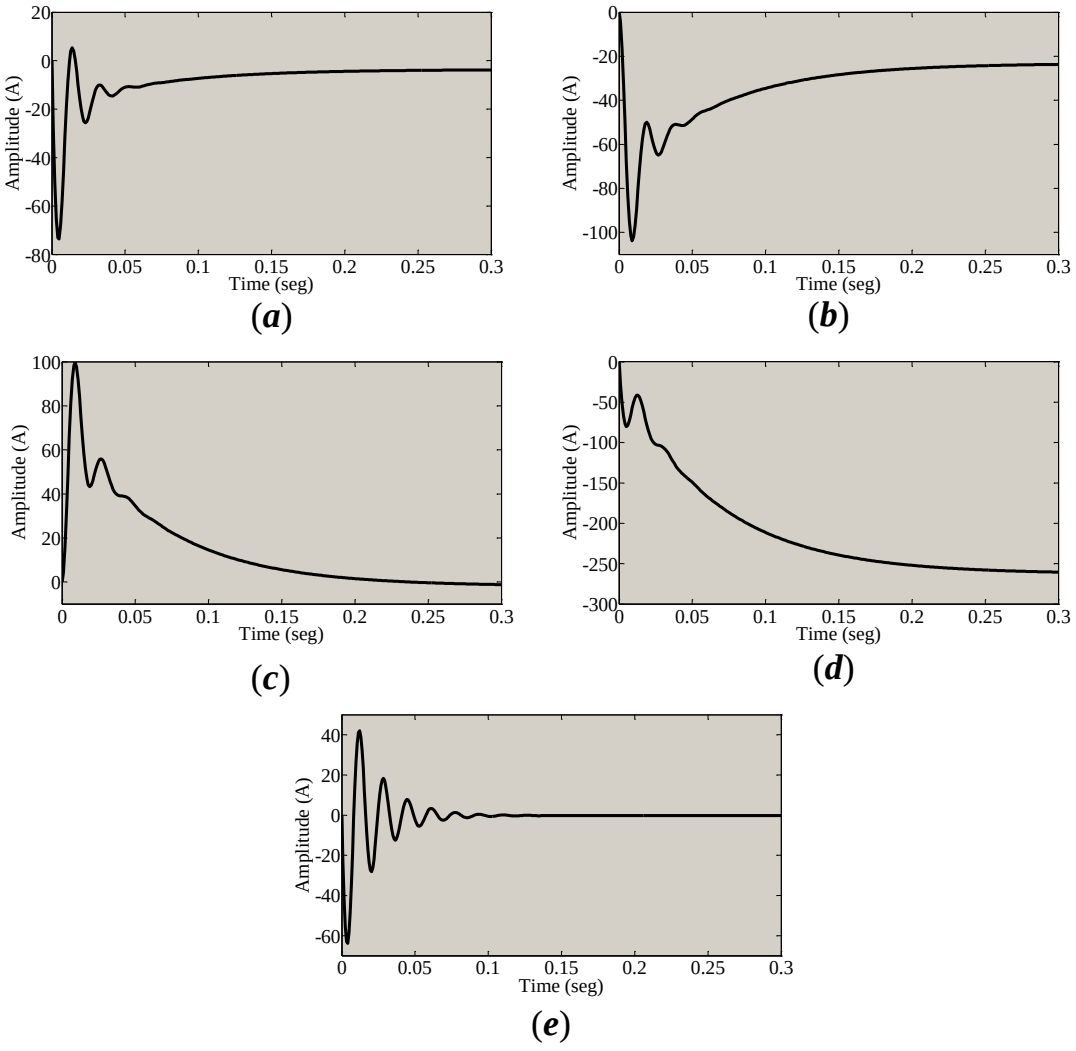

FIGURE 5.14: *(a)* $G_{i_S^d u^d}$ step response. *(b)* $G_{i_S^d u^q}$ step response. *(c)* $G_{i_S^q u^d}$ step response. *(d)* $G_{i_S^q u^q}$ step response. *(e)* $G_{i_S^0 u^0}$ step response.

In contrast, large L values in combination of any C value are associated with smaller overshoots. *(d)* In the $G_{i_S^q u^q}$ case, the greatest impact over maximum overshoots is associated with L variations. Small L values cause larger overshoots, while large L values are associated with smaller overshoots in combination of any C value. Finally, *(e)* in $G_{i_S^0 u^0}$, it is not possible to establish a pattern associated with L and C values, however, a remark is made: for some combinations of L and C values, maximum overshoots are around $3 \times 10^5\%$, these overshoots magnitude must be avoided because they can cause system failures. In conclusion, large L values are preferred due to the fact that smaller overshoots are associated with these. C values do not have a significant impact over maximum overshoot, however, C value must be selected such that in combination of any

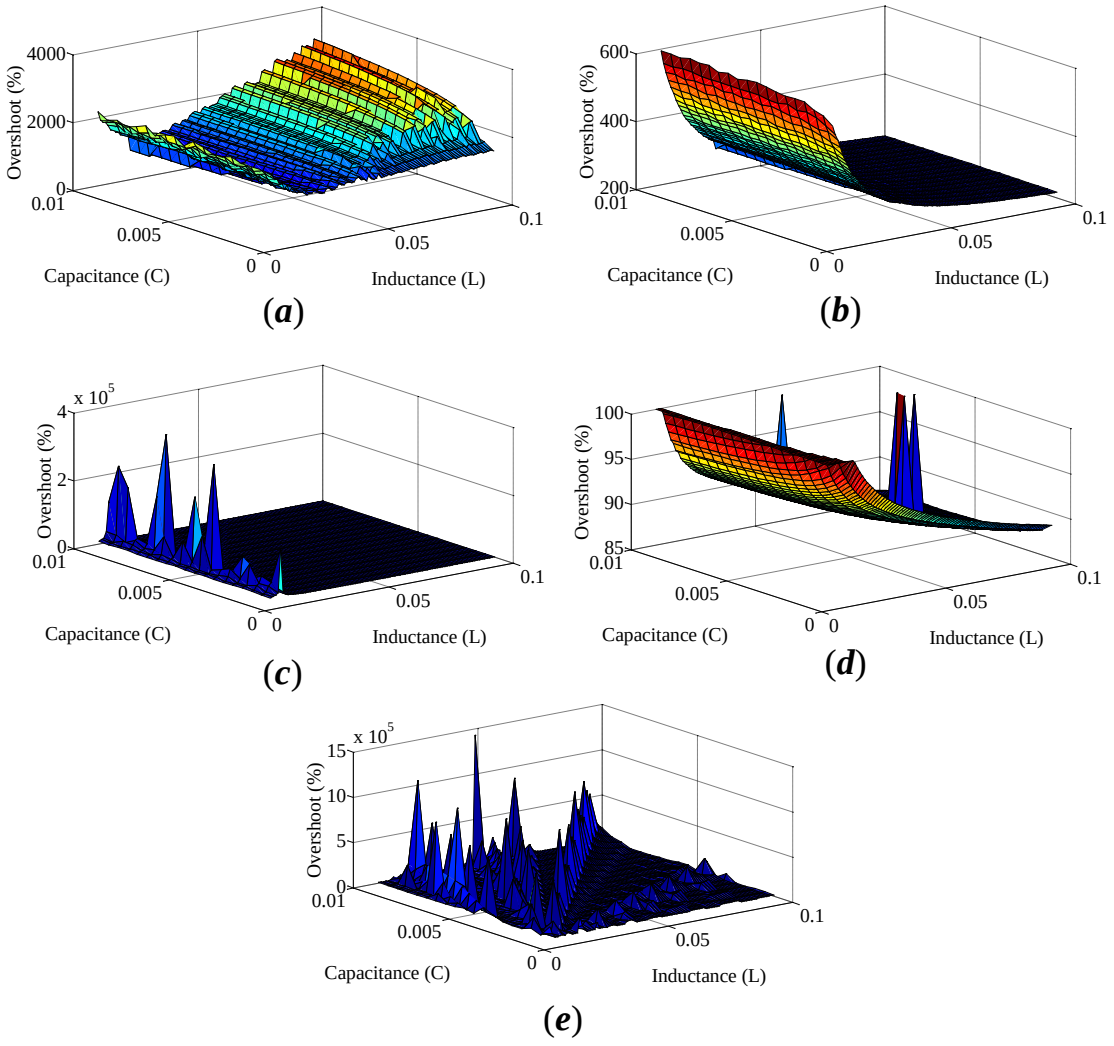

FIGURE 5.15: *(a)* $G_{i_S^d u^d}$ max overshoot. *(b)* $G_{i_S^d u^q}$ max overshoot. *(c)* $G_{i_S^q u^d}$ max overshoot. *(d)* $G_{i_S^q u^q}$ max overshoot. *(e)* $G_{i_S^0 u^0}$ max overshoot.

L value, maximum overshoots around $3 \times 10^5\%$ are avoided.

In order to keep a trade-off between system dynamic response and L and C sizes, TLSC SAPF selected inductance value and capacitance value are $L = 30mH$ and $C = 2200\mu F$, respectively. For selected L and C, $G_{i_S^d u^d}$, $G_{i_S^d u^q}$, $G_{i_S^q u^d}$, $G_{i_S^q u^q}$, and $G_{i_S^0 u^0}$ zeros and maximum overshoot are given in the table (5.3).

Figure (5.17) shows $G_{i_S^d u^d}$, $G_{i_S^d u^q}$, $G_{i_S^q u^d}$, $G_{i_S^q u^q}$, and $G_{i_S^0 u^0}$ step response for $C = 2200\mu F$ and $L = 30mH$.

From Figure (5.17) is seen that $G_{i_S^d u^d}$, $G_{i_S^d u^q}$, $G_{i_S^q u^d}$, $G_{i_S^q u^q}$, and $G_{i_S^0 u^0}$ are inverse system responses that exhibit a minimum phase behavior due to the fact that zeros are placed

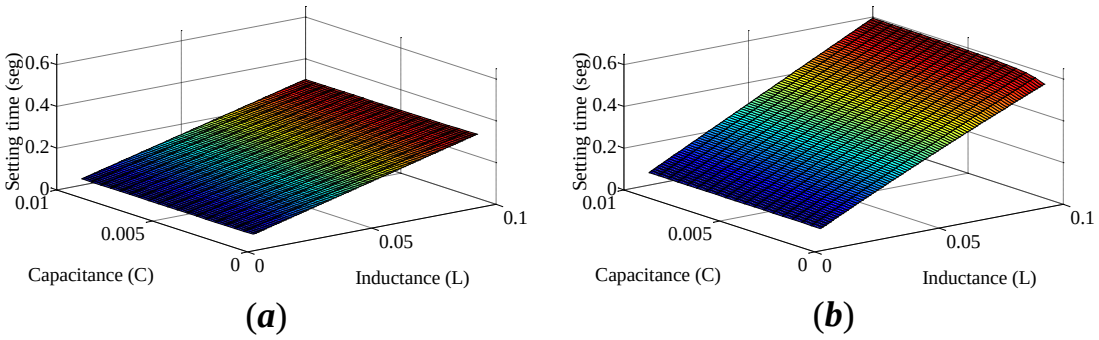

FIGURE 5.16: *(a) dq* system setting time. *(b)* zero sequence system setting time.

TABLE 5.3: Zeros and maximum overshoot.

Transfer function	**Zeros** $[radseg^{-1}]$		**Maximum overshoot** [%]
	s_1	s_2	
$G_{i_S^d u^d}$	-1,2602	-32,9336	1201,42
$G_{i_S^d u^q}$	-1,3879		300,62
$G_{i_S^q u^d}$	-0,2149		1120,94
$G_{i_S^q u^q}$	-16,6975 $\pm$ 51,8664i		93,39
$G_{i_S^0 u^0}$	-0,4545		19562,79

in the LHP.

5.3.3 System Frequency Response Verification

In order to validate the designed TLSC SAPF via simulation, frequency response of both mathematical model and PSIM circuital implementation are contrasted. The TLSC SAPF was parameterized with $L = 30mH$, $C = 2200\mu F$, $V_{DC} = 600V$, $V_{pcc}^{abc} = 120\sqrt{2}$, $R_L = 1\Omega$, and $R_o = 1k\Omega$. As system load was selected an inductive-resistive configuration with an inductive rated value $L_{load} = 44mH$ and a resistive rated value $R_{load} = 18.58\Omega$. Solving equations (5.40)-(5.42), the system equilibrium point is $I_S^q = 4.3742A$, $I_S^d = 1.1816A$, $U^d = 0.7001$, and $U^q = -0.0519$.

Figure (5.18) shows TLSC SAPF Bode diagrams for both mathematical model given by equations (5.35), (5.36), and (5.38) and PSIM circuital implementation. 100 points between $10Hz$ and $500Hz$ were taking in PSIM circuital simulation.

From Figure (5.18) is seen that most points of PSIM circuital simulation coincide with the Bode diagram of mathematical model. Thus, the TLSC SAPF PSIM circuital simulation is satisfactorily reproduced by the TLSC SAPF mathematical model given by equations (5.35), (5.36), and (5.38).

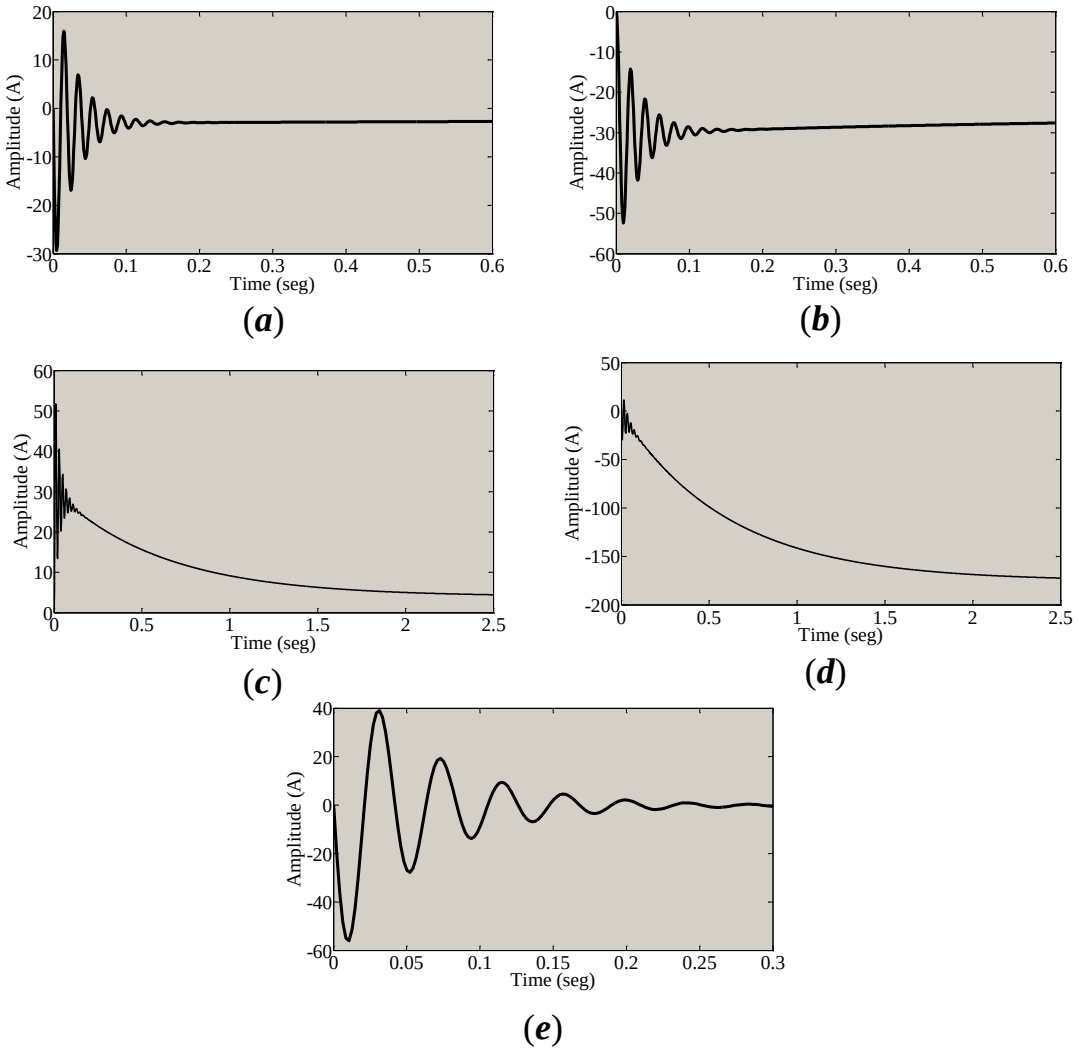

FIGURE 5.17: *(a)* $G_{i_S^d u^d}$ step response. *(b)* $G_{i_S^d u^q}$ step response. *(c)* $G_{i_S^q u^d}$ step response. *(d)* $G_{i_S^q u^q}$ step response. *(e)* $G_{i_S^0 u^0}$ step response.

5.4 Controllability Verification of the Designed TLSC SAPF

The third stage in the proposed design procedure of PECs is design controllability verification, which is composed by step 9. Then, algorithm (1) is applied to test the TLSC SAPF local controllability. The nonlinear dynamical model given by equations in (5.32) is taken as TLSC SAPF dynamical model to compute both robust reachable set $\tilde{\mathcal{R}}^t(\Omega_t)$ and robust controllable set $\tilde{\mathcal{C}}^t(\Omega_t)$. For the system controllability verification, the TLSC SAPF in the balance case is considered due to the fact that in the unbalanced case dq components have an oscillatory behavior. Zero sequence components are equal to zero in the TLSC SAPF balanced case, furthermore, state variables are i_S^d, i_S^q, and

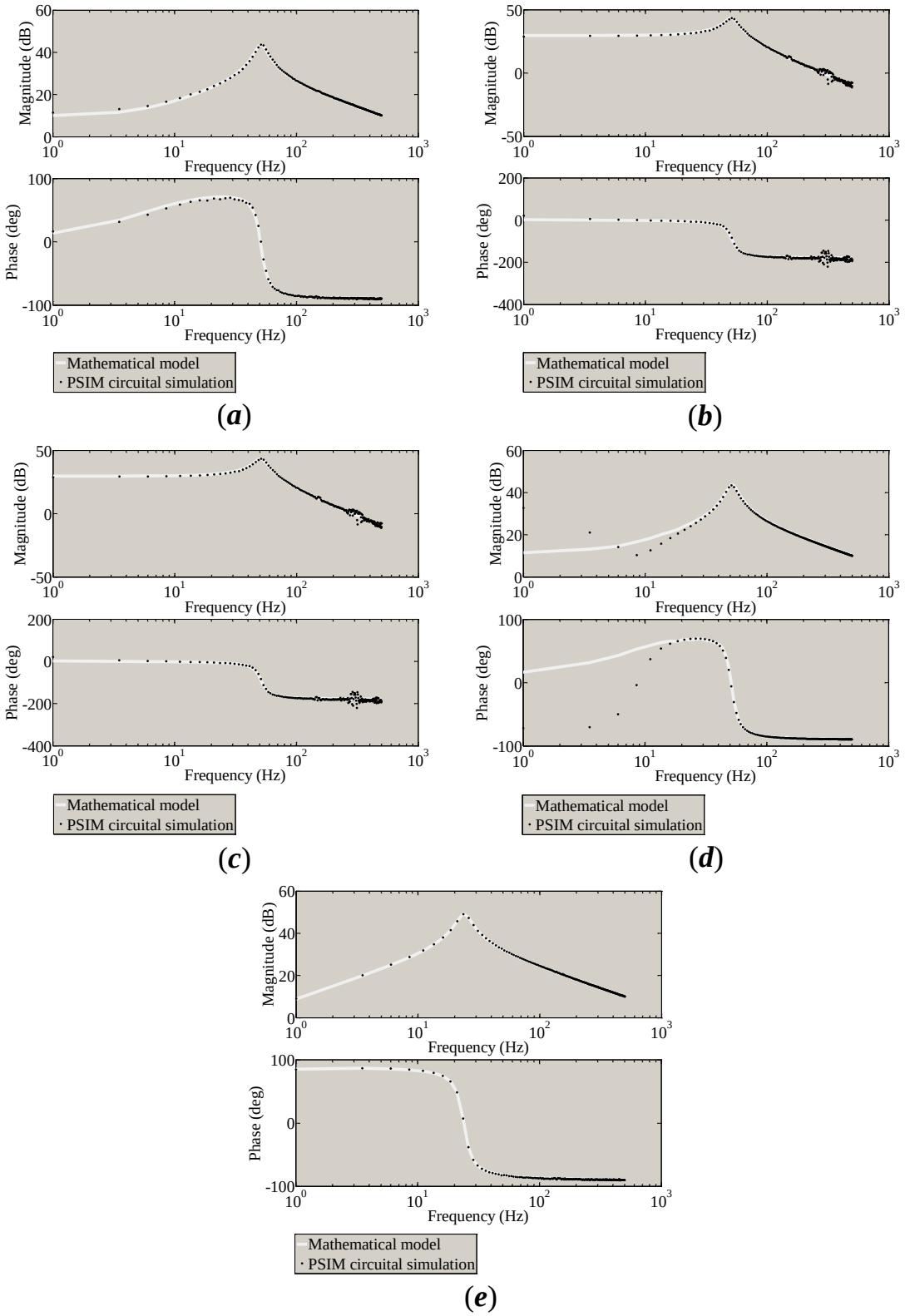

FIGURE 5.18: *(a)* $G_{i_S^d u^d}$ frequency response. *(b)* $G_{i_S^d u^q}$ frequency response. *(c)* $G_{i_S^q u^d}$ frequency response. *(d)* $G_{i_S^q u^q}$ frequency response. *(e)* $G_{i_S^0 u^0}$ frequency response.

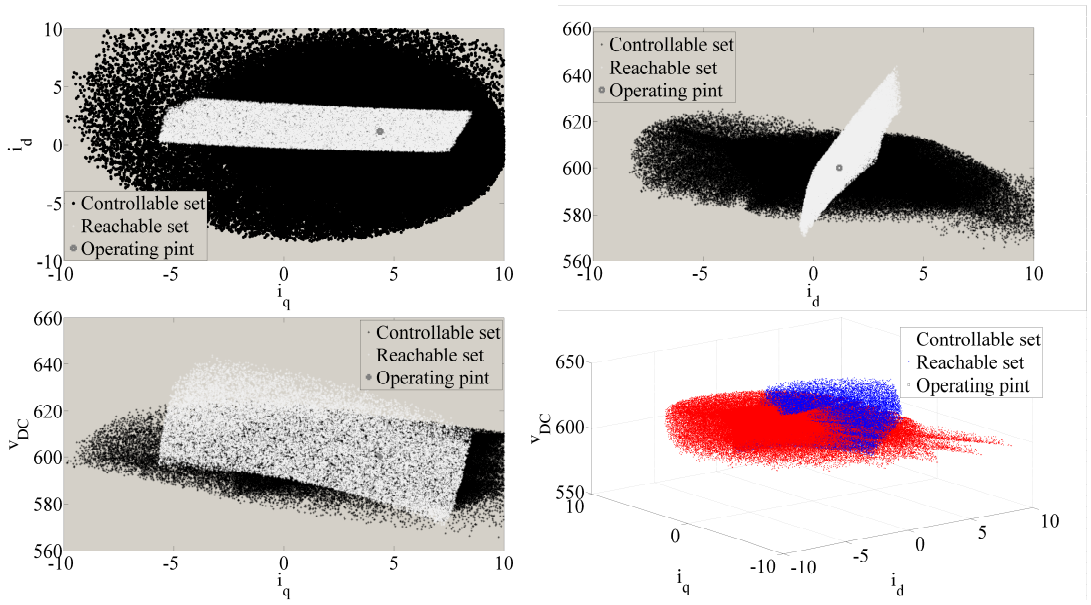

FIGURE 5.19: Robust reachable set from x_e in $t = 50ms$ and robust controllable set to x_e in $t = 50ms$ for the TLSC SAPF.

v_{DC}. Accordingly, the system state-space dimension is $X \in R^3$, this allows to compute three-dimensional system sets, which is possible to visualze in a 3D plot.

Following states and inputs boundaries were taken to compute the sets: $i_S^d \in [-10A, 10A]$, $i_S^q \in [-10A, 10A]$, and $v_{DC} \in [550, 650]$. The sample size was $N = 100000$ accordingly with Chernoff bound given by the equation (2.48).

Figure (5.19) shows the TLSC SAPF $\tilde{\mathcal{R}}^t(\Omega_t)$ from operating point $x_e = [1.1816A, 4.3742A, 600V]$ in $t = 50ms$ and $\tilde{\mathcal{C}}^t(\Omega_t)$ to x_e in $t = 50ms$.

From Figure (5.19) is seen that the robust reversible set $\tilde{\tau}^t(\Omega_t)$ exist because $\tilde{\mathcal{R}}^t(\Omega_t)$ and $\tilde{\mathcal{C}}^t(\Omega_t)$ are intersect. Furthermore, the system is locally controllable around the x_e.

The CI is computed based on 2.52, then $CI = 0.6772$, i.e., based on defined controllability index (2.49), the designed TLSC SAPF is 67.72% controllable around x_e. This result implies that exist states that are possible to reach with admissible control signals, but it is impossible to return to x_e from these states in $t = 50ms$ with the same admissible control signals. It is possible that for $t > 50ms$ these uncontrollable states become controllable. However, in this work $t = 50ms$ is considered as a prudent time to analyze the system controllability due to the switching system time $T_{sw} = 0.05ms$, i.e., $t >> 0.05ms$.

TLSC SAPF controllability analysis via set theory in control allows a visually verification of this property. From Figure (5.19) is seen that the system is locally controllable about

x_e due to the fact that, with admissible control signals, it is possible to drive the system in any state-space direction from x_e. Furthermore, exits a state-space region ($\tilde{\tau}^t(\Omega_t)$) where is possible to go and return to x_e in $t = 50ms$, i.e., the system is weakly reversible about x_e.

Finally, in the work presented by **??** is introduced a design procedure to chemical processes. This design procedure also is based on the set theory in control. Author in his work shows that the system controllability is depended of system parameters and that the CI can be maximized varying them. This optimization process is out of the scope of this work, however, results presented in here can be employed to carry out this optimization process in a future work.

5.5 Control Structure Design

The fourth stage in the proposed design procedure of PECs is control structure design, which is composed by step 10. A Voltage Oriented Control (VOC) structure is designed for TLSC SAPF and it is implemented in PSIM to evaluate dynamical system performance. The aim of this stage is to design a suitable control structure for designed TLSC SAPF such that control objective is achieved. This stage is composed of following subsections: *(1)* control structure selection, *(2)* controllers tuning, and *(3)* closed-loop system performance verification.

5.5.1 Control Structure Selection

The TLSC SAPF control objective is to supply inefficient currents requested by the load while keeping the DC-link voltage in its rated value. This control objective must be achieved such that the grid mains supply only provides the fundamental positive-sequence active power P_1^+ to the load. Efficient and inefficient system currents are directly related with $dq0$ transformation and even compatible with IEEE Std. 1459-2010 [116]. Furthermore, the use of TLSC SAPF $dq0$ models facilitates the control structure design task [10].

Assuming that the grid mains voltage supply quadrature component V_{pcc}^q is equal to zero, from the point of view of the grid mains supply, the Unit Power Factor (UPF) at Point of Common Coupling (PCC) is obtained if only the DC quantity of the direct current component i_L^d requested by the load is supplied by the grid mains supply.

A conventional Three-phase SAPF control structure is composed of two PI current controllers, one for each dq SAPF current components, and an additional PI DC-link

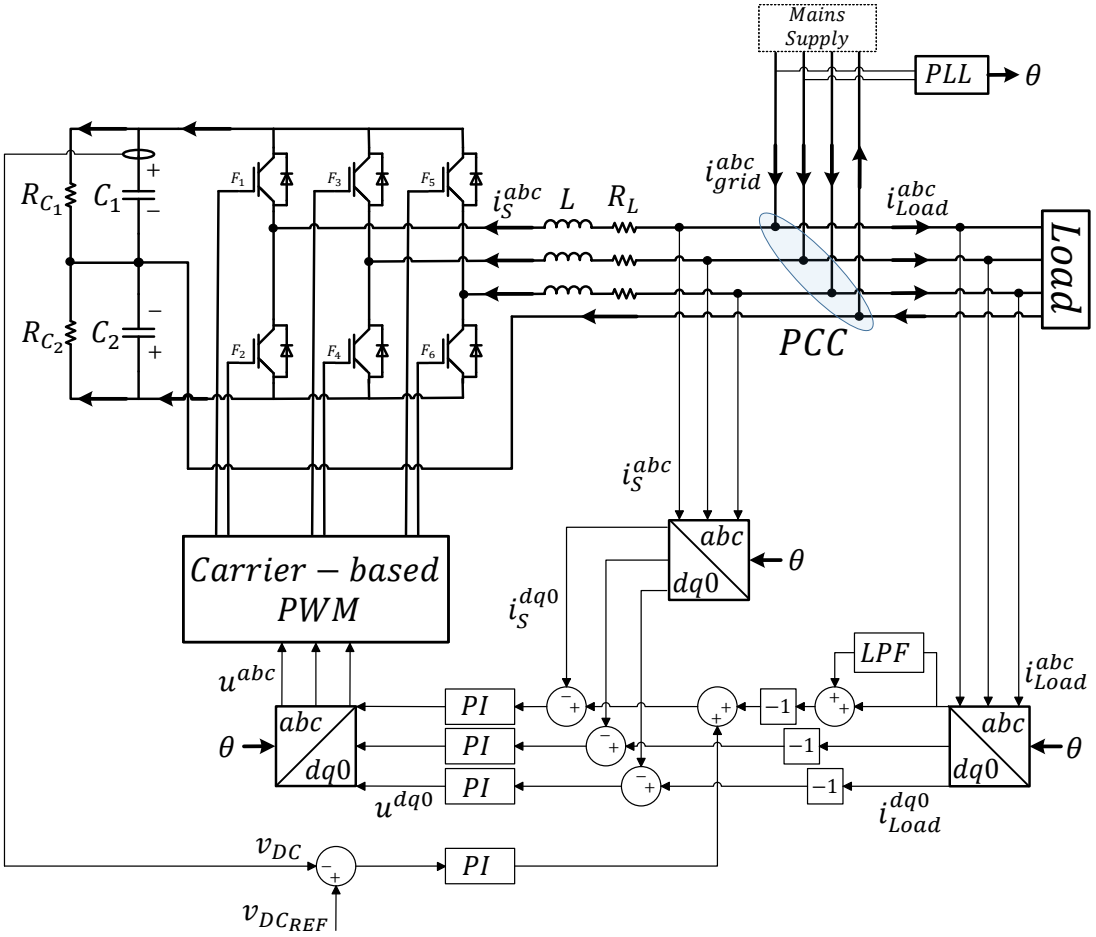

FIGURE 5.20: TLSC SAPF control structure.

voltage controller disposed in cascade form with the PI controller of the SAPF direct current component i_S^d [10].

Figure (5.20) shows the TLSC SAPF control structure block diagram. This is an extended version of the Three-phase SAPF control structure. From Figure (5.20) is seen that the control structure is composed of three PI current controllers, one for each $dq0$ TLSC SAPF component, and an additional PI DC-link voltage controller disposed in cascade form with the PI controller of the TLSC SAPF direct current component i_S^d. This control structure allows to compensate not only inefficient currents related to dq components but also the zero sequence current related with an unbalanced system condition. To achieve the control objective even under unbalanced system condition, TLSC SAPF must supply the AC quantity of i_L^d. This AC quantity is extracted by means of a Low Pass Filter (LPF) and added with opposite sign to I_S^d given by the equation (5.40). Thereby, the grid mains supply only provides P_1^+ due to the fact that the grid mains supply voltages and currents are balanced and in phase.

The general control structure for synchronous dq rotating reference-frame includes a decoupling stage [122]. However, in [10] this stage is obviated and authors show that both PI current controllers and PI DC-link voltage are designed successfully. Hence, in this work, the decoupling stage is not included.

5.5.2 Controllers Tuning

Due to the fact that the TLSC SAPF switching frequency is $20kHz$, current loops bandwidth must be smaller than $4kHz$ and DC-link voltage loop bandwidth must be smaller than $800Hz$ [88]. Additionally, a robustness index $M_s < 2$ is desired to establish a trade-off between control performance and robustness [66].

Current controllers were designed by means of the root-locus technique adopting following design specifications: *(a)* damping factor ζ equal to 0.707 and *(b)* $20kHz$ closed loop bandwidth. Designed PI controllers transfer functions for i_s^d, i_s^q and i_s^0 are given by the equation (5.88), (5.89), and (5.90), respectively. These PI controllers ensure: *a* zero steady-state error and satisfactory reference tacking for frequencies below $4kHz$ for i_s^d, i_s^q and i_s^0 observed on transfer functions $T_{i_S^d i_{S_{REF}}^d}$, $T_{i_S^q i_{S_{REF}}^q}$, and $T_{i_S^0 i_{S_{REF}}^0}$ in Figures (5.21a, b, and c), respectively. *(b)* Effective disturbance rejection of v_{pcc}^{dq0} observed in Figures (5.21a, b, and c) for i_s^d, i_s^q and i_s^0, respectively. *(c)* A $M_s = 1.2$.

$$G_{C_{i_s^d}} = -\frac{1.7s + 15452}{s} \tag{5.88}$$

$$G_{C_{i_s^q}} = -\frac{1.8s + 14911}{s} \tag{5.89}$$

$$G_{C_{i_s^0}} = -\frac{1.8s + 15122}{s} \tag{5.90}$$

Once that PI current control loops are closed, TLSC SAPF equivalent simplified representation showed in Figure (5.22) is derived. Both large-signal model and small-signal model of simplified TLSC SAPF are given by equations (5.91) and (5.92), respectively. Applying realization given by (5.34), transfer functions for the system described by the equation (5.92) are given by the equation (5.93).

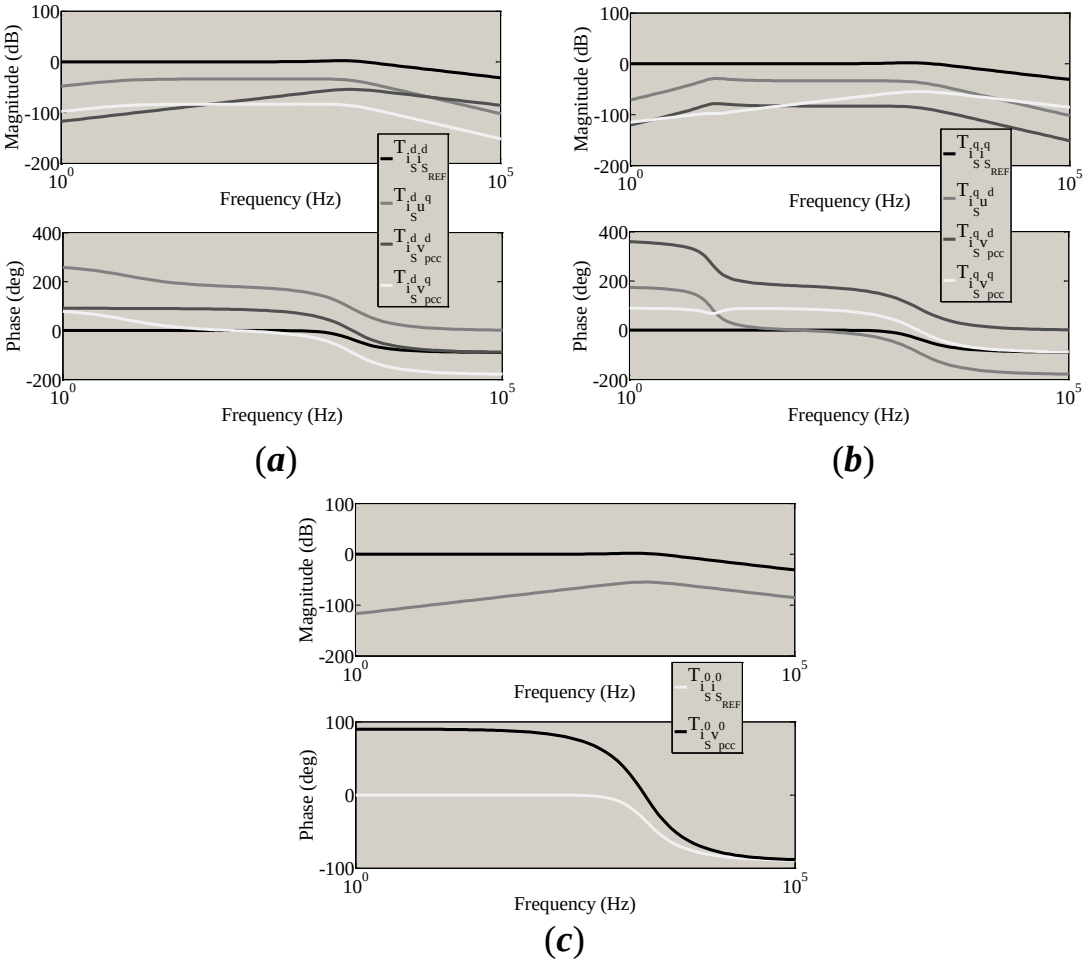

FIGURE 5.21: *(a)* i_S^d closed-loop transfer functions bode diagrams. *(b)* i_S^q closed-loop transfer functions bode diagrams. *(c)* i_S^0 closed-loop transfer functions bode diagrams.

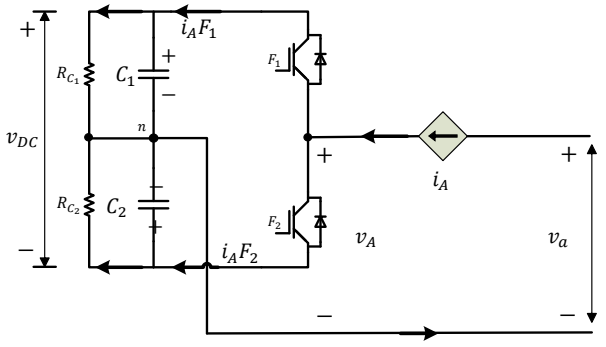

FIGURE 5.22: The TLSC SAPF equivalent simplified representation.

$$\begin{aligned} C\frac{dv_{DC}}{dt} &= i_S^{dq0}u^{dq0^T} - \frac{v_{DC}}{R_o} \\ 2C\frac{d\varepsilon_v}{dt} &= \sqrt{3}i_S^0 - \frac{2\varepsilon_v}{R_o} \end{aligned} \tag{5.91}$$

$$\begin{aligned} \begin{bmatrix} \dot{v}_{DC} \\ \dot{\varepsilon}_v \end{bmatrix} &= \begin{bmatrix} -\frac{1}{R_oC} & 0 \\ 0 & -\frac{1}{R_oC} \end{bmatrix} \begin{bmatrix} v_{DC} \\ \varepsilon_v \end{bmatrix} + \begin{bmatrix} \frac{U^d}{C} & \frac{U^q}{C} & \frac{U^0}{C} \\ 0 & 0 & \frac{\sqrt{3}}{2C} \end{bmatrix} \begin{bmatrix} i_S^d \\ i_S^q \\ i_S^0 \end{bmatrix} \\ y &= \begin{bmatrix} 1 & 0 \end{bmatrix} \begin{bmatrix} v_{DC} \\ \varepsilon_v \end{bmatrix} \end{aligned} \tag{5.92}$$

$$G_{v_{DC}i_S^{dq0}} = \frac{\begin{bmatrix} R_oU^d & R_oU^q & R_oU^0 \end{bmatrix}}{R_oCs+1} \tag{5.93}$$

A PI controller that provides the i_S^d control loop setpoint, has been designed to regulate the DC-link voltage v_{DC}. v_{DC} PI controller was designed by means of the root-locus technique adopting following design specifications: *(a)* damping factor ζ equal to 0.707 and *(b)* setting time t_s equal to $0.2s$. Due to the fact that v_{DC} open-loop setting time is about $8.61s$, a closed-loop setting time of $0.2s$ is a very restricted condition for this control loop. Designed PI controller transfer function $G_{C_{v_{DC}}}$ is given by the equation (5.94). These PI controllers ensure: *a* zero steady-state error and satisfactory reference tacking for frequencies below $30Hz$ for v_{DC} observed on transfer function $T_{v_{DC}v_{dc_{REF}}}$ in Figure (5.23). *(b)* Effective disturbance rejection of i_S^q observed in Figure (5.23). *(c)* A $M_s = 1.2$.

$$G_{C_{V_{DC}}} = \frac{0.4122s + 29.44}{s} \tag{5.94}$$

5.5.3 TLSC SAPF Performance Verification

Figures (5.24) and (5.25) show the dynamical system response of the grid without TLSC SAPF (before compensation). Three unit load step changes were applied as follow: *(a)* at $t = 0.8s$ a balanced three-phase inductive-resistive load with equivalent inductance

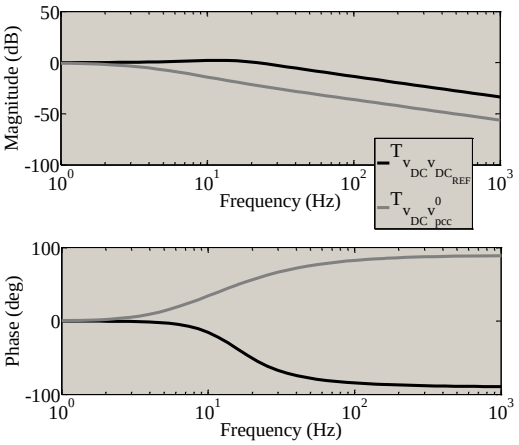

FIGURE 5.23: v_{DC} closed-loop transfer functions bode diagrams.

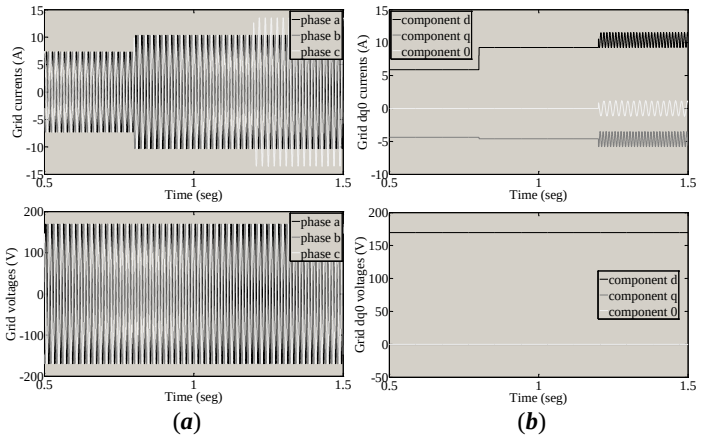

FIGURE 5.24: the grid dynamical response without TLSC SAPF.

$L = 10mH$ and equivalent resistance $R = 50\Omega$ is added in shunt form to the rated load. *(b)* At $t = 1.2s$ unbalanced system condition is set up, an inductive-resistive load with equivalent inductance $L = 10mH$ and equivalent resistance $R = 50\Omega$ is added in shunt form to phase c of the grid.

From Figures (5.24) and (5.25) are seen that $i^q_{grid} \neq 0$, this means that the load is inefficient. Moreover, at $t = 1.2s$, when unbalanced condition is set up, a sequence zero current appears flowing through the neutral wire and both i^d_{grid} and i^q_{grid} components are composed of a DC quantity and an AC quantity that oscillate at twice the grid frequency ($100Hz$). The unbalanced condition is observed in the currents plot of Figure (5.24a). Figure (5.25) shows the comparison between voltages and currents per phase.

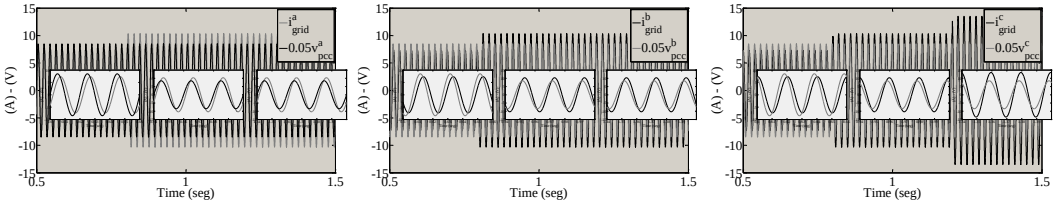

FIGURE 5.25: the grid dynamical response per phase without TLSC SAPF.

It is seen that there is a gap between currents and voltages, this gap is another evidence of the load inefficient.

To assess the closed-loop system performance, TLSC SAPF with its PI current controllers has been implemented in PSIM. Figure (5.26) shows the TLSC SAPF closed-loop response to load unit step changes described above; Figure (5.27) shows the PI current controllers tracking error; and Figure (5.28) shows the comparison between voltages and currents per phase.

From Figure (5.26a) is seen that PI current controllers track satisfactorily the reference, even in the unbalanced system condition where the reference is sinusoidal. It is also seen that the DC-link voltage is not regulated and this highlights the necessity to add an additional control loop to drive the DC-link voltage to its desired rated value ($600V$). From Figure (5.26a) is also seen that u^{abc} remains in the range $[0, 1]$, i.e., the TLSC SAPF do not present over-modulation.

From Figure (5.26b) is seen that the mains grid supply delivers efficient requested load currents and necessary current to compensate TLSC SAPF losses and to maintain DC-link voltage level. It is also seen that TLSC SAPF delivers inefficient requested load currents, even in the unbalanced system condition. Above statement is true due to the fact that i^q_{grid} component is close to zero along the entire simulation period and $i^q_S \approx -i^q_L$. Finally, from Figure (5.26b) is seen that the grid zero-component is close to zero along the entire simulation period, even in the unbalanced system condition. This means that the TLSC SAPF mitigates the requested load neutral current raising system efficiency.

From Figure (5.26c) is seen that the grid mains supply delivers both balanced voltages and balanced currents to the load. Inefficient requested load currents are delivered by the TLSC SAPF. It is seen that load neutral current and TLSC SAPF neutral current coincide. Hence, TLSC SAPF mitigates both load inefficiency and unbalanced system condition.

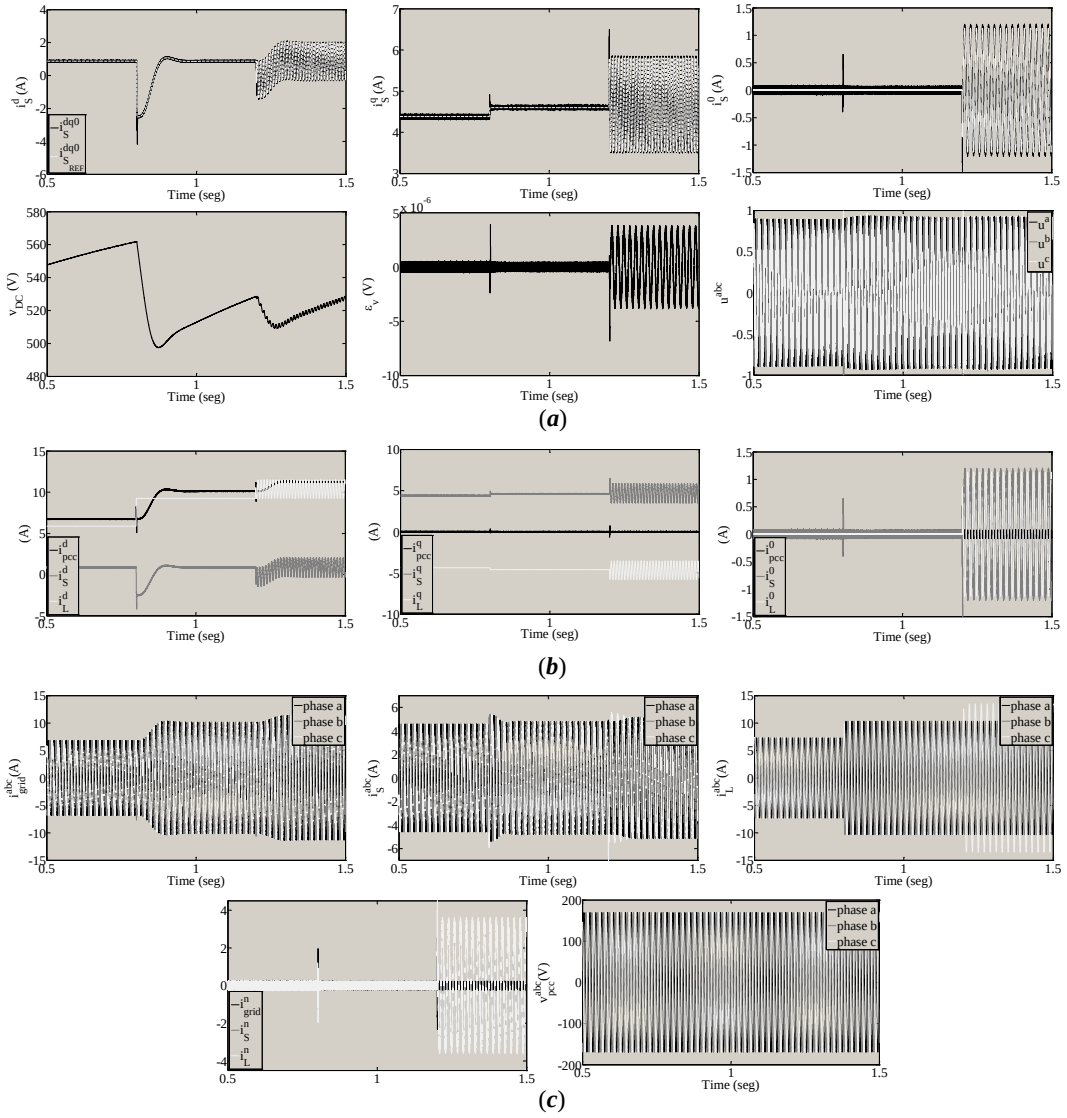

FIGURE 5.26: *(a) dq*0 reference frame closed-loop response. *(b) dq*0 currents components comparison. *(c) abc* reference frame closed-loop response.

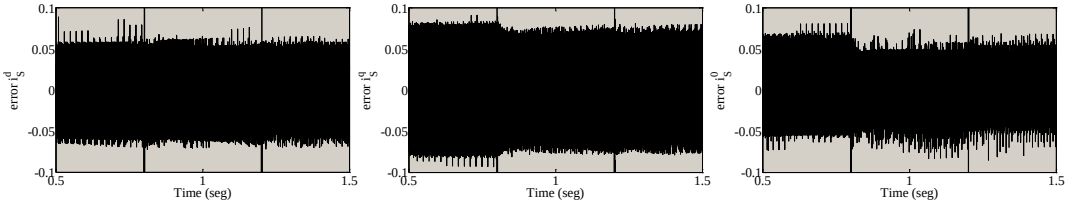

FIGURE 5.27: PI current controllers tracking error.

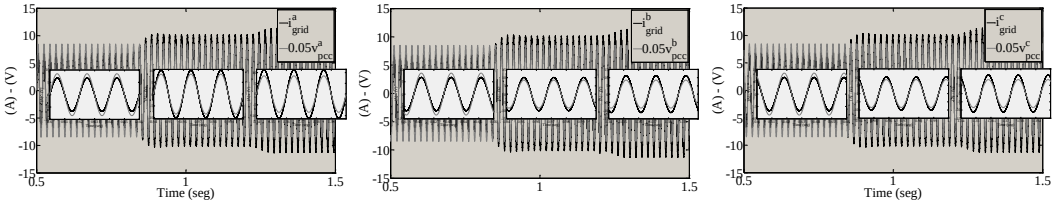

FIGURE 5.28: Grid phase verification with TLSC SAPF closed-loop of PI currents.

From Figure (5.27) is seen that the controller tracking error, along the entire simulation period, is maintained below $0.1A$, i.e., PI current controllers track the reference with an error equal to $\pm 0.1A$. This result allows to conclude that PIs performance is successful.

From Figure (5.28) is seen that there is not a gap between currents and voltages, this lack of a gap is another evidence that the TLSC SAPF mitigates both load inefficiency and unbalanced system condition. Furthermore, from the grid mains supply point of view, the load is an efficiency load.

Once that PI current controller are tested, the PI DC-link voltage controller is implemented in PSIM and TLSC SAPF closed-loop performance is assessed. Figure (5.29) shows TLSC SAPF closed-loop response to load unit step changes described above; Figure (5.30) shows PI current controllers tracking error; Figure (5.31) shows PI DC-link voltage controller tracking error; and Figure (5.32) shows the comparison between voltages and currents per phase.

From Figure (5.29a) is seen that PI current controllers track satisfactorily the reference, even in unbalanced system condition where the reference is sinusoidal. It is also seen that the DC-link voltage is regulated and that the voltage control loop drives the DC-link voltage about its desired rated value ($600V$). In unbalanced system condition, the DC-link voltage oscillate about $600V$. This oscillation also appears in Figure (5.29a) and it is because grid mains supply and load exchange energy at twice the grid frequency ($100Hz$). From Figure (5.29a) is also seen that u^{abc} remains in the range $[0, 1]$, i.e., the TLSC SAPF does not present over-modulation.

From Figure (5.29b) is seen that the grid mains supply delivers efficient requested load currents and necessary current to compensate TLSC SAPF losses and to maintain the DC-link voltage level. However, in this case, unlike the case presented in Figure (5.29b), the grid mains supply also delivers an inefficient current to the load when unbalanced system condition is set up at $t = 1.2s$. This statement is true due to the fact that there is a persistent oscillation in i^d_{grid}. From Figure (5.29b) is seen also that TLSC SAPF deliver inefficient requested load currents, even in the unbalanced system condition.

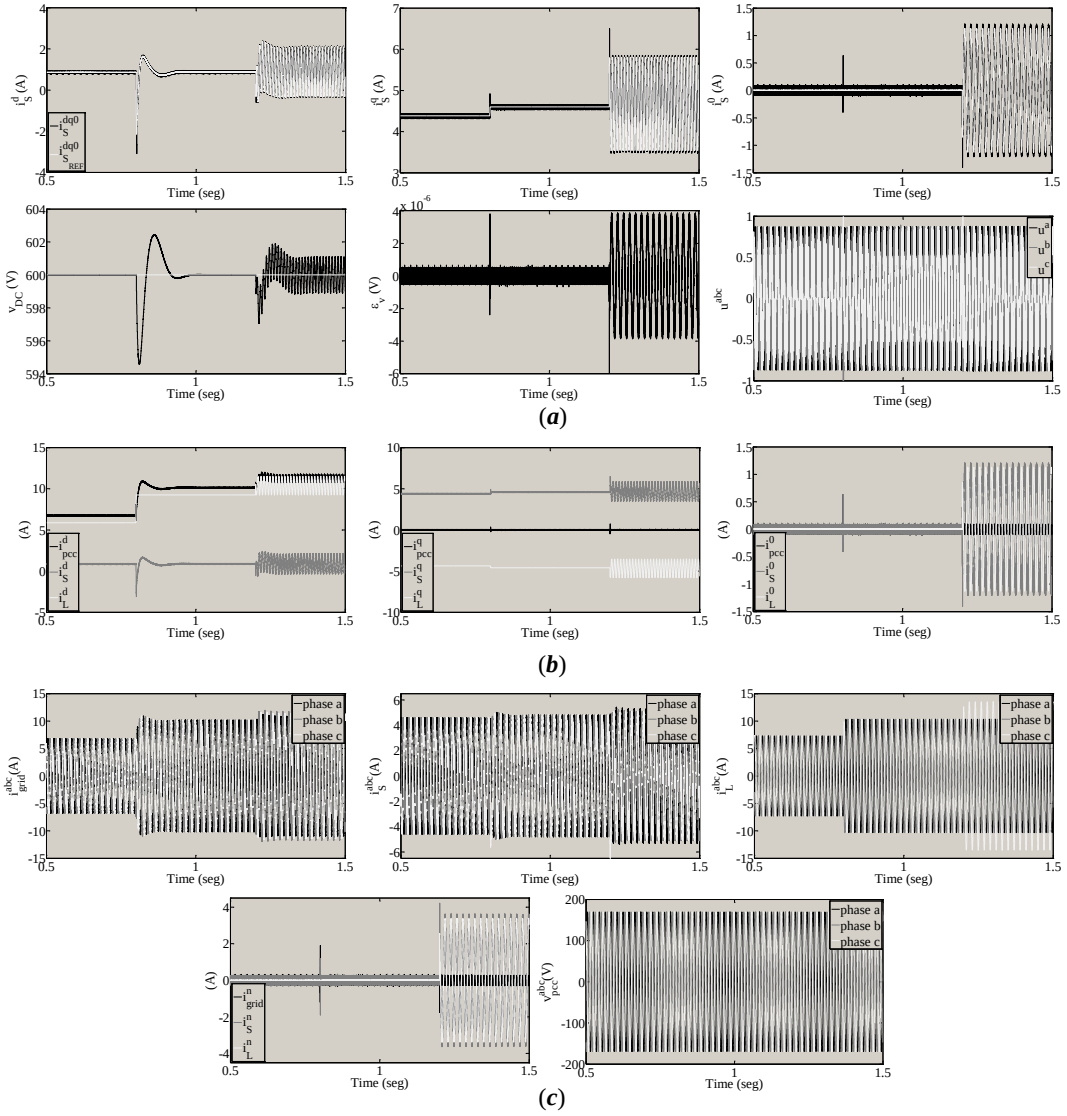

FIGURE 5.29: *(a) dq*0 reference frame closed-loop response. *(b) dq*0 currents components comparison. *(c) abc* reference frame closed-loop response.

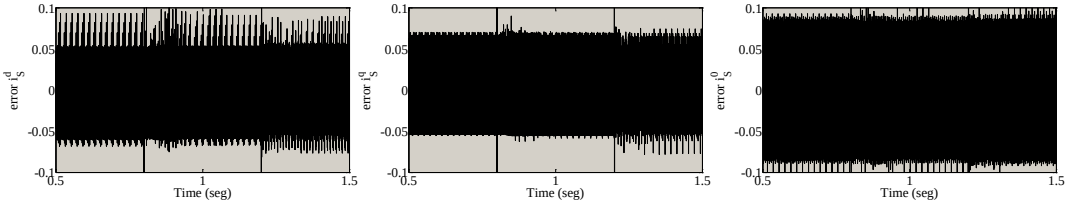

FIGURE 5.30: PI current controllers tracking error.

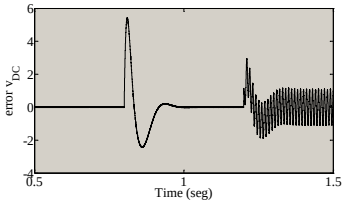

FIGURE 5.31: PI DC-link voltage controller regulating error.

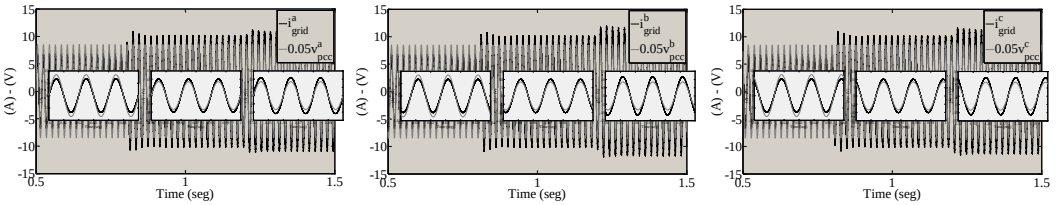

FIGURE 5.32: Grid phase verification with TLSC SAPF closed-loop of PI currents and PI DC-link voltage.

Above statement is true due to the fact that i^q_{grid} component is close to zero along the entire simulation period and $i^q_S \approx -i^q_L$. Finally, from Figure (5.29b) is seen that the grid zero component is close to zero along the entire simulation period, even in the unbalanced system condition. This means that TLSC SAPF mitigates the requested load neutral current raising system efficiency.

From Figure (5.29c) is seen that the grid mains supply delivers balanced voltages. However, currents delivered by the grid mains supply to the load are slightly unbalanced after $t = 1.2s$. Inefficient requested load currents are partially delivered by the TLSC SAPF after $t = 1.2s$. From Figure (5.29c) is seen that load neutral current and TLSC SAPF neutral current have a slightly magnitude difference. Hence, in this case, TLSC SAPF mitigates the load inefficiency, but it does not fully mitigate unbalanced system condition.

From Figure (5.30) is seen that the controller tracking error, along the entire simulation period, is maintained below $0.1A$, i.e., PI current controllers track the reference with an error equal to $\pm 0.1A$. This result allows to conclude that PIs performance is successful.

From Figure (5.31) is seen that the PI DC-link controller regulating error decreases to zero after each load unit step change. Then, the PI DC-link control loop rejects considered disturbances satisfactorily.

From Figure (5.32) is seen that there is not a gap between currents and voltages, this lack of a gap is another evidence that TLSC SAPF mitigates load inefficiency and partially unbalanced system condition.

5.6 Conclusions

In this chapter a TLSC SAPF was designed applying the proposed design procedure presented in chapter 3. Both large and small signal models were derived and were used to system design.

To determine suitable passive elements boundaries such that system operating requirements were assured, steady-state, currents and voltage waveforms, losses effect and efficiency, and zeros-based dynamical system analysis were carried out. Then TLSC SAPF passive elements were selected and several simulations of both mathematical model and PSIM circuital implementation were carried out to verify the correspondence between both models.

Later the design controllability verification was made, and both robust reachable and controllable sets were computed. CI showed that the designed TLSC SAPF was 62.72% controllable around its operating point.

Finally, a control structure composed of three PI current controllers and a PI DC-link voltage controller was designed and implemented in PSIM to verify the TLSC SAPF closed-loop performance. Designed control structure allowed to mitigate satisfactorily requested inefficient load currents in balanced system condition. In unbalanced system condition, the designed control structure allowed to partially mitigate the requested load inefficient load currents. An important aspect of the proposed control structure is that it is based on instantaneous $dq0$ power theory, which is supported in the IEEE Std. 1459-2010. To conclude, the proposed design procedure allowed to design PECs based on system knowledge and control theory that fulfil the operating requirements.

Chapter 6

Conclusions and Future Work

Conclusions

In this work a PECs design procedure was proposed. The proposed design procedure allowed to design two common PECs applications based on their physical knowledge. The first application was a Boost DC-DC converter since is the most common topology adopted in PV applications. The second application was a TLSC SAPF since in the most employed APF topology to mitigate current-related problems in the electrical power systems.

For both Boost DC-DC converter and TLSC SAPF applications, all passive elements was established such that all operating requirements were satisfied. But also, inherent converters dynamical nature were taken into account and a zeros-based dynamical analysis was carried out in order to avoid non-minimum phase system behavior or minimize their impact over dynamical system performance.

Next, the design controllability-oriented verification method based on set theory in control was applied to quantify both Boost DC-DC converter and TLSC SAPF controllability. By above analysis, the designed Boost DC-DC converter was 92.41% controllable and the designed TLSC SAPF was 62.72% controllable, i.e., applying the proposed design procedure system controllability was assured for both applications.

Finally, a common control structure was implemented for both Boost DC-DC converter and TLSC SAPF applications. For Boost DC-DC converter the CMC structure was designed and implemented in PSIM to evaluate closed-loop system performance. Some simulations under different conditions were carried out, in which were possible to verify that all operating requirements were satisfied. For TLSC SAPF a VOC structure was designed and implemented in PSIM to evaluate closed-loop system performance. This VOC

structure incorporate some additional modifications in comparison with standard VOC for three-phase SAPF application. These additional modifications allowed to mitigate zero-sequence currents due to unbalanced system condition and instantaneous mitigation of reactive currents. Some simulations under unit step load change were carried out, in which were possible to verify that the TLSC SAPF indeed mitigate current-related problems due to inefficient loads.

The proposed design procedure resulted in a effective proposal to design PECs such that all operating requirements were satisfied. The main features of proposed PECs design procedure were: *(a)* all system parameters were selected based on physical system knowledge, *(b)* inherent system dynamical nature was taken into account in the design process, *(c)* the designed PECs were controllable and it was possible quantify their controllability, and *(d)* none control structure were fixed, therefore, the design procedure will be applied to other PECs applications.

Future Work

After completing this work, the following aspects must be revised or explored toward complementing the outcome of this thesis:

- Apply the proposed procedure design in others PECs in order to find its possible limitations and restrictions.
- Experimental validation of obtained results in order to show existing discrepancies between theoretical developments and real application.
- Extend the proposed design procedure including an optimization stage that maximaze the PEC controllability.
- Explores others control structures in order to complete the proposed design procedure to suggesting any suitable control structure based on the system controllability of whichever system physical property.
- Explores other applications of set theory in control in PECs design and control field.

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