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Modeling and development of a bridgeless PFC Boost rectifier

Modelamiento y desarrollo de un rectificador Boost PFC sin puente

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ABSTRACT: This paper proposes a model of the bridgeless PFC (Power Factor Correction) boost rectifier for control purposes based on an averaged small-signal analysis. From circuital laws, four operation modes are defined and explained, ensuring a relationship of physical variables in the converter. Based on the proposed model, two-loop cascade control structures composed of Proportional-Integral (PI) lineal controllers are proposed. Design consideration for dimensioning reactive elements is included, providing minimum values for their inductance and capacitance. Implementation of a laboratory prototype of 900 W and experimental results are presented to validate and reaffirm the proposed model. Experimental results demonstrate that the use of the bridgeless PFC boost converter model allows the Power Factor (***PF***) to be elevated up to 0.99, to reduce the THD_i (Total Harmonic Distortion of the Current) to 3.9% and to control the DC voltage level on output. Compliance of standards of power quality EN 61000-3-2 (IEC 1000-3-2) are experimentally verified.

RESUMEN: Este artículo propone un modelo para rectificadores elevadores PFC (Power Factor Correction por sus siglas en inglés) sin puente para propósitos de control y basado en el análisis del promedio de pequeña señal. A partir de las leyes circuitales, cuatro modos de operación son definidos y explicados, asegurando una relación entre las variables físicas del convertidor. Basados en el modelo propuesto, dos lazos cerrados de control compuestos por controladores lineales Proporcionales e Integrales (PI) son propuestos. Algunas consideraciones de diseño para dimensionar los elementos reactivos son incluidas, de tal forma que se obtienen valores mínimos para su inductancia y capacitancia. Se presenta la implementación de un prototipo de 900 W con resultados experimentales que permite validar y reafirmar el modelo propuesto. Los resultados experimentales demuestran que el uso del convertidor PFC permite elevar el factor de potencia ***FP*** a 0,99 o más y reducir el THD_i (Total Harmonic Distortion of the Current por sus siglas en Inglés) a 3,9 %, además de controlar el bus DC en la salida. Se verifica experimentalmente que el convertidor PFC desarrollado está de acuerdo con los estándares de calidad de la potencia EN 61000-3-2 (IEC 1000-3-2).

1. Introduction

AC-DC power converters, also known as rectifiers, allow obtaining direct current from an AC power source. Rectifiers are widely used in applications such as consumer electronics products, switching power supplies, uninterrupted power supplies and charging systems for hybrid vehicles [1, 2]. Usually, conventional rectifiers are reliable and easy to design. These rectifiers are composed of a full bridge-diode and a capacitor. The capacitor charge leads to current peaks in the source; consequently, the use of conventional rectifiers in AC distribution systems is responsible for increments in the THD_i, reducing the Power Factor PF and efficiency of distribution networks [1, 2].

An increase of the THD_i in distribution networks can lead to higher power losses in cables, transformers and generators. Besides, a high THD_i can cause the magnification of resonant currents, failures in protection devices, and degradation of voltage waveform in large-impedance lines [2-4].

Compliance of power quality standards such as IEEE 519-20142 [5] and IEC 61000-3-2 suggests decreasing the THD_i, improving the PF and reducing the Electromagnetic Interference (EMI) [6].

The reduction of the THD_i and increase in PF at the source can be achieved by using passive filters or controlled rectifiers. Usually, passive filters are tuned LC filters [7]. Capacitors and inductors used in such filters exhibit high

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cost, volume and weight [8]. Moreover, controlled rectifiers are more efficient than passive filters. These rectifiers operate based on power switches and have one or more closed-loop control systems [9]. Controlled rectifiers can regulate PF, reduce THD_i and control DC voltage at the load [8,10,11].

Some AC-DC controlled converters with PFC reported by technical literature are: conventional boost rectifier composed of diodes bridge and boost converter [12-14], AC-DC interleaved boost converter [15, 16], and bridgeless boost PFC converter [17-19].

Conventional boost rectifier is the most common topology among the AC-DC converters [2, 16]. It offers a simple way to achieve high PF and regulated output voltage. Nevertheless, losses from the diode bridge rectifier are significant, particularly at lower input voltage and high output [3].

The bridgeless PFC boost converter has one semiconductor less in the line-current path from source to load, reducing power losses and improving efficiency, in comparison with conventional boost rectifier [20]. The bridgeless PFC boost converter can supply up to 3.5 kW of power to the load and can reduce the ripple voltage in load and the ripple current in source. Moreover, inductors are located on the AC side facilitating its design and EMI filtering [17-22].

A literature review of the bridgeless PFC boost converter and some experimental tests have been reported in [2]. A comparative evaluation of conventional boost rectifier, AC-DC interleaved PFC boost converter and bridgeless PFC boost converter has been presented in [1]. This work demonstrated experimentally that the bridgeless PFC boost converter is more efficient than conventional boost rectifiers. In [17, 18], an improved bridgeless PFC boost topology is proposed to reduce common mode noise. A novel technique for measuring the source current and implementation of the bridgeless PFC boost converter prototype has been introduced in [23]. A calculation of switching losses and an experimental development of the bridgeless PFC boost converter have been explained and analyzed in [21]. An analysis of the THD_i and a laboratory prototype of the bridgeless PFC boost converter have been presented in [23]. A topology with soft switching, a control strategy and an experimental approach of bridgeless PFC boost have been proposed in [3].

Although a great variety of studies have been conducted regarding the design of bridgeless PFC boost converter, the reviewed technical literature does not report the phenomenological modeling of the bridgeless PFC boost converter that allows model-based controller design, sizing of components, and analysis of its dynamics, as well as losses and performance in extreme conditions.

This paper proposes an averaged small-signal model for the bridgeless PFC boost converter that allows knowing the dynamic performance of the converter prior to its experimental implementation and the systematic design of the control system. This modeling approach could easily be generalized to other converter topologies [24]. In addition, this paper presents the principle of operation, control system design, design equations, implementation of a laboratory prototype of 900 W and experimental results that corroborate the theoretical approaches.

In this paper, the operating principle of the bridgeless PFC boost converter is studied in section II. The averaged large-signal and averaged small-signal model of the bridgeless PFC boost converter are proposed in section III and IV, respectively. The design of control systems is presented in section V. Design considerations and experimental results are given in section VI and VII, respectively. Finally, conclusions are presented in section VIII.

2. Operating Principle

This section presents the operating principle and mathematical model of the bridgeless boost PFC converter. This model represents the relationship of physical variables in the power converter. Power converters switches work in cut-off and saturation regions; consequently, the bridgeless PFC boost converter exhibits a nonlinear and time-varying dynamic behavior [24, 25].

The bridgeless PFC boost converter presented in this study works in Continuous Conduction Mode (CCM). Figure 1 shows the bridgeless PFC boost converter topology. This topology is composed of two power switches Q_1 and Q_2, two fast switching diodes D_1 and D_2, two conventional rectifier diodes D_3 and D_4, two inductors with same values L_1 and L_2, a capacitor C, and a load R_L [17-19].

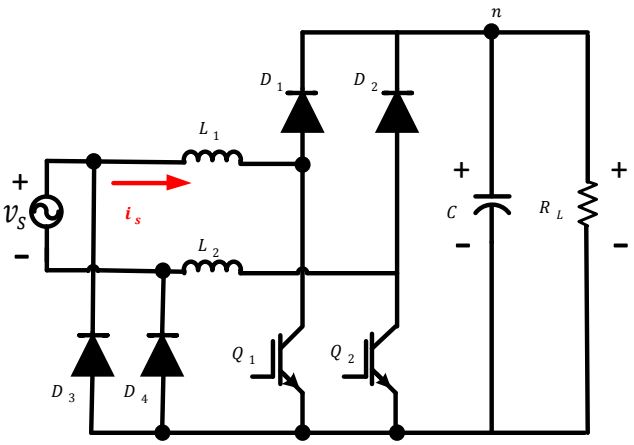

Figure 1 Bridgless PFC boost converter topology

The proposed bridgeless PFC boost converter model is obtained based on Kirchhoff's and Ohm's laws, and the commutation states of switches Q_1 and Q_2. Then, the averaged large-signal model is achieved averaging the switched model on one switching period [26]. Subsequently, the model is linearized using small variations around an operating point, obtaining the small-signal model. Finally, the model is transformed into the state-space and S domain [25, 26].

Enhancing the accuracy of the model adds complexity to it; increasing the time required for the simulation and the complexity of the control system design. Moreover, increasing the model complexity does not provide significant information about the dominant dynamic behavior of the converter [27-29]. Consequently, the model proposed in this paper is obtained based on the next simplifying assumptions: 1) switches are considered "ideal", i.e. they have zero-value resistance during conduction and infinite-value resistance when the switch is turned off; 2) switching time is infinitely short; 3) sources are considered "ideal", i.e. the voltage source provides infinite short circuit power; 3) passive elements are considered linear, time-invariant and without parasitic series resistance; and 4) switching frequency is much higher than input voltage frequency, i.e. amplitude variations in the source are not significant in one switching period (T_{SW}).

The bridgeless PFC boost converter has four operating modes. The controlled commutation of Q_1 and Q_2 during positive and negative half cycles of the AC input voltage allows output voltage regulation and input current tracking control. Figure 2 shows the four operating modes of the bridgeless PFC boost converter.

Next section describes the operating modes of the bridgeless PFC boost converter and the equations that compose the switched model.

2.1. Operating Mode 1

In operating mode 1, the input voltage (v_s) is positive and Q_1 is turned on; moreover, Q_1 and D_4 are directly polarized. Input current (i_s) increases exponentially, storing energy in inductor L_1. Simultaneously, C supplies power to the load (R_L), reducing the output voltage (v_c). The current of the capacitor (i_c) is assumed positive when it charges the capacitor. The mathematical relationship of voltages and currents in the equivalent circuit for operating mode 1 is given by Eqs. (1) and (2):

$$\frac{di_s}{dt} = \frac{v_s}{L_1} \tag{1}$$

$$\frac{dv_c}{dt} = -\frac{v_c}{R_L C} \tag{2}$$

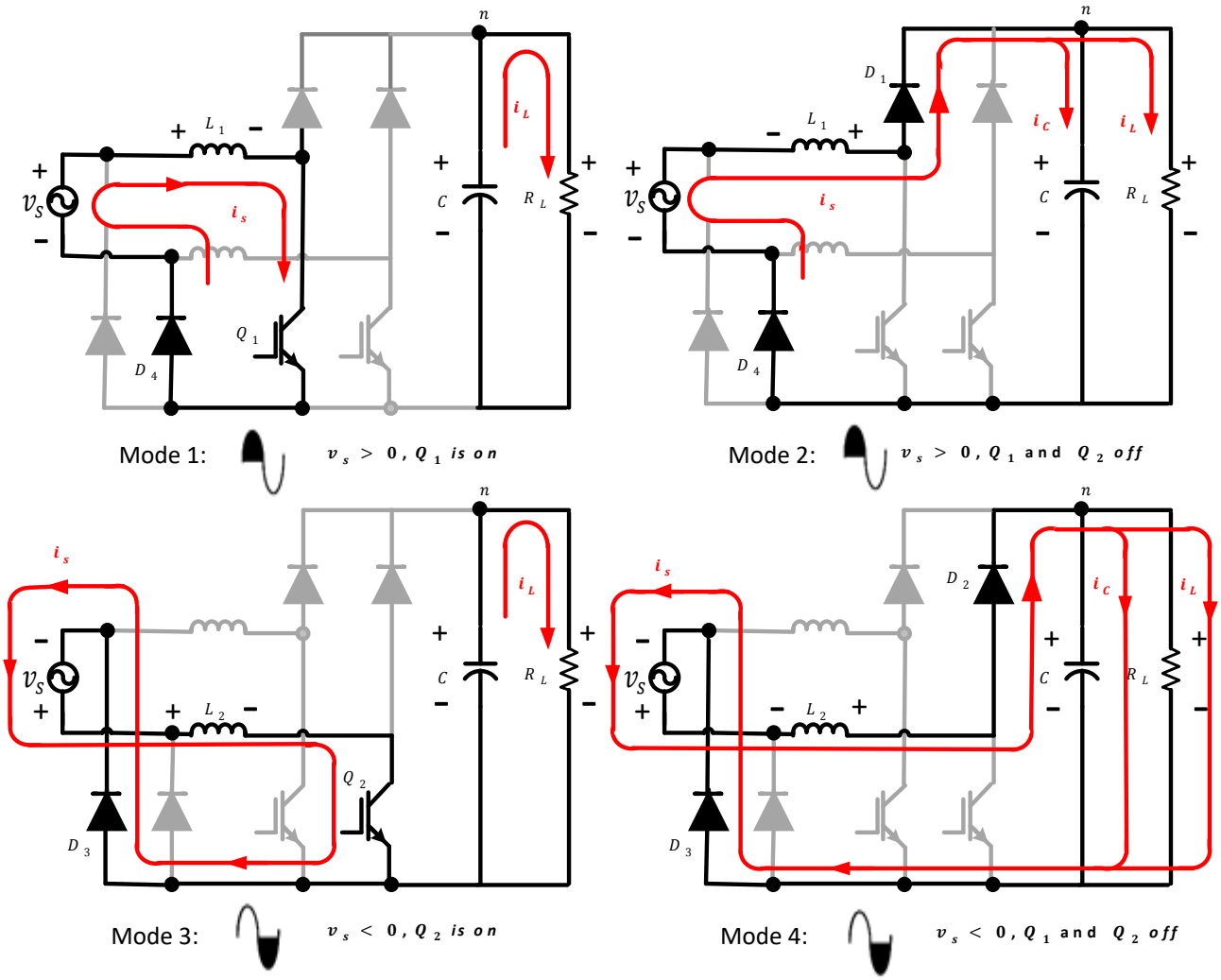

Figure 2 Operating modes of the bridgeless PFC boost converter

2.2. Operating Mode 2

In operating mode 2, v_s is positive and Q_1 and Q_2 are turned off; moreover, D_1 and D_4 are directly polarized. v_s and the voltage induced in L_1 are added, supplying power to R_L and C. v_c rises exponentially, incrementing i_c; simultaneously, i_s is reduced. The mathematical relationship of voltages and currents in the equivalent circuit for operating mode 2 is given by Eqs. (3) to (5):

$$\frac{di_s}{dt} = \frac{1}{L_1}(v_s - v_c) \tag{3}$$

$$i_s = i_c + i_L \tag{4}$$

$$\frac{dv_c}{dt} = \frac{i_s}{C} - \frac{v_c}{R_L C} \tag{5}$$

Where i_L is the load current.

2.3. Operating Mode 3

In operating mode 3, v_s is negative and Q_2 is turned on; moreover, Q_2 and D_3 are directly polarized. i_s increases, storing energy in inductor L_2. Simultaneously, C supplies power to R_L, reducing v_c. The mathematical relationship of voltages and currents in the equivalent circuit for operating mode 3 is given by Eqs. (6) and (7):

$$\frac{di_s}{dt} = \frac{v_s}{L_2} \tag{6}$$

$$\frac{dv_c}{dt} = -\frac{v_c}{R_L C} \tag{7}$$

2.4. Operating Mode 4

In operating mode 4, v_s is negative and Q_1 and Q_2 are turned off; moreover, D_2 and D_3 are directly polarized. v_s and the voltage induced in L_2 are added, supplying power to R_L and C. The mathematical relationship of voltages and currents in the equivalent circuit for operating mode 4 is given by Eqs. (8) and (9):

$$\frac{di_s}{dt} = \frac{1}{L_2}(v_s - v_c) \tag{8}$$

$$\frac{dv_c}{dt} = \frac{i_s}{C} - \frac{v_c}{R_L C} \tag{9}$$

3. Averaged large-signal model of the bridgeless PFC Boost converter

The averaged large-signal model replicates the average behavior of the power converter and it can be obtained based on switched model. The error between the averaged model and real behavior of the bridgeless PFC boost converter is negligible for control purposes. This is due to the fact that the converter cross-over frequency (f_c) is much lower than the switching frequency, i.e. $f_c \ll f_{sw}$. The averaged large-signal model is computed over a switching period (T_{sw}). Current and voltage ripples are neglected in the averaged model in one T_{sw}. This switching period is sufficiently small in relation to the system dynamics, representing the low-frequency behavior of the power converter [25, 26].

The averaged large-signal model neglects high-frequency dynamics caused by the switching of Q_1 and Q_2. The result is a continuous-time model that does not take into account high frequency dynamics [26]. The bridgeless PFC boost converter can be modeled with a second order model, due to the fact that inductors L_1 and L_2 have the same value. For subsequent analysis $L_1 = L_2 = L$. This converter can be described by means of state equations for each switching interval as shown below. The state-space model describes the differential equations of the circuits depicted in Figure 2 in canonical form, where i_S and v_L are the components of the state variables vector (x). The state-space model when Q_1 and Q_2 are turned on (t_{on}), i.e. in 1 and 3 operating modes is given by Eq. (10):

$$\underbrace{\begin{bmatrix} \frac{di_s}{dt} \\ \frac{dv_c}{dt} \end{bmatrix}}_{\dot{x}} = \underbrace{\begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{R_L C} \end{bmatrix}}_{A_1} \underbrace{\begin{bmatrix} i_s \\ v_c \end{bmatrix}}_{x} + \underbrace{\begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}}_{B_1} v_s \tag{10}$$

Where A_1 and B_1 denote coefficient matrices in operating modes 1 and 3. The state-space model when Q_1 and Q_2 are turned off (t_{off}), i.e. in 2 and 4 operating modes is defined in (11).

$$\underbrace{\begin{bmatrix} \frac{di_s}{dt} \\ \frac{dv_L}{dt} \end{bmatrix}}_{\dot{x}} = \underbrace{\begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{R_L C} \end{bmatrix}}_{A_2} \underbrace{\begin{bmatrix} i_s \\ v_c \end{bmatrix}}_{x} + \underbrace{\begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}}_{B_2} v_s \tag{11}$$

Where A_2 and B_2 denote coefficient matrices in operating modes 2 and 4, respectively.

The averaged large-signal model requires that i_S and v_c are time-continuous variables, i.e. i_S and v_c cannot change abruptly in the limit between t_{on} and t_{off}. This model can be calculated in Eqs. (12) and (13):

$$\dot{x} = (A_1 x + B_1 v_s)D + (A_2 x + B_2 v_s)D' \tag{12}$$

$$\dot{x} = \underbrace{(A_1 D + A_2 D')}_{A} x + \underbrace{(B_1 D + B_2 D')}_{B} v_s \tag{13}$$

Where A and B are the coefficient matrices of the averaged large-signal model of the bridgeless PFC boost converter, D is a duty cycle, $D' = 1 - D$, $t_{on} = D \cdot T_{sw}$, and $t_{off} = (1 - D) \cdot T_{sw}$. Coefficients of A and B matrices are given in (14).

$$\dot{x} = \underbrace{\begin{bmatrix} 0 & -\frac{(D-1)}{L} \\ \frac{(D-1)}{C} & -\frac{1}{R_L C} \end{bmatrix}}_{A} x + \underbrace{\begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}}_{B} v_s \tag{14}$$

4. Averaged small-signal model of the bridgeless PFC Boost converter

The bridgeless PFC boost converter can be perturbed by small variations in v_s, causing small variations in i_S and v_c with respect to their steady state values. The control system must modify D to control i_S and v_c state variables. These variations around the equilibrium point can be expressed by (15).

$$D = \overline{D} + \hat{d} \; ; \; v_s = \overline{V}_s + \hat{v}_s \; ; \; x = \overline{X} + \hat{x} \tag{15}$$

Where $\overline{D}$, $\overline{V}_s$ and $\overline{X}$ denote values in the equilibrium point; and $\hat{d}$, $\hat{v}_s$ and $\hat{x}$ are small-signal variations around the equilibrium point.

The averaged model can be rewritten, replacing D, vs and x from (15) into (14) as shown in (16).

$$\frac{d}{dt}(\overline{X} + \hat{x}) = [A_1(\overline{D} + \hat{d}) + A_2(1 - \overline{D} - \hat{d})](\overline{X} + \hat{x}) + [B_1(\overline{D} + \hat{d}) + B_2(1 - \overline{D} - \hat{d})](\overline{V}_s + \hat{v}_s) \tag{16}$$

Where $\frac{d}{dt}(\overline{X}) = 0$

Eq. (16) represents a non-linear model of the bridgeless PFC boost converter, since it exhibits the product of time-dependent variables. The non-linear model can be linearized based on the following assumptions: $\overline{V}s, \gg \hat{v}s$, $X \gg \hat{x}, D \gg \hat{d}$, i.e., variations of signals around the equilibrium point are small in comparison with the signal magnitude. Consequently, the magnitudes of $\hat{d}\hat{v}_s$ and $\hat{d}\hat{x}$ are negligible in comparison with the magnitudes of $\overline{V}_s$, X and D, i.e. $\hat{d}\hat{v}_s \cong 0$ and $\hat{d}\hat{x} = 0$. The non-linear model can be obtained from the previous assumptions and it is given by (17).

$$\dot{\hat{x}} = A\overline{X} + B\overline{V}_s + A\hat{x} + B\hat{v}_s + [(A_1 - A_2)\overline{X} + (B_1 - B_2)\overline{V}_s]\hat{d} \tag{17}$$

4.1. Operating Point

The operating point and the steady-state model is obtained by setting all the time derivatives given in (17) to zero, such as expressed by expressions (18) to (20). Note that, the matrix A must be invertible for appropriating solution of the equations:

$$\frac{d}{dt}\overline{X} = A\overline{X} + B\overline{V}_s = 0 \tag{18}$$

$$\overline{X} = -A^{-1}B\,\overline{V}_s \tag{19}$$

$$\overline{X} = \begin{bmatrix} \overline{i_s} \\ \overline{v_c} \end{bmatrix} = \begin{bmatrix} \dfrac{\overline{V}_s}{R_L\,(1-D)^2} \\ \dfrac{\overline{V}_s}{(1-D)} \end{bmatrix} \tag{20}$$

4.2. Linearized state-space model of the bridgeless PFC Boost converter

Linear control laws can be obtained based on the linearization of the model around an operating point. The linearized state-space small-signal model of the bridgeless PFC boost converter can be calculated replacing, (13) and (16) in (15). The linearized model around the operating point can be expressed by (21) and (22):

$$\frac{d\hat{x}(t)}{dt} \triangleq A\,\hat{x} + B\,\hat{v}_s + \underbrace{[(A_1 - A_2)\,\overline{X} + (B_1 - B_2)\overline{V}_s]}_{K}\hat{d} \tag{21}$$

$$\frac{d}{dt}\begin{bmatrix} \hat{i}_s \\ \hat{v}_c \end{bmatrix} \triangleq \underbrace{\begin{bmatrix} 0 & -\dfrac{D'}{L} \\ \dfrac{D'}{C} & -\dfrac{1}{R_L C} \end{bmatrix}}_{A}\begin{bmatrix} \hat{i}_s \\ \hat{v}_c \end{bmatrix} + \underbrace{\begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix}}_{B}\hat{v}_s + \underbrace{\begin{bmatrix} \dfrac{\overline{V}_s}{L\,(1-D)} \\ -\dfrac{\overline{V}_s}{R_L C\,(1-D)^2} \end{bmatrix}}_{K}\hat{d} \tag{22}$$

4.3. S-domain model of the bridgeless PFC Boost converter

The bridgeless PFC boost converter transfer functions can be derived from the linearized state-space small-signal model. The relation between the state and output variables is given by the following assumptions, Eqs. (23) and (24):

$$\frac{\hat{X}(s)}{\hat{V}_s(s)} = (sI - A)^{-1}B, \qquad with\ \hat{d} = 0 \tag{23}$$

$$\frac{\hat{X}(s)}{\hat{d}(s)} = (sI - A)^{-1}K, \qquad with\ \hat{v}_s = 0 \tag{24}$$

Eqs. (25) to (29) show the bridgeless PFC boost converter transfer functions.

$$\frac{\hat{X}(s)}{\hat{d}(s)} = \frac{\begin{bmatrix} \hat{I}_s(s) \\ \hat{V}_L(s) \end{bmatrix}}{\hat{d}(s)} \triangleq \frac{1}{s^2 + \dfrac{s}{R_L C} + \dfrac{D'^2}{LC}}\begin{bmatrix} \left(S + \dfrac{1}{R_L C}\right)\left(\dfrac{\overline{V}_s}{L\,D'}\right) + \dfrac{\overline{V}_s\,D'}{R_L LC\,D'^2} \\ \dfrac{\overline{V}_s}{LC} - \dfrac{\overline{V}_s\,s}{R_L C D'^2} \end{bmatrix} \tag{25}$$

$$\left.\frac{\hat{v}_c(s)}{\hat{d}(s)}\right|_{\hat{v}_s(s)=0} \triangleq \frac{\overline{V}_s}{(1-D)^2}\,\frac{\left(1 - \dfrac{L}{R_L(1-D)^2}\,s\right)}{\dfrac{LC}{(1-D)^2}\,s^2 + \dfrac{L}{R_L\,(1-D)^2}\,s + 1} \tag{26}$$

$$\left.\frac{\hat{\imath}_s(s)}{\hat{d}(s)}\right|_{\hat{v}_s(s)=0} \triangleq \frac{\overline{V}_s}{R_L(1-D)^3}\,\frac{(2+R_L C\,s)}{\frac{LC}{(1-D)^2}\,s^2+\frac{L}{R_L\,(1-D)^2}\,s+1} \quad (27)$$

$$\left.\frac{\hat{v}_c(s)}{\hat{v}_s(s)}\right|_{\hat{d}(s)=0} \triangleq \frac{1}{(1-D)}\,\frac{1}{\frac{LC}{(1-D)^2}\,s^2+\frac{L}{R_L(1-D)^2}\,s+1} \quad (28)$$

$$\left.\frac{\hat{\imath}_s(s)}{\hat{v}_s(s)}\right|_{\hat{d}(s)=0} \triangleq \frac{1}{R_L\,(1-D)^2}\,\frac{1+R_L C\,s}{\frac{LC}{(1-D)^2}\,s^2+\frac{L}{R_L\,(1-D)^2}\,s+1} \quad (29)$$

5. Design of control systems

The bridgeless PFC boost converter presented in this study exhibits a two-loop cascade control structure composed of Proportional-Integral (PI) lineal controllers as shown in Figure 3. The two feedback loops are an inner current control loop and an outer voltage control loop; two-loop cascade control is proposed to eliminate the non-minimum phase behavior of the output voltage [9]. Simulation and design of the control loops were performed using Matlab.

The inner and fast current control-loop is designed to track the waveform of v_s, allowing unity *PF to be achieved*. i_S exhibits fast dynamics and its control system must ensure high bandwidth and fast time response; nevertheless, the current control system must reject the switching noise at f_{sw}. The bandwidth of the current controller (BW_i) must be small in comparison with f_{sw}. This work uses $BW_i \leq 10 \cdot f_{sw}$ [9, 30, 31]. Outer and slow voltage control-loop is designed to regulate v_L. The bandwidth of the voltage controller (BW_v) must be small in comparison with BW_i. This work uses $BW_v \leq 10 \cdot BW_i$. In addition, the voltage control loop must reject the oscillations caused by the ripple voltage in input, i.e. $BW_v \leq$ 120Hz. The voltage control system can also reduce the steady-state error, using an integral control action. The cascade control system must reject perturbations caused by small variations of input voltage and load current [9, 30, 31].

In the control system shown in Figure 3, v_c is filtered whit low pass filter (F_v) to reduce the harmonics of 120 Hz. v_c filtered signal is compared with the set point voltage (V_{ref}), producing the voltage error signal (e_v). e_v is processed with the PI voltage controller (C_v). The voltage control output signal (I_{ref}) is multiplied by |sin (ωt)|, providing the reference signal to the current control (i_{ref}). i_{ref} exhibits the I_{ref} amplitude and $|v_s|$ waveform. The measuring signal of i_s is compared

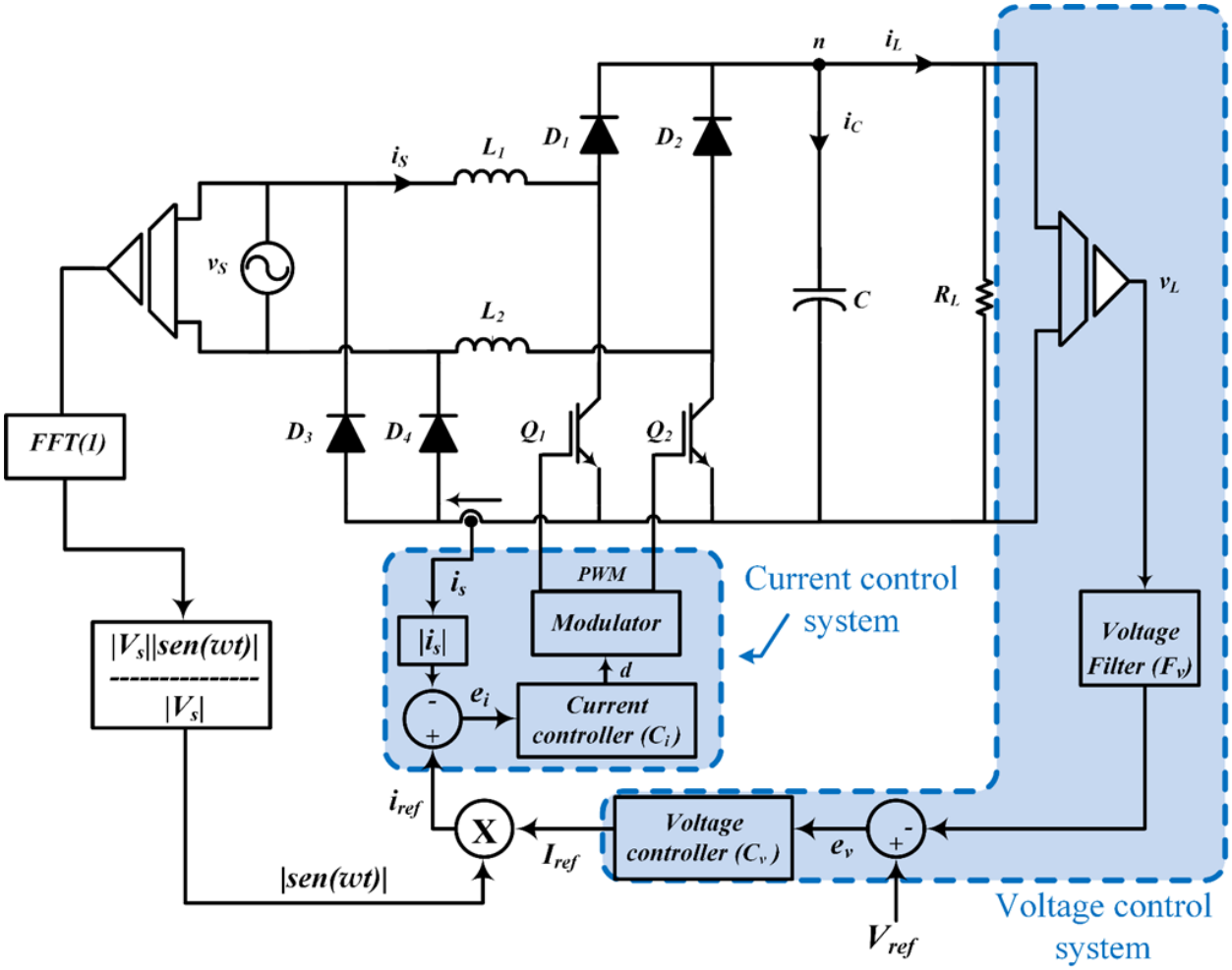

Figure 3 Control system of the bridgeless PFC boost converter

with i_{ref}, obtaining the current error signal (e_i). e_i is processed by the PI current controller (C_i). The current control output signal (d) is compared with a triangular signal in the *Modulator* to generate the Pulse-Width Modulation (PWM) signal for switching Q_1 and Q_2. The switching frequency depends on the triangular signal frequency. *FFT* provides the fundamental harmonic waveform of v_s, such waveform is the reference waveform for i_s, avoiding the bridgeless PFC boost converter to inject new harmonic currents to the distribution network [32].

Figure 4 shows the blocks diagram of the control system. G_i is the transfer function of $\hat{i}_s$ with respect to $\hat{d}$ and G_v is the transfer function of $\hat{v}_c$ with respect to $\hat{i}_s$.

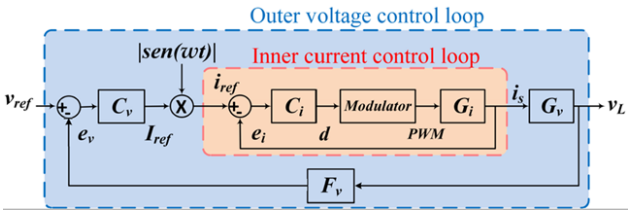

Figure 4 Blocks diagram of the bridgeless PFC boost converter control system

6. Design considerations

6.1. Calculating equations for the reactive elements of the bridgeless PFC Boost converter

Inductors L_1 and L_2 are used as boost inductors and as a filter to minimize the input current ripple, whereas the output capacitor C is used to minimize the output voltage ripple. The inductors and capacitor values can be determined using the equations that model the dynamic behavior of the converter in operating modes 1 and 3. L_1 and L_2 values are calculated with (1) and the following assumptions: 1) i_s is linear with respect to time, i.e. $dt \triangleq \Delta t$ and $di \triangleq \Delta i_s$; 2) the bridgeless PFC boost converter operates in CCM; 3) $f_{SW} \gg f_{LINE}$, where f_{LINE} is line frequency of 60 Hz; and 4) v_s changes are small in T_{ON}, i.e. $v_s \triangleq \bar{V}_s$ in T_{ON}. Besides, L_1 and L_2 values must be designed to work in the most extreme conditions and they can have the same value (L). Eq. (1) can be modified based on previous assumptions as shown in (30).

$$L = \frac{\bar{V}_s \, \Delta t}{\Delta i_s} = \frac{\bar{V}_s \, T_{ON}}{\Delta i_s} = \frac{\bar{V}_s \, D \, T_{SW}}{\Delta i_s} \tag{30}$$

Where D can be determined from (20) as shown in (31).

$$D = 1 - \frac{\bar{V}_s}{\bar{V}_L} \tag{31}$$

L value in extreme working conditions can be calculated based on (30) and (31) and it is given by expression (32):

$$L \geq \frac{v_{s(min)} \left(v_{L(max)} - v_{s\,(min)} \right)}{\Delta i_{s(max)} \, f_{SW} \, v_{L(max)}} \tag{32}$$

The maximum current trough L_1 and L_2 ($I_{s[max]}$) is presented when P_{out} is maximum and V_{in} is minimum. $I_{s[max]}$ determines the wire gauge of the inductors. $I_{s[max]}$ can be calculated by (33):

$$I_{s(max)} = \frac{\sqrt{2} \, P_{out(max)}}{\eta \, V_{in(min)}} \tag{33}$$

Where η is the expected efficiency of the bridgeless PFC boost converter.

C value must be designed to work in the most extreme conditions. C value can be calculated replacing the current and voltage in (2) and it is given by (34):

$$C \geq \frac{i_{L(max)} \, \Delta t}{\Delta v_{L(max)}} = \frac{i_{L(max)}}{2 \, f_{line} \, \Delta v_{L(max)}} \tag{34}$$

Where v_c is linear with respect to time, i.e. $dt \triangleq \Delta t$ and $dv_c \triangleq \Delta v_c$.

6.2. Functional specifications and values of components of the bridgeless PFC Boost converter.

Table 1 shows the functional specifications of the bridgeless PFC boost converter implemented for laboratory testing.

Table 2 shows values and references of elements of the bridgeless PFC boost converter implemented for laboratory testing. These elements are selected based on (32), (33) and (34).

6.3. Modulator transfer function

The PWM signal is generated by comparison between d and a signal of triangular waveform. The triangular signal is selected to have unitary amplitude and f_{SW} frequency. Eq. (35) shows the transfer function of modulator block.

$$PWM(s) = \frac{1}{\overline{v_{triang}}} = 1 \tag{35}$$

Where $\overline{v_{triang}}$ is the amplitude of the triangular signal.

6.4. Design of low-pass Filter F_v

The low-pass filter F_v is composed of an integrator as shown in (36). The integration time (T_i) is set to reach the desired cross-over frequency to 31Hz.

$$F_v(s) = \frac{1}{1 + T_i \, s} = \frac{1}{1 + 0.005 \, S} \tag{36}$$

Table 1 Functional Specifications of the bridgeless PFC boost converter

Symbol	Quantity	Value
$V_{in(min)}$	Minimum input voltage	152.7 V
$V_{in(max)}$	Maximum input voltage	186.7 V
f_L	Line frequency	60 Hz
V_c	Regulated output voltage	200 V
$V_{c(\max)}$	Maximum regulated output voltage	350 V
$P_{out(\max)}$	Maximum output power	900 W
f_{sw}	Switching frequency	40 kHz
$\Delta v_{c(max)}$	Output voltage ripple	10 V
$\Delta i_{s(max)}$	Input current ripple	0.5 A

Table 2 Value of bridgeless PFC boost converter components

Symbol	Component	Value/Model
L_1-L_2	Inductors	3.75 mH
C	Capacitor	2.5 mF
D_3-D_4	Rectifier diodes	KBPC1510, 10A, 1000V
Q_1-Q_2	Power switches	IGBT IRG4PC50UD
D_1-D_2	Fast switching diodes	QH12T Z600, 600V, 12A

Figure 5 shows the $F_v(s)$ Bode diagram. In low frequencies, the magnitude of Bode diagram is zero proving unitary gain.

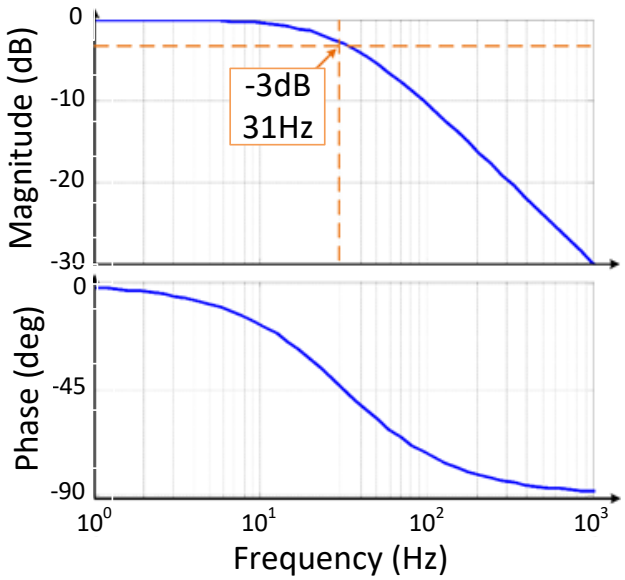

Figure 5 Bode diagram of $Fv(s)$ low-pass filter

6.5. Design of current control system

Linear controllers are designed to work around an operating point, however, the bridgeless PFC boost converter can operate with variations in load and amplitude of the input supply. The PI controllers are set to work in the middle of the load line. The operating point selected is V_{in} = 169,7 V_p,V_L=200V_{DC}, and P_{out} = 450W. The transfer function of current system is shown in (37). This transfer function is defined based on: Eq. (27), data values shown in Tables 1 and 2, and the defined operating point, see Eq. (35).

$$G_i = \frac{\hat{\imath}_s(s)}{\hat{d}(s)} = \\ = \frac{0.694\,\mathrm{s} + 6.251}{1.302\,\mathrm{x}\,10^{-5}\,\mathrm{s}^2 + 5.86\mathrm{x}\,10^{-5}\,\mathrm{s} + 1} \quad (37)$$

Eq. (38) shows the conjugate and complex roots of G_i. The real components of these roots are negative; in consequence, the current system of the bridgeless PFC boost converter is inherently stable in open loop.

$$r_{1,2} = -2.25 \pm 277.11i \quad (38)$$

Control systems can be tuned using the root-locus method and the Bode-diagrams. The root-locus method allows analyzing the effect of the gain variations over the poles allocation and absolute stability of the system. Bode-diagrams permit determining bandwidth of current and voltage systems in open and close loop. This tuning permits selecting the appropriate parameters of PI controller to achieve desired system behavior in closed loop [32]. The transfer function of current controller is given by (39):

$$C_i(s) = K_{pi} + \frac{K_{ii}}{s} = \frac{K_{pi}s + K_{ii}}{s} \quad (39)$$

Where K_{pi} *and* K_{ii} are the proportional and integral gains of the PI controller, respectively. Transfer function of the current system in close loop is shown in (40).

$$G_{i\_LC}(s) = \frac{\hat{\imath}_s(s)}{i_{s\_ref}(s)} = \frac{C_i(s)\,G_i(s)}{1 + C_i(s)\,G_i(s)} \quad (40)$$

The bandwidth of the current control system is set to reject the switching noise, i.e. the current control in closed-loop should reject noise at 40kHz and it must track to i_{ref}.

Eq. (41) shows the transfer function of the current controller. K_{pi} and K_{ii} are selected to reach the expected performance of the current system in close loop ($BW_i \leq 10 \cdot f_{sw}$, $BW_v \leq 10 \cdot BW_i$).

$$C_i(s) = \frac{K_{pi}s + K_{ii}}{s} = \frac{0{,}12s + 34}{s} \quad (41)$$

Figures 6 and 7 show the pole-zero plot and Bode plot, respectively. These plots allow comparison between open loop and close loop behavior of the current system. Figure 6 shows that the close-loop eigenvalues are in the left half-plane of pole-zero plot; therefore, the closed-loop system has absolute stability. Figure 7 shows that the feedback loop reduces the resonance peak and the closed-loop exhibits unity gain for frequencies below 1kHz. This current control system allows filtering noise at switching frequency, working as a low-pass filter.

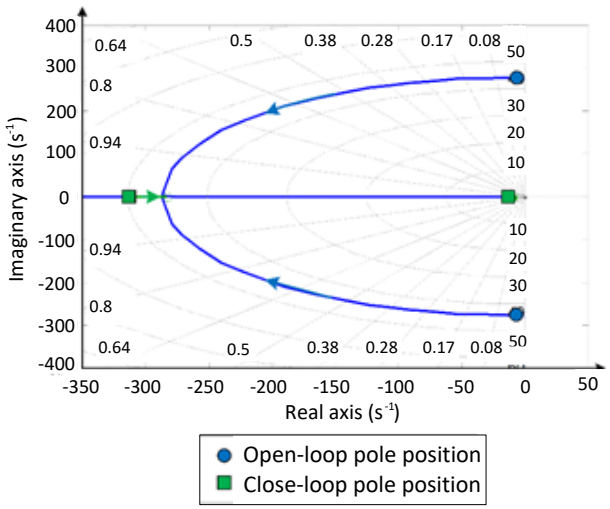

Figure 6 Pole-zero plot of dominants poles of $G_i(s)$ current system

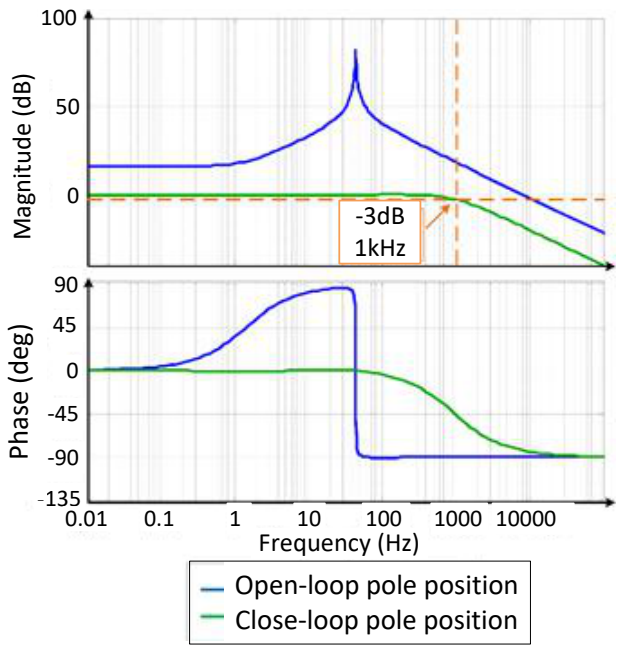

Figure 7 Bode diagram of $G_i(s)$ current system

6.6. Design of voltage control system

Rectification in the bridgeless PFC boost converter causes a low frequency ripple in the DC-link voltage at 120Hz. This ripple may induce undesired current amplitude variations. The voltage controller must reject such ripple.

G_v transfer function is shown in equation Eq. (42) and it is defined based on Eqs. (25-29) and Tables 1 and 2.

$$G_v(s) = \frac{\hat{v}_c(s)}{\hat{\imath}_s(s)} = \frac{\bar{V}_s}{2\,\bar{V}_c}\,\frac{R_L}{R_L C s + 1} = \frac{37{,}7}{0.22s + 1} \quad (42)$$

Eq. (43) shows the root of the voltage system. The real component of this root is negative. In consequence, the voltage system of the bridgeless PFC boost converter is inherently stable in open loop.

$$r_1 = -4{,}5 \quad (43)$$

Table 3 shows the expected performance specifications of voltage system in close loop

Table 3 Expected performance specification of voltage system

Parameter	Value
Steady-stable error	<3%
Stabilization time	<1s

The voltage control system must regulate the output voltage in the bridgeless PFC boost converter, reducing or removing the steady-state error. Integral control action is required in this case. Eq. (44) shows the transfer function of the voltage controller.

$$C_v(s) = K_{pv} + \frac{K_{iv}}{s} = \frac{K_{pv}s + K_{iv}}{s} = \frac{0{,}5s + 0{,}3}{s} \quad (44)$$

Where K_{pv} is the proportional gain and K_{iv} is the integration gain in the voltage controller. K_{pv} and K_{iv} are selected to reach the expected time performance of the voltage system in close loop shown in Table 3. Transfer function of voltage control system in closed-loop is given in the Eq. (45):

$$G_{v\_LC}(s) = \frac{\hat{v}_c(s)}{v_{c\_ref}(s)} = \frac{C_v(s)\,G_{i\_LC}(s)\,G_v(s)}{1 + C_v(s)\,G_{i\_LC}(s)\,G_v(s)\,F_v(s)} \quad (45)$$

Figures 8 and 9 show pole-zero plot and Bode plot, respectively. These plots allow comparison between open and close loop behavior of the voltage system. Figure 8 shows that the close-loop eigenvalues are in the left half-plane of pole-zero plot; therefore, the closed-loop system has absolute stability. Figure 9 shows that the voltage system exhibits unity gain for frequencies below 22Hz. This voltage control system helps F_v filter to reject the 120Hz ripple, working as a low-pass filter. Furthermore, the bandwidth of the voltage system in closed-loop is 45 times smaller than the current system in closed-loop; consequently, the extern control-loop is slow in comparison with the inner control-loop.

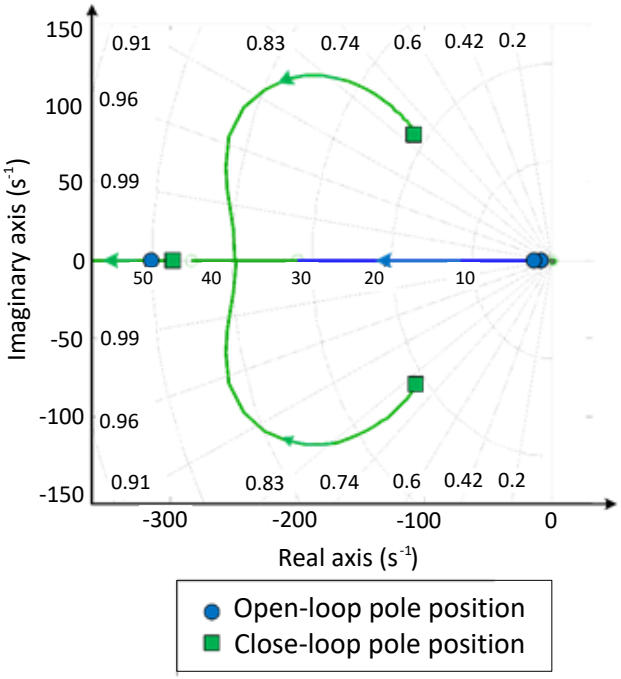

Figure 8 Pole-zero plot of dominants poles of $G_v(s)$ current system

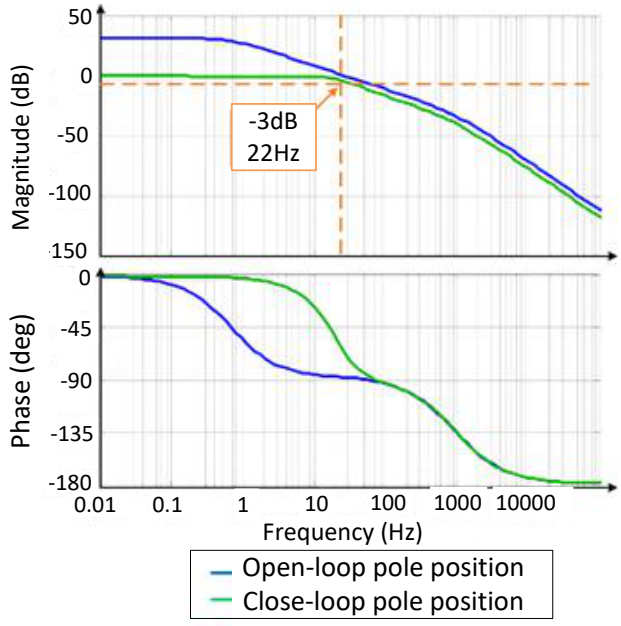

Figure 9 Bode diagram of $G_v(s)$ voltage system

7. Experimental results

A 900 W bridge PFC boost prototype was built in order to validate the proposed approach. The converter topology and control scheme are shown in Figure 3. Values of components and functional specifications of the bridgeless PFC boost converter are given in Tables 1 and 2. Power switches formed by Q_1 and Q_2 operate at 40kHz. The input voltage is almost sinusoidal, so that the PFC boost converter operates for low values of THD_v less than 2%.

LEM LV25-P and LEM LAH50-P were used for sensing voltage and current, respectively. The control system was implemented in the digital platform Single-Board Rio of National Instruments. The control algorithms were programed in LabVIEW Software. The experimental setup is shown in Figure 10.

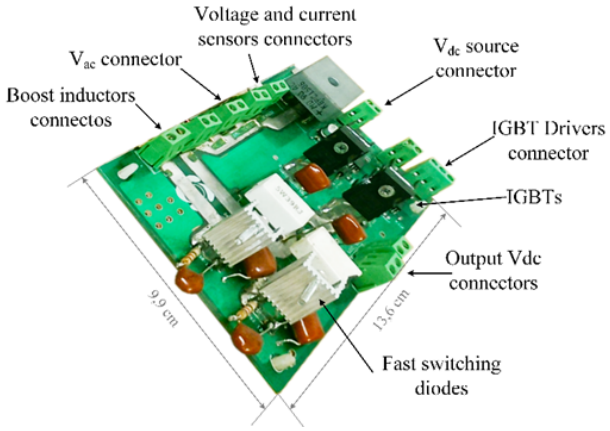

Figure 10 Bridgeless PFC boost converter prototype implementation

PF, THD_i and efficiency calculations were performed offline with relation to the output power level. The performance of the prototype was tested from 200W to 900W. Tests were performed at 111Vca, 120Vca and 129Vca in the source.

The *PF* in the source of the bridgeless PFC boost converter with relation to output power levels is shown in Figure 11. The *PF* in the source is 0.58 when the control system is turned off. The *PF* is higher than 0.993 when the control system is turned on. Tests results show that current controller allows significantly the PF in the source to be improved.

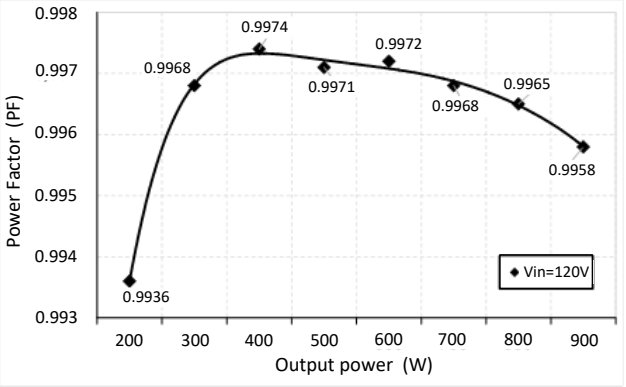

Figure 11 *PF* on the source of the bridgeless PFC boost converter with relation to output power levels

The efficiency of the bridgeless PFC boost converter with relation to output power levels is shown in Figure 12. Efficiency trend of the bridgeless PFC boost converter is decreasing in the evaluated output power range. Experimental tests show that efficiency decreases from 99.2% to 88.55% in the range from 200W to 900W. This efficiency reduction is caused by the increase in

switching and conduction losses when the output power is incremented.

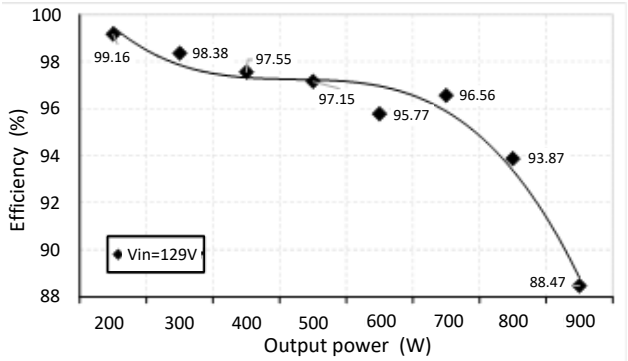

Figure 12 Efficiency of the bridgeless PFC boost converter with relation to output power levels

The THD_i of the bridgeless PFC boost converter with relation to output power levels is shown in Figure 13. Experimental tests were performed at 111Vca, 120Vca and 129Vca in the source. The THD_i is 137.4% when the control system is turned off, and is reduced until it reaches a value of 3.9% when the control system is turned on. Tests results show that the current control system in close loop reduces significantly the THD_i. Moreover, tests results in Figure 13 show that the THD_i increase is related with the increment of the input voltage amplitude.

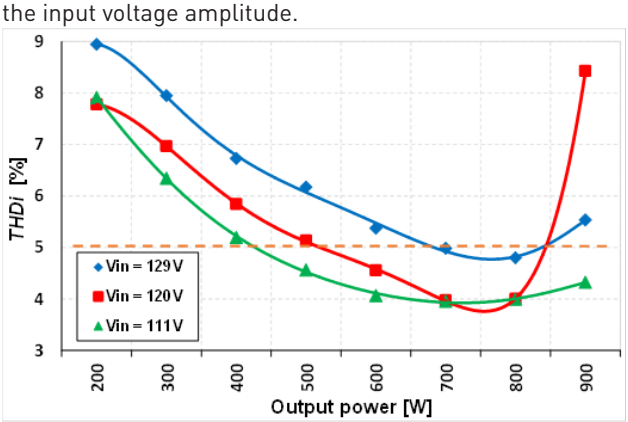

Figure 13 THD_i of the bridgeless PFC boost converter with relation to output power levels at 111Vca, 120Vca and 129Vca in the source

Harmonic orders in the input current with relation to EN 61000-3-2 class A and IEC 1000-3-3 class A standards are shown in Figure 14. Experimental tests were performed at 800W; using 111Vca, 120Vca and 129Vca. Experimental tests show that THD_i reduction allows complying 61000-3-2 class A and IEC 1000-3-3 class A standards in the complete operating range, assuring good power quality in the source. Therefore, the control design must comply with robustness requirements that ensure acceptable performance over the entire operating range.

The bridgeless PFC boost converter operates at 800W; and 111Vca, 120Vca and 129Vca. Figures 11, 12 and 13 show that the reduction of the THD_i improves PF in the

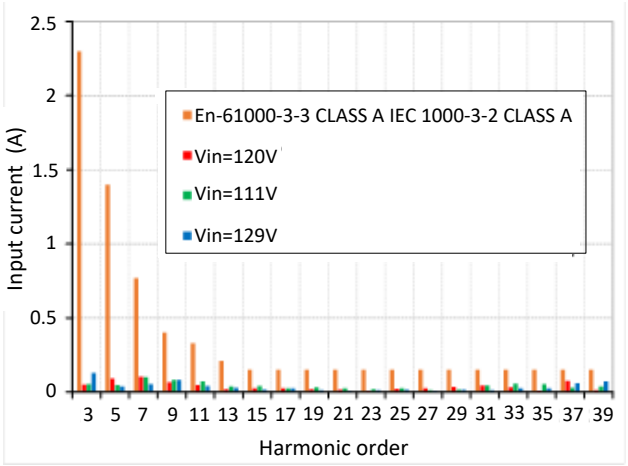

Figure 14 Harmonics order in the input current whit relation to EN 61000-3-2 class A and IEC 1000-3-3 class A standards

source, consequently the system efficiency is increased. Experimental waveforms of i_s, v_s and v_c are given in Figure 15. The input current is in phase with the input voltage. This current has a sinusoidal shape. The current control system modifies shape and phase of the input current. Moreover, the voltage control system permits regulating output voltage and to reduce 120Hz ripple. The output voltage value is greater than the input voltage value, due to the fact that the induced voltage in L_1 and L_2 allows raising the output voltage.

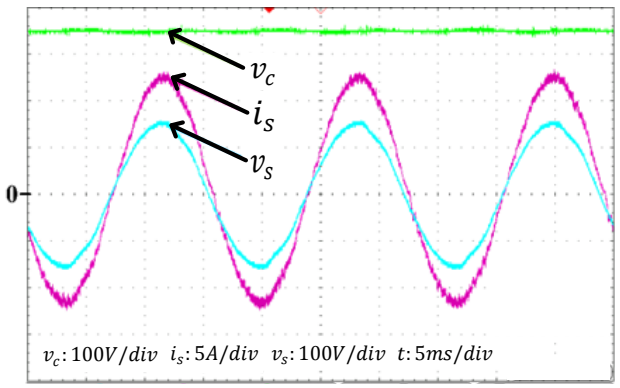

Figure 15 i_s, v_s and v_L measured on of the bridgeless PFC boost converter at P = 908.5W, PF=0.9962, THD_i = 4.3% and η=91.91%

Experimental waveforms of i_s, v_s and v_c with load variations are given in Figure 16. This test was obtained by varing the reference current. The load current was changed from 3.7A to 1.55A, this caused a variation in the output power from 523W to 219W, respectively. The dotted orange line represents the reference output voltage value (200Vdc). The cascade control system regulates the output voltage and tracks the reference current with sinusoidal waveform. The response time of the output voltage value was 922ms. The output current variation in this test corresponds to 50% of maximun current. Selected parameters for linear control system allow apropiate dynamic response in the complete operating range.

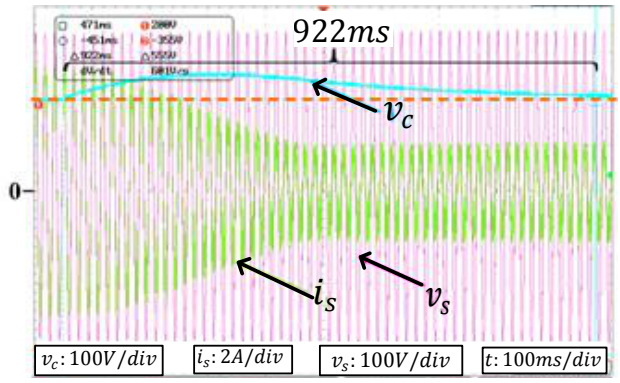

Figure 16 i_s, v_s and v_c measured on the bridgeless PFC boost converter. Initial conditions: v_{cref} = 200Vdc, P = 448W, i_s=3.7A$_{RMS}$, Final conditions v_{cref} = 200Vdc,P = 180W, i_s=1.55A$_{RMS}$, response time = 922ms

8. Conclusions

Detailed analysis of the bridgelees PFC boost converter topology in terms of modelling, control and experimental validation has been presented. Experimental results demonstrate that the bridgeless PFC boost converter allows elevating the *PF* up to 0.99, to reduce the THD_i to 3.9% and to control the DC voltage level on output. Compliance of standards of power quality EN 61000-3-2 (IEC 1000-3-2) is experimentally verified in a laboratory prototype of 900 W.

The averaged small-signal model proposed in this paper allows analyzing the dynamic performance of the converter prior to its experimental implementation. This model also allows the systematic design of the control system. This model replicates the average behavior of the power converter around the operational point. The error between averaged model and real behavior of the bridgeless PFC boost converter is negligible for control design purposes. The theoretical approaches have been verified experimentally and the expected performance has been achieved.

Experimental tests allow determining that the proposed model, use for control purposes, significantly reduces the harmonic distortion in input current; consequently, the power factor and efficiency are incremented. Moreover, the voltage control reduces the ripple voltage in load despite the variations of input line.

9. Acknowledgment

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