A NOVEL CMOS ANALOG NEURAL OSCILLATOR CELL

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Abstract- **A very flexible programmable CMOS analog neural oscillator cell architecture is presented. The proposed neuron circuit architecture is a hysteretic neural-type pulse oscillator. Its implementation consists of a transconductance comparator, a capacitor and two non-linear resistors. It has over nine decades of oscillation frequency range, i.e., $10^{-2}Hz \leq f_{osc} \leq 20MHz$. This range has been experimentally verified. The oscillator cell in the test-chip was implemented in a standard $3\mu m$ (p-well), double-metal CMOS technology, and has a dimension of about $44,000\mu m^2$ (without the capacitor). Preliminary measurements and simulated results agree very well.**

I. Introduction

The interest in neural networks is old, one main reason has been the potential to solve difficult complex engineering problems [1] - [4] that could not be easily and practically solved with conventional approaches. Using synthetic neural networks, researchers try to mimic human-like performance to solve engineering problems such as control systems, including optimization, learning and adaptive systems, also strong interest exists for speech and image recognition. A renovated interest in neural networks has arisen in the engineering scientific community among others. One of the main driving forces behind this renovated interest lies in the fact that a very large number of highly interconnected arrays of basic cells (neurons) can be, in principle, efficiently fabricated as integrated circuits. Several recent results [4] - [5] of implemented neural networks in CMOS technology show promising potential applications [2], [3], [10] and [13]. Another attractive property of a neural network is its great fault tolerance and degree of robustness.

A basic nerve cell is called a neuron. Biological neurons are permanently sending electrochemical signals back and forth to each other and modifying their communication lines with every new experience. Several researchers (see Refs. 7.1 and 7.3 in [1]) considered the brain as being associated with an energy surface whose valleys correspond to stable repeatable brain response. External stimulus determines the initial point of the energy surface. The brain, by means of firing sequency of pulses changing dynamically, reaches a stable pattern that corresponds to a valley floor on the surface. This energy surface question can be interpreted as the conventional minimization or optimization of a function often found in engineering problems (i.e., control system, circuit design, etc.), and where a stable pattern is the corresponding minimum of a function.

A neuron has both *on* (excitatory) and *off* (inhibitory) connections, the output consists of positive[1] (or negative) packages of pulses for excitatory (or inhibitory) output signal. Neurons are interconnected through synapses. A synapse can be considered as a weighted relation between the output of a neuron and the input received by another one. This relation can be modeled as inhibitory or excitatory. Interconnections form neural networks, however, researchers [13] have not agreed on precisely which part of the nervous system to model and the exact degree of fidelity. The complexity and variety of inherent algorithms associated with the human nervous system is astonishing.

Several crude mathematical models of neural nets have been reported in the literature [1] - [6], [9] where the basic model consists of a neuron producing an output determined by a weighted sum of inputs coming from other neuron outputs and external (stimuli) signals. The mathematical description [4], [7], [11] of the dynamic behavior of a neural network[2] with N neurons can be characterized by:

$$\frac{dx_i}{dt} = \underbrace{-A_i x_i}_{1} + \underbrace{I_{s_i}}_{2} + \underbrace{\sum_{j=0}^{N-1} (T_{ij} - \hat{T}_{ij}) V_j}_{3} \qquad (1)$$

x_i is the neural activity in neuron i, and can be interpreted as a voltage signal. In the above equation, Term 1 represents the passive decay of neural activity in the absence of all other signals (Terms 2 and 3), in which case $x_i(t)$ comes from a linear single time constant system and $x_i(t) = x_i(o)e^{-A_i t}$. Thus A_i is the self term. $1/A_i$ has units of time and can be inversely related to a time constant. Term 2 corresponds to external stimuli input signals I_{s_i} which can be interpreted as input current sources. Term 3 involves the synaptic weighting functions T_{ij}

[1] The positive (negative) packages of pulses are arbitrarily associated with the excitatory (inhibitory) output signal.

[2] Authors use different names for neural networks, such as neuromorphic systems, connectionist models, parallel distributed processing models, artificial neural nets or synthetic neural systems.

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and $\hat{T}_{ij}$ and the neuron state V_j. Note that T_{ij} and $\hat{T}_{ij}$ model the excitatory and inhibitory functions, respectively. V_j is the neural state which is related to the neural activity x_i by the non-linear activation function $f_j(\cdot)$, which bounds the values of V_j between a maximum and a minimum value as shown in Fig. 1, i.e., $V_j = f_j(x_j)$. Some authors use activation functions having a sharp transition as shown in Fig. 1(a); others use a function with a defined transition region between V_{jmax} and V_{jmin}, (Fig. 1(b)), and still others use functions with a soft transition as shown in Fig. 1(c); these last two activation functions are also known as sigmoids.

A variation of (1) where hysteretic elements [1], [4] – [8] are used instead of an activation function (i.e., Term 3 is modified) can be described[3] as:

$$\frac{dx_i}{dt} = -A_i x_i + I_{ei} - \underbrace{A_{h_i} H_i(x_i,\ V_i)}_{3} \tag{2a}$$

$$V_i = \sum_{j=0}^{N-1} (T_{ij} - \hat{T}_{ij}) f_j(x_j) \tag{2b}$$

where T_{ij}, $\hat{T}_{ij}$, $f_j(\cdot)$, A_i and I_{ei} are defined as before, A_{h_i} is a weighting non-negative constant and $H_i(x_i,\ V_i)$ describes a hysteresis type [6] – [8] of neuron model for a constant V_i, i.e.,

$$H(x_i,\ \text{const}) = \begin{cases} H_+ & \text{if } x < -x_- \\ -H_- & \text{if } x > -x_+ \\ \{H_+,\ -H_-\} & \text{if } -x_- < x_i < x_+ \\ [-H_-,\ H_+] & \text{if } x_i = -x_- \text{ or } x_i = x_+ \end{cases} \tag{3}$$

Fig. 2 illustrates the hysteresis loop characterized by (3). For the operation of a neural–oscillator a line crossing the origin (in Fig. 2) in the 1st and 3rd quadrant is needed; then the oscillation or no oscillation depends on the slope of the (linear) load line. Other equivalent oscillation mechanisms are possible for symmetric hysteresis loop and non–linear load resistors. One of these mechanisms is introduced later. Note that the asymmetry (for linear resistor loads) of this loop is required to guarantee the existence of one stable point [8] as will later be needed.

In this paper, we describe a CMOS analog neural oscillator cell that has some of the properties of a biological neuron. These inhibitory and excitatory properties are functions of the input sum exceeding (or not) a firing threshold level. The proposed cell is voltage programmable over a large oscillation frequency range.

II. Mathematical Approach

Let us rewrite (2) in a convenient form for our CMOS circuit implementation, that is for a single neuron characterized by the first–order state equations (for simplicity the subindice i is deleted):

$$C\frac{dx}{dt} = -Ax - G(u,\ x) + I_o(x) \tag{4}$$

where u = input, x = internal state variable, C is a non–negative constant, $I_o(x)$ is $-A_h H(x,\ V)$, and the input variable u controls the value of $G(u,\ x)$ and since the $u = I_s$ term has been incorporated in $G(u,\ x)$, it is no longer explicitly shown. The equilibrium points, neglecting the $-Ax$ term, are reached when $\frac{dx}{dt}|_{x=x_e} = 0$, resulting in

$$I_o(x_e) = G(u,\ x_e) \tag{5}$$

$G(u,\ x)$ is a nonlinear current which is defined as

$$i_N(x) = G(u,\ x) = \begin{cases} 0 & \text{for } x < 0 \\ m_1(u)x & \text{for } 0 < x < x_1(u) \\ m_2(u)x & \text{for } x_1(u) < x \end{cases} \tag{6}$$

The solutions of (5) for two different $G(u,\ x)$'s are pictorially shown in Fig. 3. Observe that the value of I_C modifies the slope $m_1(u)$, thus I_C must be a function of u. The mode of operation illustrated in Fig. 3(a) shows two equilibrium points, A and B, where A represents a stable point and B represents an unstable point. Thus, eventually the equilibrium point A is reached and x becomes x_e. Note that $x_e < V^+$. Thus $I_o(x_e) = I_b$. The mode of operation illustrated in Fig. 3(b) has two unstable points A' and B', therefore, the circuit oscillates trying to reach a stable point.

Next, we analyze (4) under this unstable mode of operation to determine the oscillating signal x. Assume $x(o) = 0$ and $I_o(0^+) = I_b$, then (4) becomes[4]

$$C\frac{dx}{dt} = -m_1 x + I_b \tag{7}$$

which solution yields

$$x(t) = \frac{I_b}{m_1}(1 - e^{-\frac{m_1}{C}t}) \tag{8}$$

This equation holds until $x(t)$ becomes V^+, (therefore, we assume $\frac{I_b}{m_1} > V^+$) at which time the output of the hysteretic element changes to $-I_b$ (we assume the ideal case where no time is taken in going from I_b to $-I_b$ on the hysteresis curve). Let t_1 be this time, with $x(t_1) = V^+$. Solving for t_1 we obtain:

$$t_1 = -\frac{C}{m_1} ln\left(1 - \frac{m_1 V^+}{I_b}\right) \tag{9}$$

after $t_1$the characterizing differential equation yields

$$C\frac{dx}{dt} = -I_b - m_1 x, \qquad \text{with} \qquad x(0) = V^+ \tag{10}$$

which solution is given by

$$x(t) = -\frac{I_b}{m_1}\left(1 - e^{-\frac{m_1}{C}t}\right) + V^+ e^{-\frac{m_1}{C}t} \tag{11}$$

This situation remains until t_2, where $x(t_2) = 0$. At this time $i_N(x)$ switches to 0 as per (6). Therefore, solving for t_2 we obtain

$$t_2 = \frac{C}{m_1} ln\left(1 + \frac{m_1 V^+}{I_b}\right) \tag{12}$$

Now the differential equation becomes

$$C\frac{dx}{dt} = -I_b \qquad \text{but with} \qquad x(0) = 0 \tag{13}$$

the solution is time linearly dependent and given by

$$x(t) = -\frac{I_b}{C}t \tag{14}$$

The time at which $I_o(x)$ changes from $-I_b$ to I_b occurs when in (14) $x(t_3) = -V^-$, thus t_3 results

$$t_3 = \frac{CV^-}{I_b} \tag{15}$$

The cycle is completed when the differential equation becomes

$$C\frac{dx}{dt} = I_b \qquad \text{with} \qquad x(0) = -V^- \tag{16}$$

and the solution becomes

[3] The physical meaning of the term $-A_i x_i$ in (2a) is different from (1).

[4] For the sake of simplicity $m_1(u)$ is simply denoted as m_1.

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$$x(t) = -V^- + \frac{I_b}{C}t \tag{17}$$

Thus $x(t_4) = 0$, thus resulting

$$t_4 = \frac{CV^-}{I_b} \tag{18}$$

The time diagram of the oscillation signals are illustrated in Fig. 4 where $\tau_1 = C/m_1$ and $\tau_2 = C/m_1$.

III. CMOS Neural Oscillator Circuit

The proposed neural oscillator cell architecture is shown in Fig. 5(a). This architecture consists of a hysteretic block, an integrator, and a non–linear resistor load R_{NL} related to $G(u, x)$. A more detailed block diagram of the oscillator cell is illustrated in Fig. 5(b) where the hysteretic element is shown to consist of a comparator connected with positive feedback and a non–linear load R_{NH}. The input (x) - output (I_o) characteristics of the hysteretic element (consisting of the comparator and non–linear resistor load) are given by

$$I_o = \begin{cases} I_b \ , & x < V^+ \\ -I_b \ , & x > -V^- \\ [-I_b, I_b] \ , & x = V^+ \ , \ -V^- \end{cases} \tag{19}$$

The corresponding characteristics of i_N for the non–linear resistor R_{NL} are given by (6). Observe that the output impedance of the comparator can be associated with the term $A_i x_i$ of (2a). The CMOS circuit implementation is shown in Fig. 5(c). Note that V_b controls the value of I_b through transistors M24, M21 and M9. M21 with M9 form a current mirror where the I_b current is injected. Transistors M1–M9 form the transconductance comparator, M10–M11 implements the non–linear resistor R_{NH}. Observe that R_{NH} consists of a diode connection of two transistors. Current I_{o2}, from Fig. 5(b), is obtained through M12P–M12N in Fig. 5(c). Transistors M22 and M23 allow us to have output currents of both polarities to be injected into other cells.

V_C determines the I_C (of Fig. 3) injected through M20 and current mirror (M13 and M18). V_C consists of an inherent value V_{C_o} (fixed) plus an input u. Furthermore, V_C determines the slope m_1 (see eqs (6) and (7)). The non–linear resistor load, R_{NL} is implemented by transistors M13 to M19. When $V_N(= x) < 0$, transistors M15 is off and the bias current, I_C (also refer to Fig. 3), of the differential pair goes through M14. Thus the current, i_N, through M17 and M19 is zero. When $V_N > 0$, M14 is non–conducting and M15 is on, and the current through M17 and M19 becomes I_C. That is $i_N = I_C$. Since transistors M14 and M15 do not have large (W/L) ratios, there is a smooth transition between the on and off states of this non–linear resistor. That is the reason the resistor, R_{NL} has been modeled by three piece–wise linear segments.

IV. Experimental Results

The circuit shown in Fig. 5(c) was implemented in a $3\mu m$ CMOS technology (through and thanks to MOSIS). A microphotograph of the CMOS analog neural oscillator–cell is shown in Fig. 6. The cell occupies an area of about $44,000\mu m^2$ without including the capacitor. In our case, we used either a $1pF$ capacitor or the parasitic capacitance at that node. All the (W/L) ratios of the transistors of Fig 5(c) are $7\mu m/5\mu m$.

The experimental results for an oscillating frequency of 19.96×10^6 Hz is shown in Fig. 7. The integrating capacitor for this result is the parasitic capacitance present at that output node. Fig. 8 shows simultaneously the voltages V_C and $x = (V_N)$,with $V_b = 3.98V$ for an oscillating frequency of about 92 KHz where V_b is the voltage producing I_b (see Fig. 5(b)). The oscillator–cell was capable of producing output pulses between 0.01 Hz and nearly 20 MHz. The experimental results for the dependance between the controlling voltage V_b and the oscillating frequencies are shown in Fig. 9.

V. Conclusions

We have extended our preliminary work on a programmable neural oscillator cell [8] using discrete components. The proposed monolithic cell is tunable over a range of 9 decades. It was built using ordinary double–metal $3\mu m$ CMOS technology and has potential for fast speed applications.

This neuron architecture has excellent voltage (or current) programmability properties. Extension of this neuron–oscillator cell to include the synaptic weighting functions as well as the nonlinear activition function is being considered. We are also currently investigating sound neural network architectures where the proposed cell can be fully exploited.

VI. Bibliography

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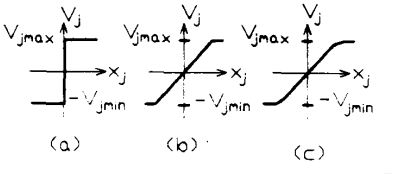


Fig. 1 Activation Function. (a) Step Type, (b) Hard Type and (c) Soft Limiting (Sigmoid) Type.

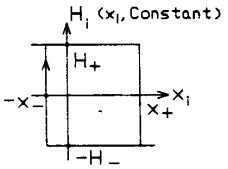


Fig. 2 Hysteresis Loop Characteristics of a Neuron Model.

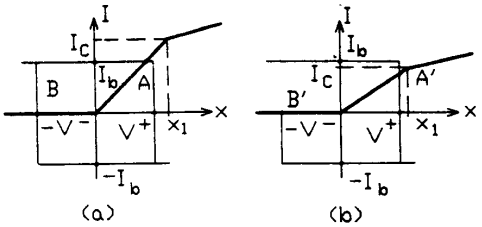


Fig. 3 Equilibrium Point Characteristics. (a) Stable Mode, (b) Oscillating Mode.

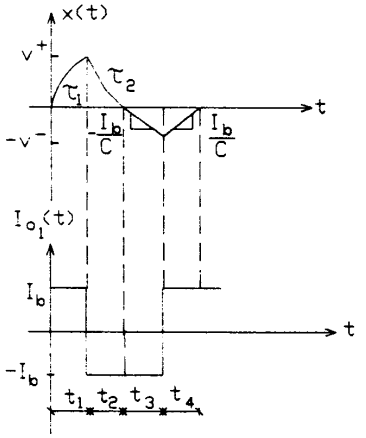


Fig. 4 Time Diagram of the Output $x(t)$ and $I_{o1}(t)$.

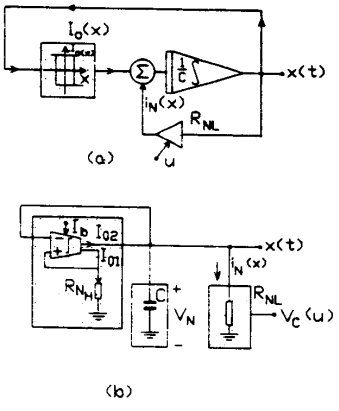
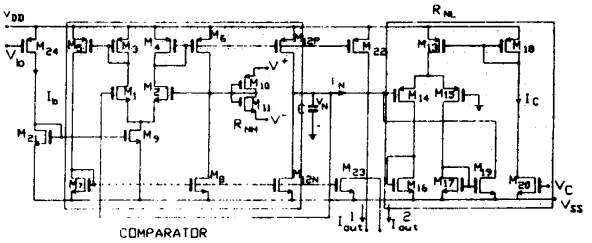


Fig. 5 Neural–Oscillator Cell Architecture. (a) Block Diagram, (b) More Detailed Block Diagram, and



(c) MOS Circuit Implementation $V_C = V_{C_p} + u$.

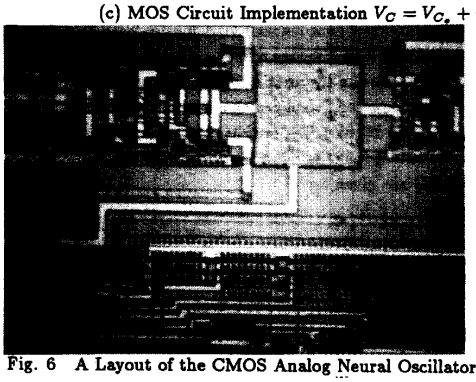


Fig. 6 A Layout of the CMOS Analog Neural Oscillator Cell.

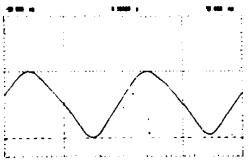


Fig. 7 Neural Oscillator Output. Oscillating Frequency 19.6 MHz.

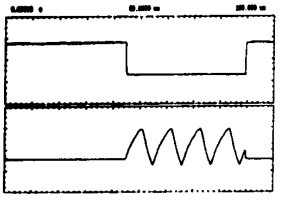


Fig. 8 V_C shown in the Upper Trace, and V_N in the Lower Trace. For an Oscillating Frequency of 92.0028 KHz.

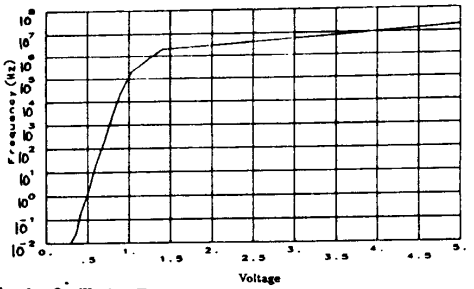


Fig. 9 Oscillating Frequency vs. Controlling Voltage V_b for $C = C_p$ (parasitic capacitance).

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Further information can be obtained from Dr. W. Kenneth Jenkins.