Space Vector Modulation Techniques for Multilevel Converters – a survey

L.G.Franquelo*, J.I. Leon, M.M.Prats and R.Portillo
* University of Seville/Electronics Engineering Department, Seville, Spain

***Abstract*— This paper presents a survey of most recent, simple and efficient Space Vector Modulation algorithms for multilevel converters. These algorithms avoid trigonometric and other complex operations, leading to more simple and cost efficient implementations. They can be applied to multilevel topologies and present freedom degrees that can be Exploited in order to optimize system parameters in the system like: capacitors voltages balancing or voltage/current ripples. Experimental results are presented to show the good performance of the algorithms.**

I. INTRODUCTION

Multilevel converters present great advantages compared to conventional and very well known two-level converters. These advantages are fundamentally focused on improvements in the quality of the output signals and an increase in the converter nominal power. These properties make multilevel converters very attractive to the industry and nowadays, researchers all over the world are spending great efforts trying to improve characteristics of multilevel converters as the control simplification and the performance of different optimization algorithms in order to enhance the output signals Total Harmonic Distortion (THD), the DC capacitors voltage balance, switching losses, load currents ripple, …, etc. However, the complexity of multilevel control algorithms has been an important drawback for their use in industrial applications especially when the number of levels of the converter is increased. Complex operations and look-up tables were normally used to carry out multilevel modulation strategies increasing the computational cost. Modulation strategies are complex algorithms that should be simplified in order to make easier the multilevel converters control.

The primary objective of a modulation strategy is to follow a voltage or current control reference obtaining a pulse train with the same averaged value over a switching period. Pulse Width Modulation (PWM) techniques were the first modulation algorithms to generate the switching signals to be applied to the transistor drivers. For multilevel converters, these techniques are systematic methods based on the comparison between the reference signal and several triangular carriers. Several possibilities appear because different relative carriers phase can be used. PWM methods can be carried out by hardware systems without any computational cost. On the other hand, multilevel converters present several important control problems as the balancing and ripple of the DC capacitors voltage that must be controlled by an external control loop. Carrier based PWM modulation methods do not permit to optimize the drivers switching in order to improve these parameters.

An alternative PWM method is the Space Vector Modulation (SVPWM). This modulation technique presents important advantages compared with classical carrier based PWM modulations. Using carrier based PWM, there is not too much freedom because only carriers amplitudes and carriers phases can be changed and these changes do not have direct influence to fulfill the control objectives. In front of this fact, SVPWM technique calculates the switching signals determining a switching sequence but the control algorithm can change the states vector order in the switching sequence to optimize control parameters in the converter. Besides, SVPWM algorithms introduce the redundant vectors concept and their important contribution to the converter control improvement.

II. STATE VECTOR SPACE FOR MULTILEVEL CONVERTERS

The state vectors space of a converter is defined as the representation of the output phase-to-neutral voltages (V_{PN}). In this work, three types of multilevel converters are considered: three-leg three-wire converters (3L3W), three-leg four-wire converters (3L4W) and four-leg four-wire (4L4W) converters. In general, for an N-level converter, each phase can obtain only N possible output V_{PN} voltages. Phase state *0* means that the phase electrical potential is the lowest possible and state *N-1* means that this electrical potential is the highest possible. Each state vector of the converter is defined as *xyz* where *x* is the state of phase *a*, *y* is the state of phase *b* and *z* is the state of phase *c*. If a fourth leg is taken into account (for 4L4W converters) each state vector is defined as *xyz|n* where *n* is the state of the fourth leg (that is connected to the neutral point of the load). These concepts are completely independent of the multilevel converter topology and they can be used with diode-clamped converters, flying-capacitor converters, cascade converters or generalized converter. Each topology will impose the phase states with different switching configurations but they have the same state vector space.

SVPWM considers a complex vector as the reference waveform to follow. This reference signal ($\vec{u}_{ref}$) is generated by means of an external control algorithm and it is sampled with a constant frequency. The converter generates it using a linear combination of the nearest state vectors determining their duty cycles. Hence, the output signal achieved by the converter is equal to the reference signal averaged over a sampling period.

III. 3L3W CONVERTERS

Considering this type of systems, V_{PN} γ coordinate is equal to zero. So, all state vectors are placed on the αβ plane and 3L3W converters state vectors space is reduced to a two dimensional problem. The two-level 3L3W converter state vectors space is shown in figure 1. State vectors '000' and '111' are placed in the same position in the plane. These state vectors are named redundant vectors and they are completely equivalent seen from the load because they apply the same phase to phase voltages to the load.

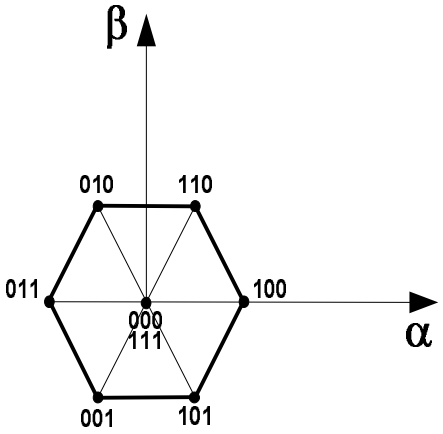

Figure 1. State vectors space for a two-level 3L3W converter

Increasing the number of levels, V_{PN} voltages can be determined and representing the state vectors space, new and external concentric hexagons appear. Besides, the redundancy of the state vectors increases if they are close to the origin. The state vectors space for a three level 3L3W converter is shown in figure 2.

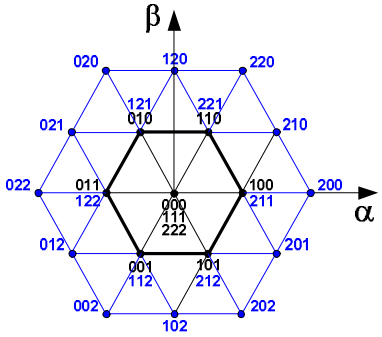

Figure 2. State vectors space for a three-level 3L3W converter

Any SVPWM algorithm has to carry out two different tasks. The first one is to identify the nearest state vectors to the reference vector. Second, duty cycles for each state vector have to be calculated. Several SVPWM algorithms for multilevel converters have been recently proposed [1][2][3]. However, an effective approach that reduces the computational cost using a decision-making algorithm was introduced in [4] based on the decision-based pulsewidth modulation for two level converters. The modulation algorithm input is the normalized reference voltage vector. The normalization depends on the number of levels of the multilevel converter and the voltage level value of the DC-link capacitors.

One of the most important contributions of [5] is that the normalised reference voltage vector u^* is transformed into u_{flat}. This transformation consists of scaling the imaginary part and multiplying it by $1/\sqrt{3}$. Using this transformation the two dimensional state vectors space for multilevel converter is flattened and after the transformation it is a hexagon where all the sectors are separated by 45º lines. This property is very useful due to the fact that the modulation algorithm can find out easily the sector where the reference vector is pointing to using different comparisons between real and imaginary parts of the complex transformed reference vector u_{flat}. This transformation makes possible to avoid complex on-line computations substituting them by simple decision making.

In [5], the search for the nearest vectors is solved for reference vectors in the first sextant. For reference vectors located in other sectors, the search is solved rotating the reference vector anti-clockwise by an angle $(n - 1)\pi/3$, where n is the sextant number, $n = 1,\ldots,6$. This rotation displaces any reference vector to the first sextant to be studied there. This algorithm improves the results of previous modulation algorithms due to the fact that its simplicity is very high. Nevertheless, there are several operations as the rotation to the first sextant and the inverse rotation to obtain the final switching sequence and the final on-state durations. In order to eliminate these complex operations, a new and faster modulation geometrical algorithm was proposed in [6]. This algorithm is based on some properties of the modulation algorithm presented before. In this case, the state vectors space is divided into three 120º possible zones and the same transformation presented above is applied to obtain u_{flat}, dividing the sectors by 45º lines. The determination of the nearest vectors uses this property to carry out the state vectors search easily and only doing simple comparisons. In figure 3, a 135º zone is represented. The search for the three nearest vectors is done thanks to comparisons between linear combinations of reference vector coordinates and their integer values. Graphically, the search is done doing comparisons between three 45º diagonal lines and two horizontal lines. So, the computational complexity is very low and the search is carried out very fast.

This geometrical algorithm drastically reduces the online calculations due to the fact that the modulation algorithm only implies very simple calculations. The switching sequence and the corresponding duty cycles are determined in the simplest way. An experimental result for this modulation algorithm using a 50KW three-level 3L3W diode clamped converter is shown in figure 4 where phase to neutral output modulated voltage is represented.

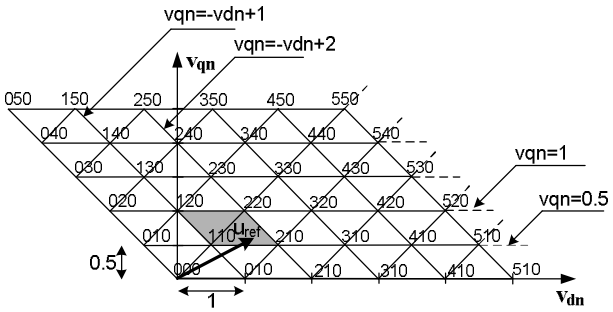

Figure 3. State vectors space of a 120º zone. States vector search using diagonal and horizontal lines doing easy comparisons

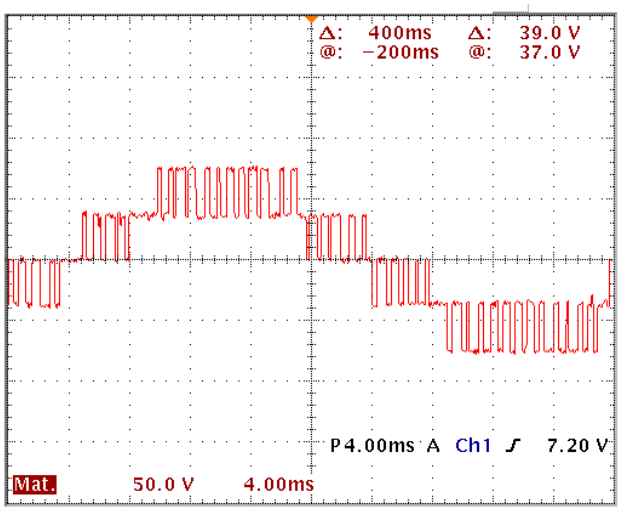

Figure 4. Switching results using modulation algorithm presented in [6] using a three-level 3L3W diode clamped converter

IV. 3L4W CONVERTERS

Three-phase converters can be implemented connecting the neutral point of the load to the middle point of the DC-link bus. These systems are named three-leg four-wire systems (3L4W systems). In figure 5 a three-level 3L4W diode clamped converter is shown. Using these converters, zero current can flow through the neutral wire and the phase currents could be not equilibrated. In this case, V_{PN} γ coordinate could be not equal to zero and the state vectors space only using the αβ plane can not be represented. Hence, 2D SVPWM algorithms can not be applied and three dimensional representation has to be used in order to represent V_{PN} voltages. In 3L4W converters, 3D SVPWM algorithms have to find out the four nearest vectors to the reference vector. This problem is graphically solved looking for the tetrahedron where the reference vector is pointing to because its vertexes are the four nearest state vectors to the reference vector [7].

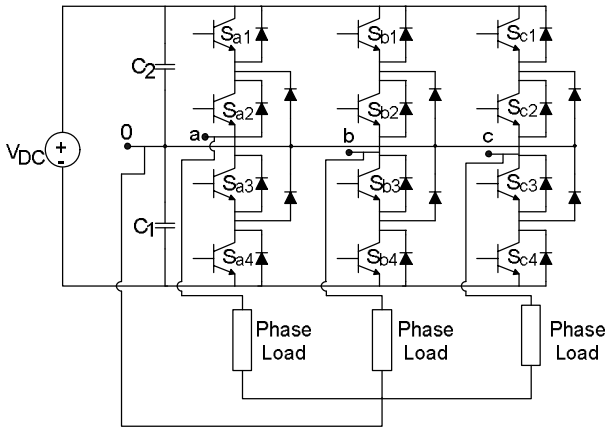

Figure 5. three-level 3L4W Diode-Clamped Converter

In 3L4W multilevel converter topologies, *abc* coordinates are used making 3D SVPWM algorithms more simple and more easily implemented. The state vectors space can be represented using *abc* coordinates instead αβγ coordinates and it is shown in figure 6 for the two-level case. The state vectors space is a cube where the state vectors are in the vertexes of the cube.

Increasing the number of levels of the converter, the state vectors space forms a control volume composed by several sub-cubes where the state vectors are the vertexes of the sub-cubes. In general, the state vectors space for an N-level 3L4W converter forms a cube in a 3D-space formed by $(N-1)^3$ sub-cubes where N is the number of levels of the multilevel converter. The state vectors space for a three-level 3L4W converter is shown in figure 7.

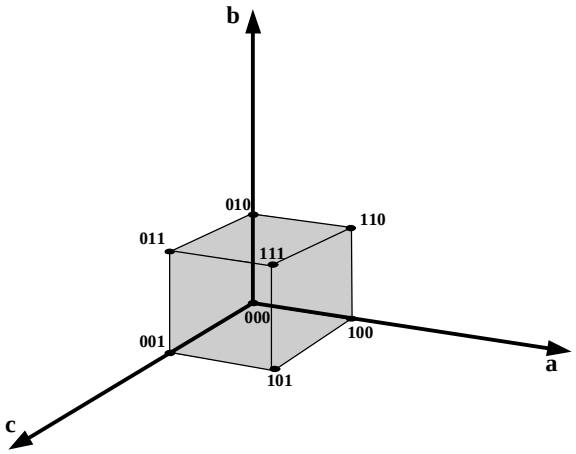

Figure 6. State vectors space for two-level 3L4W converter

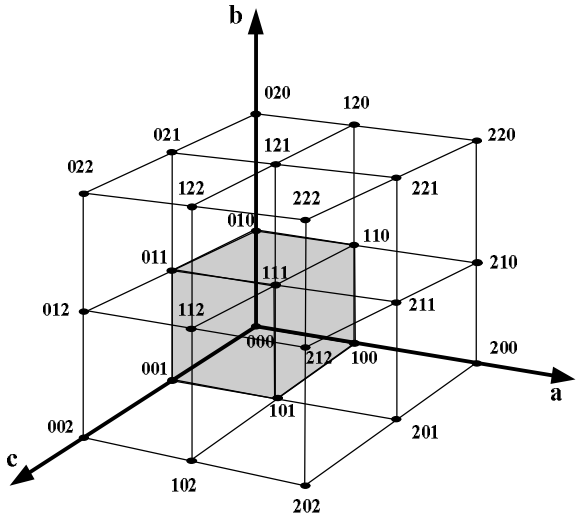

Figure 7. State vectors space for three-level 3L4W converters using *abc* coordinates

The most important 3D SVPWM algorithm for 3L4W converters is proposed in [7]. For a certain reference vector in *abc* coordinates (u_{an}, u_{bn}, u_{cn}), the integer part of each component (a, b, c) is calculated, where:

$$a = integer\ (u_{an})$$
$$b = integer\ (u_{bn})$$
$$c = integer\ (u_{cn})$$

These coordinates (a,b,c) are the origin coordinates corresponding to the reference system of the sub-cube where the reference vector is pointing to (see figure 8). Multilevel 3D SVPWM algorithm calculates the coordinates of the sub-cube reference vertex where the reference vector is located and reduces the N-level modulation problem to a two-level problem only considering this sub-cube. Each state vectors space sub-cube can be divided in six tetrahedrons (see figure 9). All diagonal planes that form the tetrahedrons are 45º planes doing very easy the comparisons to carry out the search for the nearest state vectors. The vertexes of the tetrahedrons are the state vectors that form the switching sequence. The two-level modulation problem is solved using very simple comparisons doing the search very efficient finding out the tetrahedron where the reference vector is pointing to. Experimental results for this 3D SVPWM strategy with a reference voltage with 33% of triple harmonics of fundamental component are shown in figure 10. The modulated output signals have been digitally filtered with a low pass filter that eliminates the highest frequencies. In this way, this permits to obtain the output phase to neutral voltages from 3L4W Diode Clamped inverter.

V. 4L4W CONVERTERS

In order to have better control over zero current the neutral point of the load can be connected to a new phase of the converter. These systems are named four-leg four-wire systems (4L4W systems). 4L4W two-level diode-clamped converter is shown in figure 11.

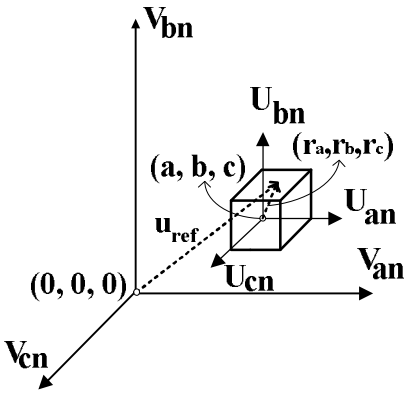

Figure 8. Sub-cube reference coordinates in generalized 3D SVPWM algorithms

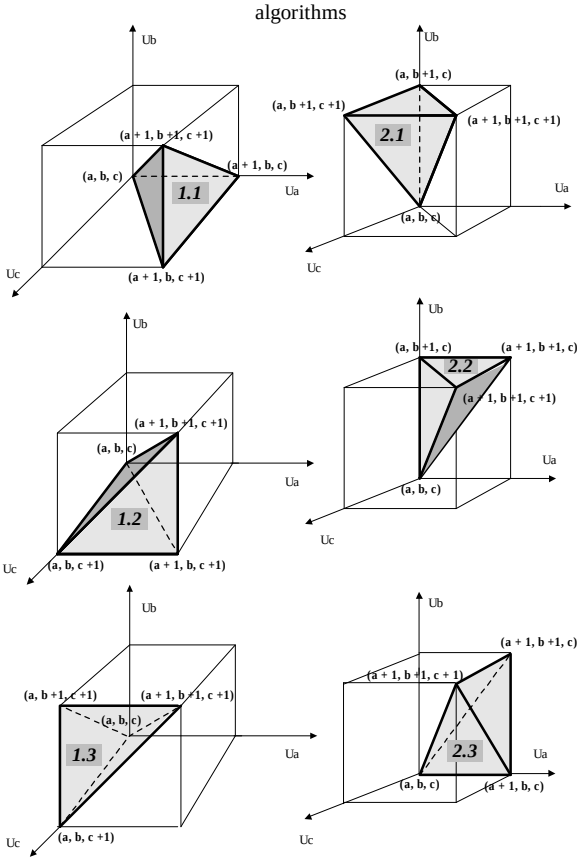

Figure 9. Possible tetrahedrons forming the state vectors space for two-level 3L4W converters

Previous works have represented the 3D state vectors space for 4L4W multilevel converters using αβγ coordinates [8]. However, a critical problem appears because using αβγ coordinates, possible volumes formed by the state vectors are not equal and systematic modulation algorithms are very difficult to develop. Several volume shapes appear and it is not easy to know the volume where the reference vector is pointing to. Some tetrahedrons formed by four state vectors using αβγ coordinates are represented in figure 12 showing the presence of not equal volumes doing 3D SVPWM algorithms very complex. In spite of it, some authors have developed modulation algorithms using αβγ coordinates. These algorithms are complex and the

computational cost is very high. This is the main drawback of this type of modulation algorithms. Using *abc* coordinates instead αβγ coordinates, the state vectors space for 4L4W multilevel converter forms a dodecahedron in a 3D-space [9]. The 3D-dodecaedron containing the state vectors which generate the reference vector in 4L4W three-level converter is shown in figure 13. As another example, 4L4W five-level converter is illustrated in figure 14.

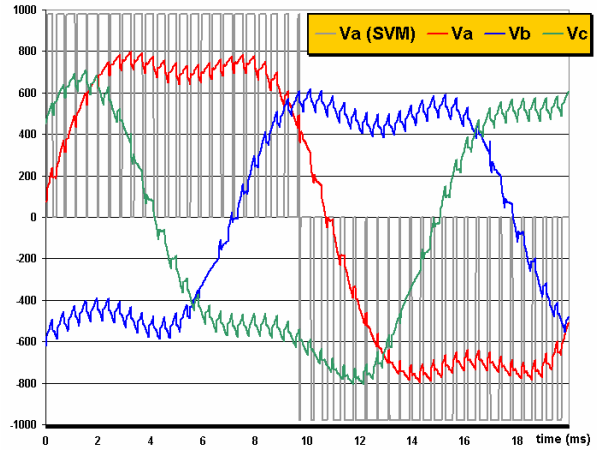

Figure 10. Phase to neutral voltages for 3D SVPWM algorithm for a three-level 3L4W diode clamped converter. Reference voltage with 33% of triple harmonics of fundamental component.

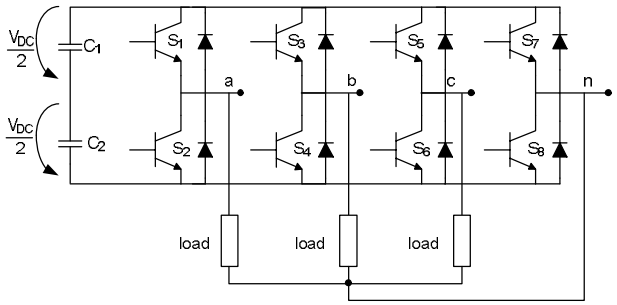

Figure 11. two-level 4L4W Diode Clamped Converter

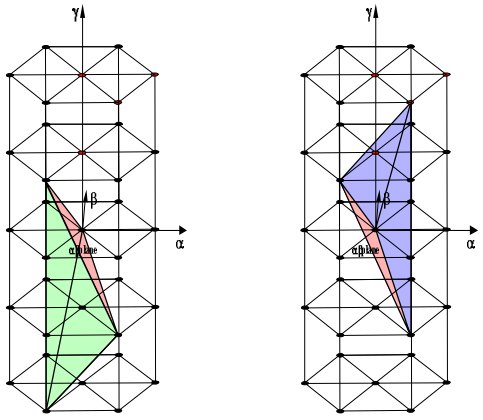

Figure 12. State vectors space for 3L4W converters using *abg* coordinates. The control volumes are not equal and modulation algorithms are complex

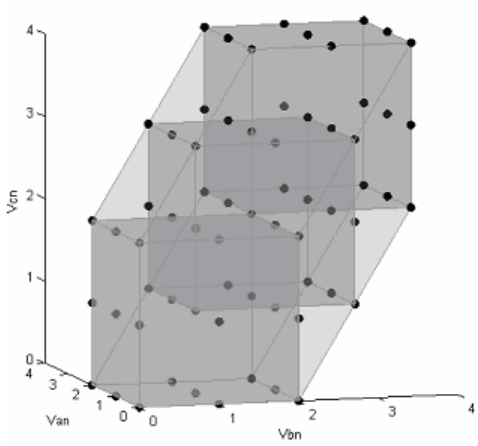

Figure 13. Generalized 3D space for 4L4W three-level converter

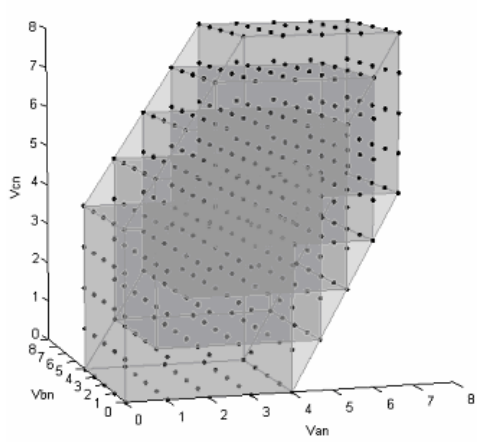

Figure 13. Generalized 3D space for 4L4W five-level converter

The 3D state vectors space can be decomposed into several sub-cubes, and each one can be divided in six tetrahedrons as it was shown in figure 9. In the same way that for 3L4W multilevel converters, 4L4W multilevel modulation problem can be reduced to a 3L4W two-level problem determining the coordinates origin for the sub-cube where the reference vector is pointing to. Once the sub-cube is found out, it can be used the 3L4W two-level modulation algorithm explained in chapter III to determine the four nearest state vectors and their corresponding duty cycles. 4L4W 3D SVPWM algorithm was presented in [9] taking into account that directly it optimizes the switching sequence minimizing the number of switching in four-leg systems. 3D SVPWM algorithm for 4L4W converters has been successfully tested using a 50KW three-level diode clamped converter. The considered conditions are a 47 Ω resistive load, a 1.4 mH smoothing inductance, a 5KHz switching frequency and a 60V dc-link voltage. The reference voltage has 80% third harmonic content. The experimental output phase to neutral voltages results shown in figure 15 have been obtained using a TMS320F2812 DSP microprocessor working in parallel with a Virtex XCV400BG432 FPGA.

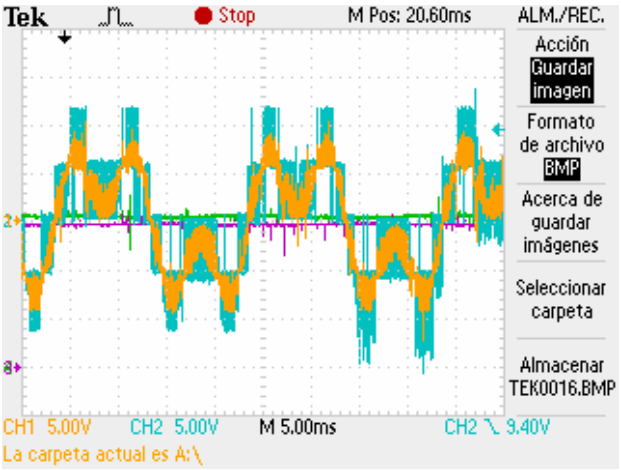

Figure 15. Experimental results of 3D-modulation algorithm for a three-level 3L4W diode clamped converter. Reference voltage with 80% third harmonic

VI. CONCLUSIONS

Several modulation techniques that are suitable for multilevel converters have been presented. It is a fact that SVPWM techniques are superior compared to PWM modulation because SVPWM has the possibility to carry out optimization methods like changing the state vector switching sequence in order to improve some converter characteristics as THD, phase load currents ripple, …, etc. SVPWM is based on the determination of the converter state vectors space, to find out the nearest state vectors to the reference vector and to generate the reference vector by a linear combination of them. State vectors spaces for different multilevel converter topologies have been presented. 2D SVPWM and 3D SVPWM algorithms have been presented. They are very useful to readily calculate the switching sequence and the on-state duration of the respective switching state vectors. They do not use trigonometric functions or look-up tables. The computational cost is drastically reduced compared with previous works. All modulation algorithms are based on geometrical considerations and they are extremely simple and efficient allowing an easy use of multilevel converters in multiple applications. These techniques can be used as SVPWM algorithms in all applications needing a 2D or 3D control vector such as 3L3W, 3L4W or 4L4W converters with applications as power converters and active filters. New 3D algorithms permit to extend two-level modulation strategies to N-level converters doing possible its implementation. The algorithms are independent of the multilevel converter topology and they can be applied to topologies as diode-clamped converters, flying capacitor converters and cascade converters. Besides, all the algorithms are independent of the number of levels of the converter. They have been satisfactorily implemented in very low-cost microcontrollers. The algorithms are extremely simple and they can be implemented in hardware systems as DSP and FPGA doing all the calculations very fast. Experimental results are presented for all the modulation strategies to demonstrate their good performance. In figure 16, 50KW three-level back-to-back diode clamped converter and 50KW three-level 4L4W diode clamped converter are shown.

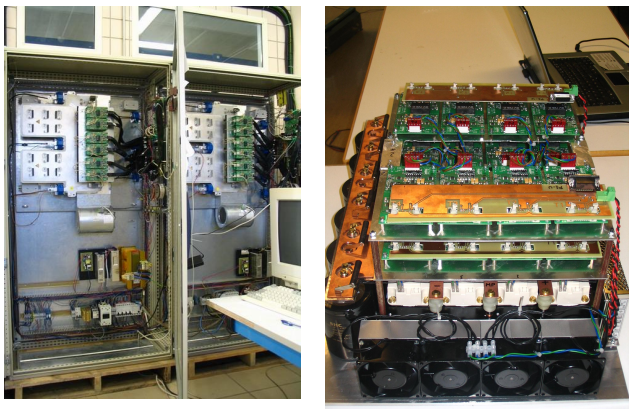

Figure 16. Pictures of 50KW three level back-to-back diode clamped converter and 50KW three level 4L4W diode clamped converter.

REFERENCES

[1] Celanovic, N.; Boroyevich, D.; "A fast space-vector modulation algorithm for multilevel three-phase converters" in *Industry Applications, IEEE Transactions on* Volume 37, Issue 2, March-April 2001 Page(s):637 – 641

[2] Pou, J.; Rodriguez, P.; Boroyevich, D.; Pindado, R.; Candela, I.; "Efficient Space-Vector Modulation Algorithm for Multilevel Converters with Low Switching Frequencies in the Devices" in Power Electronics Specialists, 2005 IEEE 36th Conference on June 12, 2005 Page(s):2521 – 2526

[3] Rodriguez, P.; Pou, J.; Luna, A.; Ghizoni, D.; Guo, J.; Francis, G.; Burgos, R.; Boroyevich, D.; "Three-dimensional SVM for modular power electronics systems" in Industrial Electronics Society, 2005. IECON 2005. 32nd Annual Conference of IEEE 6-10 Nov., 2005 Page(s):497 – 502

[4] J.-O.Krah ; J. Holtz; "High-performance current regulation for low inductance servo motors" The 1998 IEEE Thirty-Third IAS Annual Meeting Industry Applications. Volume 1, 12-15 Oct. 1998 Pages: 490 - 499 vol.1.

[5] Prats, M.M.; Carrasco, J.M.; Franquelo, L.G.; "Effective algorithm for multilevel converters with very low computational cost" in *Electronics Letters* Volume 38, Issue 22, 24 Oct 2002 Page(s):1398 – 1400

[6] New fast space-vector modulation for multilevel converters based on geometrical considerations Prats, M.M.; Portillo, R.; Carrasco, J.M.; Franquelo, L.G.; IECON 02 [Industrial Electronics Society, IEEE 2002 28th Annual Conference of the] Volume 4, 5-8 Nov. 2002 Page(s):3134 - 3139 vol.4

[7] Prats, M.M.; Franquelo, L.G.; Portillo, R.; Leon, J.I.; Galvan, E.; Carrasco, J.M.; "A 3-D space vector modulation generalized algorithm for multilevel converters" in *Power Electronics Letters, IEEE* Volume 1, Issue 4, Dec. 2003 Page(s):110 – 114

[8] Zhang, R.; Prasad, V.H.; Boroyevich, D.; Lee, F.C.; "Three-dimensional space vector modulation for four-leg voltage-source converters" in *Power Electronics, IEEE Transactions on* Volume 17, Issue 3, May 2002 Page(s):314 – 326

[9] Franquelo, L.G.; Prats, M.M.; Portillo, R.; Leon, J.I.; Perales, M.; Carrasco, J.M.; Galvan, E.; Mora, J.L.; "Simple and advanced three dimensional space vector modulation algorithm for four-leg multilevel converters topology" in Industrial Electronics Society, 2004. IECON 2004. 30th Annual Conference of IEEE Volume 3, 2-6 Nov. 2004 Page(s):2285 - 2289 Vol. 3