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Integrated Control of Five-Level Diode-Clamped Rectifiers

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Abstract

This paper presents an approach for dealing with the control of five-level, diode-clamped rectifiers. The control of such converters is challenging since the voltage balancing among capacitors is not a trivial task. Some of the existing approaches that cope with this problem use specific modifications of one of the traditional modulation techniques such as using redundant vectors in SVM. The main feature of the proposed technique is that part of the modulation is considered in the system equations and, in this way, the voltage balance can be solved designing a specific controller for this problem. As a result, several levels are used within a switching period. Furthermore, it is shown that the proposed approach hardly affects the control of active and reactive powers and total dc-link voltage in such a way that the well-known direct power control (DPC) can be applied. As a consequence, the resultant modulation stage is simpler than other techniques based on, e.g., space vector modulation (SVM). The effectiveness and good performance of the system under the proposed control approach are validated by both simulation and experimental results.

Index Terms

Power conversion, multilevel converter, grid interface, diode-clamped converter (DCC), voltage balancing, Power Control

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I. Introduction

Over the last decades, multilevel converters have emerged as a preferable solution for high-power applications and/or systems where low current distortion are required [1], [2]. Not only they offer the possibility of using lower-voltage switching devices in common applications, but also they improve the current distortion at the converter output. Nowadays, they have become a mature technology and they are used in several industrial applications such as energy conversion and generation, manufacturing or power transmission, among others [3], [4]. Despite there are some industrial well-established topologies, there is still plenty room for research as new topologies and algorithms are still being developed given the potentiality of this technology [4]–[6].

Among the different multilevel converter topologies, this paper focuses on the diode-clamped converter (DCC). Diode-clamped converter topology allows to set different voltage levels at the output of the converter thanks to the use of diodes that permit the current circulation from the grid to the selected level and vice versa. Despite they have been commercialized by a wide amount of companies, the exponential usage complexity when the number of levels is greater than three, limits its industrial implementation to three-level DCC [6].

The presence of several capacitors in the dc link leads to the control challenge for this kind of converters, that is, guaranteeing a proper voltage sharing among all of them. The aim of this paper is to present an implementable and easy-to-follow solution to this control objective in five-level DCCs with no additional cost. Several approaches have already been presented for the capacitor voltage balancing issue for five-level DCCs and can be primarily divided into several categories [7]: 1) using redundant switching vectors along with modulation strategies and control schemes or injecting zero-sequence voltages in the modulation signals of carrier-based modulators; 2) using additional circuitry; 3) applying algorithms for back-to-back converters; 4) defining a discrete-time dynamic model and applying a predictive control strategies; and 5) analyzing the capacitor voltage imbalance issue as a problem of regulating the multiple outputs of a nonlinear system subject to exogenous disturbances [8], [9]. The second approach requires additional hardware [10]–[12], which increases the converter cost and volume and, still it does not guarantee that control complexity is reduced, or even kept the same. The third approach is limited to specific applications where a back-to-back application is considered [13], [14] and, therefore, it is of no use when a standalone application is considered.

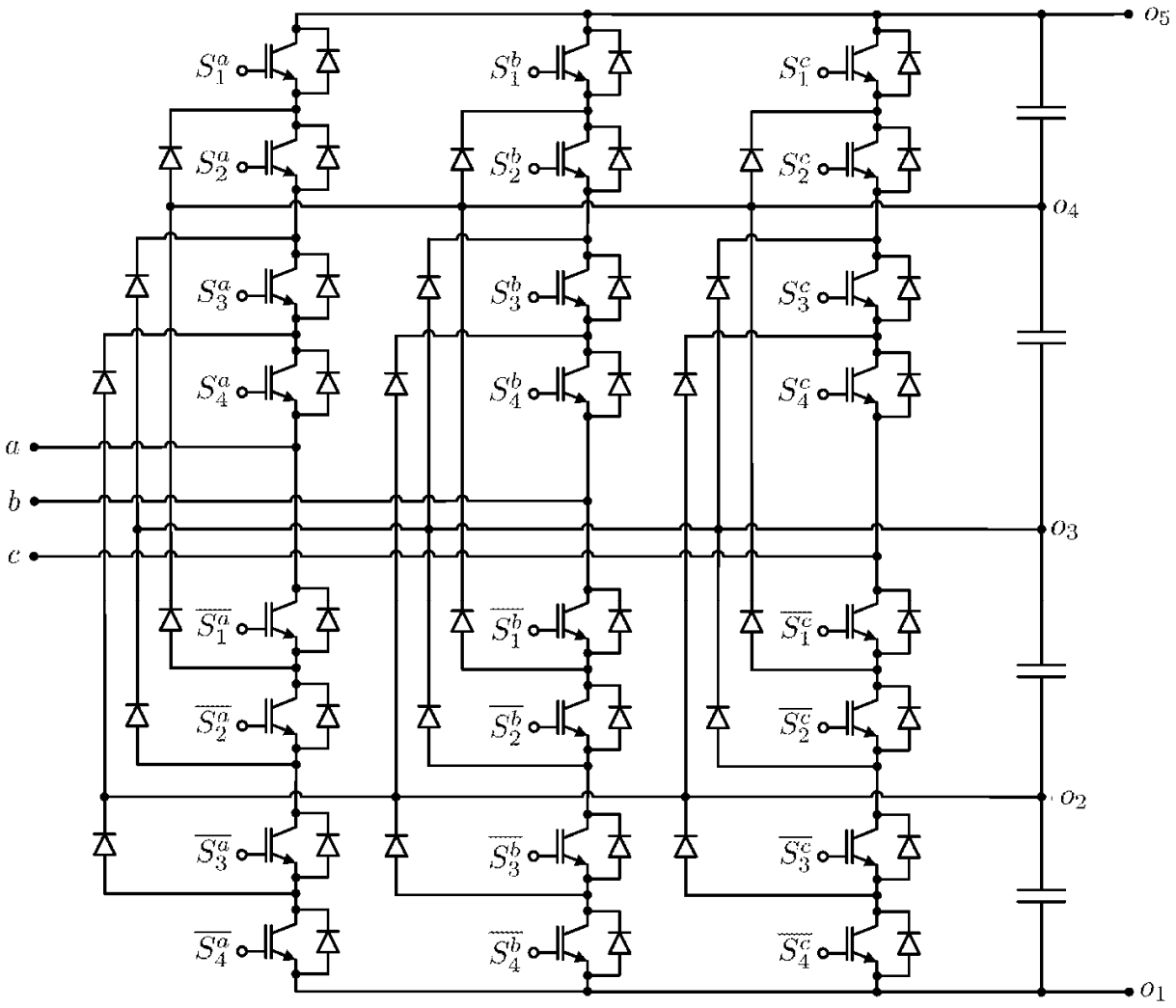

Fig. 1. Circuit of a three-phase five-level diode-clamped power converter.

A vast amount of practical solutions that exist are, in fact, related to the first category mentioned previously [15]–[21]. The considered solution consists of using the degree of freedom associated with the different switching combinations that achieve the same phase-to-phase converter voltage output, that is, circulating the phase current through different capacitors to regulate their own voltage without affecting the current performance. In [20], the SVM hexagon is separated in two regions according to the modulation index and a criteria for switching vector selection is provided. In [19] a criteria for selecting the redundant switching vector according to the most deviated capacitor is considered. However, this approach has some restrictions [22], [23] as redundant switching states may not appear when large modulation indexes are involved. The

solution stated in [18] goes through considering all the degrees of freedom the converter has, that is, using several voltage levels within a switching period. Regarding the fourth approach, in [24] a low-computational-cost predictive control technique is analyzed and evaluated in simulations. Moreover, in [25] the problem is formulated as a linear, mixed-integer programming problem that it is solved off-line and implemented interpolating in a lookup table.

As stated previously, this paper is focused on the five-level DCC topology (Fig. 1) and its aim is to deal with the voltage capacitor imbalance issue in an analytical way during the controller design instead of attacking the problem during the modulation stage. Consequently, the amount of levels used within a switching period is increased, similarly to [18], in comparison with two-nearest-level modulation approaches. On the whole, the advantages this approach offers are: 1) no external hardware required; 2) simple-to-use mathematical model; 3) different controllers can be implemented; and 4) computational burden lower than other approaches such as SVM or predictive techniques. Besides, the idea of using several levels within a switching period offers more degrees of freedom than the methods that use redundant switching vectors. Moreover, the technique could be extended to DCC converters with more than five levels by applying the corresponding set of control inputs. Obviously, the number of control inputs will increase as the level does although the simplicity of the implemented controller, as it will be shown, partially overcomes this issue. This work is an extension to [26] where the different control objectives are addressed separately using different set of control inputs. In [27] the same technique was successfully applied to a NPC rectifier. However, the previous work considered the five-level DCC converter as a grid interfacing inverter and only simulation results were presented. In this work, the necessary rearrange of the variables in order to work as a rectifier is considered, experimental results are included and the original current control has been replaced with a model-based direct power controller (DPC) [28] in order to show the flexibility of the proposed technique. Furthermore, a last modification in the algorithm is included which results in the reduction of the number of levels used per switching period.

The outline of the paper is as follows. Firstly, a brief explanation of the converter under study is given in Section II, along with the averaged dynamic model based on the duty ratios of each level at each phase. After this, Section III presents the decoupled model-based power and capacitor voltage balance controllers. Then, the algorithm modification is presented in Section IV. Afterwards, some simulation and experimental results with these controllers are shown and discussed in Section V. Finally, some conclusions are presented in Section VI.

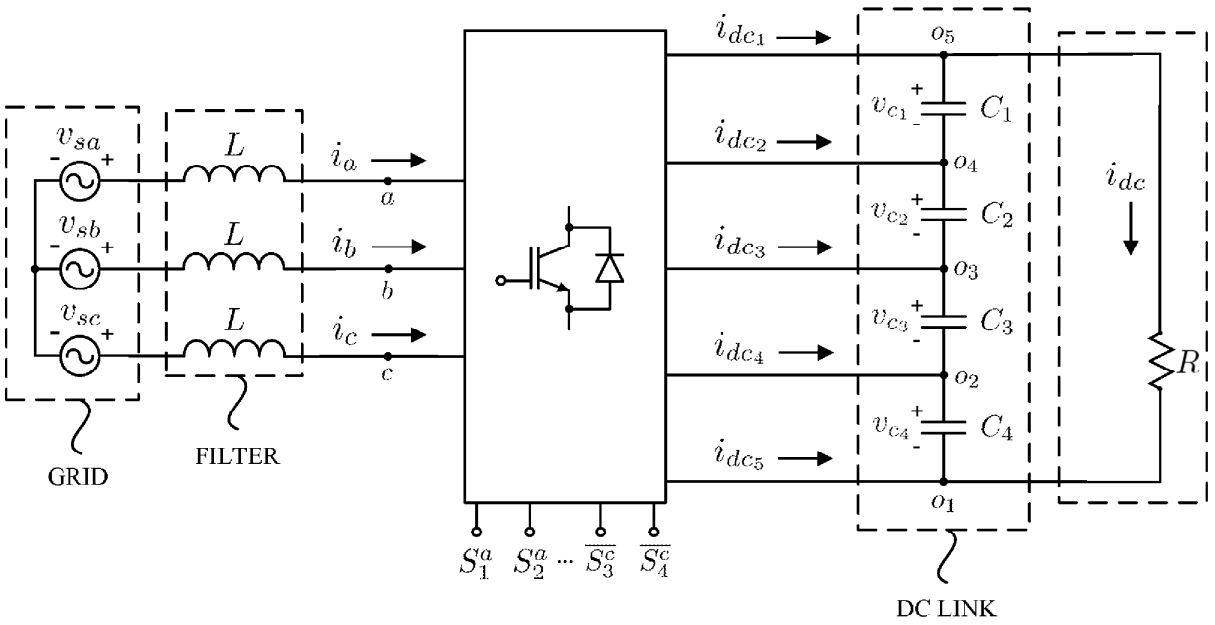

Fig. 2. Schematic diagram of the five-level diode-clamped converter operating as a rectifier connected to the utility grid.

II. Model Equations

A. System Description

The circuit configuration considered in this paper is depicted in Fig. 2 which illustrates a simple schematic diagram of the five-level DCC operating as a rectifier connected to the grid. The total dc-link voltage V_{dc} has to be controlled and the power is dissipated in a dc-link-connected resistor. The converter dc-link is composed of capacitors C_1, C_2, C_3 and C_4, all of identical capacitance C. Their respective voltages are represented by v_{c_1}, v_{c_2}, v_{c_3} and v_{c_4} attending to the criteria depicted in Fig. 2. Regarding the converter ac side, the phase voltages are denoted by v_{sa}, v_{sb} and v_{sc} and the phase currents are named i_a, i_b and i_c according to the sign criteria and phase depicted in Fig. 2. The filter inductors are considered to be equal and ideal, i.e., they all present the same inductance L.

The converter voltage output in phases a, b and c, measured with respect to the dc-link midpoint o_3, are denoted by v_a, v_b and v_c , respectively, and they represent the voltage set by the converter. These voltages depend on the converter switching states, which are determined by the switching functions $f_{i_j} \in \{0, 1\}$ –where $i = a, b, c$; $j = 1, 2, \ldots, 5$– defined in Table I.

Note that S_h^i for $i = a, b, c$ and $h = 1, 2, 3, 4$ represent the semiconductor devices depicted in

TABLE I

SWITCHING FUNCTION f_{ij} DEFINITION

f_{ij}	S_1^i	S_2^i	S_3^i	S_4^i	v_i
$f_{i_1}=1$	0	0	0	0	$-v_{c_3}-v_{c_4}$
$f_{i_2}=1$	0	0	0	1	$-v_{c_3}$
$f_{i_3}=1$	0	0	1	1	0
$f_{i_4}=1$	0	1	1	1	v_{c_2}
$f_{i_5}=1$	1	1	1	1	$v_{c_1}+v_{c_2}$

Fig. 1. Thereby, each switching function f_{ij} represents whether the terminal i of the converter is connected to the dc-link point o_j ($f_{ij}=1$) or not ($f_{ij}=0$). In this manner, it is obvious that the expression $f_{i_1}+f_{i_2}+f_{i_3}+f_{i_4}+f_{i_5}\leq 1$ for $i=a$, b, c, has to be satisfied. In other words, each ac-side points a, b and c can be connected to only one of the points o_1, o_2, o_3, o_4 or o_5 of the dc-link. It is assumed that there is always a switching state activated, i.e. the case of all switches turned-off is not considered. Then $f_{i_1}+f_{i_2}+f_{i_3}+f_{i_4}+f_{i_5}=1$.

B. Averaged Model

As stated in [26], an averaged model in $\alpha\beta\gamma$ frame within a switching period can be considered when facing power control. Therefore, the switching functions f_{ij} can be averaged and then transformed into the $\alpha\beta\gamma$ frame resulting in the variables d_{k_j} for $k=\alpha,\beta,\gamma$. These variables represent the fraction of a switching period when the transformed phase k is connected to the point o_j. It is also possible to transform them reversely from $\alpha\beta\gamma$ to abc, in which case they will be referred as duty ratios of phase i and level j. From [26], assuming that the capacitor voltages are similar ($v_{c_1}\simeq v_{c_2}\simeq v_{c_3}\simeq v_{c_4}$), taking into account the definition of the switching functions, the Kirchhoff's laws and considering the duty ratios explained previously, the averaged model

is obtained as

$$L\frac{di_\alpha}{dt} = v_{s\alpha} - (2d_{\alpha_5} + d_{\alpha_4} - d_{\alpha_2} - 2d_{\alpha_1})\frac{V_{dc}}{4} \tag{1}$$

$$L\frac{di_\beta}{dt} = v_{s\beta} - (2d_{\beta_5} + d_{\beta_4} - d_{\beta_2} - 2d_{\beta_1})\frac{V_{dc}}{4} \tag{2}$$

$$C\frac{dv_{c1}}{dt} = d_{\alpha_5}i_\alpha + d_{\beta_5}i_\beta - i_{dc} \tag{3}$$

$$C\frac{dv_{c2}}{dt} = (d_{\alpha_5} + d_{\alpha_4})i_\alpha + (d_{\beta_5} + d_{\beta_4})i_\beta - i_{dc} \tag{4}$$

$$C\frac{dv_{c3}}{dt} = -(d_{\alpha_1} + d_{\alpha_2})i_\alpha - (d_{\beta_1} + d_{\beta_2})i_\beta - i_{dc} \tag{5}$$

$$C\frac{dv_{c4}}{dt} = -d_{\alpha_1}i_\alpha - d_{\beta_1}i_\beta - i_{dc}, \tag{6}$$

where $v_{s\alpha}, v_{s\beta}$ and i_α, i_β are the grid voltages v_{sa}, v_{sb}, v_{sc} and the grid currents i_a, i_b, i_c transformed to $\alpha\beta\gamma$. Note that the power-invariant version of the Clarke transformation is being used. It can be seen that $d_{\gamma_1}, d_{\gamma_2}, d_{\gamma_3}, d_{\gamma_4}$ and d_{γ_5} do not appear in the dynamical model and, as a consequence, they do not have a direct effect on it but they still remain as control inputs.

In order to express the capacitor voltage unbalances, three error signals are defined by

$$v_{d_1} = v_{c_4} - v_{c_1} \tag{7}$$

$$v_{d_2} = v_{c_3} - v_{c_2} \tag{8}$$

$$v_{d_3} = v_{c_2} - v_{c_1}. \tag{9}$$

Substituting (3)-(6) into the definition of v_{d_1}, v_{d_2} and v_{d_3}, the error signal dynamics become

$$C\frac{dv_{d_1}}{dt} = -(d_{\alpha_5} + d_{\alpha_1})\, i_\alpha - (d_{\beta_5} + d_{\beta_1})\, i_\beta \tag{10}$$

$$C\frac{dv_{d_2}}{dt} = -(d_{\alpha_1} + d_{\alpha_2} + d_{\alpha_4} + d_{\alpha_5})i_\alpha - (d_{\beta_1} + d_{\beta_2} + d_{\beta_4} + d_{\beta_5})i_\beta \tag{11}$$

$$C\frac{dv_{d_3}}{dt} = d_{\alpha_4}i_\alpha + d_{\beta_4}i_\beta. \tag{12}$$

On the other hand, considering the provided definition of duty ratios, the following equation has to be fulfilled

$$d_{i_1} + d_{i_2} + d_{i_3} + d_{i_4} + d_{i_5} = 1, \text{ for } i = \{a, b, c\}. \tag{13}$$

By considering this constraint, the duty ratios corresponding to level 3 – d_{i_3} – are defined as a function of the remaining ones.

III. CONTROLLER DESIGN

This section is devoted to present several control stages that, in the whole, achieve the proper performance of the converter, namely: power control, total dc-link regulation and capacitor voltage balancing. First of all, a change of variables inspired by (1)–(2) and (10)–(12) is applied in order to considerably simplify the averaged model

$$T_{\alpha\beta\to u} = \begin{pmatrix} 2 & 1 & -1 & -2 \\ 1 & 0 & 0 & 1 \\ 1 & 1 & 1 & 1 \\ 0 & -1 & 0 & 0 \end{pmatrix}$$

$$\begin{pmatrix} u_1 \\ u_3 \\ u_5 \\ u_7 \end{pmatrix} = T_{\alpha\beta\to u} \begin{pmatrix} d_{\alpha_5} \\ d_{\alpha_4} \\ d_{\alpha_2} \\ d_{\alpha_1} \end{pmatrix}; \begin{pmatrix} u_2 \\ u_4 \\ u_6 \\ u_8 \end{pmatrix} = T_{\alpha\beta\to u} \begin{pmatrix} d_{\beta_5} \\ d_{\beta_4} \\ d_{\beta_2} \\ d_{\beta_1} \end{pmatrix}. \tag{14}$$

These new control variables, u_l for $l = 1, 2, \ldots, 8$, are expressed in terms of the duties shown in (1)-(12). By doing so, the behavior of the system can be easily controlled by means of a set of equations that define the value of variables u_l for $l = 1, 2, \ldots, 8$. In summary, the value of these variables will be defined by the appropriate control laws and the variable change (14) can be reverted to obtain the value of the duties.

A. Power Controllers

According to [29], the instantaneous powers of the three-phase circuit can be obtained in the $\alpha\beta$ frame by applying

$$p = v_{s\alpha} i_\alpha + v_{s\beta} i_\beta \tag{15}$$

$$q = -v_{s\alpha} i_\beta + v_{s\beta} i_\alpha, \tag{16}$$

where variables p and q represent the instantaneous active and reactive powers, respectively. In this case, the controller should be designed in such a way that the instantaneous powers are regulated to achieve the desired amount of active power p_{ref}, set by the total dc-link voltage control, and the specified amount of reactive power q_{ref}, commonly equal to 0 to achieve unity power factor.

Therefore, considering the change of variables (14), the current dynamics (1)–(2) are expressed now by

$$L\,\frac{di_\alpha}{dt} = v_{s\alpha} - \frac{1}{4}u_1 V_{dc} \tag{17}$$

$$L\,\frac{di_\beta}{dt} = v_{s\beta} - \frac{1}{4}u_2 V_{dc}. \tag{18}$$

Applying these equations into the definition of instantaneous powers (15)-(16), the power dynamics are obtained as

$$L\,\frac{dp}{dt} = v_{s\alpha}^2 + v_{s\beta}^2 + 2\pi f L q - (u_1 v_{s\alpha} + u_2 v_{s\beta})\frac{V_{dc}}{4} \tag{19}$$

$$L\,\frac{dq}{dt} = -2\pi f L p + (u_1 v_{s\beta} - u_2 v_{s\alpha})\frac{V_{dc}}{4}. \tag{20}$$

These derived power dynamics are similar to those of the two-level converter and, therefore, any of the numerous control strategies widely studied over the last years [30]– [31] can be implemented. In this paper, the solution considered is adopted from [28], where a model-based DPC control is presented, yielding

$$\begin{aligned} u_1 = {} & u_1^z + k_p v_{s\alpha}\,(p - p_{ref}) + k_{pi} v_{s\alpha} \int_0^t (p - p_{ref})\,d\tau \\ & - k_q v_{s\beta}\,(q - q_{ref}) - k_{qi} v_{s\beta} \int_0^t (q - q_{ref})\,d\tau \end{aligned} \tag{21}$$

$$\begin{aligned} u_2 = {} & u_2^z + k_p v_{s\beta}\,(p - p_{ref}) + k_{pi} v_{s\beta} \int_0^t (p - p_{ref})\,d\tau \\ & + k_q v_{s\alpha}\,(q - q_{ref}) + k_{qi} v_{s\alpha} \int_0^t (q - q_{ref})\,d\tau\ , \end{aligned} \tag{22}$$

where

$$u_1^z = \frac{4}{v_{dc}}\left(\left(1 + \frac{2\pi f L q}{v_{s\alpha}^2 + v_{s\beta}^2}\right) v_{s\alpha} + \frac{2\pi f L p}{v_{s\alpha}^2 + v_{s\beta}^2}\, v_{s\beta}\right) \tag{23}$$

$$u_2^z = \frac{4}{v_{dc}}\left(\left(1 + \frac{2\pi f L q}{v_{s\alpha}^2 + v_{s\beta}^2}\right) v_{s\beta} - \frac{2\pi f L p}{v_{s\alpha}^2 + v_{s\beta}^2}\, v_{s\alpha}\right), \tag{24}$$

and the design parameters k_p, k_q, k_{pi} and k_{qi} are the proportional and integral controller gains. These equations can be represented by the block diagram depicted in Fig. 3.

B. Total DC-Link Voltage Controller

In order to keep the dc-link voltage at the desired value, a PI controller is used [28], [32]

$$p_{ref} = k_p^{v_{dc}}(v_{dc_{ref}}^2 - v_{dc}^2) + k_i^{v_{dc}} \int_0^t (v_{dc_{ref}}^2 - v_{dc}^2)d\tau, \tag{25}$$

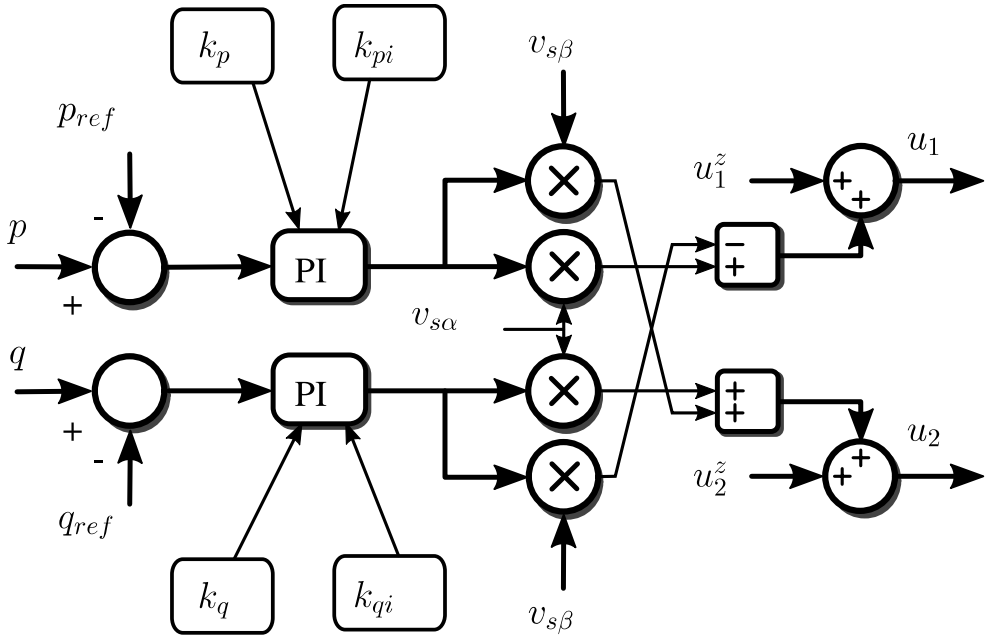

Fig. 3. Schematic diagram of the power controller

where constants $k_p^{v_{dc}}$ and $k_i^{v_{dc}}$ are the controller tuning parameters. The value $v_{dc_{ref}}$ is set by the user, usually, as a constant. The output of this controller p_{ref} is the input for the active power controller.

C. Capacitor Voltage Balance Controller

Regarding the balancing of the dc-link capacitor voltages, a model-based controller is proposed in [26]. It is based on the particular equations of the dynamics of the error signals, which can be expressed by substituting (14) into (10)-(12) yielding

$$C\,\frac{dv_{d_1}}{dt} = -\,u_3 i_\alpha - u_4 i_\beta \tag{26}$$

$$C\,\frac{dv_{d_2}}{dt} = -\,u_5 i_\alpha - u_6 i_\beta \tag{27}$$

$$C\,\frac{dv_{d_3}}{dt} = -\,u_7 i_\alpha - u_8 i_\beta. \tag{28}$$

Notice the advantage of the proposed change of variables (14). A complete decoupling of the control variables can be achieved for the different control objectives. On one hand, u_1 and u_2 are used to regulate the power variables p and q as mentioned previously, on the other hand, control variables u_3, u_4, u_5, u_6, u_7 and u_8 remain as degrees of freedom that can be used to balance

the voltage capacitors. To regulate the error signals v_{d_1}, v_{d_2} and v_{d_3} these control variables are defined as

$$\begin{pmatrix} u_3 \\ u_4 \\ u_5 \\ u_6 \\ u_7 \\ u_8 \end{pmatrix} = \begin{pmatrix} i_\alpha & 0 & 0 \\ i_\beta & 0 & 0 \\ 0 & i_\alpha & 0 \\ 0 & i_\beta & 0 \\ 0 & 0 & i_\alpha \\ 0 & 0 & i_\beta \end{pmatrix} \begin{pmatrix} k_1\, v_{d1} \\ k_2\, v_{d2} \\ k_3\, v_{d3} \end{pmatrix}, \tag{29}$$

where k_1, k_2 and k_3 are positive constant design parameters.

Introducing these control laws into the error signal dynamics, the closed-loop dynamics are described by

$$C\,\frac{dv_{d_1}}{dt} = -\,k_1 i_\alpha^2 v_{d_1} - k_1 i_\beta^2 v_{d_1} \tag{30}$$

$$C\,\frac{dv_{d_2}}{dt} = -\,k_2 i_\alpha^2 v_{d_2} - k_2 i_\beta^2 v_{d_2} \tag{31}$$

$$C\,\frac{dv_{d_3}}{dt} = -\,k_3 i_\alpha^2 v_{d_3} - k_3 i_\beta^2 v_{d_3}. \tag{32}$$

Knowing that $i_\alpha^2 + i_\beta^2 > 0$, it can be easily seen that variables v_{d_i} tend to zero for the controlled system (30)–(32), assuring its stability [26].

D. Duty Ratios Computation

By using (29) and the DPC controller (21)–(22), u_1, u_2, …, u_8 are determined. Now it is necessary to revert the change of variables (14) to obtain the duty ratios values, which result in

$$T^{-1}_{\alpha\beta\to u} = T_{u\to\alpha\beta} = \begin{pmatrix} \frac{1}{4} & \frac{1}{4} & \frac{1}{4} & \frac{2}{4} \\ 0 & 0 & 0 & -1 \\ 0 & -1 & 1 & 1 \\ -\frac{1}{4} & \frac{3}{4} & -\frac{1}{4} & -\frac{2}{4} \end{pmatrix}$$

$$\begin{pmatrix} d_{\alpha_5} \\ d_{\alpha_4} \\ d_{\alpha_2} \\ d_{\alpha_1} \end{pmatrix} = T_{u\to\alpha\beta} \begin{pmatrix} u_1 \\ u_3 \\ u_5 \\ u_7 \end{pmatrix}; \begin{pmatrix} d_{\beta_5} \\ d_{\beta_4} \\ d_{\beta_2} \\ d_{\beta_1} \end{pmatrix} = T_{u\to\alpha\beta} \begin{pmatrix} u_2 \\ u_4 \\ u_6 \\ u_8 \end{pmatrix}. \tag{33}$$

As a result, eight duty ratios in $\alpha\beta$ frame are obtained. Thus, transforming these variables into abc frame is elemental by using the inverse Clarke transformation. Notice that the values of d_{γ_1}, d_{γ_2}, d_{γ_4} and d_{γ_5} have not been taken into account until now. In [26] some guidelines are given in order to avoid saturations by making d_{γ_j} equal to a constant value denoted k_{γ_j} for

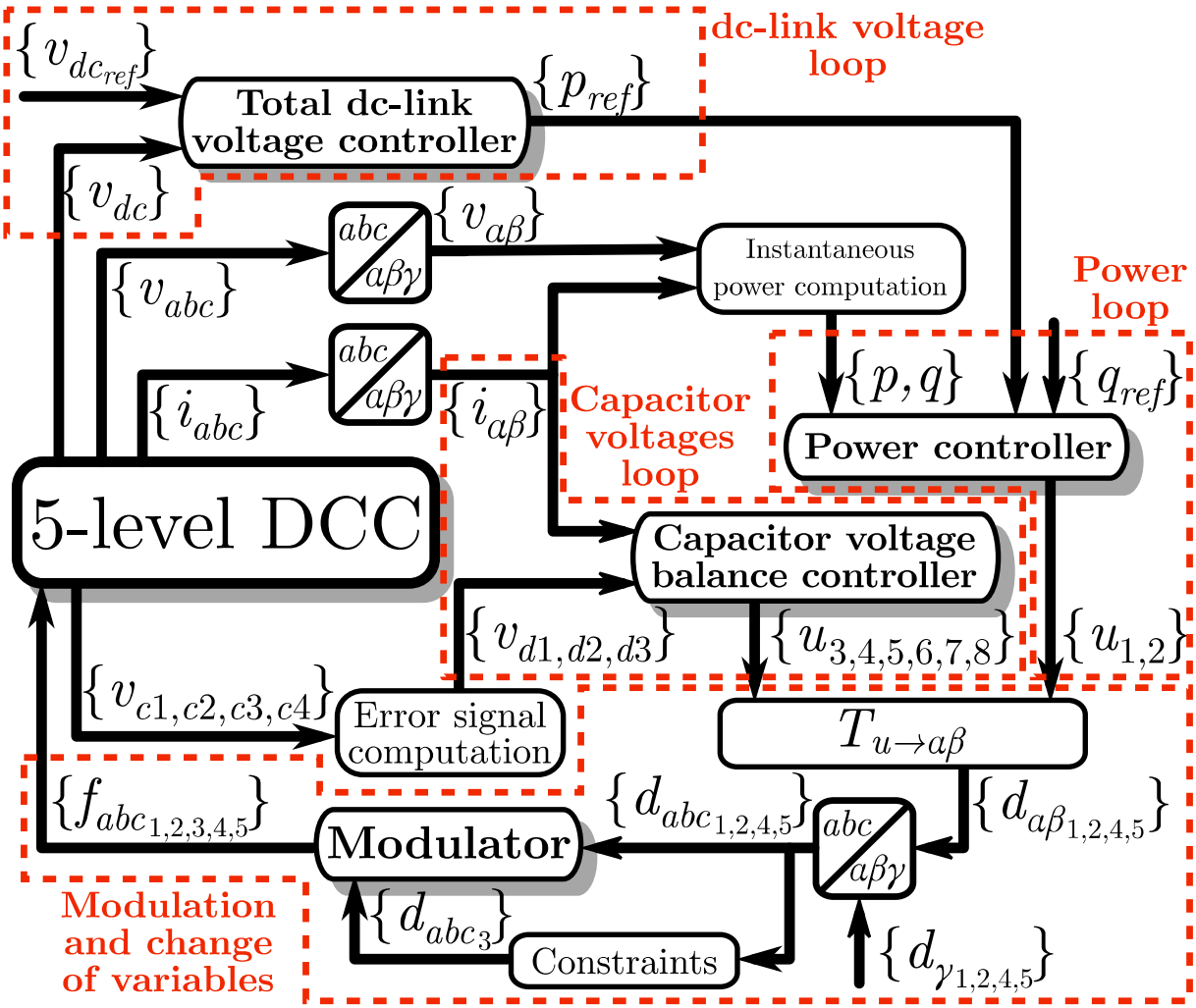

Fig. 4. Schematic block diagram of the whole control system.

$j = \{1, 2, 4, 5\}$. In the next section, reduction in the number of commutations is also considered by selecting a proper value of d_{γ_j}.

Finally, the use of (13) will yield the three remaining duty ratios d_{a_3}, d_{b_3} and d_{c_3}. After this, the modulation stage takes place to set the switching functions f_{i_j}, for $i = a$, b, c and $j = 1, \ldots, 5$ at every sampling time. A schematic block diagram that represents the implemented controls is depicted in Fig. 4.

IV. Algorithm Improvement

The values of $d_{\gamma_1}, d_{\gamma_2}, d_{\gamma_4}$ and d_{γ_5} have a direct impact on the duties value: a higher value of d_{γ_j} would lead to greater values of d_{a_j}, d_{b_j} and d_{c_j}. This fact highlights the importance of

selecting a proper value of d_{γ_j} in such a way that duty saturation is avoided, i.e., d_{i_j} remains in the interval $[0, 1]$. As stated before, [26] gives some guidelines for proper delimiting of d_{γ_j} values to avoid saturation in steady state performance. Nevertheless, some degrees of freedom remain that could be used to achieve another control objectives. In this section, an algorithm is proposed for the choice of d_{γ_j} in order to also reduce the number of commutations and, thus, the switching losses.

For this, at every sampling instant, the inverse power-invariant Clarke transformation has to be analyzed at every level j, in search for a value of d_{γ_j} that makes one of the duties d_{i_j} $(i = a, b, c)$ equal to zero and, at the same time, fulfills the saturation constrains. By doing so, the phase whose duty has been made zero is not set at the corresponding level during the sampling interval, avoiding extra-commutations.

Using the inverse Clarke transformation, the three values of d_{γ_j} for which one $d_{i_j} = 0$ can be computed as

$$d_{a_j} = 0 \rightarrow d^a_{\gamma_j} = -\sqrt{2} d_{\alpha_j} \tag{34}$$

$$d_{b_j} = 0 \rightarrow d^b_{\gamma_j} = \frac{d_{\alpha_j}}{\sqrt{2}} - d_{\beta_j}\sqrt{\frac{3}{2}} \tag{35}$$

$$d_{c_j} = 0 \rightarrow d^c_{\gamma_j} = \frac{d_{\alpha_j}}{\sqrt{2}} + d_{\beta_j}\sqrt{\frac{3}{2}}. \tag{36}$$

Given that in the Clarke transformation the relationship between the d_{i_j} and d_{γ_j} is monotonically increasing, the greatest value among (34)-(36) for each $j = 1, 2, 4, 5$ has to be chosen in order to avoid the values less than zero. The upper constraint $d_{i_j} \leq 1$ has to be checked and, in the case is not fulfilled, the commutation reduction is not possible and duty saturation is unavoidable and it will be for any other procedure for selection of d_{γ_j}. Considering this, Fig. 5 shows the planes that are defined by (34)–(36) for a level j. The selection can be interpreted as the largest vertical value for the three points associated with the given values $d_{\alpha_j}, d_{\beta_j}$. As a result, one value of d_{i_j} for $i = a, b, c$ will be zero. This choice has to be performed four times for $j = 1, 2, 4, 5$ in such a way that four duty ratios are equal to zero.

However, the cases $j = 2$ and $j = 4$ deserve special attention. Making d_{j_2} or d_{j_4} equal to zero could force the converter to switch between levels that are not consecutive, e.g. the case $d_{a_5} \neq 0, d_{a_4} = 0, d_{a_3} \neq 0$. This behavior is not desirable since it would compromise the voltage limits of the switching devices. To avoid this, the selection of one $d^i_{\gamma_j}$ for $j = 2, 4$ is only considered if the duty cycle for phase i and the extreme level next to j has been equal to zero

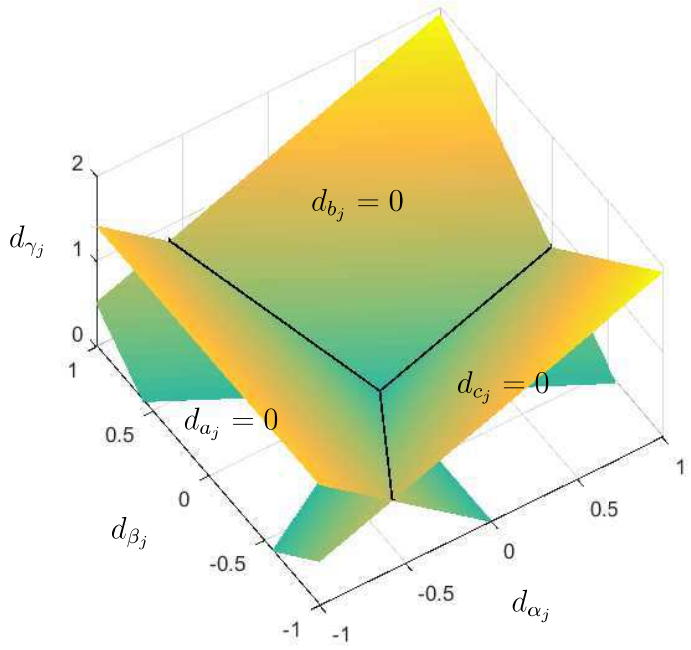

Fig. 5. The three planes that makes one duty $d_{i_j} = 0$ for $i = a, b, c$ in the $\alpha\beta\gamma$ frame. These planes are defined by equations (34), (35) and (36)

as a result of the previous computations. This algorithm is depicted in Fig. 6 for levels $j = 4, 5$ and it can be easily extrapolated to levels $j = 1, 2$.

As a result, at each sampling time, there are only two phases that commute at level 1 and 5, and it is also possible that the same phase does not commute at the consecutive level 2 or 4, depending on the value of $d_{\alpha_2}, d_{\beta_2}$ or $d_{\alpha_4}, d_{\beta_4}$, respectively.

V. Simulation and Experimental Results

In this section some experimental results are presented to verify the validity of the algorithm. The system used for this purpose is shown in Fig. 7, whose output power is rated up to 15 KVA. The values of converter and controller parameters are summarized in Table II. From the control signals, d_{i_j} for $i = a$, b, c and $j = 1, 2, \ldots, 5$, the switching sequence is generated by emulating the modulation of a typical CB-PWM where a triangular carrier wave is used. In order to show the system behaviour under different conditions, the resistive load (R) and the voltage reference in the dc-link are modified during the simulation. The load is abruptly modified from $120\ \Omega$ to

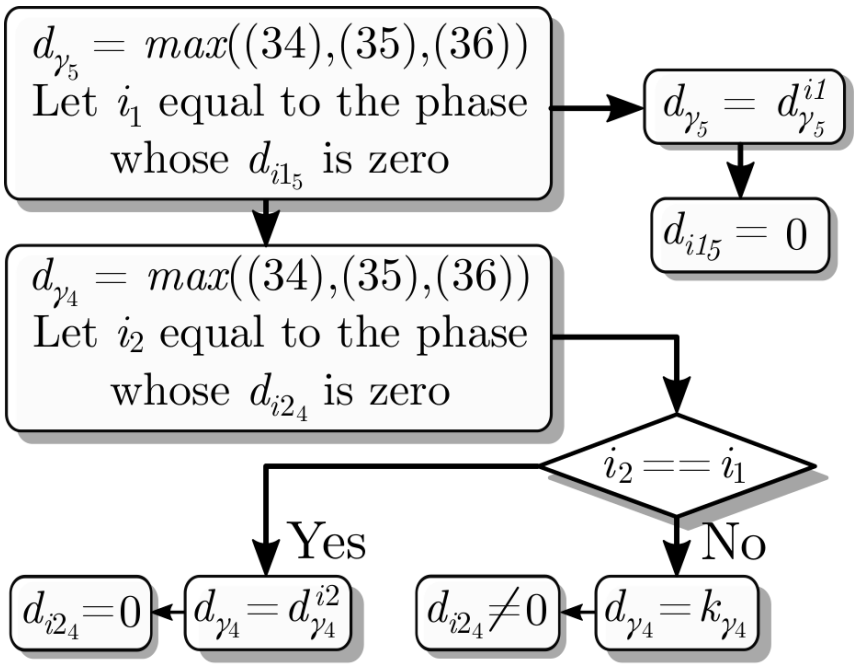

Fig. 6. Schematic diagram of the algorithm modification implementation for levels $j = 4$ and $j = 5$

TABLE II

SIMULATION AND EXPERIMENTAL PARAMETERS

Parameter	Value	Parameter	Value
f_{sw}	10 kHz	k_p	$3 \cdot 10^{-7}$
f_{grid}	50 Hz	k_i	$5 \cdot 10^{-5}$
v_{sa}, v_{sb}, v_{sc}	230 V_{RMS}	$k_p^{v_{dc}}$	0.05
L	2 mH	$k_i^{v_{dc}}$	1
C	3300 μF	k_1, k_2, k_3	$5 \cdot 10^{-5}$
$v_{dc_{ref}}$	700 $\rightarrow$ 800 V	k_{γ_1}, k_{γ_5}	0.7
R	120 $\rightarrow$ 60 Ω	k_{γ_2}, k_{γ_4}	0.1
q_{ref}	0 VAr		

60 Ω at time $t = 0.7$ s whereas the voltage reference is modified as a ramp from 700 V_{dc} to 800 V_{dc} starting at $t = 2.6$ s with a slope of 150 V/s. Afterwards, the load is brought back to 120 Ω at $t = 4.7$ s.

The control variables u_l defined by the DPC Controller and (29) are computed at the beginning

of each sampling period, and then the transformation procedure illustrated in Fig. 4 is applied. For the original algorithm, variables d_{γ_1}, d_{γ_2}, d_{γ_4} and d_{γ_5} are assumed to be constant and equal to parameters $k_{\gamma_1}, \ldots, k_{\gamma_5}$ shown in table II. Regarding the algorithm modification, these variable are computed according to Fig. 6.

The software is programmed in a Speedgoat real-time target machine using Matlab Simulink. Figure 7 shows the real-time software machine along with several stages of the converter. The semiconductor devices are mounted in different trays for each phase together with the dc-link capacitors and the IGBT gate drivers (at each side of the tray – not shown in Fig. 7). The relays shown in this figure are used for the capacitor precharge and grid-connection maneuvers. The current distortion is measured with a power quality analyzer Fluke-435 and the grid currents are sensed with current probes.

In the following, the results of the experiments are presented. In some of the figures, simulation results are also included to corroborate the validity of the model. Figure 8 shows the behavior of total dc-link voltage with the changes described previously. Figure 9 depicts the behaviour of the phase currents in steady state with $R = 60\,\Omega$ and $v_{dc} = 800\,V$. Figure 10 shows the instantaneous power of the system for both the original algorithm and the modified one along with the simulation results for the same procedure. Experimental results present a higher ripple than simulated ones due to the presence of non-idealities in real equipments, such as calibration of sensors, presence of noise and sample delays among others. Still, both cases perform an acceptable reference-tracking and the experimental behaviour is similar to the simulated one.

On the other hand, Fig. 11 shows the evolution of the error signals in simulations and experiments when starting from a unbalanced situation for both the original algorithm and the modified one. Several tests have been performed depicting them when parameters k_1, k_2 and k_3 are set with different values. Generally, the higher the parameter value the less time it takes to correct the unbalance. However, a high value of these parameters could lead to instability in the transitory events due to saturation of the duty ratios. Therefore, the selection of these value has to be regarded as a trade-off between unbalance correction speed and robustness. These tests are carried out with $R = 120\,\Omega$ and $v_{dc} = 700\,V$. In some cases, specially for small values of k_1, k_2 and k_3 there are some noticeable differences between simulations and experiments that could be explained by the presence of dead-times and turn-on/turn-off semiconductor delays. A low value of the balancing control parameters – k_1, k_2, k_3 – could result in a low value of the control signals that would yield a low value of a duty ratio. If this duty ratio value is small

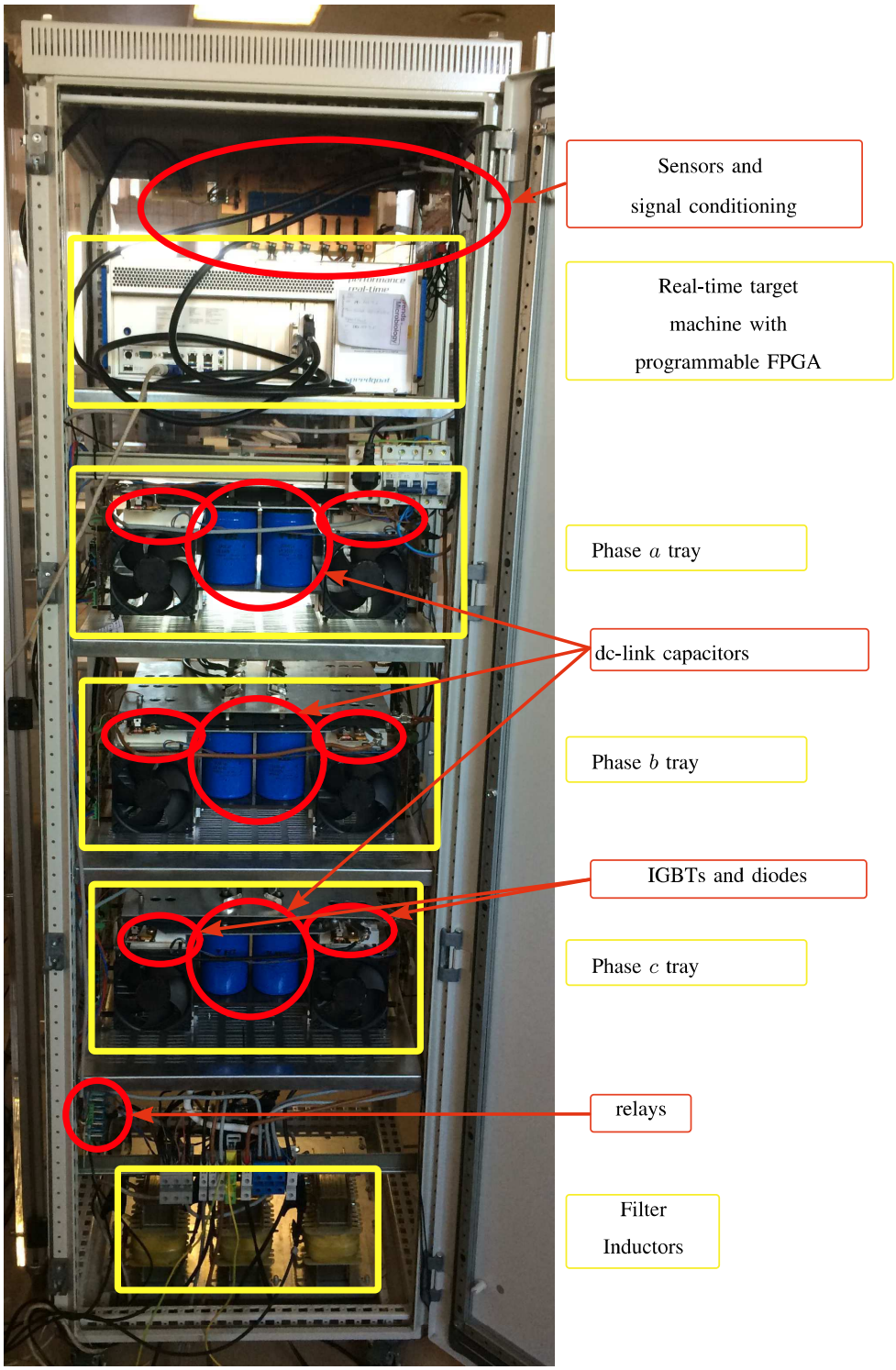

Fig. 7. Five-level DCC used to obtain the experimental results

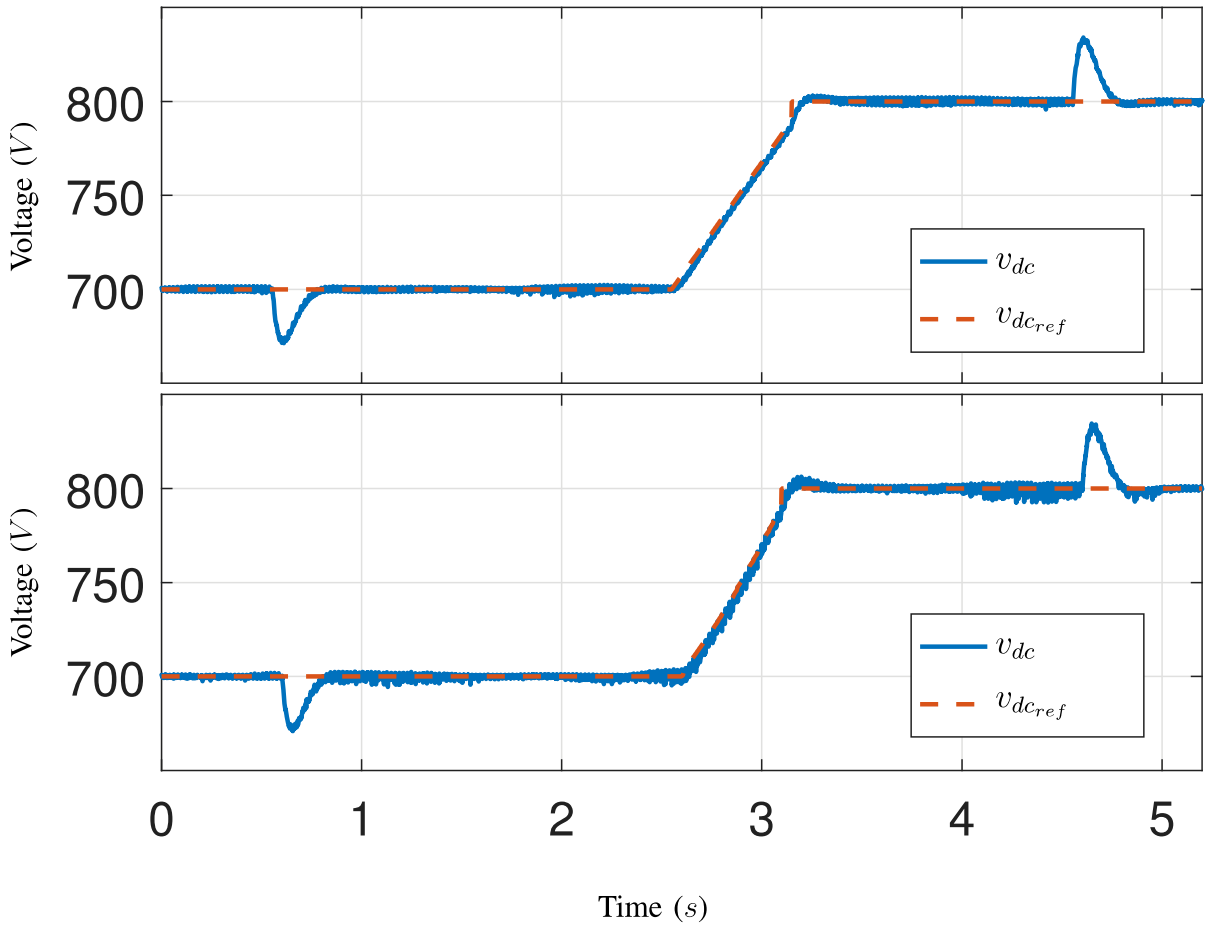

Fig. 8. Experiment: Behavior of the total dc-link capacitor voltage (solid) and its reference (dashed) for both the original algorithm (top) and the modified one (bottom).

enough it may be suppressed by the dead-time and delays presence. Therefore, this issue should be considered when selecting a proper value of k_1, k_2, k_3

Finally, the harmonic spectrum of the currents corresponding to Fig. 9 are shown in Fig. 12 where it can be seen a slight reduction in the switching frequency component when the modification is considered due to the reduction in the number of commutations. For clarity purposes, only the harmonics below the 20^{th} and between the 195^{th} and 205^{th} are shown. The THD value depicted refers to the one obtained by the power quality analyzer.

VI. Conclusions

A specific controller for balancing the capacitor voltage in five-level diode-clamped rectifier has been designed and tested through simulation and experiments at the same time the remaining

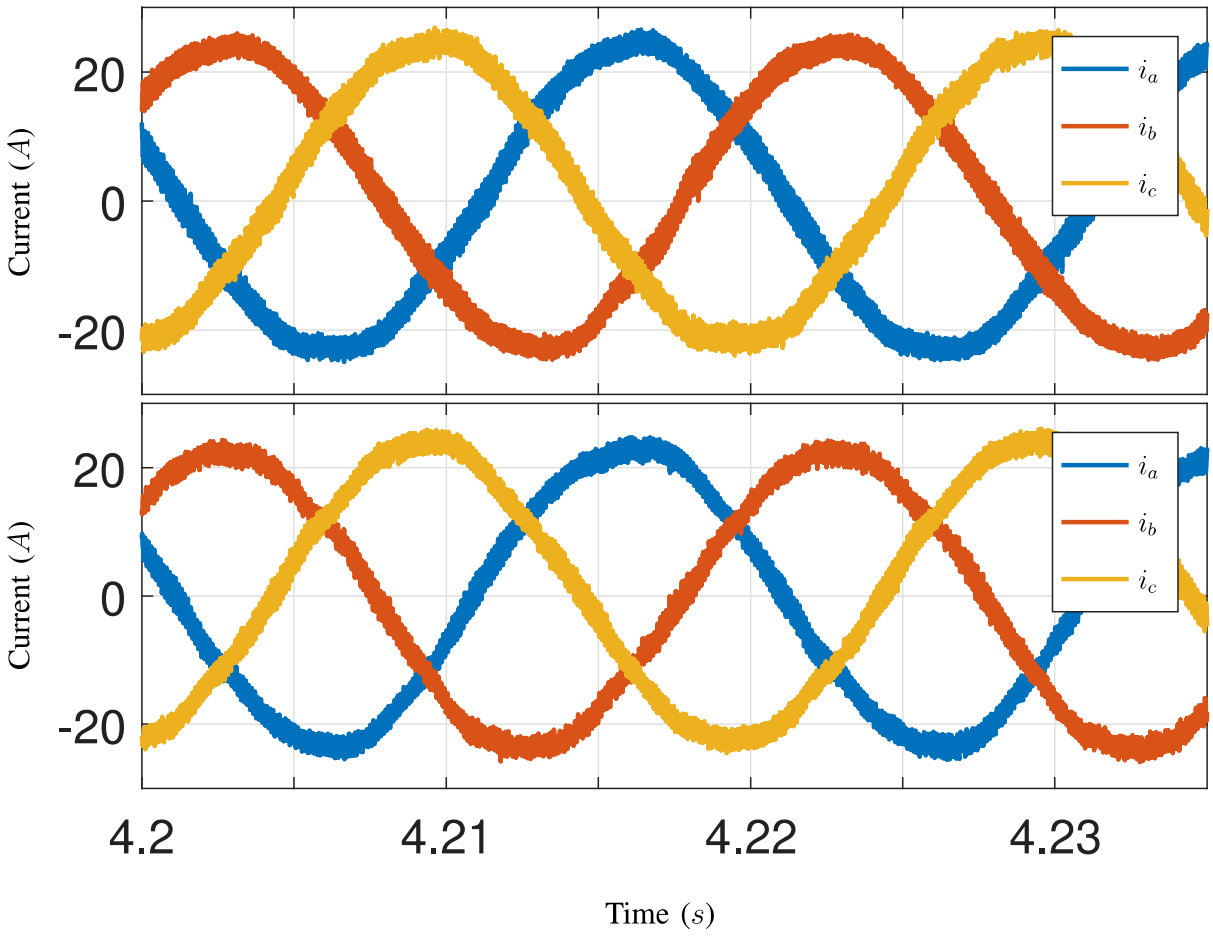

Fig. 9. Experiment: Behavior of the phase currents with the original algorithm (top) and the modified one (bottom). $R = 60\,\Omega$ and $v_{dc} = 800\,V$.

control objectives are assured. The way the rectifier has been presented allow the implementation of several strategies for current or power control, presenting in this paper a well-known DPC strategy. Simulation and experimental results have shown the good performance of the system under the proposed controllers, which are easier to implement than other existing approaches such as modifications of Virtual-Space-Vector. In addition, a modification in the algorithm allows the user to exploit the remaining degree of freedom associated with the homopolar component in such a way that the number of commutations is reduced.

This technique could be easily applied to DCC with more than five levels by applying the same procedure done here: defining a number of balancing signals equal to the number of levels minus 2; obtaining the dynamic of these signals in $\alpha\beta$ frame; defining some control inputs in terms

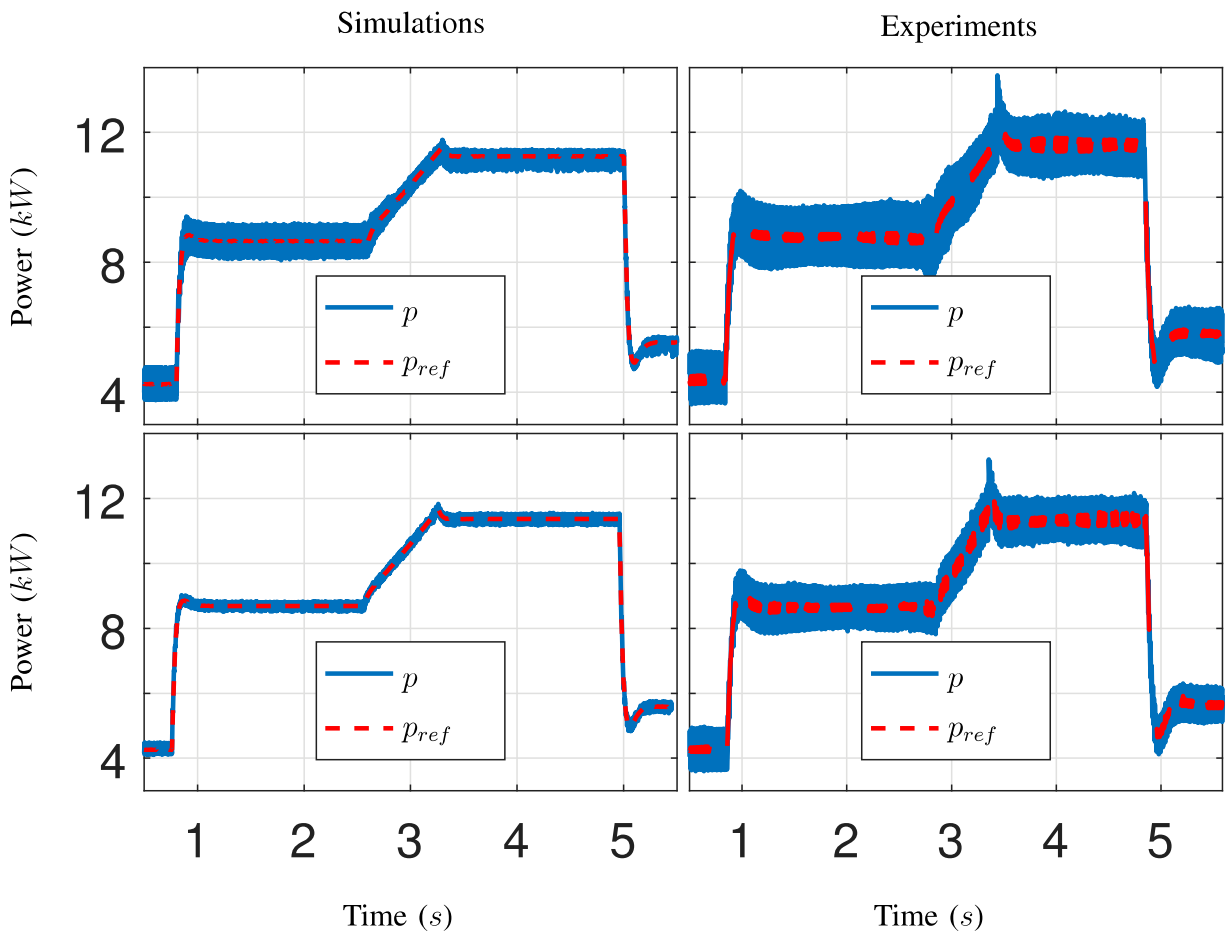

Fig. 10. Simulation and Experiment: Behaviour of the instant active power (solid) and its reference (dashed) for both the original algorithm (top) and the modified one (bottom).

of duty ratios to simplify these dynamics; and applying a simple control logic that guarantee stability in closed loop.

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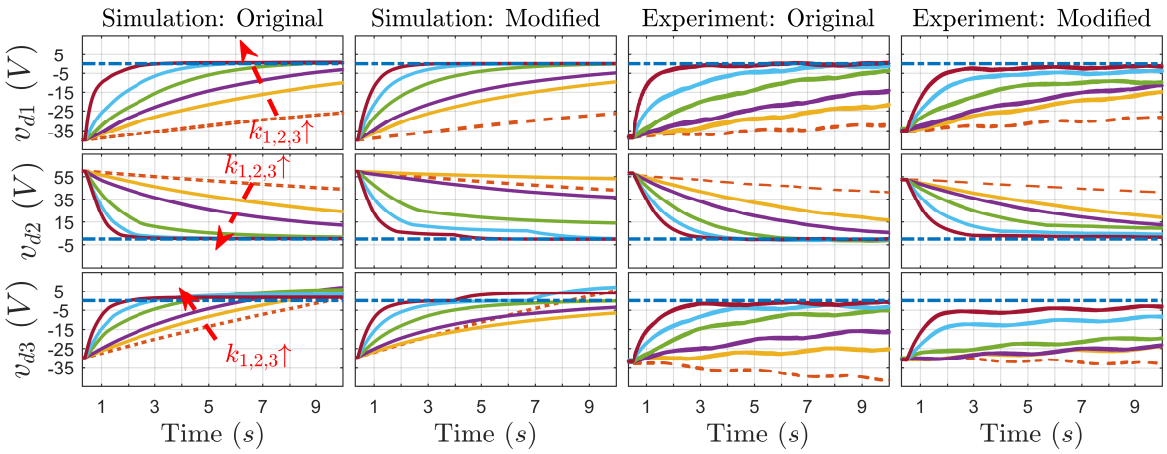

Fig. 11. Simulation and Experiment: Behavior of the error signals according to the value of k_1, k_2, k_3 for the original algorithm and the modified one either in simulations (two of the left hand side) and experiments (two of the right hand side). The values of k_1, k_2, k_3 are always equal and vary accordingly to $\{0, 10^{-5}, 2 \cdot 10^{-5}, 5 \cdot 10^{-5}, 10^{-4}, 2 \cdot 10^{-4}\}$ along the different tests. The dashed curves are the ones with the balance control deactivated ($k_1 = k_2 = k_3 = 0$) and the dashed-dotted ones are the zero-value curve.

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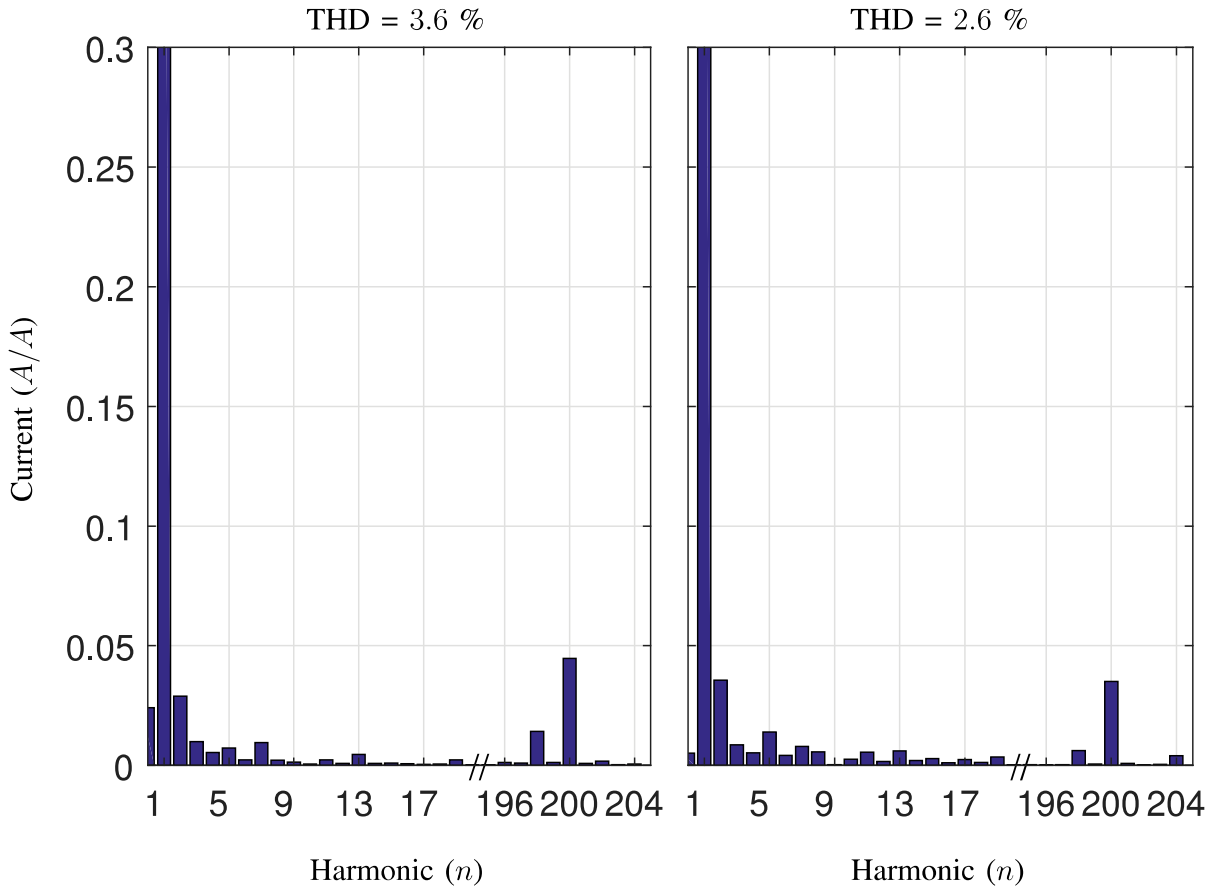

Fig. 12. Experiment: Harmonic Spectrum of the current in both the original algorithm (left) and the modified one (right). $R = 60\ \Omega$ and $v_{dc} = 800\ V$

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His research interests focus on nonlinear control with applications to mechanical, electromechanical and power electronics systems.