Offset-calibration with Time-Domain Comparators Using Inversion-mode Varactors

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***Abstract*—This paper presents a differential time-domain comparator formed by two voltage controlled delay lines, one per input terminal, and a binary phase detector for comparison solving. The propagation delay through the respective lines can be adjusted with a set of digitally-controlled inversion-mode varactors. These varactors provide tuning capabilities to the comparator; feature which can be exploited for offset calibration. This is demonstrated with the implementation of a differential 10-bit SAR-ADC. The design, fabricated in a 0.18μm CMOS process, includes an automatic mechanism for adjusting the capacitance of the varactors in order to calibrate the offset of the whole converter. Correct functionality was measured in all samples.**

***Index Terms*—Offset calibration; Time-domain comparator; SAR-ADC; Inversion-mode varactors; Forward calibration.**

I. Introduction

Successive approximation register analog-to-digital converters (SAR-ADC) [1], [2], [3] are among the preferred options for data conversion in low power scenarios as, for instance, in implantable biomedical devices. Due to the slowly varying physiological signals and their limited dynamic range, data converters should exhibit modest resolution and low sampling rates. This makes SAR converters a suitable conversion approach as they can exhibit power consumptions in the order of nWs [4]. However, besides power efficiency, care must be taken on preserving the characteristics of the captured signals after conversion, so that their processing leads to correct diagnosis or appropriate actions.

This paper focuses on the cancellation of dc offsets in biomedical recording systems to allow for an offset-free digital processing of captured signals, which otherwise could lead to erroneous estimations. For instance, there are cases in which the digital processing of bio-signals relies on the implementation of threshold detection algorithms, as in the analysis of heart rates or neural action potentials [5]; or focuses on the energy calculation in relevant frequency bands, as in the processing of neural local field potentials or EEG signals [6]. In the former case, offset-related errors may induce that events are erroneously skipped whereas, in the latter, dc offsets can contaminate energy estimates with signal-dependent terms. Hence, offsets have to be suitably canceled or significantly reduced before any signal processing task takes place.

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Given the expected low temperature and voltage supply variations in the targeted applications (wearable/implanted devices work at about the body temperature and are often supplied by batteries and/or regulated with LDOs), background offset calibration techniques, as proposed in [7], [8], are not a major requirement. Instead, foreground calibration approaches suffice in typical scenarios, potentially leading to simpler circuits and smaller die area occupations.

In this work a foreground calibration technique is proposed which relies on the use of a tunable time-domain comparator within the SAR ADC [2], [4]. Such comparator uses two Voltage-Controlled Delay Lines (VCDL), which are not preceded by any voltage pre-amplifier stage. Instead of reconfigurable differential pairs [9], bulk transistor tuning [10], digitally-controlled cascode transistors or programmable capacitor banks [11], the proposed approach uses digitally-controlled inversion-mode varactors for offset cancellation.

Compared to more conventional techniques, such as autozeroing, the proposal offers the following advantages: (i) it is an open loop system, preventing possible instabilities, (ii) neither capacitive nor resistive DACs are needed since the offset voltage is not stored, (iii) no extra clock cycles are needed in ordinary conversions, (iv) small pMOS varactors are used and, hence, the impact on the overall area of the ADC is low; (v) the calibration digital circuit follows a low-complex binary search approach and incurs in very low power consumption. Additionally, taking advantage of the foreground operation, the technique can be employed not only to cancel the offset of the ADC, but also the residual offset due to mismatch effects or switch charge injections of preceding blocks, e.g., programmable amplifiers, filters, or buffers [5]. This can be done by driving the input of the chain to a state ideally leading to null offset and, afterwards, running the calibration process to tune the VCDLs and correct the accumulated dc deviation. In the proposal, the obtained correction range is around $\pm$10mV. As will be shown, this is more than enough for correcting the offset of the SAR ADC itself, thus giving room for the eventual offset cancellation of additional blocks.

This work extends the results in [12] and presents analytical and experimental results for the offset calibration of a differential 10-b rail-to-rail monotonic mid-tread SAR converter. Section II describes the offset-correction time-domain (OCTD) comparator and the proposed calibration technique. Then, Section III develops an analytical model which is later used in Section IV for circuit sizing. Section V shows the performance of a prototype, fabricated in a 0.18μm CMOS process, and illustrates the effectiveness of the proposed approach. Finally, Section V concludes the paper.

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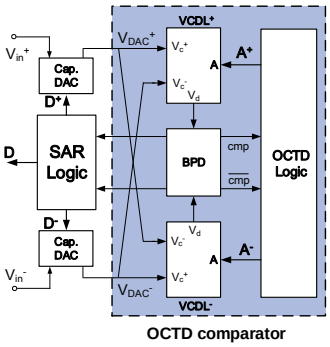

Figure 1. OCTD comparator embedded in an ADC converter.

II. OCTD COMPARATOR

The OCTD comparator, driven by the DACs of a differential SAR converter, is shown in Fig. 1. It consists of two voltage controlled delay lines (denoted as VCDL^{+} and VCDL^{-}) which are cross-connected to the outputs of the DACs, a binary phase detector (BPD) [3], and some control logic. As shown in Fig. 2(a), each delay line consists of a cascade of $N = 2^m - 1$ digitally controlled delay stages, comprised between two dummy stages for providing the same loading and driving conditions to the elements of the array [3]. All the stages are nominally identical and consist of two current-starved inverters (CSI) followed by an inversion-mode pMOS varactor connected via its gate terminal. As shown in Fig. 2(b), an nMOS transistor driven by the negative input of the comparator starves the current available through the first inverter (denoted as CSI_n); while a complementary configuration, with a pMOS current limiting transistor, driven by the positive input of the comparator, is used for the second inverter (denoted as CSI_p). The capacitances of the varactors depend on the voltage applied to their shorted drain-source terminal, V_a<i>, $i = 1, ..., N$. This voltage can be either V_{DD} or V_{SS} according to the binary values of a thermometer-coded N-bit word $\mathbf{A}$.

The OCTD block obtains the result of the comparison based on the phase difference between the output signals of the VCDLs when a rising clock signal edge is propagated along the lines. The delay of each VCDL can be digitally tuned through the digital word $\mathbf{A}$. This tuning capability supports the foreground offset calibration technique here proposed.

The procedure starts by short-circuiting the ADC inputs to the common mode voltage V_m which, in this work, it is assumed, without loss of generality, to coincide with the mid-rail voltage. Additionally, the control words $\mathbf{A}$ of both delay lines are initialized with their bits to '1'. A first conversion cycle obtains the actual offset of the complete ADC. This value is compared to the converter mid-range code (in this work, due to the mid-treat quantization, codes '511' and '512' are considered equally valid). If the ADC output, $\mathbf{D}$, coincides with the midrange code, the procedure stops. Otherwise, the OCTD logic identifies the slower VCDL and $2^{(m-j)}$, $j = 1$, bits of its associated vector $\mathbf{A}$ are set to '0'. Meanwhile, the control word of the faster VCDL remains unchanged. With this configuration, a new conversion cycle takes place using again V_m as input and comparing the result with the midrange code.

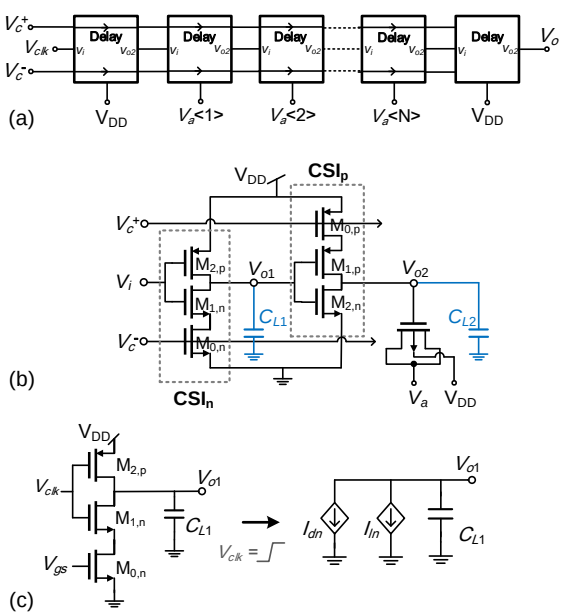

Figure 2. (a) VCDL structure. (b) Schematic of the delay stage. (c) Equivalent model of CSI_n at the V_{clk} $0 \rightarrow 1$ transition.

The process is repeated for $j = 2, ..., m$ following a binary search algorithm, until the control bits of the slower VCDL are solved. Once the calibration procedure is finished, the resulting $\mathbf{A}$ words of the delay lines (denoted as $\mathbf{A}^{+}$ and $\mathbf{A}^{-}$ in Fig. 1) are saved for later use in ordinary conversions. Note that the calibration process takes, at most, $m+1$ conversion cycles, if not terminated earlier in an intermediate step.

III. VCDL MATHEMATICAL MODEL

Figure 2(c) shows a simplified equivalent circuit model of an n-type current starved inverter, CSI_n, when a $0 \rightarrow 1$ step input transition is applied to the clock port. A similar model can be drawn for a CSI_p for the opposite clock transition. In Fig. 2(c), I_{dn} represents the current drained by transistor $M_{0,n}$, I_{ln} models the losses from transistors $M_{1,n}$ and $M_{2,p}$, and C_{L1} is the capacitive load formed by the output capacitance of the cell and the input capacitance of the following CSI_p block. The dynamics of the equivalent circuit is thus described by the differential equation, $C_{L1}\frac{dV_{o1}}{dt} + I_{ln} + I_{dn} = 0$.

Assuming that C_{L1} is constant along the output node transition, losses are negligibly small as compared to I_{dn}, and the voltage drop across $M_{1,n}$ is small so that the drain-source voltage of $M_{0,n}$ can be approximated by V_{o1}, the time elapsed until the output reaches $V_{DD}/2$ when a rising clock step is applied to the CSI_n cell is given by $t_{sn} = \nu_n \frac{C_{L1}}{I_{dn}}$, where ν_n is a parameter in voltage units which depends on the operation mode of transistor $M_{0,n}$ (see expressions for ν_n in [13] and [14] for strong- and weak-inversion operation modes, respectively).

A similar analysis allows to obtain the time delay of the p-type current starved inverter of Fig. 2(b) during a $1 \rightarrow 0$ step clock transition. In this case, an additional inversion-mode varactor with capacitance $C_{var}(V_a)$ loads the inverter. This capacitance varies nonlinearly with the gate voltage,

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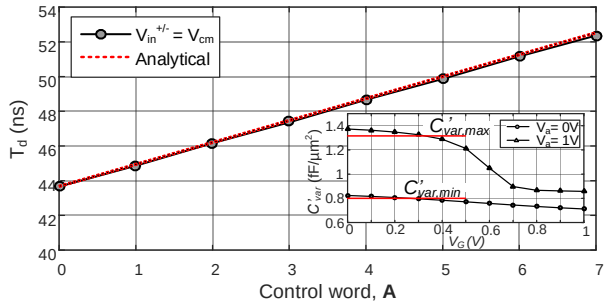

Figure 3. VCDL total delay analytical and electrically simulated curves for N=7 versus **A**. Inset: Inversion-mode varactor specific capacitance per unit area C'_{var} versus V_G.

more noticeably when the control node $V_a = V_{DD}$. This is illustrated in the inset of Fig. 3 which plots the specific capacitance per unit area of a varactor at 1V supply in the selected technology. Despite this nonlinear dependence with the output voltage of the inverter, to keep the analysis simple, it is assumed that the varactor capacitances take on constant values until reaching $V_{DD}/2$, as shown by the red lines in the inset. With this assumption, the time delay of a CSI$_p$ cell is

$$t_{sp}(V_a) = \nu_p \frac{C_{L2} + C_{var}(V_a)}{I_{dp}} \tag{1}$$

Using the definitions of t_{sn} and t_{sp}, the total time delay of the VCDL structure in Fig.2(a), can be calculated as

$$T_d = \sum_{i=1}^{N} t_{dp,i} + N t_{dn} + t_{dum} \tag{2}$$

where $t_{dum} = 2(t_{dn} + t_{dp}(V_{dd}))$ is the contribution from the dummy cells, $t_{dp,i} = (1+\eta_p)\cdot t_{sp}(V_a\text{<}i\text{>})$, $t_{dn} = (1+\eta_n)\cdot t_{sn}$ and parameters η_p and η_n account for the gradual changes of the clock signals [15].

Fig. 3 plots the simulated total time delay of a VCDL for an input voltage $V_c^+ = V_c^- = V_m$. Time delay T_d is calculated for all the possible configuration of vector **A** (for $N = 7$). Note that T_d linearly increases as the number of varactors with their control voltage connected to V_{DD} increases. Further, Fig. 3 also shows the good agreement between the simulated data and the analytical results from (2).

The difference ΔT_d between the total delays obtained by VCDL$^+$ and VCDL$^-$ when an offset ΔV is present at their inputs, i.e., $V_c^+ = V_m + \Delta V/2$ and $V_c^- = V_m - \Delta V/2$, is approximately given by:

$$\begin{aligned}\Delta T_d &\approx \sum_{i=1}^{N}\left(\Delta t_{dp,i} + \overline{t_{dp,i}}\cdot\frac{|g_{mp}|}{I_{dp}}\Delta V\right)\\ &+\left((N+2)t_{dn}\cdot\frac{g_{mn}}{I_{dn}} + 2t_{dp}(V_{DD})\cdot\frac{|g_{mp}|}{I_{dp}}\right)\Delta V \qquad (3)\\ &\doteq \sum_{i=1}^{N}\Delta t_{dp,i} + G_{VT_x}\Delta V\end{aligned}$$

where $\Delta t_{dp,i} = t^+_{dp,i} - t^-_{dp,i}$ is the delay difference between the i-th CSI$_p$ units in VCDL$^+$ and VCDL$^-$, $\overline{t_{dp,i}}$ represents the average of both delays, and g_{mn} and g_{mp} denote the transconductances in the quiescent point of transistors $M_{0,n}$ and $M_{0,p}$, respectively (see Fig. 2(b)). G_{VT_x} represents the voltage-to-time conversion gain of the OCTD comparator [3]. It depends on the number x of varactors which are switched to V_{SS} on the slower VCDL.

Table I
TRANSISTOR SIZING OF DELAY CELL

$W_{0,p} = r_{pn}W_{0,n}$	$W_{2,p} = r_{pn}W_{0,n}$	$W_{2,n} = W_{0,n}$
$W_{1,p} \gg W_{0,p}$	$W_{1,n} \gg W_{0,n}$	

Note that the term in $\Delta t_{sp,i}$ does not depend on ΔV and, hence, it can be exploited, by properly setting vectors $\mathbf{A}^+$ and $\mathbf{A}^-$, for reducing $|\Delta T_d|$ in the presence of an offset voltage. This offset can be generated, in practice, by mismatch and noise effects in the VCDL blocks of the comparator, as well as, by preceding stages of the SAR converter.

Based on (2), the variance of the total time delay of a VCDL due to mismatch is given by:

$$\sigma^2_{T_d,mis} = (N+2)\left(\sigma^2_{t_{dp}} + \sigma^2_{t_{dn}}\right) \tag{4}$$

where $\sigma^2_{t_{dp}}$ and $\sigma^2_{t_{dn}}$ can be estimated in terms of the statistical variations of the threshold voltage and current factor of transistors $M_{0,p}$ and $M_{0,n}$, respectively. For $\sigma^2_{t_{dp}}$, a 5% of standard deviation in varactors has been considered as well.

Regarding noise, following a procedure similar to [3], it can be found that the time delay variance due to thermal noise fluctuations is given by,

$$\sigma^2_{T_d,noise} = (N+2)\left(\frac{t_{sp}}{\nu_p I_{dp}}\alpha_p + \frac{t_{sn}}{\nu_n I_{dn}}\alpha_n\right)kT \tag{5}$$

where α_p and α_n are noise factors of the CSI$_p$ and CSI$_n$ cells, respectively. From (4) and (5), the variance of the delay difference ΔT_d can be estimated as,

$$\sigma^2_{\Delta T_d} \approx 2\left(k_{mis}\cdot\sigma^2_{T_d,mis} + k_{noise}\cdot\sigma^2_{T_d,noise}\right) \tag{6}$$

where parameters $k_{mis} > 1$ and $k_{noise} > 1$ have been added for empirical adjustment.

IV. DESIGNING VCDL FOR OFFSET CANCELLATION

In the proposed design, transistors in CSI$_n$ and CSI$_p$ have been sized seeking (i) to reduce the total area occupation of the delay stages, (ii) to lower the delay variability due to mismatch and noise (all transistors are designed with channel length L higher that the minimum technology value), and (iii) to make the varactor capacitances have a noticeable impact on the time delay $t_{sp}(V_a)$ in (1).

Additionally, CSI$_n$ and CSI$_p$ have been designed to have their switching thresholds around mid-rail for reducing noise margins. Hence, assuming that transistor $M_{1,n}$ is much wider than $W_{0,n}$, the width of transistor of $M_{2,p}$ is sized as $W_{2,p} = r_{pn}W_{0,n}$, where r_{pn} is approximately given by the NMOS/PMOS mobility ratio. Similar considerations lead to the sizing strategy in Table I.

Sizing of the varactor is mainly determined by the convergence of the calibration procedure described in Sec. II. This is guaranteed whenever the equivalent input-referred voltage,

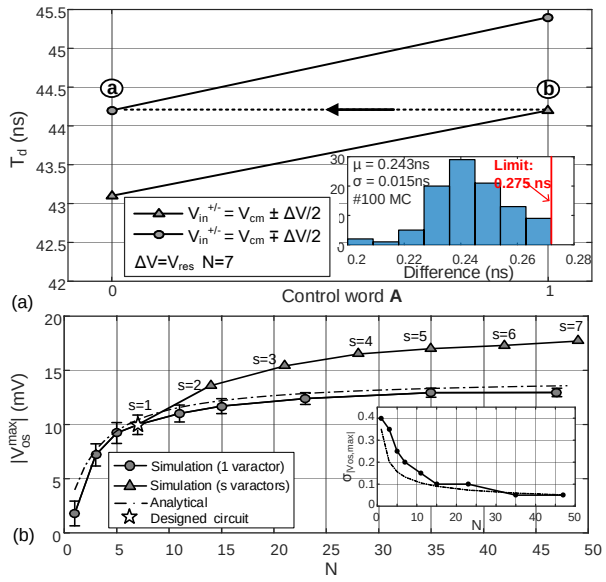

Figure 4. (a) Simulated VCDL delay for an ADC differential input signal ΔV. (inset) Histogram of the time difference of ⓐ and ⓑ. (b) Analytical and simulated values of $|V_{os}^{max}|$ in terms of N. (inset) Standard deviation of $|V_{os}^{max}|$.

obtained by switching just one varactor from the slower VCDL, is lower than the resolution of the ADC, V_{res}. Based on (3) and (6), this is expressed as:

$$G_{VT_1} \cdot V_{res} \geq (1+\eta_p)\nu_p \frac{\Delta C_{var}}{I_{dp}} + \zeta\sqrt{\sigma^2_{\Delta T_d}} \qquad (7)$$

where $\Delta C_{var} = C_{var}(V_{DD}) - C_{var}(V_{SS})$, ζ is a safety factor generally equal or greater than 3, and G_{VT_1} is the voltage-to-time conversion gain of the comparator for $\mathbf{A}^+ = \langle 1,\ldots,1,0\rangle$ and $\mathbf{A}^- = \langle 1,\ldots,1,1\rangle$ or vice versa. Eq. (7) imposes an upper limit to ΔC_{var} which must be verified under PVT and Monte Carlo variations. Note that (7) implicitly defines a trade-off between accuracy and speed as more stages are needed (G_{VT_1} approximately scales with N) if the ADC resolution decreases.

An insightful graphical interpretation of (7) is given in Fig. 4(a). It shows the total time delays of the VCDLs in Fig. 1 when a differential input signal equivalent to one LSB is applied to the OCTD comparator, i.e., $V_c^+ = V_m + V_{res}/2$ and $V_c^- = V_m - V_{res}/2$. The vertical separation between both delay curves must be compensated by switching to V_{SS} at least one varactor of the slowest VCDL (upper curve). Hence, condition (7) states that the time delay at point ⓐ should be higher than that at point ⓑ, taking into account statistical deviations and PVT variations. This defines an upper limit for ΔC_{var}. Additionally, in order to reduce the number of switchings needed to compensate one LSB, a lower limit for ΔC_{var} has to be imposed by making the time difference between points ⓐ and ⓑ small. The inset in Fig. 4(a) shows the histogram of a Monte Carlo simulation (100 instances) of such time difference in a fast-p corner (lower sensitivity to ΔC_{var} variations). As it can be seen, the time difference is positive, as required by (7), and amounts 0.275ns (3-σ).

The maximum offset range $|V_{os}^{max}|$ which can be covered by the structure of Fig. 1 is given by,

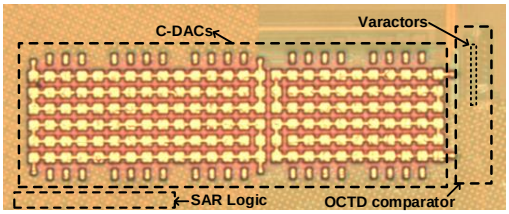

Figure 5. Micro-photograph of the fabricated SAR-ADC.

$$|V_{os}^{max}| \leq \frac{(1+\eta_p)\nu_p}{I_{dp}} \frac{N\cdot\Delta C_{var}}{G_{VT_N}} - \frac{\zeta\sqrt{\sigma^2_{\Delta T_d}}}{G_{VT_N}} \qquad (8)$$

where G_{VT_N} is the voltage-to-time conversion gain of the comparator for $\mathbf{A}^+ = \langle 0,\ldots,0,0\rangle$ and $\mathbf{A}^- = \langle 1,\ldots,1,1\rangle$ or vice versa. Fig. 4(b) plots $|V_{os}^{max}|$ in terms of N both calculated from (8) and using electrical simulations (3-σ error bars superposed). The comparator has been sized to satisfy (7) for $N = 7$. The *same* design for the VCDL cells has been used for all other values of N. It is worth noting the good agreement between the simulated mean values of $|V_{os}^{max}|$ and the corresponding analytical values. Also note that $|V_{os}^{max}|$ tends to a constant value for large N, because G_{VT_N} roughly scales with N. The second term in (8) accounts for the $|V_{os}^{max}|$ error, and it approximately scales with $1/\sqrt{N}$, as shown in the inset of Fig. 4(b). Hence, the impact of mismatch decreases with the number of stages. Fig. 4(b) also plots $|V_{os}^{max}|$ in terms of N when an additional varactor is added in parallel to the VCDL cell every time the number of stages in the delay line doubles. This effectively increases ΔC_{var} and extends the offset correction range of the comparator as N increases. Thus, for instance, $|V_{off}^{max}|$ is approximately 34mV$_{pp}$ differential for $m = 5$, when five varactors load every delay stage.

V. Implementation

The SAR-ADC architecture, presented in [12], was fabricated in a High-Voltage 0.18μm CMOS process. The micro-photograph of the chip, shown in Fig. 5, has an active area of 165μm×440μm. Comparator and calibration circuitry occupy 7.8% and 1.8% of the total ADC area, respectively. The activation of the delay stages uses axial symmetry [12].

The delay lines and programmable varactors have been sized following the procedure in Sec. IV for $m = 3$ (each VCDL comprises 7 digitally controlled delay cells). The comparator was designed to have a correction step of approximately 1.4mV$_{pp}$ to satisfy (7). With this structure, post-layout simulations show that the offset range, which can be canceled up by the OCTD comparator alone, is comprised between ±4.7 and ±5.3 LSBs, taking into account 3-σ deviations as in [1][9]. Further, it was found that the 3-σ input offset of the comparator amounts ±0.6mV (σ = 0.2mV).

The sampling rate is f_s = 4kS/s for a clock frequency of 52kHz. The SAR-ADC is supplied with 0.5V for the digital circuits, and 1V for the rest of the system. The total power consumption is 76.2nW of which 28.6nW are consumed by the OCTD comparator. The linearity performance of the ADC at low frequencies is illustrated with the DNL and

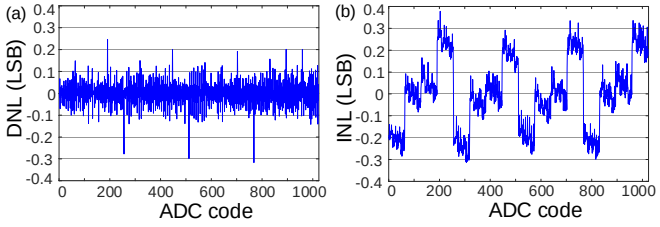

Figure 6. (a) INL and (b) DNL

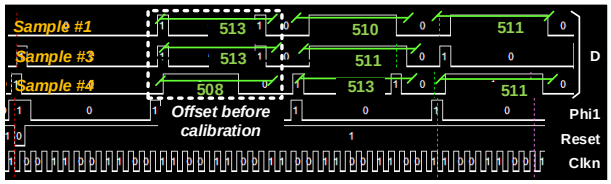

Figure 7. Offset-correction evolution for three samples.

INL plots in Fig. 6, which show peak values of 0.31 and 0.38, respectively. Close to Nyquist rate, the ADC obtains about 70dB of Spurious-Free Dynamic Range (SFDR) and an Effective Number of Bits (ENOB) higher than 9.5-b after calibration. Moreover, according to our simulations, the calibration procedure allows to improve the ENOB and SFDR by 0.1-b and 0.8dB, respectively.

To verify the proposed offset-correction technique, seven ADC samples were tested. In all cases, the ADC output **D** converged satisfactorily to mid-range. In three of them, the offset before calibration exceeded 1-LSB and, for these cases, Fig. 7 shows the evolution of vector **D** along the offset calibration process described in Sec.II.A. In a first conversion cycle (marked by the dotted box), the control logic of the OCTD comparator detects the corresponding offset deviation. Afterwards, acting on the varactors of the slower VCDL, the output of the ADC is adjusted up to the desired code ($\mathbf{D} = 511$ or $\mathbf{D} = 512$). Fig. 8 shows the correction range measured for one of these samples when an external offset is injected at its inputs. In this sample, the mechanism is able to correct more than ± 5 LSBs, enough to cancel the offset of the SAR-ADC, including the input referred offset of the comparator. In fact, it corrects its own offset (about ± 0.35 LSBs), as well as more than ± 4 LSBs of offset from other sources.

A performance summary is presented in Table II. The power consumption and offset correction range of the proposed comparator, as well as the area occupied by the calibration

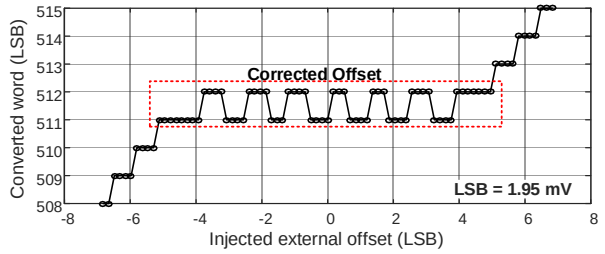

Figure 8. Total $|V_{os}^{max}|$ versus the injected external offset.

Table II
PERFORMANCE COMPARISON OF OFFSET-CANCELING COMPARATORS

	This work	[1]	[10]	[16]	[9]
Technology (nm)	180	90	500	65	180
Supply (V)	1	0.4	5	1	1.5
Offset Range (mV)	$\pm$10	$\pm$12.5	-8.3/+5.6	–	5.4
Cal. Area (mm^2)	1.35m	4.4m	–	7.7m	46.8m
Clock Freq. (Hz)	52k	7.5M	200k	500M	1M
Power (μW)	0.028	–	4.65	>20	13.5
Energy (pJ)	0.54	-	23	0.04	13.5

mechanism, are either comparable or better than prior art. Only the proposal in [16] has better energy consumption but consumes more active area, despite it was designed in 65nm.

VI. CONCLUSIONS

This brief presents a differential time-domain comparator featuring offset correction mechanisms. It relies on equalizing the time delays between the two differential signal paths by conveniently switching to the supply rails a set of inversion-mode varactors. As a proof of concept, the comparator was embedded in a SAR-ADC converter and tests over different samples proved the correct operation of the calibration process.

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