A Sub-μV_{rms} Chopper Front-End for ECoG Recording

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***Abstract*—This paper presents a low-noise, low-power fully differential chopper-modulated front-end circuit intended for ECoG signal recording. Among other features, it uses a subthreshold source-follower biquad in the forward path to reduce noise and avoid the implementation of a ripple rejection loop. The prototype was designed in 0.18μm CMOS technology with a 1V supply. Post-layout simulations were carried out showing a power consumption below 2μW and an integrated input-referred noise of 0.75μV_{rms}, with a noise floor below 50 nV/$\sqrt{\text{Hz}}$, over a bandwidth from 1 to 200Hz, for a noise efficiency factor of 2.7.**

***Index Terms*—Brain Machine Interfaces; Analog front-end; Neural Recording; Chopper; Low Noise; Low Power; Front-End; LNA; ECoG.**

I. Introduction

The emergence of intracranial BMIs (Brain-Machine Interfaces) [1] as well as the search for alternative therapies based on micro/nanoelectronics able to palliate neurological pathologies such as epilepsy, Parkinson's or Alzheimer's disease [2], has fostered the development of sophisticated neural recording systems. These devices must meet severe clinical constraints in terms of functionality, size and safety; and comply with challenging requirements on noise performance, low power consumption and high dynamic range.

One of the neural recording methods which is currently deserving more attention is Electrocorticography (ECoG), where electrical activity is captured from the exposed cerebral cortex. EcoG offers higher resolutions than non-invasive techniques, such as Electroencephalography (EGG) [3], but it may cause smaller tissue damages and potentially allow for more stable and longer recording periods compared to intracortical implants [4]. Therefore, ECoG represents an interesting mid-risk alternative for neural recording.

ECoG signals are characterized by their very low amplitude, which ranges between $5 - 500\mu$V [5]; and their low frequency content, between 1Hz and 200Hz, which coincides with the frequency band where noise in MOS technologies is dominated by flicker contributions. These features call for the use of high gain and low-noise recording techniques. In particular, care must be taken to reduce the noise level at the upper frequencies of the ECoG band, where the power content of signals is smaller [6]. Besides, neural front-ends have to satisfy others design constraints such as low power consumption, low area occupation and high linearity [2].

A common technique to reduce 1/f noise is chopper modulation [7]. According to this method, signals are modulated, amplified and demodulated to move offset and 1/f noise away from DC. Square-wave modulating signals with 50% duty cycle are used for implementing this frequency shifting operation, which ideally does not affect the spectrum of the recorded signal. Finally, a low-pass filter is used to remove frequency up-converted noise contributions and other undesired components due to imperfections in the modulation process. Hence, the final filtering stage is a critical piece in chopper-modulated front-ends.

Several front-ends specially aimed for ECoG recording have been reported [4], [8]–[11]. Some of them obtain very low noise and low power performance [10], however they do not include methods to deal with the large DC offsets at the electrode-tissue interface. In other cases, the front-end exhibits low input impedance [4], high power consumption [8] or high input-referred noise [9].

In this work, we propose a chopper-modulated front-end for ECoG recording which takes into account the above aspects and obtains, according to post-layout simulations, a power consumption of 1.89μW, an integrated input-referred noise of $0.75\mu V_{rms}$ in the bandwidth from 1 to 200Hz, with a spot noise power spectral density below 50 nV/$\sqrt{\text{Hz}}$ at 200Hz, an input impedance larger than $100M\Omega$ over the referred bandwidth, an output ripple of 1.3μV for 1mV_{pp} input, and an input range of $\pm$50mV before the onset of saturation with a residual offset lower than $\pm 500\mu$V.

The paper is organized as follows. Section II describes the topology of the proposed front-end. Section III shows post-layout simulation results in a 0.18μm CMOS technology. Finally, the conclusions are drawn in Section IV.

II. Chopper Front-end for ECoG Recording

Fig. 1 shows the block diagram of the proposed fully-differential chopper-modulated amplifier. A cascade of two transconductance amplifiers, OTA_1 and OTA_2, represents the core of the circuit. The block is chopper modulated at a frequency, f_{chop} =1kHz, which is high enough to significantly decrease flicker noise contributions, but not too large so as to severely reduce the input impedance of the chopper amplifier or increase the bandwidth requirements of the OTAs. Transconductors OTA_1 and OTA_2 employ current reuse topologies with input transistors in weak inversion for maximum transconductance efficiency [12]. A DC feedback loop around the OTAs, implemented by the pseudo-resistors R_{fb}, sets a stable biasing point for the front-end. The gain

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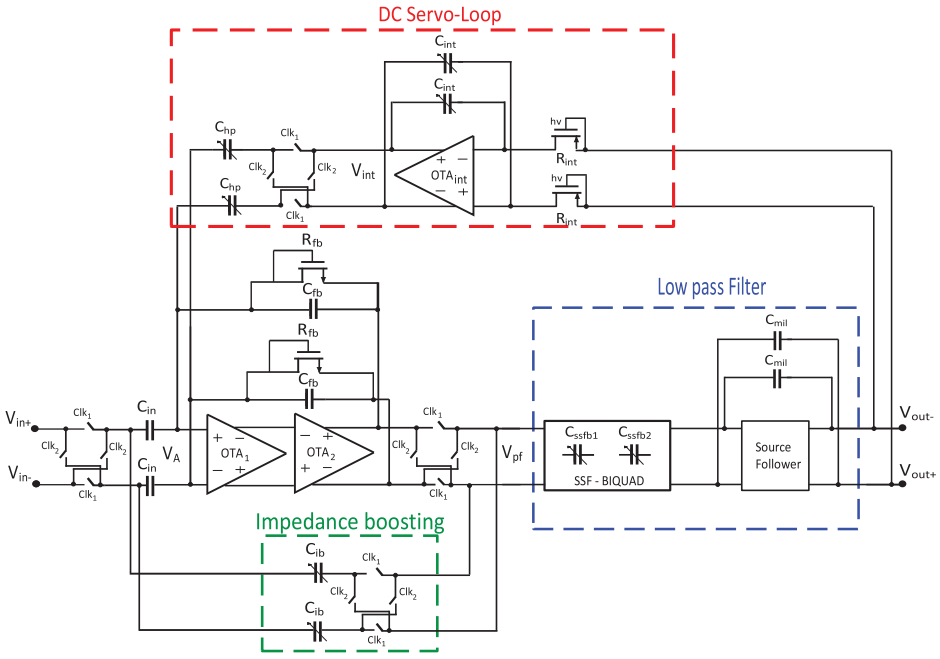

Fig. 1. Proposed fully differential chopper front-end.

of the chopper amplifier is mainly defined by the ratio of the input and feedback capacitors, i.e., $A \simeq C_{in}/C_{fb}$.

In order to increase the input impedance of the chopper amplifier, a positive feedback loop has been added around the main circuit core [13]. By setting the impedance boosting capacitors, C_{ib}, equal to the feedback capacitors, C_{fb}, it can be shown that the input impedance can be ideally increased by a factor equal to the gain of the chopper amplifier, A [14]. In practice, smaller increments can be achieved because of the degrading effect of parasitic capacitances. To ensure stability and set the highest input impedance possible, C_{ib} has been implemented as a digitally-controlled capacitor bank. According to our simulations, more than 100MΩ input impedance can be obtained by properly tuning C_{ib}.

Additionally, an integrator-based DC servo-loop (DCSL) is used to mitigate the up-modulated DC offset from the recording electrodes. This stage, which must present a high loop gain at low frequencies [5], defines the high-pass pole of the chopper amplifier as:

$$f_{hp} = \frac{C_{hp}}{C_{fb}} \frac{1}{2\pi \cdot C_{int} \cdot R_{int}} \tag{1}$$

where C_{hp} is the output capacitor of the servo-loop, and C_{int} and R_{int} are, respectively, the capacitors and the input resistances of the integrator.

Contrarily to previous proposals in which continuous-time common-mode feedback (CMFB) techniques are conventionally used [13] [15] [16], all the transconductors in the proposed design use switched-capacitor CMFB circuits, because they do not impose any restriction on the maximum allowable differential input signals, are highly linear, and allow to save power consumption [17].

A. Noise minimization strategy

The largest noise contribution of the chopper amplifier comes from the front-end transconductor, OTA_1. Its input-referred noise is given by [12] :

$$\nu_{OTA_1} = \frac{4 \cdot k \cdot T \cdot \gamma}{g_m} + \frac{K}{f \cdot W \cdot L \cdot C_{ox}} \tag{2}$$

where g_m is the transconductance of the input differential pair, γ is 1/2 for transistors in weak inversion, K is a process-dependent constant, and the rest of parameters have their usual meanings. The first term in (2) models thermal noise while the second term represents the flicker contribution. As the thermal noise term is inversely proportional to g_m, large enough quiescent currents are needed to keep the contribution low. On the other hand, the flicker term can be completely removed by the chopper modulation as long as f_{chop} is larger than the flicker corner frequency of the technology.

Another important source of noise is the integrator in the DC servo loop. Its noise contribution referred to the input of the chopper amplifier is given by:

$$\nu_{DCSL} = \frac{C_{hp}}{C_{fb}} \cdot \nu_{int} \tag{3}$$

where ν_{int} is the noise contribution of the integrator, which is mainly due to the thermal noise generated by the resistor R_{int} [13]. Note from (3) that small values of C_{hp} are needed to keep the noise contributed by the DC servo-loop low. As long as, C_{hp} also defines the high-pass pole of the amplifier is thus

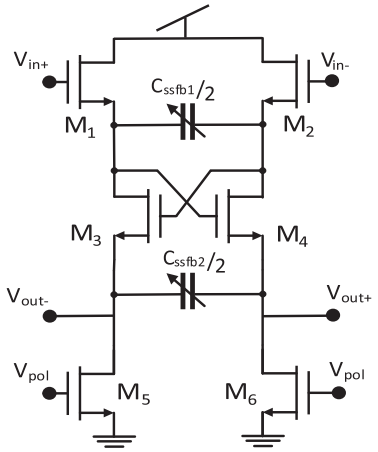

Fig. 2. Subthreshold source follower biquad.

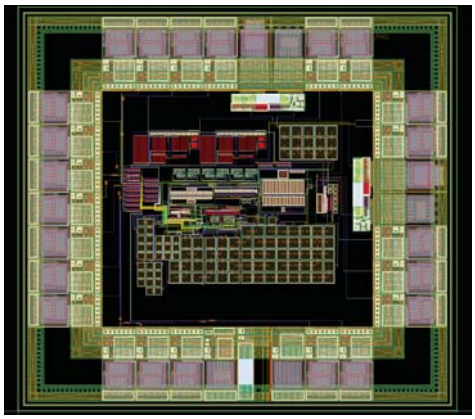

Fig. 3. Screenshot of proposed circuit layout.

important to make R_{int} very large. In the proposed design, resistors R_{int} have been implemented with pMOS pseudo-resistors. However, they exhibit large process and temperature variations, mainly because of the diodes at the p-substrate, n-well unions [18]. In order to palliate these variations and tune the high pass corner, C_{hp} has been implemented as a programmable capacitor bank. PVT simulations of the DC servo loop showed that, for every possible setting of C_{hp}, assuming a target corner frequency of 1Hz, the noise of the integrator is small compared to the noise contributed by OTA_1.

B. Low-Pass Filter

Low-pass filtering is required in chopper amplifiers to remove the high frequency harmonics arising from modulation and reduce output ripples [13], [19]. Typically, transconductor-capacitor (g_m-C) structures are used as low-pass filters. They require small transconductances if large time constants have to be implemented. This makes the filter efficient in terms of power and area, however, the structure tends to be noisy and highly nonlinear, what has motivated the search for alternative solutions [13].

In the proposed design, a subthreshold-source-follower (SSF) biquad has been used for low pass filtering. This topology, shown in Fig. 2, presents several advantages in terms of linearity, noise, area and power consumption which are extensively demonstrated and discussed in [20].

The main stage is a nMOS-based SSF Biquad compose pf transistors (M_{1-4}), two current sources (M_{5-6}) and two capacitor banks (C_{sffb1} and C_{sffb2}) to make the cut-off frequency tunable. The low-pass poles are thus giving by:

$$f_{lp} = \frac{\sqrt{(g_{m1,3} + g_{mb1,3}) \cdot (g_{m2,4} + g_{mb2,4})}}{2\pi\sqrt{C_{sffb1} \cdot C_{sffb1}}} \qquad (4)$$

where g_m, g_{mb} denote input and backgate transconductance. The gain of the stage is ideally unity,however, the body effect causes a gain loss from 3 to 5dB. Following the biquad, a p-MOS based source-follower is used to keep the common-mode voltage constant.

Using a biquad, instead of a first order filter, improves the attenuation of up-modulated noise and undesirable components due to chopper modulation. This is translated into higher linearity and noise performance. Furthermore, using a second order filter provides an significant ripple attenuation [5], with no need for an additional ripple rejection stage [19]. Indeed, the simulated output ripple amounts only 1.3μV for 1mV_{pp} input.

III. Post-Layout Simulation Results

Post-layout simulations in 0.18μm technology were carried out in order to verify the correct performance of the proposed circuit. Fig. 3 shows the layout, which occupies an active area of 0.14 mm^2. The nominal power supply of the chopper amplifier is 1V.

Fig. 4 shows the input referred noise of the circuit. For a bandwidth from 1 to 200Hz, the integrated input referred noise of the front-end without chopper is $1.6\mu\text{V}_{rms}$ while the proposed chopper front-end provides an integrated input referred noise of $0.75\mu\text{V}_{rms}$ with the noise floor below 50 $\text{nV}/\sqrt{\text{Hz}}$.

Employing a SC-CMFB and a subthreshold-source-follower biquad as a low-pass filter has allowed to achieve a total harmonic distortion below 0.5% for a input signal of 1mV_{pp} (see Fig. 5) without increasing power consumption. The total power consumption of the amplifier is $1.89\mu W$ which translates in a noise efficiency factor (NEF) of 2.7 over a bandwidth from 1 to 200Hz. Consequently, the resulting power efficency factor (PEF) is one of the lowest reported (7.7).

Fig. 6 shows the transfer function of the circuit for different setting parameters. With the proposed tuning method of low-pass and high-pass poles, we achieved a range of 0.4-3 Hz in the high-pass and 60-500 Hz in the low-pass. Both cut-off frequencies are set by capacitor banks. This tunability allows us to deal with the variations due to mismatch, corners, temperature, etc; and, in addition, to implement a selective

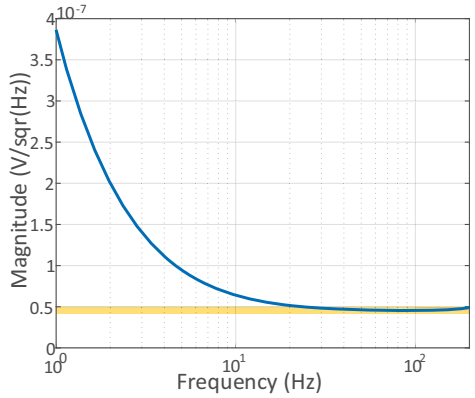

Fig. 4. Input referred noise of the proposed front-end.

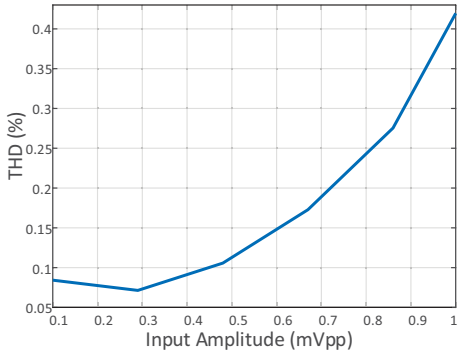

Fig. 5. Total harmonic distortion of the proposed front-end.

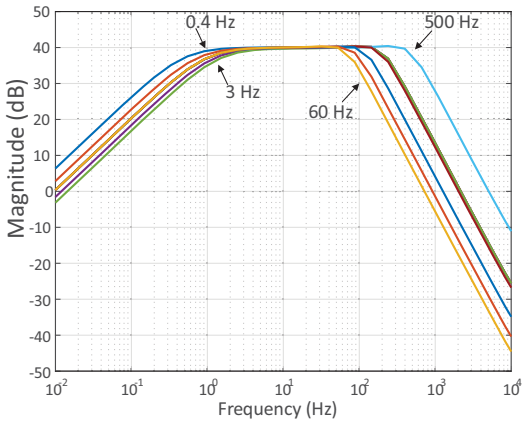

Fig. 6. Transfer function of the proposed circuit with pole tuning.

filter. A maximum input offset of $\pm 50mV$ is largely reduced by the DCSL. The output residual offset is less than $\pm 500\mu V$.

Summarizing, the most relevant specifications of the proposed front-end, is compared with other ECoG neural recording reported front-ends in Table I. It is worth to notice that we are comparing fabricated front-ends with post-layout simulations.

TABLE I
COMPARATIVE WITH OTHER NEURAL FRONT-END FOR ECOG RECORDING.

	Smith 2016 [9]	Karimi 2017 [11]	Muller 2015 [4]	**This Work**
Technology (μm)	0.065	0.18	0.065	**0.18**
Supply Voltage (V)	1.0	0.6	0.5	**1.0**
Power (μW)	1.08	0.69	2.3	**1.89**
IRN	112 nV/$\sqrt{Hz}$ (Spot Noise)	2.3 μV_{rms} (2 - 175Hz)	1.2 μV_{rms} (1 - 500Hz)	**0.75 μV_{rms} (1-200Hz) 50 nV/$\sqrt{Hz}$ (Spot Noise)**
THD @ mVpp	<1% (4)	<1% (0.2)	<0.4% (1)	**<0.5% (1)**
NEF	4.52 (Spot)	7.22 (2 - 175Hz)	4.76 (1 - 500Hz)	**2.77 (1-200Hz)**
PEF	20.43 (Spot)	31.3 (2 - 175Hz)	11.3 (1 - 500Hz)	**7.7 (1-200Hz)**

IV. CONCLUSION

Low-noise and low-power analog circuits will continuously open new outlooks for bioelectronics. This work has been focused on the design of a front-end which is is specially intended to sense very low-amplitude and low-bandwidth signals from ECoG.

The design strategy relies on several considerations and techniques to reach the lowest achievable noise level without significantly increasing power consumption. These methods have been focused on the implementation of a chopper architecture. Herein, a nW-class low-pass filter has been implemented with a subthreshold-source-follower structure. This architecture significantly reduces the power consumption, noise contribution and increases the linearity of the filtering stage. This filter also avoids the need for a noisy ripple rejection loop. This design methodology has resulted in a front-end which minimizes noise and power consumption, showing one of the lowest reported noise floor and PEF.

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