A 16 Rules@2.5Mflips Mixed-Signal Programmable Fuzzy Controller CMOS-1μm Chip

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ABSTRACT: We present a fuzzy inference chip capable to evaluate 16 programmable rules at a speed of 2.5Mflips (2.5×10^6 fuzzy inferences per second) with 8.6mW power consumption. It occupies 2.89mm^2 (including pads) in a CMOS 1μm single-poly technology. Measurements are given to demonstrate its performance. All the operations needed for fuzzy inference are realized on-chip using analog circuitry compatible with standard VLSI CMOS technologies. On-chip digital control and memory circuitry is also incorporated for programmability. The chip architecture and circuitry are based on our design methodology for neuro-fuzzy systems reported in [1]. A few architectural modifications are made to share circuitry among rules and, thus, obtain reduced area and power consumption. The chip parameters can be learned in situ, for operation in a changing environment, by using dedicated hardware-compatible learning algorithms [1][8].

1. Introduction

Fuzzy controllers employ fuzzy logic inference to model systems whose mathematical description is unknown, based on insights about local features of their behavior [2]. These models consist of nonlinear multidimensional functions (called *response surfaces*) which map inputs into outputs. For implementation purposes these maps are represented as expansions of fuzzy *basis functions*, one per each local piece of knowledge from which the global model is built. These local pieces of knowledge are expressed by mean of logic IF-THEN rules,

IF x_1 is A_{i1} **AND** x_2 is A_{i2} **AND** ... x_M is A_{iM} **THEN** *Consequent* Action

One appealing feature of fuzzy modeling is that the statements in these rules can be formulated in natural language; such as, "if the pole is falling rapidly to the left then the cart must move rapidly to the left", which simplifies capturing human expertise. Also, the locality of the pieces of knowledge, the basis on which the global surface response is built, enables simpler model updating for changes that affect only limited regions of the input space.

Fuzzy technology has proven viable for incorporation into new products within short development time and with low development cost which, together with its functionality potential, render it very well suited to build marketable intelligent systems [3]. In this scenario, dedicated hardware implementations based on analog parallel processing feature high-speed inference, reduced power consumption and simple interface to physical sensors and actuators [2].

The CMOS chip presented here is based on our design methodology for neuro-fuzzy ASICs, reported in [1]. Other CMOS monolithic analog fuzzy chips have been reported in [4][5][6][7]. [4] employs switched-capacitor circuits to obtain 0.5MFlips. The other three realize 9rules@2input@1output using continuous-time circuits. The fastest claims 10MFlip@10mW, and have very limited programmability and no internal logic [5]. [6] obtains 0.1MFlip, and gives no data about power; [7] obtains 1.6MFlips@3.1mW, again with limited programmability and no internal logic.

2. Chip Description: Architecture and Building Blocks

The chip realizes the particular case of fuzzy inference that uses constant terms (*singletons*) at the consequent of each rule [1].This procedure obtains $y = f(\mathbf{x})$ as,

$$y(x) = \sum_{i=1,5} w_i^*(x)\, y_i^*, \qquad w_i^*(\mathbf{x}) = \frac{min\{s_{i1}(x_1), s_{i2}(x_2), ..., s_{iM}(x_M)\}}{\sum_{i=1.N} min\{s_{i1}(x_1), s_{i2}(x_2), ..., s_{iM}(x_M)\}} \tag{1}$$

where $w_i^*(\mathbf{x})$ are the normalized fuzzy basis functions which corresponds to normalized rule antecedent outputs, $s_{ij}(x_j)$ are the membership functions associated to linguistic labels A_{ij}, and y_i^* are the singleton values at the consequent of each rule. Fig. 1 is a conceptual architecture to realize (1). There, processing is realized through five layers associated to the operators in (1)

Instead of a direct translation of Fig. 1 into silicon, circuitry in the reported chip is distributed to achieve high modularity. Thus, minimum and normalization circuits have been split into cells, which are further grouped into two blocks named *label block* and *rule block* in the chip architecture depicted in Fig. 2. On the other hand, membership functions are shared among different rules. Thus, there is only one membership function for each label in the rule set, and there is only a set of labels per input. Consequently:

- Membership function circuits do not need to be replicated at each rule, thus we save area and power consumption.
- We can generate only grid partitions of the universe of discourse, that is, the partition in each separate dimension or input determine the partition in the overall multidimensional input space. Therefore, scatter and tree partitions [8] are not allowed.

Although chip input and output signals are voltages, much of the internal processing is realized in current mode. Membership functions are generated from sigmoid outputs of two cross-coupled differential pairs, and complemented in order to use a multiple output maximum circuit to realize minimum in (1) through maximum plus complement operations, based on De Morgan's law [1]. At the circuit level, the sharing of the membership functions requires to replicate the complemented membership function circuit output by mean of a multiple output current mirror. This is shown in Fig.3, which depicts a basic schematic of the *label block*, where shaded areas corresponds to the input cells of the multi-input maximum circuit [1]. The input of the label block is one of the chip voltage inputs, and it provides four voltages as outputs. Since it implements shared membership functions, there is one label block for each label in the rule set. The chip contains eight label blocks, four per input.

The label blocks outputs are connected to inputs of the rule blocks through a ring bus. There is one rule block for each rule in the knowledge base, sixteen in our chip. Besides of illustrating the input space partition achieved by the chip, Fig. 4 shows the conceptual connection between both building blocks, while Fig. 5 shows the schematic of a *rule block*. Two voltage outputs

from two different label blocks are connected to the input of a rule block, whose input stage is the output stage of the minimum circuit. The output of the minimum circuit drives the normalization circuit unit cell [1]. Besides the unit cells, which share nodes A_{nor} and B_{nor} in Fig. 5, the normalization circuit is completed with one diode connected transistor at node A_{nor}, and one current mirror whose output is connected to node B_{nor} and replicates a constant current source -- both implemented in the *biasing box* of Fig.2. The normalization circuit output in each rule block is weighted by a digitally programmable current mirror, thus performing singleton weighting at the consequent of each rule [1]. Finally, the output of this current mirror is connected to the chip global output, where aggregation at fifth layer of Fig. 1 is realized by KCL.

The digital singleton programming codes are stored in a shift register which is the chip internal memory element -- serially programmed through two pads. Apart from the digital programmability of singletons, the width and location of membership functions are analog-programmable by setting the two voltages E_{j1} and E_{j2} associated to membership value of 0.5 (*crossover points*) in the membership function circuit related to each label (see Fig. 3). Finally, bias signals are mainly generated internally and shared by different blocks. They are implemented in the *biasing box* together with the shared parts of normalization circuit.

3. Experimental Results

Fig.6 is a microphotograph of the chip; total area is 2.89mm^2, and core area is 1.6mm^2. The figures Fig. 7(a) and Fig. 7(b) show two response surfaces generated by the chip. Singletons are set to decimal values 1 and 15 in Fig. 7(b), where the basis functions are clearly seen. Fig. 7(a) illustrates an exemplary surface obtained with different singleton values. Maximum circuit delay is 471ns (90% of the full scale output current) for a step input, while power consumption is 8.6mW and resolution is around 6.5% for 3σ (standard deviation) error figure. Supply voltage is 5V and the input voltage range is 3.25V.

As a final point, it is worth mentioning that we have developed hardware-compatible *learning* algorithms that enable the chip to be trained in-situ through examples and, thus, compensate second-order hardware non-linearities [8]. Thus, higher precision can be achieved by inserting the chip in a learning loop with a computer.

References

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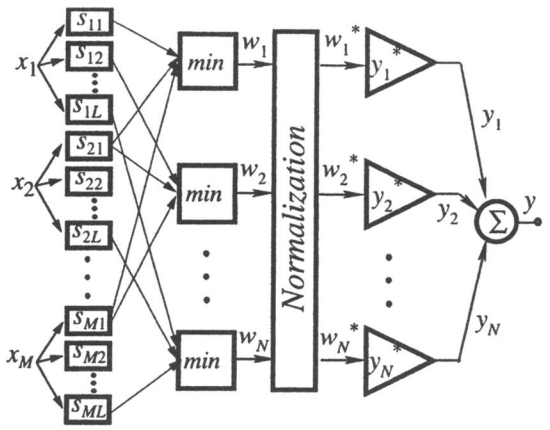

Figure 1

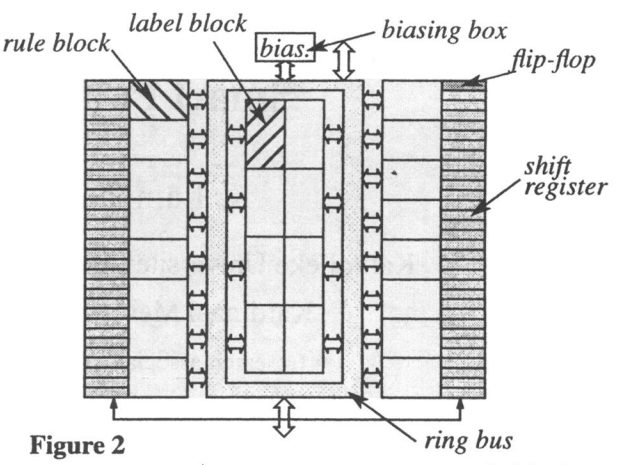

Figure 2

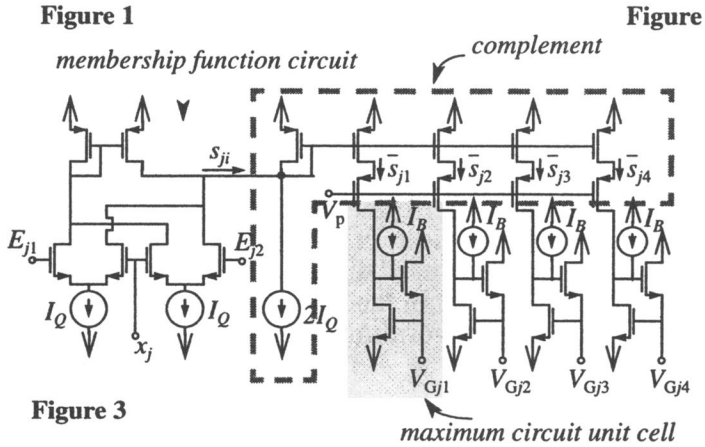

Figure 3

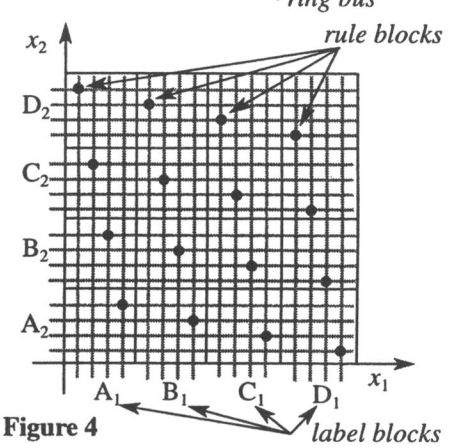

Figure 4

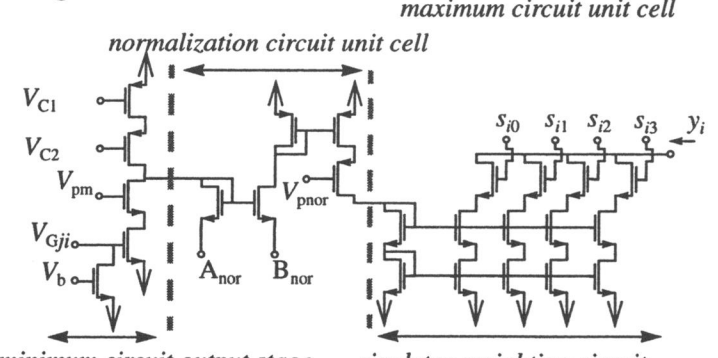

Figure 5

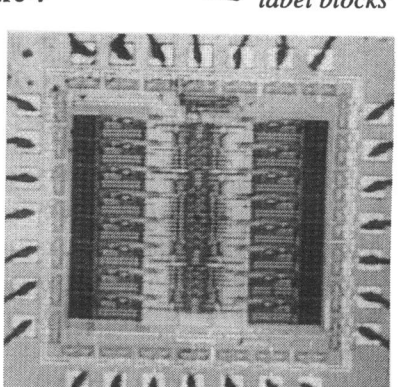

Figure 6

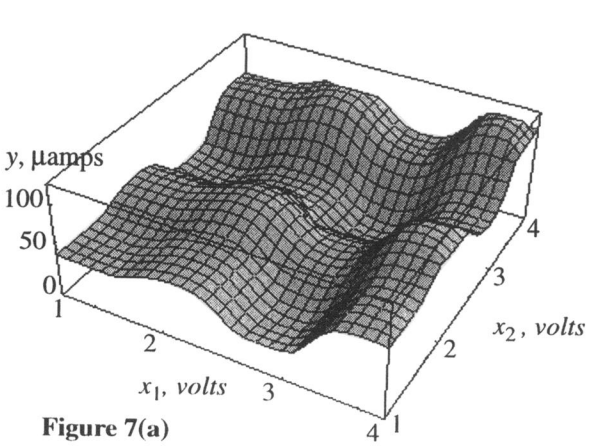

Figure 7(a)

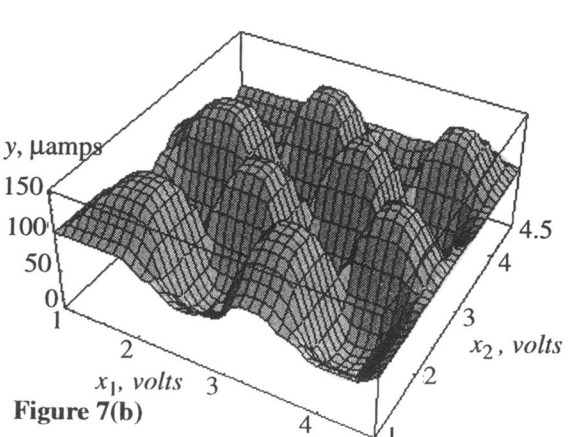

Figure 7(b)