A CMOS 0.18µm 64×64 Single Photon Image Sensor with In-Pixel 11b Time-to-Digital Converter

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***Abstract* - The design and characterization of a CMOS 64×64 single-photon avalanche-diode (SPAD) array with in-pixel 11b time-to-digital converter (TDC) is presented. It is targeted for time-resolved imaging, in particular 3D imaging. The achieved pixel pitch is 64µm with a fill factor of 3.5%. The chip was fabricated in a 0.18µm standard CMOS technology and implements a double functionality: Time-of-Flight estimation and photon counting. The imager features a programmable time resolution for the array of TDCs from 625ps down to 145ps. The measured accuracy of the minimum time bin is lower than ±1LSB DNL and 1.7LSB INL. The TDC jitter over the full dynamic range is less than 1LSB. Die-to-die process variation and temperature are discarded by auto-calibration. Fast quenching/restore circuit on each pixel lowers the power consumption by limiting the avalanche currents. Time gated-operation is possible as well.**

I. INTRODUCTION

Over the different approaches to estimate the depth map of scenes, the use of Single-Photon Avalanche Diodes (SPAD) emerges as a feasible alternative for applications involving low light conditions [1]. Fig. 1 shows a typical arrangement for depth map estimation using SPADs by sensing a pulsed-modulated light. Besides night vision applications, requiring a very high sensitivity, these SPAD-based systems find applications for complex imaging tasks such as looking around corners [2]. Human face reconstruction is also possible even with 115ps time resolution [1]. 3D vision is also used in medical imaging like positron emission tomography (PET) [3] and in other biomedical techniques dealing with a faint light source, like fluorescence lifetime imaging (FLIM) which requires a time bin below 100ps [4].

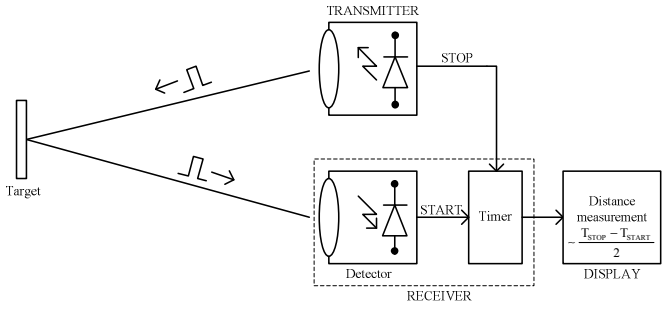

Figure 1. Principle of the ToF measurement based on pulsed modulation

The chip in this paper is oriented towards 3-D imaging for object reconstruction. The goal is to achieve the best possible performance using a standard CMOS process. The imager is also able to capture 2-D images and can be used as 64 channels time-to-digital converter. Moreover it is self-calibrated against uniform temperature variation.

Using a compact pseudo-differential voltage-controlled ring-oscillator, the in-pixel TDC area is of 1740µm^2 which is smaller than the state-of-the-art [4], [5], [7]. The normalized power consumption per TDC is of 9µW to convert a time interval of 10ns at 500fps, which is three times smaller than the one reported in [5]. Moreover we have achieved better time resolution for a smaller amount of power (see Table. I). The standard deviation of TDCs uniformity across the array is about 19 codes. This figure is evaluated without applying any pixel-to-pixel calibration. The FWHM jitter of the TDC is 133ps (or 0.92LSB). The last two measurements have been performed at 90% of the full dynamic range (or 270ns).

II. ARCHITECTURE OF THE 3D IMAGE SENSOR

The proposed design occupies an area of 5×5mm^2, including the pad ring. It incorporates an array of 64×64 2D/3D smart pixels, analog I/O buffers, fast signal distribution trees, row decoder, fast data serialiser and a programmable phase locked-loop (PLL). The block diagram of the chip is shown in Fig. 2.

The sensor array fits in less than 4.1×4.1mm^2. Analog buffers are needed to drive the voltage reference for each in-pixel ring oscillator. It is provided by the on-chip PLL. Thereby it overcomes the effects of uniform process variation and temperature [5]. Moreover analog input buffers are required to uniformly distribute the control signal for the dead time of the SPADs. Fast signal distribution network is needed to share the same START and STOP signal for the array of TDCs. In addition to that, a rolling-shutter activation strategy is applied for the converters array to decrease the overall power consumption.

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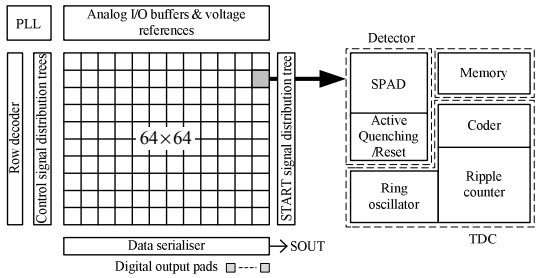

Figure 2. Block diagram of the chip

A row decoder is implemented to read the imager line by line. Notice that for this kind of sensors the most appropriate scheme is a serial input parallel output shift register. This scheme is faster, more compact than the regular decoder based on logic gates and overcomes pulse overlapping. The programmable PLL enables adjustable time resolution.

A. Functionality

The imager can be configured to work either in test, 3D or 2D mode. In test mode, TDCs can be independently measured. An external start/stop signals must be provided to the converters array by a time interval generator. This is implemented on a VIRTEX5 FPGA and has a time resolution of 27ps. The jitter of the TDC, τ_{TDC}, is estimated by $\sqrt{\tau_T^2-\tau_{START}^2-\tau_{STOP}^2}$, where τ_T is the total jitter, τ_{START} and τ_{STOP} are the jitter of the START and STOP signals. Special care needs to be put in the routing of START and STOP signals. They should be shielded and symmetrically loaded by the parasitic capacitances. Moreover they need to uniformly drive the different rows of the array, therefore a skew-less distribution scheme has been designed.

In the 3D-mode each pixel measures the time elapsed from the actual detection to the next stop pulse of the synchronization signal. In this way the depth map of the target can be inferred considering that $2T_{ToF} = T_{laser} - T_{measured}$ (see Fig. 3, 10).

The 2D-mode stands for the acquisition of the illumination map of a scene. It is done by connecting the output of the SPAD to the ripple counter of the TDC. The amount of photons impinging on one single SPAD is estimated by merely counting pulses. At the end of the integration time the number of the pulses provided by each SPAD is proportional to the intensity of the light falling on that particular photodiode. At this point VCRO is disabled. The imager requires very little power.

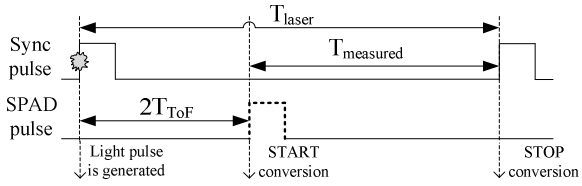

Figure 3. Reverse start-stop scheme diagram

B. Imager design

Each pixel of the array is composed by the single-photon detector, TDC, memory block and tri-state output buffers. The block diagram of the pixel is presented in Fig. 4. Basically the first block is the SPAD sensor controlled by an active quenching/ reset circuit (AQR) able to perform time-gated operation (see Fig. 6).

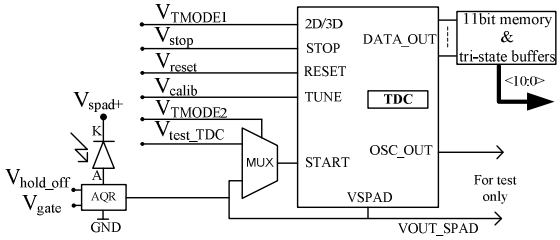

Figure 4. Block diagram of 2D/ 3D pixel

In order to build high-resolution single-photon image sensors, the area and power consumption per pixel are the most important constraints. The pixel pitch is 64µm. The main contribution to power consumption at the pixel level is the operation of the VCRO when running at maximum frequency. The average power consumption at full range and 5kfps is 2.7µW per TDC. Pixel layout is depicted in Fig. 5.

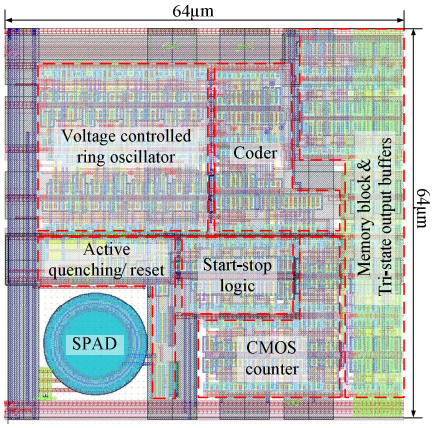

Figure 5. Pixel layout

The time-stamp digitized by the TDC is stored inside each pixel to allow offline readout at a lower speed. Tri-state buffers are controlled by a row decoder such that each row is successively connected to data serialiser.

1) Single photon detector ensemble: It is built by a SPAD and an active quenching/reset circuit (AQR). The active area of the quasi-circular SPAD has a diameter of 12µm and it has been demonstrated in a previous work [6]. In addition to that, transistors M_4 and M_5 are added to perform time-gated operations. If V_{gate} is tied to VDD then the detector is enabled for proper operation: when an event is detected the avalanche

current flows through $M_{1,2}$ and the voltage of the anode A and V_{out} go up. V_{sense} goes down and switches on transistors $M_{3,8}$. The current spike is quenched by pulling up the anode terminal. Notice that the quenching phase is speed up by the positive feedback created by M_3.

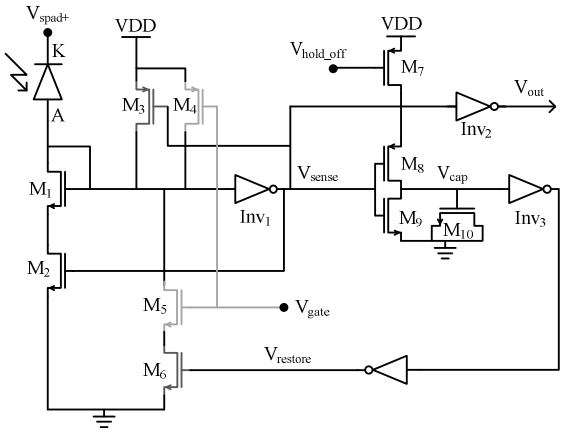

Figure 6. Proposed time-gated active quenching/reset (AQR) circuitry

In the meantime, the MOS capacitor M_{10} is charging. When V_{cap} reaches the trip-point of Inv_3 then M_6 is turned on. The anode is pulled down through $M_{5,6}$ and the SPAD junction is turned on again ready to detect new incoming photons.

If V_{gate} is tied to ground then the detector is disabled through the transistor M_4. Furthermore V_{out} and $V_{restore}$ are VDD, switching on M_6. When V_{gate} is set to VDD to enable the SPAD then M_5 turns on which automatically restore the detector through the transistors $M_{5,6}$. It is worth to mention that the SPAD will not pass through the restoring point if the time-gate is smaller than the dead-time. The latter parameter can be adjusted by the voltage $V_{hold\text{-}off}$.

The detector output V_{out} is either connected to the TDC for ToF measurements or to an 8b counter to evaluate light intensity by photon counting.

2) Pixel level TDC: In order to perform ToF measurements each pixel incorporates a low power TDC that works following a reversed start-stop scheme. Another possibility to improve the time bin by applying interpolation is to incorporate a delay line in-pixel [7]. Notice that this architecture is not completely scalable since a relatively high clock reference of 280Mhz has to be uniformly distributed across the array.

The proposed TDC is composed by a voltage-controlled ring oscillator (VCRO), an encoder and a ripple counter. A pseudo-differential ring oscillator is employed [8]. Additional control of the oscillation frequency has been incorporated. The TDC occupies $29\times28\mu m^2$. The best time bin, T_{bin} of 145ps is achieved by interpolating eight phases. The block diagram of the TDC is depicted in Fig. 7.

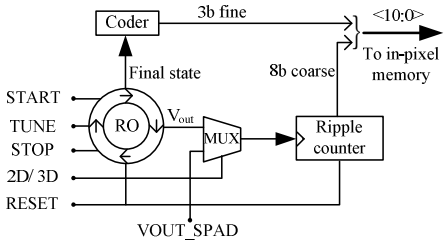

Figure 7. TDC schematic

The 8b ripple counter realizes a coarse conversion by counting the number of full oscillation periods. The thermometric encoder provides the least significant 3b from the combination of the phases of the ring oscillator.

The accuracy of a single TDC is measured as less than ±1LSB DNL and 1.7LSB INL. Additional glue logic has been incorporated to handle particular issues such as start-stop pulse overlapping, no appearance of a start pulse and variable width of the start pulse coming from the SPAD.

III. MEASUREMENTS RESULTS

This work reports measurements results on the TDC time accuracy (Fig. 8) and jitter, code uniformity across the array (Fig. 9) and waveforms of the time-gated operation (Fig. 10). The imager is controlled by a VIRTEX5-FPGA.

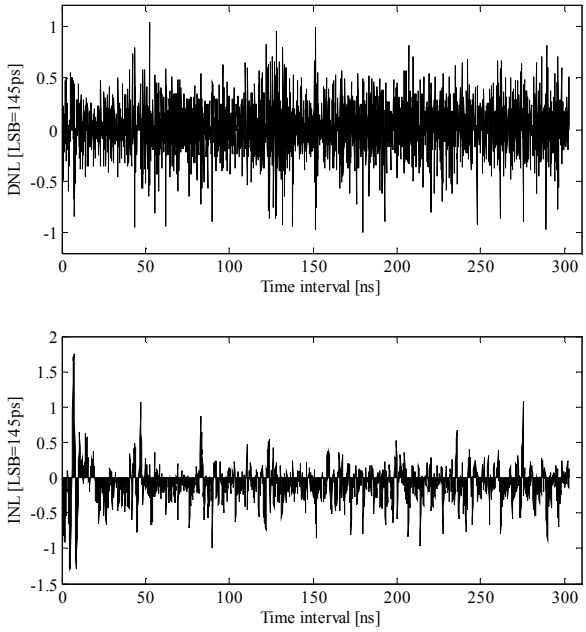

Figure 8. TDC DNL/INL less than ±1LSB/ 1.7LSB

The TDCs uniformity is evaluated converting a time interval of 270ns. It represents 90% of the full dynamic range. The standard deviation across the array is about 19 codes.

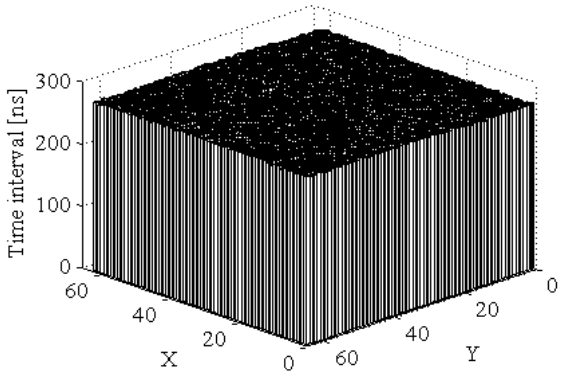

Figure 9. TDC array code uniformity

The proper functionality of the time-gated setup is depicted in Fig. 10. The imager is enabled on the lower level of TGATE signal. In this case the START signal is provided by the SPAD detector of the pixel (64, 64). The local TDC is switched on by the fist photon detection. The conversion stops on the negative edge of the synchronization signal, STOP. The time window that needs to be resolved is about 280ns (see signal TINT). The third analog channel depicts the output of the VCO divided by 64. At the end of the conversion time, the result is stored by the in-pixel memory. Each frame is read out through a single ended fast IO buffer (SOUT) for off-line data processing.

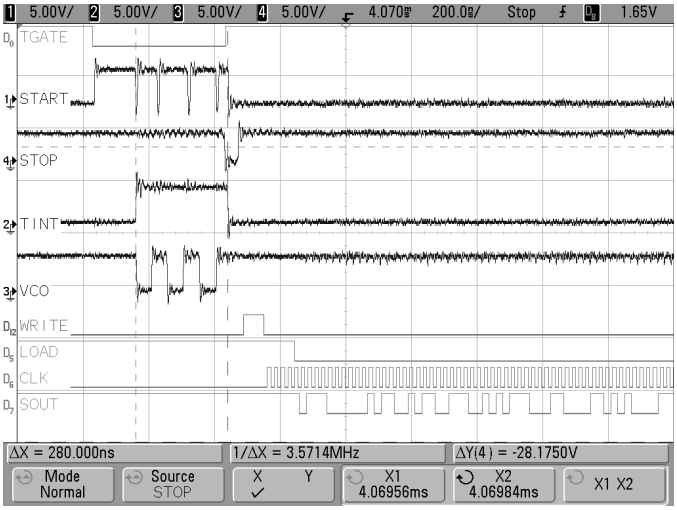

Figure 10. Signal waveforms in3D mode operation

The test mode is implicitly proved by the 3D mode whilst the only difference is that the START signal is globally generated externally, instead by each in-pixel SPAD detector.

The 2D mode uses only a part of the 3D mode architecture. Consequently the proper functionality of the 2D mode is already present in the previous measurements.

TABLE I. COMPARISON WITH STATE-OF-THE ART 3D IMAGERS

Performances	**[2]**	**[4]**	**[5]**	**This work**
Technology	HV 0.8µm	0.13µm	0.13µm	0.18µm
Format	32×32	32×32	32×32	**64×64**
Pitch/ Fill factor	58µm/ 1.1%	50µm/-	50µm/ -	**64µm/ 3.5%**
T_{bin}/ N_{bits}/ Range	115 ps/ - / 3m	119ps/ 10bit/ 15m	52,178p/ 10bits/ -	145ps/ 11bit/ **44-192m**
Dead time	<40ns	-	-	**4ns – 500ns**
TDC area			2200µm^2	**1740**µm^2
TDC avg. power	-	-	38µW[1]	**~9µW[1]**

[1]This power has been evaluated for 10ns conversion time interval and 500kfps.

IV. CONCLUSION

A 64 × 64 3-D imager based on SPADs was designed and fabricated in 0.18µm standard CMOS process. The pixel pitch is 64µm and incorporates the SPAD detector, very fast AQR with adjustable dead-time down to 4ns, low power TDC and 11b memory. The finest time resolution is about 145ps at 9µW normalized power consumption[1] per TDC which is three times smaller than [5].

ACKNOWLEDGEMENTS

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