Continuous-Time Cascaded ΣΔ Modulators for VDSL: A Comparative Study

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ABSTRACT

This paper describes new cascaded continuous-time ΣΔ modulators intended to cope with very high-rate digital subscriber line specifications, i.e 12-bit resolution within a 20-MHz signal bandwidth. These modulators have been synthesized using a new methodology that is based on the direct synthesis of the whole cascaded architecture in the continuous-time domain instead of using a discrete-to-continuous time transformation as has been done in previous approaches. This method allows to place the zeroes/poles of the loop-filter transfer function in an optimal way and to reduce the number of analog components, namely: transconductors and/or amplifiers, resistors, capacitors and digital-to-analog converters. This leads to more efficient topologies in terms of circuitry complexity, power consumption and robustness with respect to circuit non-idealities. A comparison study of the synthesized architectures is done considering their sensitivity to most critical circuit error mechanisms. Time-domain behavioral simulations are shown to validate the presented approach.

Keywords: Analog-to-digital converters, sigma-delta modulators, continuous-time circuits.

1. INTRODUCTION

Continuous-Time (CT) Sigma-Delta Modulators (ΣΔMs) have demonstrated to be an attractive solution for the implementation of Analog-to-Digital (A/D) interfaces in systems-on-chip integrated in deep-submicron standard CMOS technologies [1]. Although most reported ΣΔMs have been implemented using Discrete-Time (DT) circuits, the increasing demand for broadband data communication systems has motivated the use of CT circuit techniques. In addition to show an intrinsic antialiasing filtering, CT ΣΔMs provide potentially faster operation with lower power consumption than their DT counterparts [2,3].

In spite of their mentioned advantages, CT ΣΔMs are more sensitive than DT ΣΔMs to some circuit errors, namely: clock jitter, excess loop delay and technology parameter variations [2,3]. The latter are specially critical for the realization of cascaded architectures. This has forced the use of single-loop topologies in most reported silicon prototypes even thought low oversampling ratios (< 12) are needed [4,5], whereas very few cascaded CT ΣΔM Integrated Circuits (ICs) have been reported [6].

However, the need to achieve medium-high resolutions (> 12bits) within high signal bandwidths (> 20MHz) while guaranteeing stability, has prompted the interest in proper methods for the synthesis of high-order cascaded CT ΣΔMs [7-9]. These methods are based on applying a DT-to-CT transformation to an equivalent DT topology that fulfils the required specifications. In most cases, the use of such a transformation is normally translated into an increase of the analog circuit complexity with the subsequent penalty in silicon area, power consumption and sensitivity to parameter tolerances.

This paper presents a direct synthesis method of cascaded CT ΣΔMs which, dispensing with the DT-to-CT equivalence, make it possible to reduce the analog circuitry complexity and place the zeroes/poles of the quantization noise transfer function in an optimal way, thus yielding to more robust architectures than using a DT-to-CT transformation. As an application, the proposed methodology is used to find optimum CT ΣΔMs for Very high-rate Digital Subscriber Line (VDSL). Three fifth-order cascaded topologies are synthesized: 2-1-1-1, 2-2 and 3-2. These modulators are designed for 12-bit@20-MHz specifications and their performances are compared in terms of time-domain simulations that take into account critical error mechanisms like mismatch and clock jitter error.

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2. CASCADED CONTINUOUS-TIME ΣΔ MODULATORS

Fig.1 shows the conceptual block diagram of a m-stage cascaded CT ΣΔM. Each stage, consisting of a single-quantizer CT ΣΔM, re-modulates a signal containing the quantization error generated in the previous stage. Once in the digital domain, the outputs, y_i, of the stages are properly processed and combined (by the cancellation logic) in order to cancel out the quantization errors of all the stages, but the last one in the cascade. This latter error appears at the overall modulator output shaped by a function of order equal to the summation of the orders of all the stages.

Cascaded CT ΣΔMs are normally synthesized from equivalent (well-known) DT systems and use the same digital cancellation logic [8]. This DT/CT equivalence can be guaranteed because the overall open loop transfer function of each stage in Fig.1 is in fact a DT system [2]. Thus, in the case of a rectangular impulsive response of the Digital-to-Analog Converter (DAC), it can be shown that the equivalent DT loop filter transfer function is given by [10,11]:

$$F(z) = \sum_{p_i} \mathrm{Re}\left(\frac{F(s)}{s} \cdot \frac{e^{m_1 T_S \cdot s}}{z - e^{T_S \cdot s}} \right) - \sum_{p_i} \mathrm{Re}\left(\frac{F(s)}{s} \cdot \frac{e^{m_2 T_S \cdot s}}{z - e^{T_S \cdot s}} \right) \tag{1}$$

where $f_s = 1/T_s$ is the sampling frequency; $m_1 = 1 - t_d/T_s$; $m_2 = 1 - (t_d + \tau)/T_s$; t_d and τ are respectively the time delay and pulse width of the DAC waveform; p_i are the poles of $F(s)/s$ and $\mathrm{Re}(x)$ stands for the residue of x.

In order to get a functional CT ΣΔM while keeping the cancellation logic of the original DT ΣΔM, every state variable and DAC output must be connected to the integrator input of later stages [8]. This increases the number of analog components, i.e transconductors, amplifiers and DACs. As an illustration, Fig.2(a) shows a cascaded 2-1-1 CT ΣΔM obtained from an existing DT ΣΔM [12]. Note that at least eight scaling coefficients (k_{g2-9}) and their corresponding signal paths are needed to connect the different stages of the modulator. The number of integrating paths can be reduced – as shown in Fig.2(b) – if the whole cascaded ΣΔM is directly synthesized in the CT domain as proposed in the next section.

3. PROPOSED SYNTHESIS METHODOLOGY

The idea of dispensing with the DT-to-CT transformation was previously reported in [3] for single-loop architectures. However, in the case of cascaded architectures, the cancellation logic functions (not present in single-loop ΣΔMs) must be included in the synthesis procedure to get an optimum architecture.

Let us consider the more general case of the m-stage cascaded CT ΣΔM shown in Fig.1. The overall output, y_o, is given by:

$$y_o(z) = \sum_{k=1}^{m} y_k(z) CL_k(z) \tag{2}$$

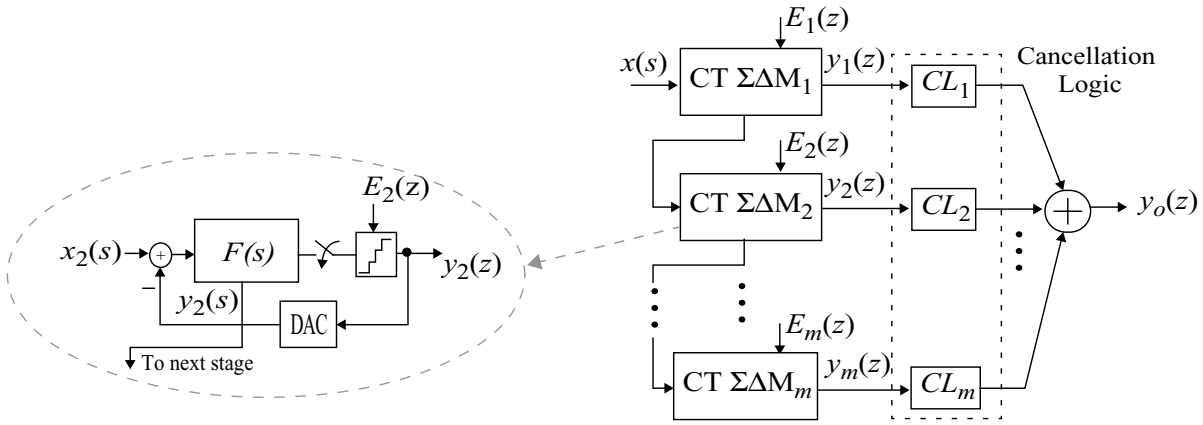


Figure 1. Conceptual block diagram of a cascaded CT ΣΔM.

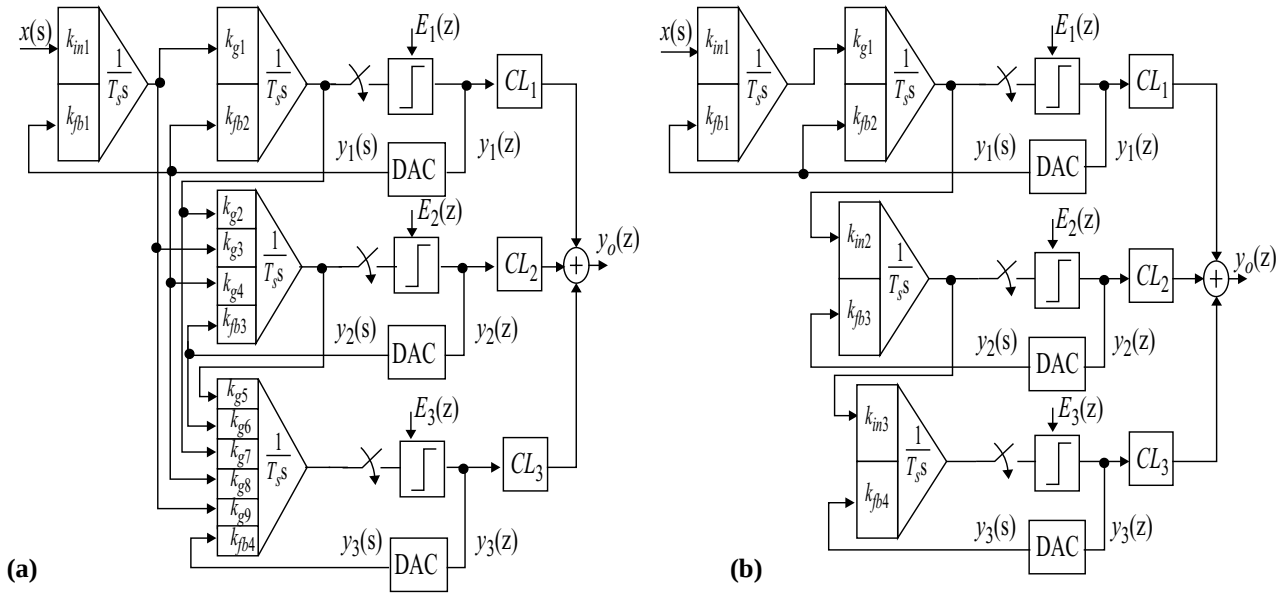


Figure 2. Cascaded 2-1-1 CT ΣΔM architecture obtained (a) from an equivalent DT ΣΔM (b) using the proposed method.

where $y_k(z)$ and $CL_k(z)$ represent respectively the output and partial cancellation logic transfer function of the k-th stage.

If the modulator input, $x(t)$, is set to zero, the output of each stage can be written as:

$$y_k(z) = \frac{E_k(z) + \sum_{i=1}^{k-1} Z\left\{L^{-1}[H_D F_{ik}]\big|_{nT_s}\right\} y_i(z)}{1 - Z\left\{L^{-1}[H_D F_{kk}]\big|_{nT_s}\right\}} \tag{3}$$

where Z stands for the Z-transform, L^{-1} is the inverse Laplace transform, $H_D \equiv H_{DAC}(s)$ is the transfer function of the DAC, and

$$F_{ij} \equiv F_{ij}(s) = \frac{\text{Input Quantizer j}}{y_i(s)} \tag{4}$$

represents the transfer function from $y_i(s)$ to the input of j-th quantizer.

Using the following notation

$$Z_{km} \equiv Z\left(L^{-1}(H_D F_{km})\big|_{nT_s}\right) \tag{5}$$

the output of each stage is given by:

$$y_k(z) = \frac{E_k(z)}{1 - Z_{kk}} + \sum_{i=1}^{k-1} \frac{Z_{ik} y_i(z)}{1 - Z_{kk}} \tag{6}$$

and the output of the modulator can be written as:

$$y_o = \sum_{k=1}^{m} y_k CL_k = \sum_{k=1}^{m} \left(\frac{E_k}{1 - Z_{kk}} + \frac{1}{1 - Z_{kk}} \sum_{i=1}^{k-1} Z_{ik} y_i \right) CL_k \tag{7}$$

The partial cancellation logic transfer functions (CL_k) can be calculated by imposing the cancellation of the transfer function of the first $m-1$ quantization errors $E_k(z)$ in (7). This gives:

$$CL_k(z) = \frac{-Z_{km}CL_m}{1-Z_{mm}} = \frac{-Z\left\{L^{-1}[H_D F_{km}]\big|_{nT_s}\right\}CL_m(z)}{1-Z\left\{L^{-1}[H_D F_{mm}]\big|_{nT_s}\right\}} \tag{8}$$

where the partial cancellation logic transfer function of the last stage, $CL_m(z)$, can be chosen to be the simplest form that preserves the required noise shaping.

Note that the design equations (2)-(8) do not only take into account the single-stage loop filter transfer functions (F_{ii}), but also the inter-stage loop filter transfer functions (F_{ij}, $i \neq j$). The latter are continuous-time integrating paths appearing only when the modulator stages are connected to form the cascaded ΣΔM and must be included in the synthesis methodology to obtain a functional modulator with minimum number of inter-stage paths.

Therefore, the following procedure can be used in a systematic methodology for the synthesis of cascaded CT ΣΔMs[††]:

- First, the poles of single-stage transfer functions ($F_{ii}(s)$) are optimally placed in the signal bandwidth for given specifications. This process is carried out entirely in the CT domain and no equivalence to an existing DT modulator needs to be imposed.
- Second, once the individual stages are designed and optimized, cancellation logics are calculated using (8).

For illustrative purposes, the 2-1-1 CT ΣΔM of Fig.2(b) was synthesized using (2)-(8) to achieve 16-bit resolution in a 750-kHz bandwidth, with a sampling frequency of 48MHz (oversampling ratio, $M = 32$) [12]. For simplicity, in order to facilitate the comparison of the performance of both modulators in Fig.2, the coefficients of the first stage ($k_{in1}, k_{g1}, k_{fb1}, k_{fb2}$) are taken to be equal in both systems and are obtained from a DT-to-CT transformation of the first stage of a DT ΣΔM in [12]. The rest of coefficients in Fig.2(b) are taken such that the time constant of the integrators is the inverse of the sampling frequency ($T_s = 1/f_s$):

$$\begin{aligned} &k_{in1} = -k_{fb1} = 1/4; \qquad k_{fb2} = -3/8 \\ &k_{g1} = k_{in2} = -k_{fb3} = k_{in3} = -k_{fb4} = 1 \end{aligned} \tag{9}$$

Hence, the single-loop and inter-stage transfer functions are given by:

$$\begin{aligned} F_{11} &= \frac{-\left(\frac{3T_s}{8}s + \frac{1}{4}\right)}{(sT_s)^2} \qquad F_{22} = F_{33} = \frac{-1}{sT_s} \\ F_{13} &= \frac{-\left(\frac{3T_s}{8}s + \frac{1}{4}\right)}{(sT_s)^4} \qquad F_{23} = \frac{-1}{(sT_s)^2} \end{aligned} \tag{10}$$

and the partial cancellation logic transfer functions can be calculated using (8)-(10). Considering a Non-Return-to-Zero (NRZ) DAC, the following cancellation logics are derived:

$$\begin{aligned} CL_1 &= \frac{z^{-1}}{48}(7 + 29z^{-1} - 7z^{-2} - 5z^{-3}) \\ CL_2 &= z^{-1}(1+z^{-1})(1-z^{-1})^2 \\ CL_3 &= 2(1-z^{-1})^3 \end{aligned} \tag{11}$$

[††] In this procedure, the modulator order, oversampling ratio and number of bits of internal quantizers are assumed to be determined for given specifications from well-known expressions [1].

where CL_3 is chosen to have three zeroes at DC, corresponding to the zeroes contributed by the first three integrators.

In order to compare the robustness of both modulators in Fig.2, the effect of mismatch on the Signal-to-Noise Ratio (SNR) was also simulated using SIMSIDES, a SIMULINK-based time-domain behavioral simulator for ΣΔMs [13]. For this purpose, maximum values of mismatch were estimated for a 0.13 μm CMOS technology and both modulators in Fig.2 were simulated considering a Gm-C implementation. The results are shown in Fig.3, where the SNR loss is represented as a function of the standard deviation of the transconductances (σ_{gm}) and capacitances (σ_C). For each point of these surfaces, 150 simulations were carried out using random variations with the standard deviation given in the diagrams. The value of SNR loss represented in Fig.3 stands for the difference between the ideal SNR, i.e with no parameter variation, and the SNR with 90% of the 150 simulations above it. It is shown that the lower analog component count in Fig.2(b) is reflected in a lower variance of the modulator coefficients, leading to a better behavior in terms of sensitivity to mismatch.

4. APPLICATION TO VDSL

As an application of the proposed methodology, three 5th-order cascaded CT ΣΔMs, shown in Fig.4, were synthesized to cope with VDSL specifications: 12-bit resolution within a 20-MHz signal bandwidth. In order to fulfil these specifications without being limited by the clock jitter error, the sampling frequency, f_s, and the number of bits of the internal quantizers (and DACs), B, must be properly chosen. In the case of a 5th-order modulators like those shown in Fig.4, the in-band jitter noise power is minimized for $f_s = 240\text{MHz}$ and $B = 4$ [14].

Another critical source of error in CT ΣΔMs is the excess loop delay. As shown in [15] this error can be compensated by adding an extra feedback branch between the output and the input to the quantizer (DAC_2 in Fig.4) and two D-latches. By adding this extra branch with the appropriate gain, the loop impulse response is exactly the same as that of the original. This extra feedback term can be easily included in the calculation of the cancellation logic. In a practical implementation it could be advantageous to make DAC_2 programmable [5].

Considering the factors above, the CT ΣΔMs in Fig.4 were synthesized using the methodology described in Section 3, taking into account the following considerations:

- The first stage of the 2-1-1-1 architecture (Fig.4(a)) is formed by a resonator which has its poles placed at $\omega_p = 2\pi\sqrt{7/9}B_w$, in order to minimize the quantization Noise Transfer Function (NTF) in the signal bandwidth, B_w. Resistor variations can be tuned out using a combination of a discrete rough tuning of the resistors (R_{in}, R_{fb} and R_r) and a continuous fine tuning of the transconductors k_{ff} and k_{g1}. This tuning can be also used to cancel the effect of finite Gain-Bandwidth product (GB) of the front-end opamp, due to the fact that this error can be modelled as an integrator gain error [5]. All the other transconductors could be tuned in order to keep the time constant C/g_m unchanged over C variations.
- An additional resonator has been used in the 2-2-1 architecture (Fig.4(b)), in order to optimally distribute the poles of NTF [16].

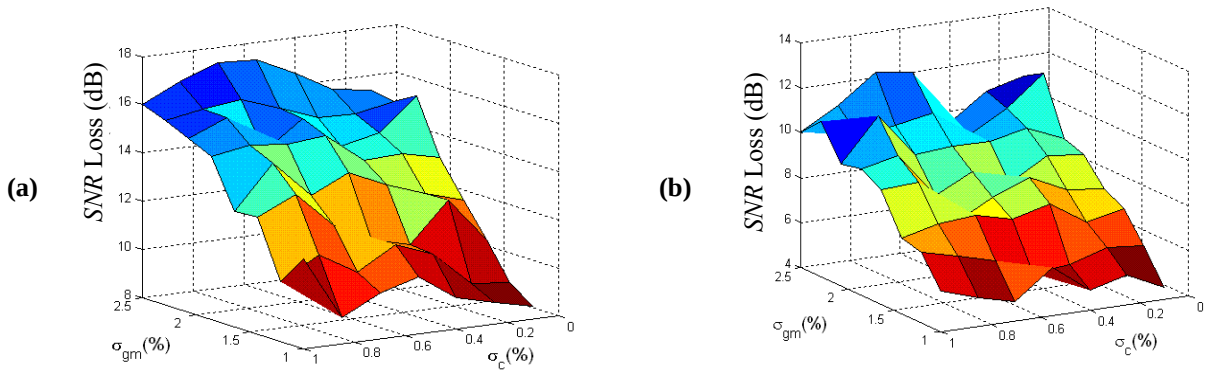


Figure 3. Effect of mismatch on the SNR of a cascaded 2-1-1 CT ΣΔM obtained from: (a) an equivalent DT ΣΔM; (b) proposed method.

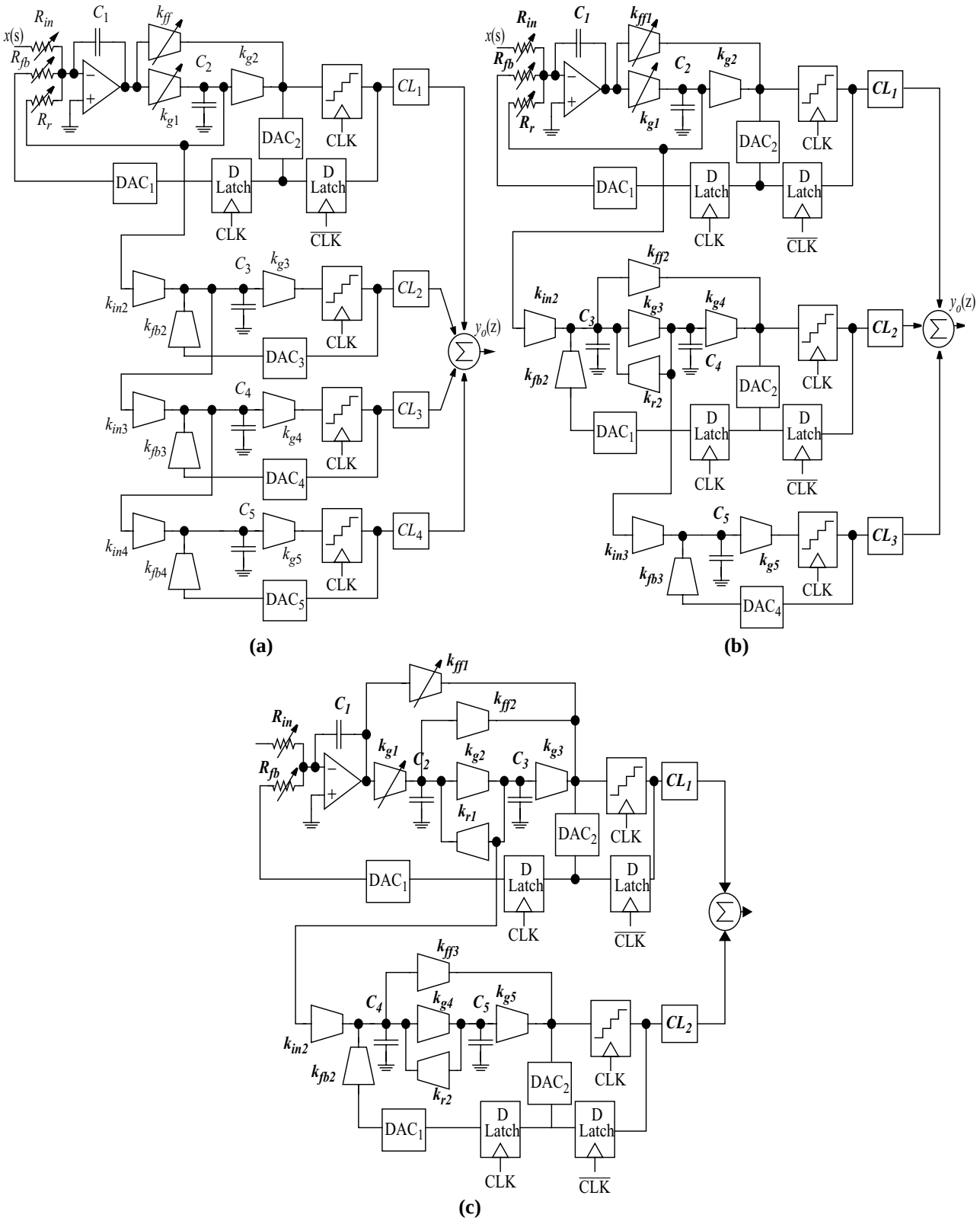


Figure 4. Cascaded CT ΣΔMs synthesized for VDSL: (a) 2-1-1-1; (b) 2-2-1; (c) 3-2.

- The 3-2 modulator shown in Fig.4(c) includes a first stage which consists of an integrator and a resonator. This topology allows the same optimum pole positioning as in the 2-2-1 modulator with one less stage. However, stability problems might arise that compromise the modulator performance.

Table 1 shows the single-loop and inter-stage transfer functions (F_{ij}) for the different architectures in Fig.4 as a function of the loop filter coefficients b_{ij}. The expressions of CL_i, obtained from (8) and (11), are also shown. It is important to note that b_{ij} are found from an iterative simulation-based process that optimizes the first stage of the modulator in order to maximize SNR while keeping stability.

The outcome of the optimization process – entirely done in the CT domain – is summarized in Table 2**.** This table includes the values of loop filter coefficients, k_i (implemented as transconductances) as well as the capacitances, C_i, and resistances, R_i obtained from the optimization process.

The modulators in Fig.4 were simulated using SIMSIDES [13]. Fig.5 shows the ideal output spectra of the modulators when clocked at f_s = 240 MHz. It can be observed the effect of the resonators poles distributed within the signal bandwidth. The impact on the in-band noise power is better appreciated in Fig.6 that represents the Signal-to-(Noise+Distortion) Ratio (*SNDR*) vs input amplitude. Note that, although both the 2-2-1 and 3-2 architectures have the same location of the zeroes of the NTF, the 3-2 modulator achieves a worse resolution. This is due to the fact that the optimization process applied to that architecture was more conservative as a consequence of the stability constrains imposed by the 3rd-order stage.

In addition to the ideal performance described above, the effect of most critical limiting factors has been taken into account in the high-level design. Fig.7 shows the *SNR* loss caused by clock jitter error. Note that the 2-1-1-1 architecture seems to be less sensitive to this error than the other architectures. However, it is important to note that the ideal *SNR* of this modulator is lower than the others. Therefore, there is a higher component of quantization noise masking the effect of clock jitter.

Two critical limiting factors in cascaded ΣΔMs, and particularly in their CT implementation, are circuit tolerances and component mismatch. The first one can be controlled by using tuning of time constants [4,5] or digital calibration [6]. However mismatch error still remains. In order to evaluate the impact of this error on the performance of the modulators in Fig.4, maximum values of mismatch were estimated for a 0.13 μm CMOS technology considering a Gm-C implementation. The

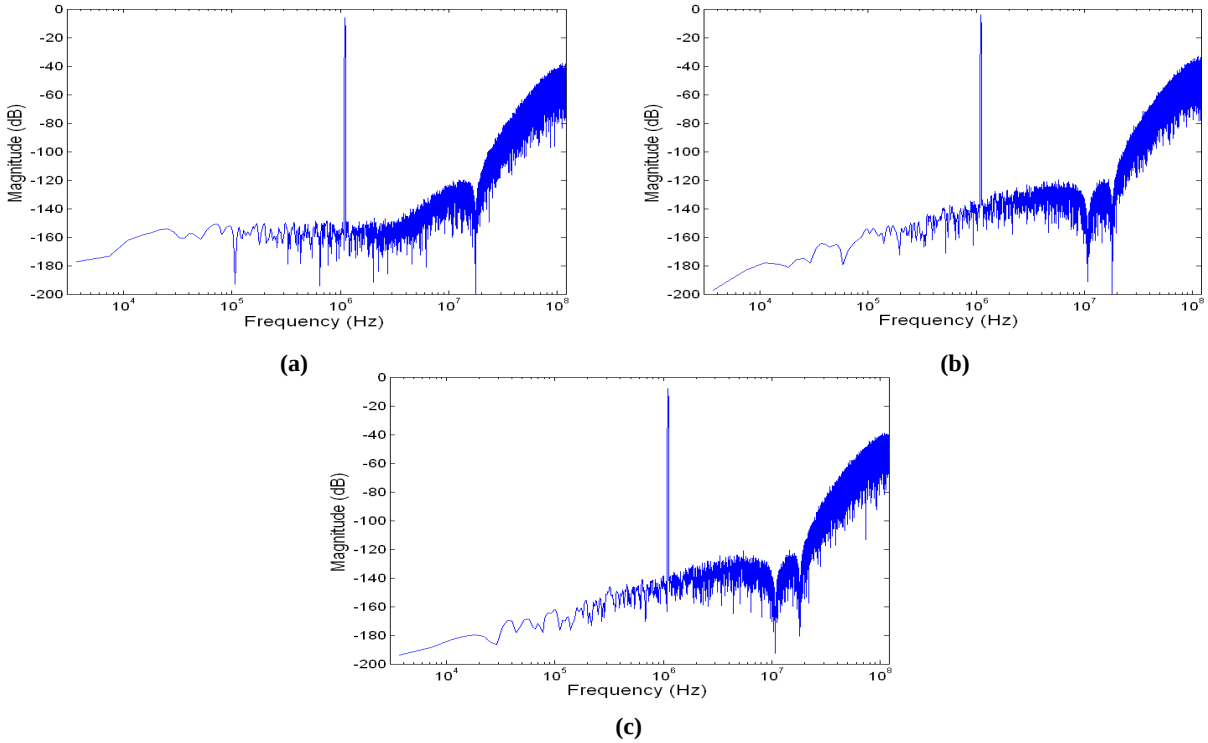


Figure 5. Ideal output spectra of the cascaded CT ΣΔMs in Fig.4: (a) 2-1-1-1. (b) 2-2-1. (c) 3-2.

Table 1: Transfer functions and cancellation logic functions of the modulators in Fig.4

Modulator	Transfer functions	Cancellation Logic
2-1-1-1	$F_{14} = \frac{b_{10}}{s^3(s^2+\omega_p^2)}$ $F_{24} = \frac{-1}{T_s^3 s^3} \qquad F_{34} = \frac{-1}{T_s^2 s^2}$ $F_{44} = \frac{-1}{T_s s}$	$CL_1 = z^{-1}(n_{14} + n_{13}z^{-1} + n_{12}z^{-2} + n_{11}z^{-3} + n_{10}z^{-4})$ $CL_2 = \frac{1}{6}z^{-1}(1+4z^{-1}-z^{-2})(1-2\cos(T_s\omega_p)z^{-1}+z^{-2})$ $CL_3 = \frac{1}{2}z^{-1}(1+z^{-1})(1-z^{-1})(1-2\cos(T_s\omega_p)z^{-1}+z^{-2})$ $CL_4 = (1-z^{-1})^2(1-2\cos(T_s\omega_p)z^{-1}+z^{-2})$
2-2-1	$F_{13} = \frac{b_{10}}{s(s^2+\omega_{p1}^2)(s^2+\omega_{p2}^2)}$ $F_{23} = \frac{b_{20}}{s(s^2+\omega_{p2}^2)} \qquad F_{44} = \frac{-1}{T_s s}$	$CL_1 = z^{-1}(n_{14} + n_{13}z^{-1} + n_{12}z^{-2} + n_{11}z^{-3} + n_{10}z^{-4})$ $CL_2 = z^{-1}(n_{22} + n_{21}z^{-1} + n_{20}z^{-2})(1-2\cos(T_s\omega_{p1})z^{-1}+z^{-2})$ $CL_3 = (1-2\cos(T_s\omega_{p1})z^{-1}+z^{-2})(1-2\cos(T_s\omega_{p2})z^{-1}+z^{-2})$
3-2	$F_{12} = \frac{b_{11}s + b_{10}}{s(s^2+\omega_{p1}^2)(s^2+\omega_{p2}^2)}$ $F_{22} = \frac{b_{21}s + b_{20}}{s^2+\omega_{p2}^2}e^{-T_s s} + k_c e^{-T_s s/2}$	$CL_1 = z^{-2}(n_{14} + n_{13}z^{-1} + n_{12}z^{-2} + n_{11}z^{-3} + n_{10}z^{-4})$ $CL_2 = (1-2\cos(T_s\omega_{p1})z^{-1}+z^{-2})(1-z^{-1})\cdot$ $(1-(2\cos(T_s\omega_{p2})-k_c)z^{-1} + (1+n_{21}-k_c 2\cos(T_s\omega_{p2}))z^{-2} + (n_{20}+k_c)z^{-3})$
Cancellation Logic Coefficients		
2-1-1-1	$n_{10} = n_{14} = \frac{-b_{10}}{T_s^3\omega_p^5}\left[\sin(T_s\omega_p) - T_s\omega_p + \frac{1}{6}(T_s\omega_p)^3\right]$ $n_{11} = n_{13} = \frac{-b_{10}}{T_s^3\omega_p^5}[(T_s\omega_p)^3\frac{2-\cos(T_s\omega_p)}{3} - 4\sin(T_s\omega_p) + 2T_s\omega_p(\cos(T_s\omega_p)+1)$ $n_{12} = \frac{-b_{10}}{T_s^3\omega_p^5}[(T_s\omega_p)^3\frac{1-4\cos(T_s\omega_p)}{3} + 6\sin(T_s\omega_p) - 2T_s\omega_p(1+2\cos(T_s\omega_p))]$	
2-2-1	$n_{10} = n_{14} = \frac{-b_{10}}{\omega_{p1}^3\omega_{p2}^3(\omega_{p2}^2-\omega_{p1}^2)}[T_s(\omega_{p1}\omega_{p2}^3 - \omega_{p1}^3\omega_{p2}) + \omega_{p1}^3\sin(T_s\omega_{p2}) - \omega_{p2}^3\sin(T_s\omega_{p1})$ $n_{11} = n_{13} = \frac{-2b_{10}}{\omega_{p1}^3\omega_{p2}^3(\omega_{p2}^2-\omega_{p1}^2)}[(T_s(\omega_{p2}\omega_{p1}^3 - \omega_{p2}^3\omega_{p1})(\cos(T_s\omega_{p1}) + \cos(T_s\omega_{p2}))) +$ $+ \omega_{p2}^3\sin(T_s\omega_{p1})(1+\cos(T_s\omega_{p2})) - \omega_{p1}^3\sin(T_s\omega_{p2})(1+\cos(T_s\omega_{p1}))]$ $n_{12} = \frac{-2b_{10}}{\omega_{p1}^3\omega_{p2}^3(\omega_{p2}^2-\omega_{p1}^2)}[T_s(\omega_{p1}\omega_{p2}^3 - \omega_{p1}^3\omega_{p2})(1+2\cos(T_s\omega_{p1})\cos(T_s\omega_{p2})) +$ $+ \omega_{p1}^3\sin(T_s\omega_{p2})(1+2\cos(T_s\omega_{p1})) - \omega_{p2}^3\sin(T_s\omega_{p1})(1+2\cos(T_s\omega_{p2}))]$ $n_{20} = n_{22} = \frac{-b_{20}}{\omega_{p2}^3}[T_s\omega_{p2} - \sin(T_s\omega_{p2})] \qquad n_{21} = \frac{-2b_{20}}{\omega_{p2}^3}[\sin(T_s\omega_{p2}) - T_s\omega_{p2}\cos(T_s\omega_{p2})]$	

Table 1: Transfer functions and cancellation logic functions of the modulators in Fig.4.(Cont.)

Mod.	Cancellation Logic Coefficients
3-2	$10 = \frac{-b_{10}(T_s\omega_{p1}\omega_{p2}(\omega_{p2}^2-\omega_{p1}^2)+\omega_{p1}^3\sin(T_s\omega_{p2})-\omega_{p2}^3\sin(T_s\omega_{p1}))}{\omega_{p1}^3\omega_{p2}^3(\omega_{p2}^2-\omega_{p1}^2)} +$ $+\frac{-b_{11}(\omega_{p1}^2(1-\cos(T_s\omega_{p2}))-\omega_{p2}^2(1-\cos(T_s\omega_{p1})))}{\omega_{p1}^2\omega_{p2}^2(\omega_{p2}^2-\omega_{p1}^2)}$ $11 = \frac{-2b_{10}(T_s\omega_{p1}\omega_{p2}(\omega_{p1}^2-\omega_{p2}^2)(\cos(T_s\omega_{p1})+\cos(T_s\omega_{p2}))+\omega_{p2}^3\sin(T_s\omega_{p1})(1+\cos(T_s\omega_{p2})))}{\omega_{p1}^3\omega_{p2}^3(\omega_{p2}^2-\omega_{p1}^2)} +$ $\frac{2b_{10}(\omega_{p1}^3\sin(T_s\omega_{p2})(1+\cos(T_s\omega_{p2})))}{\omega_{p1}^3\omega_{p2}^3(\omega_{p2}^2-\omega_{p1}^2)} + \frac{2b_{11}(\omega_{p2}^2\cos(T_s\omega_{p2})(1-\cos(T_s\omega_{p1}))-\omega_{p1}^2\cos(T_s\omega_{p1})(1-\cos(T_s\omega_{p2}))}{\omega_{p1}^2\omega_{p2}^2(\omega_{p2}^2-\omega_{p1}^2)}$ $12 = \frac{-2b_{10}(T_s\omega_{p1}\omega_{p2}(\omega_{p2}^2-\omega_{p1}^2)(1+2\cos(T_s\omega_{p1})\cos(T_s\omega_{p2}))+\omega_{p1}^3\sin(T_s\omega_{p2})(1+2\cos(T_s\omega_{p1})))}{\omega_{p1}^3\omega_{p2}^3(\omega_{p2}^2-\omega_{p1}^2)} +$ $\frac{2b_{10}(\omega_{p2}^3\sin(T_s\omega_{p1})(1+2\cos(T_s\omega_{p2})))}{\omega_{p1}^3\omega_{p2}^3(\omega_{p2}^2-\omega_{p1}^2)}$ $13 = \frac{-2b_{10}(T_s\omega_{p1}\omega_{p2}(\omega_{p1}^2-\omega_{p2}^2)(\cos(T_s\omega_{p1})+\cos(T_s\omega_{p2}))+\omega_{p2}^3\sin(T_s\omega_{p1})(1+\cos(T_s\omega_{p2})))}{\omega_{p1}^3\omega_{p2}^3(\omega_{p2}^2-\omega_{p1}^2)} +$ $\frac{2b_{10}(\omega_{p1}^3\sin(T_s\omega_{p2})(1+\cos(T_s\omega_{p2})))}{\omega_{p1}^3\omega_{p2}^3(\omega_{p2}^2-\omega_{p1}^2)} + \frac{2b_{11}(\omega_{p1}^2\cos(T_s\omega_{p1})(1-\cos(T_s\omega_{p2}))-\omega_{p2}^2\cos(T_s\omega_{p2})(1-\cos(T_s\omega_{p1})))}{\omega_{p1}^2\omega_{p2}^2(\omega_{p2}^2-\omega_{p1}^2)}$ $14 = \frac{-b_{10}(T_s\omega_{p1}\omega_{p2}(\omega_{p2}^2-\omega_{p1}^2)+\omega_{p1}^3\sin(T_s\omega_{p2})-\omega_{p2}^3\sin(T_s\omega_{p1}))}{\omega_{p1}^3\omega_{p2}^3(\omega_{p2}^2-\omega_{p1}^2)} -$ $\frac{b_{11}(\omega_{p2}^2(1-\cos(T_s\omega_{p1}))-\omega_{p1}^2(1-\cos(T_s\omega_{p2})))}{\omega_{p1}^2\omega_{p2}^2(\omega_{p2}^2-\omega_{p1}^2)}$ $20 = \frac{b_{21}\sin(T_s\omega_{p2})}{\omega_{p2}} - \frac{b_{20}(1-\cos(T_s\omega_{p2}))}{\omega_{p2}^2}$ $n_{21} = \frac{-b_{21}\sin(T_s\omega_{p2})}{\omega_{p2}} - \frac{b_{20}(1-\cos(T_s\omega_{p2}))}{\omega_{p2}^2}$

results of this analysis are shown in Fig.8 where the *SNR* is represented as a function of the standard deviation of the transconductances (σ_{gm}) and capacitances (σ_C). For each point of these surfaces, a MonteCarlo analysis of 150 simulations was carried out. The value of the *SNR* represented in the vertical axis of Fig.8 is obtained by 90% of the simulations for each case of σ_{gm} and σ_C. Note that even in the worst-case mismatch, the resolution is above the specified (72-dB).

Finally, the modulators in Fig.4 were high-level sized, i.e, the system-level specifications (12-bit@20-MHz) were mapped onto building-block specification using statistical optimization for design parameter selection, and behavioral simulation for evaluation. The results of this sizing process are summarized in Table 3 and Table 4 showing the maximum (minimum) values of the circuit error mechanisms that can be tolerated in order to fulfil the required modulator performance. As an illustration, Fig.9 shows the output spectra of the modulators taking into account the non-idealities listed in these tables. The effective resolution is $\cong 13.4$ bits and $\cong 13.2$bits for the modulators in Fig.4(b) and (c), respectively.

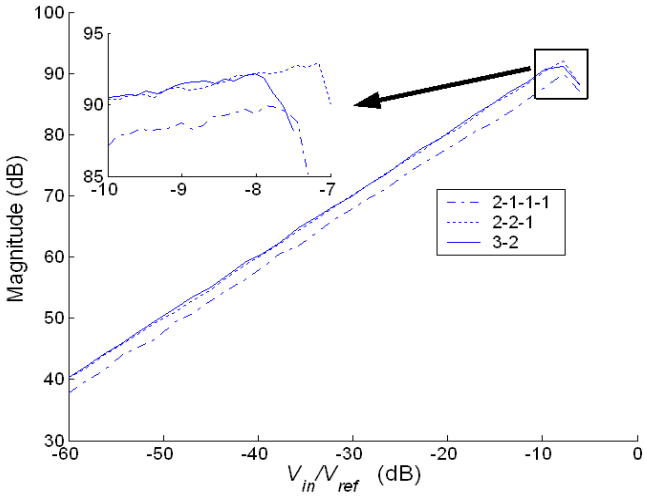


Figure 6. *SNDR* vs. input amplitude (referred to reference voltage).

Table 2: Loop filter coefficients of the modulators in Fig.4

2-1-1-1 Modulator		2-2-1 Modulator		3-2 Modulator	
$R_{in} = R_{fb} = 2\ \mathrm{k}\Omega$; $R_r = 8.2\ \mathrm{k}\Omega$		$R_{in1} = R_{fb1} = 2\ \mathrm{k}\Omega$; $R_{r1} = 9\ \mathrm{k}\Omega$		$R_{in1} = R_{fb1} = 2\ \mathrm{k}\Omega$	
$C_1 = 1.875$ pF	$C_{2\ldots5} = 0.75$ pF	$C_1 = 1.875$ pF	$C_{2\ldots5} = 0.75$ pF	$C_1 = 10$ pF	$C_{2\ldots5} = 1$ pF
$k_{g1} = 150\ \mu S$	$k_{g2} = 48\ \mu S$	$k_{g1} = 166\ \mu S$	$k_{g2} = 30\ \mu S$	$k_{g1} = 312\ \mu S$	$k_{g2} = 130\ \mu S$
$k_{g3\ldots5} = 20\ \mu S$	$k_{ff} = 60\ \mu S$	$k_{g3} = 200\ \mu S$	$k_{g4} = 46\ \mu S$	$k_{g3} = 26\ \mu S$	$k_{g4} = 182\ \mu S$
$k_{in2\ldots4} = k_{fb2\ldots4} = 180\ \mu S$		$k_{g5} = 20\ \mu S$	$k_{r2} = 13\ \mu S$	$k_{g5} = 104\ \mu S$	$k_{ff1} = 208\ \mu S$
		$k_{ff1} = 63\ \mu S$	$k_{ff2} = 112\ \mu S$	$k_{ff2} = 78\ \mu S$	$k_{ff3} = 130\ \mu S$
		$k_{in2} = k_{fb2} = 100\ \mu S$		$k_{in2} = k_{fb2} = 130\ \mu S$	
		$k_{in3} = k_{fb3} = 180\ \mu S$		$k_{r1} = 208\ \mu S$	$k_{r2} = 26\ \mu S$

Table 3: High-level sizing of Fig.4(b)

Front-end opamp	
GB	>600 MHz
DC Gain	>70 dB
Phase Margin	60º
Parasitic Input Capacitance	<0.2 pF
Parasitic Output Capacitance	<0.2 pF
Diff. Output Swing	>0.5 V
Transconductors	
DC Gain	>50 dB
Diff. Input Amplitude	0.3 V
Diff. Output Amplitude	0.3 V
Third-order non-linearity	>56 dBV

Table 4: High-level sizing of Fig.4(c)

Front-end opamp	
GB	>600 MHz
DC Gain	>60 dB
Phase Margin	60º
Parasitic Input Capacitance	<0.2 pF
Parasitic Output Capacitance	<0.2 pF
Diff. Output Swing	>0.5 V
Transconductors	
DC Gain	>60 dB
Diff. Input Amplitude	0.4 V
Diff. Output Amplitude	0.4 V
Third-order non-linearity	>53 dBV

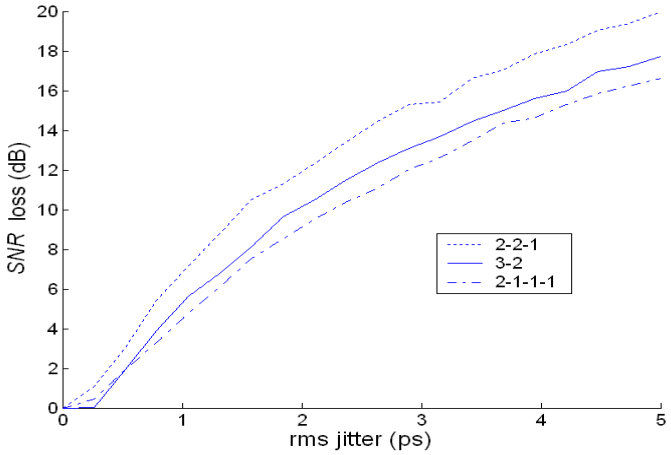
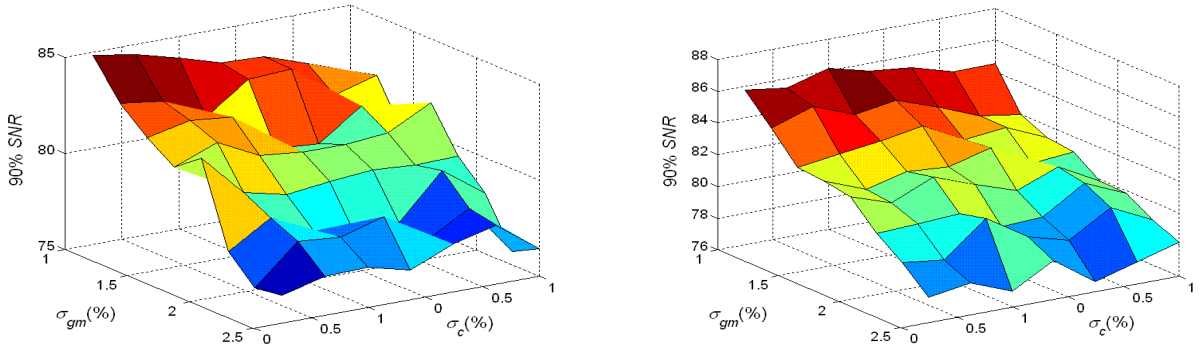
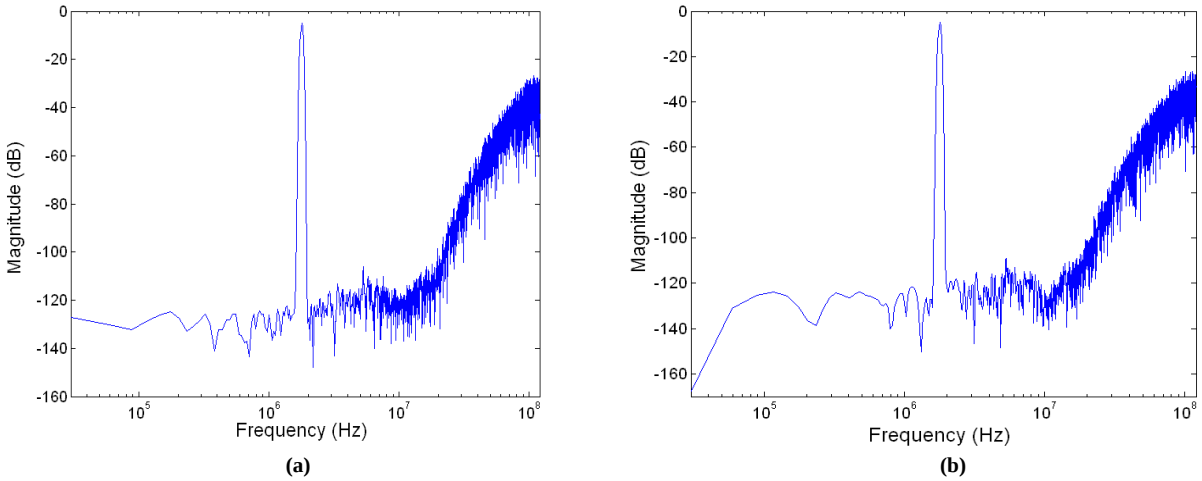


Figure 7. *SNR* loss due to clock jitter.



(a) **(b)**

Figure 8. *SNR* loss vs. mismatch for: (a) 2-2-1 CT ΣΔM. (b) 3-2 CT ΣΔM.



(a) **(b)**

Figure 9. Output Spectra for: (a) 2-2-1 CT ΣΔM. (b) 3-2 CT ΣΔM.

5. CONCLUSIONS

In this paper a new methodology of synthesizing cascaded continuous-time ΣΔ modulators has been presented. It has been demonstrated that more efficient topologies in terms of circuit complexity can be generated if the design is directly done in the continuous-time domain and the cancellation logic is taken into account in the synthesis procedure. In order to illustrate the method, several cascaded architectures have been synthesized and designed to achieve VDSL system requirements: 12-bit@20MHz. Behavioral time-domain simulations considering their most critical limiting factors show that these architectures are good candidates for in-coming broadband telecommunication systems.

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