CMOS SPADs Selection, Modeling and Characterization Towards Image Sensors Implementation

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***Abstract*—The selection, modeling and characterization of Single Photon Avalanche Diodes (SPADs) are presented. Working with the standard 180nm UMC CMOS process, different SPAD structures are proposed in combination with several quenching circuits in order to compare their relative performances. Various configurations for the active region and the prevention of the premature edge breakdown are tested, looking for a miniaturization of the devices to implement image sensor arrays without loses in their performance.**

I. Introduction

Single Photon Avalanche Diodes (SPADs) are p/n junctions biased above their breakdown voltage [1], in the so-called Geiger mode [2]. In this situation the electric field is so high that a single carrier in the depletion region can originate a self-sustained avalanche current in the milliamperes range [3]. An additional circuit is required to use the SPAD as a single-photon detector. It is the quenching circuit, and its mission is to extinguish the avalanche before damage to the structure occurs. The simplest one consists of a high-value ballast resistor connected in series to the diode (R_q in Fig. 1(a)), which is aimed to lower the bias voltage below the breakdown voltage [4], [5]. When an avalanche is triggered, the current flowing through the diode increases, inducing a voltage drop over the ballast resistor. The current starts decreasing until it reaches a threshold value called latching current, at which the avalanche is no more self-sustained [4]. Fig. 1(b) shows the typical I-V piecewise linear characteristic of the SPAD.

SPADs are a dedicated type of photodetectors that are attracting increasing interest. Their fabrication in standard CMOS technologies allows to integrate all peripheral blocks required for vision systems (arrays of SPADs and digital processing electronics) on the same monolithic chip. Thus, the combination of high gain and quantum efficiency, along with their small size, low operation voltage and insensitivity to magnetic fields make SPADs particularly attractive for different imaging and medical applications [6].

In this paper we present a testchip with several SPAD structures to be tested, together with different quenching circuits that have been chosen using the information provided by a proprietary model for SPADs based on [7]. The main objective of this work is to study the potentiality of different structures and quenching circuits for generating image sensor arrays, using the standard 180nm UMC CMOS process.

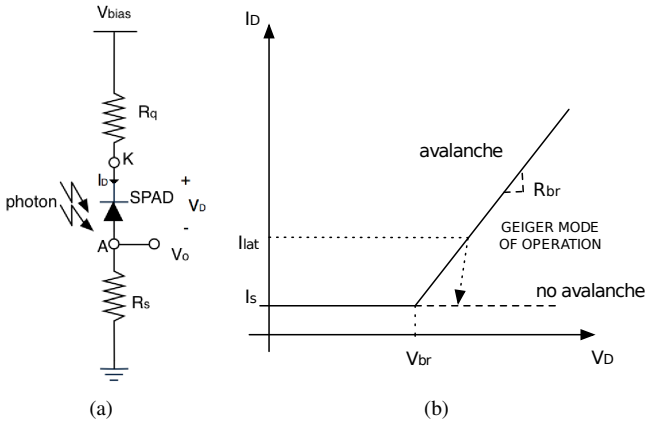

Fig. 1. (a) Scheme for illustrating the operation of the SPAD with passive quenching. (b) I-V characteristic of the SPAD.

II. Selection of CMOS SPADs Structures

In this section a variety of SPAD structures that have been used so far in different technological nodes is presented. The different modifications in the structure are intended to avoid the premature edge breakdown (PEB). It consists of a spurious avalanche that favorable takes places at the edges of the device active area, reducing its sensitivity [1]. The structures are the following:

1) **Simple p+/nwell diode**: This is the basis structure and does not include any mechanism to avoid PEB.
2) **P+/nwell diode with twell guard ring**: A deeper and lower doped implant is introduced in the periphery of the junction to raise the breakdown voltage in this region with regard to the center of the active area [8].
3) **Twell/nwell diode**: The junction is formed between the lower doped and deeper twell, and the nwell to decrease the dark count rate (DCR) and change the maximum of the photon detection efficiency (PDE) [9].

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4) **Control gate guard ring**: A biased poly layer that changes the shape of the depletion region together with a twell implant at a certain distance of the active area are introduced to increase the breakdown voltage at the edge of the junction [8].
5) **Virtual guard ring**: A higher doped implant is introduced in the central region of the active area to enhance the electric field in this zone [9].
6) **Diffused guard ring**: A lower doped and deeper guard ring in the periphery of the device is formed by diffusion, which imposes minimum size constraints [10].
7) **Shallow Trench Isolation guard ring**: An STI is used for implementing an area-efficient guard ring, increasing the fill factor and reducing the pixel area [11].

Although cases 5 and 7 seem to be promising structures in terms of scalability, they will no longer be taken into account since the use of standard CMOS technologies, to avoid excessive fabrication expenses, imposes restrictions on the availability of layers. Moreover, case 6 will be neglected because of its minimum size constraints and high DCR [5], which are very important drawbacks for image applications using sensor arrays.

Besides of the variations in the structure, changes in the SPAD sizes and geometries are of interest in order to determine the optimal image sensing response. This is done by varying the diameter of the active area and implementing SPADs with circular and octagonal shapes.

With regard to the final application, it is interesting to compare the relative performances of the different SPADs in terms of several parameters before designing the sensor array. These main parameters that characterize SPADs operation are:

- **Static I-V characteristic**: This measurement allows to determine the breakdown voltage of the SPAD and its internal resistance to check the validity of the assumed piecewise linear characteristic.
- **Noise**: The main source of internal noise is usually associated to dark counts, which are produced by photons and thermally generated carriers that trigger a new avalanche. The afterpulses also contribute to the noise. They happen when the generated carriers are trapped by crystal defects and after a certain time delay they are released producing an avalanche [8]. In the case of SPAD arrays, the crosstalk will also influence the total internal noise of the device. It occurs if carriers generated in one pixel trigger an avalanche in a near one.
- **Dead time**: Lapse of time during which the SPAD cannot detect the arrival of new photons. It comprises the quenching, during which it takes place the extinction of the avalanche, and the reset phase, where the initial bias conditions are restored. Sometimes, it is possible to control the period of time between these two stages, the hold off time, and see how it affects the afterpulsing [4].
- **PDE**: It represents the probability that a single absorbed photon generates an avalanche current. Its value depends on the wavelength of the incident photons [2].

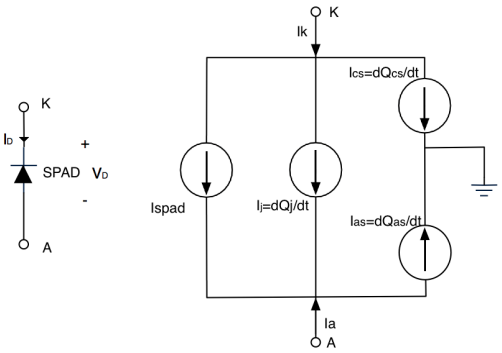

Fig. 2. Charge control model used for representing the SPAD behavior.

- **Fill factor**: When dealing with SPAD arrays, it is important to increase the fill factor, which is the ratio between the active area and the total area of the SPAD [12].
- **Time resolution**: Variation of the position in time of the different carrier avalanche pulses when the SPAD is illuminated with a pulsed laser [12].

III. Model Parametrization

Traditionally, the model used for the SPAD is that shown in [13], but there are new versions like that in [7] with a more accurate description of the device. In this work the model introduced in [7] has been updated to deal with integrated devices. This has been done by including the parasitic capacitances present in each structure and with a proper parametrization for our specific technology.

Using the information provided by the simulation of a p+/nwell diode from the technology, a two-step linear I-V curve for each one of the SPAD structures has been obtained.[1]

$$I_{\text{spad}} = \begin{cases} I_s & ,V_D < V_{br} \\ I_s + \frac{V_n}{R_{br}} \ln\left(1 + e^{\frac{V_D - V_{br}}{V_n}}\right) & ,V_D > V_{br} \end{cases} \quad (1)$$

Eq. (1) models the voltage dependence of the static current through the SPAD, where I_s is the saturation current, R_{br} is the internal resistance, V_n is a normalization voltage, V_{br} is the breakdown voltage, and V_D is the voltage across the SPAD.

Looking at the different diode structures (see Fig. 3), it can be seen that there exists a parasitic nwell/psubstrate diode. As illustrated in Fig. 2, this diode has also been incorporated in the model through the inclusion of the cathode-to-substrate capacitor to allow a complete description of the dynamic behavior of the device.

The information obtained by simulating the SPAD through its model, together with the different quenching circuits included in the testchip has been used to design the latter properly. As it will be shown in the next section, three different topologies for the quenching circuit will be studied in order to compare their performance in terms of noise (dark counts and afterpulsing) and time.

[1]The diode width and length have been chosen trying to minimize the relative error of area and perimeter compared to circular and octagonal shapes.

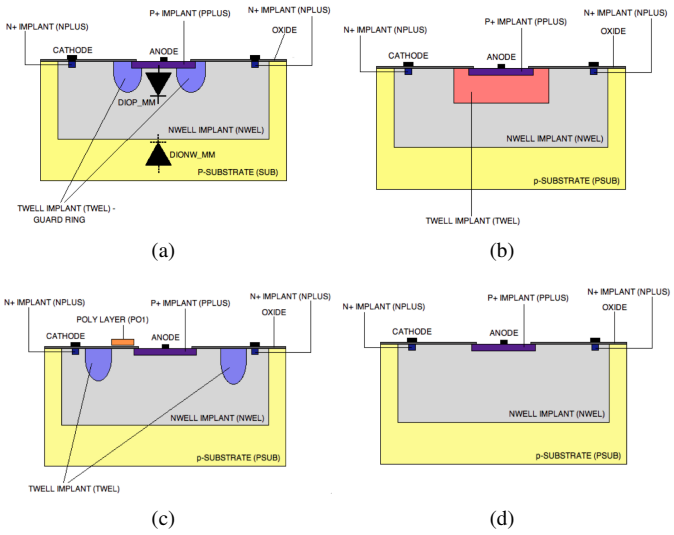

Fig. 3. SPAD structures implemented in the testchip: (a) p+/nwell diode with twell guard ring, (b) twell/nwell diode, (c) diode with control gate guard ring, (d) simple p+/nwell diode.

The comparison between the different SPAD structures together with their corresponding quenching circuits will be done in terms of some of the parameters shown previously. To deal with the desired application, special attention will be paid to the static I-V characteristic of the different test structures, the frequency of the noise sources, the dead time and the change in the PDE depending on the wavelength of the incident photons and the structure of the SPAD.

IV. Characterization Circuitry and Testchip

As stated before, for the fabrication of the testchip the standard 180nm UMC CMOS process has been chosen. Due to the constraints imposed by the layer availability of the technology it is not possible to implement the virtual guard ring and the STI guard ring structure. Moreover, the minimum size constraints of the diffused guard ring structure is a problem when implementing SPAD arrays, so it was discarded. Only the first four SPAD structures already described in section II will be implemented. They are shown in Fig. 3.

Regarding the quenching circuitry, three different alternatives have been implemented:

- Simple passive quenching circuit, implementing the ballast resistor with either an NMOS transistor or a passive resistance.
- Addition to the previous structure of an active reset branch to speed up this stage.
- Passive quenching and active reset circuit, which includes a mechanism to control the hold-off time.

This first two quenching circuits are put together (see Fig. 4), with the possibility of activating or not the active branch. This allows to start from the simplest case and then see the changes when working with a more complex quenching circuit. The comparison will be made in terms of:

- Time: Variation of the dead time and time resolution.

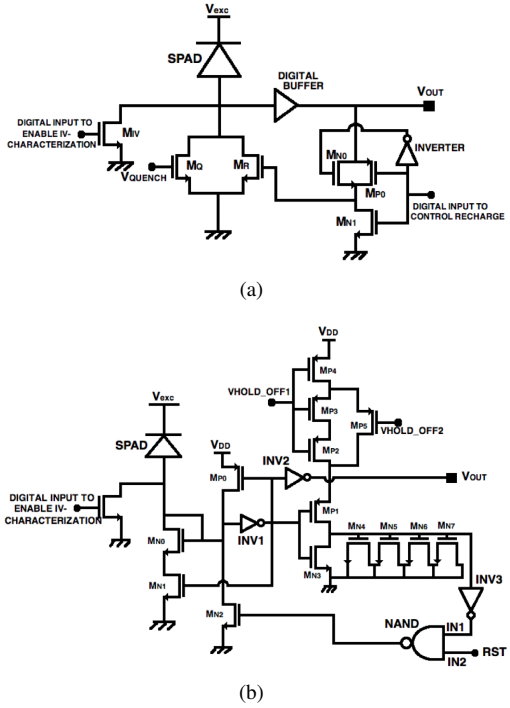

Fig. 4. (a) First quenching circuit. (b) Second quenching circuit.

TABLE I
Main characteristics of the different SPAD structures.

Test structure	Type of diode	Guard ring	Type of shape	Active area (ϕ)	Quenching circuit
#1	p+/nwell	twell	circular	7μm	Fig. 4(a)
#2	p+/nwell	twell	circular	14μm	Fig. 4(a)
#3	p+/nwell	twell	circular	21μm	Fig. 4(b)
#4	twell/nwell	–	circular	14μm	Fig. 4(a)
#5	p+/nwell	twell	octagonal	14μm	Fig. 4(a)
#6	p+/nwell	–	circular	14μm	–
	p+/nwell	twell	circular	14μm	Fig. 4(b)
#7	p+/nwell	control gate	circular	14μm	Fig. 4(b)

- Noise: Frequency of dark count and afterpulsing events depending on the quenching circuitry.
- Ability for detecting the incoming photons at different wavelengths when adding complexity to the quenching circuits, which will depend on the dead time and PDE.

The quenching circuit alternatives and the combination of different SPAD structures, sizes and shapes result into seven different test structures that are detailed in Table I. Tables II and III show the values of the geometric parameters[2] and the static I-V parameters of the different structures. As said before, this information was used for the design of the two quenching circuits.

Fig. 5 shows the layout of the different structures together with the test circuitry. The measurements expected to be done with the testchip are the following:

- The I-V characterization will be obtained for each struc-

[2] A_D and P_D refers to the dimensions of the junction diode, while A_{well} and P_{well} are associated to the nwell/psubstrate parasitic diode.

TABLE II
GEOMETRIC PARAMETERS OF THE DIFFERENT SPAD STRUCTURES.

Test structure	P_D (μm)	A_D (μm^2)	P_{well} (μm)	A_{well} (μm^2)
#1	22.0	38.5	36.4	105.7
#2	44.0	154.0	58.4	271.7
#3	66.0	346.4	80.4	514.7
#4	46.4	162.4	61.6	286.3
#5	44.0	154.0	55.9	248.8
#6	44.0	154.0	61.6	301.7
#7	44.0	154.0	51.9	214.3

TABLE III
FITTING PARAMETERS OF THE I-V CHARACTERISTIC TO EQ. (1).

Test Structure	V_n (mV)	V_{br} (V)	R_{br} (Ω)	I_s (A)
#1	10	9.68	823.4	9.7×10^{-18}
#2	10	9.70	207.2	2.8×10^{-17}
#3	10	9.73	91.9	5.6×10^{-17}
#4	10	9.70	207.2	2.8×10^{-17}
#5	10	9.70	207.2	2.8×10^{-17}
#6	10	9.70	207.2	2.8×10^{-17}
#7	10	9.70	207.2	2.8×10^{-17}

ture to see how good the fit with the model is.

- A measurement of the dead time in the different configurations of the quenching circuits will be also done, together with the time resolution using a pulsed laser.
- The noise will be characterized after leaving the SPADs in the dark for several hours. The afterpulsing can be obtained by comparing the results with the active and passive recharge if its probability is high. If not, it has to be studied in a time scale around one order of magnitude smaller than for the DCR (besides reducing the dead time, as stated before).
- The PDE will be measured after removing the influence of the dark count and afterpulsing events.

Once the relative performance of the different test structures is compared, there will be more information to be used that will allow to advance in the design of image sensor arrays.

V. CONCLUSIONS

A review of different SPAD structures and their principal characteristics is presented. Taking into account the restrictions in terms of layer availability imposed by the standard 180nm UMC CMOS technology, and the final target of implementing image sensor CMOS SPAD arrays, three of the structures are rejected. A proprietary model based on [7] and adapted to integrated devices is developed for the design of the quenching circuitry that is connected to the SPADs. The combination of several SPADs with distinct size, shape or structure, along with different quenching circuits results in seven test structures whose relative performance in terms of the main parameters of the SPADs will be studied. This work provides useful data towards the implementation of image sensors in a standard CMOS technology.

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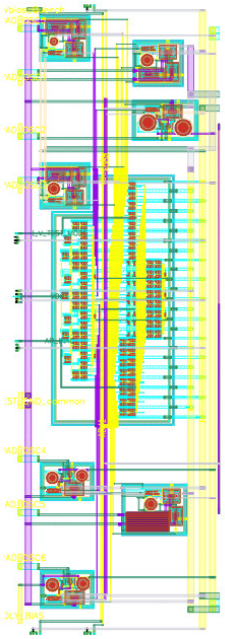

Fig. 5. Layout view of the different structures, together with the quenching and test circuitry.

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