Low-Noise and High-Efficiency Near-IR SPADs in 110nm CIS Technology

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***Abstract*—Photon detection at longer wavelengths is much desired for LiDAR applications. Silicon photodiodes with deeper junctions and larger multiplication regions are in principle more sensitive to near-IR photons. This paper presents the complete electro-optical characterization of a P-well/ Deep N-well single-photon avalanche diodes integrated in 110nm CMOS image sensor technology. The performance of time-of-flight image sensors is determined by the characteristics of the individual SPADs. In order to fully characterize this technology, devices with various sizes, shapes and guard ring widths have been fabricated and tested. The measured mean breakdown voltage is of 18V. The proposed structure has 0.4Hz/µm^2 dark count rate, 0.5% afterpulsing, 188ps FWHM (total) jitter and around 10% photon detection probability at 850nm wavelength. All figures have been measured at 3V excess voltage.**

***Index Terms*—single-photon avalanche diode (SPAD), dark count rate, afterpulsing, FHWM jitter, photon detection probability, breakdown voltage**

I. Introduction

During the last years, deep submicron **C**MOS **I**mage **S**ensor (CIS) technologies have drawn attention of **S**ingle **P**hoton **A**valanche **D**iode (SPAD) designers, since they are a good alternative to standard processes in terms of noise and photon detection probability, without the fabrication cost of a custom technology. After all, the accuracy of **T**ime-**o**f-**F**light (ToF) sensors based on SPADs is bound to the performance of photodetectors, which is determined by technology, geometry and architecture. Over the time, CIS technologies have been tweaked to constantly improve several SPAD structures [1]. In order to fabricate low-noise SPADs: (i) high doping concentrations should be avoided, as they lower the breakdown voltage and increase trap-assisted carrier tunneling; and (ii) a guard ring structure that eliminates high-field regions on the periphery of the SPAD is required [2]. Another important challenge, given the emerging market for LiDAR, is to provide significant **P**hoton **D**etection **P**robability (PDP) at longer wavelengths. This is achieved in [3] by combining an active junction between the deep N-well and the low-resistivity P-substrate (DNW/PSUB) with backside illumination. The fill factor is also a limitation, even for the finest 3D-IC [4].

When it comes to design high performance SPAD devices in a standard CIS process, all possible layer combinations have to be examined, except those not providing a uniform electric field. This entails searching for the appropriate PN junction that better fits the specifications of the application. As a general rule, **D**ark **C**ount **R**ate (DCR) can be decreased by lowering the gain of the junction, but the performance of all possible structures has to be evaluated. Recently, a P+/N-implant SPAD has been reported in a 110nm process [5].

This work concentrates on a P-well/Deep N-well (PW/DNW) SPAD structure in the same technology node, as we are interested in an enhanced sensitivity at near-IR range. The fundamental advantages are derived of a lower doping concentration and a deeper junction. PW/DNW diodes have low noise and better PDP at larger wavelengths than P+/N-well diodes [5], [6]. In exchange, PW/DNW junctions display worse jitter, afterpulsing [7] and crosstalk [8].

In this paper, we will present the implemented structures and the technological limitations in Section II. Section III is dedicated to the electro-optical characterization of different devices by measuring the key parameters like breakdown voltage, DCR, afterpulsing, PDP and jitter. Section IV presents a comparison to the state-of-the-art devices.

II. SPAD Structure

The fabricated test chip incorporates 2 modules for both transient and static characterization. Each module contains 96 PW/DNW SPAD devices of 16 different shapes and sizes (D1-16) as shown in Fig. 1. There are other structures that have been discarded. Basically the breakdown voltage (V_{BD}) of the multiplying junction plus the **E**xcess **V**oltage (Ve) cannot exceed the breakdown voltage of the inherent lateral diodes employed to isolate the SPAD from the rest of the circuitry present in the same substrate. This aspect is not contemplated in other DNW structures that can also operate as a SPAD, for instance the DNW/PSUB diode reported at [3]. The lack of isolation has an incidence in crosstalk, and limits the incorporation of additional circuitry on the same substrate. The top view and the cross section of the PW/DNW photodiode are displayed in Fig. 2. The active area of the SPAD is delimited by the polysilicon **G**uard **R**ing (GR). The N+ cathode connection surrounds the structure.

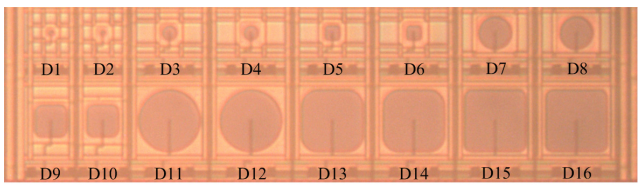

Fig. 1 Test module microphotograph.

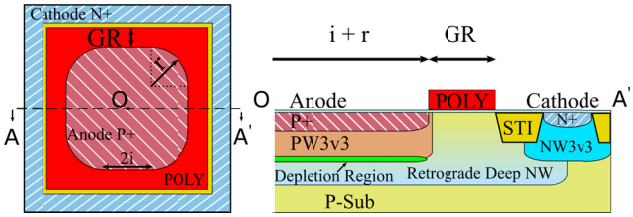

Fig. 2 Top view and cross section of the integrated SPAD structure

The multiplication junction is between PW and the DNW. The shape has been parameterized through i and r. Tested shapes range from a circular SPAD ($i = 0$) to a variety of squares with rounded corners ($i > 0$ and various values of r). The active area of the SPAD is given by:

$$A_{SPAD} = \pi r^2 + 4i(i + 2r) \quad (1)$$

III. ELECTRO-OPTICAL CHARACTERIZATION

A. Breakdown voltage

The V_{BD} of the 16 diodes of different shapes have been measured with an HP4155A semiconductor parameter analyzer. Different shapes and sizes of GR and active area of PW/DNW devices have been characterized, namely: circular SPADs of radius 2, 5, 10 and 20µm with GRs of 1 and 2µm widths (D1, D3, D7, D11 and D2, D4, D8 and D12, respectively); and squares of rounded corners with sides of 10, 20 and 40µm (2 different shapes) also with GRs of 1 and 2µm widths (D5, D9, D13, D15 and D6, D10, D14, D16, respectively). The V_{BD} has been measured with faint light for different chip samples. The values obtained are displayed in Fig. 3. It can be seen that V_{BD} is practically invariant to active area size, shape and GR width.

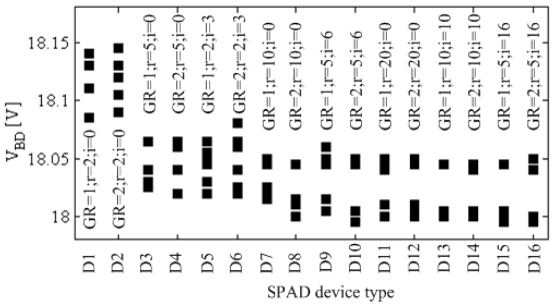

Fig. 3 SPADs structures V_{BD} : GR = guard ring size in µm; r = corner radius in µm; i = internal increment in µm.

B. Dark count rate

The majority of dark counts are due to Shockley-Read-Hall generation and band-to-band tunneling. The most straightforward dependence of the DCR is with the excess bias voltage. The increase in the electric field introduced by a higher Ve increases the avalanche-triggering probability and also the carrier generation rate. Fig. 4 displays the DCR versus Ve at room temperature for 4 different (D1, D3, D7, D15) active areas: 12.5, 78.5, 314.2 and 1742.5 µm^2, respectively. Abnormal device samples showing a larger DCR are represented with red color.

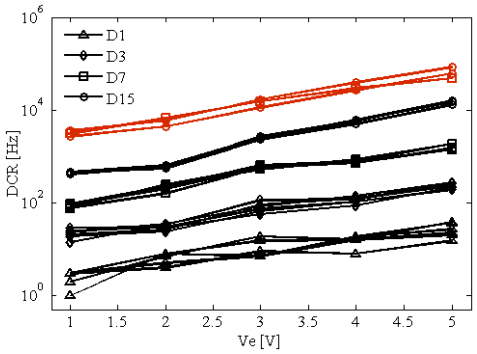

Fig. 4 DCR vs. Ve at room temperature

To understand the origin of the dark counts, DCR versus temperature for a D4 device (r=5µm) has been measured at 3, 4 and 5V excess voltage (see Fig. 5-left). The variation of V_{BD} with temperature has been compensated based on Fig. 5-right. The activation energy (E_A) of a low-DCR SPAD [8] was calculated using Arrhenius equation (dashed lines). The crossing point between thermal (high temperatures) and trap-assisted tunneling (low temperatures) generation mechanism is around 27°C.

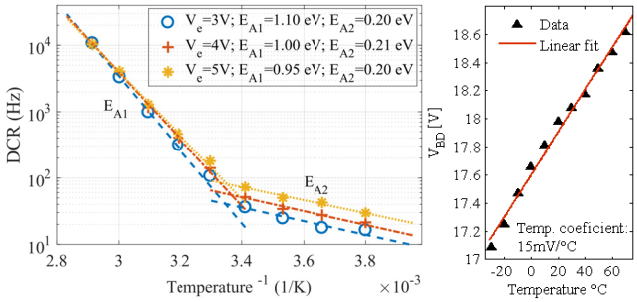

Fig. 5 DCR vs. temperature (left); V_{BD} vs. temperature (right)

DCR measurement is usually relevant at rather high Ve, where the PDP and jitter figures are acceptable. Moreover, seeking to increase the bandwidth, DCR has to be evaluated with small **D**ead **T**ime (DT). In these conditions the measured dark counts eventually include correlated noise due to afterpulsing, which is going to be contemplated in the next subsection. Fig. 6 presents the DCR measurements for a Ve of 3V and a DT below 500ns.

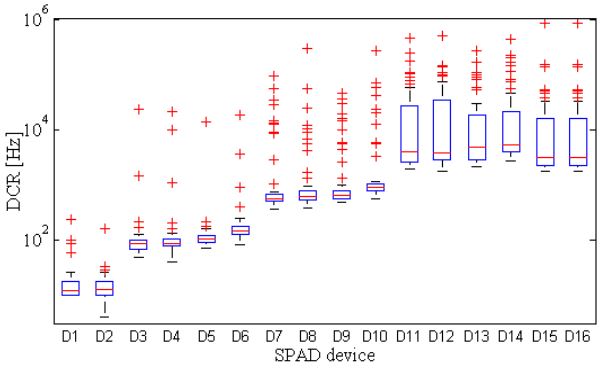

Fig. 6 DCR boxplot at Ve=3V, DT around 500ns; Room temp.; 10 chips

Sixty different instances have been measured for all D1-D16 SPADs across 10 chip samples. DCR uniformity is important to build large arrays. The larger the active area, the larger the device-to-device DCR deviation.

C. Afterpulsing

Afterpulsing (AP) is a correlated noise due to carriers trapped in the depletion region during an avalanche. They are statistically released later on, producing a spurious event. AP probability (P_{AP}) is mainly related with the magnitude of the avalanche current and cleanliness of the technology. Most of AP events appear in the first few microseconds after an avalanche occurs. For a D3 device (r=5µm), we have obtained a P_{AP} below 0.5% and 8% for 3V and 5V excess voltage, respectively. This is for a 5µs DT (see Fig. 7). For a DT of 500ns, P_{AP} is 2.7% at Ve of 3V. For a DT larger than 50µs, it is negligible. P_{AP} is measured using the inter-avalanche histogram method [9], which is robust against DT variations due to passive recharge mechanism.

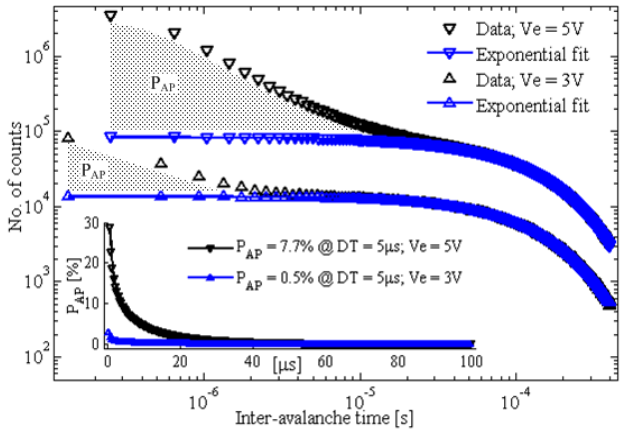

Fig. 7 Afterpulsing measurement of D3 based on inter-avalanche time

Seeking to increase the dynamic range, DT has to be reduced as far as the corresponding AP does not have an important impact on the application.

Acquiring the inter-arrival time histogram for low noise SPADs (e.g. few tens of counts per second) is time consuming. For instance, to accurately estimate the primary pulse rate with the slope of the Poisson fit in logarithmic scale, the time span of the histogram needs to cover up to few tens of milliseconds, taking more than a week of acquisition time. Less data leads to miscalculation of P_{AP} and the minimum DT that ensures negligible afterpulsing. In order to obtain an accurate measurement, the detector has been illuminated in single photon detection conditions with an uncorrelated light source. A total count rate (TCR) of 10kHz speeded up the acquisition down to one hour.

D. Photon detection probability

The setup for measuring the PDP consists in a halogen lamp, a monochromator, an integration sphere and a calibrated photodiode. Illumination has been set to single photon detection condition, being below 10nW/mm^2 for all wavelengths. SPAD output pulses are accurately integrated on a FPGA and the measurements are sent to a PC. The PDP is computed offline as follows:

$$\mathrm{PDP} = \frac{\mathrm{TCR}-\mathrm{DCR}}{\mathrm{PhR}}(1 - P_{\mathrm{AP}}) \quad (2)$$

where PhR is the photon rate impinging the active area, and the rest of the parameters have been already defined.

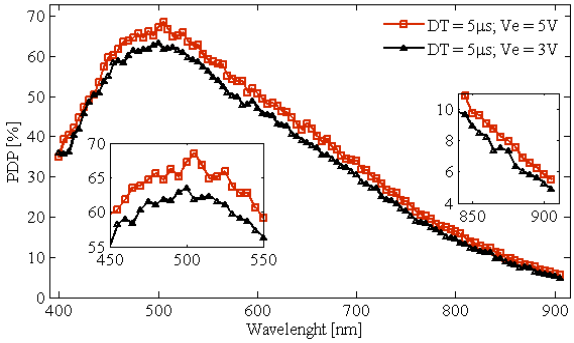

Fig. 8 PDP of D3 vs. λ; DT = 5µs; Room temperature

The measured PDP of D3 is shown in Fig. 8. It has been obtained for both 3V and 5V excess voltage. According to Fig. 7 DT has to be set to 50µs to ensure negligible afterpulsing. Therefore the maximum count rate is of 7.35kHz due to the predicted limit of $1/eDT$, where e is the Euler constant. However, employing a smaller DT extends the dynamic range avoiding distortions due to saturation. In this case, AP compensation is required for accurate measurement (eq. 2).

A PDP of 10% is obtained for Ve = 5V at 850nm wavelength. The peak is beyond 65% for Ve = 5V at 500nm. Note that beyond 3V excess voltage, PDP starts to saturate, causing an incremental improvement.

E. Jitter

The purpose of this subsection is to analyze the jitter of PW/DNW devices at different Ve, shape, size of active area and GR width. Moreover 2 different wavelengths have been considered to estimate the ToF precision in both cases. The power of the pulsed laser has been set to single photon illumination conditions. The total jitter along the signal chain has the following components:

$$\sigma_{TOT}^2 = \sigma_{SPAD}^2 + \sigma_{Laser}^2 + \sigma_{inv}^2 + \sigma_{LS}^2 + \sigma_{IOchip}^2 + \sigma_{IOFPGA}^2 \quad (3)$$

that express the contributions of the SPAD, the laser, tri-state inverters, the level shifter, the I/Os of the chip and FPGA, respectively. In the following, all the measurements represent the total jitter.

As can be seen at Fig. 9's bottom-right subset, the jitter does not depend on the size of the GR for small and circular devices (see D1-D2 and D11-D12). It can be noticed as well that the jitter is lower in circular devices (D11) than in devices with quasi-square shape (D15), especially for high Ve (see upper subsets). This might be due to a better lateral electric field uniformity in circular devices. Moreover, comparing D7 to D9 shapes, the fill factor improves by 17% while the jitter slightly increases. Finally, smaller devices have better jitter, showing smaller deviation across Ve (see bottom-left subset).

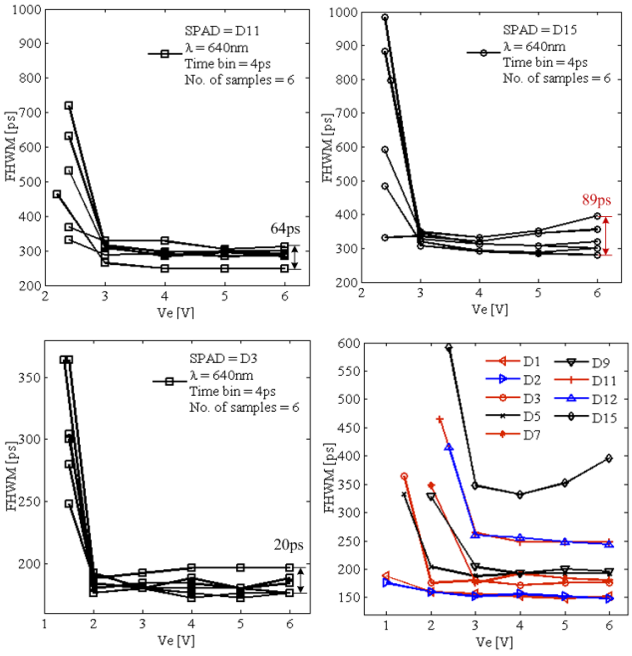

Fig. 9 FWHM jitter vs. Ve for different sizes and shapes

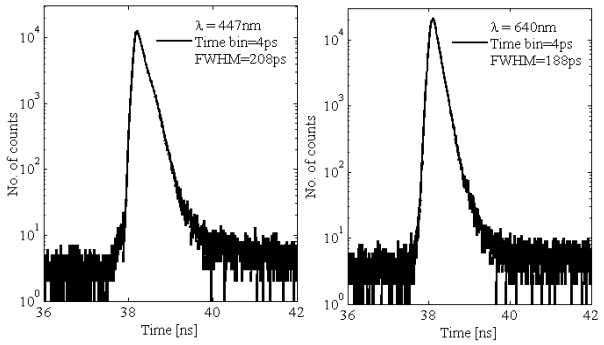

Fig. 10 ToF histograms of D3; Ve = 3V; Room temperature

Additionally we have measured the instrument response function (IRF) for D3 at Ve = 3V at two different wavelengths (Fig. 10).

IV. CONCLUSION

A SPAD with low DCR and high efficiency in the near-IR range has been designed and fabricated in 110nm CIS. A summary of its characteristics can be seen in TABLE I. The proposed device achieves a DCR among the state-of-the-art devices. DCR uniformity and jitter are better for device diameters up to 20µm. Moreover, deeper junctions have the peak PDP shifted towards longer wavelengths. Consequently, PDP improves in near-IR. PDP at 850nm is similar to the latest backside illuminated process [11]. In exchange, the proposed structure features worse jitter, possibly due to a lower intrinsic gain. Nevertheless the aforementioned performances are achieved with 3V excess voltage, without requiring high voltage transistors for the quenching and recharge front-end. The shape of the SPAD has low impact on DCR and jitter for SPADs diameters below 20µm. Therefore a Fermat [6] shape is preferred for better fill factor. Regarding the selected GRs, there are not significant changes in performance at nominal temperature. Nevertheless, wider GRs features better DCR at -20°C.

TABLE I. STATE-OF-THE-ART COMPARISON

	[5]	[8]	[10]	[11]	This work
Tech. [nm]	110 CIS	150 CIS	180nm	65 CIS	110 CIS
SPAD	P+/LDNW(1)	P+/NW	P-epi/BN(2)	PW/DNW	PW/DNW
V_{BD} [V]	20	18	25.5	12	18
Area [µm²] (ϕ)	385(20µm)	97(10µm)	113(12µm)	251(16µm)	78(10µm)
Median DCR [Hz/µm²]	0.18@3V	0.4@3V	0.3@3V	1.6@4.4V	0.4@3V
PDP peak [%] @ Ve, λ	52@6V, 455nm	27@3V, 450nm	33@3V, 480nm	30@4.4V, 660nm	64@3V, 500nm
PDP @ 850nm	5@6V	7.5@5V	9@12V	13@4.4V	10@5V
AP @ Ve, DT	-	0.85@3V, 150ns	7.2@11V, 300ns	0.08@4.4, 8ns	0.5@3V, 5µs
Jitter [ps] @ Ve, λ	80@4V, 831nm	42@4V, 831nm	97@11V 405nm	75 @ 4.4V 700nm	188(3)@3V 640nm

(1)P+/LDNW stands for P+/low doped NW; (2)P-epi/BN stands for P-epi/buried N; (3)It represents the total FHWM jitter

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