Artifact-Aware Analogue/Mixed-Signal Front-Ends for Neural Recording Applications

Norberto Pérez-Prieto, Manuel Delgado-Restituto, Ángel Rodríguez-Vázquez
Instituto de Microelectrónica de Sevillla (IMSE-CNM), CSIC-Universidad de Sevilla (Spain)
Emails: {norberto, mandel, angel}@imse-cnm.csic.es

***Abstract*—This paper presents a brief review of techniques to overcome the problems associated with artifacts in analog front-ends for neural recording applications. These techniques are employed for handling Common-Mode (CM) Differential-Mode (DM) artifacts and include techniques such as Average Template Subtraction, Channel Blanking or Blind Adaptive Stimulation Artifact Rejection (ASAR), among others. Additionally, a new technique for DM artifacts compression is proposed. It allows to compress these artifacts to the requirements of the analog front-end and, afterwards, it allows to reconstruct the whole artifact or largely suppress it.**

***Index Terms*—Neural Recording; Neural prosthesis, Brain Machine Interfaces; Analog Front-End; Artifacts; Artifacts-Aware; Analog Front-Ends; Mixed-signal Front-Ends; Dynamic Range; ASAR;**

I. Introduction

Neural signal recording is an essential function in modern prosthesis for the treatment of neurological disorders such as epilepsy, Parkinson or Alzheimer's disease [1]. Further, neural recorders play also a prominent role in BMIs (Brain-Machine Interfaces) in which conveniently instrumented devices can be solely handled through the information collected and processed from the brain [2]. Some of these applications require the implementation of a closed-loop sensor/actuator mechanism to interact with the brain and, hence, neural recorders have to co-exist with stimulators, often integrated on the same silicon die.

Neural stimulation typically induces strong reactions in the tissue. This not only corrupts the captured neural signals but it may also lead to the saturation of the recording front-end. Hence, in these closed-loop devices, neural recording systems not only should exhibit low noise, low power and low area occupation [1], [3] but they should also render tolerant to the large artifacts generated by the stimulation pulses. Together with neural stimulation, other large interfering signals may also contaminate recording, for instance, by sudden alterations of the tissue-electrode interface due to motions [3], [4]. As long as these interferes have similar effect on the recorded data as stimulation artifacts, in this paper, we will regard both cases as artifacts and simply distinguish between Common-Mode (CM) and Differential-Mode (DM) artifacts, depending on the kind of perturbation received by the neural signal.

Fig. 1 illustrates the amplitude and frequency ranges of neural signals (only Local Field Potentials (LFP) and Action Potentials (AP) are shown) as compared to CM and DM artifacts [3]. As can be seen, while frequencies overlap, amplitude differences may be orders of magnitude different.

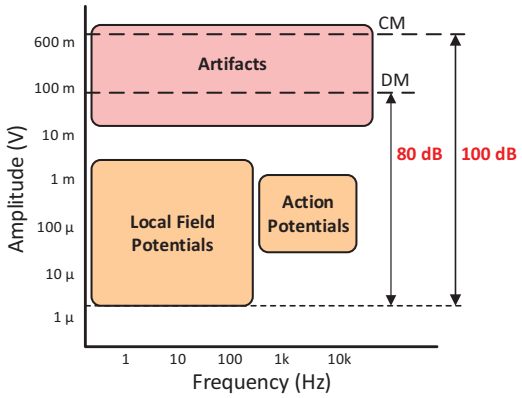

Fig. 1. Specifications of recorded neural signals.

The use of fully-differential structures with large Common-Mode Rejection Ratio (CMRR) allows to reduce the impact of CM artifacts. However, residual CM components in the differential signal path may still degrade system performance. To cope with this problem, continuous- [3] and discrete-time [5] solutions applied at the input of the recording front-end have been proposed. DM artifacts are typically smaller than CM artifacts, however, their effect is more deleterious because they superposes on the neural signal component which conveys useful information. DM artifacts could be handled by increasing the input dynamic range of the neural recorder and raising the resolution of the following ADC so as to convert both neural signals and artifacts. For example, the resolution of an ADC intended for LFP recording should be increased from 10-12 bits to some 14-15 bits if artifacts have to be covered as well [6]. Obviously, this would significantly increase the area and power consumptions of the recording system and, for this reason, other artifact-aware front-end topologies have been recently proposed. In this work, we will make a brief review of these artifact-aware algorithms and structures and analyze their pros and cons. Additionally, we will propose a new algorithm to compress and reconstruct DM artifacts.

The paper is organized as follows. Section II and III present, respectively, some relevant DM artifact-aware and suppression techniques. Section IV proposes a new algorithm for DM artifacts compression and illustrates its performance. Finally,

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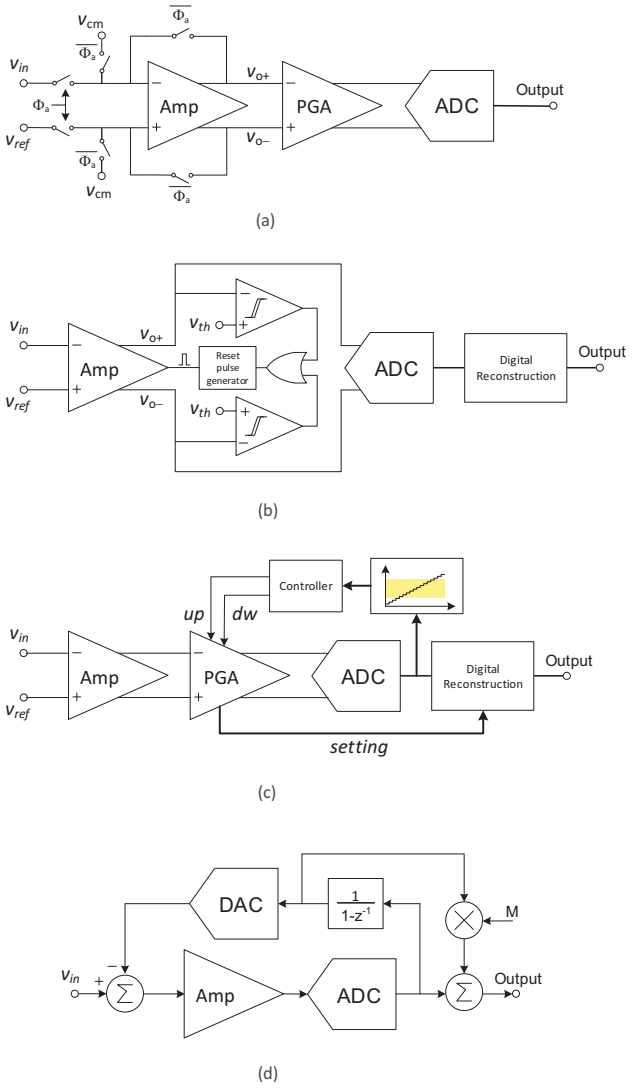

Fig. 2. Artifacts-aware techniques. (a) Channel blanking technique. (b) Signal Folding. (c) PGA tuning. (d) Delta Encoding.

Section V concludes the paper.

II. DM Artifacts-Aware Techniques

Artifact-aware topologies are aimed to relax the performance requirements of the neural recording system in terms of input dynamic range and/or converter resolution even when artifacts contaminate neural signals. Some of these topologies are analyzed below.

A. Channel Blanking

Fig. 2 (a) illustrates the basic structure of the channel blanking technique [7]. The operation principle consists in disconnecting the recording channel from the tissue when an artifact is present. This works when intentional stimulations are applied to the brain but it is useless for unpredictable interferers. Further, the technique carries out a complete loss of information while the recording channel is disconnected. For this reason, data reconstruction with interpolation techniques have been proposed [8]. Another potential problem is the long recovery time after blanking unless proper techniques are adopted [9], [10].

B. Signal Folding

Another technique employed to avoid saturation in the front-end is signal folding [11], [12]. The operation principle is shown in Fig. 2 (b). In this technique, the output voltage of the amplifier is compared with a fixed threshold voltage through a pair of comparators. If the magnitude of the output voltage is higher than this threshold a pulse resets the output node of the front-end amplifier to the nominal common-mode level. This way, saturation is avoided and the ADC requirements are relaxed.

This topology shows two main shortcomings. On the one hand, resetting the amplifier implicitly involves a loss of information. On the other, samples after resetting are invalid due to the slow settling time of the amplifier.

C. PGA Tuning

In order to avoid saturation states due to artifacts, the gain of a programmable gain amplifier (PGA) can be set [1], as shown in Fig. 2 (c). In this technique, a capacitor bank is employed to set the gain of the PGA. The capacitor bank is controlled by a digital circuit which, depending on the amplitude of the signal at the output of the ADC, performs a dynamic adjustment of the amplification. This method allows the signal to fit in the ADC swing. Then, depending on this amplification, the signal is scaled and reconstructed in digital domain.

This method operates for all kind of DM artifacts, as no disabling control is needed, and it may even address other recording problems such as the long-term degradation of the tissue-electrode interface. However, there are two main problems associated with this technique. First, it requires the PGA can be tuned over a wide amplification range, and it increases the complexity of the digital reconstruction circuit, which must scale the ADC output according to the gain value along the signal path. Second, the input-referred noise of the analog front-end and the PGA bandwidth changes with the gain setting.

D. Delta Encoding

Delta Encoding is a technique intended for reducing the ADC dynamic range requirements [5]. The operation principle relies on tracking differences between successive samples at Nyquist rate (delta signals). This inherently places a high-pass pole at half the sampling frequency which compensates the typical 1/f spectral distribution of LFPs [13], thus, reducing the dynamic range requirements of the front-end. Further, large DM artifacts can be tolerated if they are slow enough.

Delta signals are obtained at the input of the front-end amplifier by subtracting the current and previous samples, this latter regenerated through a Digital to Analog Converter (DAC) from digital domain (see Fig. 2 (d)). In order to reconstruct the signal, a scaled version of the DAC input

and the ADC output are added together. The scaling factor M has to be calibrated to compensate for DAC transfer function nonidealities. As a drawback, the amplifier must have a wide bandwidth so that settling is possible between adjacent channels, potentially compromising noise performance due to aliasing and increasing power consumption.

A straightforward extension of Delta Encoding, which follows similar operation principles, relies on sigma-delta modulation and oversampling techniques for increasing the recorder dynamic range [14]. Examples using these topologies can be found in [14]–[17].

III. DM Artifacts-Suppression Techniques

The techniques discussed in the previous section are mainly intended for avoiding saturation in the neural recorders. However, neural activity, if not destroyed, still remains embedded in the artifact. For this reason, techniques able to suppress the artifact and recover the overlapped information are needed. These suppression techniques can use mixed-signal feedback or digital post-processing.

A. Artifacts Suppression Feedback Front-Ends

They are represented in Fig. 3 (a). In this topology, artifact cancellation is performed at the input of the recorder amplifier, thus, avoiding the use of high resolution ADCs. However, this is at the expense of some extra noise contribution by the DAC to the overall input-referred noise of the recorder. To palliate this shortcoming, oversampling techniques can be used [18]. Furthermore, the clock of the circuit has to be fast enough to detect the artifact and inject the correction signal before the artifact saturate the signal path. Two of most significant artifacts suppression feedback techniques are the averaged template subtraction [19] and the adaptive stimulation filter [4].

In the first case, an artifact template is subtracted from the input of the recorder every time a new neural stimulation cycle turns on [19]. The template is calculated by means of a learning algorithm, based on recordings obtained from previous stimulation cycles. After template subtraction, a residual artifact waveform may persist in the signal path. To further enhance the artifact suppression, a post-processing digital circuit can be used to calculate the average amplitude of such residue and subtract it from the signal.

One of the main drawbacks of this approach is the high computational complexity cost and the need for offline training required for both generating the templates and calculating the artifact residues. Further, if there are substantial differences between the artifact and the stored template, the resulting residue can eventually saturate the signal path, unless a wide input range amplifier is used.

In the second case, an adaptive stimulation filter recreates the response of the neural tissue in order to subtract the artifact from the neural signal [4]. The approach takes advantage of the close correlation between the stimulation pulse, $e(t)$, and the neural tissue response, $b(t)$. Denoting by $s(t)$ and $a(t)$

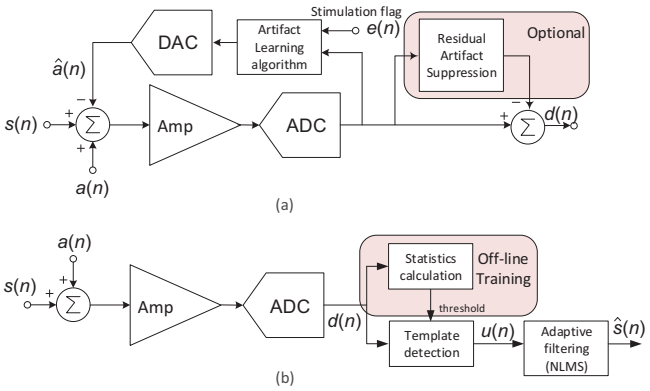

Fig. 3. Artifacts-suppression techniques. (a) Artifacts suppression feedback front-ends. (b) Post-processing artifacts suppression front ends.

the unaffected neural signal and the artifact, respectively, the recorded signal at instant n can be expressed as:

$$y(n) = s(n) + a(n) = s(n) + b(n) * e(n) \tag{1}$$

The objective is to generate a signal $\hat{a}(n) = \hat{b}(n) * e(n)$ such that, when subtracted to the input, gives an estimate

$$\hat{s}(n) = y(n) - \hat{a}(n) = s(n) + [b(n) - \hat{b}(n)] * e(n) \tag{2}$$

close to the original unaffected neural signal. The recreated response $\hat{b}(n)$ can be obtained through an adaptive filter where coefficients are updated by a Least Mean Square (LMS) learning algorithm [4]. This algorithm uses a steepest gradient descent approach to minimize errors in $\hat{s}(n)$. A simplified version of the LMS algorithm, the sign-sign LMS, facilitates hardware implementation by using a sign-bit signal representation as follows [20]:

$$\hat{b}(n) = \hat{b}(n-1) + \mu * [e(n) \times sgn(\hat{s}(n))] \tag{3}$$

B. Post-Processing Artifacts Suppression Front-Ends

In these structures, artifacts are suppressed in digital domain with no feedback to the recorder front-end (Fig. 3 (b)). This avoids any degradation on the noise performance, although, it demands a high dynamic range for the mixed-signal circuitry.

Herein, we will briefly review the blind adaptive stimulation artifact rejection (ASAR) proposed in [6], as a representative example of post-processing cancellation. Interestingly enough, the approach works with any arbitrary artifact with no prior knowledge about its structural and temporal shape. It relies on obtaining an artifact template $u(n)$ from an adjacent electrode. This template is detected when a threshold value, obtained from a previous statistics calculation phase in the absence of artifacts, is exceeded. If an artifact is detected in the recorded signal $y(n)$, the template $u(n)$ is applied to a Normalized Least Mean Square (NMLS) adaptive filter which updates the weighting factor, $w(n)$, as follows:

$$w(n) = w(n-1) + \frac{\mu}{||u(n)||^2 + \epsilon} u(n)^T [y(n) - u(n)w(n-1)] \tag{4}$$

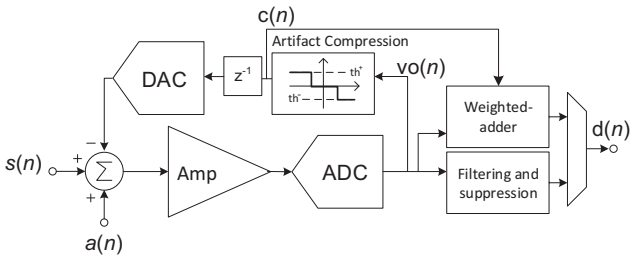

Fig. 4. Architecture of proposed DM artifacts compression technique.

where μ is the algorithm step-size and ϵ is a small positive parameter. To obtain a clean neural signal $\hat{s}(n)$, the estimated artifact is subtracted from the measured signal:

$$\hat{s}(n) = y(n) - u(n)w(n) \tag{5}$$

This approach obtains very fast convergence times and skips any modeling of the brain response in the presence of artifacts [6].

IV. Proposed DM Artifacts Compression Technique

In this section we propose a DM artifact compression technique to relax AFE requirements without losing information, increasing AFE specifications or employing complex algorithms, thus leading to simple on-chip implementation.

The proposed architecture is shown in Fig. 4. The implemented algorithm subtracts discrete voltage values, $c(n)$, from the input of the amplifier when the output of the ADC, $vo(n)$, exceeds certain threshold values, $\pm V_{th}$. This is done to avoid the saturation of the signal path. Voltage increments $c(n)$ are updated every sampling period and are given by:

$$c(n) = \begin{cases} v_{cor}(n-1) & ,|v_o(n)| \leq V_{th} \\ c(n-1) + \alpha \cdot (v_o(n) - V_{th}) & ,v_o(n) > V_{th} \\ c(n-1) + \alpha \cdot (v_o(n) + V_{th}) & ,v_o(n) < -V_{th} \end{cases} \tag{6}$$

where,

$$v_{cor}(n) = \begin{cases} 0 & ,|v_{res}(n)| \leq V_{os} \\ c(n) & ,|v_{res}(n)| > V_{os} \end{cases} \tag{7}$$

$$v_{res}(n) = c(n) - \frac{1}{N} \sum_{j=n-1}^{N-n} c(j) \tag{8}$$

α is a scaling factor which depends on the AFE voltage gain and the DAC resolution, $v_{cor}(n)$ is a corrective term aiming to eliminate any residual offset, $v_{res}(n)$, at the output of the ADC, V_{os} is an upper limit for the tolerated offset, and N is an estimation of the maximum duration of an artifact, expressed in number of samples. $v_{res}(n)$ is continuously calculated, even when $|v_o(n)| > |V_{th}|$.

The original signal can be approximately reconstructed by adding an scaled version of the increments $c(n)$ to the output of the ADC according to the expression: $d(n) = v_o(n) + \beta \cdot c(n-1)$, where β is ideally equal to $1/\alpha$, although deviations can occur due to DAC imperfections. The process is illustrated in Fig. 5 (c).

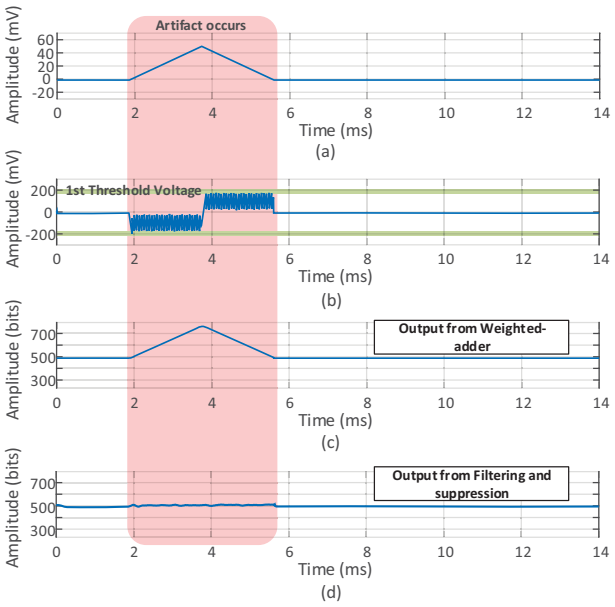

Fig. 5. Simulation results of the proposed technique. (a) Artifact plus signal at the input of the system. (b) Compressed signal at the input of the ADC. (c) Final reconstructed signal. (d) Final suppressed artifact signal.

Given the high frequency oscillations generated along the compression of artifacts, (see Fig. 5 (b)), they can be largely attenuated by using a simple low-pass filter, as can be seen in Fig. 5 (d) in which a 20-tap FIR filter is employed. This obtains an artifact attenuation of 34 dB, similar to other techniques in the literature [4], [19] but with lower hardware complexity.

V. Conclusions

In this paper, a review of analog front-ends techniques for neural recording suitable for attenuating common-mode (CM) and differential-mode (DM) artifacts has been presented. Special attention has been paid on DM artifact-aware techniques because, in this case, interferers overlap the neural signal component which conveys clinically relevant information. After classifying and discussing the pros and cons of some of the most relevant DM artifacts-aware techniques reported in the literature, the paper presents a DM artifact compression algorithm with relaxed requirements on AFE dynamic range and ADC resolution. The proposal is able to reconstruct the signal, including the artifact, or largely suppress the interferer by simple low-pass filtering.

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REFERENCES

[1] M. Delgado-Restituto, A. Rodriguez-Perez, A. Darie, C. Soto-Sanchez, E. Fernandez-Jover, and A. Rodriguez-Vazquez, "System-level design of a 64-channel low power neural spike recording sensor," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 11, no. 2, pp. 420–433, April 2017.

[2] M. Lebedev and A. Nicolelis, "Brain-machine interfaces: past, present and future." *Trends on Neurosciences*, vol. 29, no. 9, pp. 536–546, 2006.

[3] H. Chandrakumar and D. Markovic, "An 80-mVpp linear-input range, 1.6-$g\omega$ input impedance, low-power chopper amplifier for closed-loop neural recording that is tolerant to 650-mvpp common-mode interference," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 11, pp. 2811–2828, Nov 2017.

[4] A. E. Mendrela, J. Cho, J. A. Fredenburg, V. Nagaraj, T. I. Netoff, M. P. Flynn, and E. Yoon, "A bidirectional neural interface circuit with active stimulation artifact cancellation and cross-channel common-mode noise suppression," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 4, pp. 955–965, April 2016.

[5] W. A. Smith, J. P. Uehlin, S. I. Perlmutter, J. C. Rudell, and V. S. Sathe, "A scalable, highly-multiplexed delta-encoded digital feedback ecog recording amplifier with common and differential-mode artifact suppression," in *2017 Symposium on VLSI Circuits*, June 2017, pp. C172–C173.

[6] S. Basir-Kazeruni, S. Vlaski, H. Salami, A. H. Sayed, and D. Markovi, "A blind adaptive stimulation artifact rejection (asar) engine for closed-loop implantable neuromodulation systems," in *2017 8th International IEEE/EMBS Conference on Neural Engineering (NER)*, May 2017, pp. 186–189.

[7] T. L. Babb, E. Mariani, G. Strain, J. P. Lieb, H. Soper, and P. H. Crandall, "A sample and hold amplifier system for stimulus artifact suppression," *Electroencephalography and Clinical Neurophysiology*, vol. 44, no. 4, pp. 528–531, 1978.

[8] A. Zhou, S. Santacruz, B. Johnson, G. Alexandrov, A. Moin, F. Burghardt, J. Rabaey, J. Carmena, and R. Muller, "A 128-channel, closed-loop, wireless artifact-free neuromodulation device," *arXiv:1708.00556*, 2017.

[9] B. C. Johnson, S. Gambini, I. Izyumin, A. Moin, A. Zhou, G. Alexandrov, S. R. Santacruz, J. M. Rabaey, J. M. Carmena, and R. Muller, "An implantable 700w 64-channel neuromodulation ic for simultaneous recording and stimulation with rapid artifact recovery," in *2017 Symposium on VLSI Circuits*, June 2017, pp. C48–C49.

[10] Y. Jimbo, N. Kasai, K. Torimitsu, T. Tateno, and H. P. C. Robinson, "A system for mea-based multisite stimulation," *IEEE Transactions on Biomedical Engineering*, vol. 50, no. 2, pp. 241–248, Feb 2003.

[11] W. Tang and E. Culurciello, "A pulse-based amplifier and data converter for bio-potentials," in *2009 IEEE International Symposium on Circuits and Systems*, May 2009, pp. 337–340.

[12] Y. Chen, A. Basu, L. Liu, X. Zou, R. Rajkumar, G. S. Dawe, and M. Je, "A digitally assisted, signal folding neural recording amplifier," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 8, no. 4, pp. 528–542, Aug 2014.

[13] S. Y. Park, J. Cho, K. Lee, and E. Yoon, "Dynamic power reduction in scalable neural recording interface using spatiotemporal correlation and temporal sparsity of neural signals," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 4, pp. 1102–1114, April 2018.

[14] H. Kassiri, M. T. Salam, M. R. Pazhouhandeh, N. Soltani, J. L. P. Velazquez, P. Carlen, and R. Genov, "Rail-to-rail-input dual-radio 64-channel closed-loop neurostimulator," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 11, pp. 2793–2810, Nov 2017.

[15] L. B. Leene and T. G. Constandinou, "A 0.016 mm2 12 b $\delta\sigma$ sar with 14 fj/conv. for ultra low power biosensor arrays," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 10, pp. 2655–2665, Oct 2017.

[16] E. Greenwald, E. So, Q. Wang, M. Mollazadeh, C. Maier, R. Etienne-Cummings, G. Cauwenberghs, and N. Thakor, "A bidirectional neural interface ic with chopper stabilized bioadc array and charge balanced stimulator," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 10, no. 5, pp. 990–1002, Oct 2016.

[17] C. Chen, J. Crop, J. Chae, P. Chiang, and G. C. Temes, "A 12-bit 7 w/channel 1 khz/channel incremental adc for biosensor interface circuits," in *2012 IEEE International Symposium on Circuits and Systems*, May 2012, pp. 2969–2972.

[18] R. Muller, H. P. Le, W. Li, P. Ledochowitsch, S. Gambini, T. Bjorninen, A. Koralek, J. M. Carmena, M. M. Maharbiz, E. Alon, and J. M. Rabaey, "A minimally invasive 64-channel wireless ecog implant," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 1, pp. 344–359, Jan 2015.

[19] S. Culaclii, B. Kim, Y. Lo, and W. Liu, "A hybrid hardware and software approach for cancelling stimulus artifacts during same-electrode neural stimulation and recording," in *2016 38th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC)*, Aug 2016, pp. 6190–6193.

[20] S. Dasgupta, C. R. Johnson, and A. M. Baksho, "Sign-sign lms convergence with independent stochastic inputs," *IEEE Transactions on Information Theory*, vol. 36, no. 1, pp. 197–201, Jan 1990.