

A 0.18 μm CMOS Low Noise, Highly Linear Continuous-Time Seventh-Order Elliptic Low-Pass Filter

Juan F. Fernández-Bootello*, Manuel Delgado-Restituto and
Angel Rodríguez-Vázquez

Instituto de Microelectrónica de Sevilla, IMSE-CNM (CSIC)
Edificio CICA-CNM, Avda Reina Mercedes s/n, 41012-Sevilla, SPAIN
emails: {bootello|mandel|angel@imse.cnm.es}

ABSTRACT

This paper presents a fast procedure for the system-level evaluation of noise and distortion in continuous-time integrated filters. The presented approach is based on Volterra's series theory and matrix algebra manipulation. This procedure has been integrated in a constrained optimization routine to improve the dynamic range of the filter while keeping the area and power consumption at a minimum.

The proposed approach is demonstrated with the design, from system- to physical-level, of a seventh-order low-pass continuous-time elliptic filter for a high-performance broadband power-line communication receiver. The filter shows a nominal cut-off frequency of $f_c = 34\text{MHz}$, less than 1dB ripple in the pass-band, and a maximum stop-band rejection of 65dB. Additionally, the filter features 12dB programmable boost in the pass-band to counteract high frequency components attenuation. Taking into account its wideband transfer characteristic, the filter has been implemented using G_m -C techniques. The basic building block of its structure, the transconductor, uses a source degeneration topology with local feedback for linearity improving and shows a worst-case intermodulation distortion of -70 dB for two tones close to the passband edge, separated by 1MHz, with 70mV of amplitude.

The filter combines very low noise (peak root spectral noise density below $56\text{nV}/\sqrt{\text{Hz}}$) and high linearity (more than 64dB of MTPR for a DMT signal of $0.5V_{pp}$ amplitude) properties. The filter has been designed in a $0.18\mu\text{m}$ CMOS technology and it is compliant with industrial operation conditions (-40 to 85°C temperature variation and $\pm 5\%$ power supply deviation). The filter occupies 13mm^2 and exhibits a typical power consumption of 450 mW from a 1.8V voltage supply.

Keywords: Low-noise, Continuous-Time Filters, G_m -C Filters, CAD tools for VLSI

1. INTRODUCTION

Filters are essential blocks in communications systems to reject undesired signals which may be orders of magnitude larger than the desired one. Hence, the design of these filters need a special attention in the design of such communication systems. There are many factors which degrade the behaviour of monolithic filters. One key figure of merit which measures such degradation is the dynamic range (DR) of the circuit, which can be defined as the ratio among the maximum signal power level (for a given distortion at the output) which can be processed by the filter and the in-band integrated noise power^{1,2}. It can be demonstrated that the DR is directly related with the power consumption of the filter³. Thus, from a design perspective, the availability of fast procedures for the early system-level evaluation of noise and distortion in filters which takes into account imperfections of circuit elements is essential.

In this paper, we present a simple procedure for the evaluation of noise and distortion of continuous-time G_m -C filters, with no need of lengthy transient analysis. In particular, distortion is measured using Volterra's series theory⁴, and the evaluation of dynamic range can be done by simple matrix algebra, amenable for computer programming. Taking advantage of this fact, a constrained optimization routine has been implemented in MATLAB[®] which maximizes the dynamic range of a given topology while reducing the area and power consumptions of the filter⁵.

As a demonstration of the proposed approach, the design, from system- to physical-level, of a seventh-order low-pass continuous-time elliptic filter for a high-performance broadband power-line communication receiver is also described.

Main specifications of the filter are 34 MHz of cut-off frequency, more than 40dB of stopband rejection (corner at 46 MHz), less than 1dB ripple in the passband, and programmable boosting from 0 to 12dB at 2dB steps. Together, severe specifications on noise and distortion performance are also demanded. Namely, the filter must exhibit less than $60\text{nV}/\sqrt{\text{Hz}}$ of peak root spectral density in the passband, and more than 60dB of MTPR for different patterns of DMT signals of $0.5V_{pp}$ amplitude.

The paper is structured as follows. In Sec. 2, a general representation of G_m -C filters using matrices, which is at the basis of the aforementioned approach, is first described. Then, the procedures to compute the harmonic and/or inter-modulation distortion of weakly non-linear systems, as well as their noise contributions are detailed. Next, Sec. 3 describes the approach for the optimization of the dynamic range of G_m -C filters. Sec. 4 shows the system-level design of the filter used as demonstration vehicle of the proposed procedure. Sec. 5 focuses on the transconductor block, as the main building element of the architecture, and Sec. 6 shows the circuitry used for tuning. Finally, Sec. 7 presents simulations of the filter and transconductor block, and Sec. 8 gives some concluding remarks.

2. G_m -C FILTER REPRESENTATION AND EVALUATION TECHNIQUES

As noted above, in order to estimate the dynamic range of a filter, both distortion and noise must be properly evaluated. In this section, the mathematical rudiments for a fast estimation of such performances are presented.

In general, any linear continuous-time filter can be formulated by the following extended state-space representation,

$$\begin{aligned} \mathbf{E} \frac{d\mathbf{x}}{dt} &= \mathbf{A}\mathbf{x} + \mathbf{B}E_i \\ E_o &= \mathbf{C}\mathbf{x} + DE_i \end{aligned} \quad (1)$$

where \mathbf{A} , \mathbf{B} , \mathbf{C} and \mathbf{E} are matrices, D is a scalar, E_i is the input signal E_o is the output signal and $\mathbf{x} = [x_1 \dots x_n]^\dagger$ is the vector which represents the internal nodes. Expressing (1) in the frequency domain, the transfer function of the filter takes the form,

$$H(s) = \frac{E_o(s)}{E_i(s)} = \mathbf{C}(\mathbf{E}s - \mathbf{A})^{-1}\mathbf{B} + D \quad (2)$$

In the case of G_m -C filter structures based on simple integrators (as those in Fig.1), matrix \mathbf{E} in (1) represents capacitances, and matrix \mathbf{A} and \mathbf{B} transconductances. These matrices can be built-up from LC ladder equivalent filters as shown in ^{5,6}.

Now assume that the filter is composed by weakly non-linear fully-differential transconductors. In this case the transfer characteristic of the transconductor (neglecting second-order terms) can be described as

$$i = G_{mo}v(1 + a_3v^2) \quad (3)$$

where a_3 is a third-order non linearity coefficient. Using (3), equation (1) becomes

$$\begin{aligned} \mathbf{E} \frac{d\mathbf{x}}{dt} &= \mathbf{A}\mathbf{x} + a_3\mathbf{A}\mathbf{x}^3 + \mathbf{B}E_i + \mathbf{B}E_i^3 \\ E_o &= \mathbf{C}\mathbf{x} + DE_i \end{aligned} \quad (4)$$

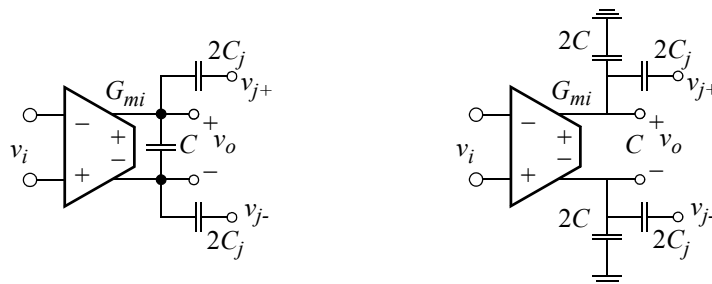


Figure 1. First order section using conventional transconductors.

From this expression, and using Volterra's series theory, the response of the intermediate nodes to an input $E_i(t)$ can be expressed as⁴

$$\mathbf{x}(t) = H_1(E_i(t)) + H_3(E_i(t)) \quad (5)$$

where

$$H_i(E_i(t)) = \int_{-\infty}^{\infty} \dots \int_{-\infty}^{\infty} h_i(\tau_1 \dots \tau_i) E_i(t - \tau_1) \dots E_i(t - \tau_i) d\tau_1 \dots d\tau_i \quad (6)$$

is the i -th order Volterra operator and $h_i(\cdot)$ is the i -th Volterra Kernel. The Laplace transformation of such multidimensional kernel is defined by

$$H_i(s_1, \dots, s_n) = \int_{-\infty}^{\infty} \dots \int_{-\infty}^{\infty} h_i(\tau_1 \dots \tau_i) e^{-(s_1 \tau_1 + \dots + s_n \tau_n)} d\tau_1 \dots d\tau_n \quad (7)$$

where s_i is the Laplace variable in the i -th dimension. Thus for example $H_3(s_1, s_2, s_3)$ describes the third-order behaviour of the system. These transformed Kernels can be evaluated using the following expressions

$$\frac{H_1(s_1)}{E_i} = (\mathbf{E}s - \mathbf{A})^{-1} \mathbf{B} \quad (8)$$

$$\frac{H_3(s_1, s_2, s_3)}{E_i^3} = (\mathbf{E}(s_1 + s_2 + s_3) - \mathbf{A})^{-1} a_3 (\mathbf{A}H_1(s_1)H_1(s_2)H_1(s_3) + \mathbf{B}^3) \quad (9)$$

Thus the distortion or inter-modulation of the filter can be computed at the system level, with no need of transient analysis, using

$$HD_3(\omega) = \frac{1}{4} \frac{\mathbf{C}H_3(j\omega, j\omega, j\omega)}{\mathbf{C}H_1(j\omega)} \rho^2 \quad (10)$$

$$IM_3(2\omega_1 \pm \omega_2) = \frac{3}{4} \frac{\mathbf{C}H_3(j\omega_1, j\omega_1, \pm j\omega_2)}{\mathbf{C}H_1(j\omega_1)} \rho^2$$

where ρ is the amplitude of the tones at the input of the system. Note from (9) that the distortion depends on the magnitude of the internal nodes of the filter and, hence, it can be reduced by decreasing the voltage level of such nodes.

On the other hand, the noise contribution of a transistor with transconductance G_m can be modelled by an output referred current source with power spectral density $S_{in} = 4kT\xi G_m$, where ξ is the noise excess factor of the transistor³. From this, the noise spectral density of a filter can be expressed as³

$$S_G(f) = \sum_i \sum_l 4kT\xi G_{mli} |g_i|^2 \quad (11)$$

where g_i is the transfer function from the output of transistor G_{mli} to the output of the filter, and i and l denote the output and input nodes of the transistor, respectively. By grouping the transfer functions g_i in a vector \mathbf{G} ,

$$\mathbf{G} = [g_1 \ g_2 \ \dots \ g_n]^\dagger \quad (12)$$

it can be easily found that,

$$\mathbf{G} = \mathbf{C}(s\mathbf{E} - \mathbf{A})^{-1} \quad (13)$$

Thus, the output referred mean-squared noise of the filter can be evaluated as

$$N_{Total} = \int_0^{\infty} S_G(f) df = \sum_i N_{oi} \quad (14)$$

where N_{oi} represents the noise contribution from the i -th internal node to the output. Note that N_{oi} depends inversely on the total transconductance connected at the corresponding node and, hence, it can be reduced increasing the total transconductance and, hence, the capacitance connected at this node.

3. G_m -C FILTER OPTIMIZATION

Filter optimization can be seen as a constrained minimization problem in which the current consumption of the structure must be reduced as much as possible while satisfying both the objective transfer characteristic of the filter and its prescribed dynamic range, which can be estimated from (10) and (14). This implies to modifying the system representation in (1) by an optimum scaling of the filter. By means of scaling, the original matrix representation of the filter is transformed according to the algebraic mappings

$$\begin{aligned} \mathbf{A} &\rightarrow \mathbf{N}(\mathbf{TAT}^{-1}) \\ \mathbf{B} &\rightarrow \mathbf{NTB} \\ \mathbf{C} &\rightarrow \mathbf{CT}^{-1} \\ \mathbf{E} &\rightarrow \mathbf{N}(\mathbf{TET}^{-1}) \end{aligned} \quad (15)$$

where \mathbf{T} is a similarity matrix which scales the magnitude level of the internal nodes of the filter, and \mathbf{N} is a matrix which modifies the noise contribution from each internal node of the circuit to the output. An optimizer based on the simulated-annealing algorithm has been used to identify the optima \mathbf{T} and \mathbf{N} matrices. As initial guess for the \mathbf{T} matrix in the simulated annealing algorithm, the L_∞ or L_2 scaling norm can be used¹. Similarly, the initial point for the \mathbf{N} matrix can be that which obtains the same noise contributions from the internal nodes to the filter output per unit bias current⁷.

Both the filter performance evaluation routines and the optimization engine have been integrated in the MATLAB/SIMULINK[®] platform. This brings numerous advantages in terms of signal processing, high flexibility for tool expansion and simulation with other electronic subsystems.

4. FILTER DESIGN

Using the approach and tools described above, a seventh order elliptic low pass G_m -C filter has been designed. Owing to the superior performance of doubly terminated LC ladder filter structures with regard to its low sensitivity to components variation, their emulation by active circuits very often constitute the candidates of choice for silicon realization³, so this emulation has been chosen to design the filter.

In the optimization process the transconductor has been assumed to have a third-order non-linearity coefficient of $a_3 = 0.006\text{V}^{-2}$, a noise excess factor of $\xi = 10$ and a power efficiency $G_m/I = 0.3\text{V}^{-1}$ at a voltage supply of 1.8 V. The optimization problem has consisted on minimizing the cost function.

$$Cost = IM_3 \times N_{Total} \quad (16)$$

where IM_3 is the third-order intermodulation of the filter and N_{Total} is the total output-referred noise power, under the constrain of keeping the power consumption below 350mW.

Fig.2 shows the comparison of the intermodulation ($IM_3(2\omega_2 - \omega_1)$), the third order distortion (HD_3) and the spectral noise density of filter before and after the optimization process. It also illustrates that the method based on transient analysis (circles) match up with the Volterra's one. For the distortion estimation it has been considered that the tones have an amplitude of $A = 140\text{mV}_{pp}$ and are separated 1 MHz.

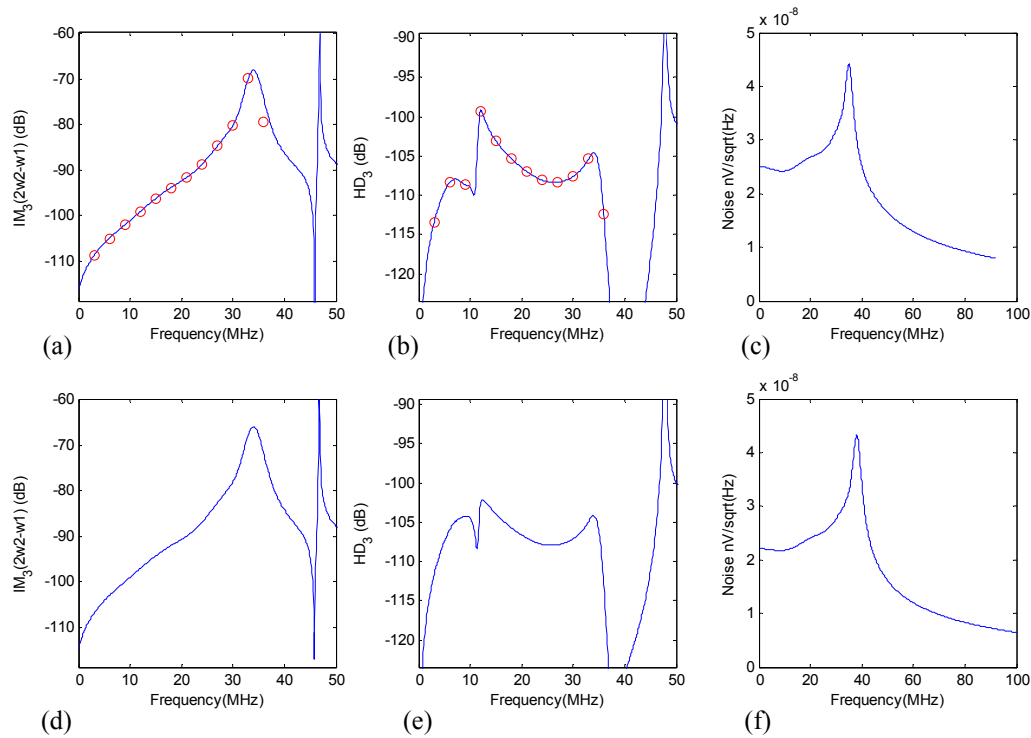


Figure 2. Intermodulation, third order distortion and noise of the non optimized filter for: (a-c) non optimized filter and (d-f) optimized filter

Table 1: characteristics of the system level filter before and after the optimization

	IM_3	HD_3	Total capacitance (pF)	Noise μV_{rms}
Non optimized	-68 dB	-99 dB	270	160
Optimized	-66 dB	-102dB	195	147

Table 1 summarizes the results obtained before and after the optimization process. It shows that for the same power consumption, the total noise and capacitance have been reduced a 9% and 18% respectively.

Fig.3 shows the simplified schematic of the filter, where transconductors G_B provide the required boosting to correct the high frequencies attenuation of the transmission channel. Table 2 and Table 3 show the number of unitary transconductors and the value of capacitors of the optimized filter.

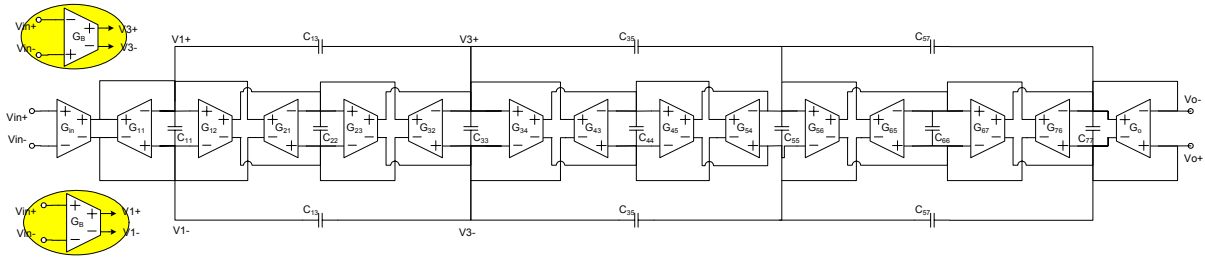


Figure 3. Simplified schematic of the filter. Programmable feedforward transconductors G_B at the insets provide transfer boosting at high frequencies.

Table 2: Number of unitary elements per transconductor.

G_{in}	G_{11}	G_{12}	G_{21}	G_{32}	G_{23}	G_{43}	G_{34}
16	16	16	16	10	16	24	12
G_{54}	G_{45}	G_{65}	G_{56}	G_{76}	G_{67}	G_{77}	
9	18	18	9	6	12	4	

Table 3: Filter capacitances.

C_{11}	C_{22}	C_{33}	C_{44}	C_{55}
34.9 pF	26.1 pF	59.7 pF	44.2 pF	29.6 pF
C_{66}	C_{77}	C_{13}	C_{35}	C_{57}
29.6 pF	31.2 pF	3.68 pF	14.02 pF	13.85 pF

5. TRANSCONDUCTOR

Fig.4(a) shows the schematic of the transconductor employed in the filter. Transistors M1, M3 and M2, M4 (enhanced by the feedback action of M5, M7 and M6, M8, respectively) ideally transfer with unity gain the input voltage of the transconductor to the pair of nominally identical degeneration resistors R1 and R2. The generated incremental current, which is ideally proportional to the input voltage as long as resistors R1 and R2 are perfectly linear, flows through the loop formed by transistors M5-M8 and it is replicated at the output by M9-M12. It can be found that the transconductance amounts

$$G_m = \frac{g_{m9}}{g_{m5}} \left[\frac{A g_{m1}}{1 + A g_{m1} R} \right] \approx \frac{g_{m9}}{g_{m5}} \cdot \frac{1}{R} \quad (17)$$

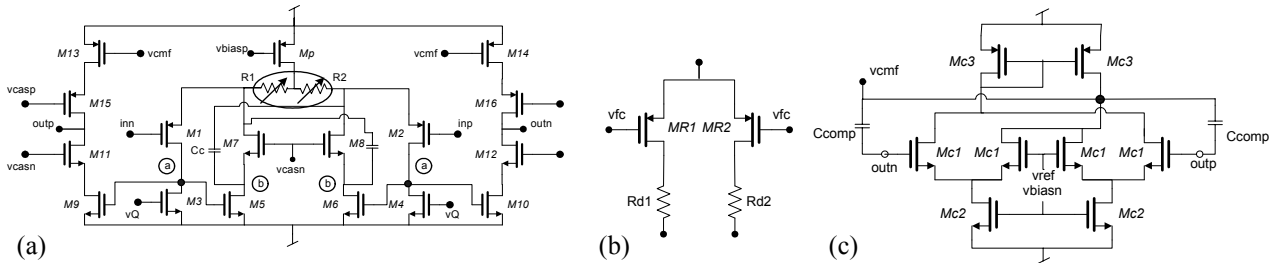


Figure 4. (a) Schematic of the transconductor; (b) tunable resistor; and (c) common-mode feedback circuit.

where g_{mj} is the transconductance of transistor Mj, R is the resistance of R1 and R2, and A is the gain of the amplifier composed by M1 and M3

$$A = \frac{g_{m1}}{g_{ds1} + g_{ds3}} \quad (18)$$

and g_{dsj} is the output conductance of transistor Mj. Approximation in (17) applies for large enough A values and reveals that the transconductance is inversely proportional to the degeneration resistance and can be scaled by the aspect ratio of transistors M9-M5 (or M10-M4). On the other hand, the non-linearity of the transconductor can be modelled, assuming perfect matching among equivalent elements, by a third order non-linearity coefficient given by

$$a_3 = \frac{1}{8} \left(\frac{1}{A g_{m1} R^3 I^2} \right) \quad (19)$$

where I is the current provided by the tail transistor Mp. According to (19), in order to reduce IM_3 for a given transconductance, I and/or A must be increased. Whatever design strategy is used for improving linearity care must be taken to not severely degrade the current efficiency of the transconductor or its high-frequency performance (parasitics at nodes (a) must be kept low). Taking into account those parasitics (18) is transformed as follows

$$A = \frac{g_{m1}}{g_{ds1} + g_{ds3} + sC_a} = \frac{A_o}{s/\omega_a + 1} \quad (20)$$

where C_a and ω_a are the capacitance and the pole associated to the nodes (a) and A_o is the low frequency gain of the amplifier. On the other hand, considering the frequency characteristics of such amplifier, the third order non-linearity coefficient becomes

$$a_3 = \frac{1}{8} \left(\frac{1}{A_o g_{m1} R^3 I^2} \right) \left(1 + \frac{s_1 + s_2 + s_3}{\omega_a} \right) \quad (21)$$

Resistors R1 and R2 are implemented as shown in Fig.4(b), where transistors MR1 and MR2 are operated in the ohmic region by means of the analogue control signal v_{fc} . This allows to continuously vary the resistance R (and thereafter, the transconductance G_m), what is exploited to correct variations in the cut-off frequency of the filter, as explained later on.

In the structure of the Fig.4 (a), the noise excess factor ξ is given by,

$$\xi = \frac{2}{3} \left(g_{m9} + g_{m5} + g_{m13} \frac{g_{m9}}{g_{m5}} \right) R + \frac{g_{m9}}{g_{m5}} \quad (22)$$

and, hence, it can be reduced, for a given G_m value, by lowering the transconductances of M5, M9 and M13. This can be done by increasing their overhead voltages, taking into account the limited power supply (1.8V) and speed requirements.

A small-signal analysis of Fig.4 (a) reveals that the structure presents poles and zeros approximately given by

$$\omega_{p1} \approx \frac{g_{m7}}{C_b} \quad \omega_{p2} \approx \frac{g_{m11}}{C_d} \quad \omega_{p3} \approx \frac{g_{m1} g_{m5}}{C_a G} \quad \omega_z \approx \frac{G}{C_c} \quad (23)$$

where C_a , C_b , C_d are the capacitances associated to corresponding nodes in Fig.4 (a), and C_c is a compensation capacitor which aims to counteract the phase lag produced by the poles. Note from (22) and (23), that by decreasing g_{m5} the noise excess factor is reduced but the frequency response of the transconductor worsens. Thus, there is a trade-off between speed and noise. Phase response of the transconductor can be modified (Q-tuned) by controlling the current through transistors M1, M3 (and M2, M4), using terminal v_Q .

Fig.4 (c) shows the common-mode feedback circuit of the transconductor. Indeed, this circuit is shared by all the paralleled transconductors connected to the same nodes of the filter in Fig.3. To avoid stability problems, two compensation capacitors connect the output nodes of the transconductors to the control node, v_{cmf} . These capacitors must be subtracted from the integrating node.

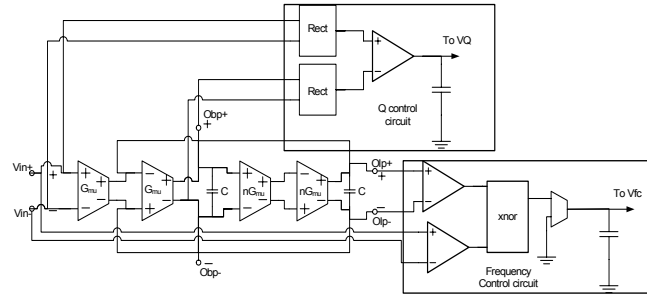


Figure 5. Tuning circuit.

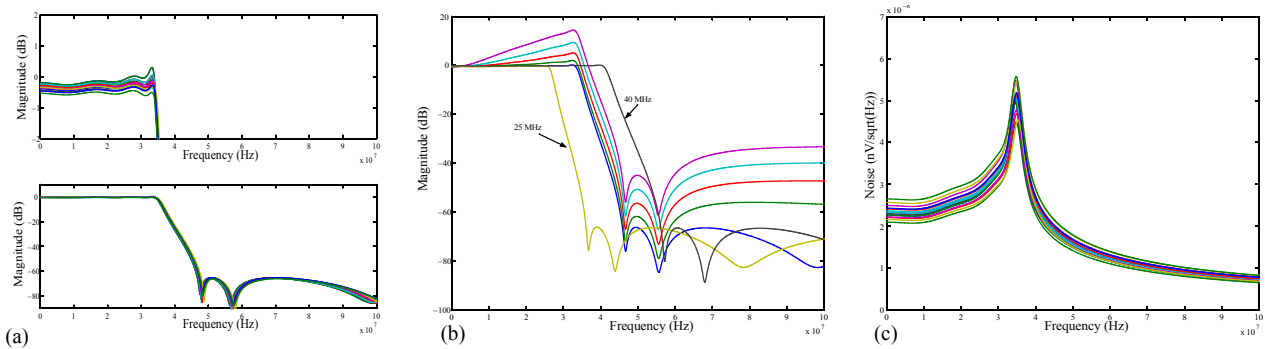


Figure 6. a) AC characteristics of the filter. b) Programmability of the filter. and c) Power spectral density of noise.

6. TUNING CIRCUIT

Fig.5 shows the circuitry used to tune the cut-off frequency and quality factor of the (slave) filter of Fig.3. It is based on a voltage-controlled biquad (master) externally driven by a precise clock reference. Transconductors in the master and slave filter are matched and controlled by the same tuning variables obtained from the circuit of Fig.5. At the angular frequency $\omega_c = nG_{mu}/C$, the band-pass output voltage of the biquad (labelled obp in Fig.5) is in phase with the input and have the same amplitudes. At the same frequency, the low-pass output voltage of the biquad (labelled olp in Fig.5) also shows the same amplitude than the external reference, but they are in quadrature. By comparing the phase of olp with that of the external clock, and integrating the error signal in a capacitor, the feedback loop determines a control voltage v_{fc} such that the transconductance becomes $G_{mu} = (2\pi/n)f_{clk}C$, where f_{clk} is the frequency of the external reference. Because integrating capacitors in the biquad and the slave filter are also matched, the feedback loop allows to define the cut-off frequency of the filter in terms of f_{clk} . Similarly, by comparing the amplitude of obp and the external reference and integrating the errors in a capacitor, the feedback loop determines a control voltage v_Q that tunes the quality factor of the slave filter. The biquad has a quality factor $Q = n = 8$, which is close to the worst case Q of the poles of the filter.

7. SIMULATIONS RESULTS

Fig.6 (a) shows the AC characteristics of the filter in the main corners of the technological process. Fig.6 (b) shows its programmability (changing the cut-off frequency and providing boost) and Fig.6 (c) shows its spectral density of noise.

To simulate the distortion of the filter, it has been excited with two tones of 140 mV_{pp} of amplitude separated 1 MHz. Fig.7 shows its HD_3 and IM_3 when the frequency is swept in the range of interest. Also shows that the simulated results fit with the theoretic ones predicted by Volterra's series theory using the third order non linearity coefficient described in (21) and using the model in (14) and (15). Fig.8 (a) shows the intermodulation of the transconductor in the same conditions like

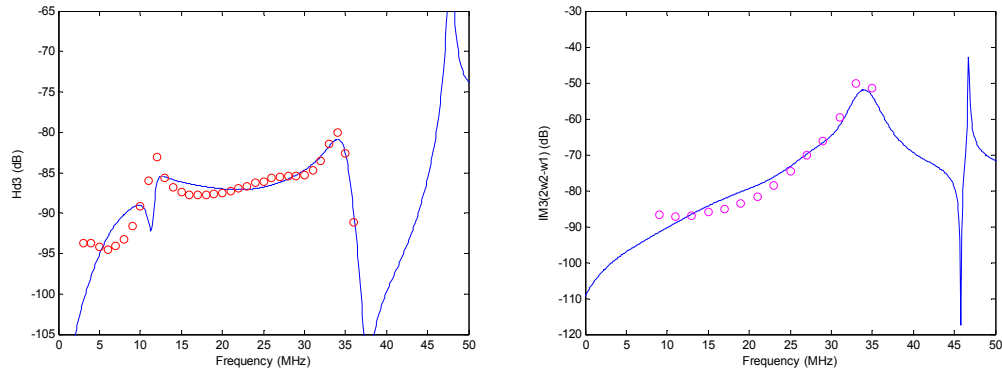


Figure 7. (a) HD_3 and (b) IM_3 of the filter and its approximation using Volterra's series method.

the filter. It shows that the linearity decreases when the frequency increases like predicts (21). Fig.8 (b) shows the response of the filter to a digital multi-tone (DMT) input of 500 mV_{pp} of amplitude and bandwidth from 2 to 34 MHz. As can be seen, the multi-tone power ratio (MTPR) is 64 dB.

In order to compare the filter with others in the literature, the third order distortion (HD_3) has been simulated with an input frequency of 5 MHz to have the same conditions of simulations that theirs, i.e with an input frequency approximately a sixth of the cut-off frequency. In this conditions the filter achieves a HD_3 of -49 dB @ 1.2 V_{pp} differential input thus showing a DR of 69 dB. Table 4 shows the main characteristics of the compared filters where FOM denotes the power per pole per edge frequency³. Fig. 8 (c) shows the FOM vs DR of those filters where the filter proposed is in the best adjustment line.

8. CONCLUSIONS

Design considerations and simulated results of a seventh order elliptic, low-pass G_m -C filter have been presented. The filter has low noise (less than $56\text{ nV}/\sqrt{\text{Hz}}$ power spectral density of noise) and high linearity (-49 dB for a 1.2 V_{pp} @ 5 MHz input). It consumes 450 mW and occupies 13 mm² in a 0.18 CMOS technology @ 1.8 V.

Also, techniques to evaluate and minimize the noise and distortion at the system level have been presented. This techniques allow to maximize the DR and are based on simple matrix manipulation and Volterra's series theory.

ACKNOWLEDGMENT

This work has been partially funded by the spanish MCyT under Project TIC2003-02355 (RAICONIF).

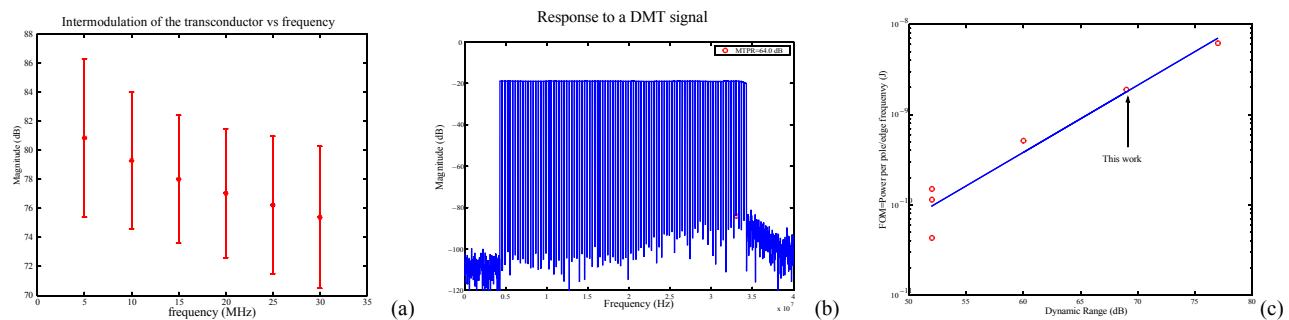


Figure 8. a) Intermodulation of the transconductor vs frequency. b) Response of the filter to a DMT signal. and c) Comparison of several filter design.

Table 4: Comparison of several filter designs

Reference	Silva ⁸	Chen ⁹	Mehr ¹⁰	Yang ¹¹	Rezzi ¹²	This work
Technology	0.35 CMOS	0.35 CMOS	0.6 CMOS	BiCMOS	BiCMOS	0.18 CMOS
Order	7	4	7	7	7	7
Power supply (V)	3.3	2.3	5	2.5	5	1.8
Edge frequency	200 MHz	150 MHz	25 MHz	600 KHz	50 MHz	34 MHz
HD ₃ (dB)	-44 @ 500 mV _{pp} f _{in} =30 MHz	-44 @ 2 V _{pp} f _{in} =20 MHz	-40 @ 640 mV _{pp} f _{in} =2 MHz	-49 @ 2 V _{pp} f _{in} =100 KHz	-40 @ 700 mV _{pp}	-49 @ 1.2 V _{pp} f _{in} = 5 MHz
Noise rms	397 μV	1.69 mV	-	198 μV	650 μV	155 μV
DR (dB)	51	52	60	77	52	69
Power (mW)	60	90	60	26	40	450
FOM (J)	4, 29x10 ⁻¹¹	1, 50x10 ⁻¹⁰	5, 14x10 ⁻¹⁰	6, 19x10 ⁻⁹	1, 14x10 ⁻¹⁰	1, 89x10 ⁻⁹

REFERENCES

1. G.Groenewold."The Design of High Dynamic Range Continuous-Time Integratable Bandpass Filters", IEEE Transactions on Circuits and Systems, Vol.38, pp. 838-852, Aug 1991.
2. G. E. Efthivoulidis, L. Tóth, Y. P. Tsvividis. "Noise in Gm-C Filters", IEEE Transactions on Circuits and Systems-II, Vol. 45, pp. 295-302, Marc 1998.
3. Y. P. Tsvividis, and J.O. Voorman, Integrated Continuous-time Filters, IEEE Press, New York, 1993.
4. M.Schetzen, The Volterra and Wiener theories of nonlinear systems, Malabar, Florida, Krieger, 1980
5. J.F. Fernández-Bootello, M. Delgado-Restituto, A. Rodríguez-Vázquez, "System-Level Optimization of Baseband Filters for Communication Applications". Microtechnologies for the New Millennium 2003, Maspalomas, Spain, May 2003.
6. N.P.J. Greer, R.K. Henderson, L. Ping J.I. Sewell. "Matrix methods for the design of transconductors ladder filters", IEE Proc.-Circuits Devices Sys., Vol.141, pp. 89-100, Apr 1994.
7. F. Behbahani, W. Tan, A. Karimi-Sanjaani, A. Roithmeier, and A. A. Abidi, "A broad-band tunable CMOS channel-select filter for a low-IF wireless receiver," *Solid-State Circuits, IEEE Journal of*, Vol. 35, Iss. 4, pp. 476-489, 2000.
8. J. Silva-Martinez et al. "A 60-mW 200-MHz continuous-time seventh-order linear phase filter with on-chip automatic tuning system," *Solid-State Circuits, IEEE Journal of*, Vol. 38, Iss. 2, pp. 216-225, 2003.
9. M. Chen et al. "A 2-V/sub pp/ 80-200-MHz fourth-order continuous-time linear phase filter with automatic frequency tuning," *Solid-State Circuits, IEEE Journal of*, Vol. 38, Iss. 10, pp. 1745-1749, 2003.
10. I. Mehr and D. R. Welland, "A CMOS continuous-time Gm-C filter for PRML read channel applications at 150 Mb/s and beyond," *Solid-State Circuits, IEEE Journal of*, Vol. 32, Iss. 4, pp. 499-513, 1997.
11. F. Yang and C. C. Enz, "A low-distortion BiCMOS seventh-order Bessel filter operating at 2.5 V supply," *Solid-State Circuits, IEEE Journal of*, Vol. 31, Iss. 3, pp. 321-330, 1996.
12. F. Rezzi et al. "A 70-mW seventh-order filter with 7-50 MHz cutoff frequency and programmable boost and group delay equalization," *Solid-State Circuits, IEEE Journal of*, Vol. 32, Iss. 12, pp. 1987-1999, 1997.