CORA Cork Open Research Archive
Cartlann Taighde Oscailte Chorcaí

UCC Library and UCC researchers have made this item openly available. Please let us know how this has helped you. Thanks!

Title	Integrated silicon photonic packaging
Author(s)	Hwang, How Yuan
Publication date	2019
Original citation	Hwang, H. Y. 2019. Integrated silicon photonic packaging. PhD Thesis, University College Cork.
Type of publication	Doctoral thesis
Rights	**© 2019, How Yuan Hwang.** http://creativecommons.org/licenses/by-nc-nd/3.0/ 
Embargo information	Not applicable
Item downloaded from	http://hdl.handle.net/10468/9524

Downloaded on 2021-11-27T09:18:25Z


UCC
University College Cork, Ireland
Coláiste na hOllscoile Corcaigh

Ollscoil na hÉireann

NATIONAL UNIVERSITY OF IRELAND, CORK

Integrated Silicon Photonic Packaging

A thesis presented by

How Yuan Hwang, B. Eng., M. Sc.

orcid.org/0000-0002-8536-0974

for the degree of

Doctor of Philosophy

Supervisor: Prof. Peter O'Brien

Head of Department: Dr. Fatima Gunning

Tyndall National Institute

University College Cork

January 2019

DECLARATION

This is to certify that the work I am submitting is my own and has not been submitted for another degree, either at University College Cork or elsewhere. All external references and sources are clearly acknowledged and identified within the contents. I have read and understood the regulations of University College Cork concerning plagiarism.

How Yuan Hwang

9th Jan. 2019

ABSTRACT

Silicon photonics has garnered plenty of interests from both the academia and industry due to its high-speed transmission potential as well as sensing capability to complement silicon electronics. This has led to significant growth on the former, valuing at US$ 626.8M in 2017 and is expected to grow 3-fold to US$ 1,988.2M by 2023, based on data from MarketsandMarkets™. Silicon photonics' huge potential has led to worldwide attention on fundamental research, photonic circuit designs and device fabrication technologies. However, as with silicon electronics in its early years, the silicon photonics industry today is extremely fragmented with various chip designs and layouts. Most silicon photonic devices fabricated are not able to reach the hand of consumers, due to a lack of information related to packaging design rules, components and processes. The importance of packaging technologies, which play a crucial role in turning photonic circuits and devices into the final product that end users can use in their daily lives, has been overlooked and understudied. This thesis aims to – 1. fill the missing gap by adapting existing electronics packaging techniques, 2. assess its scalability, 3. assess supply chain integration and finally 4. develop unique packaging approaches specifically for silicon photonics.

The first section focused on high density packaging components and processes using University of California, Berkeley's state-of-the-art silicon photonic MEMS optical switches as test devices. Three test vehicles were developed using (1) via-less ceramic and (2) spring-contacted electrical interposers for 2D integration and (3) through-glass-via electrical interposers for 2.5D heterogeneous integration. A high density (1) lidless fibre array and (2) a 2D optical interposer, which allows pitch-reduction of optical waveguides were also developed in this thesis. Together, these components demonstrated the world's first silicon

photonic MEMS optical switch package and subsequently the highest density silicon photonic packaging components with 512 electrical I/Os and 272 optical I/Os.

The second section then moved away from active optical coupling that was used in the former, investigating instead passive optical packaging concepts for the future. Two approaches were investigated - (1) grating-to-grating and (2) evanescent couplings. The former allows the development of pluggable packages, separating fibre coupling away from the device while the latter allows simultaneous optical and electrical packaging on a glass wafer in a single process.

Lastly, the knowhow and concepts developed in this thesis were compiled into packaging design rules and subsequently introduced into H2020-MORPHIC, PIXAPP packaging training courses (as a trainer) and other packaging projects within the group.

LIST OF ACRONYMS

Acronym	Description
AlN	Aluminum nitride
BER	Bit error rate
BOX	Bottom silicon oxide
CMOS	Complementary metal-oxide semiconductor
CTE	Coefficient of thermal expansion
DOF	Degree of freedom
EDX	Energy dispersive x-ray microscopy
EME	Eigenmode expansion
EMIB	Embedded multi-die interconnect bridge
ENIG	Electro-less nickel immersion gold
FA	Fibre array
FC/APC	Ferrule connector/Angle polished connector
FDTD	Finite-difference time-domain
FPGA	Field programmable gate array
MEMS	Micro-electromechanical systems
MPO	Multi-fibre push on
MPW	Multi-project wafer
MTP	Multi-fibre termination push on
OSAT	Outsourced assembly and test
PCB	Printed circuit board

PDK	Process and design kit
PIC	Photonic integrated circuit
RDL	Redistribution line
SAC	Tin-silver-copper
SEM	Scanning electron microscopy
SFP+	Enhanced small form-factor pluggable
SLD	Superluminiscent diode
SMF	Single mode fibre
TE	Transverse electric
TGV	Through glass via
TM	Transverse magnetic
TOX	Top silicon oxide
TSV	Through silicon via

ACKNOWLEDGMENT

I would like to express my deepest gratitude towards my supervisor Prof. Peter O'Brien who gave me the opportunity to undertake this research in Photonics Packaging Group, Tyndall National Institute. I appreciate his guidance and support in making the achievements presented in this thesis possible. I would also like to thank my thesis committee Dr. Emanuele Peluchi and Mr. Brian Corbett for the insightful discussions.

Special thanks to all the colleagues in Photonics Packaging Group, particularly Jun Su Lee, Lee Carroll (introduction to Lumerical), Sean Collins, Marc Rensing and Noreen Nudds (sample wire bonding), colleagues from Specialty Products and Services - Finbarr Waldron (sample x-ray), Paul Tassie (sample dicing), and Krimo Khalfi and colleagues from III-V Materials and Devices - James O'Callaghan and Mahbub Akhter for entertaining my various requests.

I would also like to thank Prof. Ming C. Wu and his team from University of California, Berkeley for a packaging collaboration using their state-of-the-art switching devices, various industrial suppliers (Applied Thin Film Products, ECS Circuits, LEW Techniques, Milltech, SAMTEC Microelectronics and TEEM Photonics) for accepting and fabricating the various components that I designed and Science Foundation Ireland (SFI) for funding the activities. Last but not least, I would like to thank my family and friends for all the supports given to me throughout the years.

How Yuan Hwang

9th Jan. 2019

TABLE OF CONTENTS

LIST OF FIGURES

6.5	Common type of fibre coupling materials and polished angles for silicon photonic devices. Generic fibre array is cheap.	**157**
6.6	Common electrical interconnects structure and metallization layers on device bond pad.	**158**
A1	Auto-aligner by Newport Corp. used for fibre alignment from 1-channel all the way to 136-channels as demonstrated in this thesis. The system consist of two 6-degree of freedom alignment arms, one top and one side view camera to assist with active alignment process. Suitable for vertical or planar fibre coupling, with the help of specially designed fibre array gripper. Travel distances of the alignment arms, top and side cameras have to be carefully considered during the design stage to prevent obstructions.	**161**
A2	Manual wire bonder by K&S used for Au stud bumping on device bond pads and wire bonding to connect device to interposer or test board. Typical wire diameter used on the system is 0.8 and 1.0 mil.	**162**
A3	Solder jetting system by Pactech (SB^2-SM), used to form solder bumps on device bond pads. The system can currently process only Φ50 µm SAC 305 solder spheres. Operation can be automated with the help of bond map. Bond pad metallization preferably to be Au finishing for better wetting with Sn from SAC 305.	**163**
A4	Flip chip bonder by Finetech (Fineplacer lambda), used for flip chip and thermo-compression bonding of various components. Can go up to 40 N force and 400 °C reflow. Maximum alignment field of view of 2.5 mm x 2.5 mm at highest magnification. Alignment between top and bottom components are based on matching fiducials (alignment marks) on both components.	**164**
A5	Inert (N_2) reflow oven by LPKF (Protoflow-S) used for board level reflow. Reflow temperature can reach 320 °C thus suitable for AuSn assembly. Can be used as curing oven for underfill and die attach as well.	**165**
A6	Engineering drawings for fibre array grippers used in this thesis. As one set of grippers consist mirrored components, only one side is shown here. (a) Main body and gripping plate for vertical fibre coupling. (b) Main body and gripping plate for planar fibre coupling. (c) Adjustable arm suitable for both vertical	**166**

	and planar fibre coupling. Components were designed considering travel length of Auto-aligner and expected board size that can be mounted on the system.	
A7	Two of the fibre array grippers fabricated in this thesis, (a) for vertical fibre coupling and (b) planar fibre coupling.	**169**

LIST OF TABLES

LIST OF PUBLICATIONS

JOURNAL ARTICLES

1. M. Passoni, F. Floris, **H. Y. Hwang**, L. Zagaglia, L. Carroll, L. C. Andreani, and P. O'Brien, "Co-optimizing grating couplers for hybrid integration of InP and SOI photonic platforms, *AIP Advances 8*, 095109, 2018. **DOI:** 10.1063/1.5046164.

2. **H. Y. Hwang**, J. S. Lee, T. J. Seok, A. Forencich, H. R. Grant, D. Knutson, N. Quack, S. Han, R. S. Muller, G. C. Papen, M. C. Wu, P. O'Brien, "Flip Chip Packaging of Digital Silicon Photonics MEMS Switch for Cloud Computing and Data Centre*", IEEE Photonics Journal*, vol. 9, no. 3, pp. 1-10, June 2017. **DOI:** 10.1109/JPHOT.2017.2704097. **Invited.**

3. L. Carroll, J. S. Lee, C. Scarcella, K. Gradkowski, M. Duperron, H. Lu, Y. Zhao, C. Eason, P. Morrissey, M. Rensing, S. Collins, **H. Y. Hwang**, P. O'Brien, "Photonic Packaging: Transforming Silicon Photonic Integrated Circuits into Photonic Devices," *Appl. Sci*. 2016, 6, 426. **DOI**: 10.3390/app6120426.

CONFERENCES AND PROCEEDINGS

1. B. Abasahl, I. Zand, N. Quack, K. Gylfason, M. A. Jezzini, **H. Y. Hwang**, M. A. G. Porcel, C. L. Arce, S. Kumar, W. Bogaerts, "Generic Platform for Silicon Photonics based on MEMS Reconfigurable Photonic Integrated Circuits," *Photonics & Electromagnetics Research Symposium (PIERS)*, June. 2019.

2. N. Quack, H. Sattari, A. Y. Takabayashi, Y. Zhang, P. Edinger, C. Errando-Herranz, K. B. Gylfason, X. Wang, F. Niklaus, M. A. Jezzini, **H. Y. Hwang**, P. O'Brien, M. A. G. Porcel, C. L. Arce, S. Kumar, B. Abasahl, P. Verheyen, W. Bogaerts, "Silicon Photonic MEMS: Exploiting Mechanics at the Nanoscale to Enhance Photonic Integrated Circuits," *OFC Conference Symposia*, Mar. 2019. **Invited**. **DOI:** 10.1364/OFC.2019.M2D.3.

3. B. Abasahl, I. Zand, C. L. Arce, S. Kumar, N. Quack, M. A. Jezzini, **H. Y. Hwang**, K. Gylfason, M. A. G. Porcel, W. Bogaerts, "Towards Low-Power Reconfigurable Photonic ICs Based on MEMS Technology," *AIP Conference on Optoelectronic and Microelectronic Materials and Devices (COMMAD)*, Dec. 2018. **Invited**.

4. **H. Y. Hwang**, J. S. Lee, J. Henriksson, K. Kwon, T. J. Seok, M. C. Wu and P. O'Brien "Pluggable Silicon Photonics MEMS Switch Package for Data Centre," *IEEE Electronics Packaging Technology Conference*, Singapore, Dec. 2018. **DOI:** 10.1109/EPTC.2018.8654270.

5. **H. Y. Hwang**, P. Morrissey, J. S. Lee, J. Henriksson, T. J. Seok, M. C. Wu and P. O'Brien, "128 x 128 Silicon Photonics MEMS Switch Package using Glass Interposer and Pitch Reducing Fibre Array," *IEEE Electronics Packaging Technology Conference*, Singapore, pp. 1-4, Dec. 2017. **DOI:** 10.1109/EPTC.2017.8277436.

6. **H. Y. Hwang**, P. Morrissey, J. S. Lee, J. Henriksson, T. J. Seok, M. C. Wu and P. O'Brien, "128 x 128 Digital MEMS Switch Package," *Photonics Ireland*, Galway, Sept 2017.

7. **H.Y Hwang**, J.S. Lee, T.J. Seok, L. Carroll, M.C. Wu, P. O'Brien, "Packaging of 50 x 50 MEMS-Actuated Silicon Photonics Switching Device for High performance Computing and Large-Scale Data Centres*," IEEE Electronics Packaging Technology Conference*, Singapore, pp. 245-249, Dec. 2016. **DOI:** 10.1109/EPTC.2016.7861480.

8. T.J. Seok, **H.Y. Hwang**, J.S Lee, A. Forencich, H.R. Grant, D. Knutson, N. Quack, S. Han, R.S. Muller, L. Carroll, G.C. Papen, P. O'Brien, M.C. Wu, "12 x 12 Packaged Digital Silicon Photonics MEMS Switches," *IEEE Photonics Conference*, Hawaii, pp. 629-630, Oct. 2016. **DOI:** 10.1109/IPCon.2016.7831260.

PREFACE

OBJECTIVE

Most of the research on silicon photonic to date focuses mainly on device functionalities, device fabrication and physical behaviors, leading to increasing gaps between a device and its final packaged form. The objective of the thesis thus is to develop and demonstrate advanced silicon photonic packaging technologies with future manufacturability in mind. High density 2D and 2.5D heterogeneous integration and passive optical assembly of silicon photonic devices formed the major theme of the thesis. It is hoped that the various concepts, designs, materials, and process flows used in this thesis provide the much needed boost toward mass manufacturing of silicon photonic packages in the future.

STRUCTURE OF THE THESIS

This thesis consists of two sections. Section I (Chapters 2 and 3) discusses high density optical and electrical packaging of silicon photonic devices, whereby active optical assembly after electrical packaging is used. State of the art silicon photonic MEMS switches from University of California, Berkeley are used as packaging test devices. Section II (Chapters 4 and 5) discusses passive optical and electrical assembly, whereby optical coupling can be achieved simultaneously during electrical packaging. The following provides an overview of the content for each chapter.

Chapter 1 introduces readers to the world of silicon photonic packaging and its associated electrical and optical packaging approaches and challenges. 2D-FDTD simulations comparing vertical and planar fibre coupling on uniform and non-uniform gratings are presented. A review of prior art on electrical interposers and optical coupling solutions for photonic packaging and integration is also included. The chapter ends with a discussion on the rationale behind using actual silicon photonic test devices to properly demonstrate high density optical and electrical packaging components.

Chapter 2 demonstrates first generation packaging solutions for optical and electrical integration using silicon photonic MEMS optical switches as test devices. The test vehicle (herein refer to as TV1) is developed through the use of a single metal layer aluminum nitride interposer and lidless fibre array to demonstrate the concept of 2D packaging and integration. The designs and components introduced led to the world's first functional silicon photonic MEMS optical switch package with 12 x 12 ports.

Chapter 3 expands the work done in the earlier chapter to demonstrate higher density optical and electrical integration. UC Berkeley's latest silicon photonic MEMS optical switch was used as a test device following some package-able reconfiguration discussions. Two test

vehicles – a pluggable package (herein refer to as TV2a) and through-glass via package (herein refer to as TV2b) are developed to demonstrate the concept of 2.5D packaging and integration. TV2a consists of a single metal layer aluminum nitride interposer with secondary spring-contacted interposer, while TV2b consists of three metal layers with drilled through holes on glass interposer. This chapter also introduces the 2D 136-channel pitch-reducing optical fibre array made from ion-exchange processes.

Chapter 4 turns the attention away from active fibre alignment, exploring gratings-to-gratings coupling based on a pair of gratings stacked vertically. This concept is meant to be integrated with TV2a – the pluggable package from Chapter 3 in the future. Simulations and experimental results are documented.

Chapter 5 subsequently explores evanescent coupling on a buried glass waveguide meant to be integrated with TV2b – through-glass-via package in the future. The design, simulations and challenges encountered are documented.

Chapter 6 provides generic design rules and considerations for readers who are interested in silicon photonic packaging and integration.

Chapter 7 summarises the work done in this thesis and suggestions for future work.

The appendix introduces the various equipment used and mechanical components designed and fabricated for the activities in this thesis.

INTRODUCTION

1.1 SILICON PHOTONICS AND PACKAGING

In a 2013 white paper [1], Cisco had estimated that only about 10 billion out of the 1.5 trillion things (0.6%) were connected globally through the internet, and in 2015 [2], predicted that as much as 500 zetta-bytes of information will be generated by 2019, up more than threefold from 135 zetta-bytes in 2014. As we progress toward the era of internet of everything (IoE), CMOS electronics, which have been responsible with the processing and local transmission of information can no longer keep up with the growth, especially as Moore's law is approaching its end [3]. Moreover, traditional high-speed electronics require copper connections on hybrid (Rogers) printed circuit board as well as cables running from metres to kilometres, leading to massive signal attenuations, limiting transmission speed.

Silicon photonics on the other hand, have the ability to complement existing microelectronics by enhancing the transmission speed currently being limited by electrical traces (heat generation) through the optical domain [4]-[6]. By incorporating photonic components on the device and PCB, together with fibre optic cables for point to point connections, this allows more efficient signal transfers with lower energy losses. In fact, the first microprocessor with integrated photonic components to allow higher communication speed with off-chip memory was demonstrated recently [7], while companies such as Finisar, Macom and Huawei and leading the way in making high speed communications a reality.

Aside from improving the way we communicate, silicon photonics also allows new generation of sensing/imaging capabilities, improving disease/chemical detection and making autonomous driving possible. In fact, autonomous shuttle system is already under trial worldwide, such as Singapore, Germany, and Australia while in the consumer space, Ford,

Audi and Toyota are investing heavily into the development of autonomous cars [8]. As silicon photonic device fabrication technologies continue to mature, the demand for packaged products is increasing as well. However, limited activities into understanding packaging technologies and processes for silicon photonic devices have led to slow manufacturing throughput and thus higher cost.

Packaging is meant to provide a smooth transition in physical sizes, from the sub-micron features of integrated circuits to metre-scale systems while protecting them at the same time from environmental damages. Due to the wide level of integrations required, packaging is often categorised into the following [9], [10]:

a. Level 0 – Integration of various functional elements within a device
b. Level 1 – Device to substrate integration within a package
c. Level 2 – Package to board integration
d. Level 3 – Board to board integration within a sub-assembly
e. Level 4 – Sub-assembly integration within a system
f. Level 5 – Between systems

Level 0 involves the implementation of gate-to-gate interconnects on a device at wafer level through the use of electro-plating, physical vapour deposition or evaporation. The wafer will then be diced into individual devices, and subsequently form into a package (Level 1) through the use of wire bonding or flip chip bonding. Level 2 will see multiple packages being integrated onto a board, again through the use of wire bonding or flip chip bonding. Subsequent levels of integration (Level 3 to 5) involve the use of connectors and cables. It is worth highlighting at this stage that this thesis focuses mainly on level 1 and 2 integrations. With that in mind, let's dive deeper into silicon photonic packaging.

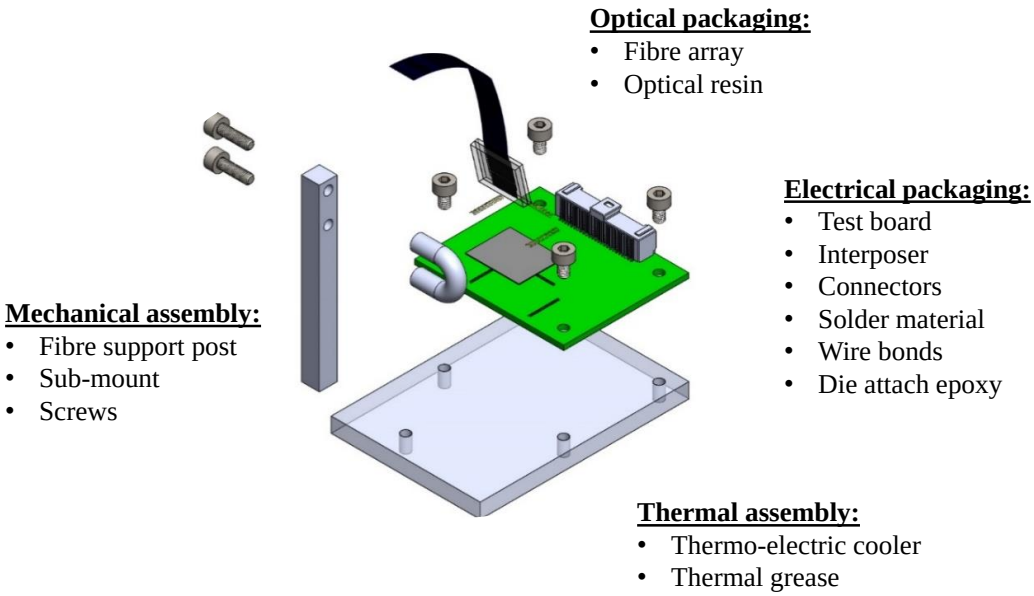


Fig. 1.1. Generic assembly of a silicon photonic package, consisting of thermal and mechanical considerations, in addition to optical and electrical packaging.

The packaging of silicon photonic devices often comes with multiple technical challenges, requiring electrical, optical, thermal, mechanical and material knowhow (Fig. 1.1). While similarities exist between traditional electronics packaging and silicon photonics packaging, there are differences involved as well. Aside from electrical interfaces, silicon photonics have additional optical interfaces in the form of gratings or inverted tapers that have to be connected to a system, typically through the use of optical fibers. This additional requirement reduces the degree of freedom for photonic packaging compare to electronics in the form of package design, materials to be used and the associated process flow.

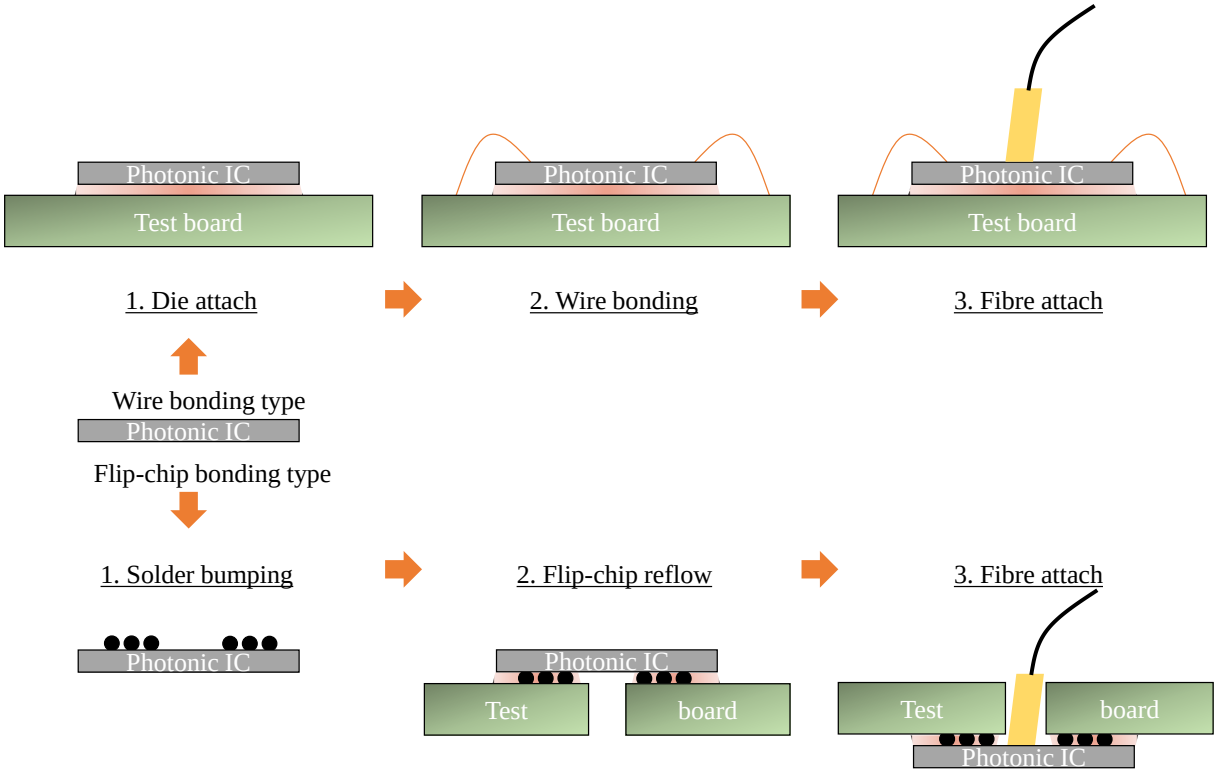


Fig. 1.2. Generic packaging sequence for silicon photonic devices. Note that fibre attach is always the last component to be assembled.

For silicon photonics packaging, the optical interfaces are usually the last to be processed (Fig. 1.2) due to its temperature sensitivity as most packaging processes are performed at elevated temperatures, i.e. die attach at 120 °C, thermo-sonic wire bonding at 150 °C and lead-free solder reflow at 260 °C. Meanwhile, the various materials have coefficients of thermal expansion (CTE), ranging from as low as 2.9 ppm/K for silicon to as high as 70 ppm/K for under-fill resins and 200 ppm/K for optical resins, thus will expand or contract with processing temperatures. Optical resins are also not stable at elevated temperatures, often losing optical clarity and adhesion strength that is necessary to hold a fibre against its optical interface on the device. Adhesion strength degradation and thermo-mechanical stress due to temperature also occur on fibre v-groove assembly. While a fibre-last approach is commonly adopted due to the above reasons, there have been demonstrations

using specialty optical resins, fibre v-groove assembly and optical fibres such as that by Doerr *et al* [11]. At the same time, there are fabrication tolerances on fibre v-groove that can accumulate and add to the fibre pitch as fibre counts increase, leading to optical insertion losses due to misalignment. At the same time, as the typical minimum fibre v-groove pitch is 127 µm, increasing the number of fibre channels to beyond 100 will lead to a large photonic die, increasing packaging complexity due to alignment in 6-degree-of-freedom. A careful consideration of the packaging sequence, processes, materials and design of a silicon photonic device is thus necessary.

1.2 ELECTRICAL INTERCONNECT AND INTERPOSER TECHNOLOGY

In its simplest form, an interposer functions as the electrical intermediary between integrated circuits on a device and a system board (Fig. 1.3). Continuous downscaling of integrated circuits, driven by the relentless pursuit of miniaturisation, leads to increasing dimensional mismatches between them and at the same time, reliability concerns. The interposer thus bridges the two by spreading tightly distributed electrical ports from the device to a wider pitch on the system board for easier assembly. Aside from serving as an electrical intermediary, the interposer is also used to integrate various devices with different functionalities (heterogeneous integration) into a mini-system, prior to board level assembly, thus terms such as 2D and 2.5D are common in the electronics packaging industries.

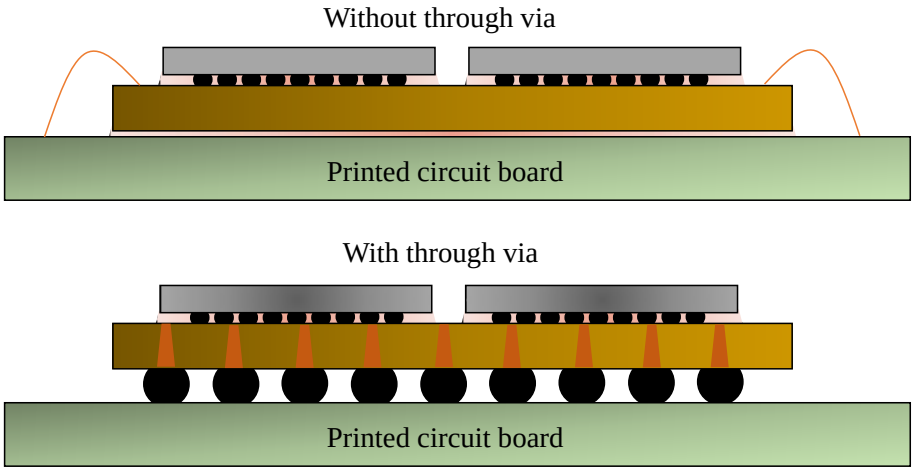


Fig. 1.3. Schematic of generic interposer (without and with through via) used for electrical interfacing between device and system board.

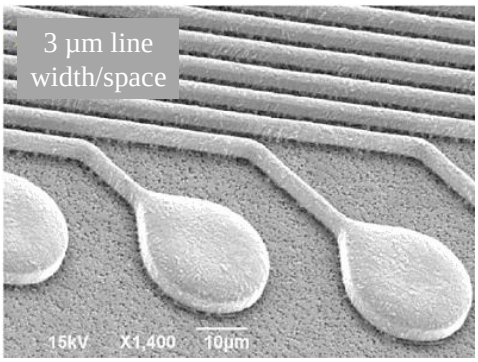
Moreover, in terms of operational reliability, an interposer as an intermediary offers a gradual transition in mechanical stresses arising from the differences in coefficient of thermal expansion (CTE) between various components used. For example, device made of silicon has a CTE of 3 ppm/K while system board has CTE ranging from 14 to 70 ppm/K depending on core materials and the number of metal layers. Other materials used in packaging such as

eutectic lead-based and lead-free solders have on average CTE of 24 ppm/K, organic die attach and under-fill materials have CTE of about 30 ppm/K while bond wires have CTE ranging from 14 to 23 ppm/K, depending on whether it is gold, copper or aluminium.

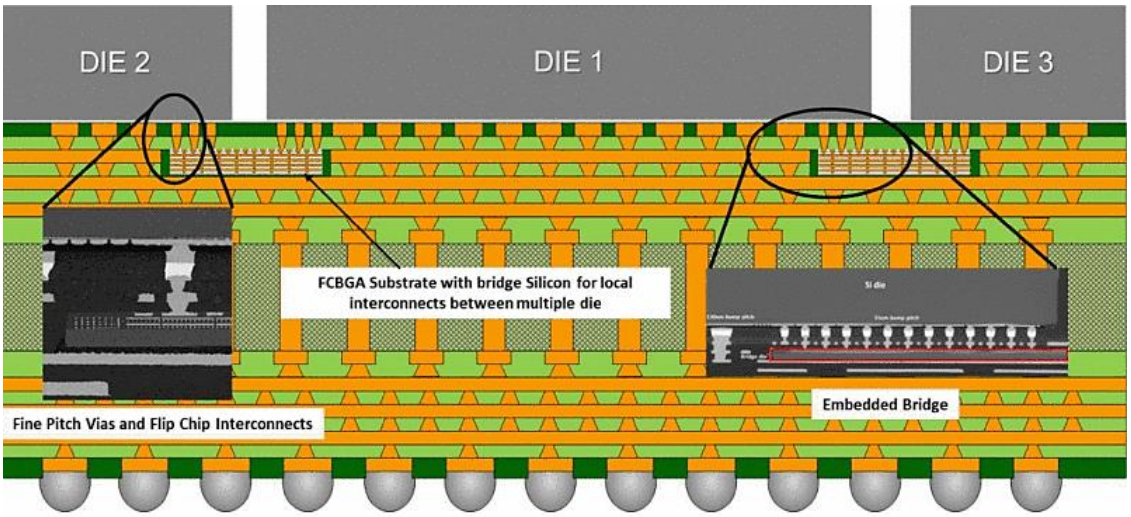
Due to its various benefits, efforts have been made especially by the electronics packaging industries into developing interposer technologies. Over the years, interposer technologies have evolved from being (1) via-less to through-via to reduce the electrical length, (2) single metal layer to multiple layers and (3) reduction in metal line width/space in order to increase the density of electrical ports. Today, they are various interposer technologies based on organic [12]-[14], silicon [15], [16], glass [17], [18] or ceramic [19], [20] materials and structures, with their respective merits and demerits.

Types of interposer to be used in any packaging design have to be based on the application, operating speed, cost and ease of integration [21]-[25]. For example, glass is better suited for high speed applications due to its low dielectric constant, ceramic is better suited for high power applications due to its high thermal conductivity, silicon is better suited for ultra-fine electrical interconnection due to its CMOS compatibility, while organic interposers are of lower cost. Nevertheless, the decision to use a particular type of interposer technology is highly dependent on the ease of availability and design rules from suppliers.

(a)



(b)



(c)

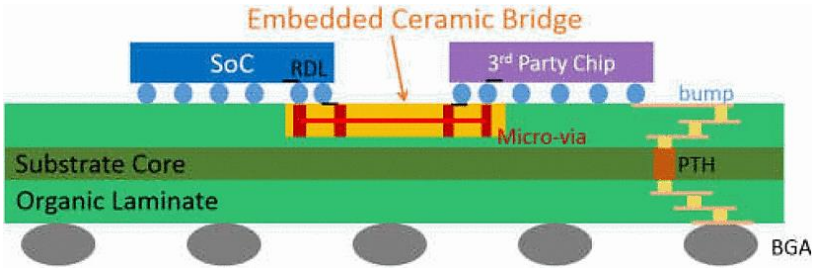


Fig. 1.4. Examples of interposer technologies. (a) Fine metallization lines on organic interposers from [13], (b) EMIB approach from [16] and (c) embedded ceramic concept from [20].

1.3 OPTICAL INTERCONNECT AND COUPLING TECHNOLOGY

Table 1.1 Comparison of silicon photonic optical coupling techniques

	Pros	**Cons**
In-plane coupling (nano-tapers)	Larger bandwidth	Violates CMOS design rules
		Requires post-processing (edge facet polishing)
		Wafer level testing not possible
		Difficult fibre coupling without fiducial
		Couplers limited to single row
		Polarisation cannot be separated
Out-of-plane coupling (gratings)	Does not violates CMOS design rules	Finite bandwidth
	Does not require post-processing (edge facet polishing)	
	Full wafer level testing	
	Easy fibre coupling with fiducial incorporated	
	High density couplers application (staggered rows)	
	Polarisation can be separated	

Silicon nano-tapers (in-plane) and surface gratings (out-of-plane) are the two common approaches used in silicon photonics as optical interconnects. The former, while having both higher bandwidth and coupling efficiency compare to the latter, is typically located at the edge of a silicon photonic device and requires an additional spot-size converter. At the same

time, post fabrication probing is not possible for silicon nano-tapers unlike surface gratings, thus making it less popular. Additional spot-size converters and edge facet polishing also make it less compatible with CMOS foundries. Welch [26], in an IEEE presentation, summarised the comparison between the two which is reproduced in Table 1.1 above.

Over the years, the majority of the research efforts in silicon photonics has focused on understanding surface gratings and their fabrication in order to expand the bandwidth and coupling efficiency (Fig. 1.5). Today's surface gratings are designed for first diffraction order for reversibility (receiving and emitting) and can be generally grouped into two categories – uniform and non-uniform gratings. The design, fabrication and improvement of gratings are not the focus of this thesis, thus only a general overview of their behaviour from the packaging perspectives shall be discussed.

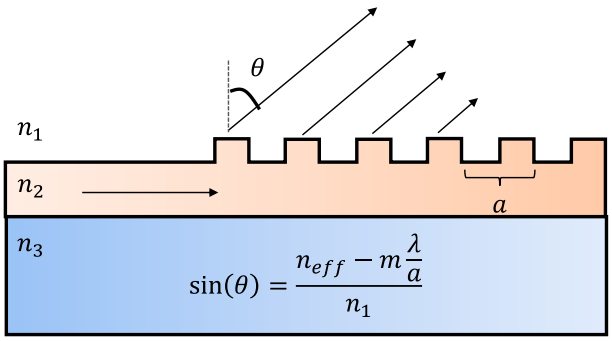


Fig. 1.5. Generic surface grating structure and its formula, where m is order of diffraction, Θ is angle of diffraction, λ is wavelength, a is grating period, n_1, n_2, n_3 are refractive indexes of layers 1, 2 and 3, n_{eff} is the average of index value of the thick and thin region of the grating.

In terms of packaging, there are two approaches in which a fibre array can be coupled onto a grating coupler – vertical or planar. Vertical coupling allows optical signals to enter the grating directly, while planar coupling relies on total internal reflection at the polished interface to direct the optical signals. 2D-FDTD simulations illustrating the differences

between vertical and planar fibre couplings using non-uniform gratings design from [27] are shown in Fig 1.6. It can be seen that planar coupling has higher transmission losses compare to vertical coupling. A comparison is further done using non-uniform [27] and uniform grating [28] designs from existing literatures. The results are tabulated in Tables 1.2 and 1.3. There are N.A entries in Tables 1.2 and 1.3 as the configuration isn't physically possible. "Distance" in the tables are referring to the fibre core centre to the top oxide surface of the grating coupler used in simulation space.

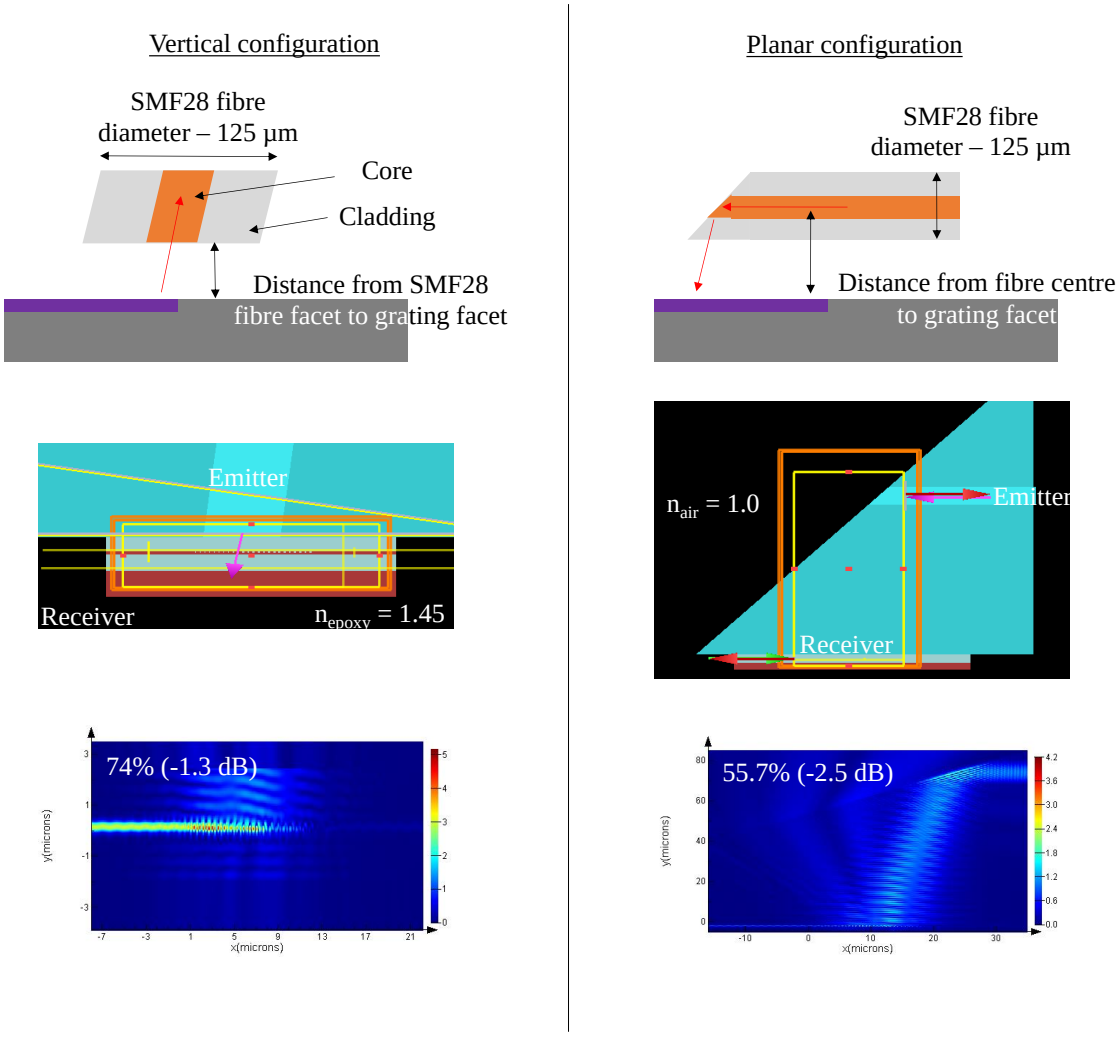


Fig. 1.6. 2D-FDTD simulation of vertical fibre coupling (left) and planar fibre coupling on non-uniform gratings (right).

Table 1.2. Insertion losses of non-uniform grating system between vertical fibre and planar fibre couplings. Units in dB.

Distance	**Vertical fibre**		**Planar fibre**
	n_{air} = 1	**n_{epoxy} = 1.45**	**n_{air} = 1**
Zero gap	- 1.3	N.A	N.A
10 µm	- 1.86	- 1.33	N.A
62.5 µm	- 2.66	- 2.25	- 2.5

Table 1.3. Insertion losses of uniform grating system between vertical fibre and planar fibre couplings. Units in dB.

Distance	**Vertical fibre**		**Planar fibre**
	n_{air} = 1	**n_{epoxy} = 1.45**	**n_{air} = 1**
Zero gap	- 2.98	N.A	N.A
10 µm	- 2.89	- 2.96	N.A
62.5 µm	- 4.05	- 3.66	- 4.52

While the simulation exercise shows that planar coupling suffers from lower coupling efficiency due to additional losses from total internal reflection and larger vertical distance, it is more stable than vertical coupling from a mechanical point of view. An example is shown in Fig. 1.7, whereby a vertically assembled fibre array had decoupled from its original position. Planar assembly has larger surface area for mechanical support and at the same time close to negligible fiber bending stress due to gravity, which is common for vertical assembly.

It also allows low profile packaging assembly compare to vertical coupling that requires a fiber support post. These shortcomings of vertical coupling have led some companies such as Sumitomo Electric to introduce unique fiber bending technology to allow low-profile vertical coupling [29].

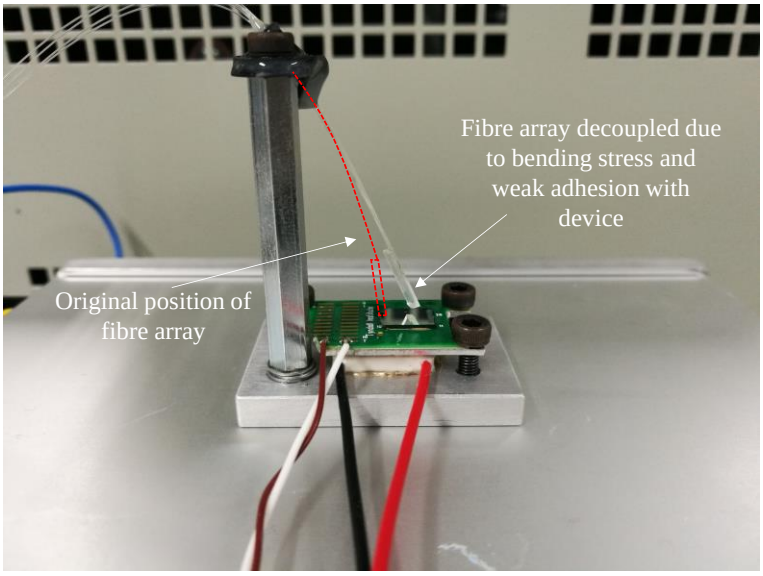


Fig. 1.7. Example of a decoupled vertical fibre array assembly due to bending stress and weak adhesion with device.

1.4 REVIEW OF PRIOR ART ON OPTICAL PACKAGING

In general, packaging and integration of silicon photonics devices can be approached in multiple ways, but the key theme is always to eliminate active alignment and to allow multi-device configurations on a test board. Some of the interesting ideas that have been proposed are briefly introduced below.

Asperation Oy and VTT Electronics had demonstrated a planar polymer based waveguide with integrated micro-mirrors on FR4 substrates over a decade ago [30]. Their paper described the concept of an optical/electrical printed circuit board for three dimensional (3-D) optical interconnects (Fig. 1.8) which offers low-cost mass fabrication.

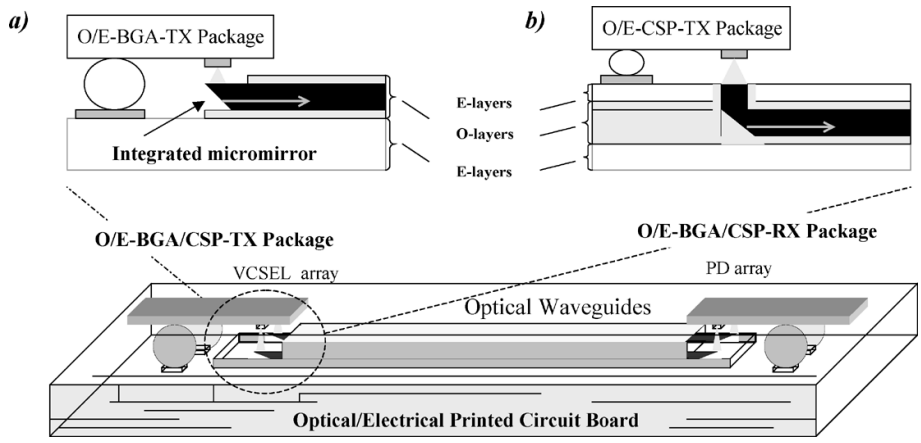


Fig. 1.8. Optical/electrical substrate using polymer waveguide with micro-mirrors from [30].

Similarly, IBM Zurich also proposed the application of polymer waveguides on organic substrates due to its low cost attractiveness. There are two coupling approaches demonstrated, (1) pin-guided butt coupling [31] and (2) evanescent coupling [32] as shown in Fig. 1.9 and Fig. 1.10 respectively.

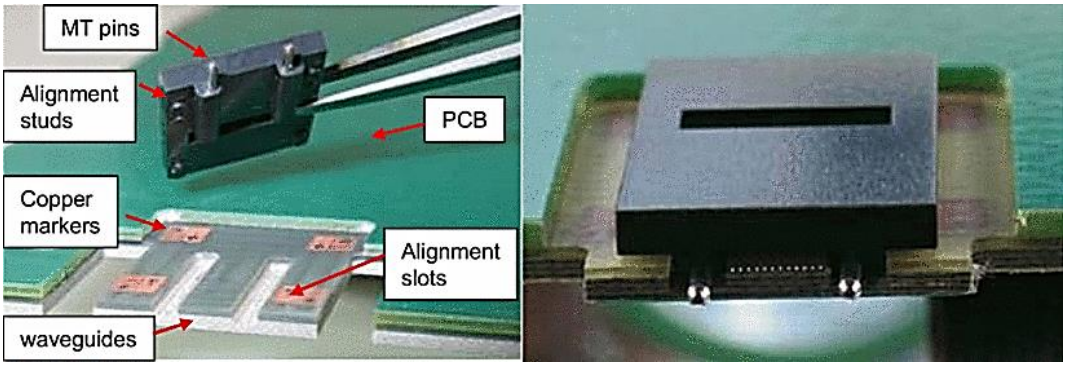


Fig. 1.9. Butt coupling concept of polymer waveguide within organic substrate from [31].

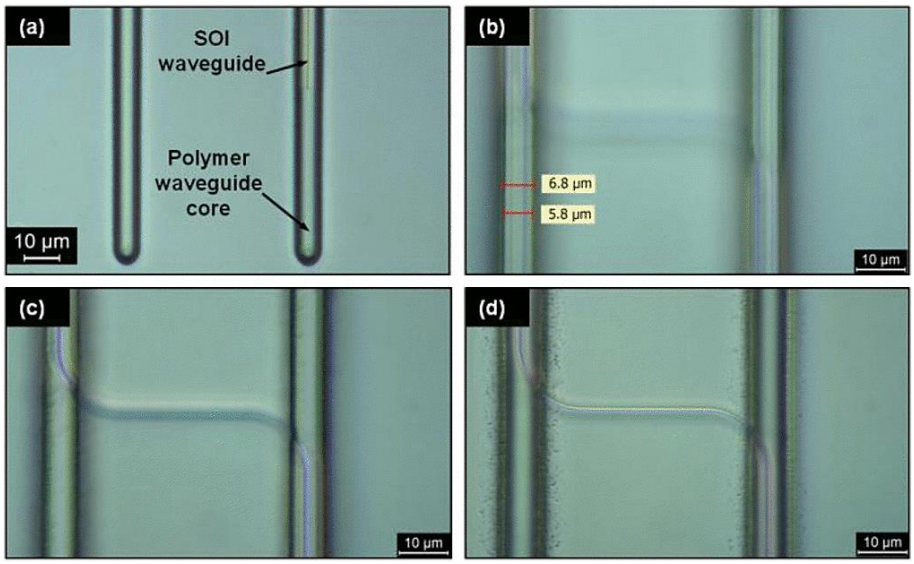


Fig. 1.10. Evanescent coupling concept of polymer waveguide on organic substrate from [32].

It is worth noting that both Asperation Oy and IBM Zurich's concepts of polymer waveguide on organic substrate are limited in 2-D. Karlsruhe Institute of Technology (KIT) on the other hand, introduced photonic wire bonding in 2012 [33], which allows 3-D integration of devices. The photonic wires are formed using two-photon lithography – pulsed laser writing on negative tone resist. Unreacted resist were then washed away, leaving only the wires (Fig. 1.11).

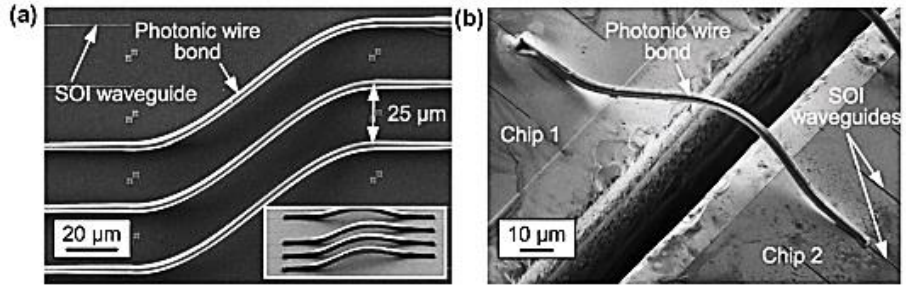


Fig. 1.11. Photonic wire bonds linking two devices from [33].

NTT and Kyoto University in 2004 proposed the used of multi-layer glass substrates to form 3-D optical waveguides [34]. Epoxy resin was used to fabricate the planar waveguides on a glass substrate and then laminated, diced and polished at an angle to form the 3-D waveguides. Total internal reflection will promote coupling into gratings on the photonic device. The concept is shown in Fig. 1.12.

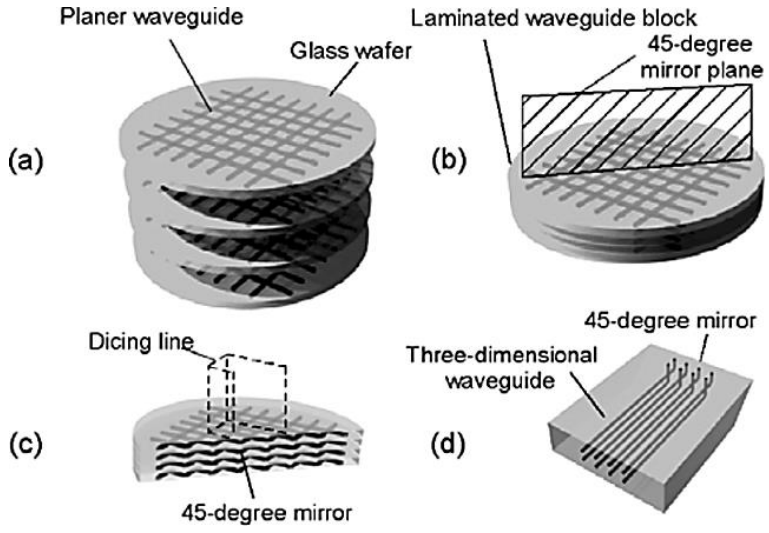


Fig. 1.12. Illustration of 3-D waveguides fabrication through lamination of planar polymer waveguide on glass from [34].

IMEC and LioniX on the other hand introduced a silica based optical interposer based on Triplex technology (Fig. 1.13) [35]. A mirror array was formed at the edge of the waveguides to couple light into the gratings on a photonic device.

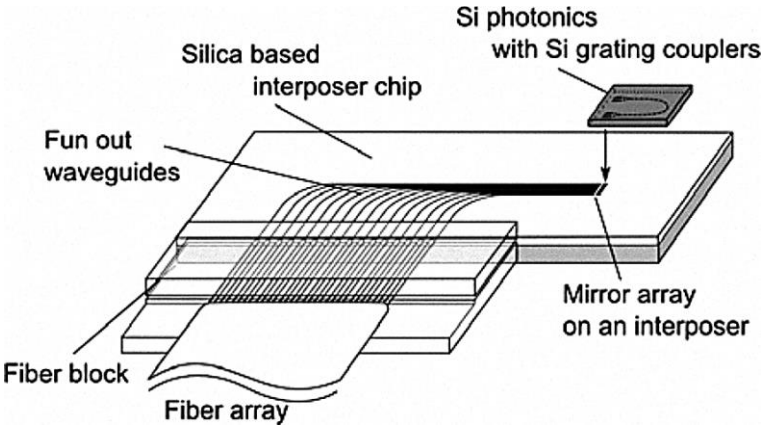


Fig. 1.13. Triplex optical interposer for silicon photonics integration from [35].

Next, Fraunhofer IZM and Georgia Tech also developed their own approaches using glass substrates. The former utilised ion-exchange process to form planar waveguides on the glass, and then polished at one end to couple light into surface gratings on the device [36]. Georgia Tech on the other hand, plugged polymer material into laser drilled vias to form optical vias for photonic device integration [37]. Their respective concepts are shown in Fig. 1.14 and Fig. 1.15 below.

Finally, Oracle proposed and demonstrated high density chip-to-chip optical coupling using silicon mirrors [38]. The concept is shown in Fig. 1.16.

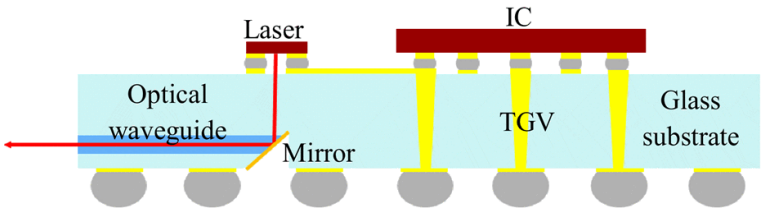


Fig. 1.14. Polished ion-exchange waveguides from [36].

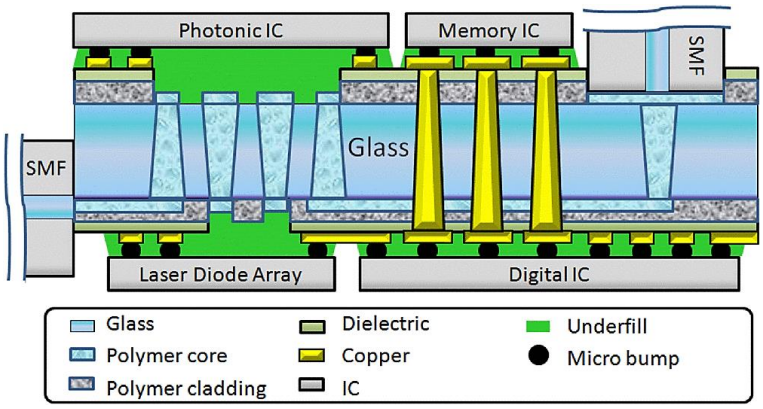


Fig. 1.15. Polymer plugged via to light coupling from [37].

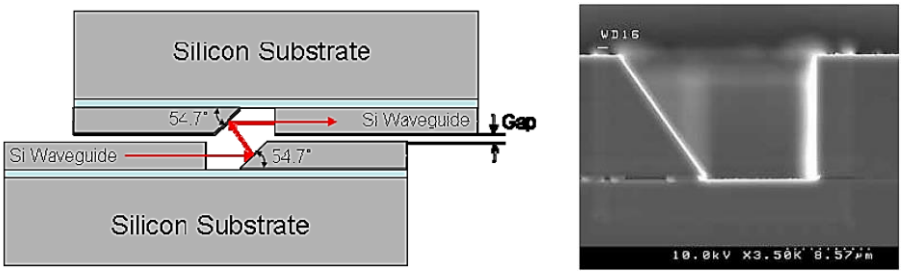


Fig. 1.16. Chip-to-chip optical proximity communication approach using silicon mirror from [38].

1.5 TEST DEVICE FOR PACKAGING DESIGN AND DEMONSTRATION

As mentioned in the objective, this thesis aims to develop and demonstrate advanced silicon photonic packaging approaches for future manufacturing. Proper packaging test vehicles are necessary in order to make the development as realistic as possible, and the test devices to be used play an important role. Through collaboration with University of California, Berkeley (UCB), functional packaging demonstrations can be made using their state-of-the-art silicon photonic MEMS optical switch.

While a purposely designed and fabricated test device from MPW foundries can be done, only a "dummy" packaging test vehicle can be demonstrated in this scenario, and the challenges associated with packaging a "live" device cannot be fully appreciated. Secondly, the focus of this thesis is about high density optical and electrical packaging developments, but MPW runs offer limited size, interconnect density and functions (Fig. 1.17). Moreover, the cost associated with MPW runs are on the high side and can cost up to € 150,000 (Table 1.4) and often come with long lead time. A collaboration and partnership with UCB is thus a win-win scenario.

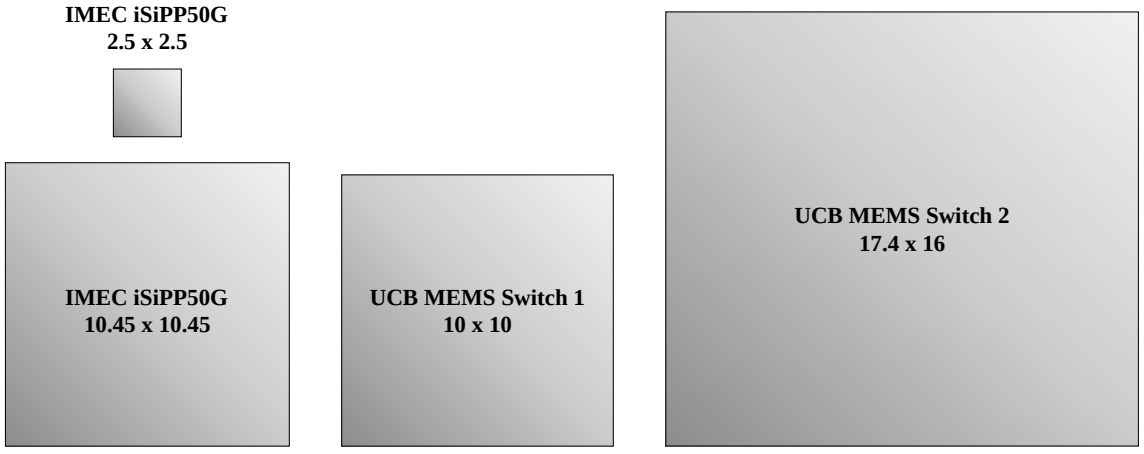


Fig. 1.17. Size comparison of the test devices from UC Berkeley that were used to develop packaging design and components in this thesis versus standard devices from MPW foundries such as IMEC.

Table 1.4: Comparison of device fabrication surface area and cost from different Multi-Project-Wafer (MPW) foundries [39]-[44].

Area (mm^2)	Cornerstone	IMEC passives	IMEC iSiPP50G	LETI Si310-PHMP2M	IHP SG25H5_EPIC	AIM Photonics passive	AIM Photonics active	CMC Microsystems
Every 1 x 1					€ 8,000			
Every 2 x 1				€ 1,600				
2.5 x 2.5			€ 10,000					
8							$25,000	
5.15 x 2.5		€ 6,100	€ 20,000					
3 x 8								C$13,300
25							$50,000	
5.5 x 4.9	£7,000							
5.15 x 5.15		€ 11,600	€ 40,000					
50						$30,000	$100,000	
10.45 x 5.15		€ 20,600	€ 80,000					
11.47 x 4.9	£10,000							
100							$200,000	
10.45 x 10.45			€ 150,000					

1.6 CHAPTER SUMMARY

In this chapter, the basics of packaging and difference between electronic and silicon photonic packaging had been introduced. 2D and 2.5D interposer packaging approaches and types of optical couplings were also briefly discussed together with a review of state-of-the-art silicon photonic packaging approaches that was currently found in the literature. Subsequent chapters will further introduce advanced packaging approaches and processes that can be used for packaging silicon photonic devices, using silicon photonic MEMS switch as test subjects. These chapters shall form the basis of this doctoral thesis.

1.7 REFERENCES

[1] Cisco, “Embracing the Internet of Everything to Capture Your Share of $14.4 Trillion,” *White Paper*, 2013.

[2] Cisco, “Cisco Global Cloud Index: Forecast and Methodology, 2014-2019” *White Paper*, 2015.

[3] M. M. Waldrop, “The chips are down for Moore's law,” *Nature*, vol. 530, pp. 144-147, 2016.

[4] L. Michal, "Overcoming the limitations of microelectronics using Si nanophotonics: solving the coupling, modulation and switching challenges," *Nanotechnology*, vol. 15, p. S622, 2004.

[5] R. Soref, "The Past, Present, and Future of Silicon Photonics," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 12, pp. 1678-1687, 2006.

[6] L. C. Kimerling, "Photons to the rescue: Microelectronics becomes microphotonics," *The Electrochemical Society Interface*, vol. 9, pp. 28-31, 2000.

[7] C. Sun, M. T. Wade, Y. Lee, J. S. Orcutt, L. Alloatti, M. S. Georgas, *et al.*, "Single-chip microprocessor that communicates directly using light," *Nature*, vol. 528, pp. 534-538, 12/24/print 2015.

[8] Capgemini, “The Autonomous Car – A Consumer Perspective,” 2019. https://www.capgemini.com/news/the-autonomous-car-report/

[9] P. Viswanadham, “Essentials of Electronic Packaging: A Multidisplinary Approach,” *ASME*, 2011.

[10] TE Connectivity, “Levels of Packaging,” https://www.te.com/commerce/Document

Delivery/DDEController?Action=srchrtrv&DocNm=1-1773853-5_levelspkg&

DocType=DS&DocLang=EN

[11] C. Doerr, J. Heanue, L. Chen, R. Aroca, S. Azemati, G. Ali, G. McBrien, L. Chen, B. Guan, H. Zhang, T. Nielsen, H. Mezghani, M. Mihnev, C. Yung, M. Xu, "Silicon Photonics Coherent Transceiver in a Ball-Grid Array Package," *Optical Fiber Communication Conference Post Deadline Papers*, Th5D.5, 2017.

[12] H. Kuo, Y. Aritsuka, T. Masaya, R. Kasai, J. Suyama, M. Takeda, Y. Okazaki, H. Iida, D. Kitayama, K. Sakamoto, T. Takamo, M. Akazawa, H. Sato, S. Yamada, S. Kuramochi, "Introduction of Sub-2-micron Cu Traces to EnCoRe Enhanced Copper Redistribution Layers for Heterogeneous Chip Integration," International Conference on Electronics Packaging and IMAPS All Asia Conference, 2018.

[13] W.C. Chen, C. W. lee, M. H. Chung, C.C. Wang, S.K. Huang, Y.S. Liao," Novel ultra-fine line 2.1D package with organic interposer," IEEE CPMT Symposium Japan, 2017.

[14] K.F. Chang, R. Li, C. Jin, T.G. Lim, S. W. Ho, H.Y. Hwang, B. Zheng, "77-GHz Automotive Radar Sensor System With Antenna Integrated Package," IEEE Transaction on Components, Packaging and Manufacturing Technology, Vol. 4, No. 2, 2014.

[15] A. Martwick, "Silicon Interposer and TSV Signaling," IEEE 65th Electronic Components and Technology Conference, 2015.

[16] R. Mahajan, R. Sankman, N. Patel, D.W. Kim, K. Aygun, Z. Qian, Y. Mekonnen, I. Salama, S. Sharan, D. Iyengar, D. Mallik, "Embedded Multi-die Interconnect Bridge

(EMIB) – A High Density, High Bandwidth Packaging Interconnect," IEEE 66th Electronic Components and Technology Conference, 2016.

[17] K. Inoue, T. Fujimure, M. Takayama, S. Onitake, "Direct copper metallization on TGV (Thru-Glass-Via) for high performance glass substrate," European Microelectronics Packaging Conference, 2017.

[18] M. Tanaka, Y. Okazaki, J. Suyama, S. Kuramochi, Y. Han, O. Horiuchi, Y. Katoh, "Experimental Study of Through Glass Via Effects on High Frequency Electrical Characteristics," International Conference on Electronics Packaging and IMAPS All Asia Conference, 2018.

[19] Kyocera, "Fine Ceramics Offer a Wide Range of Thermal Conductivity."

[20] B. Wu, "Ceramic Interconnect Bridge for Heterogeneous Integrationg and Multiple Chip Packaging," China Semiconductor Technology International Conference, 2018.

[21] L. Li, P. Ton, M.Nagar, P. Chia, "Reliability Challenges in 2.5D and 3D IC Integration," IEEE 67th Electronic Components and Technology Conference, 2017.

[22] John H. Lau, "Recent Advances and New Trends in Flip Chip Technology," ASME J. Electron. Packag. 138 (3), pp. 1-23, 2016.

[23] W.S. Tsai, C.Y. Huang, C.K. Chung, K.H.Yu, C.F. Lin, "Generational Changes of Flip Chip Interconnection Technology, "12th International Microsystems, Packaging, Assembly and Circuits Technology Conference, 2017.

[24] A. Usman, E. Shah, N. B. Satishprasad, J. Chen, S. A. Bohlemann, S. H. Shami, A. A. Eftekhar, A. Adibi, "Interposer Technologies for High Performance Applications,"

IEEE Transactions on Components, Packaging and Manufacturing Technology, Vol. 7, No. 6, pp. 819-828, 2017.

[25] R. Radojcic, “More-than-Moore 2.5D and 3D SiP Integration,” Springer, 2017.

[26] Welch, B., “PSM4 vs WDM: A Silicon Photonics Perspective,” *IEEE 803.bm Fibre Optic Task Force*, 2013.

[27] X. Chen, C. Li, C. K. Y. Fung, S. M. G. Lo, H. K. Tsang, “Apodized Waveguide Grating Couplers for Efficient Coupling to Optical Fibers,” *IEEE Photonics Technology Letter*, Vol. 22, No. 15, 2010.

[28] Lumerical, “Grating coupler 2D-FDTD”, *Lumerical Knowledge Base*, 2017, https://apps.lumerical.com/pic_passive_grating_coupler_2d.html

[29] Sumitomo Electric, “FlexBeamGuidE,” https://global-sei.com/fiber_optic_interconne ct/products/FlexBeamGuidE/

[30] M. Immonen, M. Karppinen, and J. K. Kivilahti, "Fabrication and characterization of polymer optical waveguides with integrated micromirrors for three-dimensional board-level optical interconnects," IEEE Transactions on Electronics Packaging Manufacturing, vol. 28, pp. 304-311, 2005.

[31] F. Horst, "Combining Si-photonics and optical PCB's," in LEOS Annual Meeting Conference Proceedings, 2009. LEOS '09. IEEE, 2009, pp. 14-15.

[32] A. L. Porta, J. Weiss, R. Dangel, D. Jubin, N. Meier, J. Hofrichter, et al., "Silicon photonics packaging for highly scalable optical interconnects," in 2015 IEEE 65th Electronic Components and Technology Conference (ECTC), 2015, pp. 1299-1304.

[33] N. Lindenmann, G. Balthasar, D. Hillerkuss, R. Schmogrow, M. Jordan, J. Leuthold, et al., "Photonic wire bonding: a novel concept for chip-scale interconnects," Optics Express, vol. 20, pp. 17667-17677, 2012/07/30 2012.

[34] S. Hiramatsu and M. Kinosihta, "Optical path redirected multichannel waveguide connectors for surface mount technologies," IEEE Photonics Technology Letters, Vol. 16, pp. 2281-2283, 2004.

[35] K. Watanabe, A. Leinse, D. V. Thourhout, R. Heideman, and R. Baets, "Silica-based optical interposer for Si photonics," in Lasers and Electro-Optics 2009 and the European Quantum Electronics Conference. CLEO Europe - EQEC 2009. European Conference on, 2009, pp. 1-1.

[36] L. Brusberg, H. Schr, der, T. M, pper, and H. Reichl, "Photonic System-in-Package technologies using thin glass substrates," in Electronics Packaging Technology Conference, 2009. EPTC '09. 11th, 2009, pp. 930-935.

[37] B. C. Chou, Y. Sato, V. Sukumaran, J. Sun, V. Sundaram, G. K. Chang, et al., "Modeling, design, and fabrication of ultra-high bandwidth 3D Glass Photonics (3DGP) in glass interposers," in 2013 IEEE 63rd Electronic Components and Technology Conference, 2013, pp. 286-291.

[38] X. Zheng, J. E. Cunningham, I. Shubin, J. Simons, M. Asghari, D. Feng, H. Lei, D. Zheng, H. Liang, C. Kung, J. Luff, T. Sze, D. Cohen, A. V. Krishnamoorthy, “Optical Proximity Communication Using Reflective Mirrors,” Optics Express, Vol. 16, No. 19, PP. 15052 – 15058, 2008.

[39] Cornerstone, http://www.cornerstone.sotonfab.co.uk/mpw-design-rules

[40] Europractice, http://www.europractice-ic.com/SiPhotonics_pricing.php

[41] LETI, https://mycmp.fr/datasheet/silicon-photonic-ics-si310-phmp2m

[42] IHP, https://www.ihp-microelectronics.com/en/services/mpw-prototyping/schedule-price-list.html

[43] AIM Photonics, http://www.aimphotonics.com/mpw/

[44] CMC Microsystems, https://www.cmc.ca/en/WhatWeOffer/Products/CMC-00200-03001.aspx

FIRST GENERATION OPTICAL AND ELECTRICAL PACKAGING

2.1 OVERVIEW OF TEST DEVICE

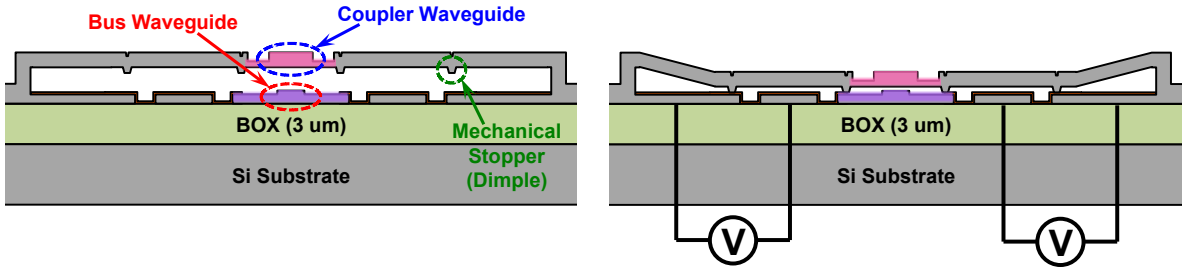


Fig. 2.1. Schematics of MEMS switch unit cell depicting coupler and bus waveguides, the mechanical stoppers and their operating principle during OFF state (left) and ON state (right).

The operating principle of the silicon photonic micro-electro-mechanical-system (MEMS) switch is illustrated in Fig. 2.1 [1]-[3]. The switching element consists of a pair of adiabatic couplers suspended above the bus waveguides. When the device is under OFF state, the adiabatic couplers are suspended at 1 μm above the bus waveguides and do not interfere with the light propagation within the bus waveguides. When a voltage is supplied (ON state), the initially suspended adiabatic couplers are pulled down by the integrated MEMS actuators electrostatically, allowing light coupling from the bus waveguides to the first adiabatic couplers. After a 90 ° turn, light is coupled to orthogonal bus waveguides through the second adiabatic couplers. Mechanical stoppers patterned by photolithography define the coupling distance between adiabatic couplers and bus waveguides precisely. The optical insertion loss and crosstalk are independent of the bias voltage applied to the MEMS actuators. The intrinsic digital operation of MEMS actuators enables large scale digital switching operations and the switch can operate over ten billion cycles without failures [4].

Fig. 2.2 shows the 50 x 50 switching device selected for the first optical and electrical packaging demonstration. In general, for an N x N digital switching device, there are N^2 electrical interconnects (excluding grounds) and 2N optical interconnects. 2500 silicon photonic switches are monolithically integrated on silicon-on-insulator (SOI), within an area of 7.6 mm x 7.6 mm. Each pair of suspended MEMS actuators (Fig. 2.2) are controlled by the bond pad in the centre. This switching architecture is highly scalable as light passes through only one switching element regardless of the switch size. The grating couplers implemented on the switch device have a uniform pitch of 640 nm and a duty cycle of 50 % for optimum coupling of TE-polarized light. Although this device was designed for TE-polarized light, it has been reported that polarization insensitive switches can be demonstrated using the same silicon photonic MEMS switching architecture [5]. Device level characterisation has shown a sub-microsecond switching time (approximately 3 orders of magnitude faster than commercial 3-D MEMS switches), broad spectral bandwidth (1400 – 1700 nm), high extinction ratio (> 50 dB) and digital switching characteristic.

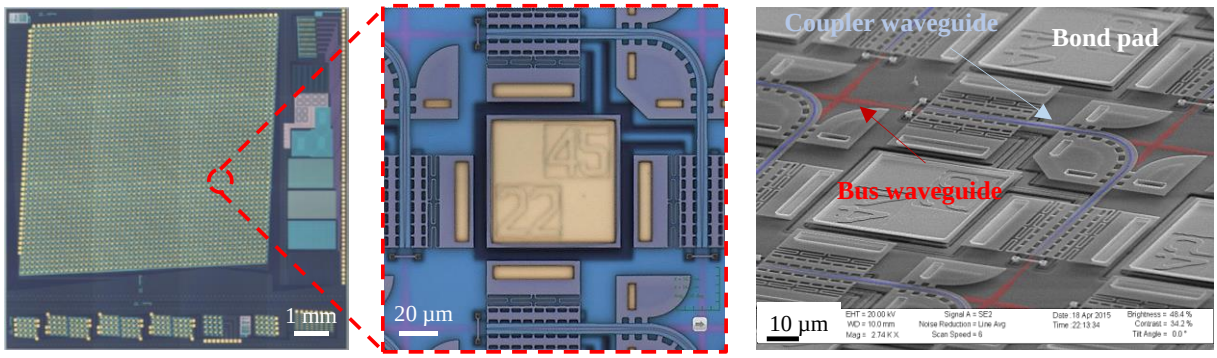


Fig. 2.2. Overview of the 50 x 50 switching device (left) used in packaging demonstration and a switch unit cell under optical (middle) and scanning electron microscope (SEM) (right).

In every packaging activity, be it electronics or silicon photonics, complete understanding of the problems, challenges and availability of equipment and materials are important to arrive at a solution. First of all, packaging of MEMS devices are typically more

challenging than conventional electronics as delicate movable structures which are sensitive to particles are involved [6] - [9]. Secondly, in order to realize the full potential of the switching device, there is a need to address the large number of electrical ports. For instance, an N x N switching device will require N^2 electrical interconnects at the test board interfacing the device and end user. The density of electrical bond pads to be connected and their locations in the centre of the device do not allow straightforward wire bonding onto the test board as long wires can lead to sagging and shorting.

At the same time, exposed and suspended MEMS structures located at the four corners of electrical bond pads do not allow the use of material that can leave residues such as solder flux [10], [11] and polymer resin such as glob top to keep the wires rigid and in place or under-fill to improve solder strength. Finally, there is a mismatch between the device and printed circuit board (PCB) design rules, making direct flip-chip bonding onto the board challenging. Difference in coefficient of thermal expansion (CTE) between silicon (2.9 ppm/K) and PCB (FR4, 14 ppm/K) could lead to reliability issues especially when under-fill materials are not used.

Having properly understood the problems and challenges, the following processes were proposed and illustrated in Fig. 2.3.

a) Solder bump formation on MEMS device
b) Flip-chip MEMS device onto interposer
c) Attach flip-chip assembly onto test board
d) Wire bond from interposer to test board
e) Optical assembly

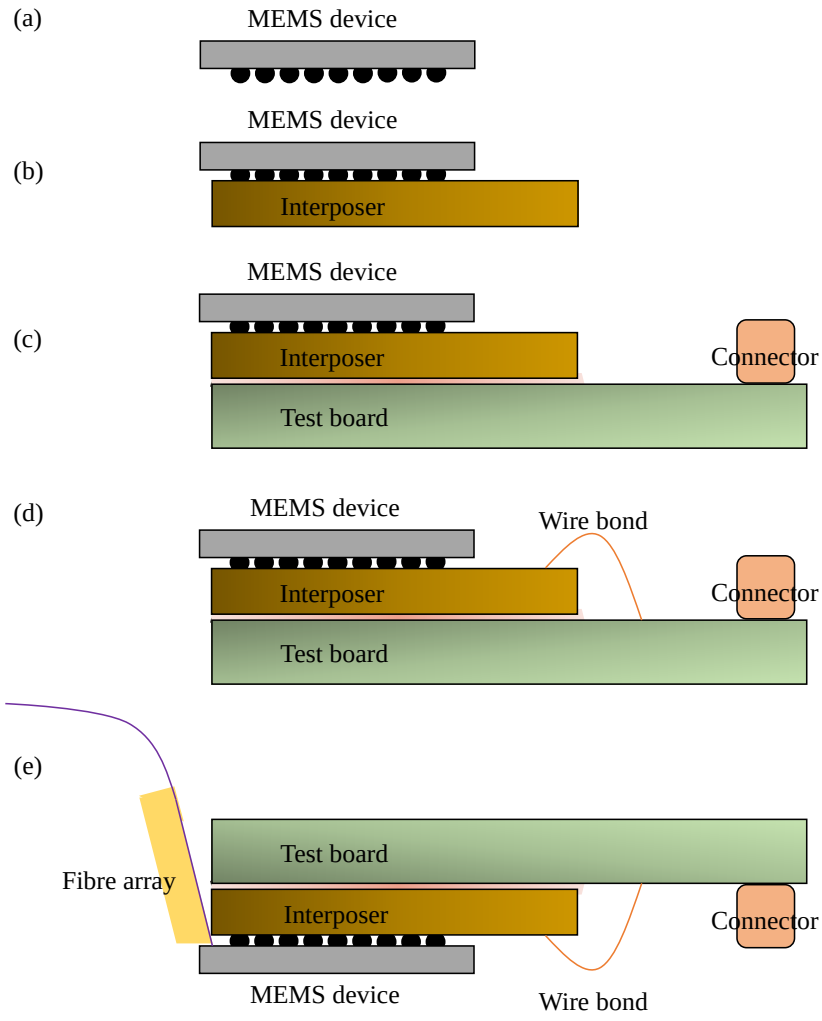


Fig. 2.3. Proposed packaging and assembly process flow for the silicon photonic MEMS device. (a) Solder bump formation on MEMS device, (b) flip-chip MEMS device onto interposer, (c) attach flip-chip assembly onto test board, (d) wire bond from interposer to test board, (e) optical assembly.

2.1 ELECTRICAL PACKAGING DESIGN

In this first packaging demonstration (Test Vehicle 1), we selected a sub-array of 12 x 12 (out of 50 x 50) switching cells for faster assembly, which results in 146 electrical interconnects (including ground pads). Instead of a direct flip-chip-bonding onto the PCB, a 250 µm thick aluminium nitride (AlN, 4.5 ppm/K) interposer was used as an intermediate substrate between the device and board to minimize CTE mismatches. Unlike wire bonding, flip-chip requires a mirrored bond pad orientation on the substrate, thus the design convention (device face up or face down) of the interposer layout should be decided at the beginning and consistently followed. This is particularly important for symmetrical pad-array configuration.

Based on the device layout, only 3 edges of the interposer can be used to populate the electrical bond pads connecting to the PCB, as optical interconnections are needed at one of the four edges. Single metal layer electrical redistribution lines (RDL) were designed using 25 µm line width and space specification to fan-out the 146 electrical interconnects from the device. This design resulted from the decision to connect every alternate bond pad from the device, effectively doubling the pad pitch from 145 µm to 290 µm thus relaxing the routing density. Titanium/platinum/gold (Ti/Pt/Au) was used as the RDL metallization on the interposer as a standard offering from fabrication supplier. The number of switching cells can be readily expanded / scaled up with the use of multi-layer RDL or finer line width and space RDL design rules available with advanced silicon and glass interposers. Simplistically speaking, assuming similar line widths of 25 µm, two metallization layers will be required should the number of electrical interconnect be doubled from 146 to 292 (assuming that the pad pitch remains the same), but this will add to the manufacturing cost as well.

At the same time, a two-layer PCB was also designed to connect the 146 electrical ports from the interposer, with the bond pads arranged in staggered fashion to match the pad

pitch of the interposer. This minimizes the wire bonding length and prevents overlapping and sagging of bond wires, thus preventing electrical shorts. The bond pads were finished with electro-less nickel immersion gold (ENIG) plating for wire bond process-ability and joint reliability. Three pluggable electrical sockets, each capable of taking 50 discrete electrical wires, were placed at one side of the PCB and served as the interface for testing and characterisation. The final design of the ceramic interposer and PCB are shown in Fig. 2.4. The electrical assembly was then matched and confirmed with optical assembly before components manufacturing were committed.

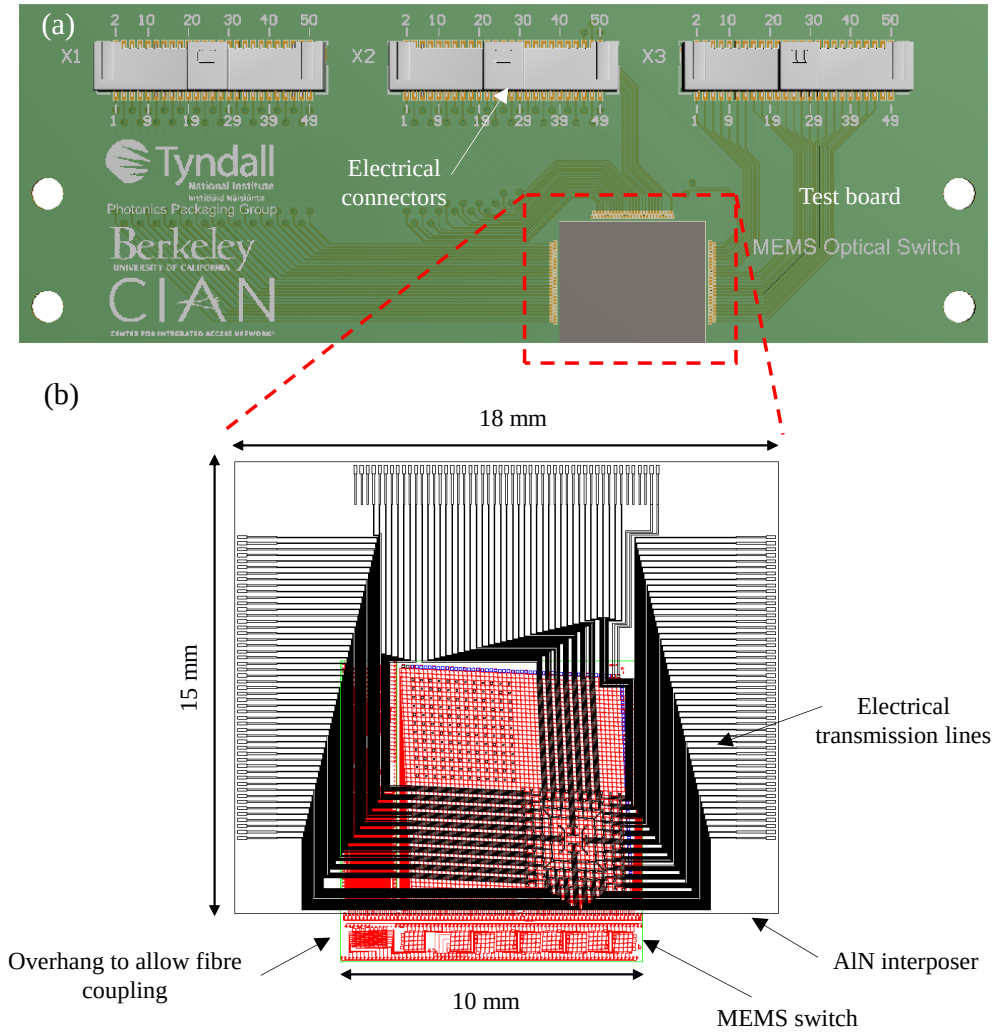


Fig. 2.4. Design of (a) ceramic interposer to fan-out 12 x 12 electrical interconnects located at the bottom right quadrant of the device and (b) printed circuit board (PCB) assembly.

2.3 OPTICAL PACKAGING DESIGN

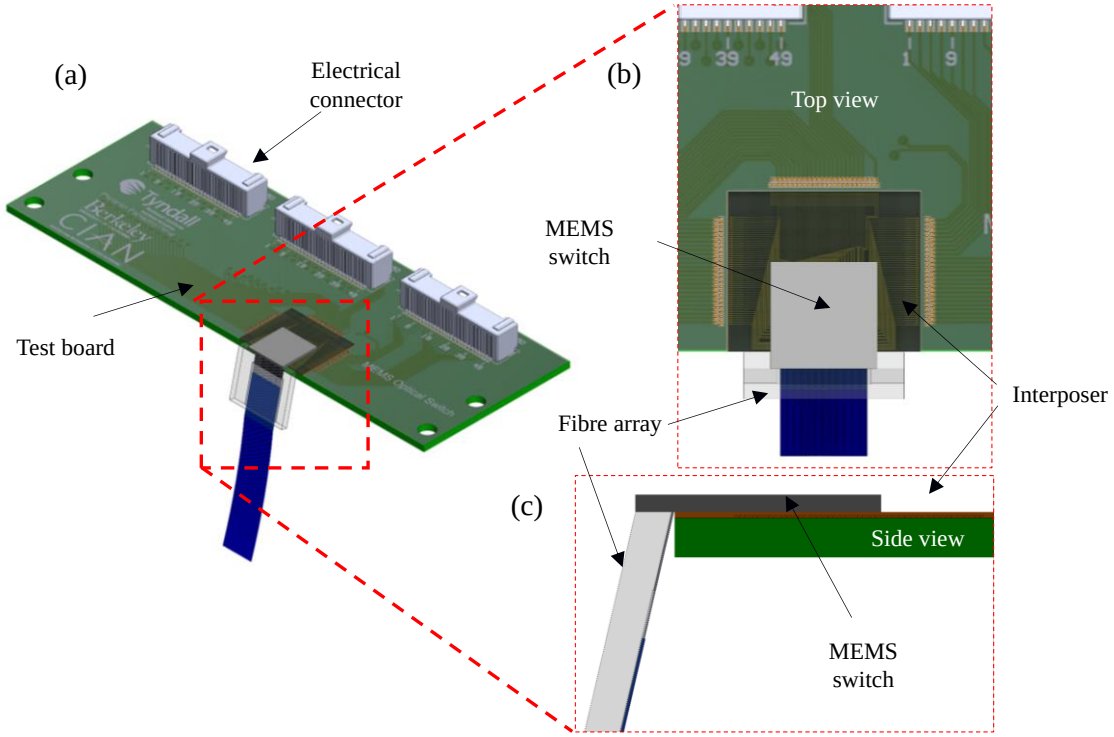


Fig. 2.5. 3-D SolidWorks models showing (a) the expected package assembly, (b) top view of the model showing FA alignment onto device, interposer and PCB and (c) side view of the model showing that only a lidless fibre will be able to couple to the device gratings due to proximity to interposer edge.

Similar to electrical packaging, there is also a need to address the large number of 2N optical interconnects needed for an N x N switching device. In this packaging demonstration, there are 36 optical ports serving as input, through and drop ports which can only be accessed using a 64-channel fibre array (FA), owing to the device configuration. The PCB, FA and mechanical housing (not shown) were put together using SolidWorks in 3-dimensions (3-D) during the design stage to confirm the optical assembly (Fig. 2.5).

The model made clear that the close proximity between the grating couplers and the interposer edge would not allow a typical FA with top lid to reach the couplers. Although a

planar coupling approach would have solved this issue, a high polished angle (51.5 °) FA could not be sourced during the current project phase due to the large array size. High angle polishing, in which individual fibres are resin-fixed on the V-groove, proved to be challenging as some fibre peel off was observed [12]. Thus, a 13 ° polished lidless FA was used instead.

2.4 RESULTS AND ANALYSIS

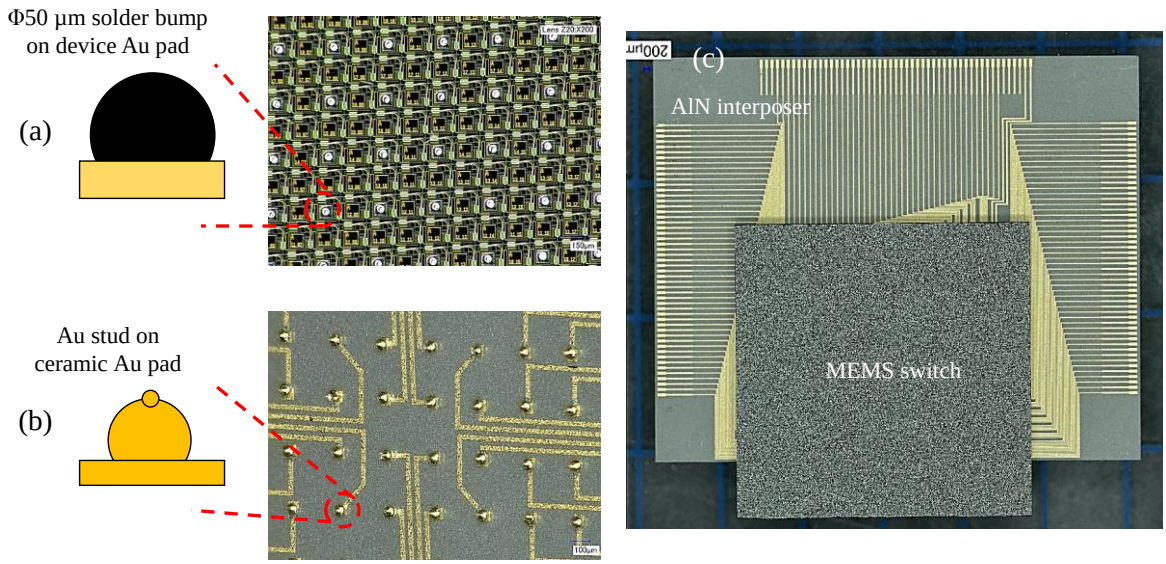


Fig. 2.6. (a) Solder (SAC 305) bumps on switch device and (b) gold (Au) stud bumps on ceramic interposer and (c) flip chip assembly of the device on interposer.

Prior to flip chip assembly, 50 µm diameter solder spheres made of tin-silver-copper (SAC 305, Duksan Hi-Metal Co. Ltd.) were laser jetted onto the device bond pads using PacTech SB^2-SM (Fig. 2.6 (a)). The jetting process was automated by generating a rhombus shape bond map, defining the coordinates where a solder bump was required on the device. Gold stud bumps were also made on an AlN interposer using 0.8 mil (20.3µm) wires and coined (flattened) for co-planarity and flip-chip height control (Fig. 2.6 (b)). The stud bumps were necessary as the interposer did not have top passivation to prevent solder flow and shorting between metal lines. The device was then flipped and aligned onto AlN interposer using a Fineplacer Lamda (Finetech AG) flip chip bonder and reflowed at a peak temperature of 260 °C within a N_2 enclosure. Flux-less reflow was used to prevent residue on MEMS actuators and optical gratings. Similarly no capillary under-fill was used to improve solder joint strength in order to prevent gap filling within MEMS actuators and obstruct their motions. The reflowed assembly is shown in Fig. 2.6 (c).

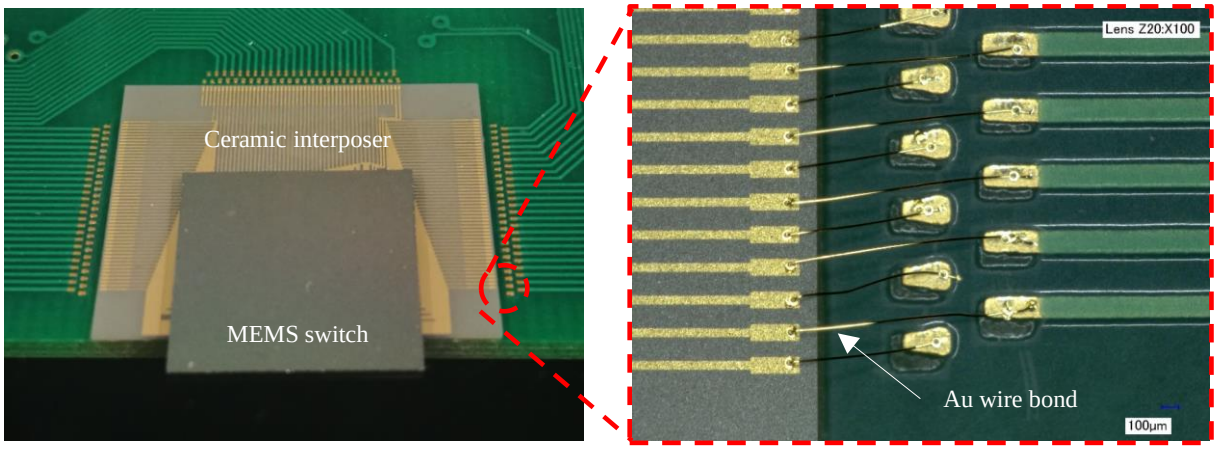


Fig. 2.7. Flip-chip assembly bonded onto PCB (left) and gold wires connecting AlN interposer to PCB (right).

The assembled component (device and interposer) was then attached onto a PCB using thermal epoxy, making sure that the pads on the interposer were aligned properly to within 0.1 mm with those on the PCB (Fig. 2.7). Electrical connections to test sockets were finally formed between the interposer and PCB through gold wires and protected with glob top (Fig. 2.7). The board was finally attached onto a mechanical carrier made for optical packaging. As mentioned in Chapter 1, optical coupling is typically processed as the final packaging step due to sensitivity in index-matching resin to temperature. Glass-transition-temperatures (T_g) of these materials are generally lower than those used for electronic encapsulation and molding. Process temperatures above T_g soften the resin, leading to optical alignment issues [13].

In order to confirm the flip-chip alignment after reflow, samples were analysed through non-destructive and destructive methods. Non-destructive methods such X-ray imaging allows a quick confirmation of the alignment after reflow process. On the other hand, destructive methods such as mechanical polishing can provide more information, including solder joint quality, assembly height and bump height variations across the flip chip assembly. Further analysis after mechanical polishing can also be done using scanning

electron microscopy (SEM) and energy dispersive x-ray microscopy (EDX) to study the solder joint microstructures and reveal fine cracks and delamination not immediately clear through optical microscopy. Fig. 2.8 (b) shows an x-ray image of the flip-chip assembly, in which solder bumps on the device were properly aligned with the stud bumps on the interposer. Mechanical polishing of the assembly also confirmed the bump alignment, the solder-stud joint quality and the assembly height (Fig. 2.8 (c)).

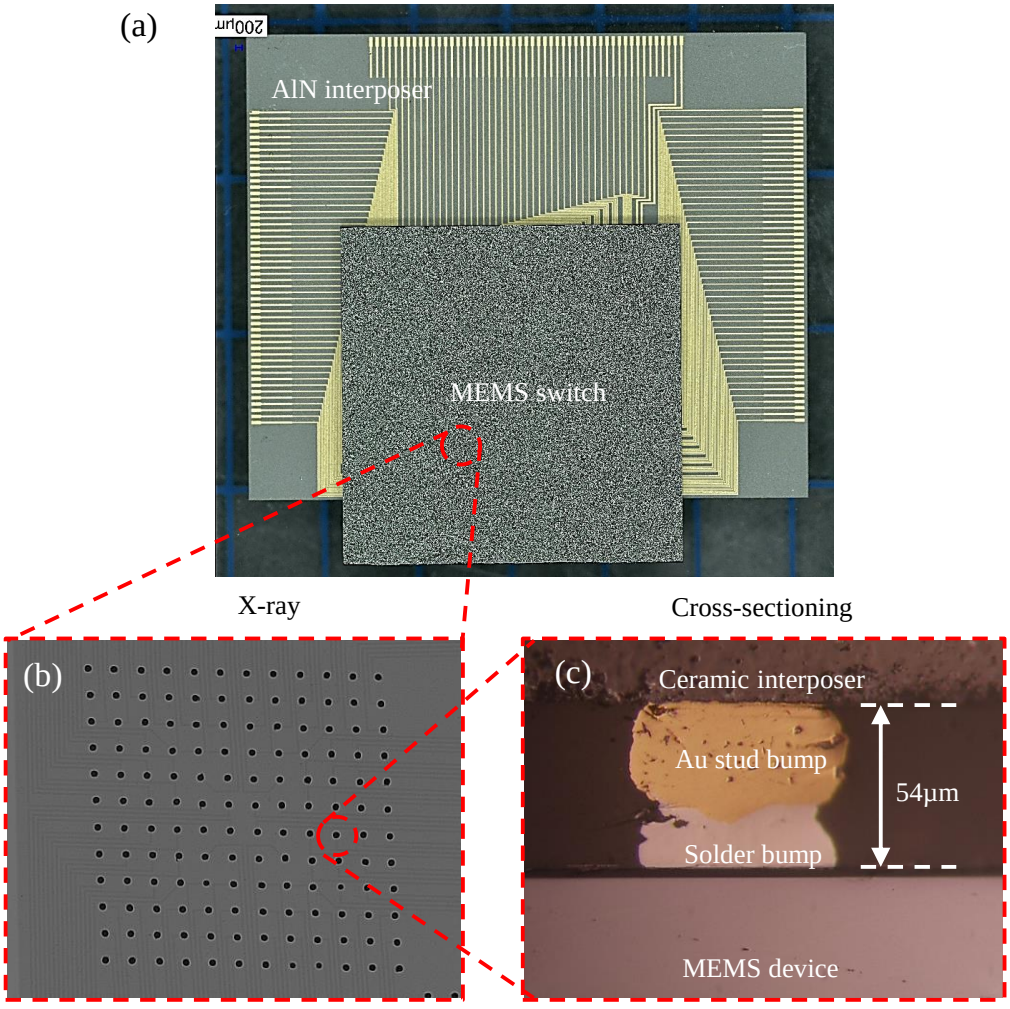


Fig. 2.8. (a) Overall assembly, (b) X-ray of flip chip assembly and (c) mechanical cross-section showing Au stud and solder bump alignment.

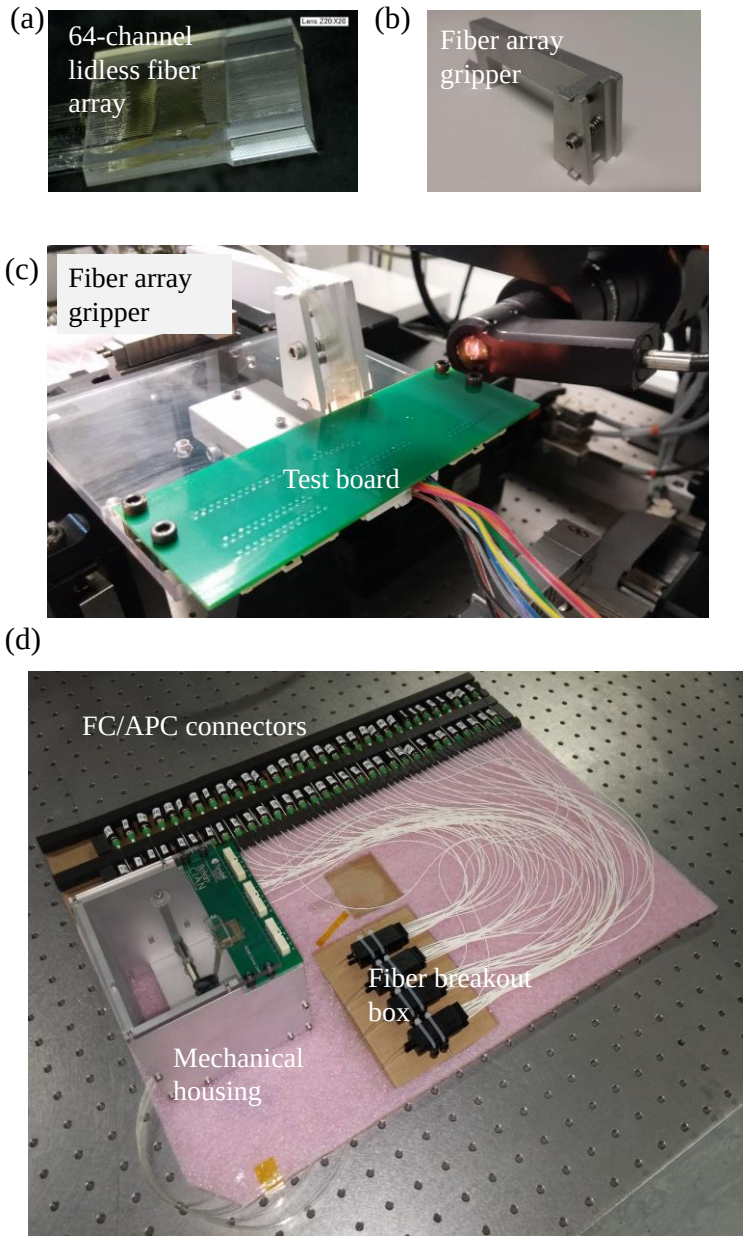


Fig. 2.9. (a) Lidless FA and (b) the FA gripper used during (c) active alignment. (d) The fully assembled optical switch package completed with mechanical housing.

After electrical assembly, the lidless 64-channel FA (Fig. 2.9 (a)) was coupled near-vertically at 13 ° to the device gratings through active alignment using a 6-DOF alignment system from Newport Corp (Fig. 2.9 (c)). A gripper (more on this in Appendix) capable of handling a large FA was designed and fabricated (Fig. 2.9 (b)). Due to the large width of FA, the alignment process becomes more challenging even with the assistance of shunts on the

device. The FA had to be slowly adjusted to make sure that it was parallel to the gratings plane, because a larger gap between FA and grating couplers will lead to higher insertion loss. Index-matching resin (NOA 61, Norland) was then applied to fill the air gap between the FA and grating couplers before finishing with OP-4-20632 (Dymax) at the edges for mechanical strength. Extra care and precise dispensing of optical resin were needed to prevent the resin from flowing into the flip-chip gap.

Finally a fibre post was attached onto the carrier, fixed with room-temperature-curing resin and transferred to a mechanical housing to maintain the integrity of the assembly. The fully assembled silicon photonic switch package is shown in Fig. 2.9 (d). The packaging assembly had been designed for ease of characterisation using long fibre terminated with FC/APC connectors. For commercial application, MTP or MPO connectors can be used as optical fibre termination to keep the package lean.

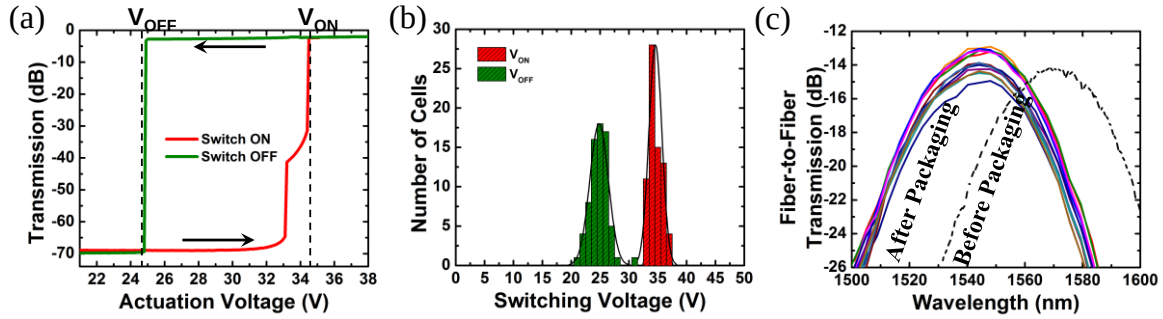


Fig. 2.10. (a) Measured transmission as a function of bias voltage of a switch cell, (b) switching voltage distribution of 70 MEMS switch cells and (c) fibre-to-fibre transmissions of various switch path. Figures from UC Berkeley.

Subsequently, the fully assembled package was tested and analysed. The MEMS actuations were driven using a Keithley 2400 power supply by varying the voltage only. Input light source was supplied by a 1550 nm peak superluminescent diode (SLD) and the fibre-to-fibre transmissions were measured using an Anritsu MS9710C spectrum analyser.

Fig. 2.10 (a) showed the transmission characteristics of a switch cell as a function of bias voltage. The OFF- and ON- state switching voltages were measured to be 34.6 V and 24.8 V with standard deviations of 1.1 V and 1.6 V respectively (Fig. 2.10 (b)). The 10 V difference between OFF- and ON- state voltages is due to intrinsic bias hysteresis of the gap-closing actuators. Meanwhile, fibre-to-coupler loss was measured to be 4.25 dB / facet and fibre-to-fibre transmissions between 12.9 dB to 14.5 dB near 1550 nm were recorded (Fig. 2.10 (c)). The variation in fibre-to-fibre transmission was due to the optical path length difference of the 12 x 12 ports being analysed.

From Fig. 2.10 (c), it can be seen that there is a shift of approximately 25 nm in the peak wavelength, before (~1570nm) and after (~1545) packaging. Similarly, there is a difference in the coupling efficiency before and after packaging. It is worth clarifying here the potential reasons behind the differences. First of all, the spectrum "before packaging" was measured using a UC Berkeley setup while the "after packaging" spectrum was measured using Tyndall's setup. A spectrum that was measured is sensitive to insertion angle, and this can vary depending on the polished angle of the fibre tip, as well as the allowable range of the rotational arm gripping the fibre. Secondly, the designed wavelength of the grating couplers at insertion angle of 13° was intended for 1550 nm (telecom C-band), thus from the results, it was deemed that packaging processes did not affect significantly the intended spectrum in any way. The effect of mechanical strain (photo-elasticity) was therefore not studied in this work.

Lastly, system level characterisation was performed on the package to analyse the switching performance. For bit error rate (BER) experiment, a 10 Gb/s Ethernet data stream was generated by a Virtex-6 field-programmable-gate-array (FPGA) and drove an enhanced small form-factor pluggable (SFP+) transceiver module. The optical data stream from the

SFP+ module was inserted to the switch package. The output signal from the package was sent to the SFP+ module on the FPGA to measure BER. For the longest optical path switching configuration (worst case), BER was measured to be 10^{-11}.

For the switch reconfiguration experiment, the system experiment setup shown in Fig. 2.11 was used. The optical data stream was split and sent to two input ports of the switch package. In the stream paths, an erbium-doped-fibre-amplifier (EDFA) and attenuators were used to compensate the split loss and recover the output power of the SPF+ module for each stream. Two switch cells were controlled to select one of two input streams and send it to an output port. The output stream from the package was split and monitored by a linear detector (yellow trace in Fig 2.11) and a SPF+ module on the FPGA board (green trace in Fig. 2.11). The physical switch reconfiguration time of the package was recorded to be 0.4 μs.

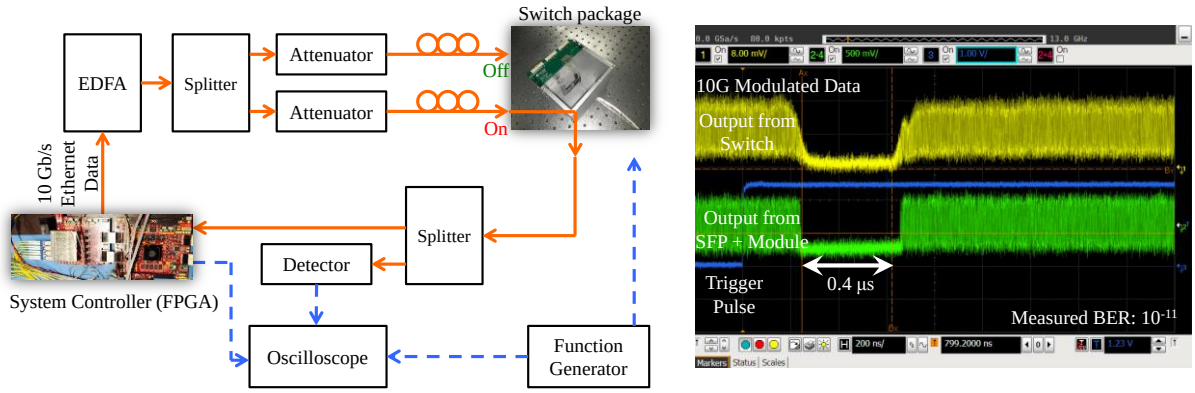


Fig. 2.11. Block diagram of system level characterization (left) and switching performance with 10 Gb/s data stream (right). Figures from UC San Diego.

2.5 CHAPTER SUMMARY

The first MEMS-based silicon photonic optical switch package with 12 x 12 ports was successfully demonstrated using flip-chip configuration. The packaging challenges involving densely populated electrical interfaces were addressed with the use of 25µm line width / space redistribution lines on a ceramic interposer. A flux-less reflow process with laser jetted solder bumps demonstrated good contact and alignment between the device and interposer. A 64-channel SMF-28 lidless fibre array was used to couple to the device grating couplers due to tight access. An average switching ON voltage of 34.6 V with a standard deviation of 1.1 V, switch reconfiguration time of 0.4 µs, and bit-error-rate (BER) of 10^{-11} was demonstrated. The packaging design and concept utilized in this chapter were included in a recent Horizon 2020 project call by European Commission – MORPHIC and was successfully funded.

2.6 REFERENCES

[1] S. Han, T. J. Seok, N. Quack, B. -W. Yoo, and M. C. Wu, "Large-scale silicon photonic switches with movable direction couplers," *Optica*, vol. 2, no. 4, pp. 370-375, 2015.

[2] T. J. Seok, N. Quack, S. Han, R. S. Muller, and M. C. Wu, "Highly Scalable Digital Silicon Photonic MEMS Switches," *Journal of Lightwave Technology*, vol. 34, no. 2, pp. 365-371, 2016.

[3] N. Quack, T. J. Seok, S. Han, R. S. Muller and M. C. Wu, "Scalable Row/Column Addressing of Silicon Photonic MEMS Switches," *IEEE Photonics Technology Letters*, Vol. 28, No. 5, p. 5610564, 2016.

[4] T. J. Seok, N. Quack, S. Han, R. S. Muller, and M. C. Wu, "Large-scale broadband digital silicon photonic switches with vertical adiabatic couplers," *Optica*, vol. 3, no. 1, pp. 64-70, 2016.

[5] S. Han, T. J. Seok, K. Yu, N. Quack, R. S. Muller, M. C. Wu, "50 x 50 Polarization-Insensitive Silicon Photonic MEMS Switches: Design and Experiment," *European Conference on Optical Communication (ECOC)*, 2016.

[6] R. Ramesham and R. Ghaffarian, "Challenges in Interconnection and Packaging of Microelectromechanical Systems (MEMS)," *Electronic Components and Technology Conference*, 2000.

[7] Y. C. Lee, B. A. Parviz, J. A. Chiou and S. Chen, "Packaging for Microelectromechanical and Nanoelectromechanical Systems," *IEEE Transactions on Advanced Packaging*, Vol. 26, No. 3, pp. 217-226, 2003.

[8] R. Darveaux and L. Munukutla, “Critical Challenges in Packaging MEMS Devices,” *IEEE/SEMI Advanced Semiconductor Manufacturing Conference,* 2005.

[9] Z. Wang, “3-D Integration and Through-Silicon Vias in MEMS and Microsensors,” *Journal of Microelectromechanical Systems*, Vol. 24, No. 5, pp. 1211-1244, 2015.

[10] S. Lim, J. Chou, M. Durham, A. Mackie, “Flux Challenges in Flip-Chip Die-Attach,” *17th Electronics Packaging Technology Conference*, 2015.

[11] M. Durham, H. Jo, S. Lim, J. Chou, A. C. Mackie, “Ultra-low Residue Semiconductor-Grade Fluxes for Cu-Pillar Flip Chip Assembly,” *Chip Scale Review*, Vol. 19, No. 4, pp. 21-25, 2015.

[12] Email communications with Nasser Aghdam, *OZ Optics*, 16th March, 2016.

[13] A. Bachmann, J. Arnold and N. Langer, “Movement Between Bonded Optics,” *Dymax Corporation Technical Report,* www.dymax.com, Sept., 2001.

SECOND GENERATION HIGH DENSITY OPTICAL AND ELECTRICAL PACKAGING

3.1 OVERVIEW OF TEST DEVICE

The general operating principle of silicon photonic MEMS switch has been briefly discussed in Chapter 2, and readers are recommended to refer to the chapter or references [1], [2] for more details. The major difference between the previous and current generation silicon photonic MEMS switch lies in the actuation format. In the former configuration, MEMS switch cells are individually actuated, thus an N x N switch matrix relies on N^2 electrical ports to function. The current switch on the other hand exploits the inherent hysteresis of the electrostatic MEMS actuator, effectively reducing the required electrical ports to 2N, and has been termed row/column addressing [3].

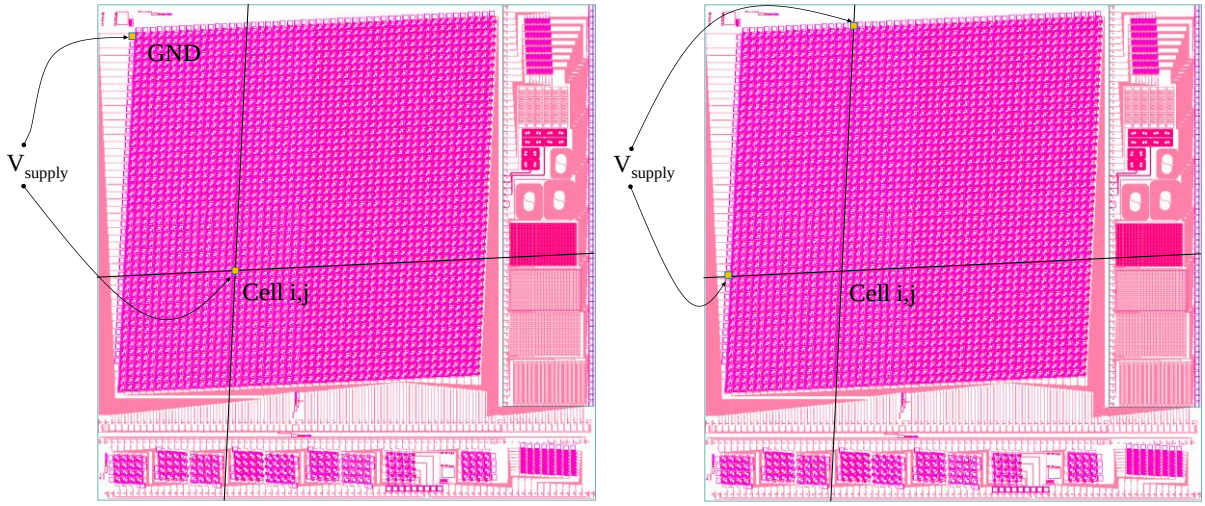


Fig. 3.1. Illustration of individual (left) versus row/column (right) addressing approaches on silicon photonic MEMS switch. Individual addressing requires 2500 electrical ports while row/column addressing requires only 100 electrical ports.

In order to illustrate the difference between individual and row/column addressing and the latter's benefits; consider the MEMS switch package demonstrated in Chapter 2. In individual addressing scheme (Fig. 3.1), an electrical interface is located right beside the MEMS actuators within the same cell, with the common ground located outside the MEMS cells. Direct electrical access is required drive any MEMS switch cell, thus a 50 x 50 switch package would require an interposer and a test board that can accept 2500 electrical ports for a full demonstration.

However, through row/column addressing (Fig. 3.1), direct electrical access to individual MEMS cell is no longer required through the application of a "floating voltage" across the row or column of MEMS cells. A cell will only be activated when the "floating voltage" of a row and column coincide. This approach allows electrical interfaces to be located outside the MEMS cell array and reduces them to 100 (2N) instead of 2500 (N^2) for a full demonstration, making it much more attractive from the packaging perspective. Nevertheless, this approach relies on a trade-off between ease of integration and achievable switching speed, as the individual switch unit cells can only be addressed sequentially due to "floating voltage". It is also worth highlighting that row/column addressing does not change the optical interface configuration. The number of optical interfaces will remain as 2N as in individual addressing.

Following the new row/column addressing approach, a 128 x 128 silicon MEMS switch has been designed and fabricated. This new switch contains 512 electrical and 272 optical ports, and is the largest ever demonstrated on silicon photonic platform at the point of writing [4]. The device has been designed with flip-chip packaging configuration in mind, having 512 electrical ports (instead of 256 at 2N configuration) for mechanical stability (Fig.

3.2) and 272 optical ports (instead of 256) for optical fibre alignment (Fig. 3.3). The switch device is shown in Fig. 3.4.

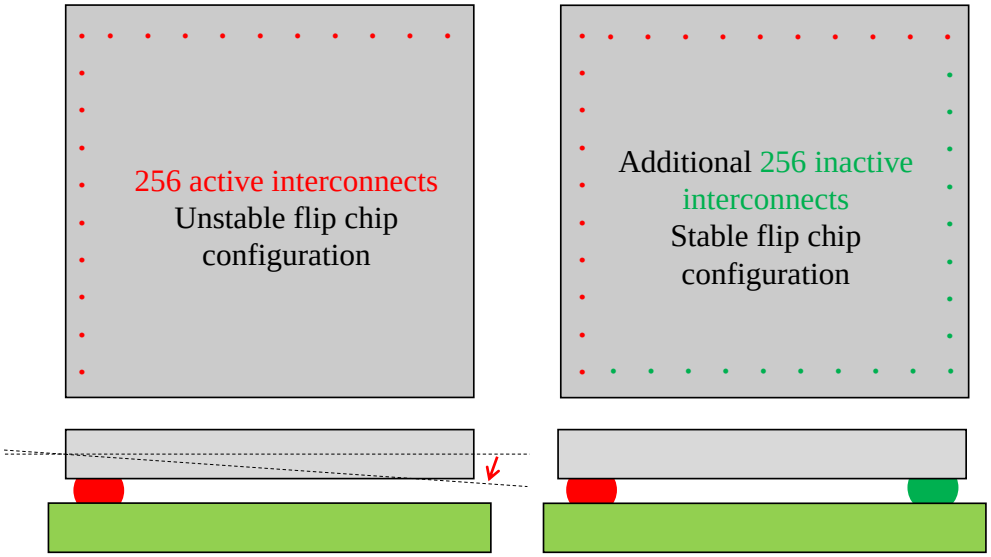


Fig. 3.2. Additional 256 flip chip joints were added for assembly stability. Similar to a chair with only 2 legs, without the additional rows of flip chip joints (in green), the die will be unstable and collapsed from slight handling movements.

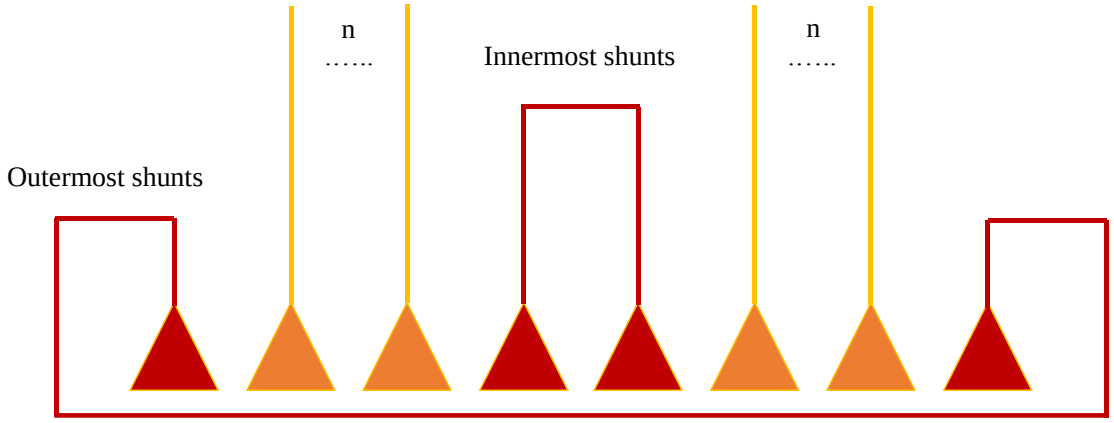


Fig. 3.3. Outermost pairs of optical shunts are typically placed to assist with fibre array alignment during package assembly while inner shunts to extract insertion losses of grating couplers. In this work, 8 pairs of shunts were added for the above reasons, thus increasing the total number of optical ports from 256 channels to 272 channels.

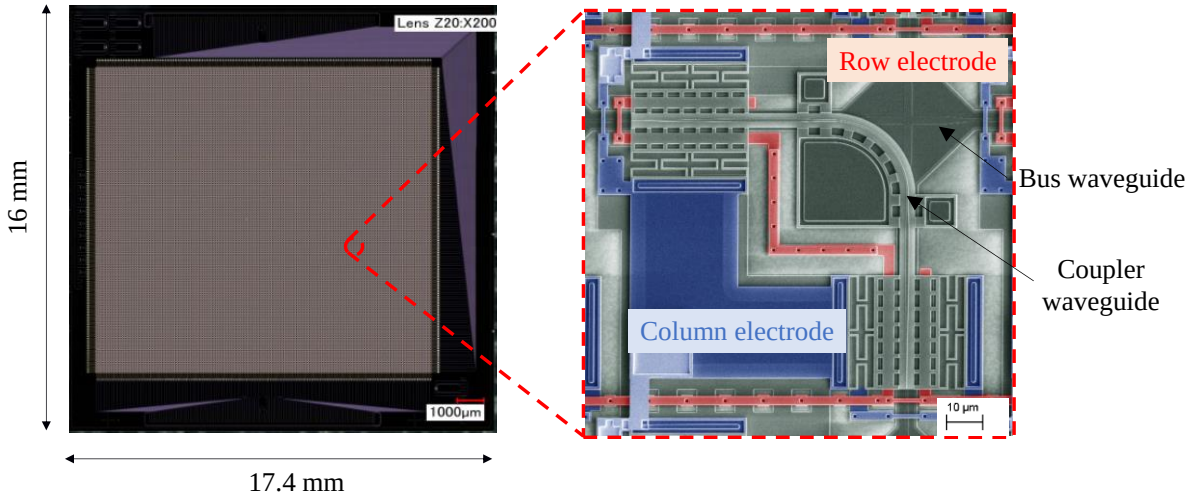


Fig. 3.4. Test device, 128 x 128 silicon photonic MEMS switch used for packaging demonstration and its MEMS switch unit cell.

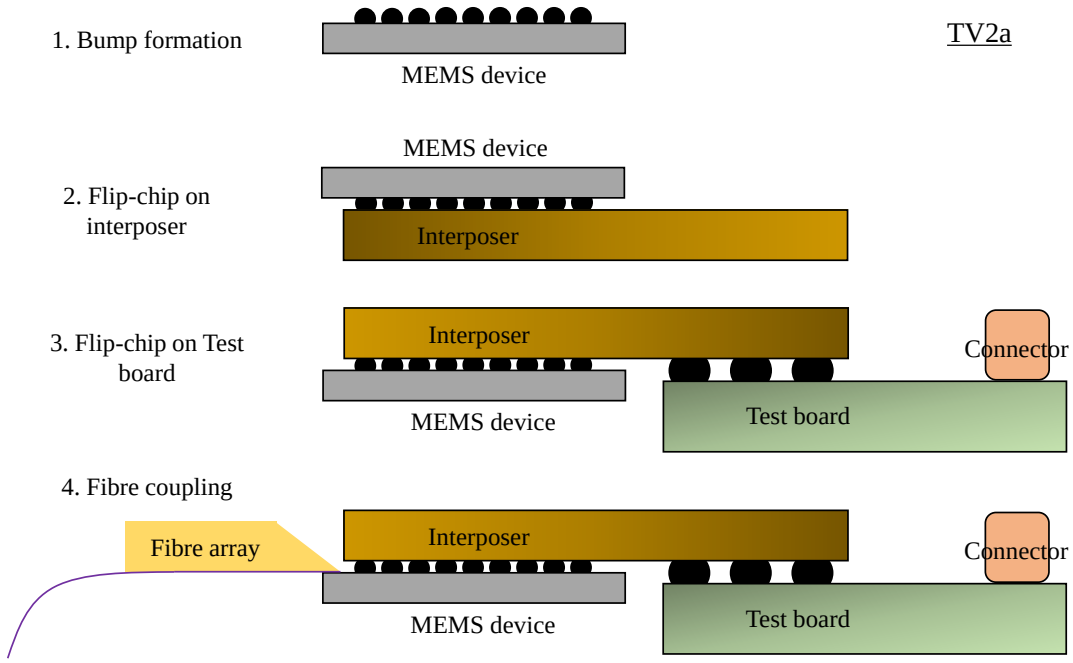


Fig. 3.5. Proposed Test Vehicle 2a (pluggable package) packaging and assembly process flow for the silicon photonic MEMS device. (a) Solder bump formation on MEMS device, (b) flip-chip MEMS device onto interposer, (c) flip-chip assembly onto test board, (d) optical assembly.

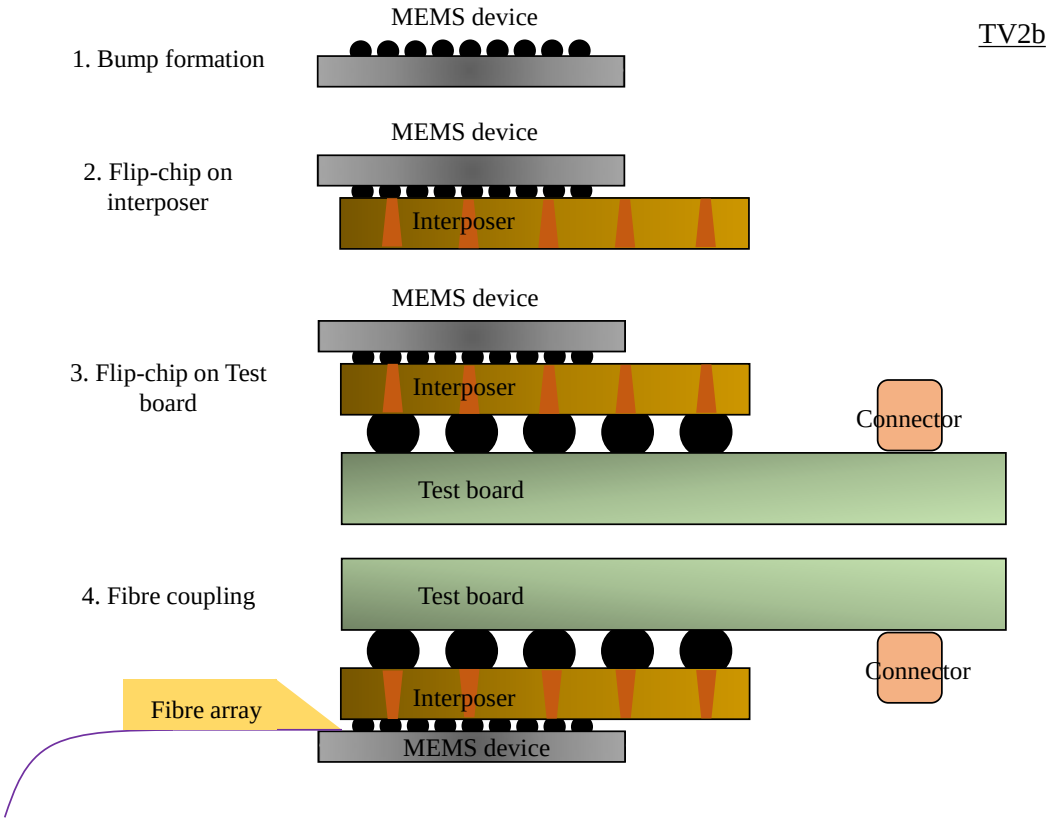


Fig. 3.6. Proposed Test Vehicle 2b (through glass via) packaging and assembly process flow for the silicon photonic MEMS device. (a) Solder bump formation on MEMS device, (b) flip-chip MEMS device onto interposer, (c) flip-chip assembly onto test board, (d) optical assembly.

Similar to the previous chapter, new packaging structures and materials are demonstrated, keeping in mind that the MEMS device is again non-capped (exposed) and is thus sensitive to environment. Full flip-chip configuration is adopted, instead of hybrid packaging consisting of both flip-chip and wire bond that was demonstrated previously. Two types of electrical interposer – pluggable package (Test Vehicle 2a, TV2a) and through glass via package (Test Vehicle 2b, TV2b) will be introduced in the next section. Figs. 3.5 and 3.6 briefly illustrate the respective designs and process flows for respective test vehicles.

3.2 ELECTRICAL PACKAGING DESIGN

Unlike its predecessor (Test vehicle 1), the second generation switch has almost four times the amount of electrical ports to be redistributed (512, compared to 146 previously). These interfaces are distributed along the periphery of the MEMS switch device instead of in a grid format. However, there are 272 optical ports evenly distributed along two opposing edges of the device as well, reducing the freedom of electrical routing to only two directions. Recall that the first generation interposer had the freedom to redistribute the electrical ports from the device in three directions. With these restrictions in mind, the interposers were designed as follows.

3.2.1 PLUGGABLE PACKAGE

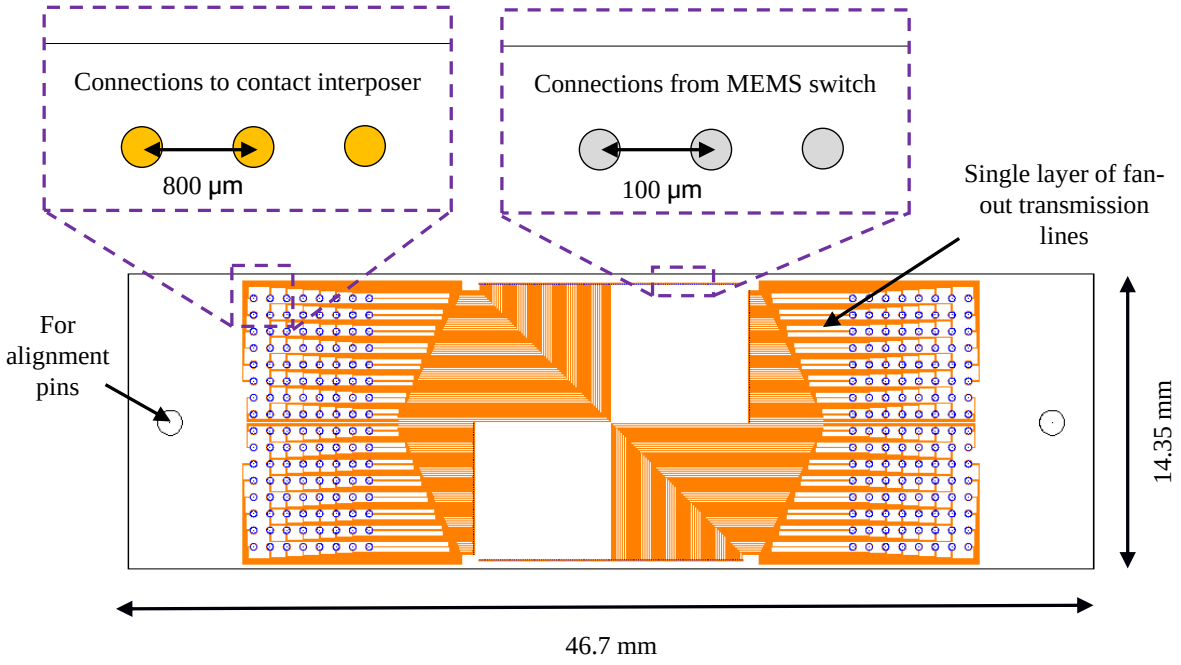


Fig. 3.7. Ceramic interposer design to redistribute 256 electrical bond pads from the MEMS device using single layer metallization with line width and space of 25 µm.

Test Vehicle 2a aims for a pluggable silicon photonic package demonstration (passive optical assembly will be discussed in Chapter 4), akin to a computer processor onto the motherboard. A ceramic interposer was first designed using line width and space of 25 µm on a single layer metallization to route the minimum 256 electrical ports from the MEMS switch device. A pair of secondary contact interposers, each interfacing 64 x 64 MEMS cells, was then incorporated into the ceramic design at two opposite ends (Fig. 3.7). Two holes were added at the ends to insert the alignment pins. The designed ceramic interposer measured 14.35 mm x 46.7 mm. Although the ceramic interposer had been designed for pluggable concept in mind, it can be used for direct flip-chip onto the test board as well.

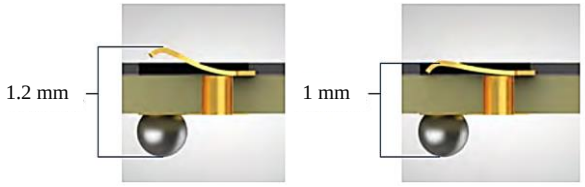


Fig. 3.8. Illustration of the off-the-shelf contact interposer before and after compression.

The contact interposer (Fig. 3.8), as its name implies, has an array of contact springs on one surface to interface with the board, and can be obtained off-the-shelf. A test board was also designed to match these secondary contact interposers with holes for the alignment pins. In order to reduce the size of the board, both surfaces were utilized to place the connectors. PCB routing was done by supplier based on specifications provided, such as the overall PCB size and shape, the location of the components to be placed and the bond pad spacing and metallization required. The pluggable package assembly and test board designs are illustrated in Figs. 3.9 and 3.10 respectively.

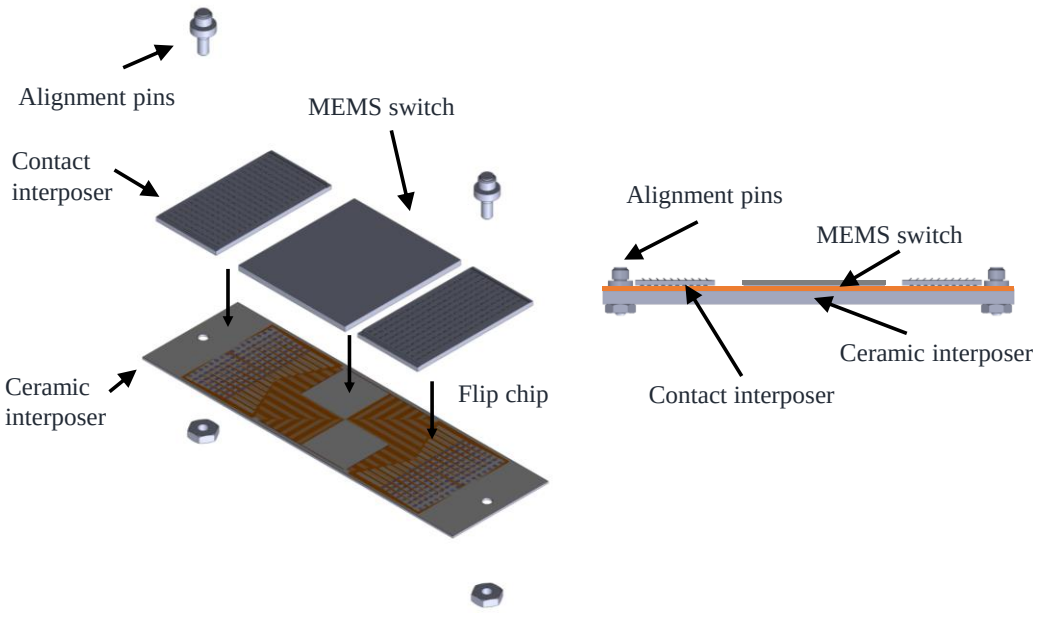


Fig. 3.9. Illustration of the pluggable package assembly with the contact interposers and alignment pins.

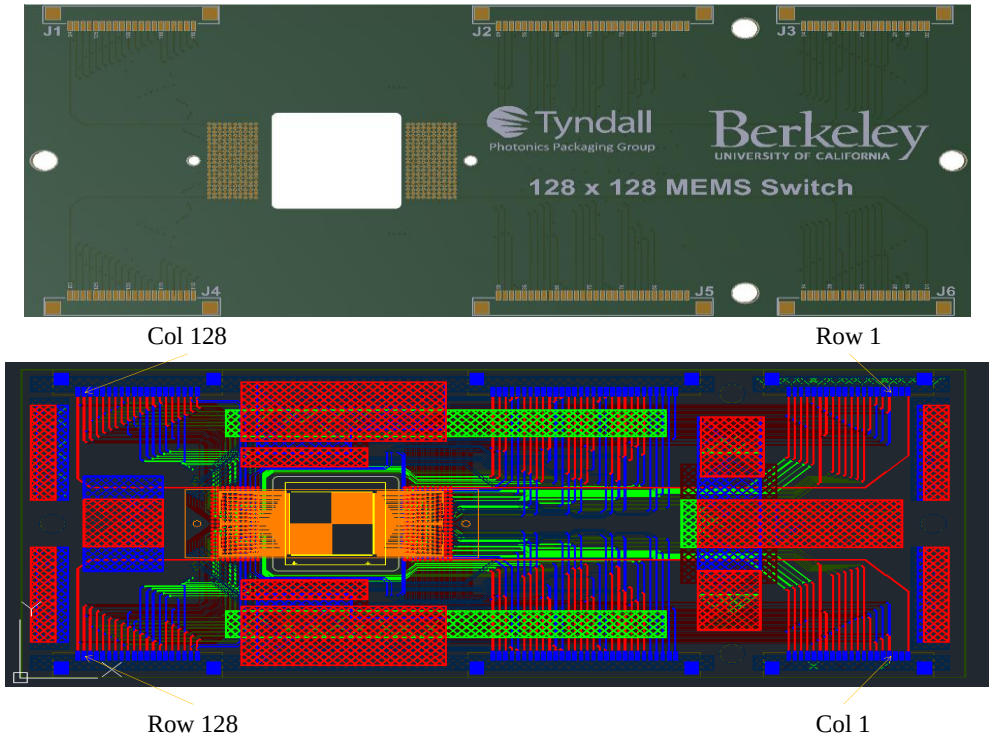


Fig. 3.10. Test board and overall electrical routing design (from MEMS switch device, through ceramic interposer and finally test board) for Test Vehicle 2a.

3.2.2 THROUGH GLASS VIA PACKAGE

Test vehicle 2b on the other hand aims to demonstrate a 2.5D silicon photonic package through the use of through glass via (TGV) interposer with two layers of redistribution lines to route 512 electrical interfaces from the device. Through via interposers drastically reduce the electrical length (resistance), allowing smaller form factor packaging and higher switching performance. Compare to the ceramic interposer from Test Vehicle 2a, the glass interposer measured only 14.35 mm x 21.95 mm but doubled the amount of electrical ports. Furthermore, through glass interposer technology can be integrated with optical waveguides in the future for passive assembly, and this topic will be discussed in Chapter 5. It is should be highlighted here that both the ceramic and glass interposer have a similar width of 14.35 mm to allow sufficient optical alignment access to the ports for subsequent packaging processing.

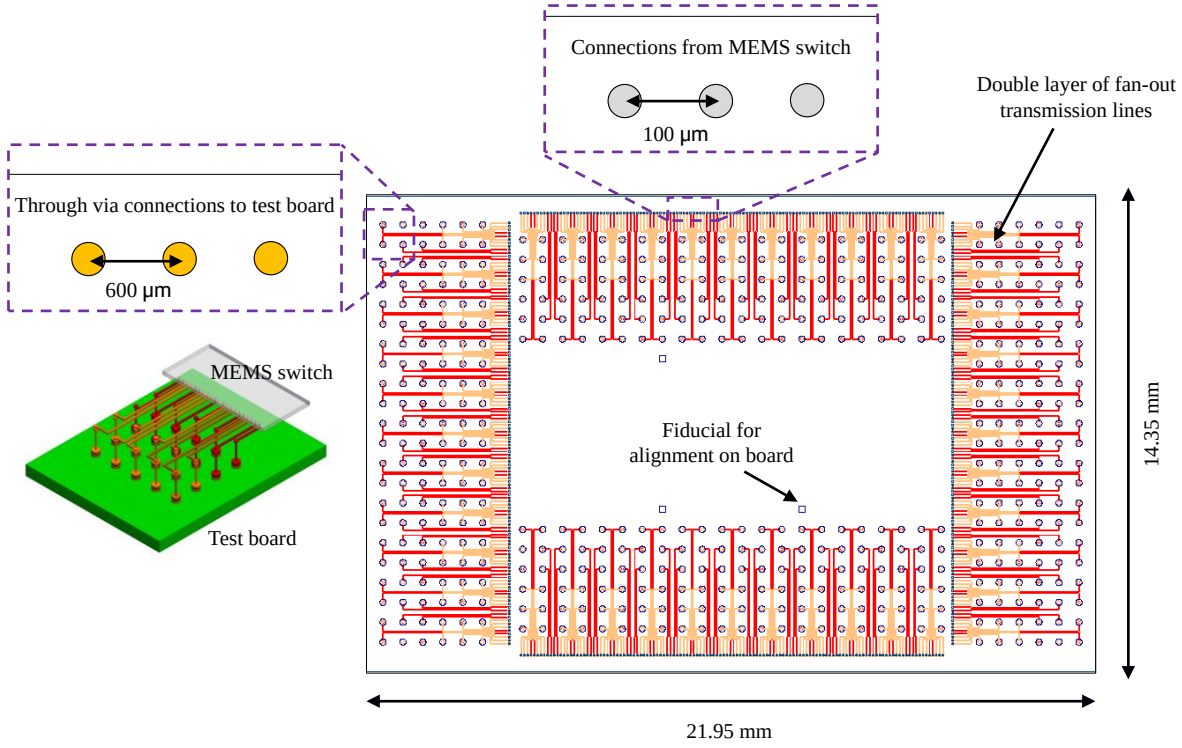


Fig. 3.11. Through glass interposer design consisting of two layers of redistribution lines (orange and red colour) and 512 through glass vias.

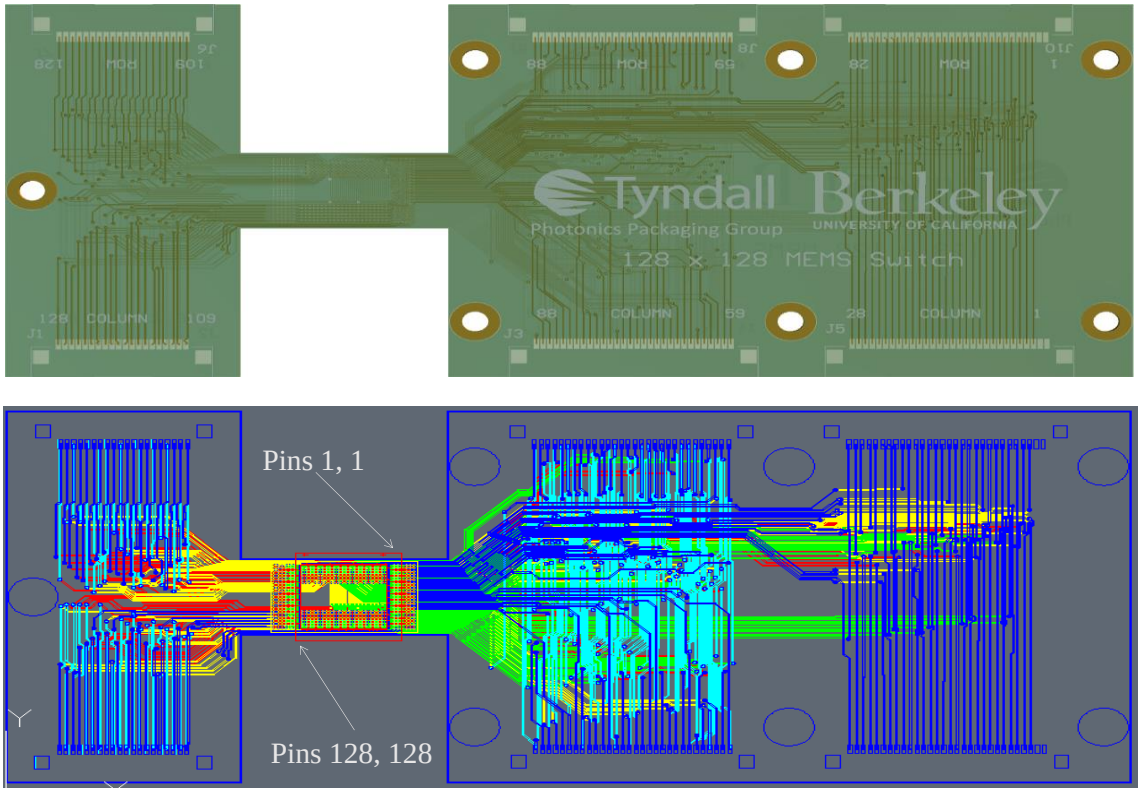


Fig. 3.12. Test board and overall electrical routing design (from MEMS switch device, through glass interposer and finally test board) for Test Vehicle 2b.

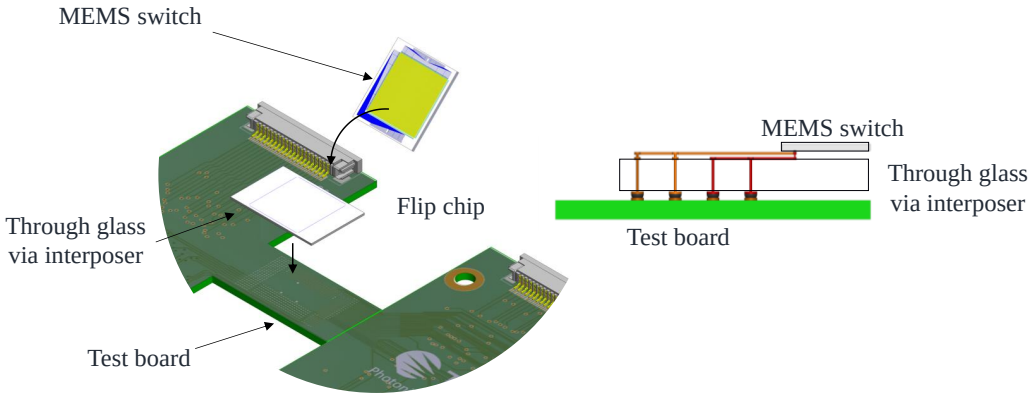


Fig. 3.13. Illustration of the 2.5D silicon photonic MEMS switch assembly with through glass interposer.

This interposer had been designed to route 512 electrical ports from the MEMS switch device using two layers of redistribution lines (RDL) with line width and space of 25

μm on one surface. An alternative design also showed that all the 512 electrical ports can be fully routed in a single layer by reducing the RDL line width and space from 25 μm to 15 μm. These lines were then connected to the opposite surface of the interposer through 512 electrical vias with a diameter of Φ40 μm (Fig. 3.11) to interface with the test board. The board was then designed, keeping in mind optical assembly that requires access from two edges. PCB routing was done by supplier based on specifications provided, such as the overall PCB size and shape, the location of the components to be placed and the bond pad spacing and metallization required. Unfortunately, the neck structure from the H-shape design limits the density of transmission lines that can pass through, and only 256 electrical ports (the minimum contacts) from the through glass via could be routed to external electrical connectors. Alternative fabrication supplier will have to be sourced for in the future for higher density development. Due to the large number of electrical ports, both surfaces of the test board were utilised to place the connectors. The test board design and package assembly are illustrated in Figs. 3.12 and 3.13 respectively.

3.3 OPTICAL PACKAGING DESIGN

Similar to electrical packaging, there are 272 optical ports (256 input and drop ports, 16 alignment and test ports) to be coupled in order to fully demonstrate the MEMS switch device. Due to the large number of optical ports, its pitch had been halved, down to 63.5 μm to reduce the overall device size. Secondly, the optical couplers were improved from a uniform design in Chapter 2 (4.25 dB insertion loss) to a non-uniform design (2.5 dB insertion loss). Lastly, the operating range of the optical couplers has been changed from 1550 nm to 1310 nm for telecommunication band.

This new configuration with smaller optical pitch necessitates the use of an unconventional optical coupling approach for the following reasons. Assuming that the typical 127 μm pitch remained on the device, a v-groove array would have to be at least 18.2 mm wide to cater for 136 optical ports. In the case of vertical coupling, such as that of Chapter 2, the mechanical integrity of such a large fibre array block with 136 optical fibres comes into question. While this could be easily accommodated by changing the coupling configuration to planar, the high angle polishing of 50 ° required will lead to another challenge – fibre peel-off from v-groove or fibre tip chipping as encountered during the previous activities [5].

In light of the possible challenges, an optical interposer based on ion-exchanged waveguides was designed and fabricated instead to match test vehicle 2a and 2b. The pitch of optical waveguides can be freely varied to suit the device as photolithography is used for patterning. Together with the fact that the optical waveguides are buried inside the glass substrate, there will not be a risk of fibre peel-off or fibre tip chipping during high angle polishing. The polished facet was then coated with an aluminium mirror layer to prevent signal loss from optical resin climb during assembly, as the optical channels were buried 10

μm away from the bottom surface. Note that the optical core of a standard lidless v-groove assembly with SMF-28 is located 62.5 μm away from the bottom surface, thus resin climb is of lower risk.

The optical interposer was then edge-coupled at 8 ° to a standard 127 μm fibre v-groove, and terminated with FC/APC connectors for testing. MTP/MPO connectors can be easily integrated for commercial applications in the future. A holder was also incorporated in the optical interposer design for ease of alignment process and package assembly, together with specially designed fibre array grippers (more on these in Appendix). The optical interposer design and fabrication process flow are shown in Figs. 3.14 and 3.15, while the full assembly of test vehicles 2a and 2b are shown in Fig. 3.16.

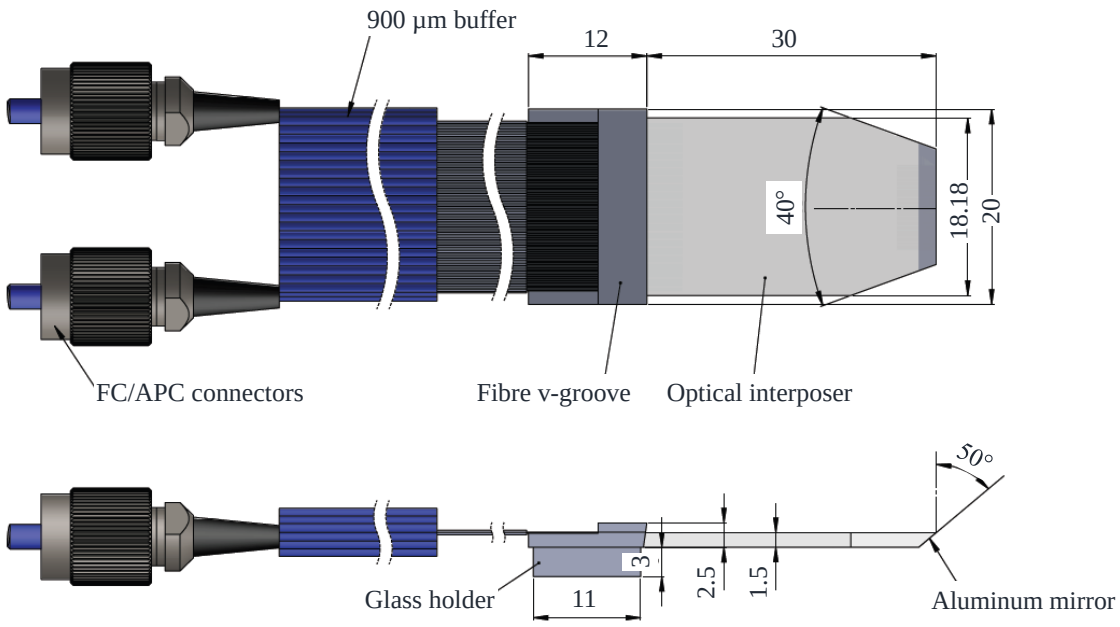


Fig. 3.14. Design of the planar optical interposer with pitch reducing optical waveguides buried underneath the glass surface. Figure from TEEM Photonics based on author's design specifications.

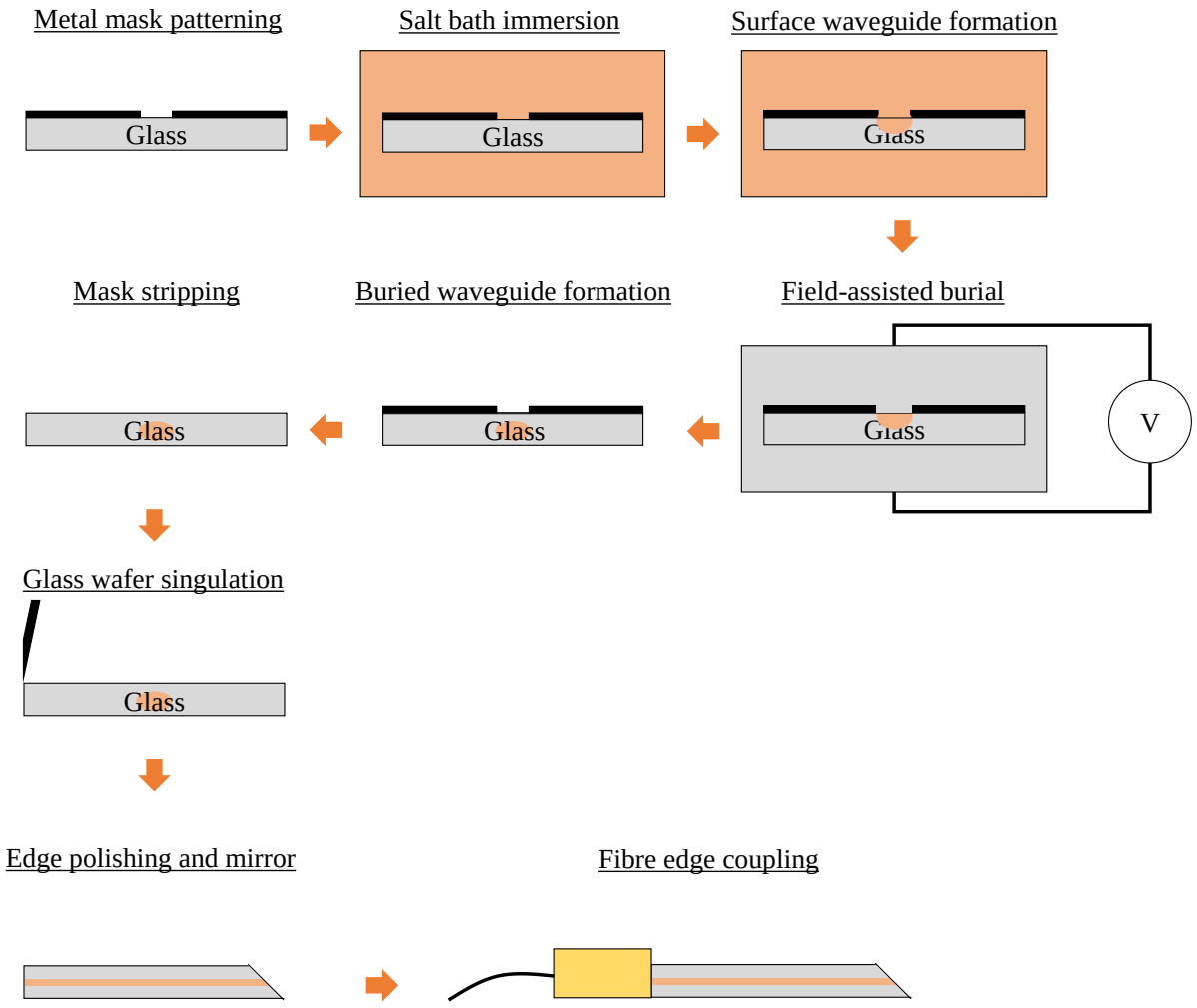


Fig. 3.15. Planar optical interposer fabrication process flow, starting from metal mask patterning all the way to regular v-groove coupling.

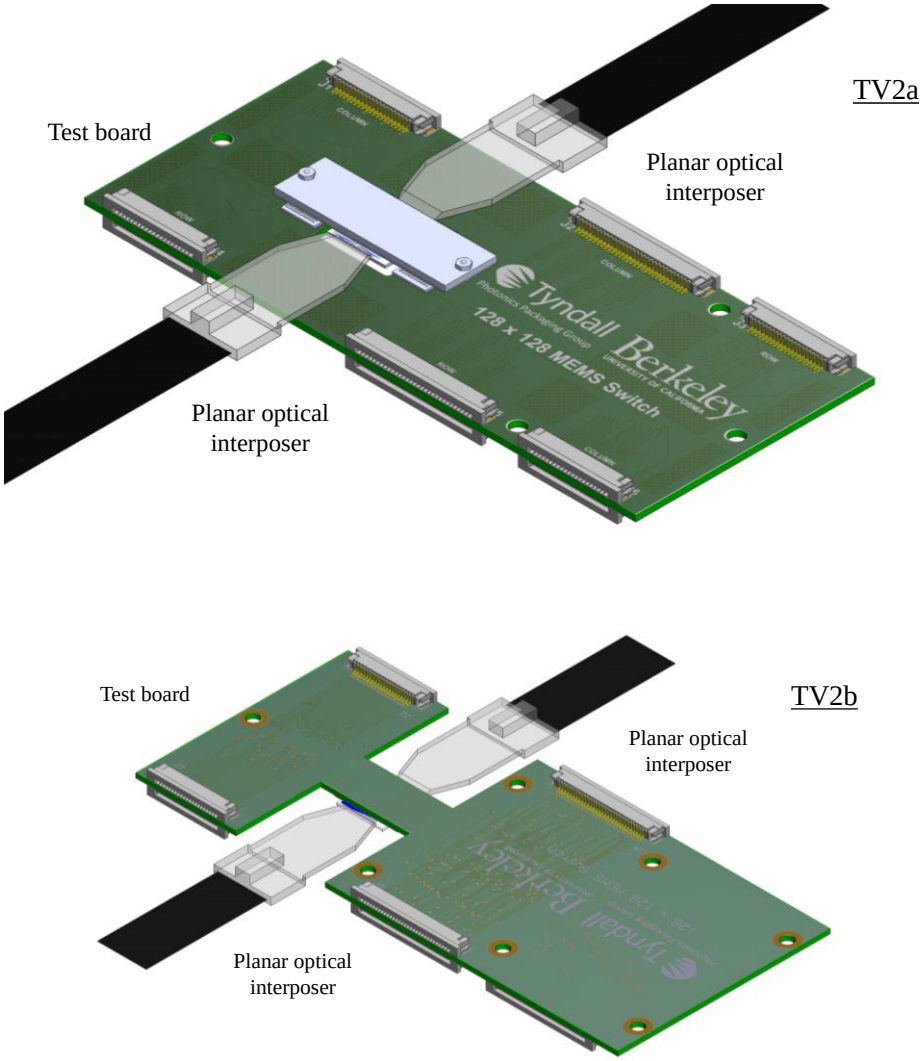


Fig. 3.16. 3-D illustration of the overall test vehicle assembly (optical and electrical) for Test Vehicle 2a – pluggable package (top) and 2b – through-glass-via package (bottom).

3.4 RESULTS AND ANALYSIS

3.4.1 DEVICE POST PROCESSING

Out of fabrication foundry, the bond pads on MEMS switch device comes in tungsten (W) metallization, which cannot be wetted by tin (Sn) from solder ball and formed intermetallic species [6] that dictates solder joints strength. Similarly, W metal pad cannot be wire bonded to form a gold stud, a flip-chip assembly method introduced in Chapter 2. Three metallization schemes – Pt/Au, Cr/Au and Ti/Au were proposed as the adhesion and wetting layers for solder bumping as these metals are inert to chemicals used during MEMS release step. ϕ50 µm tin-silver-copper (SAC305, Duksan Hi-Metal Co. Ltd) solder balls were then laser jetted onto bond pads with the above metallization stack, reflowed to simulate the assembly processes and sheared to obtain the joint strength. This is critical for flip chip bonding, particularly when underfill is not used to fill the assembly gap. The solder joint strength results were then normalised against the bond pad area and plotted in Fig. 3.17. Results showed that Pt/Au and Cr/Au metallization strength are comparable at time zero (as jetted). Following discussions with MEMS device collaborator, Cr/Au was selected as the final bond pad metallization scheme due to availability of sputtering target. Additional process simulations (multiple reflow) found that joint strength of Cr/Au metallization would have reduced from an average of 4.5 gf / sq mil to 3.5 gf / sg mil (1 gf/sq mil is equivalent to 15.2 MPa).

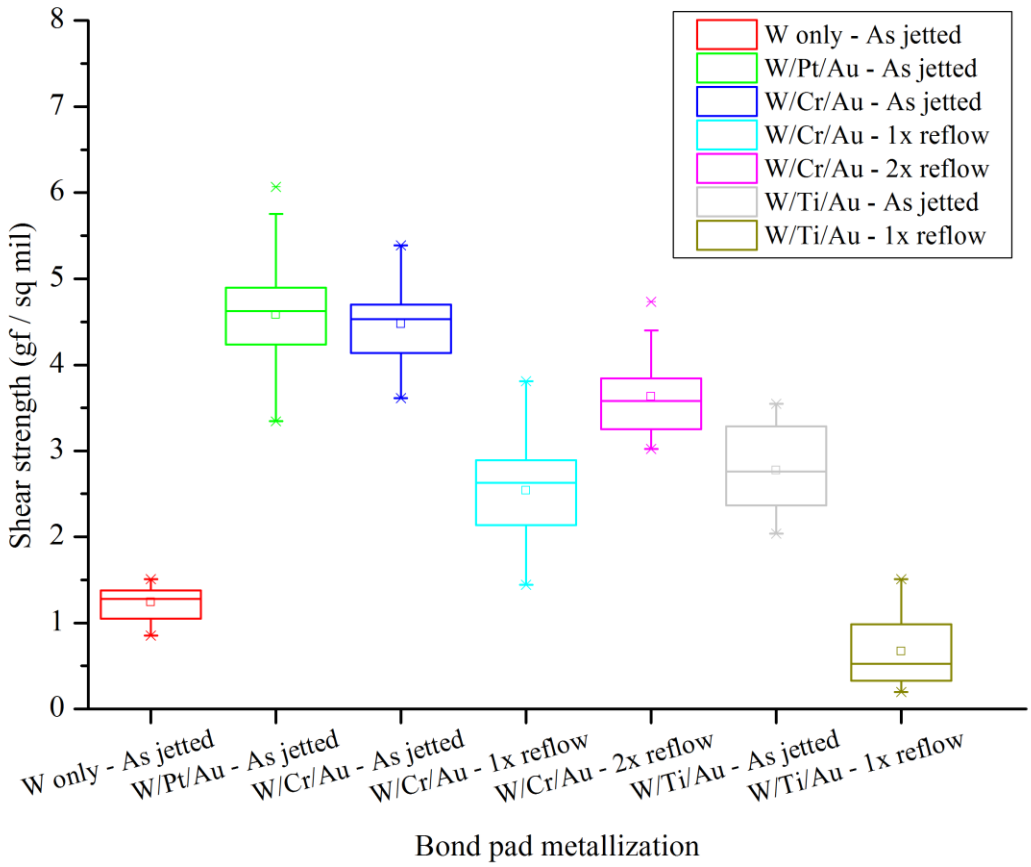


Fig. 3.17. Solder bump shear strength on various bond pad metallization, normalised against bond pad surface area. It can be seen that W/Pt/Au and W/Cr/Au metallization gave the best solder shear strength. The number of solder bump shear performed on all types of bond pad metallization was 20 bumps on 2 samples.

3.4.2 PLUGGABLE PACKAGE ASSEMBLY

Fig. 3.18 shows the assembly process of the pluggable package. The two secondary contact interposers were first aligned and assembled using Fineplacer Lambda onto the ceramic interposer, followed by the MEMS switch. Prior to this, solder bumps had been formed on the MEMS switch's W/Cr/Au bond pads using PacTech SB^2-SM. Fig. 3.19 shows the completed pluggable assembly. X-ray analysis showed good alignment (within 50 µm) between various components on the ceramic interposer. The assembled package was then attached onto an aluminium holder using the alignment pins and can now be plugged onto the test board (Fig. 3.20), followed by optical assembly.

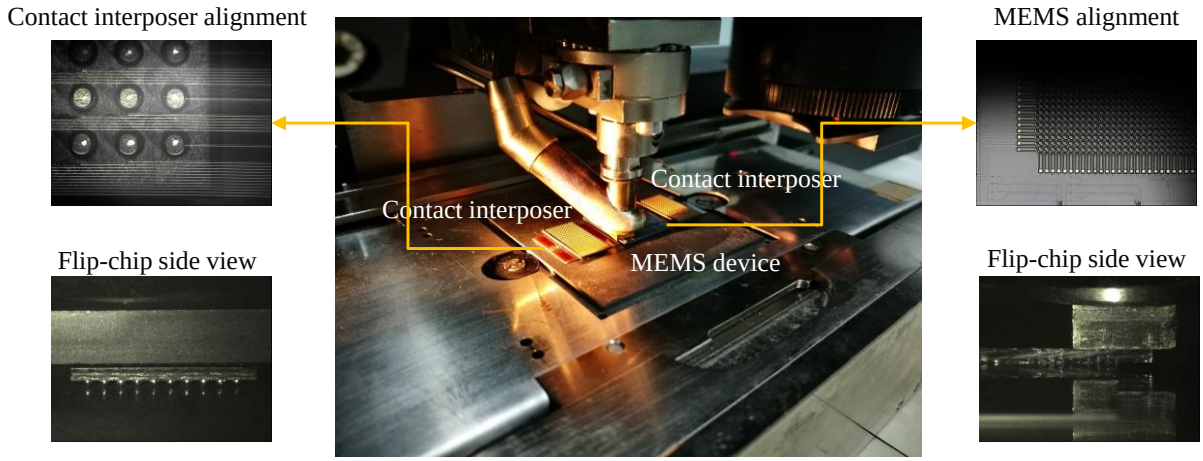


Fig. 3.18. Flip chip processing of the secondary contact interposer and 128 x 128 silicon photonic MEMS switch on AlN interposer.

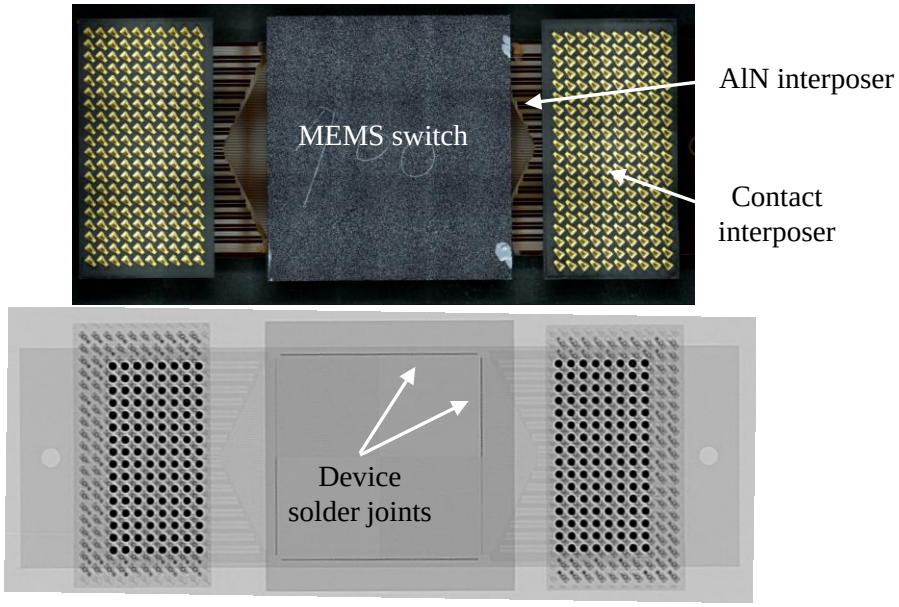


Fig. 3.19. Assembled pluggable MEMS switch package (top) and x-ray image of the assembly (bottom).

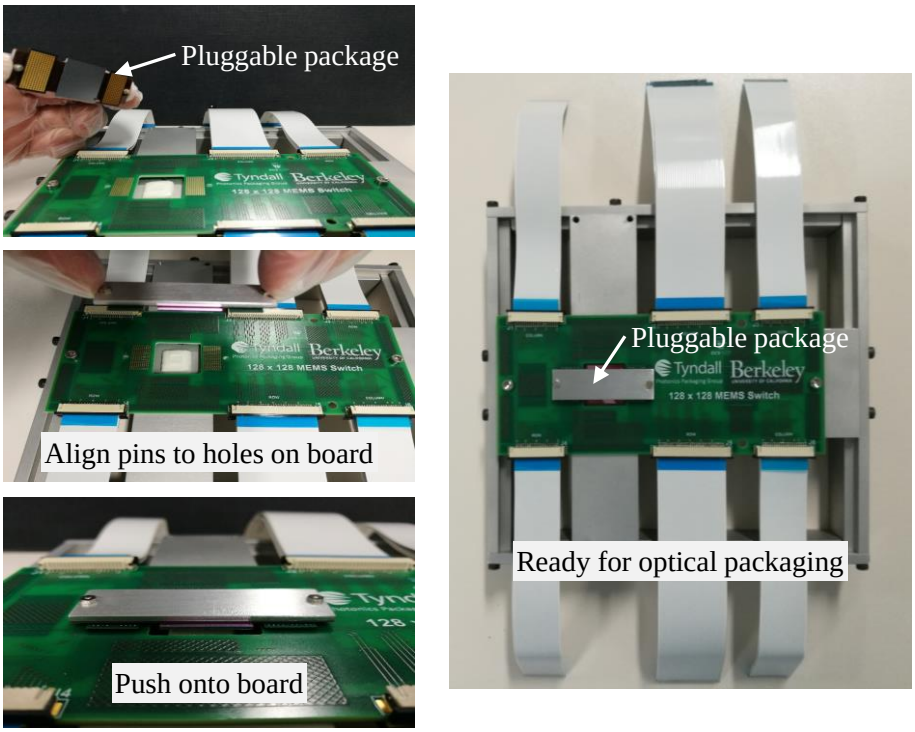


Fig. 3.20. Demonstration of the pluggable package onto test board (counter-clockwise from top left).

3.4.3 THROUGH GLASS VIA PACKAGE ASSEMBLY

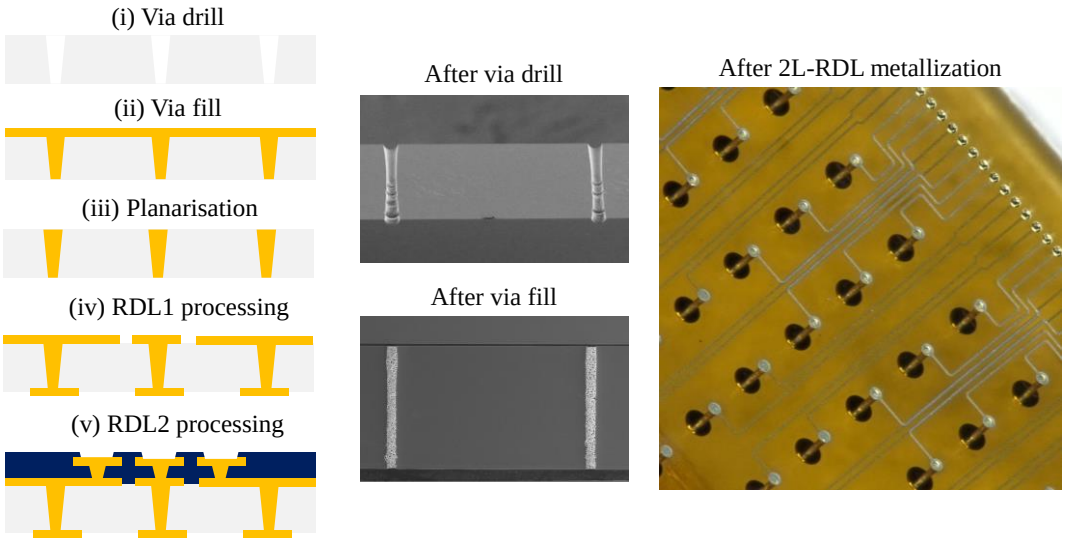


Fig. 3.21. Fabrication process flow (left), cross-sectional SEM images of drilled and filled via (middle) and after RDL metallization (right) of the through glass via interposer.

Fig. 3.21 shows the fabrication process flow of the through glass via interposer. It began with laser drilling on an 8" glass wafer followed by via filling with conductive paste. Chemical-mechanical-polishing (planarization) was then performed to remove excess conductive paste and prepare the wafer surface for subsequent processes such as seed layer deposition, photolithography patterning and copper plating to define the first layer re-distribution lines (RDL1). These processes were then repeated to define RDL2 before the wafer is singulated into individual pieces measuring 14.35 mm x 21.95 mm. The yellowish appearance of the glass interposer was due to three layers of polyimide passivation.

Fig. 3.22 further shows the assembly processes of the MEMS switch, consisting of two-step flip chip alignment using Fineplacer Lambda (Finetech AG) and reflow using LPKF's ProtoFlow S oven. A combination of two different solder materials was used to achieve the two-step reflow – SAC305 for device-to-interposer assembly and Bi58Sn for interposer-to-board assembly. SAC305 has a melting temperature of 217 °C thus will not re-

melt during the second reflow of Bi58Sn, which has a melting temperature of 138 °C. Reflow profile for both materials were carefully configured on the oven to minimize temperature stress on the various components.

Fig. 3.23 further shows the optical and x-ray inspection result, confirming the process alignment fully-melted solder materials between various components. The board assembly was finally attached and secured onto a mechanical mount (Fig. 3.24) to support the optical fibre attachments.

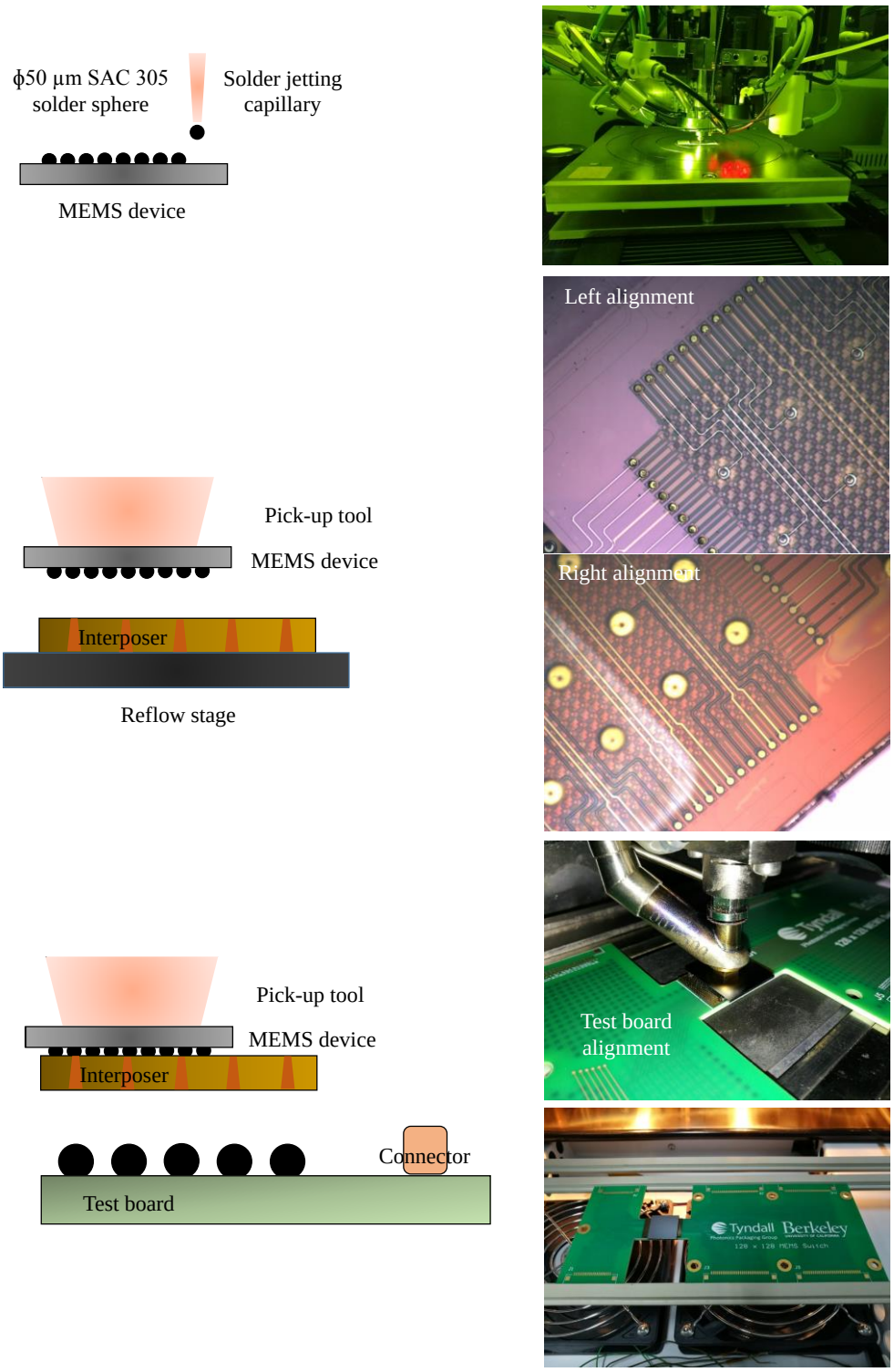


Fig. 3.22. Flip chip assembly processing of Test Vehicle 2b with two-step reflow processing, starting from solder jetting on device (top), followed by device-to-interposer assembly (middle) and finally interposer-to-board assembly (bottom).

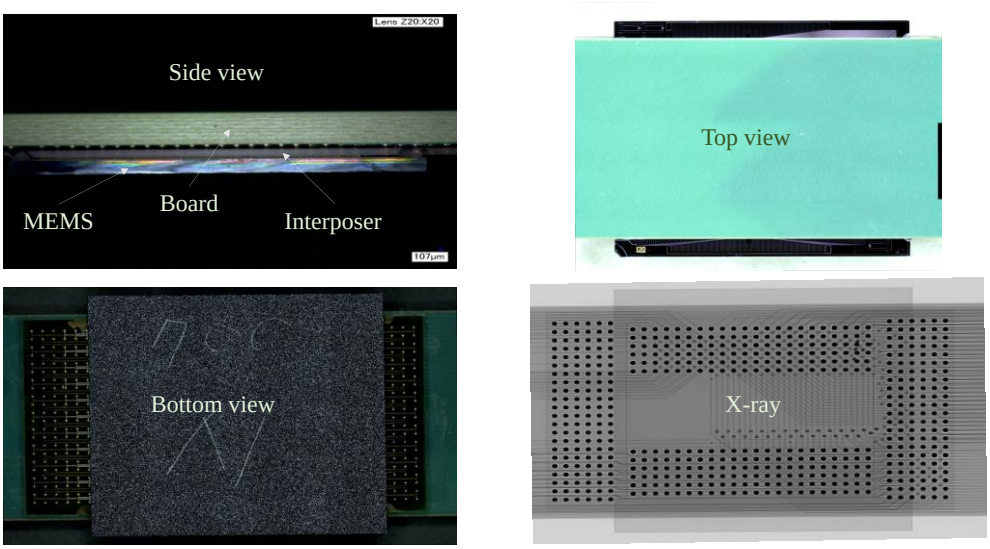


Fig. 3.23. Various optical views and X-ray images of the assembled through glass via MEM switch package.

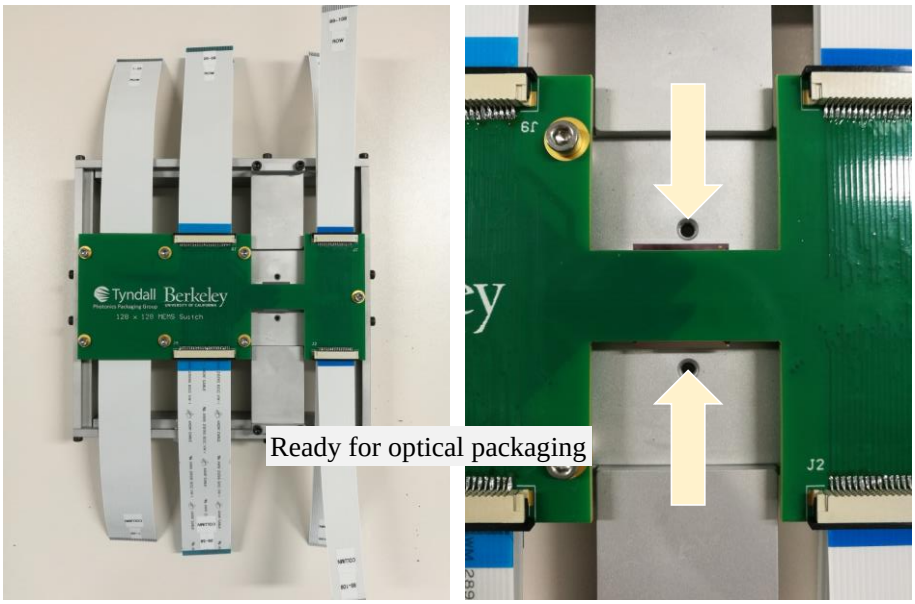


Fig. 3.24. Board level assembly onto mechanical mount, ready for subsequent optical assembly.

3.4.4 ASSEMBLY ELECTRICAL CONNECTIVITY EVALUATION

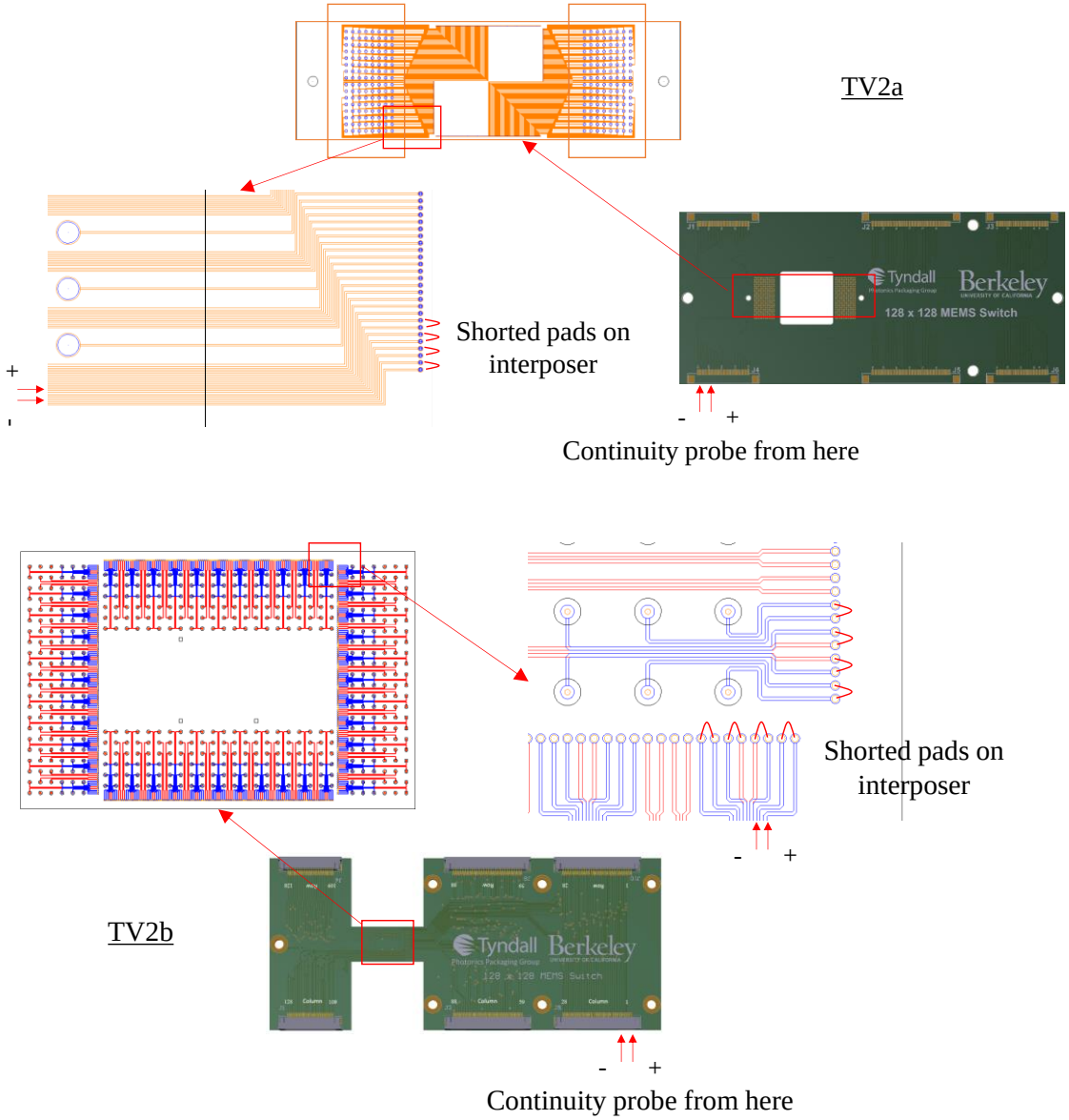


Fig. 3.25. Continuity measurement approaches on TV2a – pluggable (top) and TV2b - glass interposer (bottom) package assemblies.

In order to confirm that the packaging design and processes work as intended for the two types of interposer, continuity check was used. Both interposers were assembled onto their respective test boards and the bond pads interfacing the device were shorted using wire bonds (Fig. 3.25). The number of open/short connections measured on ceramic interposer (TV2a) was 10 on one sample while that on glass interposer (TV2b) was 17 on one sample. The small

sample size was due to the limited number of interposers (10 each were ordered) fabricated for assembly process development and final assembly. This open/short test requires 1. bond wire shorting of interposer pads and 2. soldering onto the test board. A re-use of the interposers was thus not possible.

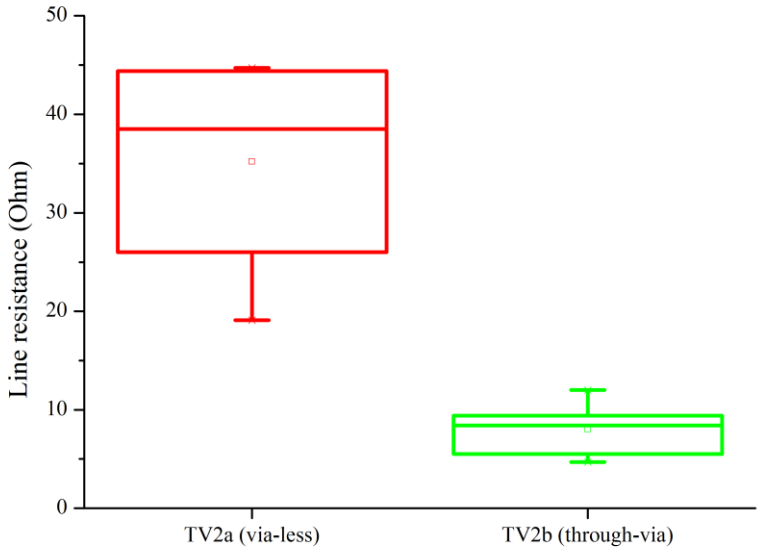


Fig. 3.26. Continuity measurements of pluggable and glass interposer packages show that the electrical packaging components designed and fabricated worked as intended. Test Vehicle 2a has higher line resistances due its much longer transmission lines without vias.

Continuity check of the two assemblies showed distinctly different line resistance, but matches expectation as both interposers have different electrical lengths. Line resistances on the interposer without vias are roughly 3x higher compare to that with vias, thus showing the advantage of through via technology with shorter electrical length (Fig. 3.26). The shortest/longest transmission line on ceramic interposer are 5.5/25.1 mm while that on glass interposer are 2.7/8.5mm including the 0.4mm through via. This shows the viability of a through via approach in reducing line resistances and thus the energy lost during propagation.

This exercise also shows that the packaging design and processes worked as intended with various electrical connections properly connected, and full MEMS switching can be fully demonstrated once the actual device is available in the future.

3.4.5 TEST VEHICLE CROSS SECTIONAL ANALYSIS

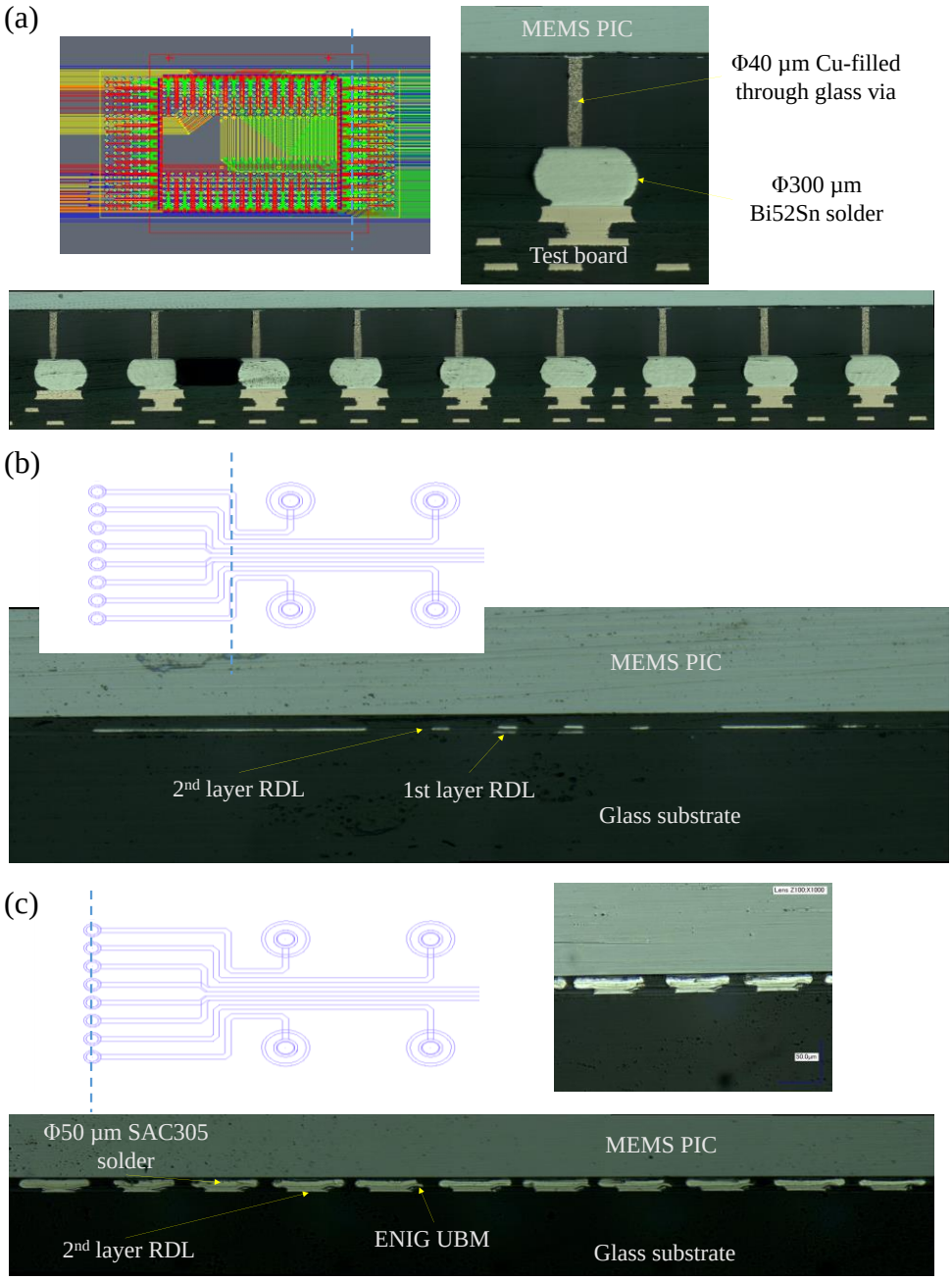


Fig. 3.27. Cross-sectional images of Test Vehicle 2b, highlighting assembly alignments at various sections (a) through via, (b) 2-layer RDL and (c) device bumps.

A sample assembly from Test Vehicle 2b was also mechanically polished to expose the various sections of electrical connections and is shown in Fig. 3.27. In Fig. 3.27 (a), it can be seen that Bi58Sn was properly reflowed and connected to the test board and at the same

time shows a good assembly alignment. Fig. 3.27 (b) further shows the two metallization layers on the glass interposer while Fig. 3.27 (c) shows the SAC305 solder bumps between MEMS switch device and glass interposer. Although the figure shows a rather flattened SAC305 bumps, shorts between neighbouring bumps did not occur, and this flattening can be rectified with a lower assembly force in the future.

3.4.6 OPTICAL PACKAGING AND SYSTEM SETUP

Once all the thermal processes related to electrical packaging were completed, the optical interposer could be finally coupled to the MEMS switch device and permanently supported by the mechanical mount. However, prior to that, the optical losses of the device had to be measured and this can be done through the optical shunts on the device. Fig. 3.28 compared the optical losses of the largest shunts (port 1-135) between the designed planar optical interposer and vertical SMF-28 probing. The planar coupling configuration recorded a higher optical loss of 1.17 dB per port, as expected (Chapter 1 has Lumerical simulation that compares optical losses between planar and vertical configurations and readers are recommended to refer to Fig. 1.6).

The difference in peak wavelength of approximately 14 nm on the other hand can be explained by the fact that the pitch angle (one of the 3 rotational axes) of the planar optical interposer wasn't perfectly parallel with the surface of the MEMS device during measurements. The peak wavelength can be shifted by tilting the optical interposer for approximately 0.5 ° (rule of thumb: 10 nm wavelength shift is equivalent to a change in 1 ° optical insertion angle). This change shall be incorporated into the final assembly using actual devices when they are available in the future.

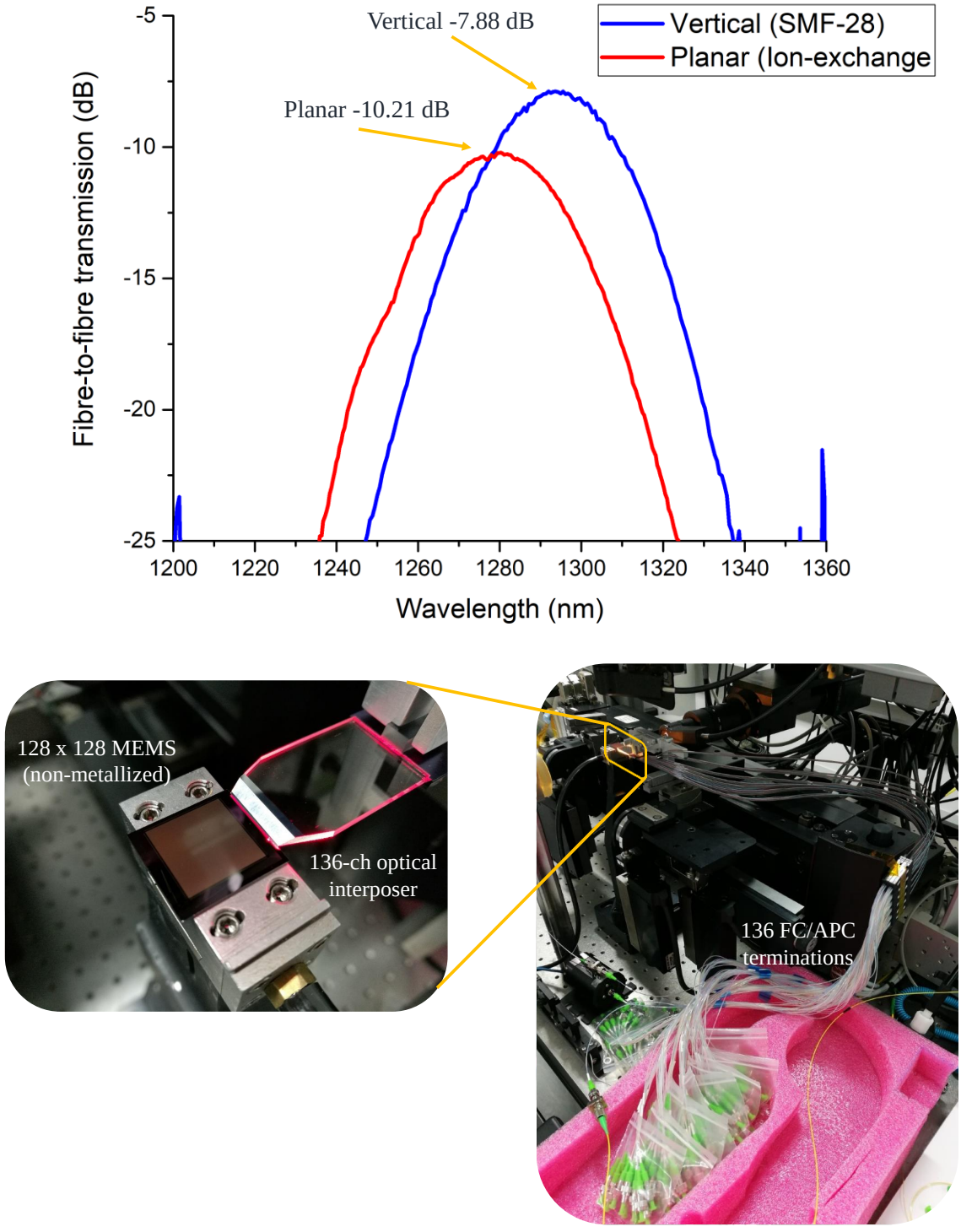


Fig. 3.28. Shunt transmission measurement of the MEMS switch device using the optical interposer.

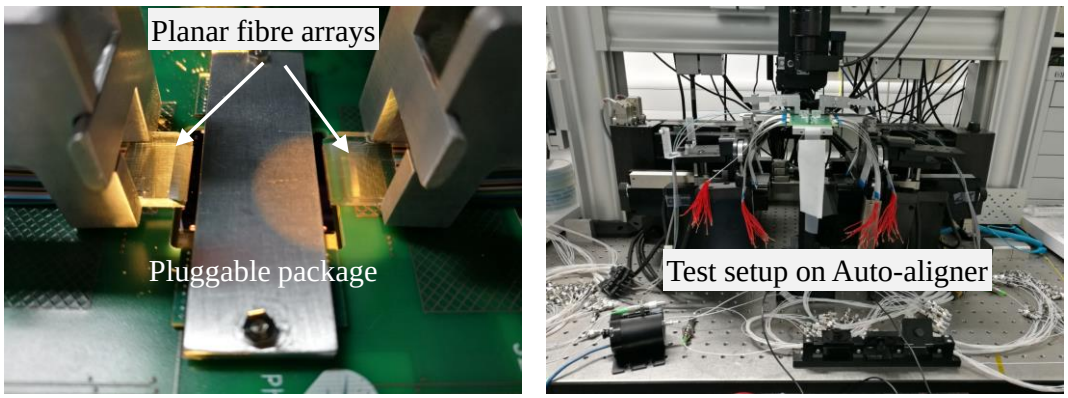


Fig. 3.29. Optical assembly test run on Auto-aligner using Test Vehicle 2a.

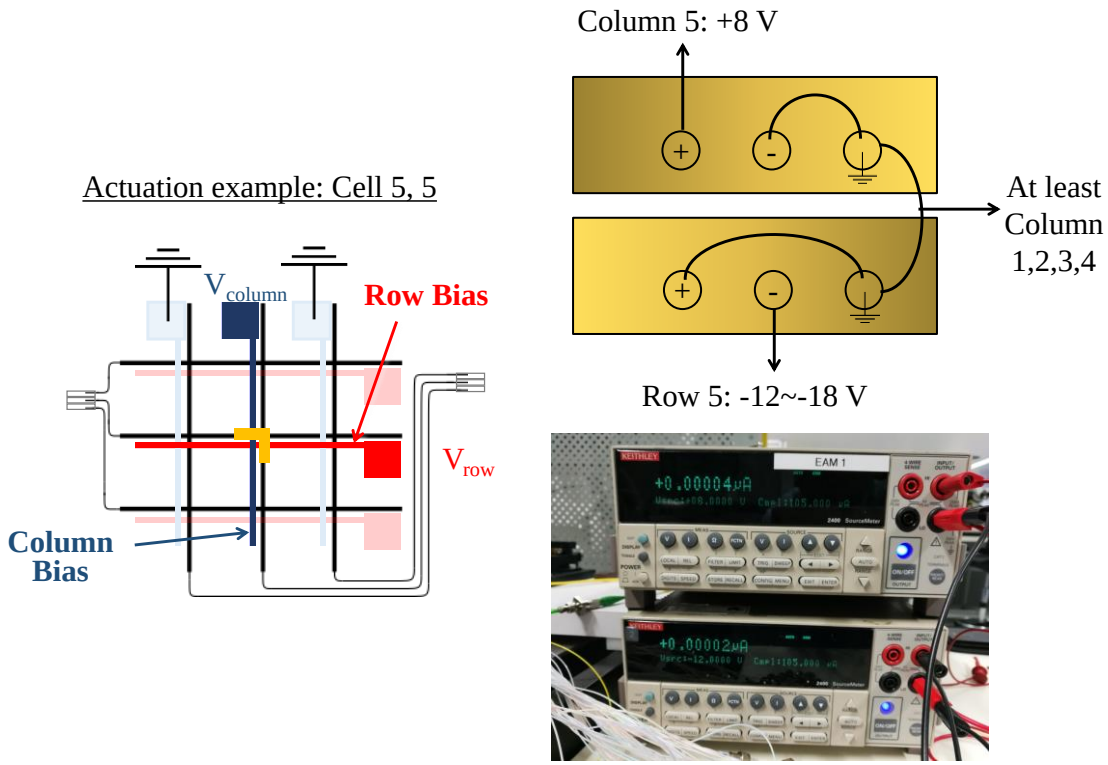


Fig. 3.30. MEMS switch actuation setup and configurations using Test Vehicle 2a.

Once the planar optical interposer performance was characterised, a full optical assembly was attempted using Newport Auto-aligner to confirm that the packaging designs worked as intended for both the test vehicles (Fig. 3.29) together with the actuation setup (Fig. 3.30). These test runs are necessary to rectify any other packaging design and process issues not visible during design stage while waiting for the final device to be available.

3.5 CHAPTER SUMMARY

In this chapter, two different state-of-the-art test vehicles demonstrating 2.5D advanced technology node had been designed, fabricated and assembled. Test vehicle 2a introduced a pluggable silicon photonic MEMS switch package that allows de-coupling of optical assembly processes (fibre attachment) from the device itself. The de-coupling concept will be further elaborated in Chapter 4. Test vehicle 2b on the other hand reduces the overall size of the MEMS switch package through the use of through glass via interposer from 14.35 mm x 46.7 mm to 14.35 mm x 21.95 mm. This effectively reduces the electrical length of the transmission lines that connect a device to the board, reducing line resistances. The through glass via interposer also introduces two-layer metallizations which isn't available on ceramic interposer, allowing higher integration density for future electronic-photonic devices. Glass interposer can also be integrated with optical waveguides in the future (more details in Chapter 5), and the concept had been briefly introduced in this chapter in the form of ion-exchanged optical interposer. Optical interposer allows the reduction of optical port pitches on the device down to 25 µm, unlike typical fibre v-grooves that have a minimum pitch of 127 µm. Although full switching demonstrations for both test vehicles could not be performed during the course of the thesis as final devices are not ready, continuity checks confirmed that the packaging designs work as intended and thus will be available for future demonstrations.

3.6 REFERENCES

[1] T. J. Seok, N. Quack, S. Han, R. S. Muller, and M. C. Wu, "Large-scale broadband digital silicon photonic switches with vertical adiabatic couplers," *Optica*, vol. 3, no. 1, pp. 64-70, 2016.

[2] T. J. Seok, N. Quack, S. Han, R. S. Muller, and M. C. Wu, "Highly Scalable Digital Silicon Photonic MEMS Switches," *Journal of Lightwave Technology*, vol. 34, no. 2, pp. 365-371, 2016.

[3] N. Quack, T. J. Seok, S. Han, R. S. Muller and M. C. Wu, "Scalable Row/Column Addressing of Silicon Photonic MEMS Switches," *IEEE Photonics Technology Letters*, Vol. 28, No. 5, p. 5610564, 2016.

[4] K. Kwon, T. J. Seok, J. Henriksson, J. Luo, L. Ochikubo, J. Jacobs, R. S. Muller and M. C. Wu, "128 x 128 Silicon Photonic MEMS Switch with Scalable Row/Column Addressing," *Conference on Lasers and Electro-Optics*, 2018.

[5] Email communications with Nasser Aghdam, *OZ Optics*, 16th March, 2016.

[6] Predel B. () Sn-W (Tin-Tungsten). In: Madelung O. (eds) Pu-Re – Zn-Zr. Landolt-Börnstein - Group IV Physical Chemistry (Numerical Data and Functional Relationships in Science and Technology), vol 5 J. Springer, Berlin, Heidelberg.

GRATING TO GRATING COUPLING

4.1 OVERVIEW OF CONCEPT

The previous two chapters have shown how conventional silicon photonic packaging, consisting of separate electrical and optical assembly processes are done. This process separation can be attributed to two reasons.

The first reason is due to the sensitivity of materials used for optical packaging such as index matching optical resin to temperature. Typical electrical packaging involving solder materials will have to be processed at a peak temperature of 260 °C, and last for at least 3-4 minutes. As most optical resin has a low glass transition temperature (T_g) and high coefficient of thermal expansion (CTE) due to its non-filler based nature, it will expand and contract more during thermal processing. At the same time, the optical resin may not maintain its optical transparency and refractive index post thermal processes and can become slightly opaque. Adhesion strength is also lower than polymer resins used in electronics packaging due to lower chemical dopings.

The second reason is that electrical packaging is a passive and high-throughput process in outsourced assembly and test (OSAT) foundries, often relying on visual recognition and self-alignment during processing, while optical packaging requires active alignment in order to maximize coupling power. Grating couplers have a narrow bandwidth (30-40 nm for uniform gratings at 1 dB loss) and are coupling angle dependent, thus the requirement of active alignment. The general rule of thumb is that each degree of change in the coupling angle will lead to a 10 nm wavelength shift in the coupling peak.

Now, with active alignment processing, the time required to fully assemble a silicon photonic package will be drastically increased. This in turn can lead to higher manufacturing

cost due to lower throughput. This chapter will explore gratings-based proximity coupling, which can be used to (1) remove active alignment processing, (2) allow heterogeneous 2.5D integration and (3) realise pluggable system-in-package for silicon photonics that can be used for Test Vehicle 2a from Chapter 3.

The pluggable optical/electrical concept is illustrated in Fig. 4.1 using U.C Berkeley's silicon photonic MEMS switch from Chapter 3 as an example. In that chapter, a pluggable test vehicle had been demonstrated through the use of contact interposer and alignment pins. However, the optical ports were still actively aligned and attached with fibres after electrical packaging processes were completed.

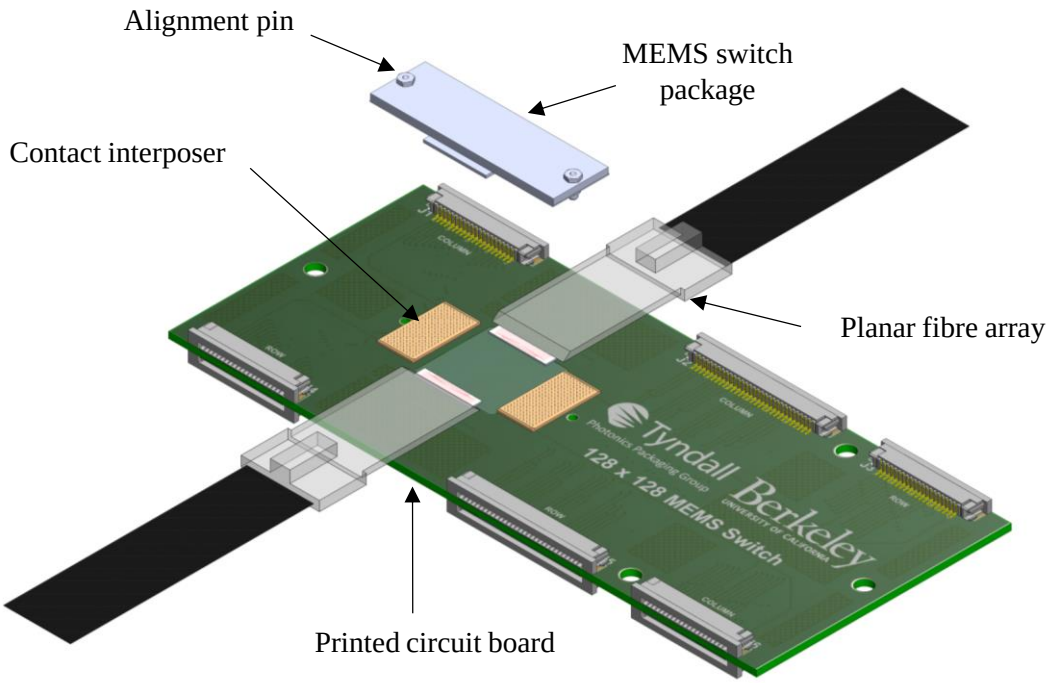


Fig. 4.1. Pluggable optical/electrical packaging concept, using reconfigured Test Vehicle 2a from Chapter 3 as example.

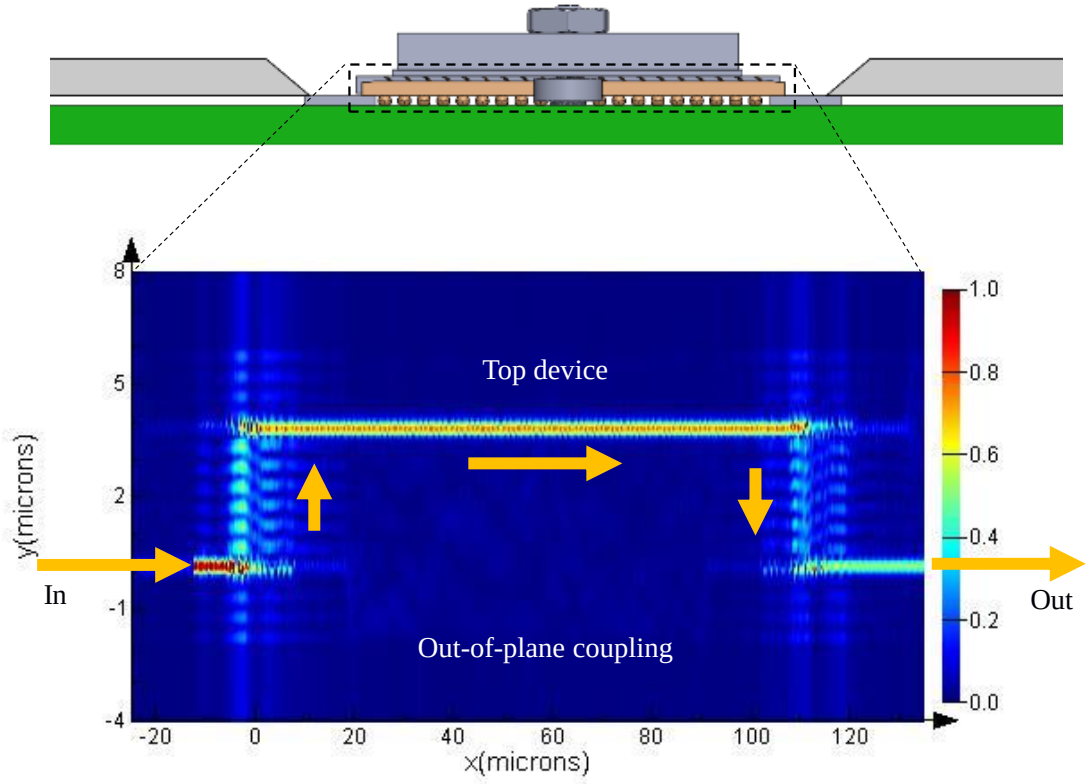


Fig. 4.2. A pair of vertically stacked gratings can interact, allowing broadband transmissions of optical power.

Fortunately, a pair of vertically stacked gratings interacts in a similar fashion as with a grating-to-fibre pair, but with broader bandwidth (Fig. 4.2) [1], [2]. This behaviour allows the development of a separate optical interposer and rerouting of optical waveguides becomes possible, similar to an electrical interposer. Cost savings can be realised through active device size reduction by eliminating unnecessary optical routings, considering the fact that active runs are 3.3x to 5.6x more expensive than passive runs in front end foundries [3], [4]. The higher coupling tolerances between the pair of gratings also allow a passive pluggable concept to be realised, transforming the silicon photonic package to “purely electrical.” For more advanced applications, an optical/electrical interposer can be developed by integrating optical gratings together with electrical transmission lines.

4.2 FDTD SIMULATION

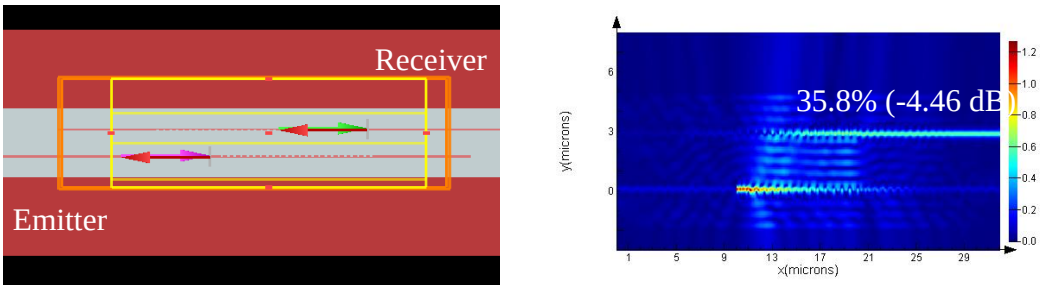


Fig. 4.3. 2D-FDTD simulation showing interaction between two vertically stacked uniform gratings at zero gap.

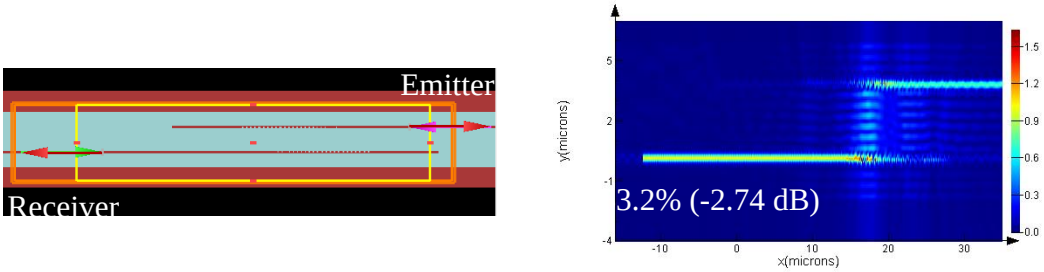


Fig. 4.4. 2D-FDTD simulation showing interaction between two vertically stacked non-uniform gratings at zero gap.

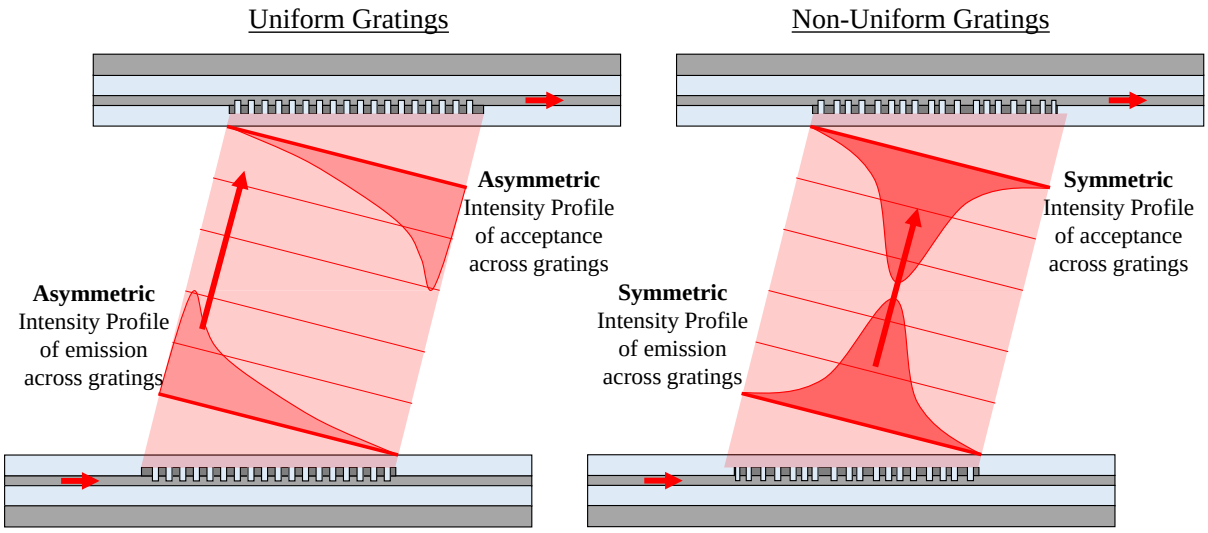


Fig. 4.5. Difference of mode profile between uniform and non-uniform gratings affecting coupling between them.

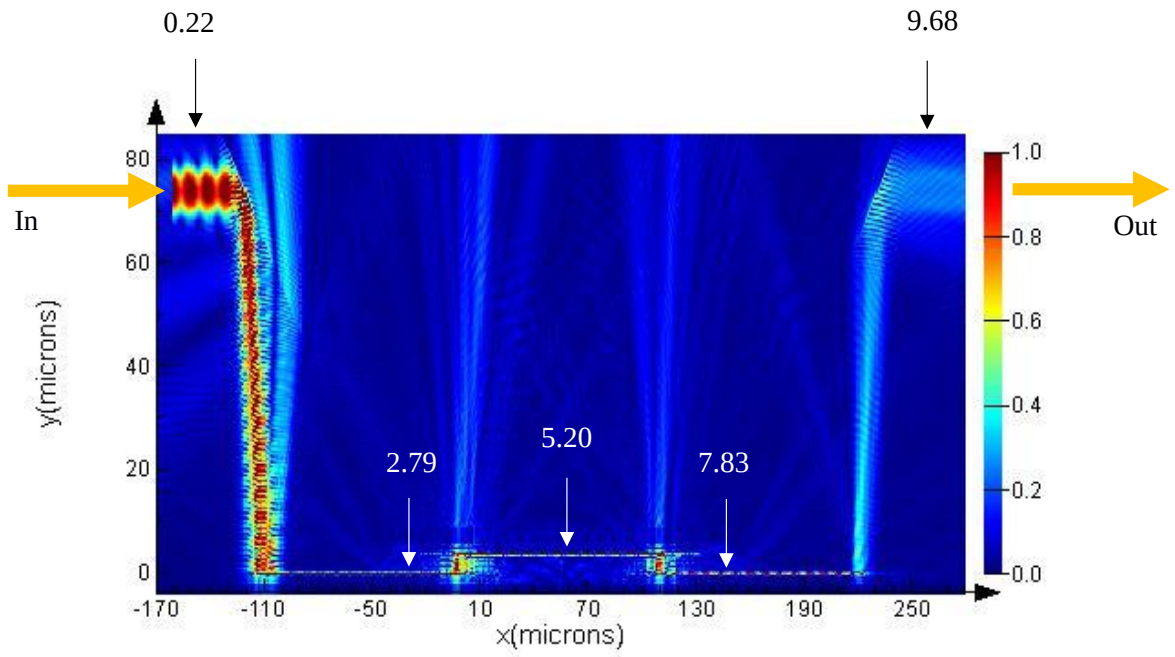


Fig. 4.6. FDTD simulation result showing the cumulative transmission losses (in dB) across various segments for grating-to-grating coupling, beginning and terminating with planar fibres.

Interactions between two vertically stacked pair of gratings couplers were first studied using 2D-FDTD on uniform [5] and non-uniform [6] grating-pair designs, and the results are shown in Figs. 4.3 and 4.4 respectively. From the simulations, it can be seen that a pair of stacked uniform and non-uniform gratings have transmission losses of - 4.46 dB and – 2.74 dB respectively. These values were based on the optimized position at zero gap. The simulation exercise, while confirming that any type of grating-pair design can interact between themselves, also showed that a difference in mode profile between uniform and non-uniform designs affects the transmission (Fig. 4.5). Uniform grating-pair showed a lower coupling efficiency due to its asymmetric intensity profile whereas non-uniform grating-pair has a symmetrical form for better mode overlap. Kuno *et al* [7] came to the same conclusion while designing inter-layer grating-pair as well. The FDTD simulation of the overall pluggable configuration (Fig. 4.6) shows the cumulative transmission losses across various

segments using non-uniform grating. The simulation began and ended with planar fibre assemblies.

Table 4.1. Insertion losses (from FDTD simulations) of uniform grating system between vertical fibre, planar fibre and grating-to-grating (G2G) couplings. Units in dB.

Distance	**Vertical fibre**	**Planar fibre**	**G2G**
Zero gap	- 2.98	N.A	- 4.46
10 µm	- 2.96	N.A	- 4.53
62.5 µm	- 3.66	- 4.52	- 5.62

Table 4.2. Insertion losses (from FDTD simulations) of non-uniform grating system between vertical fibre, planar fibre and grating-to-grating (G2G) couplings. Units in dB.

Distance	**Vertical fibre**	**Planar fibre**	**G2G**
Zero gap	- 1.3	N.A	- 2.74
10 µm	- 1.33	N.A	- 2.64
62.5 µm	- 2.55	- 2.5	- 2.9

For real applications however, the gap between a pair of gratings cannot be at zero due to metallization thickness or solder bumps. Additional simulations were performed at different gap distances (in air), and also compared against vertical and planar fibre couplings (with optical resin). The results are tabulated in Tables 4.1 and 4.2 for uniform and non-uniform grating-pair respectively. First of all, as the vertical separation between the gratings increases, (1) insertion losses increase for both designs and (2) larger increase in losses for

uniform gratings can be seen. Secondly, grating-to-grating coupling has higher transmission losses compare to vertical and planar fibre couplings, but the difference becomes smaller as the gap increases, particularly for non-uniform gratings. It should be highlighted that most foundry optical couplers are optimised with fibre coupling in mind.

Table 4.3. Effect of optical epoxy on grating-to-grating couplings. Units in dB.

Distance	**Uniform gratings**		**Non-uniform gratings**	
	Air	**Epoxy**	**Air**	**Epoxy**
Zero gap	- 4.46	N.A	- 2.74	N.A
10 µm	- 4.53	- 5.5	- 2.64	- 1.95
62.5 µm	- 5.62	- 6.84	- 2.9	- 2.72

Table 4.3 further shows the effect of optical resin between a pair of vertically stacked gratings at various gaps, as under-fill is typically used on flip chip packages to improve solder joint reliability. The effect on uniform and non-uniform gratings are drastically different, as the addition of optical resin (assumption: refractive index 1.45) increases the transmission loss for uniform gratings but reduces the loss for non-uniform gratings, bringing the latter closer to the values seen on fibre coupling.

4.3 MATERIALS AND METHOD

In order to experimentally demonstrate grating-to-grating coupling, test structures with non-uniform gratings were sourced from a project collaborator. These test structures were different from the designs used in simulation exercises in the earlier section and cannot be disclosed due to knowhow limitation. Fibre-to-fibre transmission of the gratings were first measured using vertical and planar coupling with optical resin between the fibre-grating interfaces. Vertical coupling and planar coupling gave insertion losses per facet of 1.73 dB and 2.59 dB respectively. Next, only one facet of the gratings was coupled with a planar fibre (50 ° polished) and optical resin, while leaving the opposite end open (Fig. 4.7). One of these samples was then flipped above the other, and the pair of opened grating facet was visually aligned using a flip-chip bonder (Fig. 4.7).

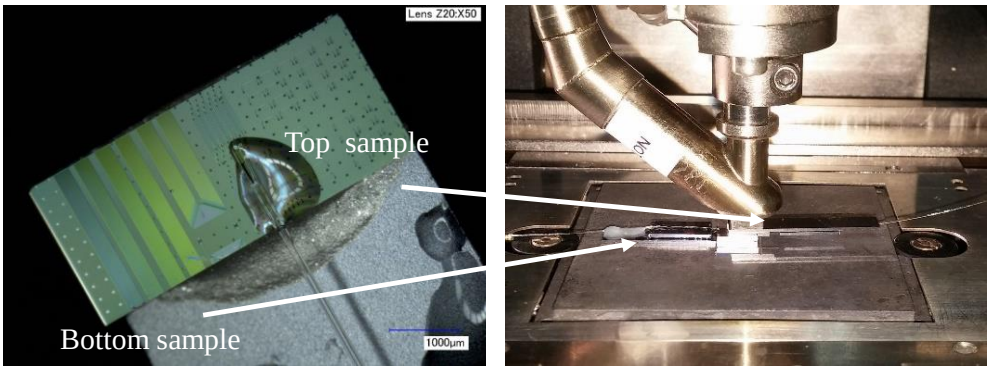


Fig. 4.7. Test samples with non-uniform gratings used in gratings-to-gratings coupling experiments. One sample was vertically stacked and aligned on top of another during flip chip assembly.

With this configuration, optical signal is now transmitting from a planar fibre through a grating facet from the top sample, then vertically from the top grating facet into the grating facet of the bottom sample, and finally exits through a planar fibre from the bottom (Fig. 4.8). Subsequently, tolerance scan in the z-, x- and y-directions were performed (Fig. 4.8). z-

direction corresponded to the vertical distance between the pair of grating facets and measurements were done in steps of 1 and 5 µm up to 35 µm. x-direction corresponded to "across" the grating axis and y-direction corresponded to "along" axis and measurements were done in steps of 0.5 µm up to ± 5 µm. No optical resin was used between the top and bottom gratings during measurements. All fibre-to-fibre spectra were then collected and analysed.

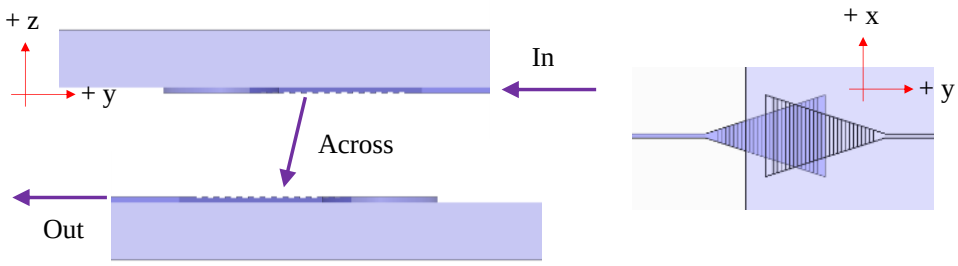


Fig. 4.8. Optical path through the assembly configuration and its corresponding axes.

4.4 RESULTS AND ANALYSIS

The individual coupling spectrums of top (grey line) and bottom (red line) and the coupling spectrum (pink line) of the assembly configuration at zero gap (z = 0) is shown in Fig. 4.10. The transmission spectrums of sample A and B were first aggregated (blue line), as only one grating facet is fibre-coupled on each sample. The spectrum between two grating facets (green line) was then obtained by subtracting the measured spectrum from the aggregated spectrum. Fig. 4.9 illustrates the various spectrums mentioned in Fig. 4.10.

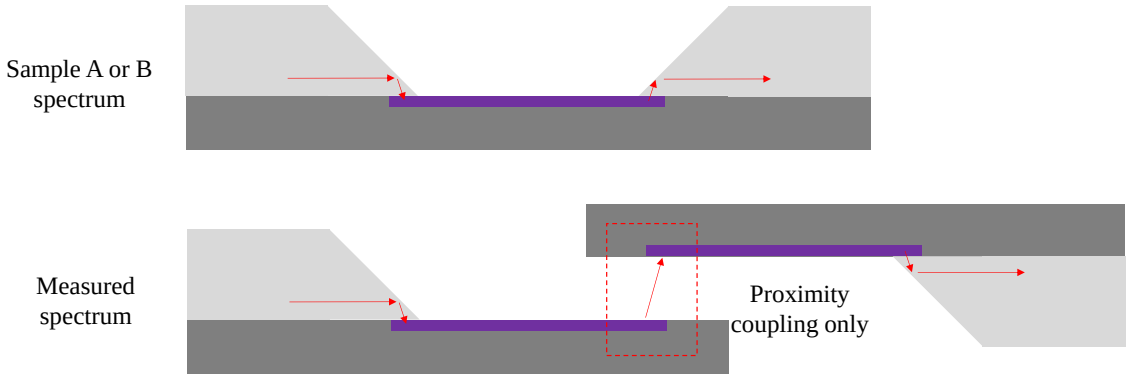


Fig. 4.9. Schematic depicting the various spectrums mentioned in Fig. 4.10.

The broad bandwidth shown by the coupling between two grating couplers (green line) could be attributed to the perfectly matched 1. angle of emission/incident, 2. phase and 3. mode from each grating tooth of the coupler pair. Reader can refer to schematic in Fig. 4.5. This hypothesis is now being studied by another Ph.D candidate within the group and future work will include integrating both optical (grating-to-grating) and electrical flip chip assembly based on this behavior. Ideally, sample A and B spectrums should coincide while measured spectrum should have the same peak wavelength in order to give a coupling spectrum that is relatively parallel to the horizontal axis. Yet, the spectrum is tilted, and this could be attributed to (1) the differences in insertion angles of the samples during individual fibre attachment, (2) co-planarity of sample A and B during experiment and (3) device

variations from fabrication. Nevertheless, experimental result had showed that the transmission between two grating facets is broadband (green line) compare to fibre-to-grating system's narrow band (grey or red lines). Using the peak wavelength of 1330 nm from the aggregated wavelength, the insertion loss of gratings-to-gratings coupling is found to be 3.63 dB and higher than 2.59 dB measured by planar fibre.

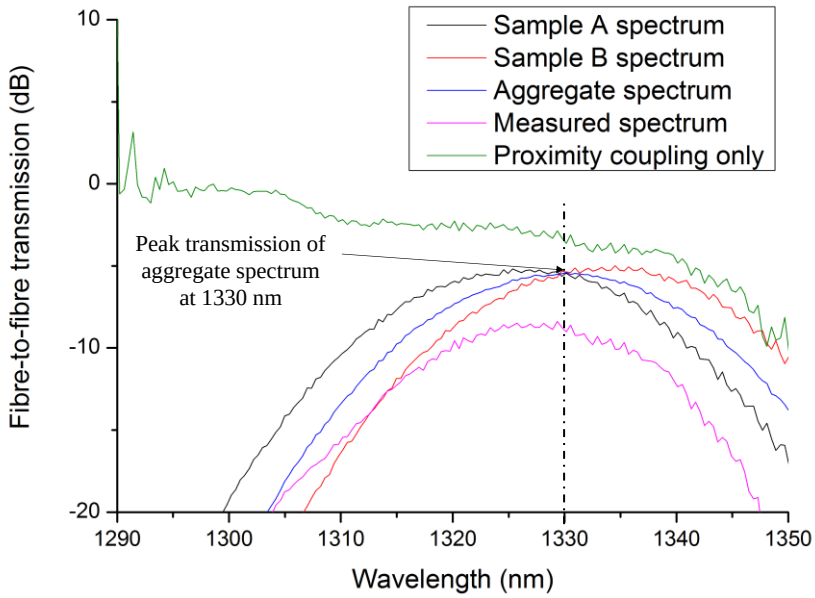


Fig. 4.10. Subtraction of aggregate spectrum (blue) from measured spectrum (pink) to obtain gratings-to-gratings coupling only spectrum (green).

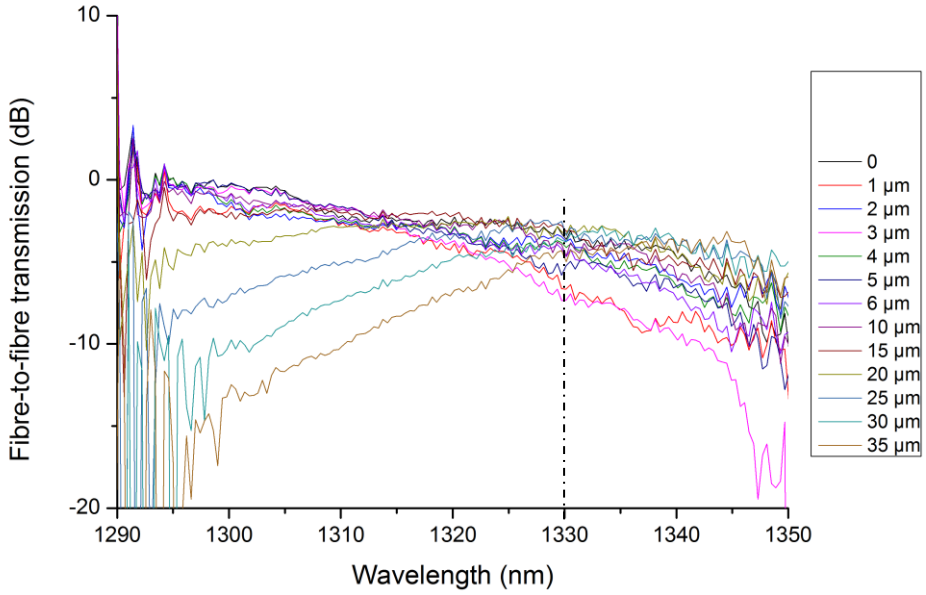


Fig. 4.11. Gratings-to-gratings coupling spectrums of various z-displacement from zero gap to 35 µm.

Fig. 4.11 shows the grating-to-grating coupling spectra of various vertical heights (z-direction) at optimized position. From the figure, it can be seen that while the bandwidth remained broad, the spectrums appeared to tilt counter-clockwise as the gap between the grating couplers were increased, achieving a relatively horizontal spectrum at 15 and 20 µm gap. This tilt was hypothesized to be due to the inability for the top grating die to maintain consistent co-planarity with the bottom grating die during the alignment arm stepping.

Using the peak wavelength of 1330 nm from the aggregated wavelength, the insertion losses were plotted in Fig. 4.12. Interestingly, an oscillation can be seen as the top grating facet is moved away from the bottom facet in the z-direction until they are spaced approximately 10 µm. Grating-to-grating coupling had the lowest insertion loss of 3.15 dB at gap of 15 µm from the plot.

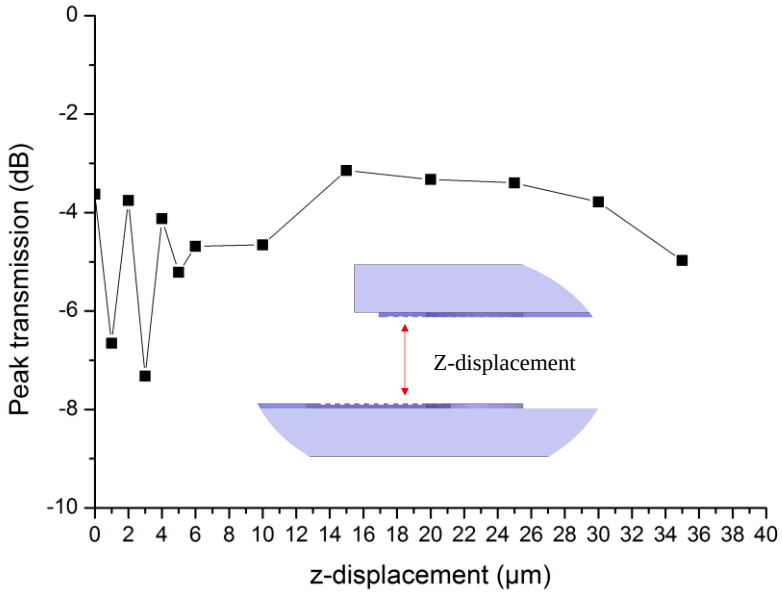


Fig. 4.12. Peak transmission variation with z-displacement. Oscillations can be seen between 0-10 μm displacements.

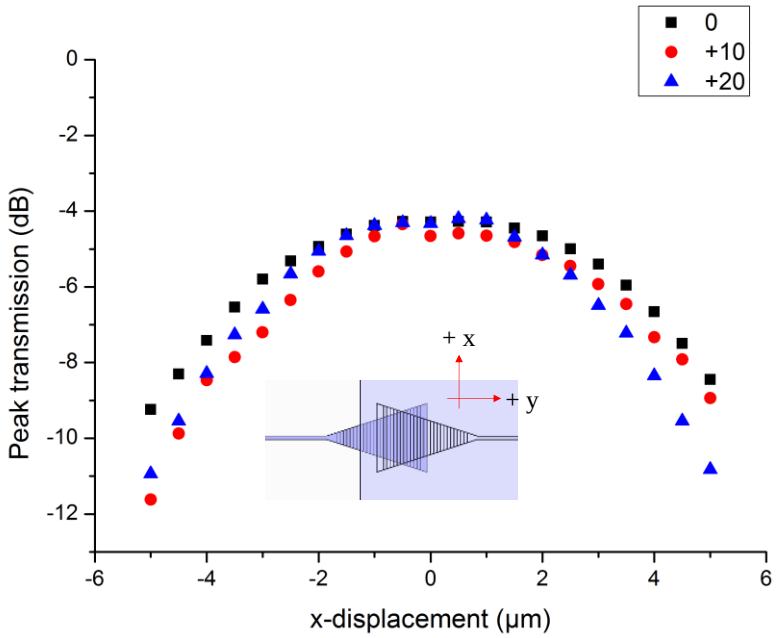


Fig. 4.13. Tolerance scan of coupling along the x-direction (across gratings) at various z-displacements.

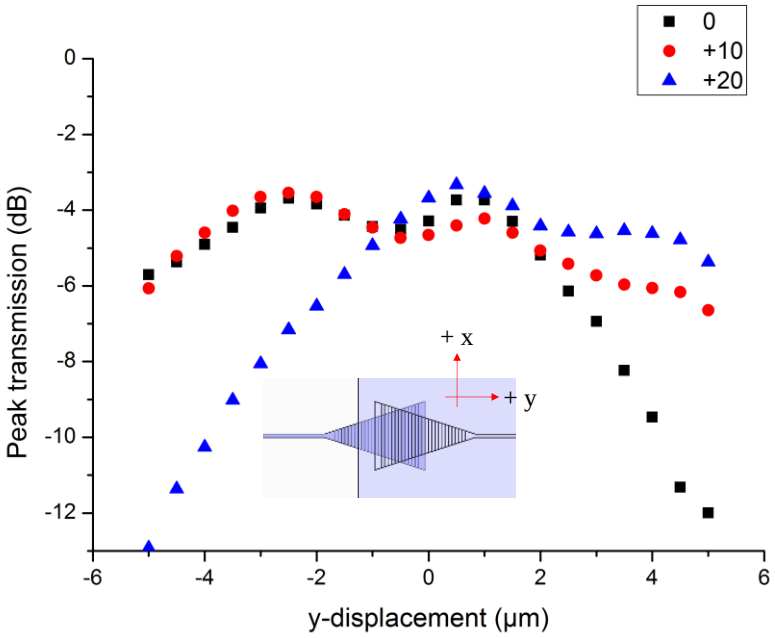


Fig. 4.14. Tolerance scan of coupling along the y-direction (along gratings) at various z-displacements.

Following a similar approach of using 1330 nm as the peak wavelength, tolerance scan in the x- (across gratings) and y-directions (along gratings) at z = 0, 10 µm and 20 µm were plotted and shown in Fig. 4.13 and 4.14 respectively. The coupling experiments showed a stable 6 µm alignment tolerance of 3 dB in the x-direction at all vertical heights while in the y-direction, it had a 10 µm tolerance of 3 dB at z = 0 and 10 µm. It reduced to 7 µm at z = 20 µm. Furthermore, in Fig. 4.14, it can be seen that there was modulation at z = 10 µm. Aside from Fabry-Perrot effect shown in Fig. 4.12, it was hypothesized that as the top grating die is moved in the y-direction, the 1. angle of emission/incident, 2. phase and 3. mode from each grating tooth were broken, leading to the oscillating trend observed.

4.5 IMPROVED GRATINGS DESIGN

Following the experimental results demonstrated, external interests on the pluggable configuration began to increase, leading to additional improvements together with fellow colleagues within the Photonic Packaging Group in Tyndall. The improved gratings used a larger mode field diameter of 13.6 µm, which is optimized for planar fibre coupling and meant for 1550 nm applications. Two of the improved gratings on 220 nm and 340 nm SOI platform were then simulated for grating-to-grating configuration as an initial indication of trend and differences with the results shown in Fig. 4.15. In the figure, F2G refers to fibre-to-gratings while G2G refers to grating-to-grating. It can be seen that fibre-to-grating transmission loss is lower for gratings designed on 340 nm SOI (-0.79 dB) versus on 220 nm SOI (-2.03 dB), as thicker silicon material provides stronger scattering strength from the teeth.

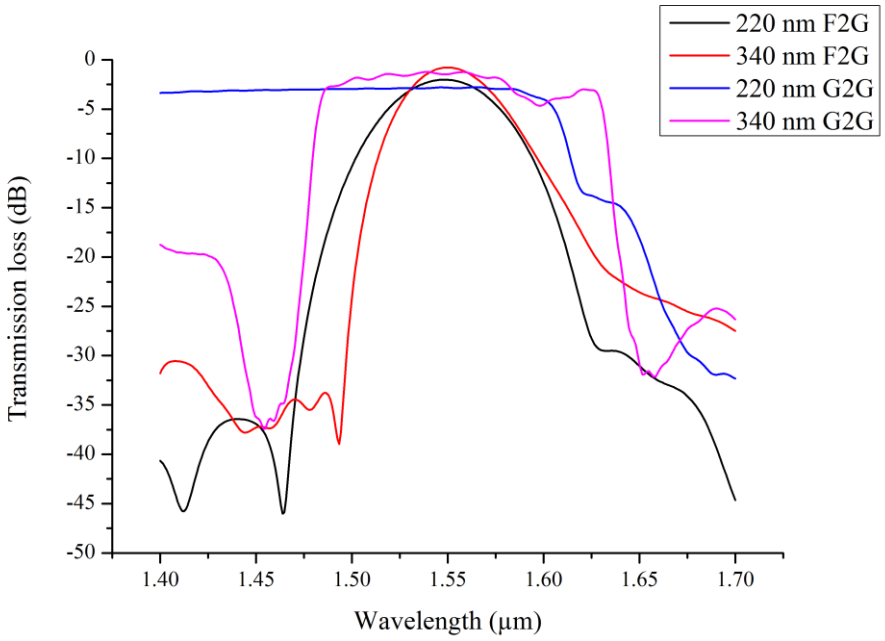


Fig. 4.15. Comparison of transmission losses between gratings designed on 220 nm and 340 nm SOI. F2G refers to fibre-to-gratings while G2G refers to gratings-to-gratings.

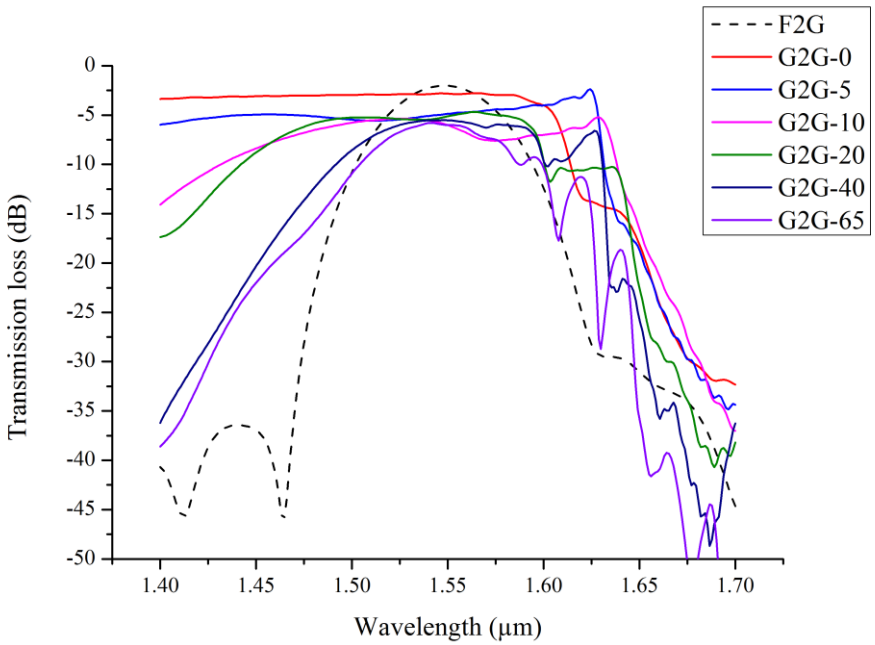


Fig. 4.16. Evolution of transmission losses and bandwidth as gap between the pair of vertically stacked gratings based on 220 nm SOI is increased.

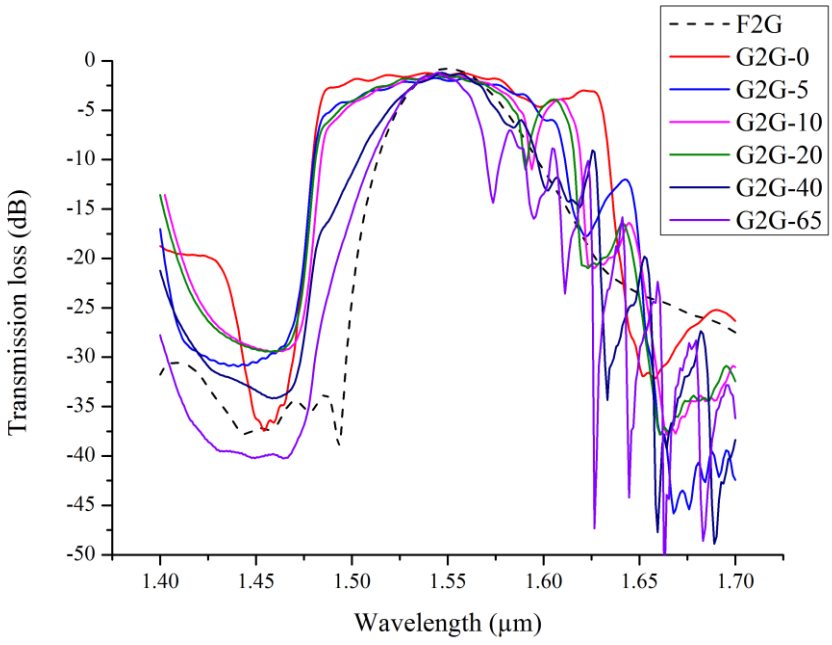


Fig. 4.17. Evolution of transmission losses and bandwidth as gap between the pair of vertically stacked gratings based on 340 nm SOI is increased.

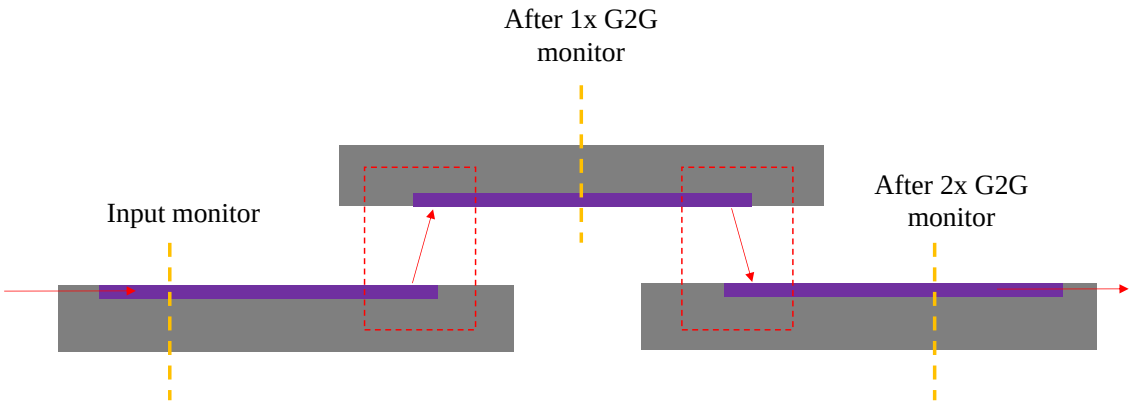


Fig. 4.18. Schematic illustrating the three spectrums found in both Figs. 4.19 and 4.20. The simulations were performed to observe the transmission losses, bandwidth and shape as a signal passed through the first grating-pair (input) and second grating-pair (output).

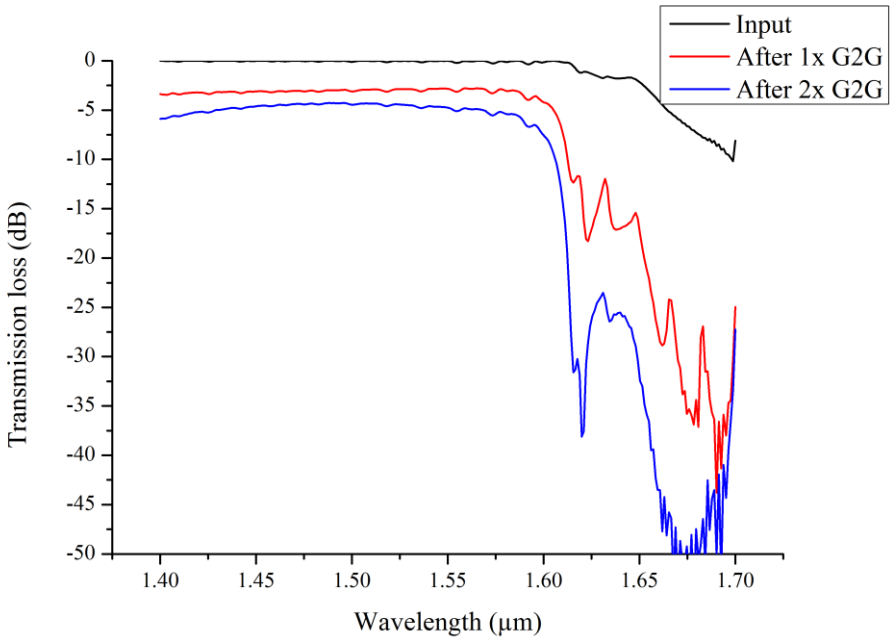


Fig. 4.19. Evolution of transmission losses and bandwidth after one and two pairs of vertically stacked gratings designed on 220 nm SOI.

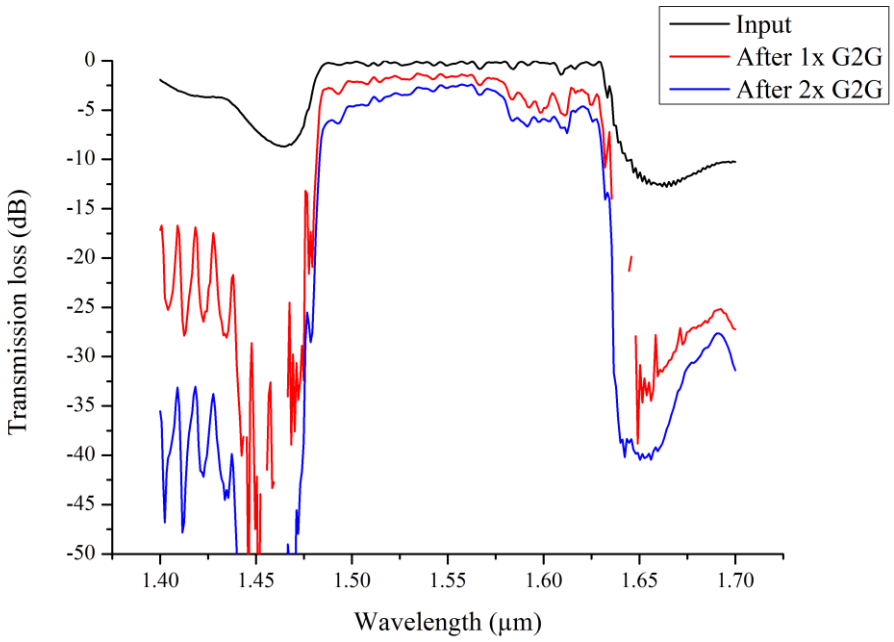


Fig. 4.20. Evolution of transmission losses and bandwidth after one and two pairs of vertically stacked gratings designed on 340 nm SOI.

Figs. 4.16 am 4.17 further shows the transmission loss and bandwidth evolution as the gap between two vertically stacked gratings is increased from 0 to 65 µm. In both simulation cases, an air gap between the pair of gratings was assumed. The shape of transmission curve can be seen to slowly approach that of fibre-to-grating transmission (Gaussian) as the vertical gap is increased. Both figures also show oscillations at longer wavelength, and as the periodicity of the oscillations was constant, they were likely to be a Fabry-Perrot effect. More works are currently being done by another Ph.D student to ascertain the hypothesis.

Lastly, Figs. 4.19 and 4.20 compare the transmission losses and bandwidth after one and two pairs of gratings design on 220 nm and 340 nm SOI. It can be seen that while transmission loss increases after each facet, the transmission bandwidth remained relatively broad and constant, showing the benefit of such system and the new gratings designed by the group. All the new designs are to be fabricated and demonstrated in the future.

4.6 CHAPTER SUMMARY

Gratings-based optical proximity coupling is attractive for pluggable assemblies due to its relatively wide coupling tolerances and bandwidth. While the concept in this chapter is devised form photonic MEMS switch device, it can be extended to other systems, particularly in the field of medical or chemical sensing, whereby a sensor device is typical disposable after a single use. Simulation has shown that coupling is independent of gratings design, as long as the pair are similar, and foundry has existing PDKs that users can tap into. Cost savings can be realised by optical routing area reduction on active device (3.3x to 5.6x more expensive than passive runs). New gratings designed together with fellow colleagues within the packaging group also showed that the transmission losses can be further minimized using thicker SOI platform.

4.7 REFERENCES

[1] J. Yao, X. Zheng, G. Li, I. Shubin, Y. Luo, H. Thacker, A. Mekis, T. Pinguet, S. Sahni, K. Raj, J. E. Cunningham and A. V. Krishnamoorthy, "Grating-coupler-based optical proximity coupling for scalable computing systems," *Proc. SPIE 7944, Optoelectronic Interconnects and Component Integration XI*, 794405, January 17, 2011.

[2] S. Bernabé, C. Kopp, M. Volpert, J. Harduin, J-M. Fédéli and H. Ribot, "Chip-to-chip optical interconnections between stacked self-aligned SOI photonic chips," *Opt. Express 20*, 7886–7894, 2012

[3] http://www.europractice-ic.com/docs/180517_MPW2018-general-v6.0.pdf

[4] http://www.aimphotonics.com/mpw/

[5] Grating coupler 2D-FDTD, Lumerical Knowledge Base, 2017

[6] X. Chen, C. Li, C. K. Y. Fung, S. M. G. Lo, H. K. Tsang, "Apodized Waveguide Grating Couplers for Efficient Coupling to Optical Fibers," *IEEE Photonics Technology Letter*, Vol. 22, No. 15, 2010.

[7] Y. Kuno, J. Kang, Y. Hayashi, J. Suzuki, T. Amemiya, N. Nishiyama, S. Arai, "Design of apodized hydrogenated amorphous silicon grating couplers with metal mirrors for inter-layer signal coupling: Toward three-dimensional optical interconnection," *Japanese Journal of Applied Physics* 54, 04DG04, 2015.

EVANESCENT COUPLING ON GLASS

5.1 OVERVIEW OF CONCEPT

Evanescent coupling involves transfer of energy from one waveguide to an adjacent waveguide due to physical overlap of the propagating waves. A familiar example would be the silicon photonic MEMS switch devices used in the high density packaging demonstrations (Chapter 2 and 3). During MEMS actuations, 94 % of energy transfer occurs when the coupler (cantilever) and bus (static) waveguides are in close proximity (80 nm gap) and this value drops to 3 % as the gap increases to 600 nm [1]. Evanescent coupling is thus attractive from the packaging perspective as energy transfer is based purely on the proximities between two adjacent waveguides, allowing passive optical coupling to be realised. Unlike fibre-to-grating coupling, evanescent coupling is broadband and polarisation independent as well. In this chapter, evanescent coupling on glass waveguides are investigated.

5.2 MODE (EME SOLVER) SIMULATION

Lumerical MODE (EME solver) was first used to establish the baseline trend and understand the coupling behaviours between silicon nano-tapers and buried glass waveguide. The advantage of EME (Eigen mode expansion) solver lies in its lower computational cost compare to FDTD (finite difference time domain), thus ideal for long distance propagations [2], [3].

Simulations were done covering three general perspectives – (1) materials, (2) design and (3) process. Materials simulation was done to understand the effects of glass (a) refractive index and (b) contrast, design simulation to understand the effects of (c) size and shape of glass waveguide and (d) tip width of silicon nano-taper and lastly process simulation to understand the effects of (e) buried depth, (f) gap between silicon nano-tapers and waveguides during assembly and (g) oxide thickness on top of silicon nano-tapers.

Table 5.1: Simulation variables to establish the baseline coupling trend

Materials	**Design**	**Process**
(a) Refractive index	(c) Waveguide size and shape	(e) Buried depth
(b) Index contrast	(d) Silicon nano-taper tip	(f) Gap during coupling
		(g) Top oxide thickness

The MODE-EME model consist of three cell groups with total length of 30 µm in the following sequence – 5 µm of buried glass waveguide only, 20 µm of silicon nano-taper and buried glass waveguide and 5 µm of silicon nano-waveguide. The second cell group was

meshed with 40 cells for an Eigen mode propagation length of 1 mm. TE propagation mode at the start (Port 1) and end (Port 2) of EME simulation region is selected, while monitors were placed at various locations to observe the electric field profiles. The transmission from Port 1 to Port 2 in MODE-EME was given by the absolute square of user S-matrix, |S21|^2.

The simulation model and electric field profiles at various taper widths are shown in Fig. 1. From Fig. 1b, it can be seen that TE- and TM-mode behaves differently, with TE-mode transferring more efficiently into the buried glass waveguide due to tapering effect of silicon nano-tapers. Fig. 1b further compares the TE-mode transfer of 1310 nm and 1550 nm wavelengths at various taper width and shows that the smaller the wavelength, the smaller taper width is needed.

The following assumptions were used throughout the simulation exercises. A reference 220 nm thick silicon nano-taper, with its width linearly increasing from 80 nm to 500 nm for a length of 1 mm, except for case (d) and zero top oxide, except for case (g). Zero buried depth for glass waveguide within the glass substrate, except for case (e). Zero gap between silicon nano-taper and glass waveguide, except for case (f). Glass refractive index and step index contrast of 1.45 and 0.5% respectively, except for cases (a) and (b). Square glass waveguide size of 5 µm x 5 µm, except case (c). Wavelength is assumed to be 1550 nm. The simulation variables and model are shown in Table 5.1 while Figs. 5.2 – 5.8 show the respective simulation results from cases (a) – (g).

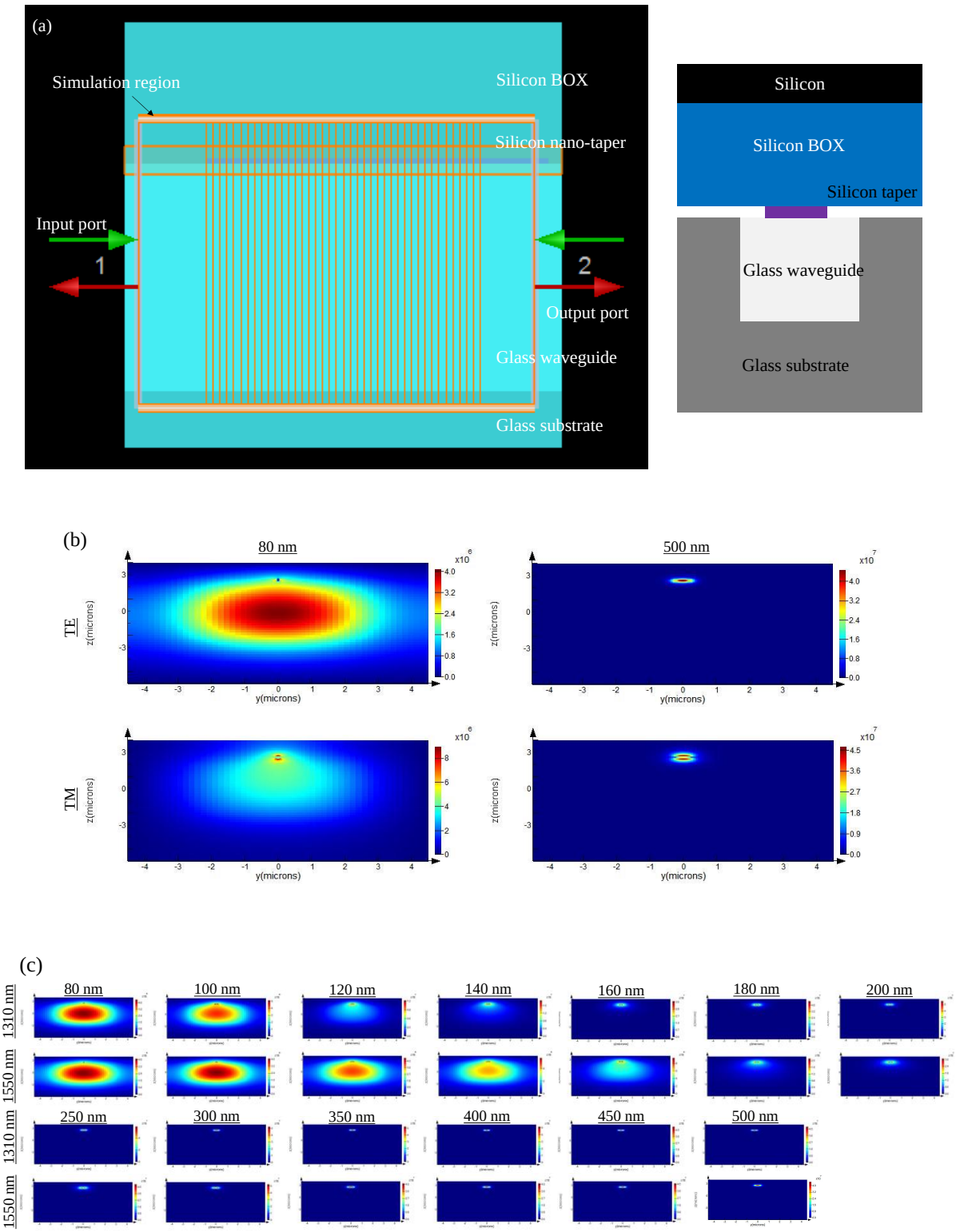


Fig. 5.1. (a) Simulation model, (b) TE-/TM-mode at start/end of taper and (c) TE-mode transfer at various taper width.

Fig. 5.2 shows the effect of glass materials (refractive indexes) on evanescent coupling with 0.5 % index contrast between glass waveguide and substrate. Based on simulation, the closer the substrate refractive index is to the oxide layer underneath the silicon nano-taper, the better the coupling efficiency. Coupling efficiency continues to decrease and reaches a plateau after refractive index of 1.5.

Fig. 5.3 on the other hand shows the effect of index contrast between glass waveguide and the substrate. It can be seen that coupling efficiency peaked at a contrast of 1.5 %, and has approximately 10 % higher coupling than a contrast of 0.5 %. It is worth highlighting at this point that single mode transmission cannot be maintained at an index contrast above 0.5 %.

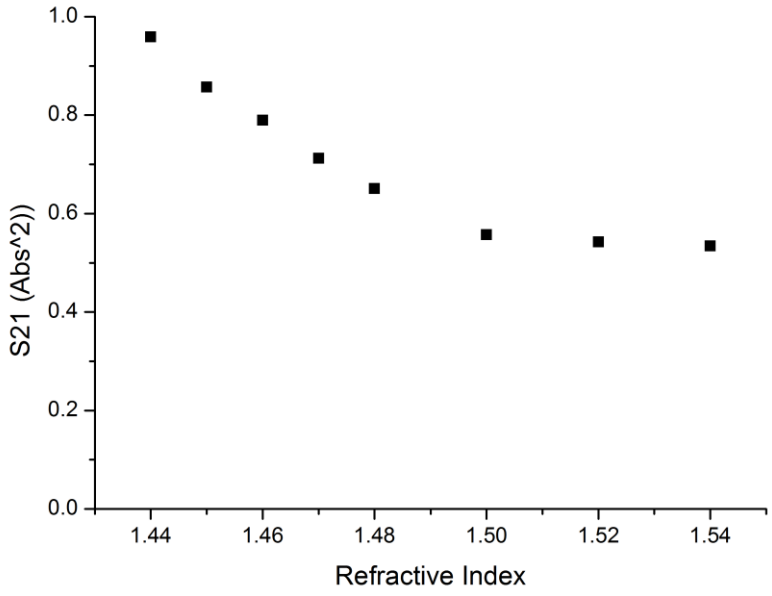


Fig. 5.2. Case (a), effect of glass refractive index. Higher the refractive index, the lower the coupling

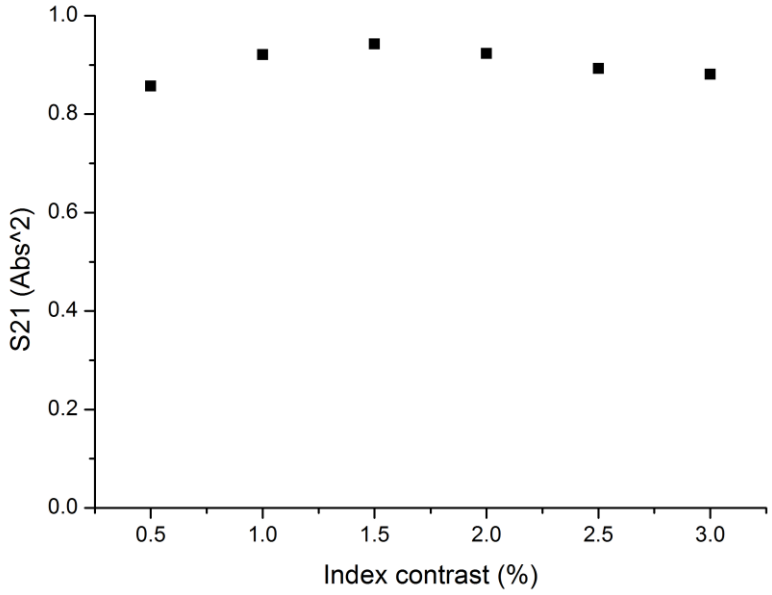


Fig. 5.3. Case (b), effect of index contrast. Index contrast should be low to maintain single mode transmission even though the coupling is weaker.

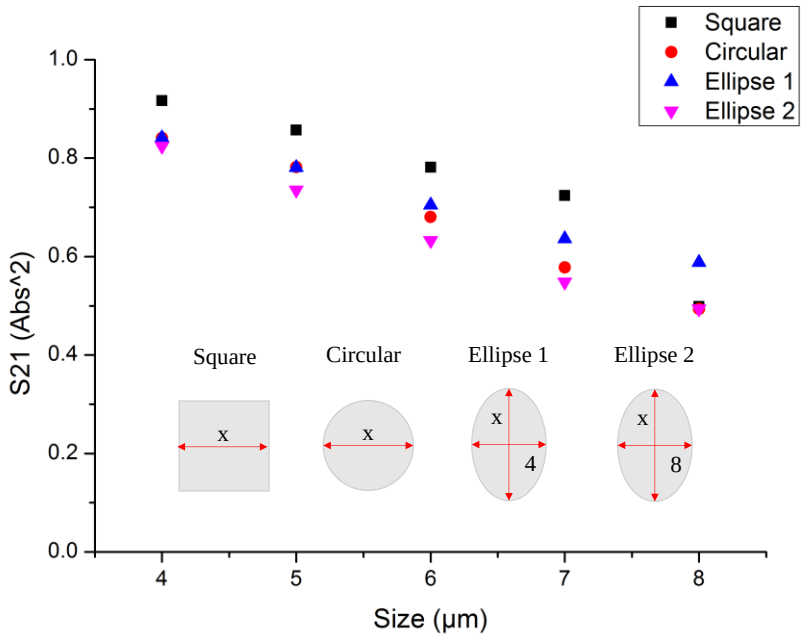


Fig. 5.4. Case (c), effect of glass waveguide size and shape. A square glass waveguide would improve coupling.

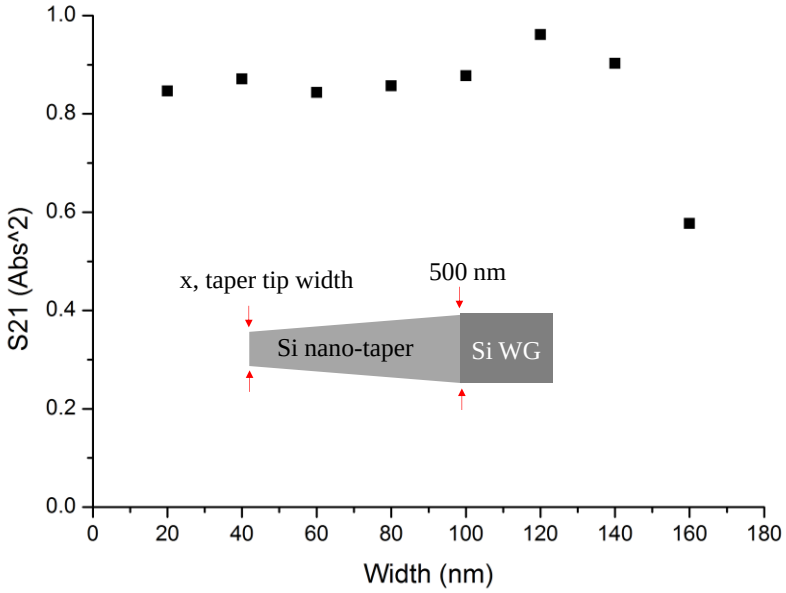


Fig. 5.5. Case (d), effect of silicon nano-taper tip. A clear coupling drop can be seen at taper width of 160 nm.

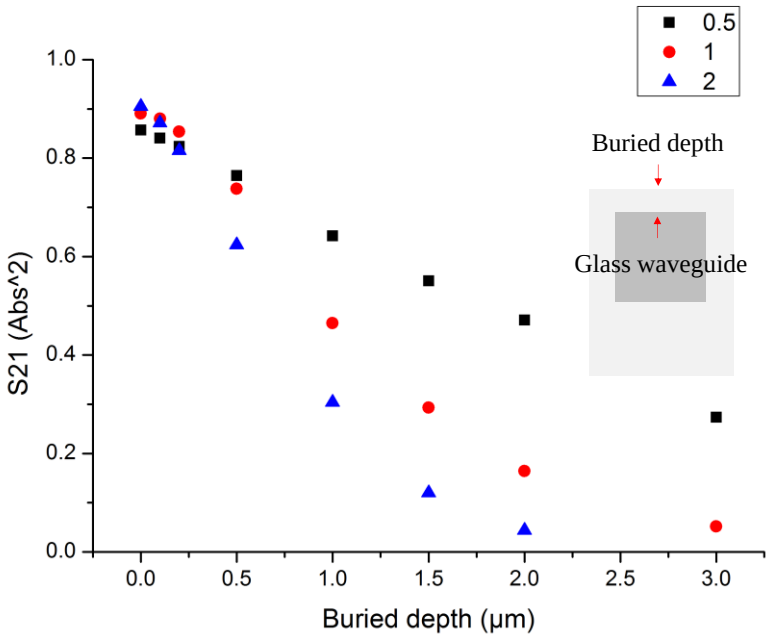


Fig. 5.6. Case (e), effect of buried depth of glass waveguide. Coupling falls drastically with increasing buried depth.

Fig. 5.4 shows the effect of glass waveguide's size and shape on evanescent coupling. The shape of the waveguide in this case should not be confused with the shape of mode profile propagating within it. From the simulation, it can be seen that a square glass waveguide allows better coupling into the silicon nano-taper, and it gets better with smaller sizes. Sizes smaller than 4 μm cannot be simulated as the mode profile cannot be properly confined within the glass waveguide in Lumerical MODE.

Fig. 5.5 shows the effect of the tip width on a linearly increasing silicon nano-taper. The silicon waveguide length is fixed at 1 mm while the taper width is gradually increased from "x" to 500 nm. In order to obtain the optimum taper tip width, x is varied in a step of 20 nm from 20 – 160nm. It can be seen that using a 5mm x 5mm glass core, the peak transmission efficiency remains stable above 80% with a peak at 120 nm taper tip width. Transmission efficiency drops substantially as the taper tip width is further increased to 160 nm. This could be attributed to the fact that in the system under consideration, this width is larger than the taper width region where the optimum energy transfer between the glass core and silicon waveguide occurs. Further in depth studies could be done by future Ph.D candidates to verify the hypothesis. This exercise shows that fabrication tolerance on a silicon PIC can affect the coupling efficiency and has to be properly accounted for during the design stage.

Fig. 5.6 shows the effect of glass waveguide's buried depth on evanescent coupling at various index contrast. The best coupling occurs when the glass waveguide is exposed on the substrate surface, and decreases as the buried depth increases. The decrease is more drastic with higher index contrast, as the mode profile is more tightly confined within the waveguide.

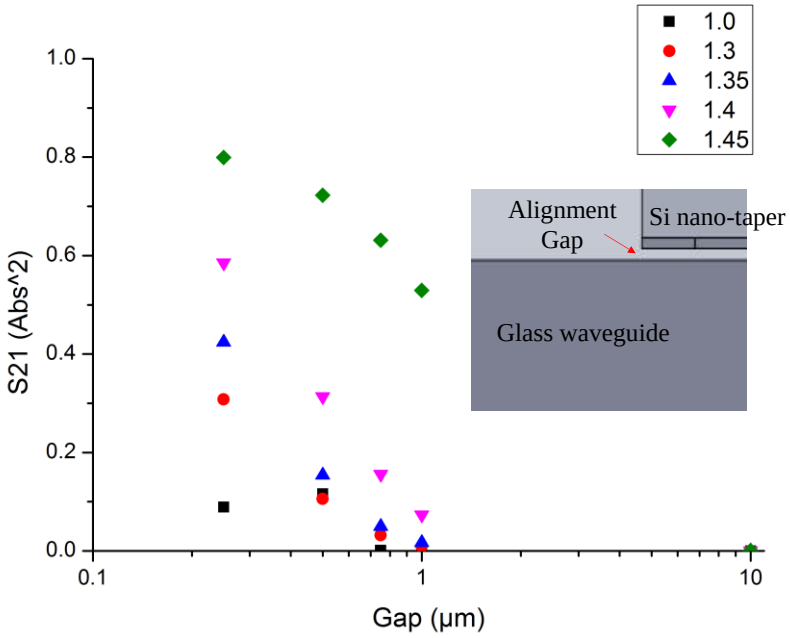


Fig. 5.7. Case (f), effect of assembly gap. Coupling falls drastically with increasing assembly gaps.

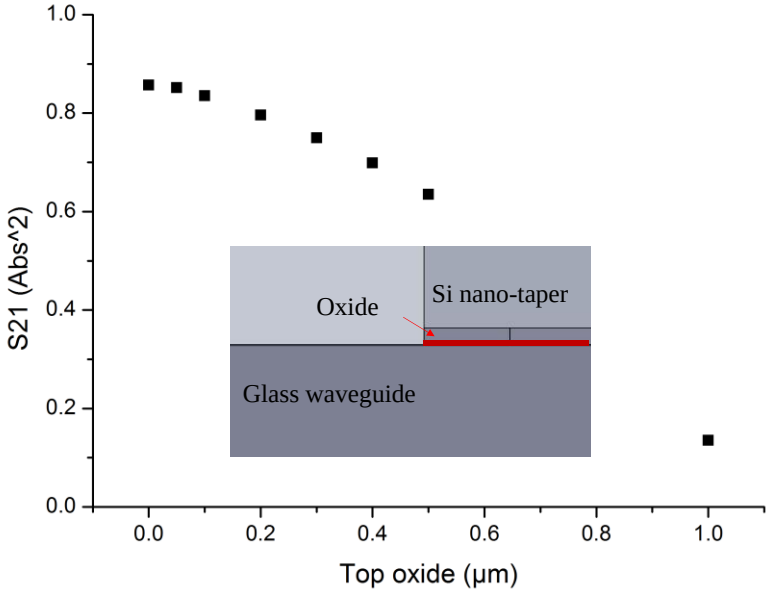


Fig. 5.8. Case (g), effect of oxide thickness on top of silicon nano-taper. Taper should be exposed and no TOX should cover it.

A similar decreasing trend can be seen during silicon PIC and glass substrate assembly, which is defined by the gap between the two (Fig. 5.7). An air gap as little as 0.25 μm would have drastically decreased the coupling efficiency from mid-80 % to below 10 %. It can however be recovered back close to 80 % if the gap is filled with optical resin that has a refractive index of 1.45.

Lastly, Fig. 5.8 shows the effect of oxide on top of the silicon nano-taper to coupling efficiency. The thicker the oxide is, the lower the coupling will occur. While native oxide that grows on exposed silicon is typically around 2 nm [4], silicon PIC fabrication usually involves high processing temperature and devices are topped with a thicker oxide as a protective layer, hence the need for this simulation exercise.

In a nutshell, the following can be inferred from the MODE-EME simulation exercises.

- The closer the substrate refractive index to the silicon BOX, the better the coupling.
- Smaller and square shape glass waveguide provide better coupling
- Glass waveguide has to be buried as close to the coupling surface as possible.
- Assembly gap between silicon PIC and glass substrate has to be minimised.
- Filling the assembly gap with the right optical resin will improve coupling.
- Silicon nano-taper's tip width has to be as small as possible.
- Existence of oxide layer on silicon nano-taper should be minimised.

5.3 MATERIALS AND METHODS

There are two common approaches in forming glass waveguides. The first approach is laser engraving, and the second approach is ion-exchange (first introduced in Chapter 3). The former relies on a focused laser to restructure the glass, creating a higher optical index path than its surrounding while the latter relies on chemical diffusion between the glass and the chemical bath. Laser engraving is much more versatile and has higher degrees of freedom, allowing three dimensional optical waveguides to be created within a glass substrate. Ion-exchange on the other hand is based on chemical diffusion on the surface of a glass substrate, before being diffused further into the substrate through an electrical field.

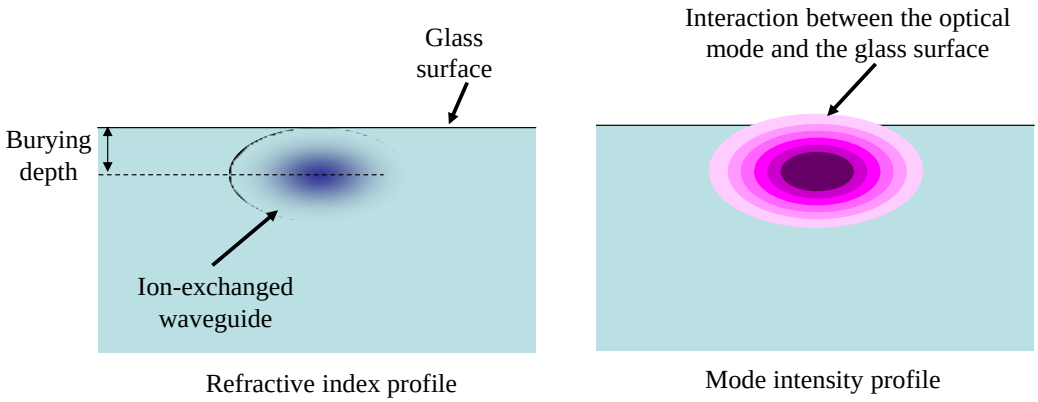


Fig. 5.9. Illustrations of the refractive index and mode intensity profiles of buried glass waveguides.

In order for evanescent coupling to occur between a silicon waveguide and a glass waveguide, both has to come into close contact, as predicted by Lumerical MODE-EME simulations earlier. As laser engraving is based on beam focusing, optical waveguides can only be formed beneath the glass surface, at least 30 μm away [5]. Additional polishing can be done to expose the buried waveguides, but this can cause unnecessary mechanical damages and higher cost. Considering various risks involved with laser engraving, it was thus

decided that ion-exchanged processing is a better approach to demonstrate evanescent coupling on glass.

The graded refractive index and mode intensity profile of ion-exchange waveguides is illustrated in Fig. 5.9 [6], while the glass waveguide fabrication flow is shown in Fig. 5.10. Field assisted burial is applied only towards the edge of singulated glass substrate to prevent signal leakages.

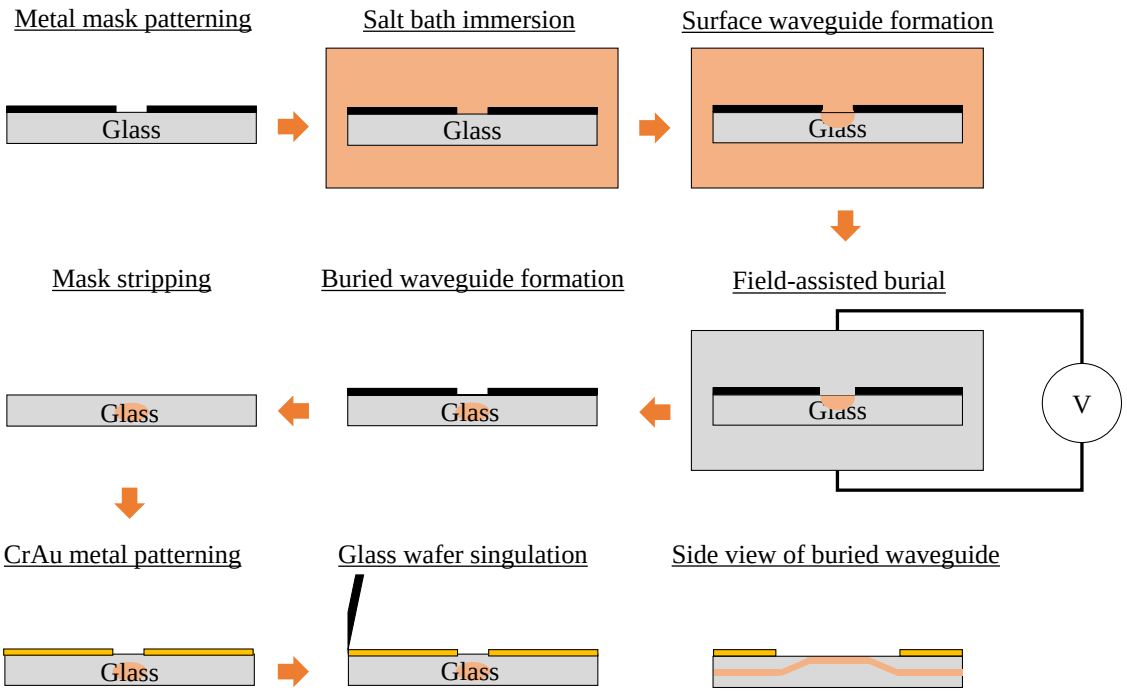


Fig. 5.10. Fabrication process flow of buried glass waveguide.

5.4 TEST VEHICLE DESIGN

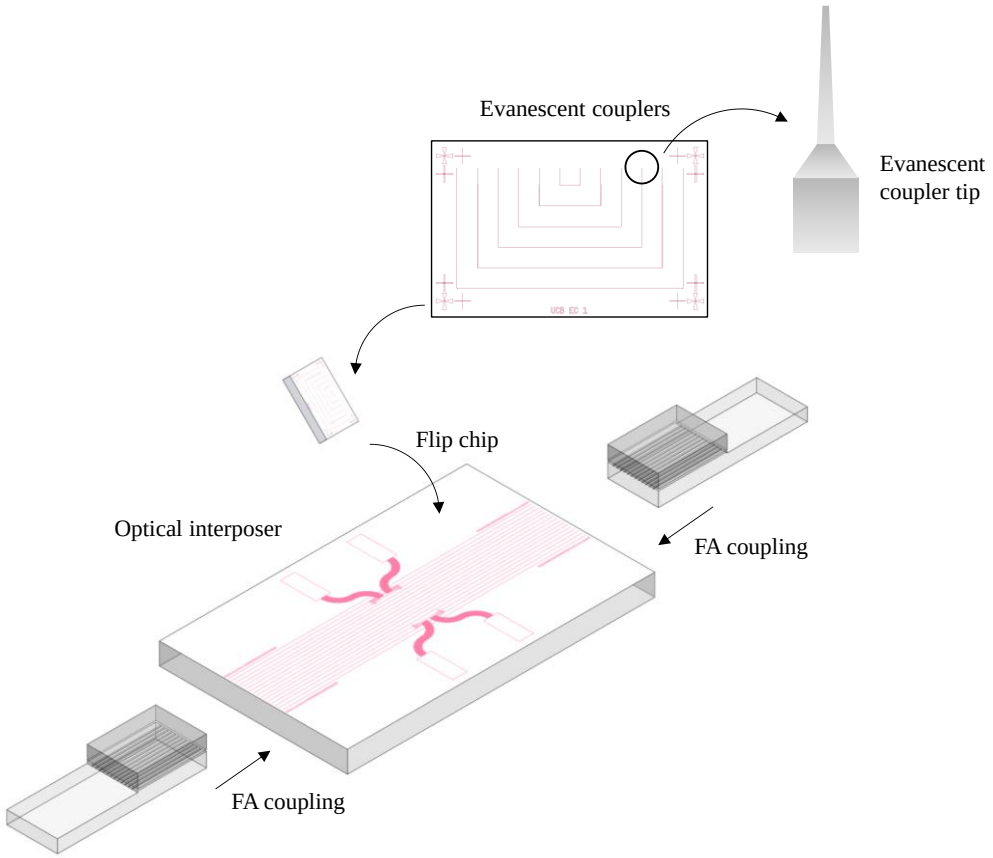


Fig. 5.11. Test vehicle design for evanescent coupling on buried glass waveguides.

In order to demonstrate the concept of evanescent coupling at package level, a test vehicle based on glass substrate is proposed (Fig. 5.11). It consist of an optical interposer, complete with straight ion-exchanged waveguides buried underneath the surface and a silicon component with U-shape silicon nano-tapers. Both the interposer and silicon component has thin Cr/Au metallization and alignment marks for flip chip bonding.

Simulation was also done using Lumerical MODE-EME to optimize the silicon nano-tapers based on the material properties of the glass substrate (n_{clad} = 1.5066) and ion-exchanged waveguide ($n_{core,\ graded}$ = 1.5466). Ion-exchanged waveguide is kept at 4 µm x 4 µm during the simulation, while silicon thickness at 220 nm. Silicon nano-tapers' tip width

are kept at 150 nm, following foundries' design rules using UV and e-beam lithography. Two initial silicon nano-taper designs are shown in Fig. 5.12 below. Design 1 has two-segment with coupling efficiency of 53.9% with a length of 200 µm while design 2 has three-segment with coupling efficiency of 61.4% with a length of 210 µm. Coupling efficiency will improve to over 90% with smaller taper tip width, but this will require access to better foundry. These designs (simulation and fabrication) were to be validated with experimental results and further improved on.

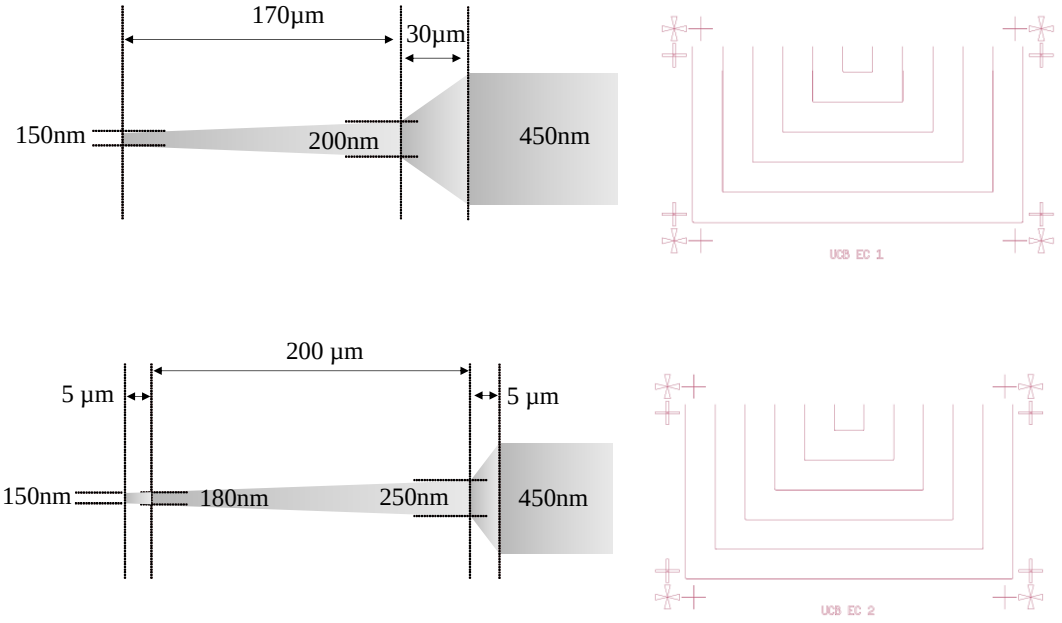


Fig. 5.12. Silicon nano-taper designed to match ion-exchange waveguide coupling on substrate.

5.5 RESULTS AND ANALYSIS

Fig. 5.13 shows the initial design of the glass interposer, consisting of six Cr/Au metallization pads for electrical continuity check and sixteen ion-exchanged waveguides. The waveguides were running just under the glass surface in the centre of the interposer, and then buried deeper as they travels toward the edges. Completed glass interposer was then probed using visible red laser. While the laser visibly travelled along the waveguides, it disappeared as it reached the section with Cr/Au metallization (Fig. 5.14). A sample was wet-etched to remove the Cr/Au metallization, and it was found that metal diffusion in the ion-exchanged waveguides could have occurred. It can be seen in Fig. 5.15 that ion-exchanged waveguides that ran underneath Cr/Au metallization had turned cloudy/opaque, while segments without Cr/Au maintained their optical transparencies.

Once it was determined that metallization interacted with glass waveguides, two of the metallization were removed (Fig. 5.16). Similar probing using visible red laser showed that the signal travelled smoothly across the glass interposer, and visibly recoupled back into an optical fibre (Fig. 5.17).

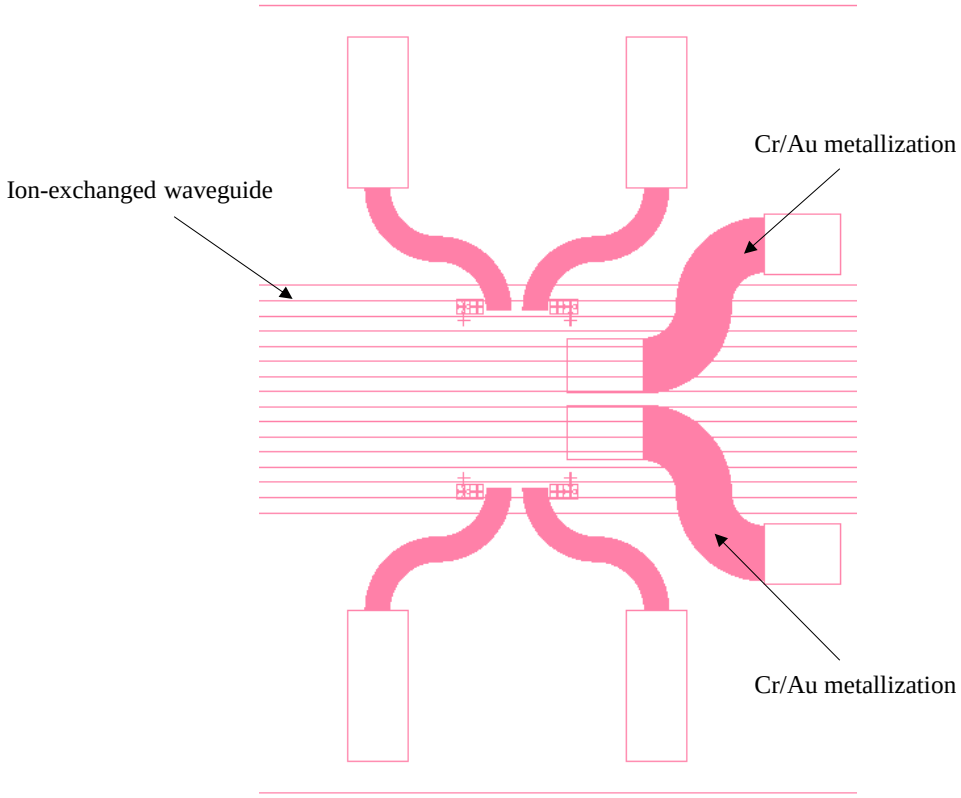


Fig. 5.13. Initial design of glass interposer with Cr/Au metallization on top of ion-exchanged waveguides.

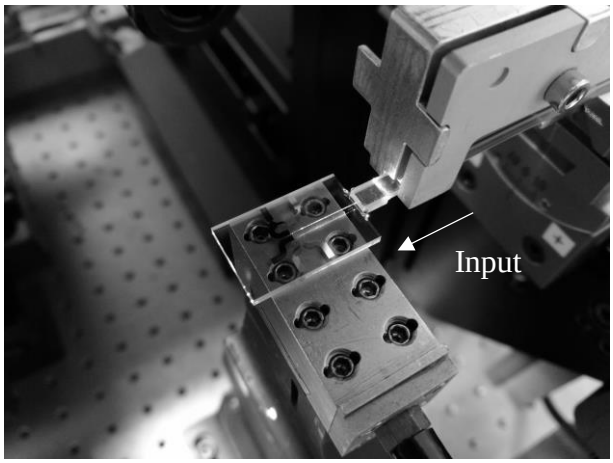


Fig. 5.14. Ion-exchanged waveguide probing using visible red laser. Image taken in monochrome shows that light passes through the waveguides but obstructed by Cr/Au metallization.

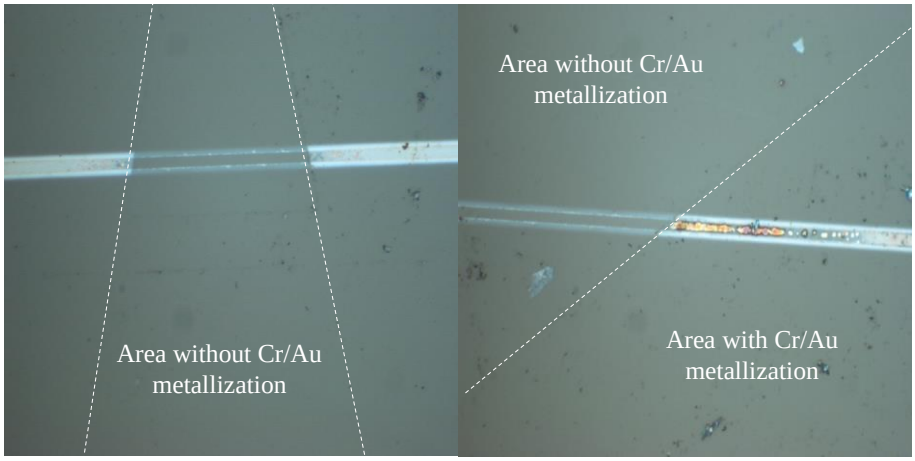


Fig. 5.15. Images of glass interposer post Cr/Au metallization wet etching, showing cloudy/opaque sections of ion-exchanged waveguide in areas covered by the metallization.

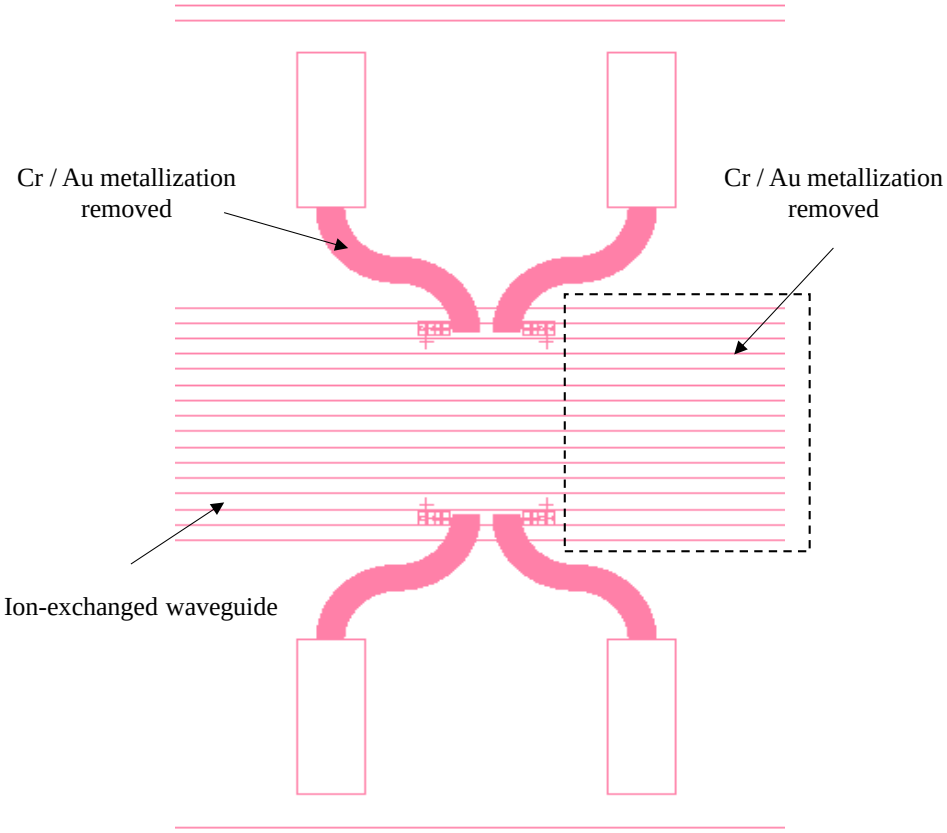


Fig. 5.16. Second design of glass interposer, whereby Cr/Au metallization above ion-exchanged waveguides have been removed.

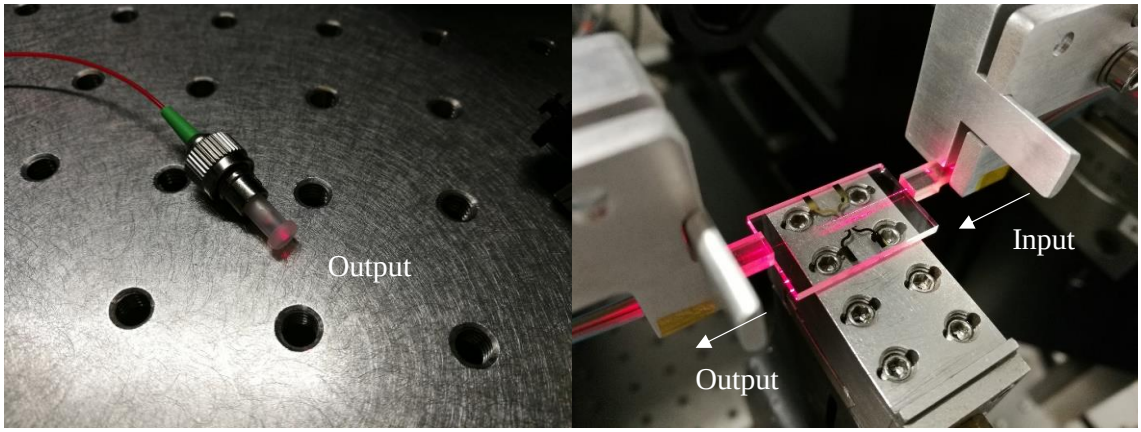


Fig. 5.17. Ion-exchanged waveguide probing using visible red laser. Image shows that light passes through the waveguides without obstruction.

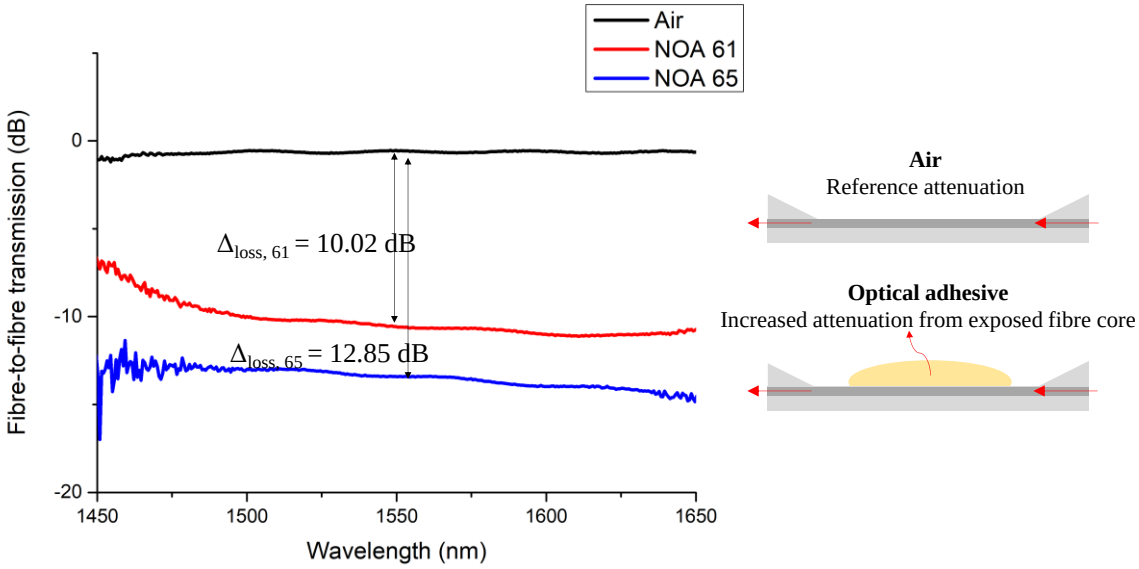


Fig. 5.18. Attenuation response of side-polished single mode fibre (SMF-28) with air (n = 1), optical resin NOA 61 (n = 1.56) and NOA 65 (n = 1.524).

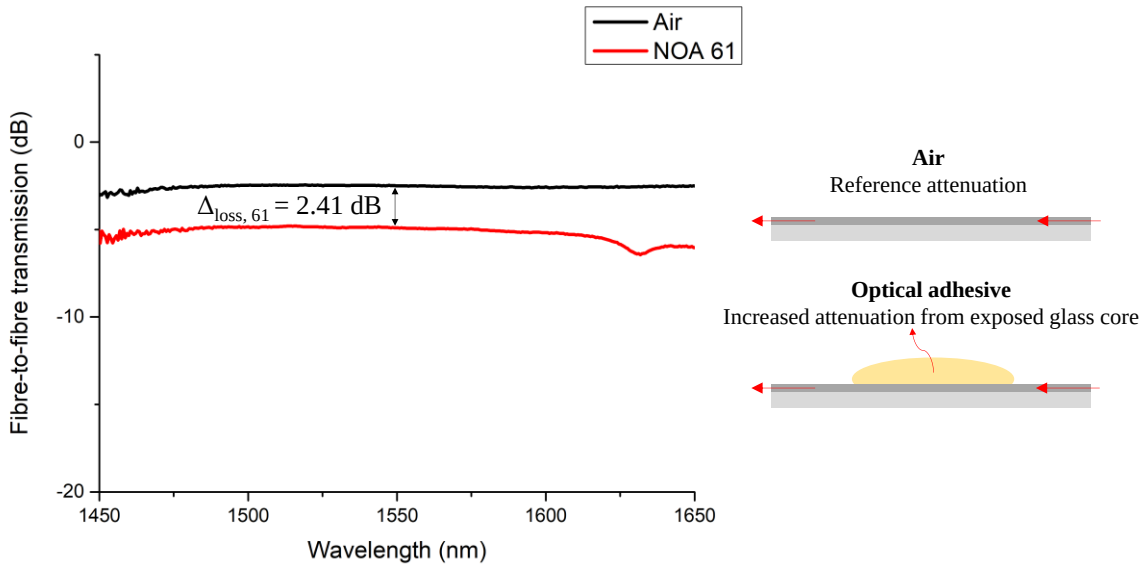


Fig. 5.19. Attenuation response of ion-exchanged glass waveguide with air (n = 1) and optical resin NOA 61 (n = 1.56).

Attenuation response of the glass waveguide with optical resin was then compared with a reference sample using side-polished SMF-28 fibre (Fig. 5.18). It can be seen that the attenuation effect of an exposed fibre core differs depending on the refractive index at the core boundary. Insertion loss of 0.57 dB in air (n = 1) increases to 10.59 dB when optical resin NOA 61 (n = 1.56) [7] was applied. The insertion loss further increases to 13.42 dB when optical resin NOA 65 (n = 1.524) [8] with lower refractive index was applied.

Subsequently, NOA 61 was applied on the ion-exchanged waveguide, and the attenuation response is shown in Fig. 5.19 for a single channel and Fig. 5.20 for all channels. Unlike the attenuation seen on reference sample (SMF-28 fibre), the effect of refractive index changes at the core boundary of ion-exchanged waveguide is less significant. Ion-exchanged waveguide shows an increase in transmission loss between 2.41 to 3.61 dB compare to 10.02 dB on side-polished SMF-28 fibre. This could be due to the fact that (1) the ion-exchanged

waveguide was buried much deeper than intended, or that (2) the graded index profile of the ion-exchanged waveguide was tightly confining the optical profile.

Nevertheless, an attenuation of 2.41 dB still corresponds to 42.6% of the input power escaping from the surface and thus could be used for the evanescent coupling test. Simply speaking, the input power for evanescent coupling will then be 0.426 mW instead of 1 mW and the coupling output through silicon nano-taper will be normalised against 0.426 mW.

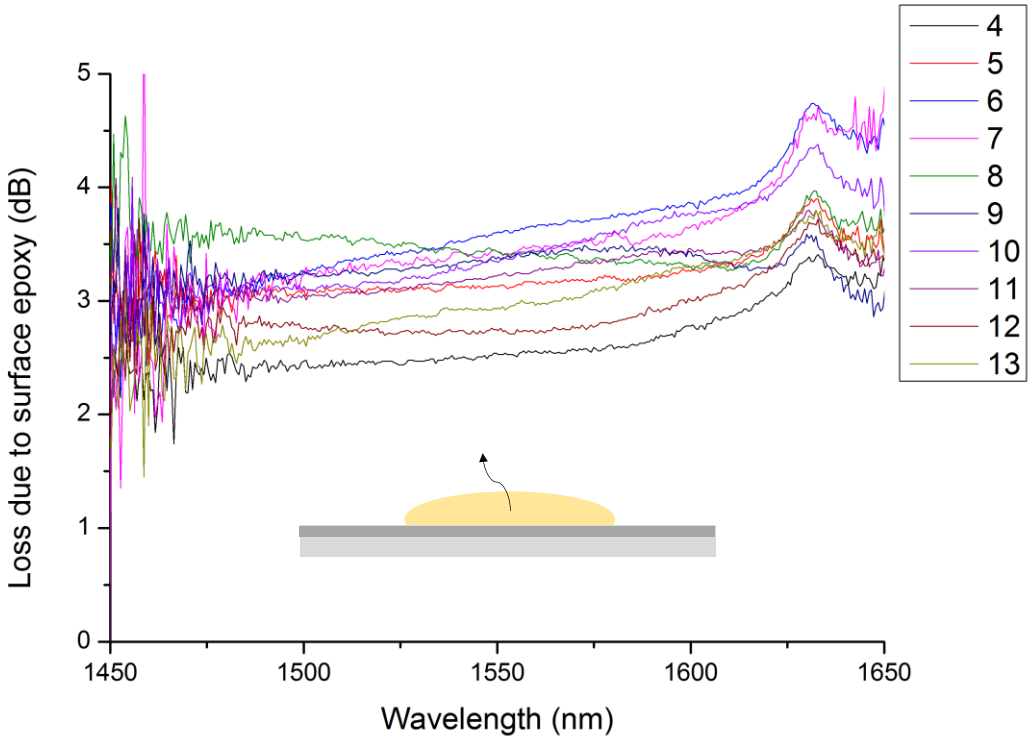


Fig. 5.20. Losses caused by optical resin NOA 61 (n = 1.56) on the surface of ion-exchanged glass waveguides. Graph depicts losses from buried channels 4 to 13.

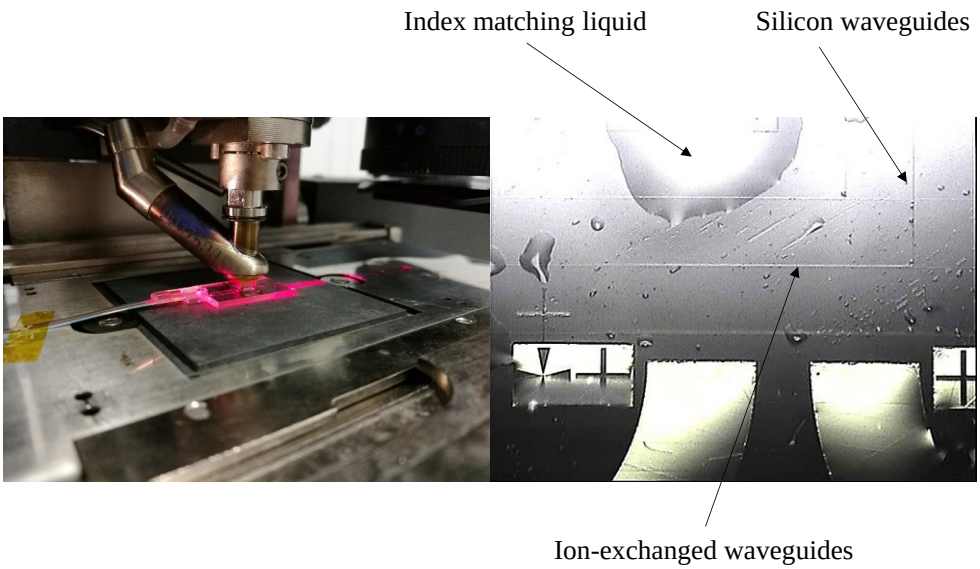


Fig. 5.21. First silicon device/glass substrate alignment and evanescent coupling test using Fineplacer Lambda.

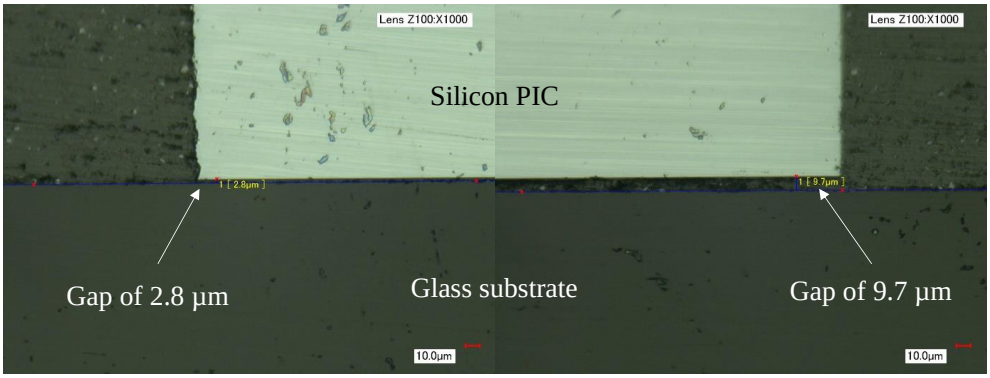


Fig. 5.22. Cross-section of the assembly shows that a gap ranging from 2.8 µm to 9.7 µm exists between silicon PIC and glass substrate.

Upon confirmation that the fabricated ion-exchanged waveguides were working, the first evanescent coupling test was attempted using Fineplacer Lambda. A glass substrate with ion-exchanged waveguides was placed on the stage, while the silicon PIC was mounted on a pick-up tool above the substrate. Alignment marks on both the silicon PIC and the glass substrate can be easily seen through the system camera and alignment was done manually

until the marks converged (Fig. 5.21). Refractive index oil from Cargill (n = 1.46) was then applied on the surface of the glass substrate, and silicon PIC was brought into contact.

No coupling signal was observed during the first assembly test, and the sample was mechanically polished to examine the interface between the silicon PIC and the glass substrate (Fig. 5.22). It was found that a gap at least 2.8 µm existed between the two components, and that the pick-up tool and the stage of Fineplacer Lambda was not perfectly parallel. For electronics flip-chip bonding, this will not be an issue as bond pads about 50 µm in diameter while solder bumps height are higher than 30 µm. However, optical coupling features are 20x smaller than electronics, and even a small 0.5 µm misalignment will cause a signal change.

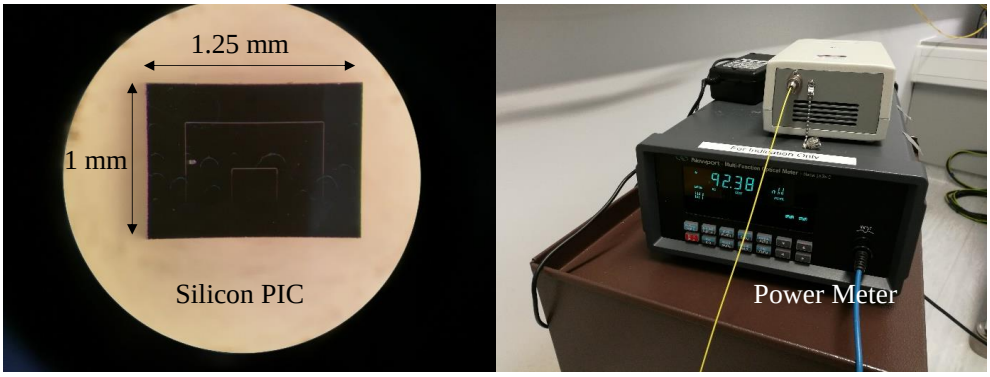


Fig. 5.23. Contact area reduction to reduce the assembly gap appears to be in the right direction with nW coupling power observed.

In order to minimize assembly gap and co-planarity issues, the silicon PIC size was reduced from 10 mm x 10 mm to 1 mm x 1.25 mm to reduce the contact area on the glass substrate. The experiment was repeated with the same configuration, and a faint optical coupling was observed through the output power meter (Fig. 5.23). A further reduction in contact area was subsequently attempted by splitting the glass substrate through mechanical

dicing and polishing. However, dicing and polishing burr at the edges of the glass substrate damaged the silicon waveguides on the PIC and render it unusable (Fig. 5.24).

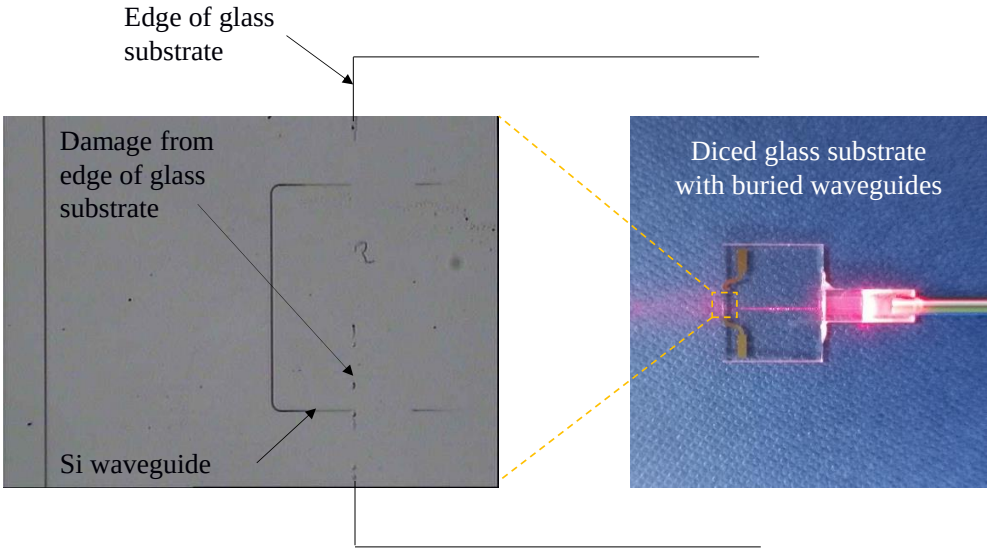


Fig. 5.24. Glass substrate was mechanically diced and polished in the middle to further reduce the contact area with silicon PIC, but caused burr damage on silicon waveguide instead.

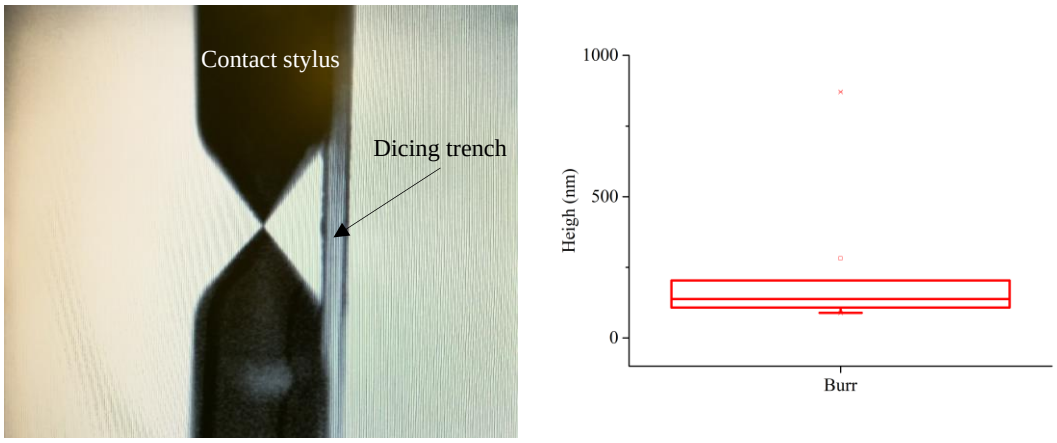


Fig. 5.25. Surface profiling of dicing burr. Graph shows the distribution of burr heights across different dicing trenches.

Analysis of dicing burrs using Tencor's surface profiler showed that they can be as high as 870.5 nm. Aside from its potential in damaging silicon nano-tapers (220 nm), a

natural gap will exist between the tapers and buried waveguides, preventing evanescent energy exchange between the two.

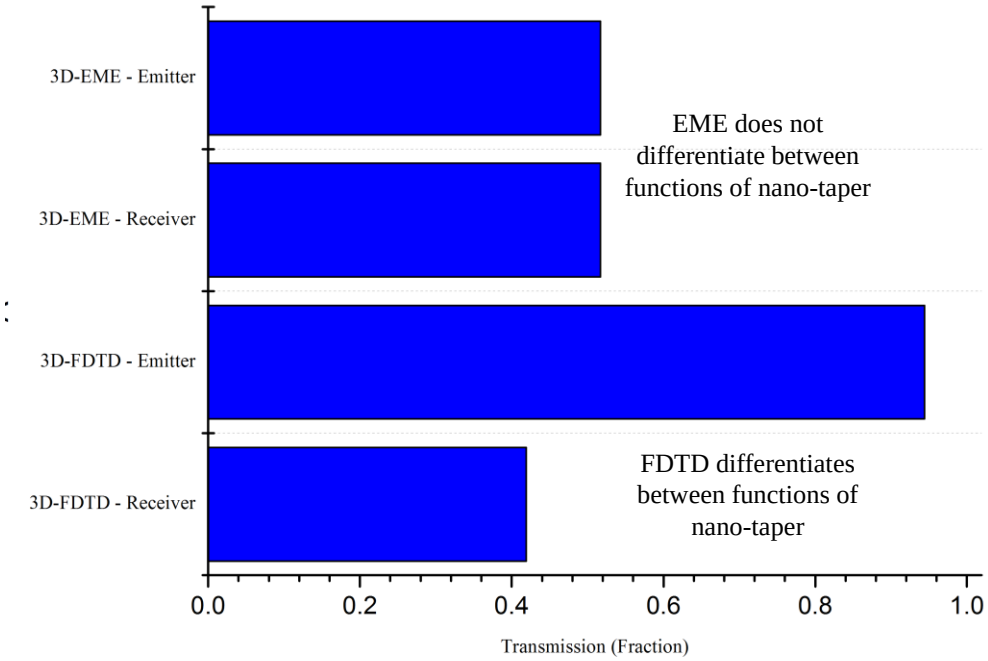


Fig. 5.26. Difference between MODE-EME and 3D-FDTD, using silicon nano-taper design 1 as simulation structure.

While the test vehicle designs cannot be verified experimentally, attention was later directed towards understanding the difference between MODE-EME and 3D-FDTD, using design 1 as an example. 3D-FDTD, while more resource-heavy compare to MODE-EME, showed an interesting behaviour that cannot be detected in the latter (Fig. 5.26). As MODE-EME solves only the eigenvalues at the interfaces and is bi-directional, the function of silicon nano-taper as an emitter or receiver was not differentiated. 3D-FDTD on the other hand showed that the silicon nano-taper will perform well as an emitter, allowing 94.4% transmission into the buried glass waveguide. However, it can receive only 41.9% transmission from the glass waveguide. It is further hypothesised that a smaller taper tip will be necessary to improve performance of silicon nano-tapers as receivers, and that tapers will have to be optimized separately depending on its functions.

5.6 CHAPTER SUMMARY

In this chapter, evanescent coupling based on buried glass waveguides had been proposed for future integration with through glass via (TGV) interposers. Baseline simulations and test vehicle designs using Lumerical MODE-EME were performed and experimentally tested. It was found that equipment capability (co-planarity control, dicing burrs, etc.) and clean room environment (particles and contamination) are the critical factors in realising glass coupling in the current configuration. At the same time, constant abrasion due to hard glass surface is detrimental to non-oxide/nitride protected silicon nano-taper. It is thus recommended to add a soft buffer layer to reduce abrasion and improvements in assembly equipment are needed for subsequent work. It was also found that the silicon nano-taper behaves differently depending on its function as a receiver or an emitter, and designs have to be separately optimized for real applications. The knowhow and assembly experiences gained from this work also allows a collaboration with an industrial company (non-disclosure agreement in place) to be formed to further investigate and improve evanescent coupling designs using polymer waveguides.

5.7 REFERENCES

[1] S. Han, "Highly Scalable Silicon Photonic Switches Based on Waveguide Crossbar with Movable Waveguide Couplers," *Dissertation for Doctor of Philosophy in Engineering*, University of California, Berkeley, 2016.

[2] EME, *Lumerical Knowledge Base*, Lumerical Inc.

[3] D. F. G. Gallagher, T. P. Felici, "Eigenmode Expansion Methods for Simulation of Optical Propagation in Photonics – Pros and Cons," *Proceedings of SPIE*, Vol 4987, p.69-82, 2003.

[4] M. Morita, T. Ohmi, E. Hasegawa, M. Kawakami, M. Ohwada, "Growth of native oxide on a silicon surface," *Journal of Applied Physics,* Vol. 68, No. 3, pp. 1272-1281, 1990.

[5] Email communications with Phillipe Bado, *Translume*, 6th May, 2016.

[6] Email communications with Florent Gardillou, *TEEM Photonics*, 3rd November, 2016.

[7] Technical data sheet, NOA 61, Norland Products.

[8] Technical data sheet, NOA 65, Norland Products.

DESIGN RULES

6.1 PACKAGING DESIGN RULES

The way a device is laid out dictate how it can be packaged. This is thus the single most important factor for any device designer to keep in mind, unless the device is only meant to stay on the probe station in the laboratory. As previously discussed in Chapter 1 and further demonstrated in Chapter 2 and 3, a silicon photonic device typically has both electrical and optical ports, while some may have additional ports, e.g. fluid injection ports and microfluidic routing channels for sensing applications. Preferably, a chip designer should first communicate with the targeted packaging foundry on the acceptable requirements. Co-designing a device with a packaging foundry is gaining traction nowadays as it mitigates potential design incompatibility between upstream and downstream processes. Co-designing also reduces time-to-market and brings down manufacturing cost, thus benefitting consumers. The following sections highlight some of the design rules that a designer can consider for packaging, some of which are being adopted for H2020-MORPHIC, an EU funded programmable MEMS optical switch project and other projects within the group.

.

6.1.1 DISTRIBUTION OF ELECTRICAL AND OPTICAL PORTS

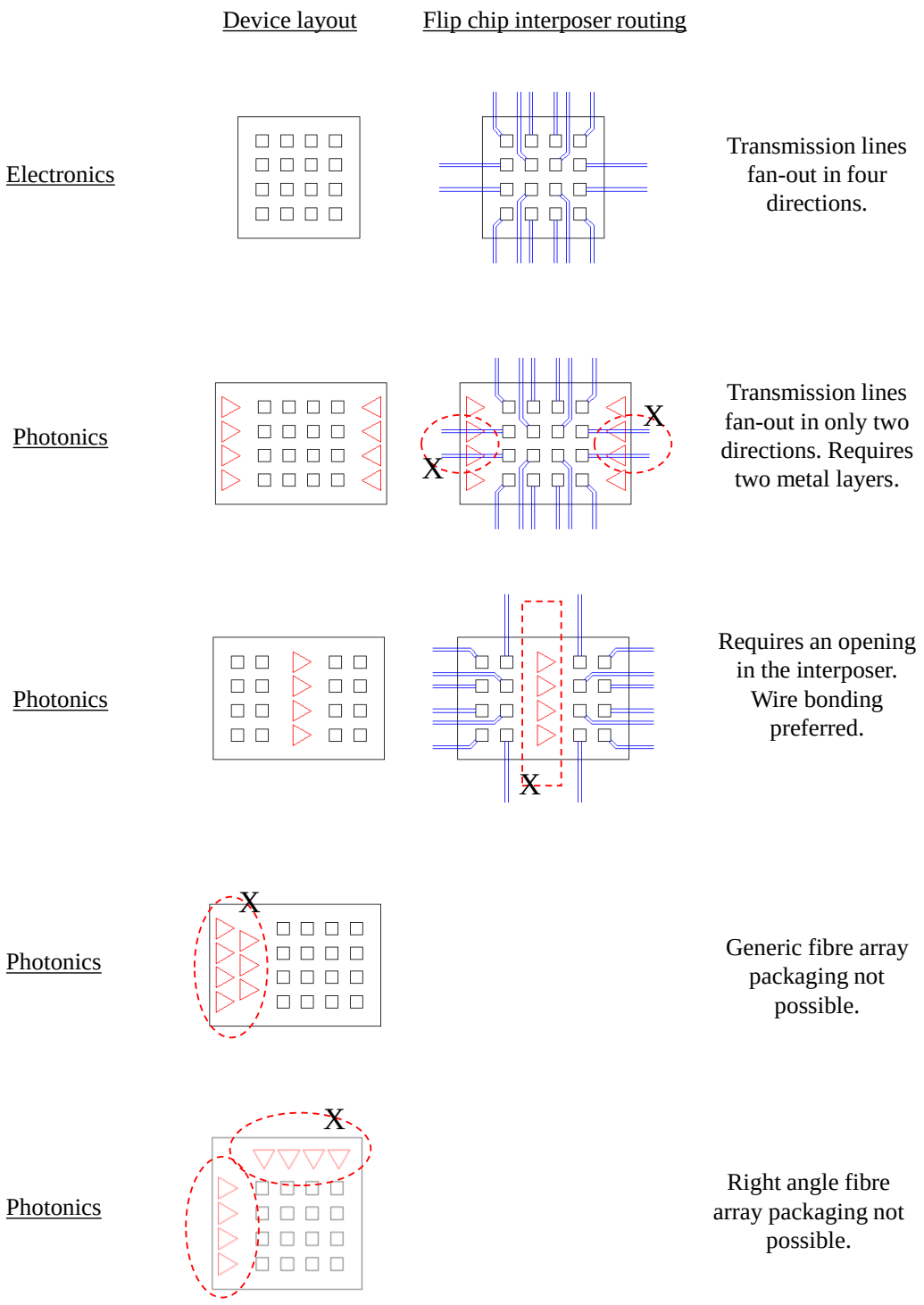


Fig. 6.1. Effect of device layout on packaging design and transmission lines routing on electrical interposer. Electronic device packaging is included for comparison.

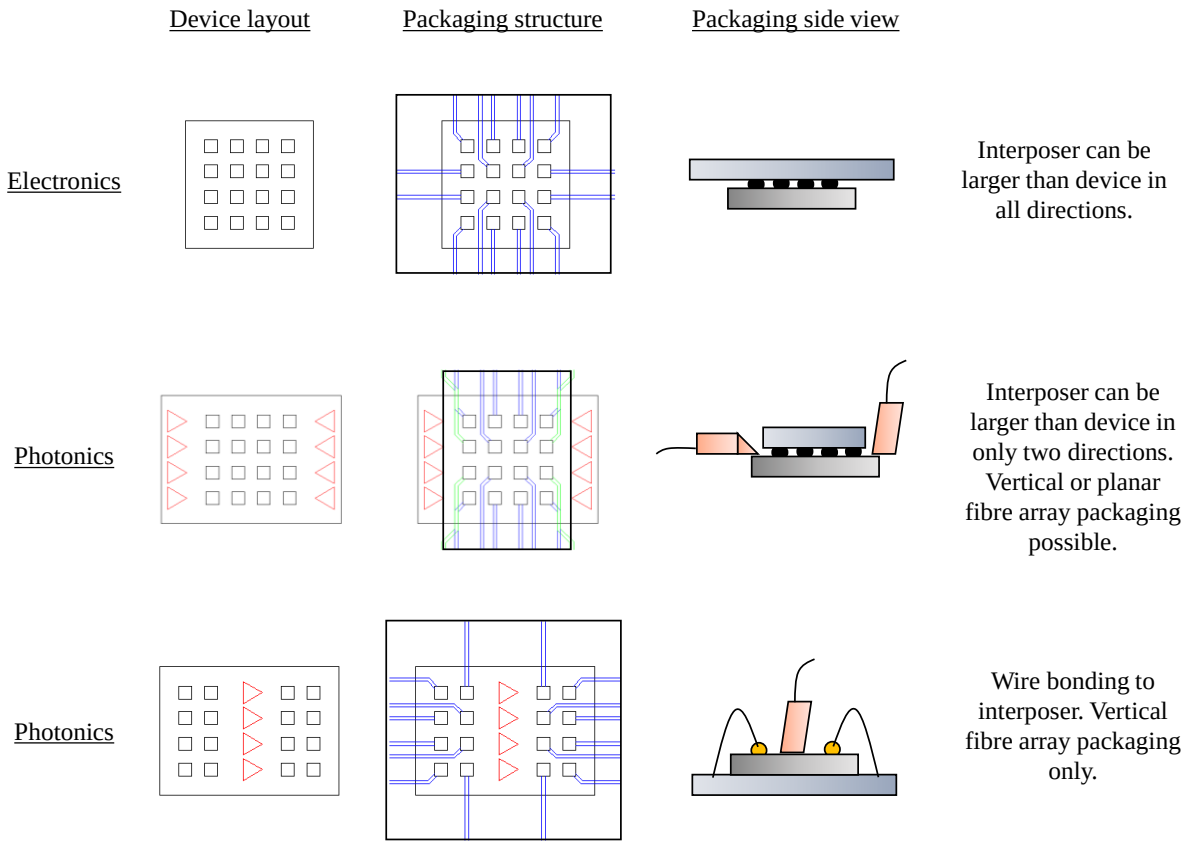


Fig. 6.2. Suggested flip chip packaging structure based on generic device layout. Electronic device packaging is included for comparison.

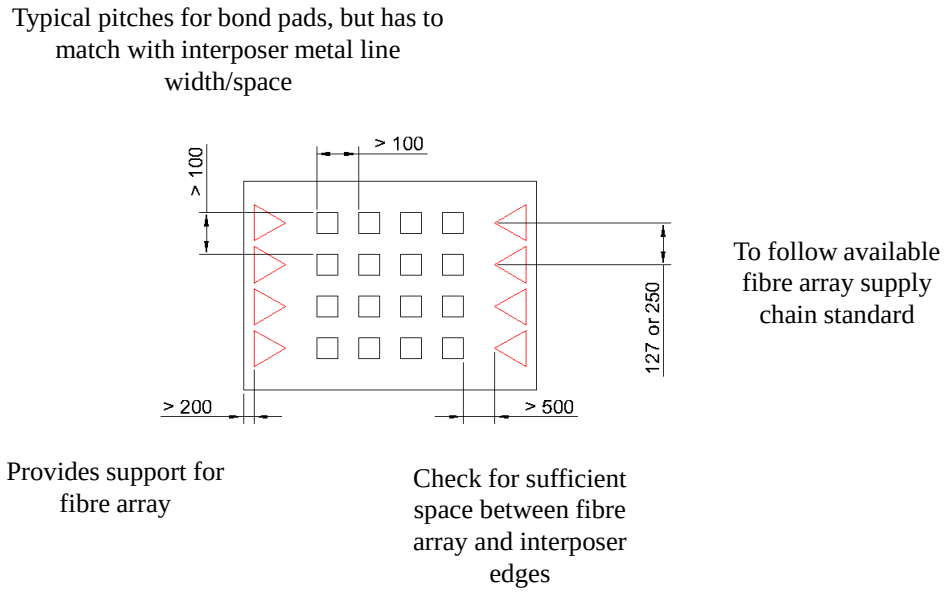


Fig. 6.3. Suggested dimensions (in μm) on a silicon photonic device.

6.1.2 COMMON PACKAGING MATERIALS

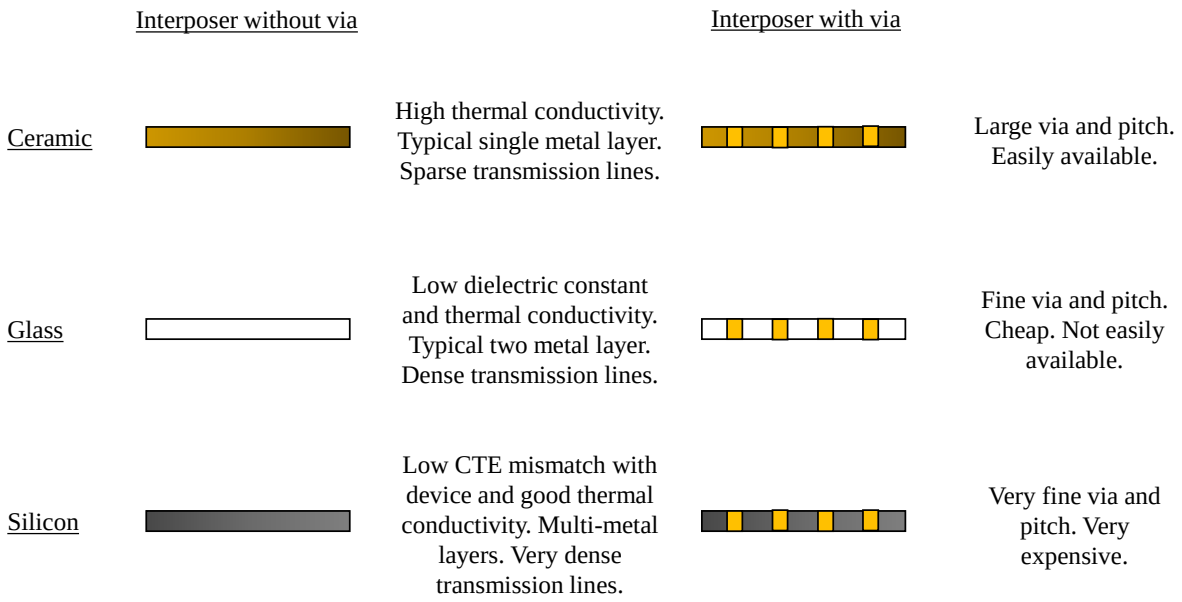


Fig. 6.4. Typical materials for electrical interposers and their availabilities for research purposes. Cost is heavily influenced by requested volume and interposer designs.

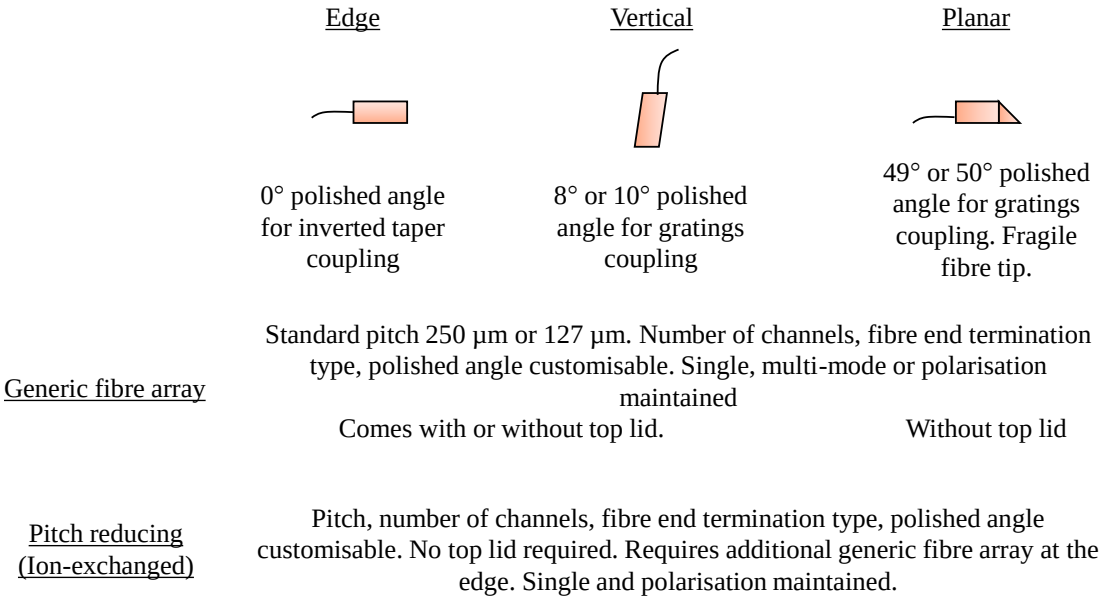


Fig. 6.5. Common type of fibre coupling materials and polished angles for silicon photonic devices. Generic fibre arrays are cheap.

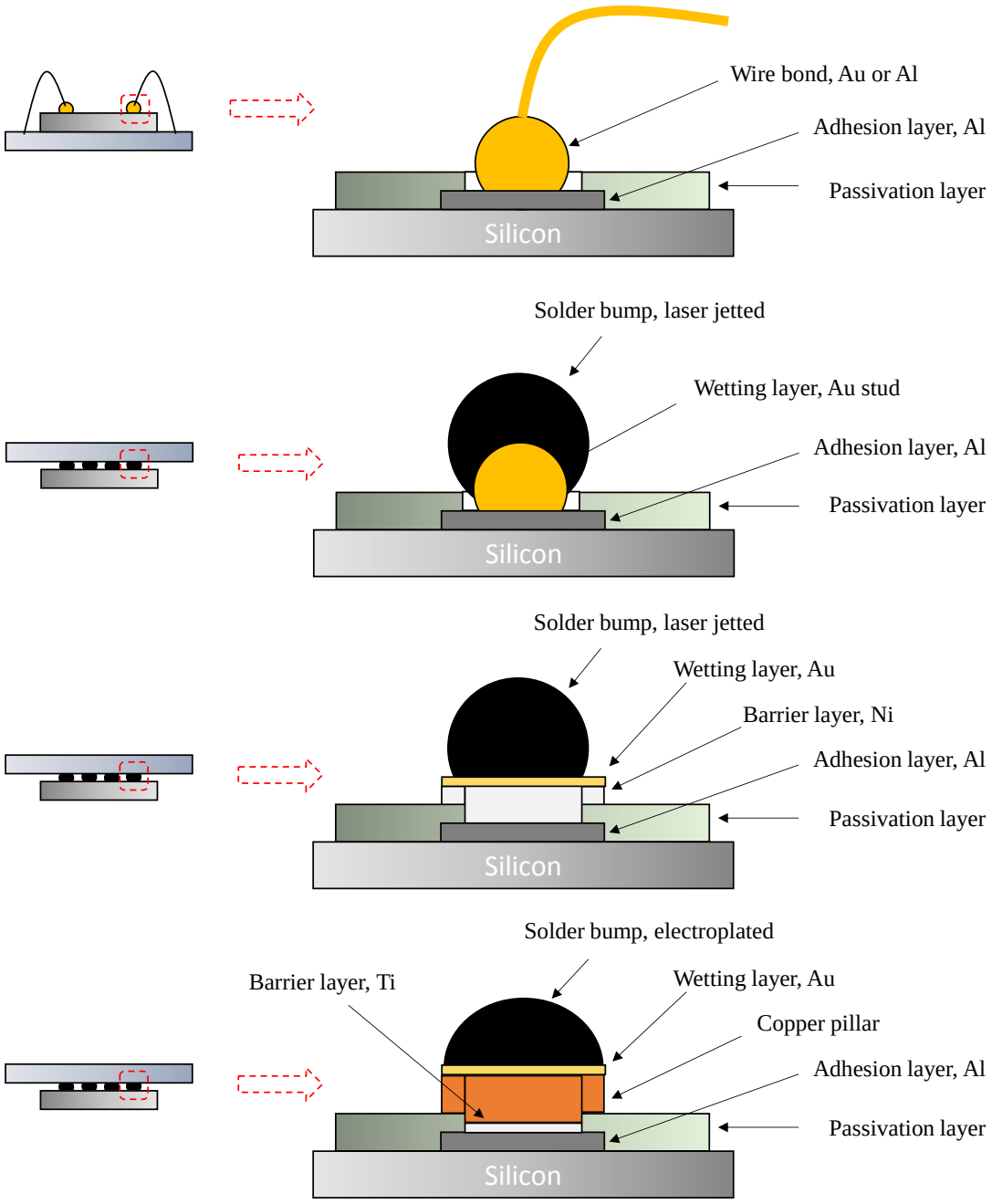


Fig. 6.6. Common electrical interconnects structure and metallization layers on device bond pad.

CONCLUSIONS

Silicon photonic industry has experienced tremendous growth over the past three decades, with various functionalities realised to date. MarketsandMarkets™ has expected the industry to grow from "US$ 626.8 M in 2017 and is expected to reach US$ 1,988.2 M by 2023." The growth has been made possible with the advancement in CMOS processing, driven by consumable electronics. However, similar to the electronics industry in the early years, silicon photonic industry today is extremely fragmented with various chip design and layout. Most silicon photonic devices fabricated were never meant to reach the hand of consumers, due to a lack of information related to packaging design. While much of the processes, equipment and materials can be generally adopted from the electronics packaging industry, the existence of optical interfaces has led to a reduction in freedom in terms of packaging design, process and materials integration.

In this thesis, readers have been introduced to a variety of new silicon photonic packaging technologies and concepts. Section I successfully demonstrated high density optical and electrical packaging components through collaboration with University of California, Berkeley. Innovative package designs and process integration of various components and materials for 2D and 2.5D heterogeneous integration such as through-glass-via and fan-out optical interposers, were fabricated and demonstrated. Together, these components demonstrated the world's first silicon photonic MEMS optical switch package and subsequently the highest density silicon photonic packaging components at 512 electrical I/Os and 272 optical I/Os. The concepts and design rules demonstrated in the section had been utilized in H2020-MORPHIC and other packaging projects within the group. A set of

packaging design rules to assist silicon photonic circuit designer was also complied and included in this thesis.

Section II further expanded the discussions on advanced silicon photonic packaging, focusing on passive optical coupling. Approaches such as grating-to-grating and evanescent (inverted taper to glass) coupling that can be integrated in the future with packaging test vehicles demonstrated in Part I were discussed and studied. Key interests for these approaches will be the removal of active fibre coupling from devices thus suitable for msas productions. The concepts and background research done in this section served as the foundation for future Ph.D candidates as well as other packaging projects within the group.

APPENDIX

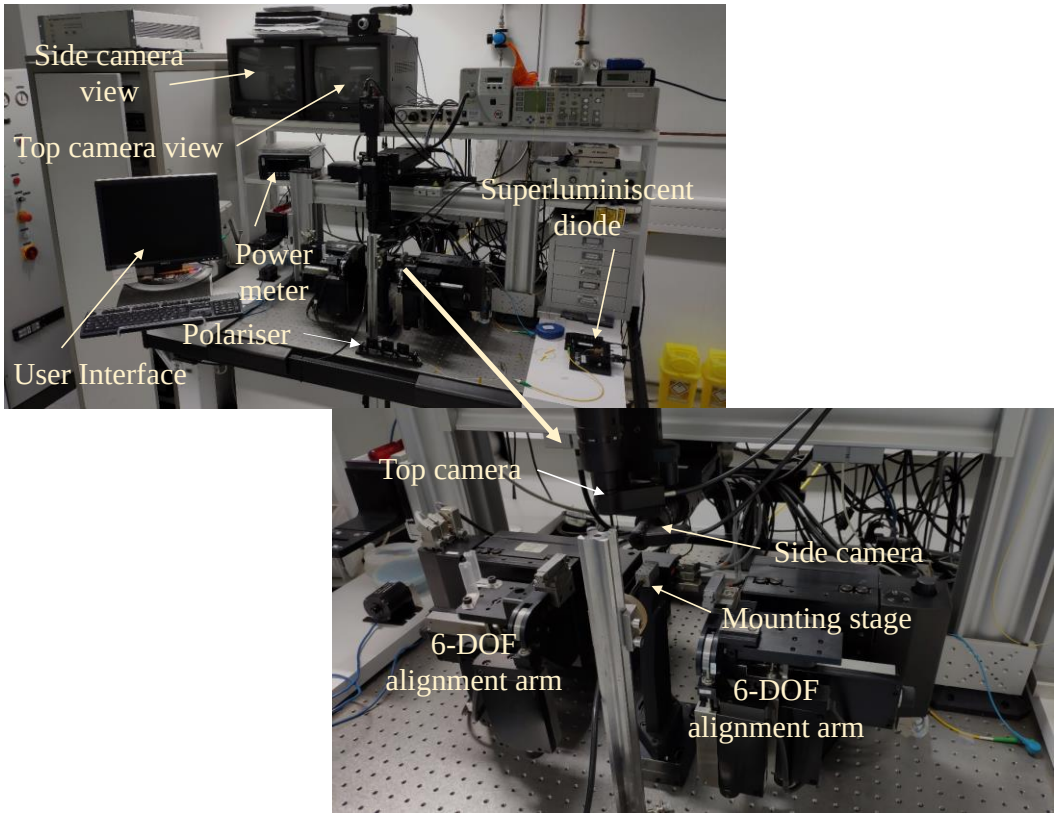


Fig. A1. Auto-aligner by Newport Corp. used for fibre alignment from 1-channel all the way to 136-channels as demonstrated in this thesis. The system consist of two 6-degree of freedom alignment arms, one top and one side view camera to assist with active alignment process. Suitable for vertical or plaanr fibre coupling, with the help of specially designed fibre array gripper. Travel distances of the alignment arms, top and side cameras have to be carefully considered during the design stage to prevent obstructions.

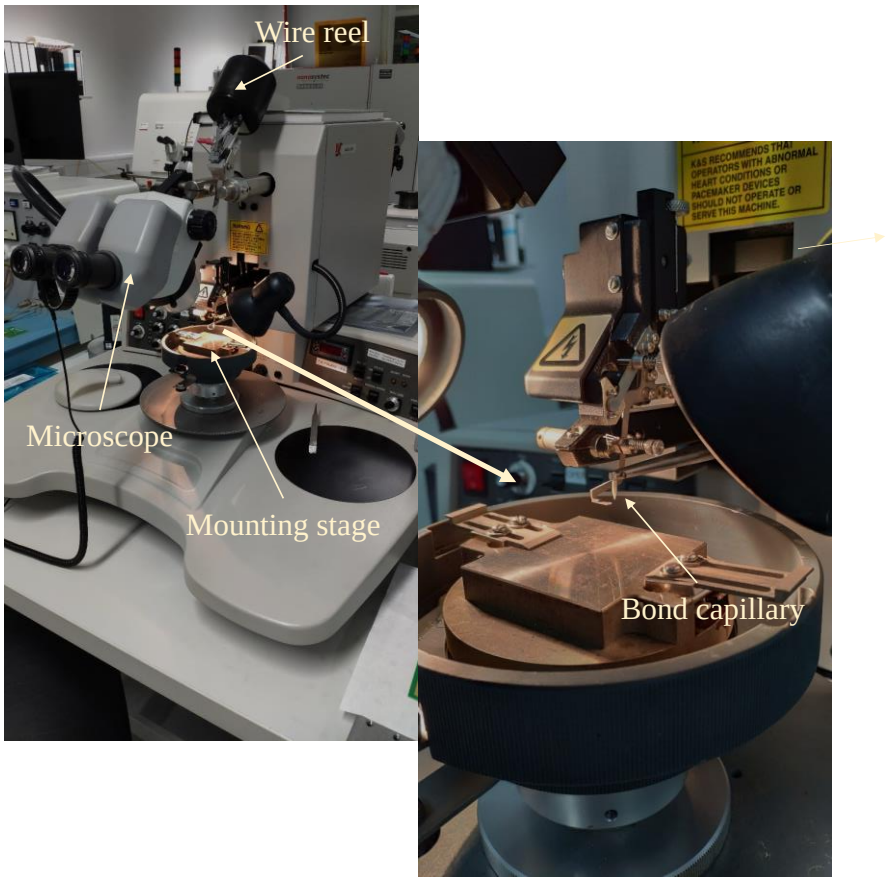


Fig. A2. Manual wire bonder by K&S used for Au stud bumping on device bond pads and wire bonding to connect device to interposer or test board. Typical wire diameter used on the system is 0.8 and 1.0 mil.

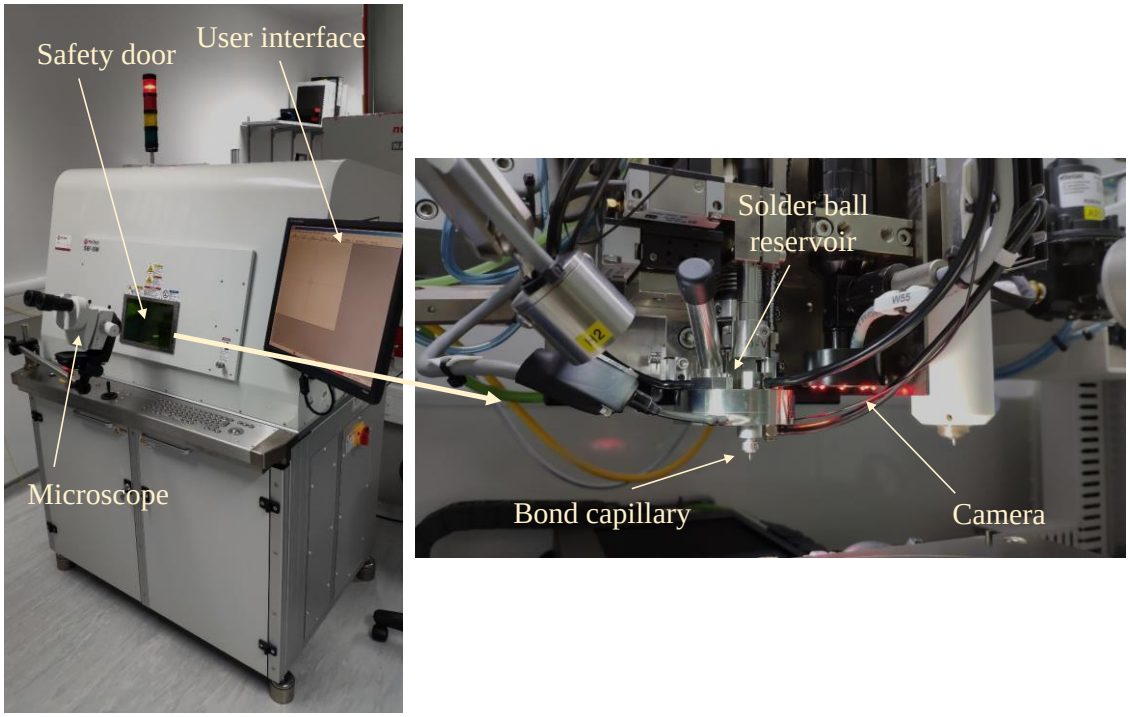


Fig. A3. Solder jetting system by Pactech (SB^2-SM), used to form solder bumps on device bond pads. The system can currently process only Φ50 μm SAC 305 solder spheres. Operation can be automated with the help of bond map. Bond pad metallization preferably to be Au finishing for better wetting with Sn from SAC 305.

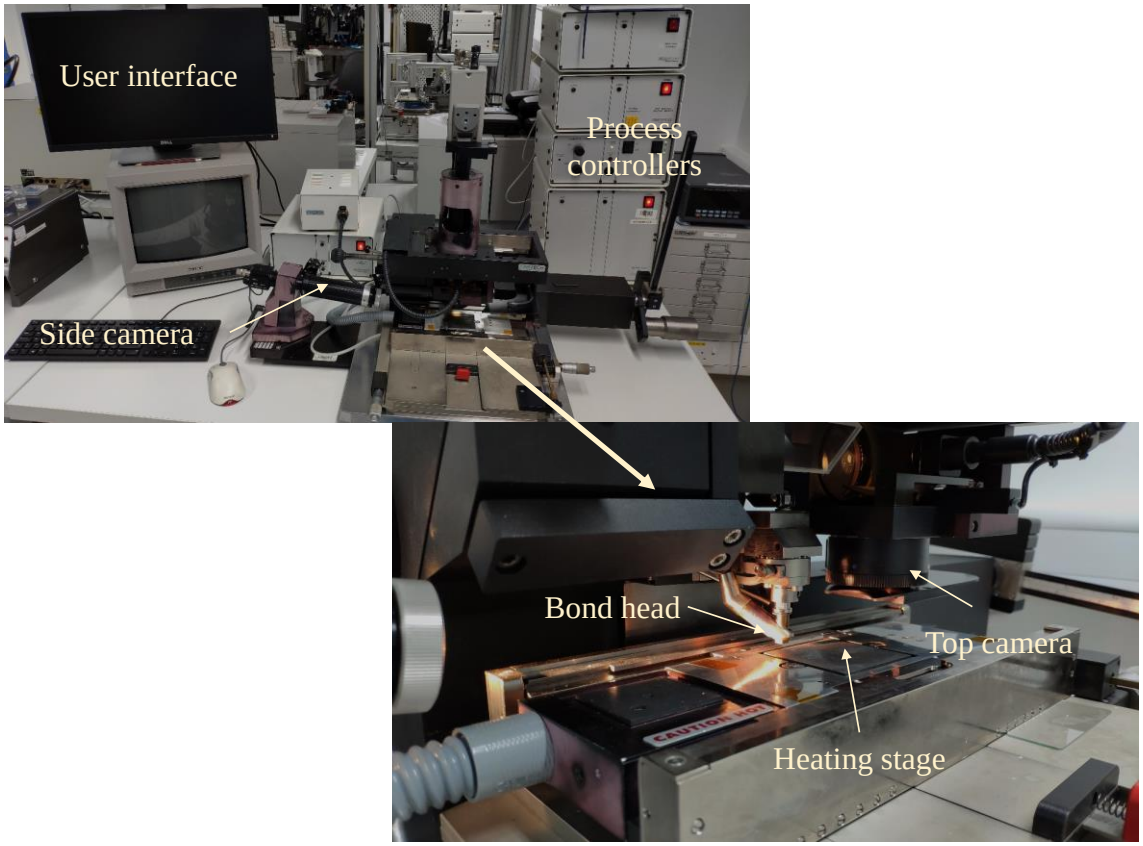


Fig. A4. Flip chip bonder by Finetech (Fineplacer lambda), used for flip chip and thermo-compression bonding of various components. Can go up to 40 N force and 400 °C reflow. Maximum alignment field of view of 2.5 mm x 2.5 mm at highest magnification. Alignment between top and bottom components are based on matching fiducials (alignment marks) on both components.

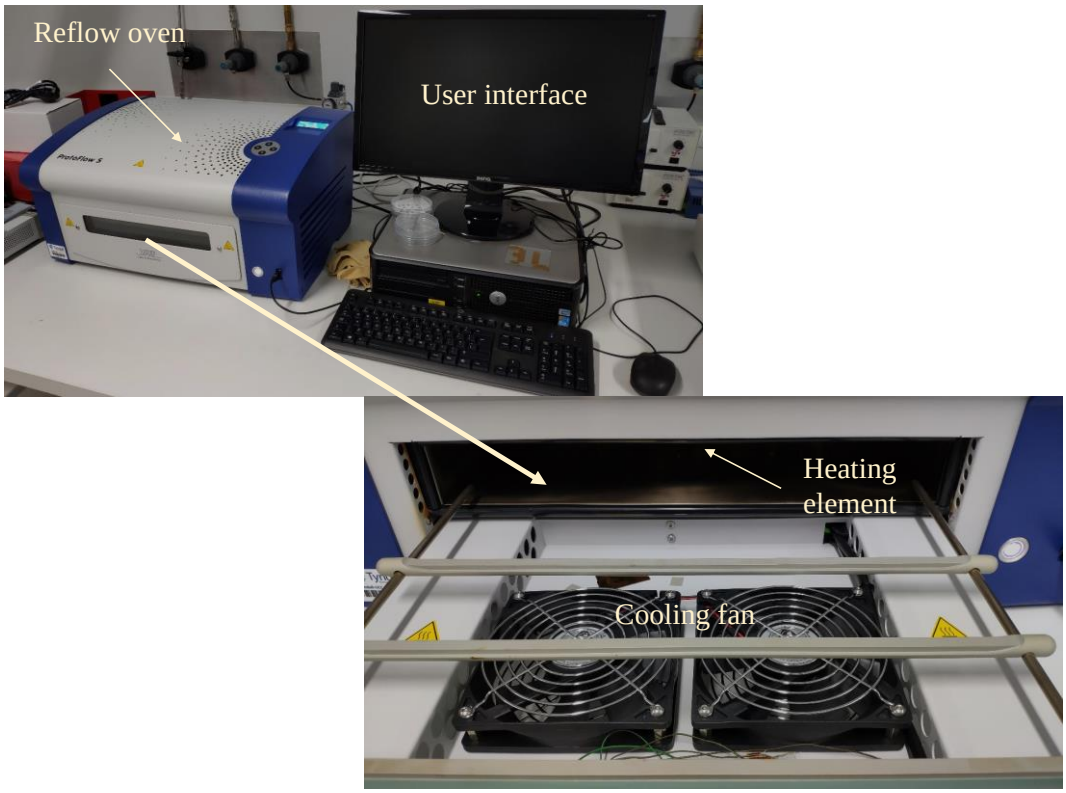
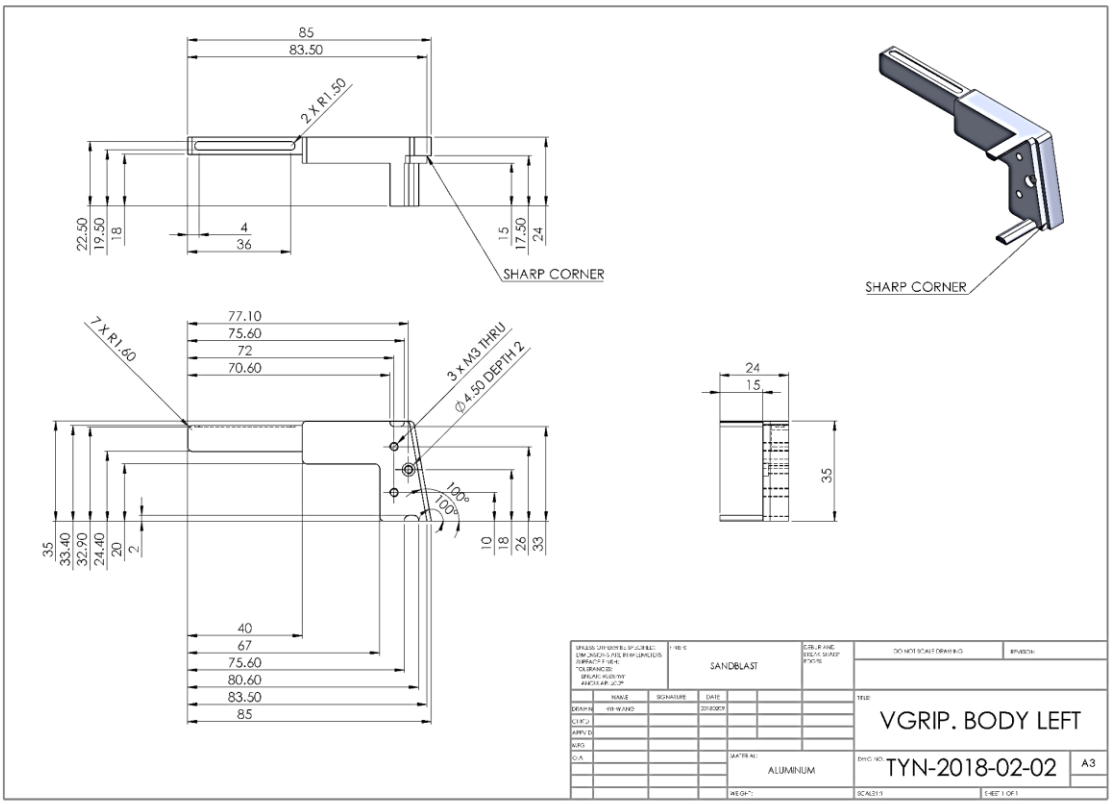
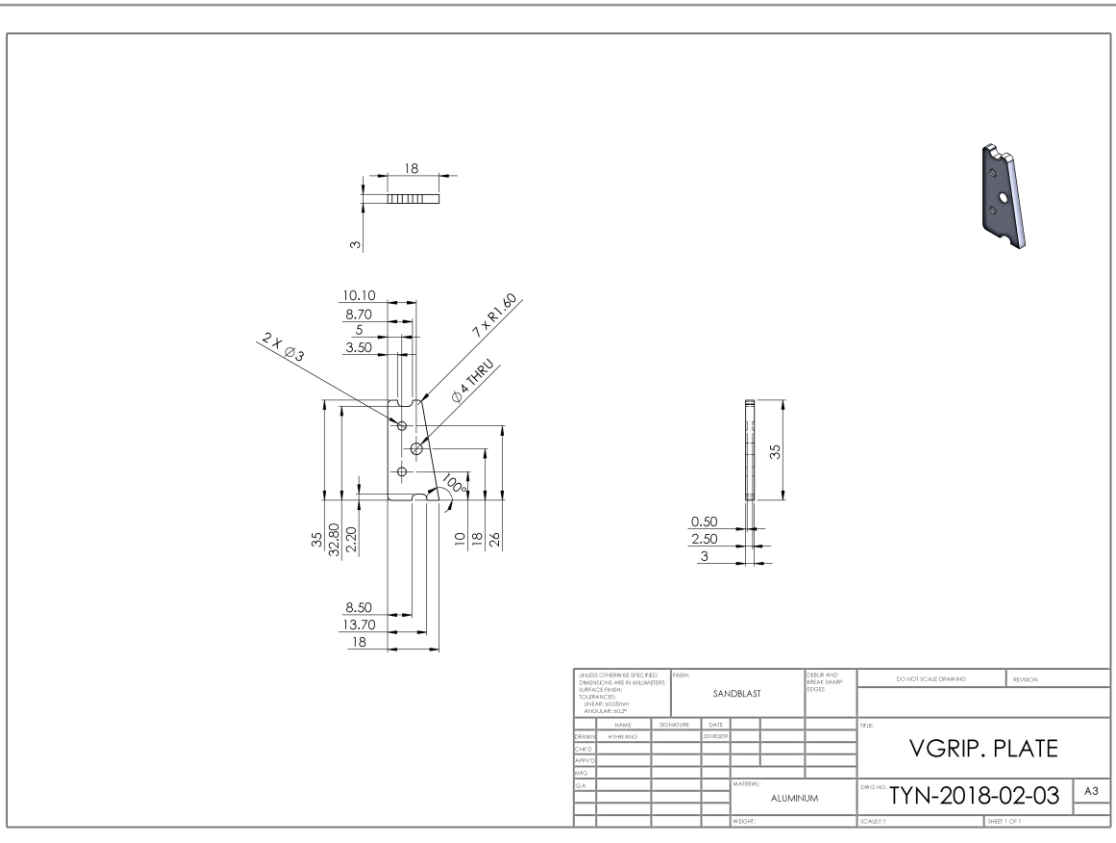
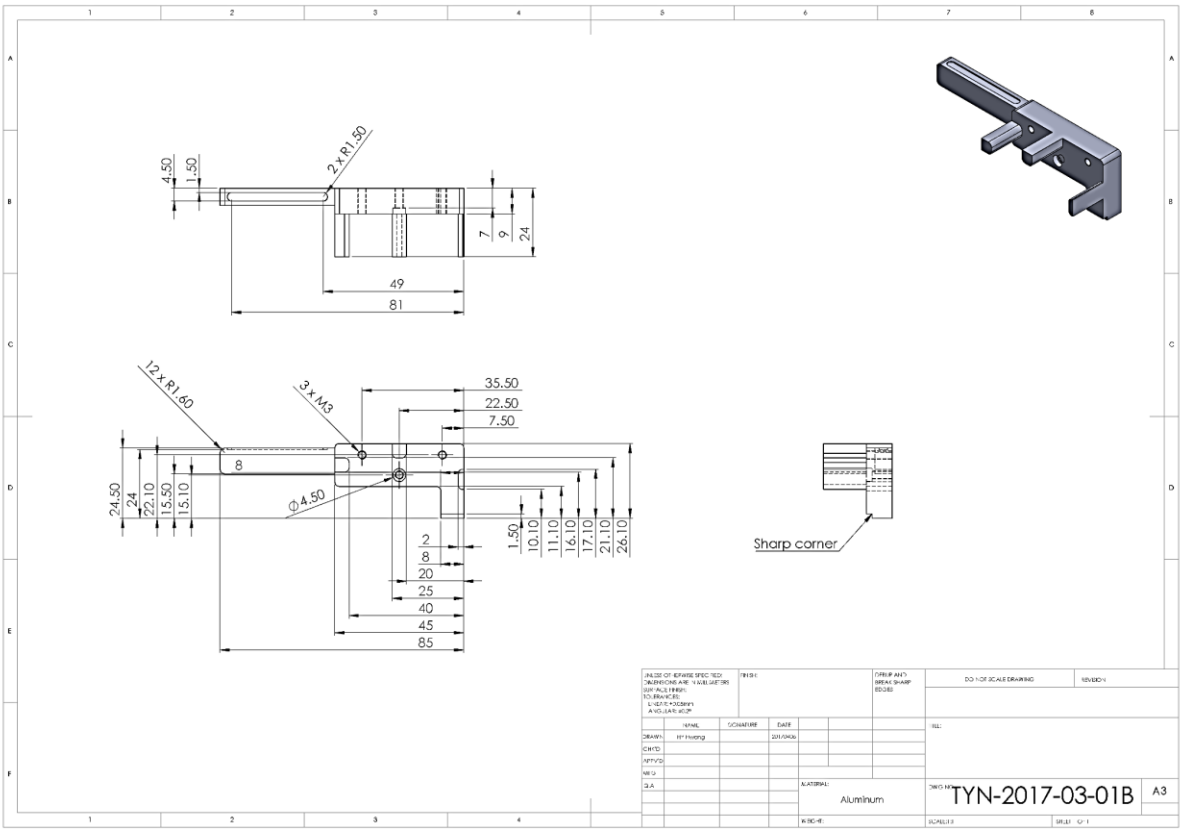
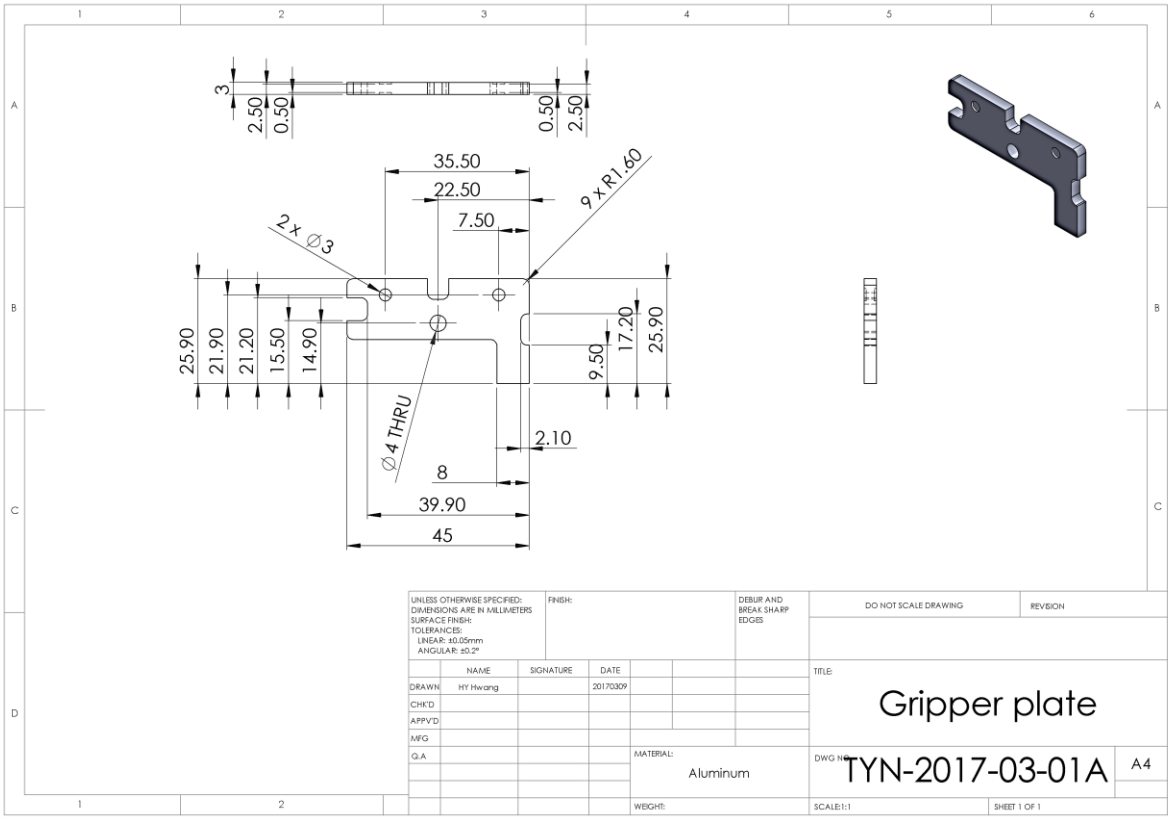


Fig. A5. Inert (N_2) reflow oven by LPKF (Protoflow-S) used for board level reflow. Reflow temperature can reach 320 °C thus suitable for AuSn assembly. Can be used as curing oven for underfill and die attach as well.


85
83.50
2 X R1.50
22.50
19.50
18
4
36
15
17.50
24
SHARP CORNER
SHARP CORNER
7 X R1.60
77.10
75.60
72
70.60
3 x M3 THRU
Ø4.50 DEPTH 2
100°
35
33.40
32.90
24.40
20
2
10
18
26
33
24
15
35
40
67
75.60
80.60
83.50
85
SANDBLAST
ALUMINUM
VGRIP. BODY LEFT
TYN-2018-02-02
A3


18
3
10.10
8.70
5
3.50
2 X Ø3
7 X R1.60
Ø4 THRU
100°
35
32.80
2.20
10
18
26
8.50
13.70
18
35
0.50
2.50
3
SANDBLAST
ALUMINUM
VGRIP. PLATE
TYN-2018-02-03
A3


2 x R1.50
4.50
1.50
7
9
24
49
81
12 x R1.60
3 x M3
35.50
22.50
7.50
8
24.50
24
22.10
15.50
15.10
⌀4.50
2
8
20
25
40
45
85
1.50
10.10
11.10
16.10
17.10
21.10
26.10
Sharp corner
Aluminum
TYN-2017-03-01B
A3


3
2.50
0.50
0.50
2.50
35.50
22.50
7.50
9 x R1.60
2 x ⌀3
25.90
21.90
21.20
15.50
14.90
9.50
17.20
25.90
⌀4 THRU
2.10
8
39.90
45
UNLESS OTHERWISE SPECIFIED:
DIMENSIONS ARE IN MILLIMETERS
SURFACE FINISH:
TOLERANCES:
LINEAR: ±0.05mm
ANGULAR: ±0.2°
FINISH:
DEBUR AND BREAK SHARP EDGES
DO NOT SCALE DRAWING
REVISION
NAME
SIGNATURE
DATE
DRAWN
HY Hwang
20170309
CHK'D
APP'V'D
MFG
Q.A
MATERIAL:
Aluminum
WEIGHT:
TITLE:
Gripper plate
DWG NO.
TYN-2017-03-01A
A4
SCALE:1:1
SHEET 1 OF 1

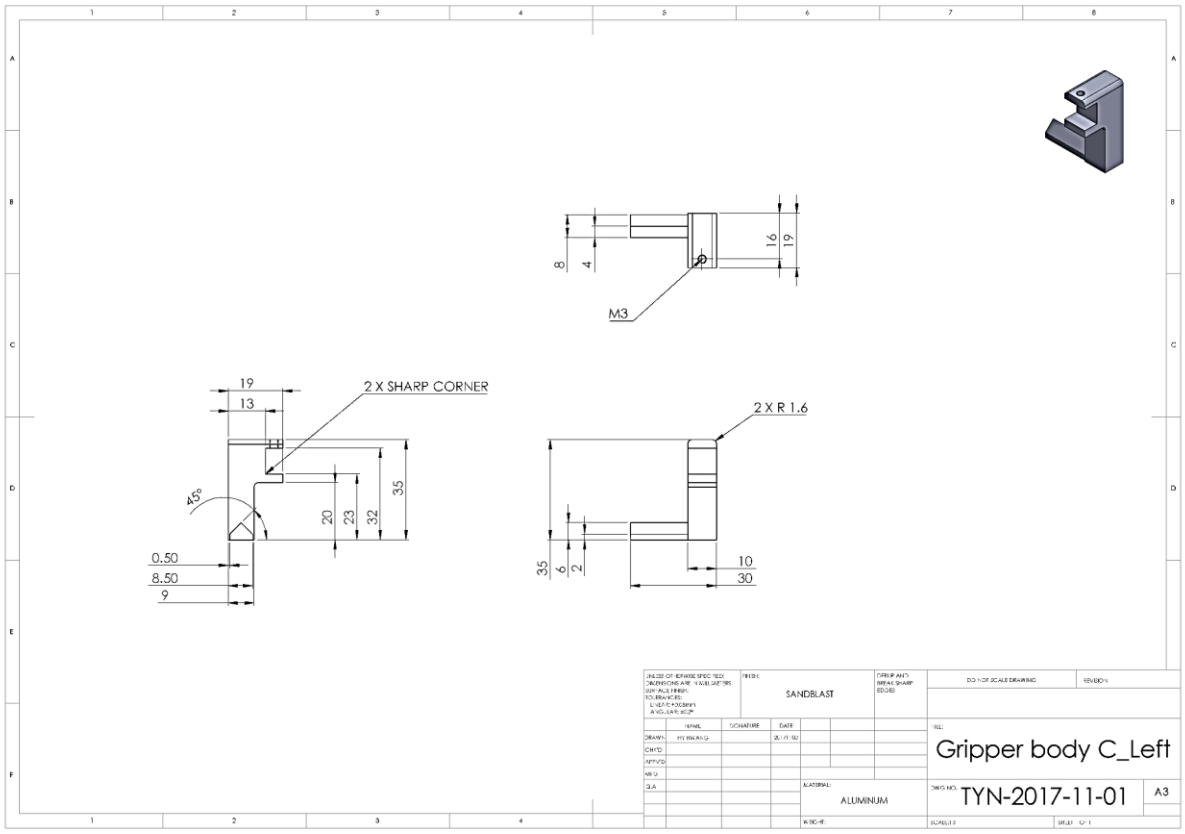


Fig. A6. Engineering drawings for fibre array grippers used in this thesis. As one set of grippers consist mirrored components, only one side is shown here. (a) Main body and gripping plate for vertical fibre coupling. (b) Main body and gripping plate for planar fibre coupling. (c) Adjustable arm suitable for both vertical and planar fibre coupling. Components were designed considering travel length of Auto-aligner and expected board size that can be mounted on the system.

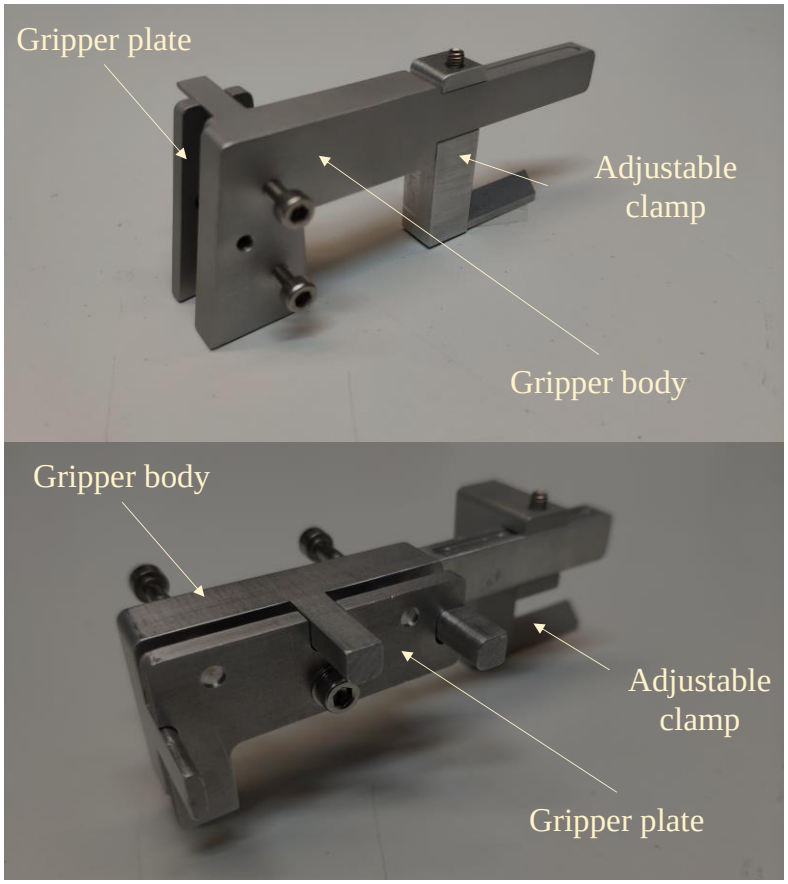


Fig. A7. Two of the fibre array grippers fabricated in this thesis, (a) for vertical fibre coupling and (b) planar fibre coupling.