POLLACK PERIODICA
An International Journal for Engineering and Information Sciences
DOI: 10.1556/606.2019.14.2.19
Vol. 14, No. 2, pp. 211–222 (2019)
www.akademiai.com

A MULTI-CHANEL ELECTRICAL IMPEDANCE METER BASED ON DIGITAL LOCK-IN TECHNOLOGY

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Received 2 January 2018; accepted 26 November 2018

Abstract: The presented multichannel measuring system working on various frequencies is suitable either for electrical impedance spectroscopy or tomography. The authors of this paper have developed the complete measurement system and a graphical user interface platform. The accuracy of impedance amplitude and phase are 1 ppm and 0.01°, respectively. The basic instrument works with 8 channels and can be expanded to 64 channels with the application of multiplexing or multiple parallel connected instruments in the same system.

Keywords: Digital signal processor based instrument, Impedance measurements, Lock-in amplifier

1. Introduction

Today measuring methods, as Electrical Impedance Spectroscopy (EIS) [1] and Electrical Impedance Tomography (EIT) [2], [3] are frequently applied in various science disciplines: medicine, diagnostics and material investigations as well. For most instruments of this field the use of lock-in amplifier is indispensable in the measurement method. Lock-in amplifier is an effective device for weak signal detection, even in the presence of high noise level. The lock-in amplifier has been widely applied to various scientific areas including detection of electric signals, weak optical signals, weak magnetic signals, vibration signals, and physiological signals, etc. Lock-in amplifiers

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can be categorized into two types based on phase sensitive detectors in use: analogue lock-in amplifiers and digital lock-in amplifiers.

There are several approaches for developing lock-in amplifiers using different technological concepts and methodologies. Paper [4] describes a digital implementation of a lock- in amplifier, based on the classic quadrature technique and on a mathematical algorithm for error signal extraction. In [5] a digital lock-in amplifier built with a couple of input/output boards in a personal computer is described. Paper [6] presents a novel approach to the design of a digital ohmmeter with achieved resolution of < 60 μΩ using only a general-purpose microcontroller and a high-impedance instrumentation amplifier. In [7] a high performance digital lock-in amplifier implemented in a low-cost Digital Signal Processor (DSP) board is described, where the lock-in amplifier is capable of carrying out measurements applying different excitation frequencies (chirp signals). The tech market offers many instruments, which are developed with different functionalities applying the lock-in amplifier technique for the measurement. The market leader companies that develop these instruments are the Zurich Instruments [8] and the Stanford Research Systems [9].

In case of high precision measurements many methods are used: Fourier analysis [10], information-filtering demodulation [11], impedance measurement system based on digital auto-balancing bridge [12], four-point single sinusoidal signals instantaneous frequency estimation method [13], or the lock-in amplifier method [14], [15]. The reason for choosing the lock-in amplifier is its extremely high resilience to noise effects [7].

Regarding the complex multi-channel measuring instruments the development of a Field-Programmable Gate Array (FPGA) based embedded system is advantageous [16]. On the other hand, numerous simple impedance analyzers were reported recently, which are based on microcontrollers and dedicated impedance converters [17]. Keysight Technologies is one of the leader companies that offers high-precision impedance measuring and analyzing instruments [18].

2. Basic overview of the instrument

The main goal was to develop a multifunctional instrument, which can be used for EIS and EIT measurements. The instrument is capable of measuring impedance, impedance spectra, and Fast Fourier Transform (FFT) spectra on each channel independently. In order to perform multi-frequency EIT measurements, it is practical to measure the impedance values in the spectral domain. The FFT spectrum of a measured signal contains essential information about the excitation and the properties of the measured domain as well. As a result of research activity, an up to 64 channels, high precision and high resolution lock-in amplifier had been developed. The realized system incorporates FPGA, Advanced Risk Machine (ARM) and Personal Computer (PC) technologies. The system (*Fig. 1*) consists of the following elements:

- generator board - contains a digital sine generator, DA converters and an analog signal mixer;

- receiver boards - they consist of analog boards which receive analog signals and convert them into a digital form; and a digital receiving board as well, which implements signal processing routines.

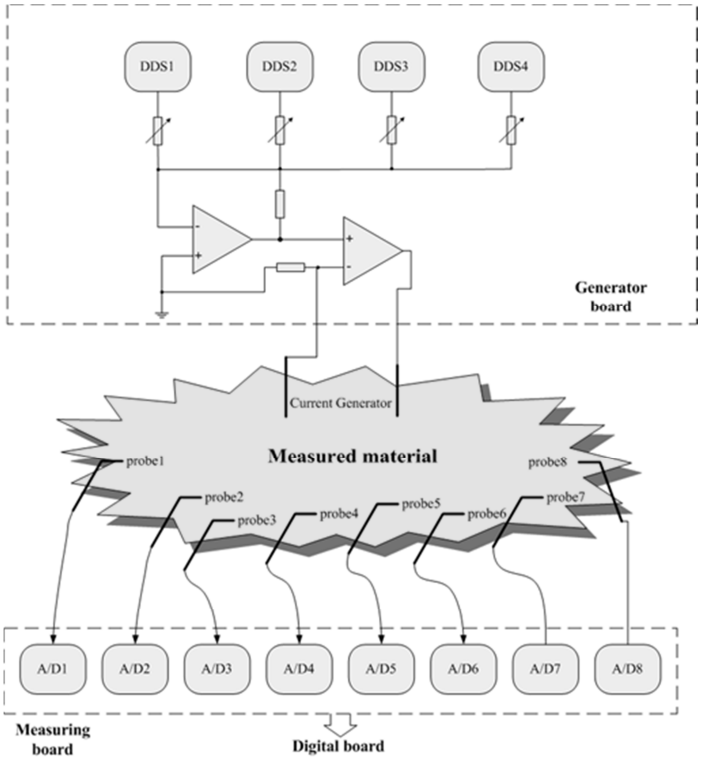

Fig. 1. Conceptual scheme of measurement process

The generator can be operated as current, or voltage generator. It provides monochromatic sine wave in a frequency range between 1 mHz to 100 kHz, with a Total Harmonic Distortion +Noise (THD+N) greater than –100 dB. The maximum noise levels in the frequency range 0.1 Hz to 40 kHz are 150 fA_{eff} for the current, while 1.5 μV_{eff} for the voltage. The range of applicable excitations is 110 dB in both current-generator and voltage-generator modes with maximum values of 10 mA peak to peak and 10 V peak to peak, respectively. The signals are digitalized by the receiver board applying 24-bit Analog-Digital (AD) converters and processed further on the digital platform controlled by the PC. During the precise impedance calculations (48 bit resolution for both real and imaginary parts) all operations regarding signal manipulations and parameter extractions are performed in the digital domain. One of the most important sensitivity features of the equipment is the accuracy of 1 ppm for amplitude and 0.01° for phase.

Fig. 1 shows the basic measurement set-up of the instrument. The generator board allows the measured domain to be excited with four independent sinusoidal signals simultaneously, and the measurements are carried out by measuring eight channels simultaneously. The measurements can be performed with differential probes connected to the channels of the receiver board. The number of probes (8 by default) can be increased by the application of a multiplexer (up to 64 channels), and/or adding further receiving boards. In case of multiplexed inputs, the measurement time increases as well, depending on the extent of multiplexing.

Fig. 2 shows the block-scheme of the digital board, which contains an FPGA chip used for parallel signal processing, four DSP processors for the implementation of the digital filters and one ARM processor for additional calculations and communication with the personal computer. *Fig. 3* shows the realized instrument.

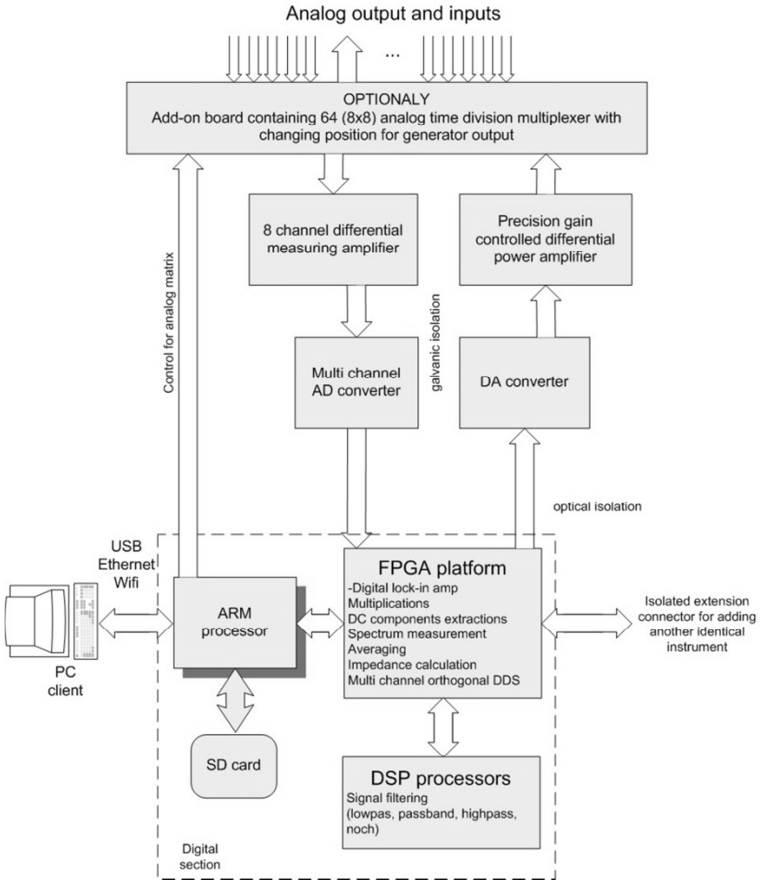

Fig. 2. Data processing part of the system

Fig. 3. The measuring instrument

The whole measurement procedure is conducted by PC software called Embedded System for Impedance Measurement (ESIM). The ESIM displays the results on the screen and it is capable of saving all measurement data either on Secure Digital (SD) card or Hard Disk Drive (HDD). The measurement system is capable of working without the PC as well.

3. Elementary test circuits and measurement procedures

The functions of the system were tested with elementary circuits, which consist of resistors and capacitors. Three test circuits have been constructed for perform the test measurements (see *Fig. 4*). In the circuits two different (R_{ref} = 1 kΩ and R_x = 10 kΩ) precise resistors were used as it can be seen in *Fig. 4a* and *Fig. 4b*. The resistor tolerance is 1% and the temperature coefficient is less than 2 ppm/°C [19]. For measurement of the parallel RC circuit (*Fig. 4c*) a capacitor (C_x = 100 nF with 5% tolerance) was added. The temperature coefficient of the capacitor was 200 ppm/°C [20].

By measuring the test circuits shown in figures *Fig. 4a* - *Fig. 4c*, it is possible to perform a statistical estimation of the accuracy of the system by calculating the average, the Relative Standard Deviation (RSD), the absolute and the relative error of the measured values. With current generator excitation (*Fig. 4a*) using a 1 kΩ reference resistor, it is possible to calculate the value of R_x resistor with the following equation (the I-V method): [21]

$$R_x = R_{ref} \cdot \frac{V_x}{V_{ref}} . \tag{1}$$

In order to test the advantages of the developed impedance measurement technique the test arrangement depicted on *Fig. 4b* was used (the same arrangement as in [21]). According to the patented method, the calculation of R_x is possible with the following formula:

$$R_x = R_{ref} \cdot \frac{V_x - V_{ref}}{V_{ref}} . \tag{2}$$

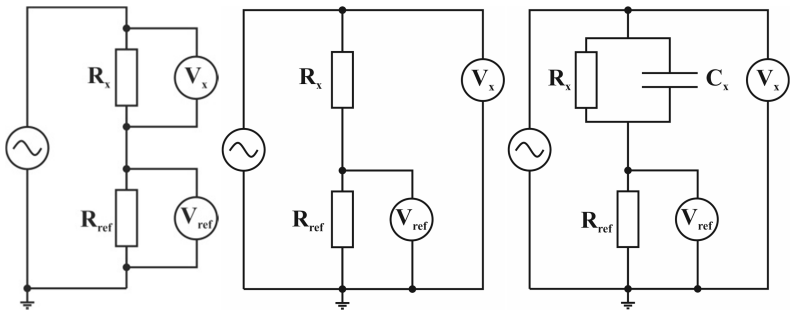

Fig. 4. Passive test circuits

By adding the capacitor C_x (*Fig. 4c*), the result of the calculation is the impedance (Z_x) of the parallel RC circuit. The impedance measurements (*Fig. 4a* - *Fig. 4c*) were performed with 159.16 Hz excitation frequency, which is the cut-off frequency of the RC-circuit. By selecting the cut-off frequency the effectiveness of the system can be verified: the measured impedance value have unique properties (phase value is -45°, the real and imaginary parts of impedance are equal etc.). The measurements had been carried out using lock-in averages lasting for 1, 5 or 10 seconds. Since the data acquisition lasted for one minute in each of the test measurements above, the statistics had been calculated from 60, 12 and 6 values respectively (see tables). EIS measurements were also performed with the circuit shown in *Fig. 4c*, at 100 distinct frequencies between 1 Hz and 10 kHz.

3.1. FFT spectrum measurement

With FFT spectrum measurement the device is able to record FFT spectra of two channels at the same time. The purpose of the FFT measurement is the verification of the effect of digital filtering applied. The measurement process applies digital filters at two stages:

- In the first step of the digital processing, where the input digitalized signal can be pre-filtered. This process is optional;
- Post-filtering corresponding to the lock in amplifier concept to eliminate the non-DC components. This filtering is always applied.

It is possible to choose among the built-in digital filters: Low Pass (LP), Band Pass (BP), High Pass (HP), Notch (N), and Band Stop (BS) (50Hz and 60 Hz) filters. If the FFT spectrum measurement is performed using a filter, the effect of the filtering will appear on the recorded spectrum.

3.2. Impedance measurement

This function enables to perform measurements either with two channels or at the same time with four different frequencies, or with eight (or maximum 64 optionally) channels with one frequency. In both cases, one channel is needed for current measurement besides the other voltage measuring channels.

3.3. Electrical impedance spectrum measurement

If the goal of the investigation is the frequency characterization of the electrical impedance measured on a material, the EIS measurement is the appropriate function. During this procedure, the device executes impedance measurements for a predefined number of generator frequencies between the lower and upper limit, defined by the user. When the lock-in amplifier is applied, the sinusoid product signals shall be integrated over an integer multiple of a whole period. The integer multiple of the period shall be equal to an integer multiple of the sampling time that is:

$$kT_p = nT_s\,, \tag{3}$$

where T_p is the period of the exciting sinusoid signal, while T_s is the sampling time, and k, n are integers. In order to perform an EIS measurement, the start and end frequencies as well as the resolution of the frequency interval shall be defined. The results are displayed in two Cartesian coordinate systems (usual Bode-plot).

4. Measurement results

These results demonstrate the capabilities of the entire equipment together with the ESIM and the embedded hardware. For the demonstration, measurements on the test circuit shown in *Fig. 4a* were performed. *Table I* summarizes the results of the measurement with statistical data for each channel.

Table I

Statistical measurements results related to *Fig. 4a*

Ch.	1 sec		5 sec		10 sec		e_Z (%)
	Z (Ω)	RSD (ppm)	Z (Ω)	RSD (ppm)	Z (Ω)	RSD (ppm)	
1	10049.838	33.76	10049.982	5.11	10050.061	5.81	0.50
2	9953.927	5.56	9953.916	3.50	9953.889	5.04	0.46
3	10006.714	5.47	10006.744	3.43	10006.774	5.81	0.07
4	9996.216	11.97	9996.248	8.92	9996.048	2.50	0.04
5	10004.612	10.87	10004.782	11.36	10004.796	4.91	0.05
6	10015.942	8.70	10015.997	13.69	10015.959	0.97	0.16
7	10048.744	7.69	10048.789	3.42	10048.783	4.58	0.49
8	9996.511	6.96	9996.508	3.02	9996.486	1.03	0.04

The measurements were performed with 1 s, 5 s, 10 s averaging time as well. The duration of the measurement was 1 min in every test. Thus, the averages and RSD (ppm) values in 2nd, 4th, 6th columns of *Table I* were calculated from 60, 12 and 10 values. The error of impedance (Z) values consists of two components: the constant error of analogue measuring channels and the resistor tolerance. The last column contains the relative error of Z values (magnitude and phase respectively), which is calculated by the following formulae:

$$e_Z = 100 \cdot \frac{Z_i - Z}{Z}, \; e_\varphi = 100 \cdot \frac{\varphi_i - \varphi}{\varphi}, \tag{4}$$

where e_Z and e_φ are the relative errors (%), Z_i and φ_i are the measured values corresponding the i-th channel (i = 1,...,8), while Z is the magnitude and φ is the phase of impedance (theoretical value).

The maximum relative error of Z_i (0.5006%) is less than the resistor tolerance. As a consequence of the lock-in principle, by increasing the averaging time, the standard deviation of measured values decreases [22]. This tendency can be seen clearly in *Table I*. The maximum RSD values calculated in case of different averaging times are 33.76 ppm (1 s), 13.69 ppm (5 s) and 5.81 ppm (10 s). The phase values are less than 0.01°, so these values are neglected. The results of the measurements performed on the test arrangement shown in *Fig. 4b* are summarized in *Table II*, which shows the advantages of the selected measuring method.

Table II

Statistical measurements results related to *Fig. 4b*

Ch.	1 sec		5 sec		10 sec		e_Z (%)
	Z (Ω)	RSD (ppm)	Z (Ω)	RSD (ppm)	Z (Ω)	RSD (ppm)	
1	10047.439	4.85	10047.437	4.53	10047.440	2.32	0.48
2	9945.228	13.06	9945.940	4.16	9945.478	4.37	0.55
3	10004.541	10.91	10004.528	3.49	10004.541	4.01	0.05
4	9994.382	8.01	9994.328	3.19	9994.287	2.51	0.06
5	9999.670	6.74	9999.653	4.91	9999.697	2.50	0.01
6	10015.813	7.27	10015.792	3.65	10015.778	2.59	0.16
7	10049.204	5.33	10049.205	2.87	10049.148	2.81	0.50
8	9991.281	7.12	9991.314	3.60	9991.316	1.28	0.09

The calculation of Z_i values rejects some errors (common mode error and instability), which appear during the measurement process. This can be seen from the maximum RSD values: 13.01 ppm for 1 s, 4.91 ppm for 5 s and 4.37 ppm for 10 s. Compared to the test measurement shown in *Fig. 4a*, the actual RSD values are lower, which means that the patented measurement method leads to more stable measurement data. In this case, the maximal relative error is 0.55%, while for the phase it is less than 0.01°(neglected). Thus, the test measurement shown in *Fig. 4b* satisfies the expectations:

the RSD values are resulted by the temperature coefficient and the impedance values are in tolerance as well. For the verification of the phase measurement, the test circuit shown in *Fig. 4c* had been constructed. The measuring process is described in [21]. The measured values are shown in *Table III* and *Table IV*.

Table III

The results (magnitude) of statistical measurements performed on test arrangement shown in *Fig. 4c*

Ch.	1 sec		5 sec		10 sec		e_Z (%)
	Z (Ω)	RSD (ppm)	Z (Ω)	RSD (ppm)	Z (Ω)	RSD (ppm)	
1	7046.486	5.74	7046.239	2.13	7046.191	2.49	0.35
2	6974.169	5.72	6974.187	3.17	6974.202	2.63	1.37
3	7017.069	4.90	7017.244	3.35	7017.247	2.39	0.76
4	7010.006	3.41	7009.996	2.86	7009.976	1.72	0.86
5	7013.605	5.32	7013.610	3.36	7013.606	0.87	0.81
6	7024.930	5.83	7024.928	2.82	7024.920	1.42	0.66
7	7048.301	3.06	7048.290	3.09	7048.308	3.19	0.32
8	7007.978	5.35	7007.912	2.76	7007.908	2.91	0.90

Table IV

The results (phase) of statistical measurements performed on test arrangement shown in *Fig. 4c*

Ch.	1 sec		5 sec		10 sec		e_φ (%)
	φ (◦)	RSD (ppm)	φ (◦)	RSD (ppm)	φ (◦)	RSD (ppm)	
1	-45.265	9.01	-45.258	2.76	-45.258	1.41	0.57
2	-45.295	4.83	-45.296	2.47	-45.296	1.71	0.66
3	-45.245	5.13	-45.247	3.88	-45.247	2.15	0.55
4	-45.262	4.99	-45.262	4.10	-45.261	1.77	0.58
5	-45.262	4.47	-45.262	3.65	-45.262	0.58	0.58
6	-45.262	4.99	-45.262	4.10	-45.261	1.77	0.58
7	-45.244	5.00	-45.244	3.87	-45.244	1.54	0.54
8	-45.226	4.90	-45.226	3.23	-45.226	1.93	0.50

As the excitation frequency was 159.16 Hz, the corresponding magnitude of the theoretically calculated impedance is 7070.96 Ohm and the phase is -45.00°. Compared to the theoretical values, the maximum relative error of the measured impedance is 1.3683% for the magnitude and 0.6555% for the phase. The RSD values for magnitude and phase are 5.83 ppm (1 s), 3.36 ppm (5 s) and 3.19 ppm (10 s), while for phase 9.01 ppm (1 s), 4.10 ppm (5 s) and 2.15 ppm (10 s) respectively. The results of EIS measurement can be seen in *Fig. 5*.

The maximum relative error for the magnitude of the impedance (calculated for

the whole frequency domain of the measurement) is 1.37%. Regarding the measured phase values, the maximum relative error is 0.66%.

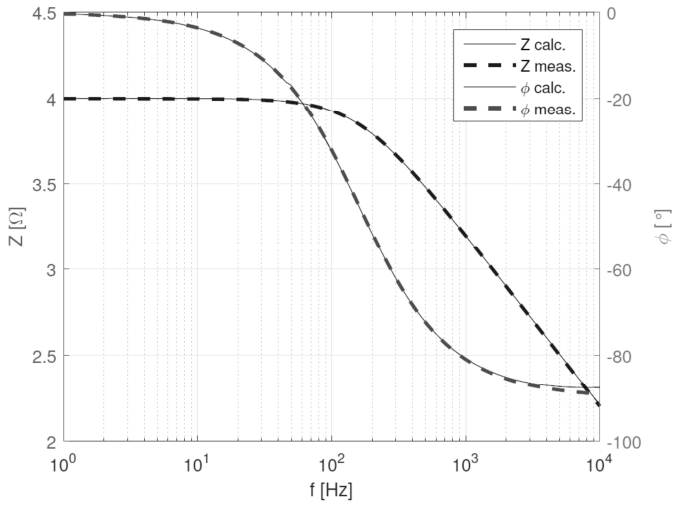

Fig. 5. Result of EIS measurement performed on test circuit (*Fig. 4c*)

5. Possible applications

The measurement system is developed mainly for medical diagnostics ([23]-[25]), but it is capable for performing nondestructive measurements in environmental engineering. [26]-[27] The aim of the research work in this specific field is to develop a measurement method, so-called multi-frequency Electrical Impedance Tomography [28], which is a non-destructive technique for investigation of materials (biological structures). The developed method takes advantages of the frequency dependence of measured material. Therefore, the first results were published in the field of spectroscopy [28]. Based on the measured data presented in [28], by using the developed measurement system, it is possible to gain outstanding statistics and high spatial resolution: at least 4%.

6. Conclusion

This paper presents a complex measurement system for EIT and EIS applications. For the control of this complex embedded system (hardware) a software (ESIM) had been developed. This equipment incorporates every necessary element of the proposed measurement method in order to investigate, display and gather the measured data in a suitable graphical form for further analysis. For this purpose test circuits to demonstrate

the tomography and spectroscopy capabilities and the statistical properties of the system have been constructed. The test results, performed on these circuits are able to prove the impressive accuracy and stability of this system. In all cases of test measurements, the measured error was less than the tolerance of built-in resistors and capacitors. The RSD-s, calculated from measured resistance values are resulted from temperature coefficients of the resistors and the capacitor.

The future goal of the research is to enable specific applications (especially in the field of tomography and spectroscopy) by using the features of this system, and develop more stable and precise measurement methods based on the lock-in principle.

Acknowledgements

The development was supported by grants GINOP-2.3.2.-15- 2016-00022, EFOP-3.6.1-16-2016-00004, GOP-1.3.1-09/A- 2009-0051, and Karotázs Ltd.

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