Techniques for Wideband All Digital Polar Transmission

by

Kevin Grout

A Dissertation Presented in Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy

Approved October 2019
Graduate Supervisory Committee:

Jennifer Kitchen, Chair
Bertan Bakkaloglu
Douglas Garrity
Waleed Khalil
James Aberle

ARIZONA STATE UNIVERSITY

December 2019

ABSTRACT

Modern Communication systems are progressively moving towards all-digital transmitters (ADTs) due to their high efficiency and potentially large frequency range. While significant work has been done on individual blocks within the ADT, there are few to no full systems designs at this point in time. The goal of this work is to provide a set of multiple novel block architectures which will allow for greater cohesion between the various ADT blocks. Furthermore, the design of these architectures are expected to focus on the practicalities of system design, such as regulatory compliance, which here to date has largely been neglected by the academic community. Amongst these techniques are a novel upconverted phase modulation, polyphase harmonic cancellation, and process voltage and temperature (PVT) invariant Delta Sigma phase interpolation. It will be shown in this work that the implementation of the aforementioned architectures allows ADTs to be designed with state of the art size, power, and accuracy levels, all while maintaining PVT insensitivity. Due to the significant performance enhancement over previously published works, this work presents the first feasible ADT architecture suitable for widespread commercial deployment.

DEDICATION

Theologus esse volebam: diu angebar: Deus ecce mea opera etiam in astronomia celebratur.

-Johannes Kepler

Soli Deo Gloria

TABLE OF CONTENTS

Page

LIST OF TABLES

LIST OF FIGURES

Figure Page

Figure Page

Figure Page

CHAPTER 1

INTRODUCTION

1.1. Motivation

RF front and back ends have traditionally always been very analog in nature, and have not benefitted from the aggressive scaling commonly seen in digital electronics. The traditional transmitter architecture can be seen in Fig. 1. However, in recent times, there has been a significant effort to move towards digital RF systems. These digital systems have the advantage of being inherently frequency agile, since digital electronics naturally function over a broad range of frequencies. Furthermore, they are easily scaled to new device sizes, since scaling rules are well understood within digital processes. In addition to these benefits, digital transmitters have the advantage of being compatible with switch-mode power amplifiers (SMPAs), such as class D and class E. SMPAs are capable of generating the same high accuracy and high power waveforms of a standard linear power amplifier (PA), with significantly higher efficiency. This is because SMPAs contain no biasing circuits or quiescent current, and power is only dissipated in the charging and discharging during clock edges. [1] These amplifiers can theoretically achieve efficiencies up to 100%, though circuit non-idealities ultimately limit the upper bound of their efficiencies. Being as PAs are the highest power block in the transmit chain, and they often have efficiencies on the order of 10%, this signifies a significant power and cost savings to the transceiver hardware. [2] These reductions in area and cost are extremely significant, as both are limiting factors for mobile and wearable devices. In order to reap the benefits of these high efficiency, small form factor modulators, much

work has been spent in both academia and industry to implement modulators that are compatible with SMPAs.

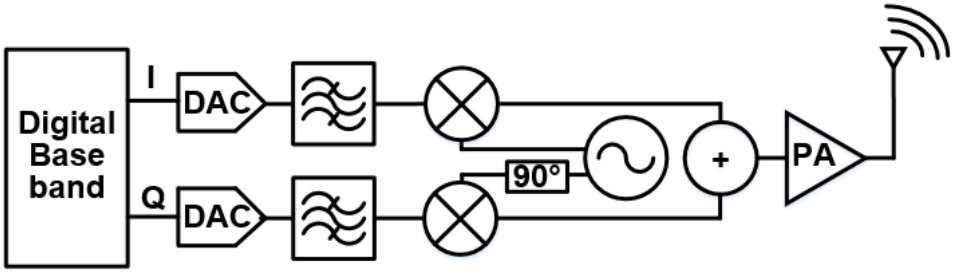


Figure 1. Traditional Analog Cartesian Transmitter Architecture

Several architectures of ADTs have been explored through the years. Unfortunately, the majority of these architectures are more correctly classified as "digitally-assisted" architectures rather than "all-digital" architectures. The most common of these digitally assisted architectures is the RF DAC implementation, as shown in Fig. 2. This architecture uses an array of RF DACs that are clocked with a digital LO waveform. This architecture has the advantage of allowing all signal processing to occur within the digital domain, and enables the usage of digital Delta Sigma noise shaping prior to upconversion. After the DAC, as lowpass or bandpass filter is inserted to reconstruct the desired waveform. Thus, everything downstream of the reconstruction filter is analog, and therefore requires a linear power amplifier. While this architecture boasts significant advantages, particularly noise shaping, it does not qualify as truly "all-digital" due to the analog power amplification. This architecture does not benefit from the efficiency enhancement associated with using a SMPA. It will be shown in Section 1.3 that these architectures tend to consume significantly more area and power than their all-digital counterparts.

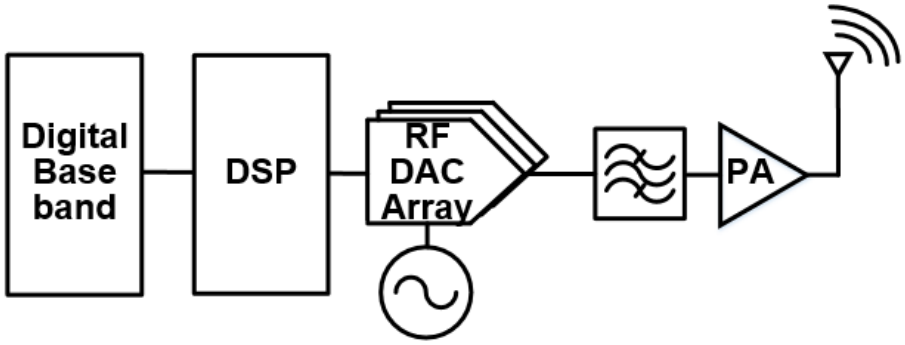


Figure 2. RF DAC Transmitter Architecture

The two possible configurations of a truly all digital transmitter architecture are shown in Figures 3 and 4. As all blocks in these architectures, including the power amplifier(s), are digital circuits, these architectures can rightfully be called “all-digital”. It can also be seen that this architecture can be done in either a Cartesian (Fig. 3) or a polar (Fig. 4) manner. The Cartesian method relies on generating the in-phase (I) and quadrature phase (Q) portions of the waveform separately. This requires two PAs to run in parallel and then be power combined. This method suffers from timing and amplitude mismatch between the PAs, which can potentially reduce the system accuracy. Furthermore, the addition of a second PA and power combining network introduces a large increase in the size and power consumption. As the PA is generally the largest and most power-consumptive block within the transmitter, this increase in area and power is expected to be higher than 100%.

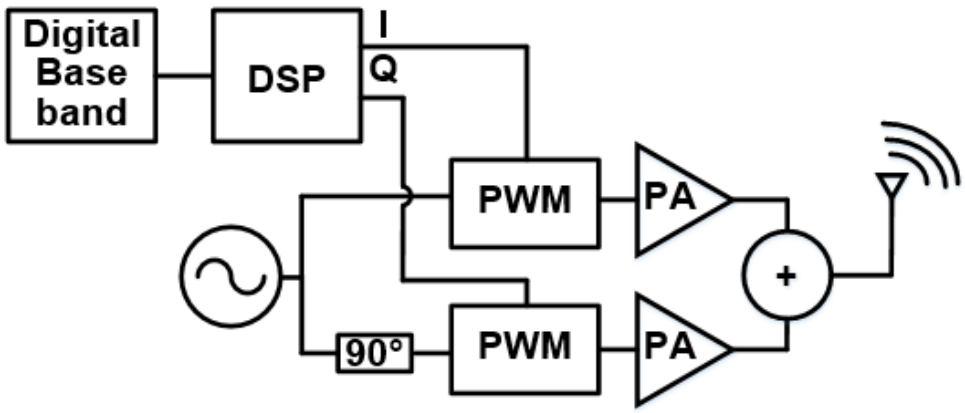


Figure 3. Cartesian Digital Transmitter Architecture

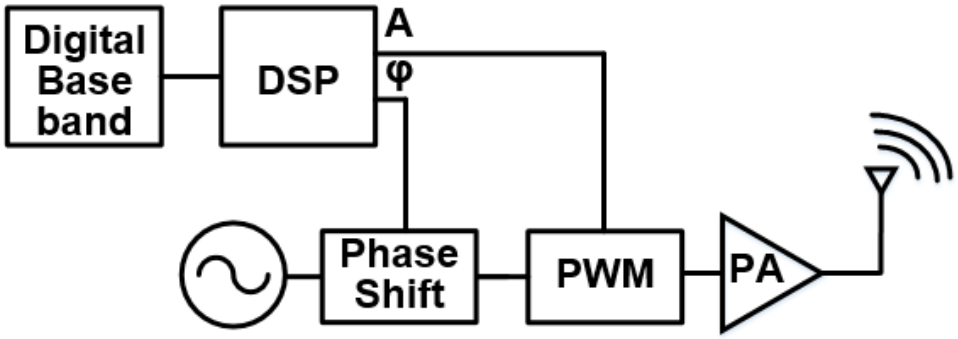


Figure 4. Polar Digital Transmitter Architecture

The alternative architecture is the polar ADT, shown in Fig. 4. This architecture processes both amplitude and phase on the same carrier waveform, thus making it possible to use a single SMPA without any power combining, thus saving significant area and power. Furthermore, since there is only a single path, there is no possibility for timing/amplitude mismatch errors. This architecture will be the focus of the remainder of this work.

1.2 Amplitude Modulation Techniques

There are several reasons why the all-digital architectures have not yet seen widespread adoption. These reasons range from issues with harmonic emissions to low

resolution levels. However, the largest issue has traditionally been amplitude modulation. Up until recently, SMPAs were considered incapable of transmitting traditional amplitude modulated signals. While the phase of these signals can be easily controlled, the input to these switch-mode PAs is digital, meaning amplitude variations do not affect the output, provided the variation is smaller than the switching threshold of the digital circuit. This quality makes switch-mode PAs very useful for communication standards such as GSM or other PSK/MSK based constellations, but also makes it virtually unusable for more complex constellations, such as WLAN's 64QAM that require transmission in both phase and amplitude information. [2]

Luckily, RF pulsewidth modulation (RFPWM) can provide amplitude modulation in these switch-mode amplifiers. By taking the Fourier transform of a rectangular pulse train, one can see that the amplitude, A, of the fundamental frequency is proportional to the sine of the duty cycle, w, as [3].

$$A = sin(w/2)$$

Therefore, by changing the duty cycle of the carrier waveform, the system can output different amplitudes through the switch-mode PA. This technique is known as RF PWM and the basic system implementation is shown in Fig. 5.

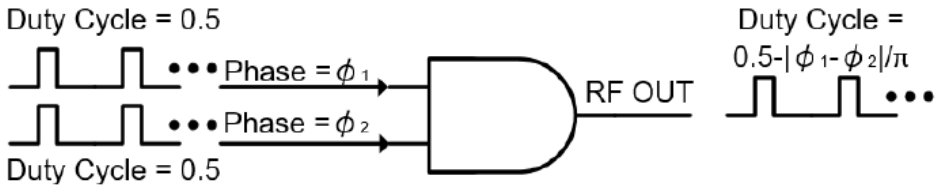


Figure 5. RFPWM Simplified System Diagram

There are other methods for generating amplitude modulation in switch-mode PAs, including baseband pulsewidth modulation (BB PWM) and envelope tracking. Brief descriptions of these methods are included below. BBPWM will be used indirectly in the Delta-Sigma phase interpolator work presented in Chapter 4. It is assumed that envelope modulation may be used in conjunction with the methods described in this work, particularly for pulse shaping and spectral compression, but these methods operate independently to the proposed methods and have been adequately explored in prior literature. As such, the basic operating theory will be introduced, but no in-depth discussion will be included in this work.

BBPWM functions in a similar manner to RFPWM. While RFPWM varies the pulsewidth of each individual carrier pulse, baseband varies the number of pulses that are transmitted for each symbol as shown in Fig. 6. This allows the duty cycle of each individual pulse to be fixed at 50%, which is ideal for some variations of switch-mode PAs. Furthermore, by not transmitting all the pulses for low amplitude signals, the coding efficiency, and consequently the power efficiency, of the system increases. [4] Unfortunately, this method comes with several disadvantages such as higher EVM and bandwidth limitations. A table of comparisons between RFPWM and BBPWM is provided below. Sizes are based on a chip taped out by the author containing both modulators with similar specifications on the same die.

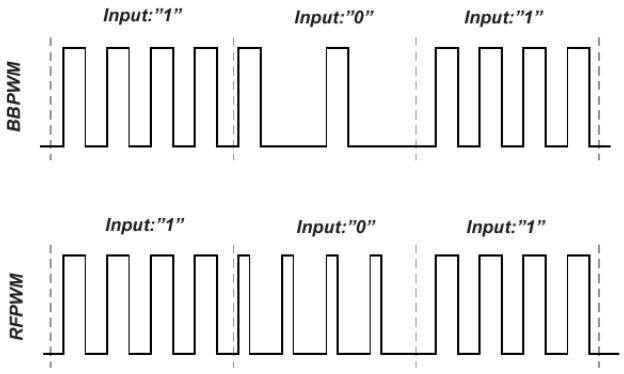


Figure 6. Comparison of RFPWM and BBPWM Waveforms

Parameter	RFPWM	BBPWM
Harmonics	even and odd	even only
Physical Size (mm^2)(1)	0.00002	0.009
Number of Amplitude Quantizations	low	high
EVM(2)	low	high
Coding Efficiency	low	high
Sensitivity to Mismatch	high	low
Subject to Pulse Swallowing	yes	no
Linear Amplitude Control	no	yes
Dynamic Range Limited by Bandwidth	no	yes
Phase Shifters Needed	2	1

(1) Excludes phase shifters.

Table 1. Comparison of Modulation Schemes

Unlike RFPWM and BBPWM, envelope tracking type amplitude modulation schemes do not rely on any form of pulsewidth modulation. Rather, it varies the supply voltage of the switch-mode power amplifier to provide a time varying amplitude variation. The main issue with this modulation scheme is that it requires high bandwidth analog supply modulators, which is a research topic in and of itself. Furthermore, the efficiency of the power amplifier becomes limited by the supply modulator, which can mitigate the added efficiency from using a switch-mode power amplifier. While this is

certainly an interesting and promising area of research, it falls more under the umbrella of power electronics (high speed switching converters and regulators) and will not be discussed further in this work.

It will be show in Chapter 4 of this work that RFPWM and BBPWM can actually be hybridized to generate a modulation scheme that has the benefits of both systems. Details on this methodology are provided in Section III.

The purpose of this work is to demonstrate novel RFPWM-based digital modulator systems that are capable of modern communications protocols without the need for intricate calibration. It is the expected that each presented design will yield at least one specification that is greater than any current state of the art publications under similar operation, without the associated calibration schemes used by previous authors. It is also expected that each of the presented architectures operate independently, and could theoretically be combined to achieve simultaneous improvement in multiple specifications.

1.3 Previous State of the Art

This section serves as a summary of the limitations of the previously published state of the art performances. A table of the summarized performance for each family of transmitter architecture is included. For each work, the number of PAs is defined as the number of single ended PAs would be needed to amplify the signal, though some of the works shown below do not include the amplifiers in their work.

	[5]	[6]	[7]	[8]

Architecture	BBPWM	BBPWM + DSM	BBPWM + DSM	BBPWM
Frequency (GHz)	0.94-2.4	0.65-1.95	1.95	0.9-2.4
Modulator Power (mW)	NR	120	NR	NR
Modulator Area (mm^2)	0.18	0.15	0.2	0.18
BW (MHz)	5	5	7	5
EVM (-dB)	26.7	29.3	31	25
# of PAs	4	2	1	8
OOB Emissions (-dBc)	8	44	0	16
Tech (nm)	65	90	90	65
Dynamic Range (dB)	10.4	8.1	3	10.3

Output Power (dBm)	NR	-16	20	21

Table 2. Summary of State of the Art BBPWM Transmitters

	[9]	[10]	[11]	[12]
Architecture	DSM RF DAC	DSM RF DAC	Interleaved RF DAC	RF DAC
Frequency (GHz)	1.49	1.5	0.9-3.1	0.35-1.65
Modulator Power (mW)	55	843	146	360
Modulator Area (mm^2)	0.18	1.26	0.21	1.16
BW (MHz)	50	100	57	100
SNR (dB)	54.5	56	33	NR
# of PAs	NA	NA	NA	NA
SFDR (-dBc)	58.5	65.5	-49	71

Tech (nm)	130 (SiGe)	130 (SiGe)	40	28
Dynamic Range (dB)	NR	NR	NR	NR
Output Power (dBm)	-13.8	-10.5	9.2	13.5

Table 3. Summary of State of the Art RF DAC Transmitters

	[13]	[14]	[15]	[16]	[17]	[18]
Architecture	Out-phased RFPWM	Multi-phase RFPWM	Multi-phase RFPWM	Carrier Switching	Multi-level RFPWM	Single Phase RFPWM
Frequency (GHz)	1.5-2.5	2.45	1.9	2-2.3	2.66	0.9-2.6
Modulator Power (mW)	NR	54.3	NR	98	70	50
Modulator Area (mm^2)	~0.7	0.13	NR	0.46	0.48	0.48

BW (MHz)	0.2	10	0	20	1.4	40
EVM (-dB)	26.7	30	NR	-25.5	-24.9	-29
# of PAs	4	32	18	2	2	1
OOB Emissions (-dBc)	NR	30	NR	30	NR	NR
Tech (nm)	65	45	40	130	65	40
Dynamic Range (dB)	6	NR	15	23	6.4	7.3
Output Power (dBm)	26.7	NR	31.5	25.6	22.4	NR

Table 4. Summary of State of the Art RFPWM Transmitters

It can be seen from the above tables that each family of modulators suffers from a common set of limitations. For instance, BBPWM generally is capable of high peak to average power (PAPR) and medium EVM transmission, but results in high amplitude spurs, images, and (sub) harmonics. It should be noted that the reported numbers are only for the close in OOB emissions, and it is expected that even larger spurs and images will be located outside of the reported frequency ranges, unless external filtering is applied. These conclusions match the assertions given in [19]

RF DAC based architectures also have clear limitations. It can be seen that these systems are capable of transmitting high bandwidths with extremely low spurs. Unfortunately this comes at the cost of large power and area consumptions. It should also be reiterated that these architectures require linear power amplifiers, and therefore do not qualify as all-digital amplifiers.

RF PWM can be seen to provide low EVM transmission with low spur levels, but is generally not capable of high PAPR transmission without combining large numbers of PAs. It should also be noted that those works that claim higher than average PAPR transmission are often reporting the PAPR of the modulator, but not the SMPA. This is somewhat deceptive, as it measures the dynamic range before pulse swallowing would have occurred. In reality, the achievable dynamic ranges of these modulators would be much lower if measured at the PA output. These conclusions also match the assertions shown in [19].

Though this work focuses solely on architectures for RFPWM based modulation, it will be shown that the presented architectures are capable of the accuracy of RFPWM and dynamic range of BBPWM, while maintaining state of the art values for size, power, spur levels, and frequency range.

The remainder of this work is formatted as follows. Section II. Describes a novel upconverted phase modulation process that is capable of generating polar-modulated waveforms over a very large reconfigurable bandwidth. Section III presents a power amplifier system capable of meeting harmonic emissions requirements over a large frequency range. Section IV describes a Phase Lock Loop (PLL) architecture that is capable of generating lower noise than the current state of the art for ring oscillator based

PLLs. Section V presents a novel method for increasing the phase resolution of polar modulators while maintaining PVT invariance. Section VI serves as a conclusion to the presented work.

CHAPTER 2

UPCONVERTED PHASE MODULATION

2.1. Background

Phase modulation for digital modulators is traditionally accomplished by cascading delay units and switching between the chain's intermediate nodes, as illustrated in Fig. 7 [5]. These delay units are often implemented using inverters, RC delays, or transmission lines. However, each of these delay units provide a constant time delay, rather than constant phase shift. Therefore, these time delays correspond to a varying percentage of the overall phase as frequency changes. For example, a transmission line may have a fixed propagation delay of 100ps, which corresponds to 1° at 35MHz, but only 36° at 1GHz. This inherently limits the frequency reconfiguration range. Some phase shifters have attempted to add frequency tunability by varying the inverter's supply voltage [8], by using current starved inverters [20], or by adding additional delay units and changing the number of delays units used as a function of frequency [18]. However, even with some level of tunability, these cascaded delays are typically not a sufficient solution for high frequency, high QAM communications because the delay units cannot achieve small enough time differences. Methods of artificially reducing the minimum time difference (interpolators) have been proposed, but these will be discussed in Chapter 4.

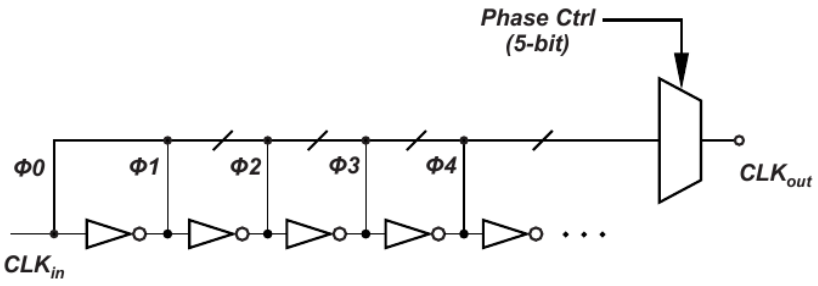


Figure 7. Tapped Delay Line Based Phase Modulation

Additionally, the propagation time of a given time delay block is generally directly (or exponentially) proportional to the physical size of the delay unit used. This causes unrealistic physical constraints on the size of low frequency shifters. This would imply that phase shifting should be done at as high of a frequency as possible.

However, extremely small time delay units tend to suffer the most extremely from phase noise, as well as PVT/mismatch variations. This is in addition to the fact that phase shifter resolution reduces at high frequency. This would imply that highly accurate phase shifting should be done at low frequencies, which is in direct contradiction to the assertions in the preceding paragraph. It can then be reasoned that a real system must operate in a state of compromise between the two. This “sweet spot” operates in a delay range where it is relatively immune to PVT/mismatch, but is not so large that the physical size become un-obtainable. Unfortunately, the frequency of the “sweet spot” is a function of the actual delay block used, not the system it is being integrated into. Therefore, it would be ideal if the phase shifting can always be done near the frequency at which the phase shifter is in its “sweet spot”, and then have this phase shifted output re-synthesized to match the correct carrier frequency. This must be done carefully, as frequency

synthesis has the potential to remove the imposed phase information from the carrier waveform. An example of such an information loss is included below:

Take for example, a quadrature phase shifter (i.e. potential phase outputs of 0°, 90°, 180°, and 270°). If one was to synthesize a new waveform at a frequency four times higher than the original, all four original phases wrap back into either 0° of 180°. For example, 90° multiplied up by two is 180°. A graphical explanation of this behavior is shown in Fig. 8.

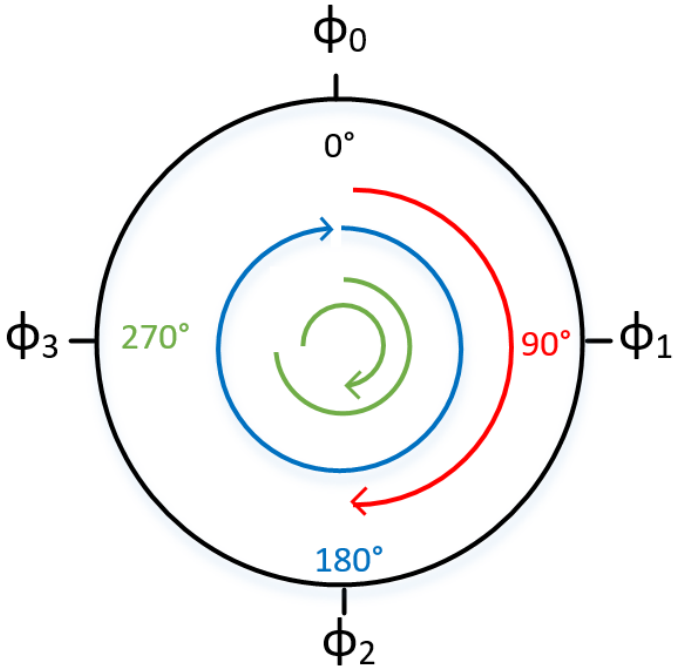


Figure 8. Graphical Demonstration of Loss of Phase Information During Frequency Upconversion

However, there are clearly cases where phase information is not necessarily lost. Take for example the same quadrature phase shift, but multiplied up by 3 instead of 2. This is shown graphically in Fig. 9. It can be seen that the phases are reordered, but the total number of (and identity) of unique phases is preserved. This is known as an

isomorphic, or mapping transform, and implies that no information is lost in the process. The reordering can be removed very simply by use of another isomorphic transform, namely a simple look-up table (LUT) at the input that contains the inverse of the reordering. It will be shown in the following section that the condition an isopmorphic frequency upconversion is that the number of quantizations, and the multiplication factor of the frequency upconversion circuit are relatively prime, that is, they share no prime factors.

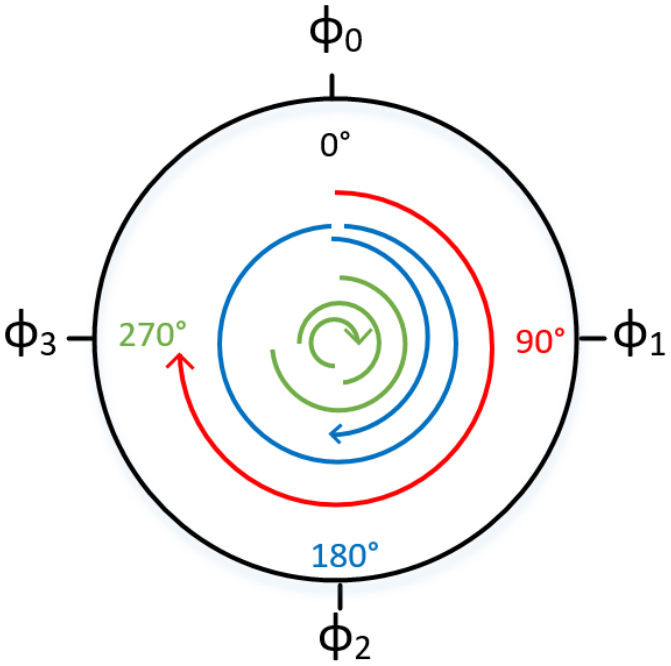


Figure 9. Graphical Demonstration of Lossless Frequency Upconversion

2.2. Theory

A simplified schematic of the proposed architecture is included in Fig. 10.

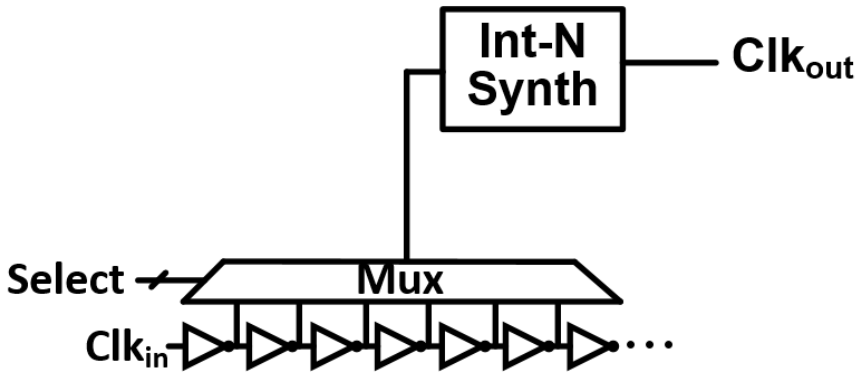


Figure 10. Conceptual 2-Step Phase Modulator

This system works by phase shifting a clock via delay locked loop, then running frequency synthesis with the shifter clock as the reference frequency. If this is done correctly, then the phase information from the low frequency clock will not be altered after frequency upconversion.

It was stated in the previous section that the phase mapping's isomorphic property during frequency synthesis is a function of the number of quantizations (k) and the multiplication factor (N). This section seeks to provide formal proof of this assertion.

Assuming that a phase shifter has k taps (or $\frac{k}{2}$ differential taps), the phase shifter's possible phases can be represented in degrees by

$$\phi_{in} = \left\{1 \cdot \frac{360}{k}, 2 \cdot \frac{360}{k}, \dots \ k \cdot \frac{360}{k}\right\}.$$

The quantizations can then be normalized to

$$\phi_{in} = \{1, 2, \dots \ k\},$$

where k is equivalent to 0° or 360°. If these taps are then multiplexed and fed to a second stage synthesizer, as shown in Fig. 10, then each phase will be multiplied by the synthesizer's integer divider ratio, N. This yields output phases

$$\phi_{out} = N \cdot \phi_{in} = \{N, 2N, \dots kN\}.$$

It is intuitive from this that, regardless of whether or not resolution is maintained, the elements in ϕ_{out} are uniformly spaced, where the space is equal to N. Furthermore, phase is cyclic with periodicity 360°, which is defined to be equal to k. Thus, the output phases are more appropriately written as

$$\phi_{out} = \{N \bmod k, 2N \bmod k, \dots kN \bmod k\},$$

where $kN \bmod k$ equals 0 by definition.

Since it has already been concluded that all output phase quantizations are equally spaced, then if any two adjacent quantizations share the same spacing as ϕ_{in}, then it follows that they must all have the same spacing as the original. If the output contains the same number of quantizations, and they are all spaced equally to the input phases, then the output must be an isomorphic transform.

It is known that one element of the list must be zero ($kN \bmod k$). This is intuitively pleasing, as zero appeared in the set of the original phases, and zero multiplied by anything should still be zero.

The spacing of the input phases was originally defined such that it was normalized to 1. Therefore, if 0 exists in the output phases, the frequency synthesis is isomorphic if and only if 1 also exists in the output phases.

For 1 to appear in the output phase list, there must be some input phase, α, such that

$$\alpha N \bmod k = 1.$$

For this condition to be true, αN must be one larger than an integer multiple of N. This unknown integer multiple can be referred to as β In this case,

$$\alpha N = \pm \beta k + 1.$$

By rearranging these terms, it is shown that

$$\alpha N + \beta k = 1,$$

where the minus is dropped from the β coefficient as a matter of notation. Without loss of generality, the sign of β can be flipped. This would simply represent a phase inversion at the output, but does not constitute a change in resolution.

The above equation is the definition of relatively prime numbers, which means their greatest common divisor is 1. Thus, it has been proven that the frequency synthesis is an isomorphic transform if and only if k and N are relatively prime to one another. If this condition is fulfilled, then the output phases will be equivalent to the input phases, albeit potentially reordered. This reordering process is purely deterministic, and can be undone by adjusting the routing definitions accordingly.

If the number of input phases and the multiplication factor are not relatively prime to one another, then 1 will not be present in the list of output phases. This means that the spacing is greater than 1, which implies a loss of phase resolution.

This proof can also be extended to the case where N is not constrained to be an integer. This represents the case where the second stage synthesizer is a fractional-N architecture instead of integer-N. In this case, each phase will be multiplied by some non-integer real number, $\frac{N}{M}$. However, this raises problems. For the system to be time invariant, then the following must be true:

$$N \cdot 0 = N \cdot 360 = \gamma N \cdot 0,$$

For any integer, γ. This should be intuitively pleasing, as it ensures that 0° always equals 0° regardless of when you define the start time. This can further be expressed as

$$\frac{N}{M} \cdot 0 = \frac{N}{M} \cdot 0 \; mod \; k = 0.$$

Furthermore, since 0°, 36°, and k are definitionally the same, this can be expressed as

$$\frac{kN}{M} = \frac{kN}{M} mod \; k = \left(\frac{N}{M} - floor\left(\frac{N}{m}\right)\right) \cdot k.$$

Since $\frac{N}{M}$ is definitionally not an integer,

$$\frac{N}{M} - floor\left(\frac{N}{m}\right) \neq 0$$

Which means

$$\left(\frac{N}{M} - floor\left(\frac{N}{m}\right)\right) \cdot k \neq 0$$

This implies the multiplication at 0° and at 360° does not yield identical values. This indicates that such a system is time variant. As such, it is clear that fractional-N synthesizers are not a suitable second stage synthesizer for generating steady state phase shifts.

The proof included in this section is fairly simple, and relies on some level of high level understanding of the circuit in question. A formal proof that does not rely on circuit specific assumptions is provided in Appendix B. However, the penalty for the lack of reliance on circuit specific assumptions is the proof must be done in a more general form, which requires an understanding of ring theory and abstract algebra.

2.3. Implementation

The overall system architecture of the designed system is shown in Fig. 11.

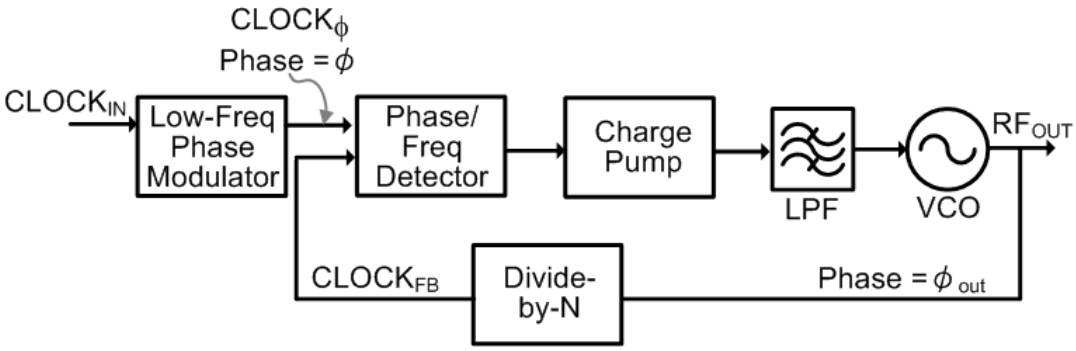


Figure 11. Two-Step Upconverted Phase Modulation Architecture

The low frequency phase modulation is accomplished via a wideband Delay Lock Loop (DLL) formed using current starved inverters. The DLL has each interior node tapped and sent to a multiplexer, making it a tapped delay line (TDL) This TDL is controlled by digital control word. The total number of stages in the DLL is also controlled via digital control word, which allows for a change in the number of phase quantizations in the DLL.

The output of this low frequency phase modulation is then input to the PFD of a second stage integer-N synthesizer. For the purpose of this work, the multiplication ratio, N, is fixed to 7. Since 7 is a prime number, any number of phase quantizations is a relative prime, so long as it is not an integer multiple of 7.

The PFD used in this work was a standard bang-bang PFD coupled to a single stack charge pump, as shown in Fig. 12. The charge pump was implemented via a reconfigurable RC filter.

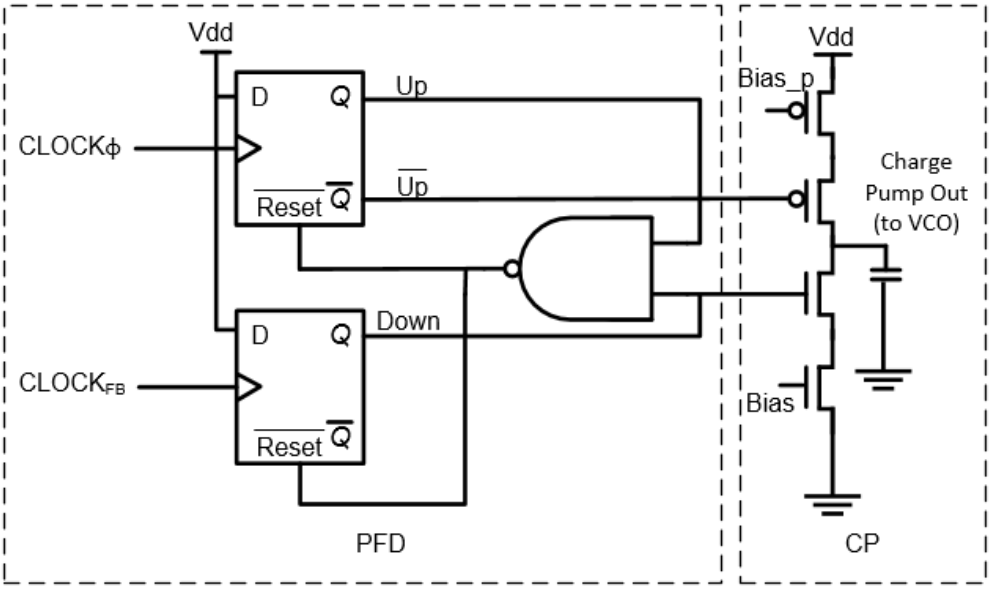


Figure 12. Simplified PFD/CP Schematic

2.4. Challenges

The implementation described in Section II of this chapter was taped out on a 2mm x 2mm die using a 45nm silicon on insulator (SOI) process. This process was provided by Global Foundries, and the fabrication was done through an intermediary, MOSIS of UCLA. There were significant problems regarding the manufacture of this circuit.

The first major roadblock in the manufacture of this chip was fabrication delays. Due to the cost, volume, and availability of circuit fabrication runs, the circuit was placed on a wafer alongside several other designs from other customers. As these other circuits are from other customers, the author is not provided with any level of knowledge or control over them. It was reported by MOSIS that at least one wafer run was destroyed due to experimental devices placed on the same wafer as our design. The subsequent re-

fabrication(s) took significant amount of time, and after all, the entire circuit fabrication was delayed by nearly a year.

After this delay, it was found by the author that the bondpads placed on the die were not connected. The origin of this problem is not nearly as cut and dry. The pads themselves were provided by a previous student, who had claimed that they were fully validated through multiple previous tapeouts. Unfortunately, the student had only verified the top metal connections, and had left lower level metals floating. This issue was allowed to propagate because the PDK provided by MOSIS (on behalf of Global Foundries) did not allow for the checking of designs containing the pads. Additionally, it appears that the foundry did not check the densities associated with the missing metals, which further allowed the problem to go unnoticed.

As only the top metal is connected to the pads, only the pads designated for high current are connected. This means the outputs, as well as rail voltages are connected, but none of the analog or digital inputs (including bias voltages) are connected. As such, the internal circuitry is running entirely open-loop, unbiased, and without configuration data. This was enough for very basic test of the on-chip drivers, but resulted in a complete inability to test or verify any of the internal modulation circuits. As such, no measurement results are presented at this time. Discussions are in progress with MOSIS attempting to receive a re-fabrication of the circuit that includes the missing pad connections, but this is a topic for future work, as the fabrication takes, at minimum, a few months to fabricate.

Luckily, the very basic level of test was enough to at least verify functionality of the high voltage silicon drivers. A re-design of these same drivers is used in the following Chapter in order to generate an extremely wideband reconfigurable power amplifier.

2.5. Simulation Results

Using the identities proven in the preceding sections, a conceptual system was designed in a 65nm process according to the same schematic as shown in Fig. 10. However, rather than fixing the divider ratio to 7, a variable divider was used. In conjunction with a 31 stage delay lock loop, the presented system is capable of generating upconverted phase modulation. However, since N is variable, the output frequency can be varied digitally. The DLL is sized so that it provides optimal phase shifting in the range of 20-50 MHz. For the purposes of measurement, 35 MHz is used, as it represents the center frequency of the DLL. Other frequencies could be used for the reference if needed.

This system utilizes a series of three VCOs multiplexed at their respective outputs. Each VCO is of the same current starved topology, as shown in Fig. 13, but the device sizes are scaled to allow each VCO to operate in a different frequency band.

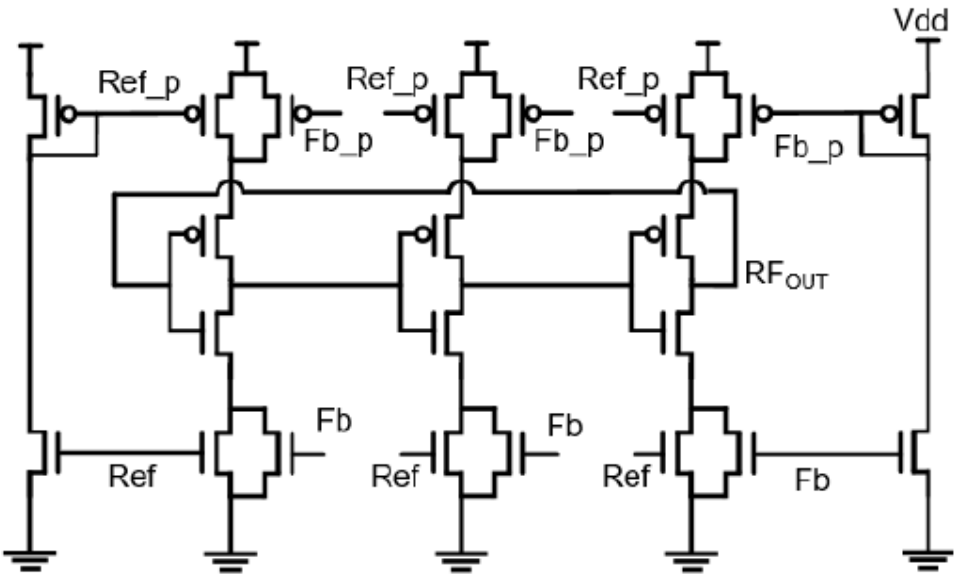


Figure 13: Simplified VCO Schematic

In this schematic, there are two control voltages for each current branch. The ref(p) current is controlled by externally applied biases, and sets the gross frequency tuning of the VCO. The FB(p) path represents the feedback from the PFD/CP, and is responsible for the fine tuning of the VCO's frequency. The overall frequency of this arrangement is approximately 0.6-2.7 GHz.

To show the system is capable of maintaining phase resolution over a large frequency range, the presented system is simulated using post-extracted models. The results are shown in Fig. 14. In Fig. 14a the upconverted phase output of each stage of the DLL is shown. As can be seen, the output phases are equally spaced, linear, and maintain 31 unique quantizations. Fig. 14b shows the resolution of the system for swept output frequency, which is controlled by changing the value of N. As can be seen, the system's phase resolution is maintained at 11.6 degrees (360/31) over the entire frequency range, except for 1.085 and 2.170 GHz. This is to be expected as these frequencies correspond

to 31 and 62 times the reference frequency. Since the DLL has 31 stages (k), 31 and 62 are the only values of N that are not relatively prime to 31 within the VCOs operating range. It is expected that designers would take these deadbands into account, as places these resolution nulls into unused bands. This can be done by specifically choosing the reference value to avoid transmitting at 31 or 62 times the reference frequency.

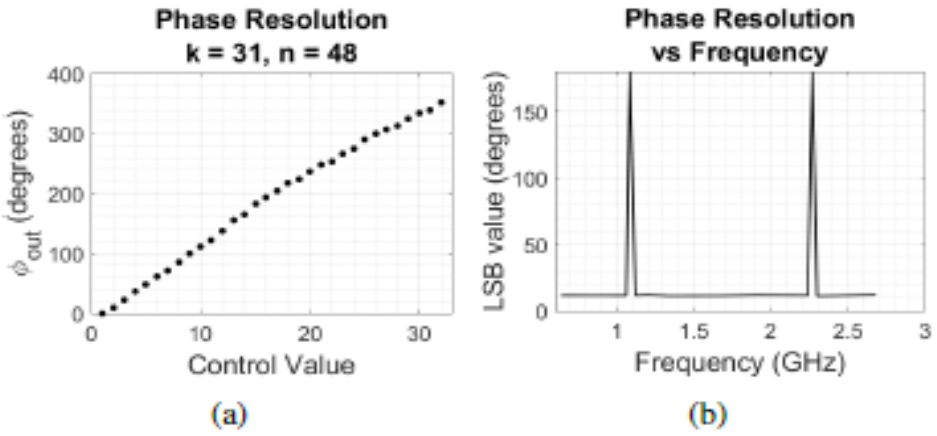


Figure 14. Simulated Output Phase Resolution

A table of the simulated performance is provided in Table 5.

	[7]	[4]	[8]	This Work[1]
Technology	40nm	40nm	32nm	65nm
Topology	Delay line	Delay line	Outphasing	PLL
Power (mW)	25-200	40-120	12[1]	<1[2]
Area (mm^2)	0.35	0.48	0.4	<0.01[2]
Frequency (GHz)	1-1.4	0.9-2.6[3]	2.4	0.64-2.7
Resolution (bits)	7-8[3]	7-8[3]	8	7

[1] Simulation only
[2] Power, Area do not account for the PLL, since synthesizer is assumed to already exist in system.
[3] Resolution only for minimum frequency. Resolution decreases as frequency increases

Table 5. Comparison to Prior Art

CHAPTER 3

POLYPHASE HARMONIC REJECTION AMPLIFIER

3.1. Background

Within the RF industry licensed frequency spectrum is frequently referred to as “the world’s most expensive real estate”. Companies and institutions pay exorbitant amounts of money to own exclusive rights to transmit within a particular range of the electromagnetic spectrum. As such, they are generally zealous in the protection of the spectral content within their bands. In order for this work to present a full system, it is important to establish a technique for ensuring harmonic emissions compliance. The following sections introduce a technique referred to as Polyphase Harmonic Cancellation which will be used to ensure the harmonic emissions compliance.

When a transmitter transmits spectral content is one band, it always has undesired spectral content that falls into other bands. This undesired emission can be in the form of noise, spurs, harmonics, etc. For a product to co-exist in the modern environment, it is important that these undesired emissions are mitigated to the extent possible. In that vein, many modern specifications have harmonic/spurious content limitations that must be met. These specifications can vary between loose or stringent depending on the application, frequency range, and geographic location.

Such specifications generally separate the undesired emissions into two distinct categories. The first of these categories is close-in out of band emissions (OOB). [21] As the name implies, this type of emission is related to how a given signal may corrupt other sub-bands/channels immediately adjacent to the transmitted signal. This type of undesired emission has been studied very thoroughly, and many solutions exist to

mitigate potential problems. Among these solutions are Digital Pre-Distortion (DPD) and pulse shaping. While this type of undesired emission is undoubtedly important, and a requirement for being able to transmit a given protocol, it is not the focus of this paper. It will be shown that the OOB requirements for GSM are met for the presented circuit.

The second form of undesired emissions is referred to as far out spurious emissions. This type of undesired emission refers to spectral contents that are separated from the desired carrier by a large frequency offset, usually greater than at least two channels. While the name may imply that these emissions are limited to spurs, the more common issue is with harmonics. While spurs are also capable of causing a given circuit to fail to meet its associated spurious emissions specifications, harmonics are the primary topic of this work. It can be shown that the methods presented later in this work are equally applicable to spurs. However, since spurs occur at arbitrary frequencies, it is very difficult to formulate the problem in general terms. As such, this work only discusses harmonics, and should they need to be extended to a spur, the mathematics may be adjusted to indicate a “harmonic” at the same frequency at which the spur occurs.

Harmonic emissions are caused by many physical mechanisms. In linear power amplifiers, gain compression, device nonlinearity, and clipping are the main contributors. These effects have been well studied for decades, and are fairly simple to mitigate. [2] The more problematic circuit topology is the switch-mode power amplifier (SMPA). Since SMPAs operate with squarewaves, their outputs (prior to filtering/termination) generally have harmonic content is according to the Fourier coefficients of the square wave. Furthermore, since there are potentially asymmetric pull-up versus pull-down

devices, single-ended SMPAs are liable to self-generate even order harmonics, even when transmitting a 50% duty cycle waveform.

While there have been many publications relating to the mitigation of OOB requirements [22,23], there has been surprisingly little work done towards the reduction of harmonic content. Generally SMPAs provide some level of harmonic termination or bandpass filtering, but this introduces a number of issues. The first and most obvious issue with using bandpass filters to reject the harmonics is the loss and area cost of the addition of passive components. Since the components used have finite quality factors, it is clear that these components will reduce the overall available power from a system. This effect is compounded when considering multi-band or reconfigurable circuits. For the circuits to be able to cover large frequency range(s), the passive terminations must be either wideband or reconfigurable. If it is wideband, then the Q must be significantly reduced per the Bode-Fano criterion [24]. This decrease in Q corresponds to increased power loss within the output network. Correspondingly, if the terminations are reconfigurable instead of wideband, there must be either switches or tuning elements (e.g. varactors) associated with passive elements. Switches inherently have series resistance, and therefore lower the effective Q of the passive element that it is associated with. While tunable elements do not necessarily have the series resistance associated with the switches, the physical manner in which they are implemented usually corresponds to a fairly lossy device[25]. Furthermore, wideband tuning elements rarely are capable of handling the powers associated with power amplifiers. [26]

There is yet another limitation on the bandwidth of an amplifier with harmonic terminations. If the circuit must short circuit the second harmonic, then it should be

intuitively obvious that the circuit will be unable to transmit at twice the frequency of its lowest carrier frequency, as it sees a short circuit load. This places a fundamental limitation of less than an octave of bandwidth for (single-ended) harmonically terminated PAs [29]. A similar restriction exists for differential PAs, but is limited to an octave and a half since they require no 2^{nd} harmonic termination due to their differential configuration. [30] This limitation could be fixed using reconfigurable or tunable harmonics, but they still exhibit the issues listed above.

The goal of this work is to demonstrate a harmonic rejection power amplifier that is capable of transmitting over a frequency range exceeding the octave and a half theoretical limitation without the use of any reconfigurable harmonic terminations. Rather, the harmonics will be cancelled using a polyphase technique. By virtue of not having these passive terminations, it is expected that the performance and power of the presented circuit will significantly increase.

3.2. Current State of the Art

There have been a variety of publications on the subject of harmonic rejection. Specifically within the area of switch cap PAs, most harmonic rejection is done using series resonances. These resonances are either done explicitly with lumped inductors and capacitors, or rely on the parasitics of the circuit's bondwires to provide the necessary reactance. For the purposes of the following discussion, both lumped and parasitic resonances will not be distinguished as they have identical issues.

First of all, series resonators are inherently narrowband. Unless the quality factor is significantly reduced, they are unable to have any significant frequency reconfiguration range. If the Q is reduced, power will be lost in the output network. Furthermore, the

reduction of Q is expected to result in reduced harmonic cancellation ability. Even if these issues were not present, the fundamental frequency limitation of an octave (described in Section I) is still present. This cannot be mitigated without the use of reconfigurable terminations, which tend to be associated with significant performance degradation.

Additionally, the series resonance operates on the assumption that the implied filter acts in an ideal manner over the entirety of its harmonic frequency range. However, parasitics within the filter cause each of the components to have a self-resonance frequency. These internal resonances will cause the filter to have multiple undesired modes of operation. As a single anecdote, the author has had significant issue with a 4^{th} order lowpass filter having near unity gain at approximately five times its corner frequency. For this reason, the blind assumption that a resonator or filter will prevent all harmonic emissions above its corner frequency is not viable. To fully comply with harmonic emissions standards, it is likely that many existing academic works would require significant additional filtering to deal with their higher order harmonics.

There have, however, been some works published describing more involved methods of suppressing the harmonics of switch-mode power amplifiers. One of the most effective techniques has been duty cycle calibration/control. In this method, the duty cycle of a square wave is carefully calibrated and/or monitored via closed loop control. [31,32] By controlling the duty cycle, it is theoretically possible to suppress even order harmonics. Unfortunately, this method does nothing for the odd order harmonics, and thus is not suitable as a sole solution. Furthermore, this method relies on the waveform having constant pulsewidth, which disallows the usage of BBPWM or RFPWM for

amplitude modulation. Unless supply modulation is used, there is no way to transmit a non-constant envelope waveform using this technique. Lastly, this method does not account for asymmetry in the amplifier which self-generates even order harmonics. As such, it is expected these self-generated tones will still potentially exceed harmonic emissions specifications.

Multilevel modulation has also been proposed as a means of suppressing harmonics [33]. Unfortunately, this does not function as a pure SMPA. As SMPAs rely on hard switching between VDD and GND, simple class SMPAs, such as class D's are unable to transmit such multilevel waveforms without significant modification or power combining networks. Furthermore, this technique does not scale well to high voltages, as the switches for high voltage silicon typically require multiple transistors in a cascode configuration. Since this technique does not scale to high voltage, it is not suitable for high power applications.

A similar method to multilevel modulation is the usage of harmonic rejection mixers [34, 35]. While this is not multilevel modulation in the strictest sense, the output of the mixers is still a multilevel waveform, which, like the multilevel modulation, is incompatible with traditional switch-mode power amplifiers. Additionally, it reintroduces analog mixers, which removes the benefit of the ADT's digital polar implementation (e.g. LO feedthrough, I/Q mismatch, etc).

Lastly, polyphase power combining has been proposed as a means of harmonic suppression [36]. This technique uses multiple power amplifiers in parallel running at offset phases and/or amplitudes. These offsets are carefully determined to cause their respective harmonics to cancel with each other during power combining. This is the

general technique that is used by the author, with the following differences from previously published works. While previous works relied on narrowband, fixed RC filters to partially cancel harmonics 2-4 by a fixed amount, this work presents a 7-fold wideband reconfigurable phase shifter capable of canceling arbitrary, potentially non-sequential harmonics. Furthermore, the presented system relies solely on phase modulation, and does not require each PA to run at a different amplitude. This prevents any issues with timing errors, reduces complexity, and allows each of the PAs to be running at its maximum power (and consequently maximum efficiency) at all times.

3.3. Theory

The presented technique uses switched capacitor power amplifiers (SCPAs) to generate the switching output signals. The underlying theory and analysis of SCPAs has been covered in depth by other authors [37-40], and will not be discussed in this work. However, a brief introduction to the conceptual operation is included below.

A simplified schematic illustrating a generic SCPAs operation is included in Fig. 15. The SCPA operates by switching the bottom plate of a capacitor between two or more levels. These levels are usually assumed to be VDD and ground, though other intermediate levels are possible. Whenever the switch toggles, a sharp edge occurs at the bottom plate, which capacitively couples onto the common node. The summation of all of these capacitive currents then flows through a reconstruction filter and into the desired load. The capacitors may also be sized in various fashions (binary, thermometer, C-2C, etc.) in order to create weighting coefficients. The presence of these weighting coefficients allow the circuit to generate multilevel waveforms to accomplish amplitude modulation. [41].

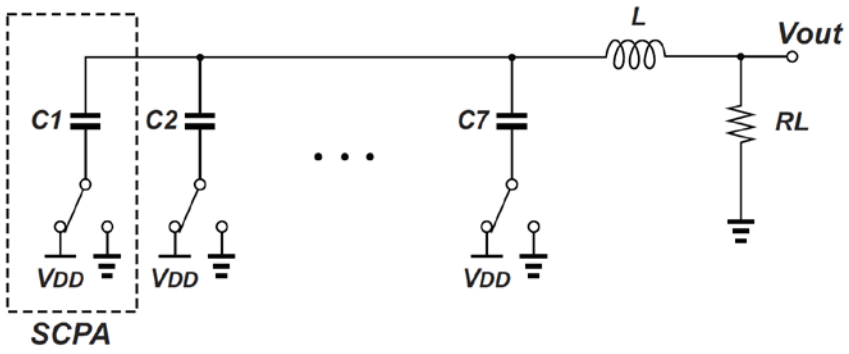


Figure 15. Generic SCPA Architecture

Unfortunately, the switching operation of such SCPAs is a non-linear function, and thus creates significant harmonics. As described in Section I, the goal of the presented technique is to avoid the use of passive harmonic terminations. Therefore, the harmonics that are generated by this switching action must be addressed using active techniques. Particularly, this work demonstrates cancellation via polyphase combining.

If two or more signals are combined via outphasing, it can be seen the total fundamental amplitude vector's angle is equal to the weighted average of the constituent vectors. However the harmonic amplitude's vectors are calculated using the phases multiplied by the corresponding harmonic number as shown in Fig. 16.

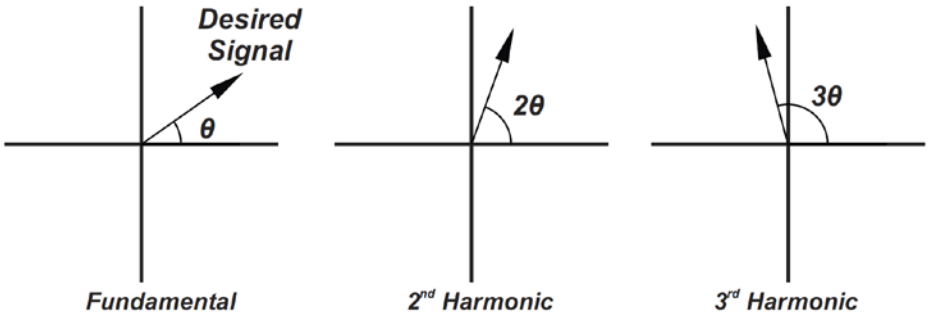


Figure 16. Graphical Demonstration of Harmonic Upconversion

As such, it is mathematically possible to construct a (solvable) system of equations that allows for the cancellation of a finite number of harmonics while maintaining non-zero amplitude for the fundamental frequency. An example of such a system of equations for 5 signals is listed below:

$$\begin{cases} \sum_{k=1}^{5} sin(1(w+\phi_k)) = 0 \\ \sum_{k=1}^{5} sin(2(w+\phi_k)) = 0 \\ \sum_{k=1}^{5} cos(2(w+\phi_k)) = 0 \\ \sum_{k=1}^{5} sin(3(w+\phi_k)) = 0 \\ \sum_{k=1}^{5} cos(3(w+\phi_k)) = 0 \end{cases}$$

It is shown in [36] that N signals is always capable of cancelling N/2 harmonics, or more if partial cancellation is allowable. However, in [36], the system of equations is solved by adding in scalar multiples to each phase, which in reality assumes an extra level of amplitude modulation – an unnecessary level of complexity for a power amplifier. This technique instead assumes all amplitudes must maintain a normalized amplitude of one, and does harmonic cancellation directly. A full derivation of the numerical methods used to find the exact phases for a given system is included in Appendix B. A graphic example of harmonic cancellation is provided in Fig. 17.

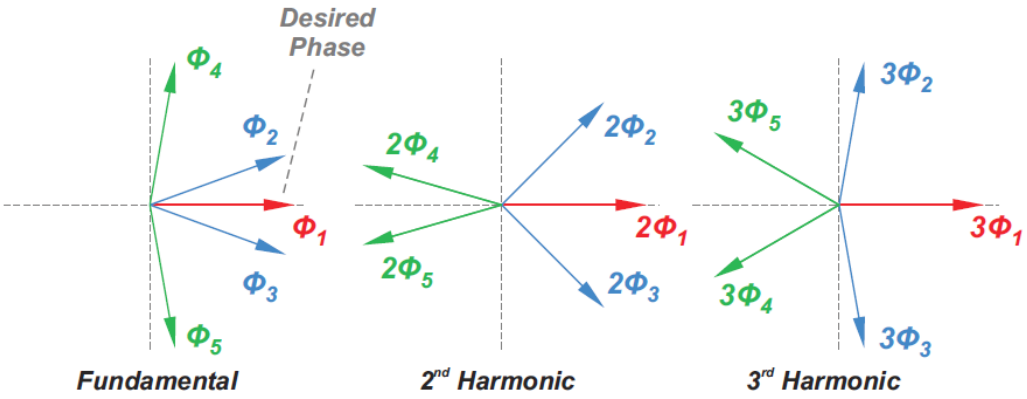


Figure 17. Graphical Example of Cancelling 2nd and 3rd Harmonic Using 5 Signals

The actual amount of harmonic cancellation possible using this method is primarily defined by the level of quantization error in the phase shifter. The full derivation of this quantization error is also included in Appendix B.

The total (ideal) efficiency of this system is defined by

$$\frac{P}{P_{max}} = \frac{1 + \sum_{k=2}^{N} cos(\phi_k))}{N}.$$

It can also be seen that higher number of outputs and higher order harmonics have a tendency to yield higher efficiencies. For example in the arrangement shown in Fig. 18, the efficiency degradation is only 0.9dB.

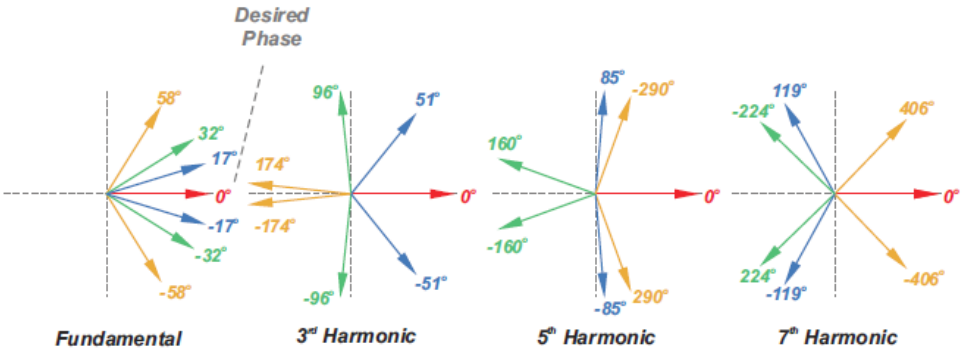


Figure 18. 7 Vector Cancellation of First 3 Odd Harmonics

3.4. Implementation

The overall on-chip circuit architecture is included in Fig. 19. Not shown is a SPI circuit used to load the configuration data and phase select bits.

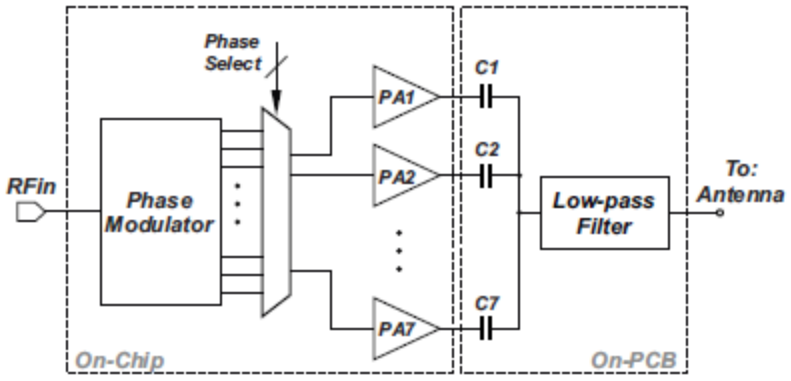


Figure 19. Simplified System Architecture

The phase modulator in this system is a traditional tapped delay line circuit as shown in Fig. 20.

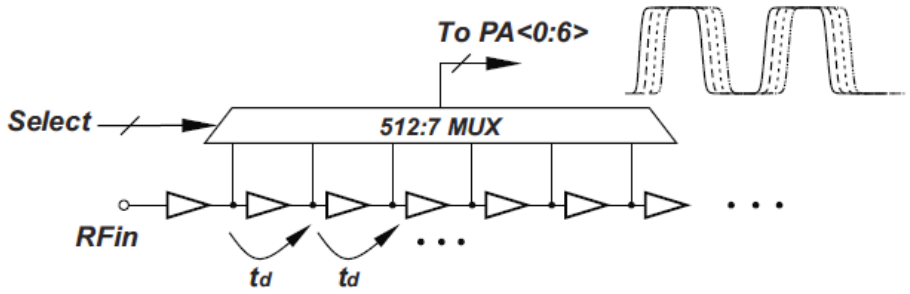


Figure 20. Simplified Tapped Delay Line Schematic

This circuit functions by inputting a known carrier reference and delaying it by a multitude (512 in this particular case) of identical series elements. As these elements have a non-zero propagation delay, each node corresponds to a monotonic increase in the time delay, which then directly translates to a correspondingly rotationally monotonic phase delay. These nodes are then tapped and buffered before being sent to a multiplexer which allows the various phase states to be selected from via digital control word.

The delay elements in a tapped delay line can be any arbitrary element so long as it possesses the qualities of having a forward path and a regular time or phase delay. For this particular design, inverter elements are used as they conform well to the switching waveform being used. They are sized at 9x the minimum size for the technology node being used, and each element has a fan-out of 1.33. These values correspond to a minimum delay of 7-13 ps, depending on the value of the supply voltage of the inverters. A 7ps delay corresponds to roughly a 3° quantization at 1.2GHz. This quantization will limit the maximum harmonic cancellation ability as described in section III. Because there are 256 differential delay elements in this design, frequencies down to approximately 250MHz can be achieved.

Because these delay elements are relatively small, it is expected that there will be significant levels of manufacturing variance, even with dummies and other matching techniques being used. This variance will alter the actual delay time to any particular node. However, since the elements are all in series, it is ensured that the delay is at least a monotonic function of the state. There is some level of non-monotonicity that can be attributed to the difference in the multiplexers, however this is expected to be small relative to the overall delay transfer function. The multiplexers themselves are standard cell IP from TSMC cascaded in order to form a 512:7 mux. Additionally, all routing has been deliberately matched so that the multiplexers are driven by identical input networks.

Since all elements in the phase modulator are series buffers, it is expected that the phase modulator itself will contribute minimal amounts of noise to the overall system. It is expected that the output noise will be defined jointly by the input's (signal generator) noise and the noise floor of the technology node's inverter.

Realistically, the output of a standard call mux is not sufficient to drive any real antenna. To amplify the signal up to useable power ranges, as driver is included as shown in Fig. 21. The overall architecture is a 3-stacked cascade, and is based upon the design presented in [4,42]. This amplifier is duplicated seven times on chip to allow for the cancellation of 3 harmonics. Since the 2nd, 3rd, and 4th harmonics are likely the strongest, it is assumed that these are the harmonics which will be cancelled.

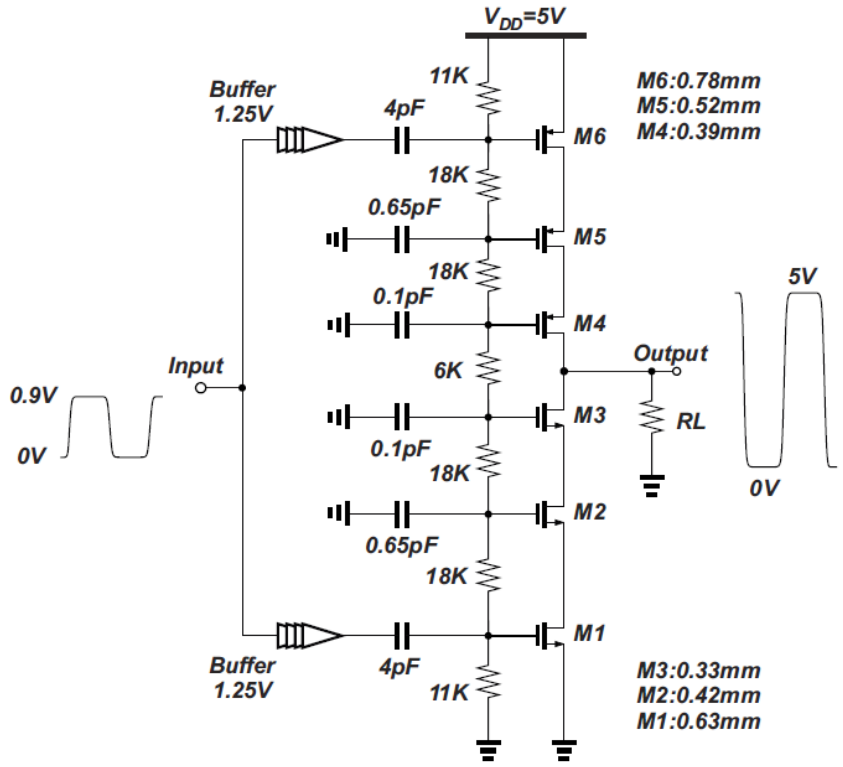


Figure 21. Power Amplifier Schematic

Since this PA uses long gate lengths, thick oxide devices, and 3-stacked transistors, it is capable of operating with rail voltages in excess of 5VDC plus inductive swings. Extensive simulations and physical tests have been completed to ensure the amplifier's ability to handle the high voltage levels.

The internal devices within the amplifier are sized in order to minimize the rise and fall time of the output. Rise/fall times between 50-300ps are observed, depending on operating conditions. Furthermore, two buffer stages are included in between the phase modulator and the amplifier in order to meet fan-out requirements, as well as to allow for an intermediate voltage level for ease of level shifting.

For the amplifier to function correctly, it is required that each branch's transistors switch at the same time. A simple RC level shifter is designed in order to create such an arrangement. In this type of level shifter, the DC bias of each transistor is set via resistive divider, while the capacitors allow the switching waveform to couple onto the gates, turning them on and off. [44] While this level shifter is technically a high pass filter, the component sizes are such that no de-biasing should occur at frequencies higher than 5MHz, which is an order of magnitude lower than the anticipated frequency range minimum.

As is explained in [4] the die is mounted directly to the PCB rather than being packaged. This is shown in Fig. 22. The package is omitted primarily due to concern over parasitics within the output network. The output network itself contains 3 aluminum bondwires with grounded downbonds interleaved in order to reduce inter-signal coupling.

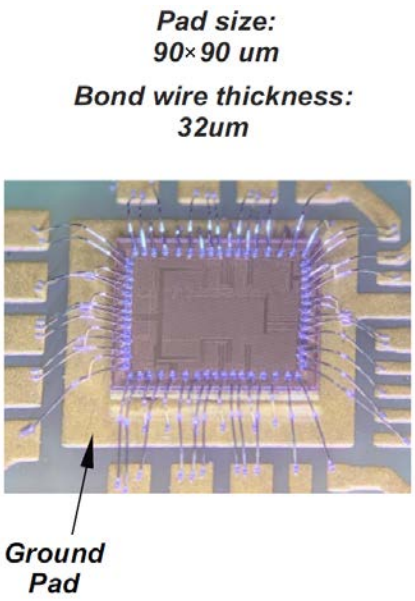


Figure 22. Unpackaged Die Photo

The overall frequency of the bonded amplifier is 50MHz-1.8GHz. However, there are issues with compression at high output powers near 1.2 GHz, and as such only the range of 50MHz-1.1GHz is used for measurements. As these drivers consume the majority of the power in the system, their efficiencies will be the largest factor in the overall system efficiency.

Each of the seven polyphase amplifiers is capacitively coupled to a common node as shown in Fig. 19. This common node is terminated by a 50 ohm load provided by the measurement equipment, with an intermediate transmission line provided by SMA cable. For the purposes of debug, the seven amplifiers' common nodes are actually broken into segments separated by 0 ohm jumpers, however, for measurement purposes they are all shorted together. These jumpers allow differing numbers of amplifiers to be combined during debug, such as testing just a single amplifier. The capacitors are all sized at 10pF, which is approximately the value that provides a resonance at the middle of the 300M-

1.1GHz range. However, as this is an extremely low Q resonance, its exact location is not particularly important. The board also includes a 4^{th} order Chebyshev lowpass filter realized using lumped component inductors and capacitors. This filter as a corner frequency of approximately 1.2GHz, which is motivated by the compression point of the amplifier running at maximum supply voltage. During low frequency operation, this filter is able to reject the high order harmonics, such at the 9^{th} harmonic, which are not cancelled using the polyphase technique. During high frequency operation, all harmonics fall outside the passband of the filter. As reduced harmonic cancellation is needed for high frequency operation, the circuit can then transmit more coherent waveforms, increasing the overall output power by reducing the outphasing constant. This helps mitigate the power compression that is seen at high frequencies. It is expected that in a full system, this filter would be omitted. Rather than an explicit filter, the antenna being used will have finite bandwidth and will provide higher order harmonic rejection inherently.

3.5. Results

The system described in the previous sections was implemented on a 45nm silicon on insulator process. A micrograph of this circuit is included in Fig. 23.

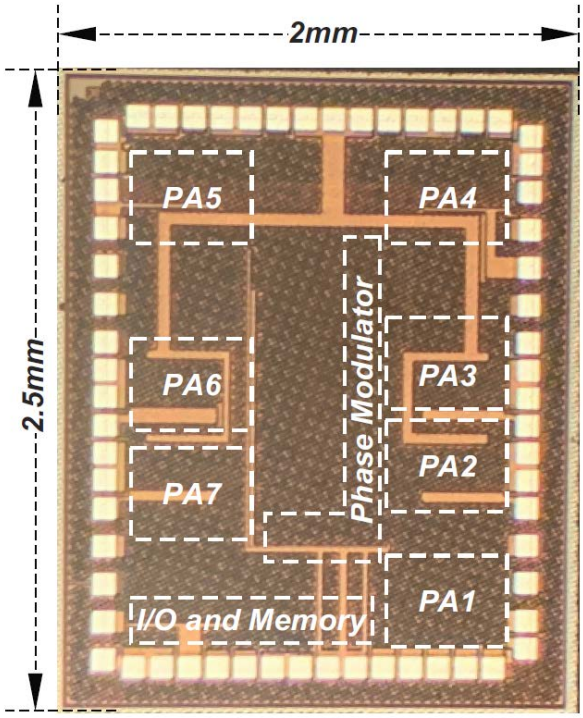


Figure 23. Die Micrograph

The chip dimensions are 2mm x 2.5mm with a total active area of approximately 0.67mm^2. All area that was not used for the core functionality was filled using high density decoupling capacitors in the attempt to mitigate supply droop/bounce caused by the parasitic inductance of the bondwires.

The circuit was tested using a custom PCB connected to a commercial FPGA evaluation board as shown in Fig. 24. The FPGA allowed the circuit to be (re)configured programmatically, and also contained the look up tables that mapped the harmonics to be cancelled to time delays for each frequency. Integrated into this look up table was also a generated inverse function intended to mitigate measured non-linearity within the phase shifter.

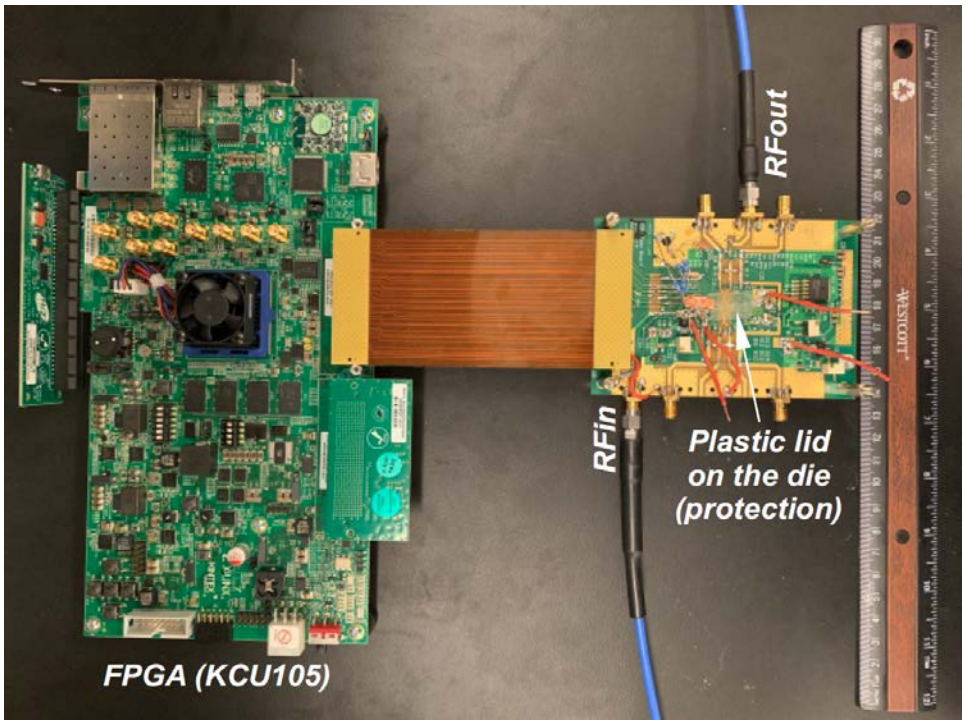


Figure 24. Board Level Test Setup (additional cabling omitted)

The phase-shifter's transfer function was measured using a high frequency oscilloscope. The results are included in Fig. 25. The nonlinearity characteristics were derived from this transfer function and are plotted in Fig. 26. As can be seen, the transfer function has significant non-linearity issues arising from manufacturing variance. It is expected that the DNL causes the effective ENOB of the phase shifter to be reduced, thus limiting the (RMS) harmonic cancellation ability. The INL, on the other hand, is easily fixed by use of an inverse function being superimposed onto the FPGA's lookup table values. Since this lookup table already is present, there is no additional overhead associated with the inclusion of the inverse function.

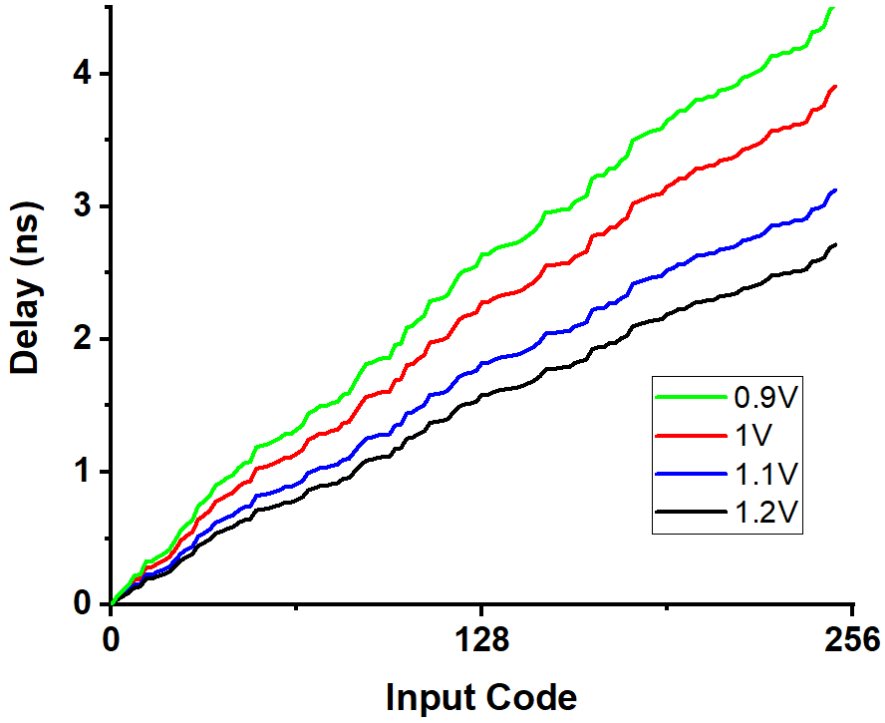


Figure 25. Measured Phase Shifter Transfer Function

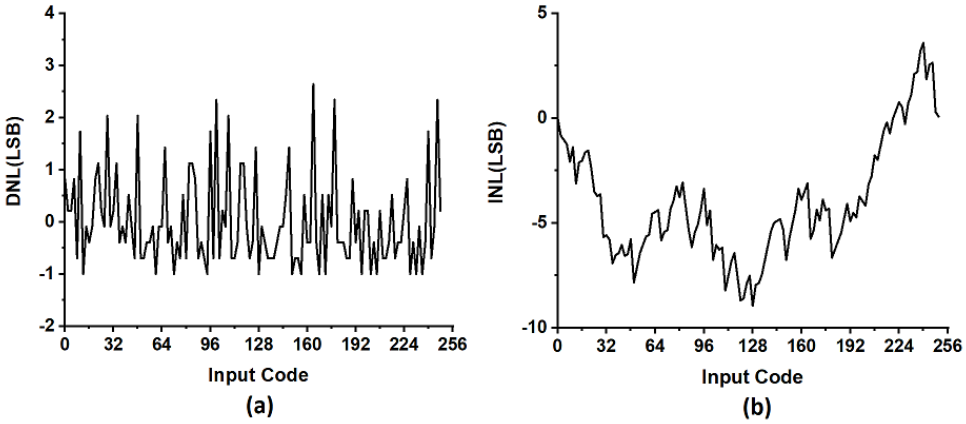


Figure 26. Derived Phase Shifter (a) Dynamic and (b) Integral Nonlinearities

The actual requirements for harmonic emissions are quite complex, and are a function of frequency, power level, application, and geographic location. For the sake of simplicity, all measurements refer to the baseline standard for a 3GPP category A home base station. When operating at max power, this specification dictates a maximum

harmonic level of -33dBc for all harmonics between 9kHz and 12.75GHz. The presented circuit's measured harmonic content for each carrier frequency is plotted in Fig. 27.

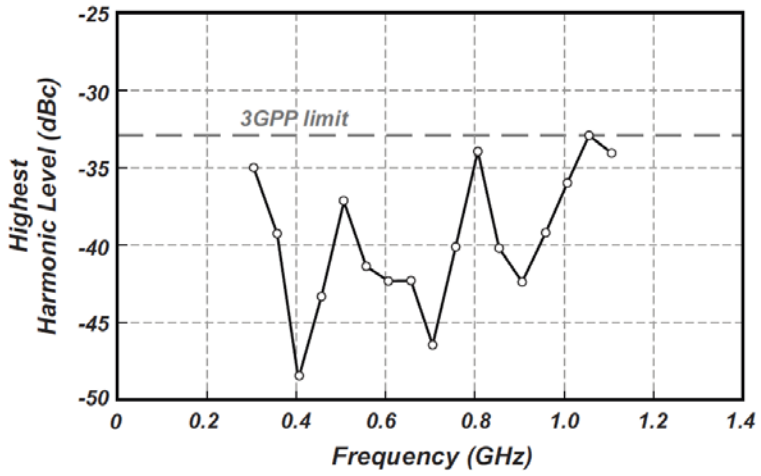


Figure 27. Highest Harmonic Levels

For the purposes of this measurement, all harmonics up to 6GHz are measured. While this does neglect any harmonic content between 6GHz-12.75GHz it is assumed that these harmonics are of extremely low value, due both to their relative harmonic number, and the filter at the output. It can be seen in this plot that the presented system is capable of staying within this limit over the entire range of 300MHz-1.1GHz. This upper limit of 1.1GHz was chosen to correspond to the compression point of the PA running at maximum supply voltage. The 300MHz is approximately $1/4^{th}$ of the upper frequency, which is to be expected, as the system is able to cancel 3 harmonics.

The PA was characterized and the resulting plots are included in Fig. 28 and 29. These plots correspond to the max Power versus frequency and efficiency versus frequency respectively. Since the actual output power of the full polyphase combined signal is a function of the outphasing coefficients, the presented plots are for each PA

driving separate loads. Similar plots are yielded by combining all signals coherently. During actual harmonic cancellation mode, the actual output power is generally within approximately 3dB of the coherent maximum.

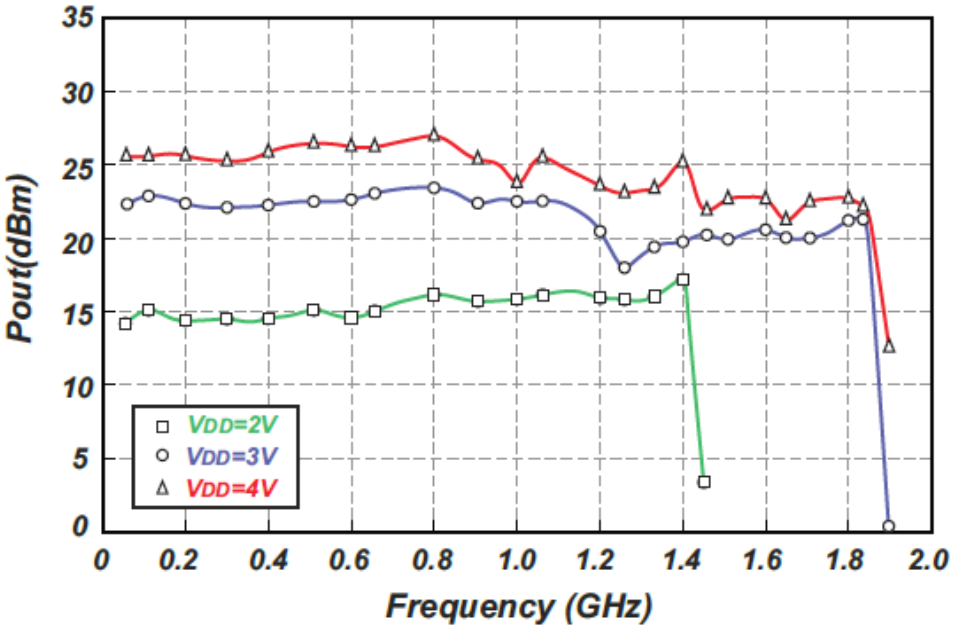


Figure 28. PA Max Power vs. Frequency

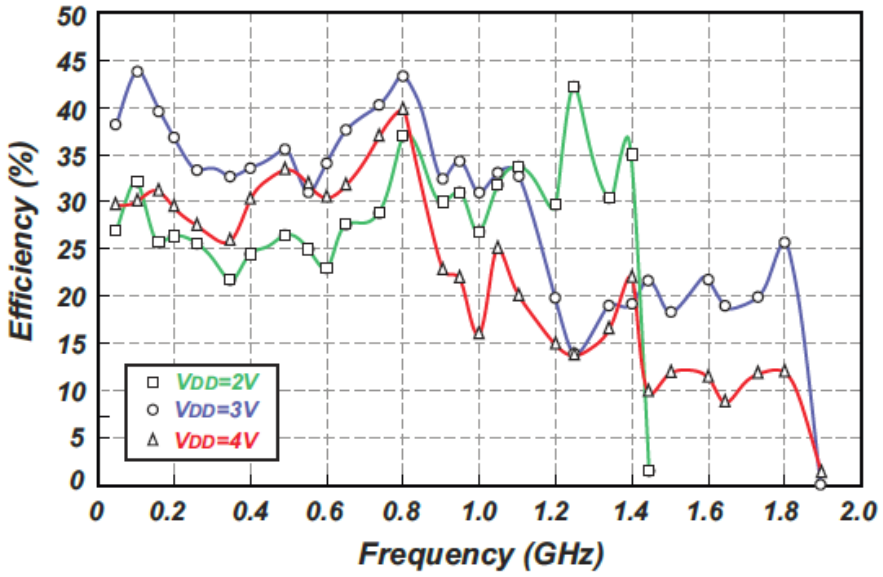


Figure 29. PA Efficiency vs. Frequency

To demonstrate this system's compliance with OOB specifications, the system was tested using a 200kHz GSM waveform using a carrier frequency of 900MHz. GSM is used in this context, since no amplitude modulation circuits exist on this particular design, despite the fact that the presented harmonic cancellation technique extends to amplitude modulation as well as phase modulation. The resulting spectrum is shown in Fig. 30. with the GSM spectral mask superimposed. It can be seen that the system fully meets the GSM spectral mask requirements without the need for additional DPD or pulse shaping techniques. To further demonstrate the bandwidth capabilities of the system, a 1MHz GSM waveform is also used and plotted in Fig. 31. Since no actual spectral mask exists for such a waveform, a scaled version of the standard GSM mask is used. However, regardless of the particular mask being used, it can be seen that the rolloff characteristics of the 1MHz spectrum is nearly identical to the 200kHz case, which indicated that there is no significant spectral spreading issues. It is suspected that this system is capable of transmitting bandwidths in significant excess of 1MHz, however the measurements are fundamentally limited by the available test equipment, and therefore spectrums corresponding to bandwidth over 1MHz cannot be included. Furthermore, the same 200kHz waveform was swept over the full 300MHz-1.1GHz carrier frequency range, and the mask was able to be met over all the entire range. For the sake of brevity, these additional spectral masks are not included.

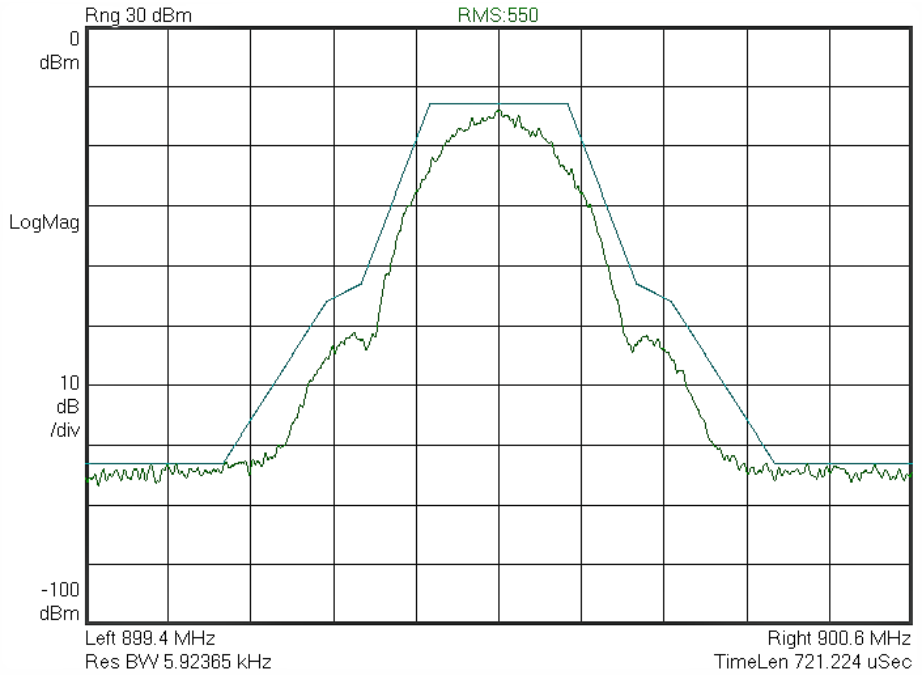


Figure 30. 900MHz , 200kHz BW GSM Spectrum

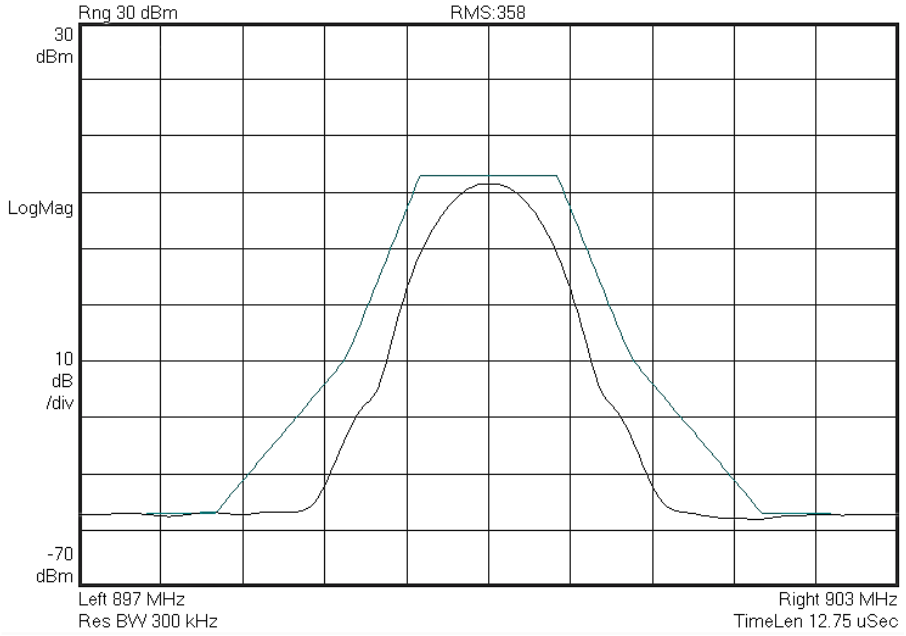


Figure 31. 900MHz , 1MHz BW GSM Spectrum (spectral mask adjusted to accommodate 1MHz BW)

The 900MHz output of this system was demodulated and a constellation diagram was generated, and is included in Fig. 32. It can be seen in this figure that there are secondary points adjacent to each desired constellation point. These are actually artifacts due to the signal generator used as a frequency reference. These same constellation errors exist even when the presented circuit is removed and the signal generator is directly connected to the vector signal analyzer. As such, their contribution to the overall EVM is neglected, as they do not correspond to meaningful data.

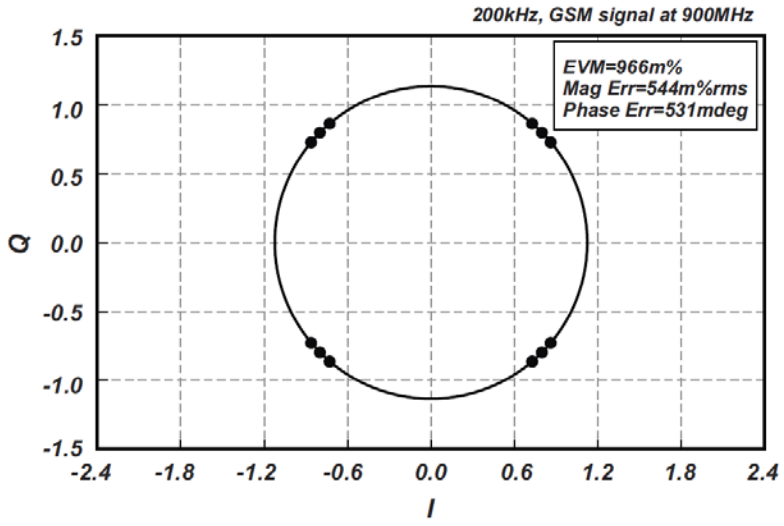


Figure 32. Measured Constellation from 900MHz, 200kHz BW GSM

It can be seen from this figure that the overall EVM of this particular case is approximately 1%, which is easily within the EVM requirements of GSM. This value represents the lowest EVM of any published harmonic rejection switch-mode power amplifier. Furthermore, the EVM was measured for a variety of other carrier frequencies using the same 200kHz bandwidth. The resulting EVMs at each carrier frequency are plotted in Fig. 33. As can be seen, the EVM remains roughly the same over the entire

operating range, with the exception of a slight increase above 1GHz, which is caused by the circuit compression. However, even with this increase, the system still demonstrates EVMs significantly lower than the GSM specifications.

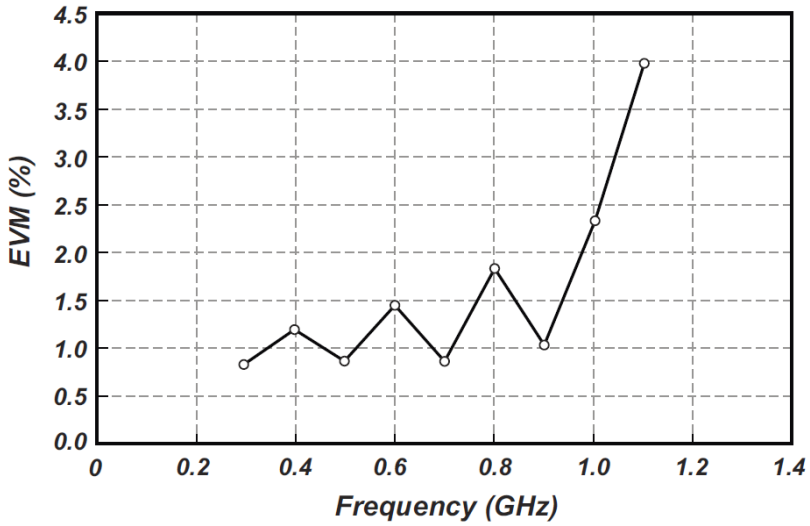


Figure 33. Measured EVM vs. Carrier Frequency

Lastly, Table 6 summarized the characteristics of this system compared to prior art. It can be clearly seen from the table that the presented system demonstrates best in class EVM, power, and frequency reconfigurability. It should be noted that this table includes only previous works on the topic of harmonic rejection switch-mode power amplifiers, and not generic SMPAs or SCPAs. While some of these generic PA papers may represent higher powers than are shown in this work, they are not a fair comparison due to their lack of bandwidth and/or harmonic cancellation.

COMPARISON TO PRIOR WORK

	[14]	[17]	[18]	[19]	[15]	This Work
Technology	40nm	90nm	40nm	40	65nm	45nm
Topology	Polyphase SMPA	Multilevel and Transformer	Duty-correction	Duty-correction	Staggered LOs	Polyphase SMPA
Supply Voltage (V)	1.1	1.2	1	1 / 3	1.2 / 2.4	1 / 4
Max Power (dBm)	8.9	5.3	1.2	0	25.6	27
Active Area (mm*)	0.13	0.2*	0.3*	1.1	3.6	0.67
Frequency (MHz)	850-1200+	906-924	2400	2400	700-1600	300-1100
Highest Harmonic (dBc)	-30+	-37	-50†	-46†	-57□	-40◇
EVM (%)	Not Reported	2.5	5.2	Not Reported	4.9	1
Peak Drain Efficiency (%)	43	62	39	9‡	20‡	43
IBW (MHz)	0.1	1	1	Not Reported	20	1

(+)Estimated from graph
(*)Estimated from micrograph
(◇)Average across entire frequency range
(‡)System efficiency
(†)HD2 only. No higher order cancellation
(□)HD3 only. No higher order cancellation

Table 6 – Comparison to Prior Art.

3.6. Conclusion

Overall, the conclusion of this chapter is to show that the presented technique of polyphase harmonic cancellation is a viable solution to the problem of harmonic emissions, as well as a remedy to the theoretical frequency limitations caused by the addition of harmonic terminations. It is shown that high power, high performance, and reconfigurable transmission can be generated through the use of this method. However, this method only allows for the cancellation of already modulated signals. To create a fully functional and complete transmission chain, work also must be done towards high precision modulation, which is the subject of the following chapter.

CHAPTER 4

SAMPLED LOWPASS DIVIDERLESS PLL

4.1. Background

For digital transmitters to be a feasible option for modern communication schemes, it must be able to meet the EVM requirements of the standards in question. This has traditionally been one of the issues preventing mainstream use of these circuit topologies, as digital transmitters have a reputation of relatively high EVM values. This is due to two factors – random noise and fixed distortion. Random noise represents time varying, and typically Gaussian noise distributions caused by imperfections in the transmitting circuits. Fixed distortion is caused by the inability of the transmitter to generate the desired waveform due to quantization or dynamic range limitations. This Chapter seeks to present methods of generating signals with extremely low random noise, with no regard for the fixed distortion. Mitigation of distortion and quantization noise will be covered in Chapter V.

As discussed in Chapter 1, RFPWM systems require polyphase digital outputs to accomplish pulsewidth modulation. This makes ring oscillators the natural choice for oscillator topologies. Alternatively a tuned oscillator could be used, but then a secondary digital phase shifter would be needed downstream of the oscillator, which ultimately reduces to the noise performance to that of the phase shifter. As digital phase shifters are realized with similar topologies to ring oscillators, either situation reduces to effectively the same problem.

While ring oscillators are very useful for generating polyphaser outputs, they do not have good noise performance. Wide bandwidth ring oscillators typically have Qs of less than 10. Due to this extremely low Q, the overall noise of a ring oscillator PLL is significantly increased over a tuned oscillator based PLL. To generate low noise modulated waveforms, particular attention will need to be payed to the design of the digital modulator's frequency generation circuitry.

4.2. Current State of the Art

The current state of the art for low noise PLLs is the subsampling architecture. A graphical example of the subsampling PLL architecture is included in Figure 34.

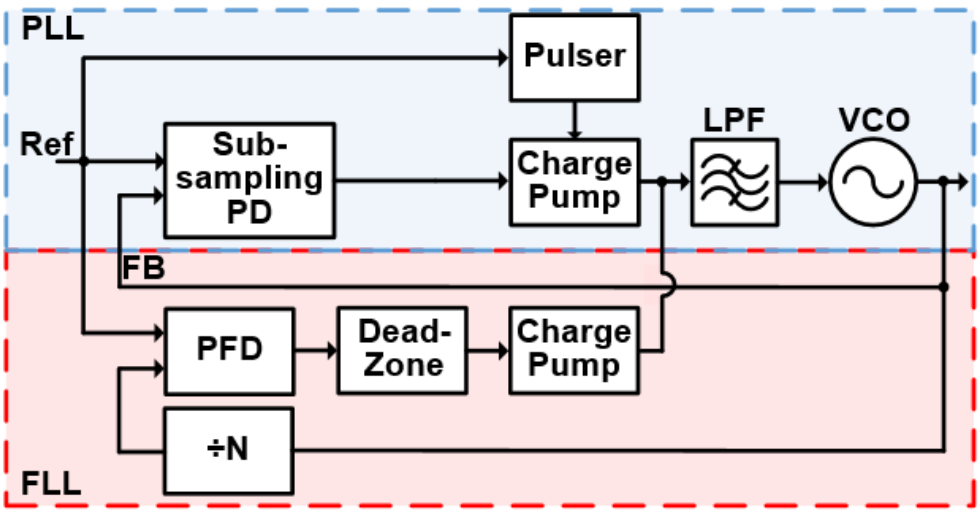


Figure 34. Simplified Subsampled PLL Architecture

In this architecture the VCO is fed to the input of the phase detector without going through a frequency divider. This phase detector functions by sampling the value of the

VCO output at the edges of the reference signal. Assuming the sampling and charge pump are entirely linear, then the overall transfer function of the PD/CP is simply

$$\beta_{PD/CP} = K_{CP} \sin(\Delta\phi).$$

Where K_{CP} is the gain of the charge pump. If the output phase is near the locked condition, then the small angle approximation can be used, resulting in

$$\beta_{PD/CP} = A_{VCO} \cdot K_{CP} \Delta\phi,$$

Where A_{VCO} is the amplitude of the sampled signal. Because this transfer function's denominator does not contain any N terms, there is no PD/CP N^2 noise present in the PLL. However, this advantage comes at the cost of several stipulations. First of all, the above transfer function is only valid when the phase is already at/near the locked location. Thus, subsampling PLLs generally require an auxiliary loop to provide the initial lock. These axillary circuits do not need to be designed for particularly low noise or low noise operation, since they can be disabled after the initial lock. However, their addition necessarily yields higher complexity and area consumption.

Furthermore, the subsampling architecture requires the output of the VCO to be sinusoidal (or triangular). This is because the VCO output amplitude must be sampled by the reference signal. If the output is a square wave with negligibly fast rise/fall times, there are only two amplitudes that could be sampled by the phase detector. This case reduces to a one-bit quantization, which yields significantly sub-par noise performance. Various techniques can be used to mitigate this issue, but in each case area consumption and circuit complexity are increased by their addition.

Another issue with the subsampling PLL is the design of the sampling block. Because the phase detector's sampling circuitry must be able to sample at high

frequencies, the design becomes significantly constrained. To maintain linearity, the area generally must be made quite large. Large holding capacitors to reduce noise require large areas. Large capacitors and devices require high VCO output drive strengths, which increases the power computation. Switching action in the sampler also yields pedestal and aperture errors at the input to the charge pump.

Yet another issue associated with the subsampling architecture is the charge pump. Because the phase detector is sampling the amplitude of the VCO output, the charge pump must be able to provide a range of analog currents. The requirement of a continuous range of current outputs adds significant complexity to the charge pump, and generally makes the linearity difficult to maintain.

It is clear from the above issues that the subsampling architecture has significant tradeoffs associated with the use of the sampling block. Thus, it would be advantageous if one could provide frequency synthesis with subsampling noise performance without the need for an explicit sampling block in the phase detector. The following sections of this chapter seek to introduce a novel PLL architecture that maintains subsampling noise performance without any explicit sampling block within the phase detector block.

A table of the current state of the art for ring oscillator based subsampling PLLs is included in Table 7.

	[7]	[8]	[9]	[10]	[11]	[12]	[13]
Technology	130nm	65nm	65nm	28nm	65nm	65nm	65nm
Topology	SSPLL	Active SSPLL	SSPLL w/ FeedForward	SSPLL	Switched Loop	Injection Lock	SSPLL
Oscillator Type	Multi-ring	Ring	Ring	Ring	SFT Ring	Ring	Ring
Supply Voltage (V)	1.3	1.2	0.94	1	1.2	1.1	1.2
Active Area (mm^2)	0.21	0.0049	0.022	0.023	0.08	0.06	0.008
Frequency (MHz)	800-1300	1100-2600	2000-2800	2.08-2.72	3000	0.96-1.44	2000-3200
Reference Spur (dBc)	-42*	-37	-55	-63	-71	-53	-64
Integrated Jitter (fs)	571	720	633	248	357	185	422
Integration Bandwidth	10k-100M	10k-100M	1k-100M	10k-100M	1k-80M	10k-40M	1k-100M
PN @ 1MHz (dBc)	-121.0	-114.4	-119.1	-125.4	-105.0	-113.5	-122.6
Power (mW)	19	4.59	5.86	4.1	4.6	9.5	6.1
FoM$^+$	-230.0	-236.2	-236.3	-246.0	-242.3	-244.9	-239.7

† All results specified for 2.0GHz * Fractional Spur $^+FoM = 10log_{10}(\frac{\sigma^2}{1s} \cdot \frac{P}{1mW})$

Table 7. State of the Art Ring Oscillator Based PLLs

4.3. Theory

A simplified schematic of the presented PLL architecture is included in Figure 35.

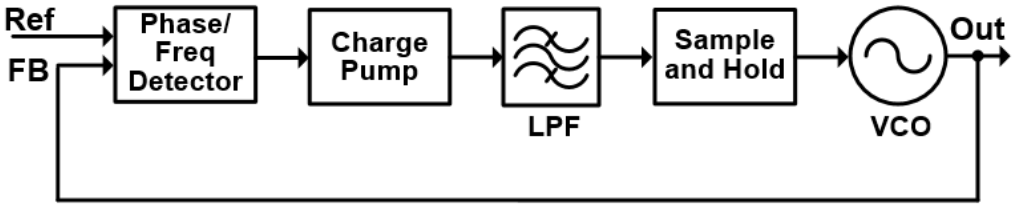


Figure. 35. Simplified PLL Architecture

As can be seen, the presented architecture looks very similar to a standard integer-N architecture with two main differences. First of all, there is no divider in the feedback loop. Secondly, there is a sample and hold placed after the lowpass filter in the feedforward loop. It should be noted that there is no sampler present in the phase detector or charge pump blocks.

A simplified schematic of the presented circuit's phase detector is included in Fig. 36.

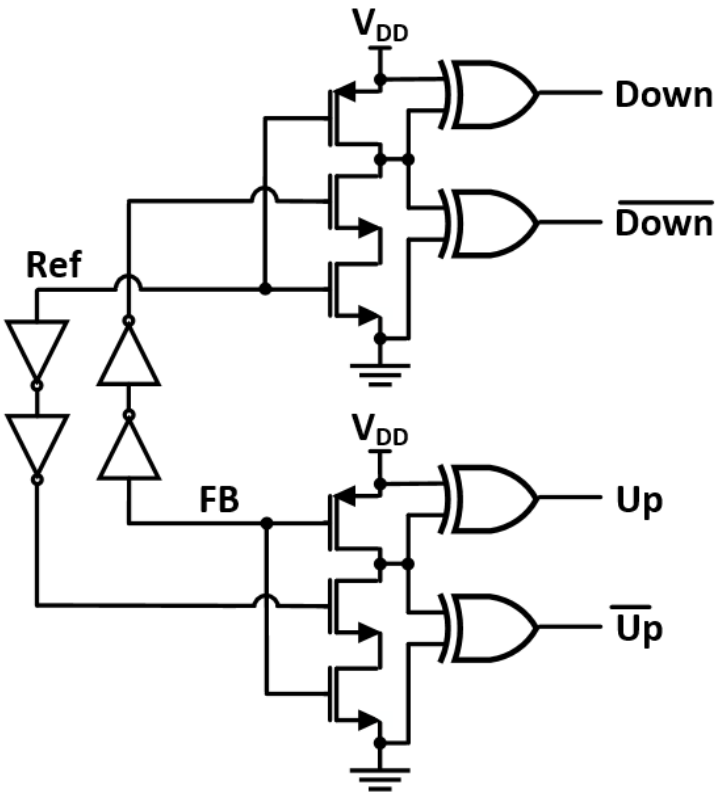


Figure. 36. Simplified PFD Schematic

This PFD is a modified version of the precharged PFD presented in [45]. This topology of PFD has been used previously in frequency synthesis circuits. This work seeks to extend their usage to dividerless frequency synthesis circuits. In the presented circuit, the outputs (Up/Down) are fed to the charge pump described in Fig. 37.

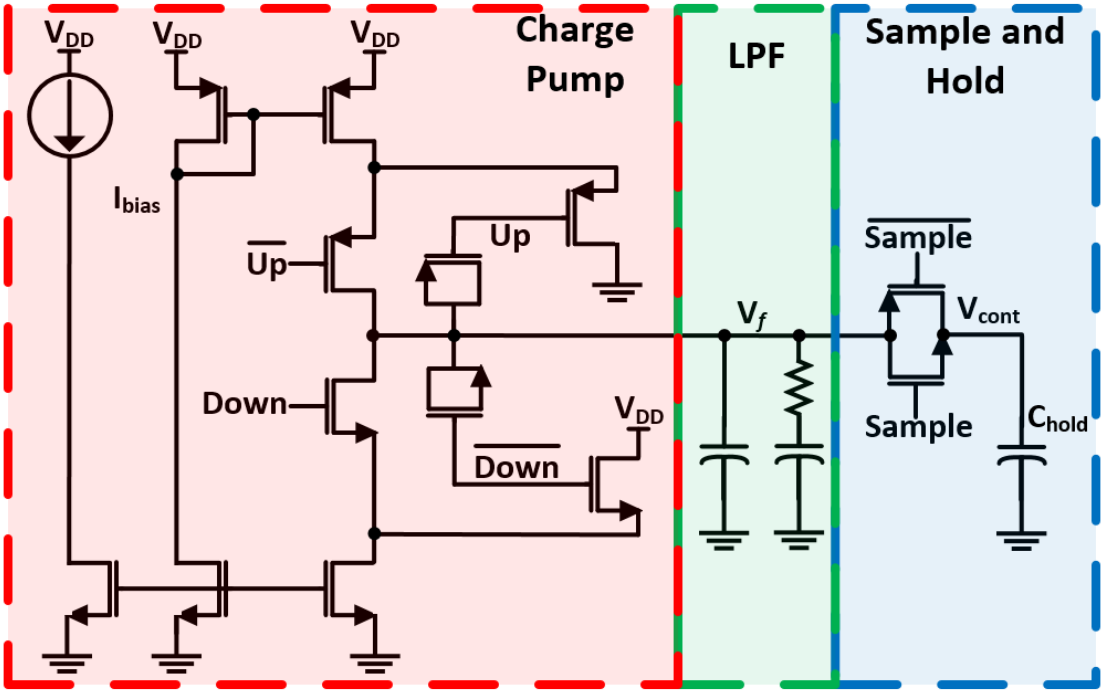


Figure. 37. Simplified CP Schematic

This CP is a standard current steering topology with an additional sample and hold added to the output of the LPF. This sample and hold is sampled at a rate defined by the “Sample” signal, which is a logically generated pulse when both Up and Down have been low for more than two propagation delays. By sampling the filter output when both up and down are idle, the circuit is able to disregard un-useful data, which will be shown in the following sections. It should be noted that the addition of this sample and hold block within the feedforward path does introduce an additional pole in the transfer function. However, this sampling is happening at a frequency equal to the reference frequency. Frequency synthesizers are generally designed such that the poles are a decade or more lower than the reference frequency. As such, the pole at the reference frequency should be located at a frequency where the transfer function’s phase has already crossed 180°, and therefore does not significantly affect stability. Furthermore, the holding

capacitor downstream of the transmission gate (C_{hold}) is negligibly small compared to the ripple rejection capacitor, making it have a negligible effect on the lowpass filter's transfer function.

The presented PFD and CP circuits have well understood behaviors when the Ref and FB signals are of similar frequencies. However, significantly different behavior emerges when the two frequencies are disparate by more than 50%. A graphic explanation of this behavior is included in Fig. 38. It is assumed throughout this work that FB is significantly higher frequency than ref, since ref is an external reference and FB is the output of the VCO. These definitions could be switched without loss of generality, but it would yield a non-feasible PLL architecture.

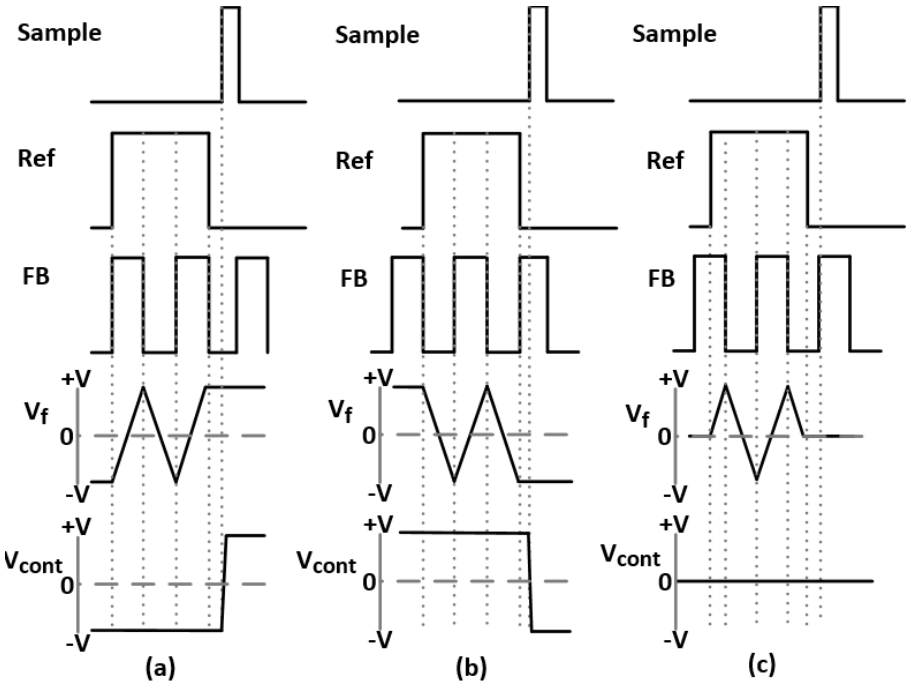


Figure 38. Graphic Demonstration of PD/CP Operation

During each full period of FB, it can be seen that there are period of current flowing into and out of the ripple rejection capacitor. The current mirrors can easily be

matched such that the sum of these currents equals zero. Pairs of up/down current swings that sum to zero shall be referred to in this text as “corresponding pairs”. Since FB is a significantly higher frequency than ref, the total number of corresponding pairs per period of ref is $Floor(\frac{N}{4})$.

Since these corresponding pairs have zero sum current during each period of FB, it follows that the voltage at V_f does not have any net change at the end of each period of FB. If the net change is zero, and only the final value matters due to the sampling block downstream of the filter, it follows that the sampled value of V_f is not a function of how many of these corresponding pairs occur.

If the corresponding pairs yield no change in the filter output, the entirety of the transfer function can be defined in terms of the “non-corresponding pairs” – that is current swings that do not sum to zero. These current swings only occur at the very beginning or end of a ref cycle (depending solely on definition). This is shown in Fig. 38. In 38a, it can be seen that there is a corresponding pair where V_f increases then decreases back to the original value. However, there is an additional upwards swing that has no associated downward swing. This non-corresponding swing causes the final value to be sampled at a value higher than the original value, thus indicating that the output is lagging. Similar results are yielded in 38b, but with the unmatched pair being a downward swing, indicating that the output is leading. Lastly, 38c shows the case where all current swings are part of a corresponding pair, which yields no net change at the output of the filter. This case is the locked condition. It should be noted that fixed input-output phase offsets are introduced as a complex function of N. Particularly, a 45°offset is introduced when N/2 is an odd number.

The source of PD/CP N^2 noise within traditional charge pump PLLs is due to the CP having a gain that is linearly decreased with N. However, it can be seen in the presented architecture, the gain, ß$_{CP}$, is defined in terms of the bias current I_{CP}, as

$$\beta_{CP} = \frac{\Delta I_{average}}{\Delta \phi} = \int_0^{T_{Ref}} \frac{I_{CP}}{2\pi \cdot T_{Ref}} dt,$$

Which simplifies to

$$\beta_{CP} = \frac{I_{CP}}{2\pi},$$

Where ϕ_{out} has been normalized such that zero is defined as the phase at which the system locks. A similar transfer function could be written in terms of absolute phase, but it would have to take into account the phase offsets, which are a complex nonlinear function of the PD, but do not affect the noise transfer function. Since this gain is not dependent on N, there is no source of gain degradation as a function of N. This implies that there is no source of PD/CP N^2 noise in the presented architecture. The derived gain of the presented CP is exactly equal to the gain of a Subsampling PLL with a VCO output amplitude of 1. [46]. As it is already been proven that the subsampling transfer function yields no PD/CP N^2 noise, showing an identical transfer function for this architecture is sufficient proof of the lack of this noise in the presented system.

There significant advantages to placing the sample and hold downstream of the charge pump. Because Vf has already been lowpass filtered, the signal occupies bandwidth well within the sampler's first Nyquist zone. This prevents aliasing problems, and also prevents the possibility of aperture error due to finite transmission gate switching time. Furthermore, the any error signal injected by the sampling operation is

downstream of two high gain blocks (PD and CP). If the same error signal were to be injected upstream of these blocks, the output error would be expected to be larger by a ratio equal to the product of the two gains ($K_{PD}K_{CP}$)

4.4. Implementation

The presented system was designed and taped out in a 65nm bulk CMOS process. The total area of the PLL circuitry is 0.0066 mm^2. An additional 0.0074mm^2 is used for the buffer chain used to drive off-chip loads. As the goal of this work is to demonstrate the feasibility of digital transmitters, all blocks in the presented system were designed using pre-made digital IP blocks to the maximum extent possible. The main exception to this rule was the VCO, which while highly digital in operation, requires significant attention to analog details, particularly matching and parasitics. Parasitics are important in the VCO design, as they define the achievable frequencies. For the purpose of accurately predicting the VCO frequency requires several iterations of post extraction.

The VCO used in the presented system is a 5 stage differential ring oscillator as shown in Fig. 39.

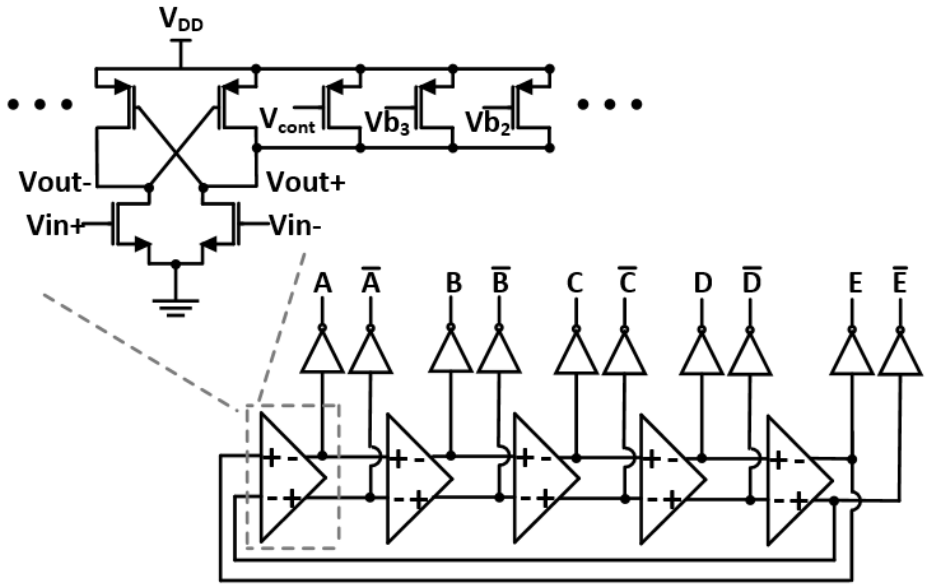


Figure 39. Simplified Ring Oscillator Schematic

As discussed in Section 4.1, ring oscillators have suboptimal noise performances due to low Qs. They do however have the advantage of small areas, low power consumption, ease of digital integration, polyphase outputs, and wide frequency reconfigurability ranges. This particular ring oscillator does have a significantly higher Q than a traditional current starved ring oscillator, but that advance is purchased at the cost of reduced frequency range. However, the presented ring oscillator is still capable of operating over a range of 1.15-2.5GHz, which covers the majority of sub 3GHz communication bands. A plot of the achievable frequencies as a function of Vdd and VCO code is included in Fig. 40:

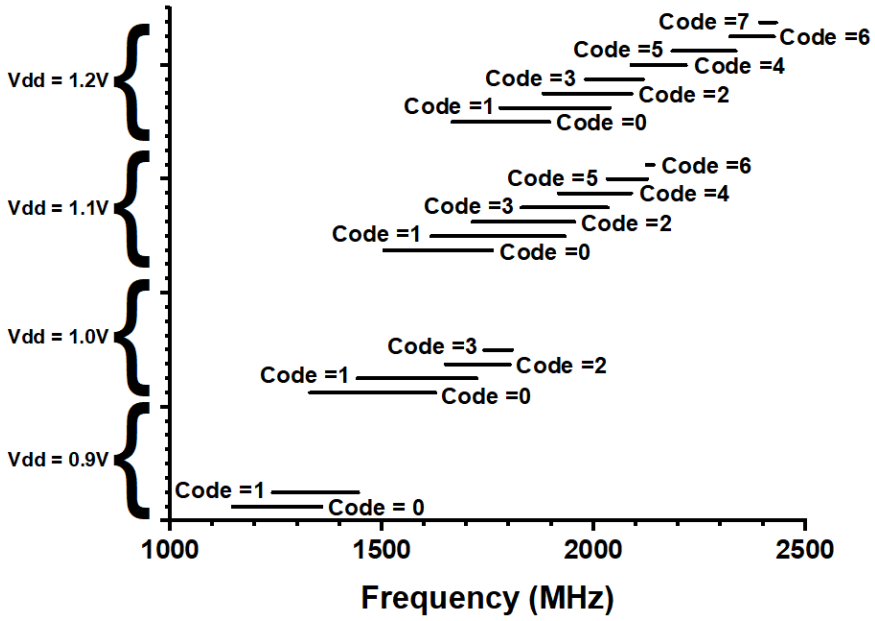


Figure 40. Achievable Output Frequencies

Regardless of the details of the particular oscillator being used, the theory presented in the previous section is not a function of the VCO characteristics. As such, any suitable oscillator (including tuned oscillators) could be substituted in the system without loss of generality, so long as they have appropriate center frequencies, frequency gains, etc.

The delay stage shown in Fig. 39 contains 3 bits of digital tuning, which are controlled by the digital inputs labelled a_x. These head transistors being enabled lowers the effective resistance of the delay stage, making it able to charge faster. Additionally, one transistor is controlled by analog tuning voltage V_{cont}, which is provided by the output of the sample and hold block downstream of the loop filter.

The polyphase outputs of the VCO are connected to a 10:1 multiplexer to select the desired phase. This multiplexer is generated using standard cell IP blocks. Because the standard cells only consist of multiplexers with 2^n inputs (e.g. 2, 4, 8, 16, …) a 16

input multiplexer is used, and the remaining inputs are connected to 6 of the 10 polyphase signals. This ensures equal loading of all multiplexer inputs to ensure a consistent propagation delay, which helps mitigate potential phase distortion. Since this leaves 4 of the 10 polyphase signals with a reduced capacitive load, these four are connected to an identical dummy multiplexer whose output is not used.

After phase selection, the polyphaser signal undergoes further modulation. However, as this section is only interested in the noise characteristics of the PLL, this section is bypassed. After this bypassed section is a chain of inverters which are used to increase the signals drive strength to be able to drive off chip loads. This inverter chain is expected to have some detrimental effect on the PLL's output noise performance, but unfortunately it is a requirement for the chip to be able to drive the available test equipment.

A micrograph of the presented circuit is shown in Fig. 41.

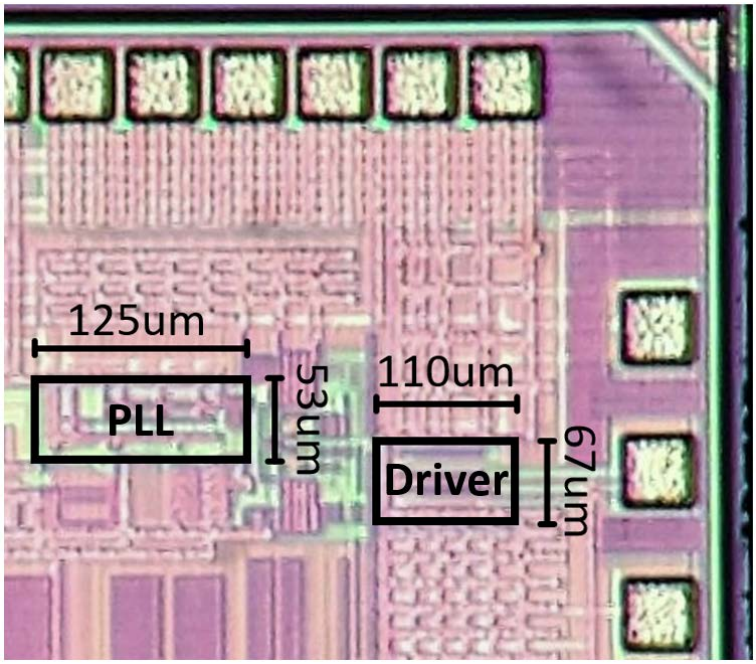


Figure 41. Chip Micrograph

4.5. Results

Measurements were taken on the presented circuit to verify its performance. The first characteristic to be verified was the frequency synthesis capabilities of the presented circuit. Fig. 42 shows a plot of the output frequency vs reference frequency. For the purpose of this test, all other variables were kept constant. Particularly, VDD and VCO code were set to 1V and 001 respectively. The reference frequency was swept via external source from 100MHz to 1.7GHz. higher frequencies could be used if the VCO code or VDD were increased to such that the VCO covers the desired band of frequencies. It can be seen in this figure that the output frequency is always equal to the closest integer multiple of the reference frequency. The slope of the resulting lines (m) represents the multiplication factor of the synthesizer. As can be seen, the two are equivalent (m = N). It can also be seen from the regression lines (blue lines) that all slopes intersect exactly at the origin, which proves that there is no frequency offset errors introduced in the frequency synthesis operation.

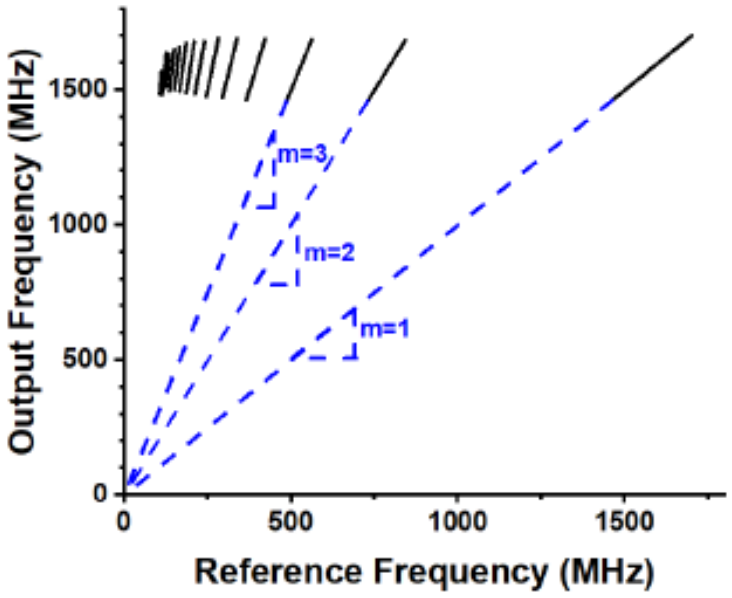


Figure 42. Output Frequency Versus Reference Frequency

The limit for the maximum value of N is defined by solely by the bandwidth of the VCO. Similar to most SSPLLs, the bandwidth of the VCO should be less than the reference frequency. Otherwise, the VCOs range would contain more than one potential integer multiple of Ref, causing a non-deterministic output frequency. To realize larger values of N, the presented circuit would require an additional auxiliary loops to discriminate between the potential output frequencies. Alternatively a more narrowband VCO, or a 2-step locking procedure [47] could be used.

The main goal of the presented circuit is to demonstrate in-band noise comparable with subsampling PLLs without the use of sampling blocks in the PD. To prove the noise performance of the presented circuit architecture, the presented circuit underwent extensive phase noise measurements. A plot of the best case output noise characteristics is included in Fig. 43. For the sake of brevity and clarity, only 3 arbitrary frequencies are plotted which roughly correspond to lower, mid, and upper frequency operation. Though

the out-of-band noise floors differ slightly between the frequencies, it can be seen that the in band noise performance is nearly identical between them. Using an integration window of 10kHz to 40kHz, the integrated jitters for these frequencies are 618fs, 380fs, and 250fs respectively. It should be noted that the main factor in the difference in jitter is the fundamental frequency, not the noise level.

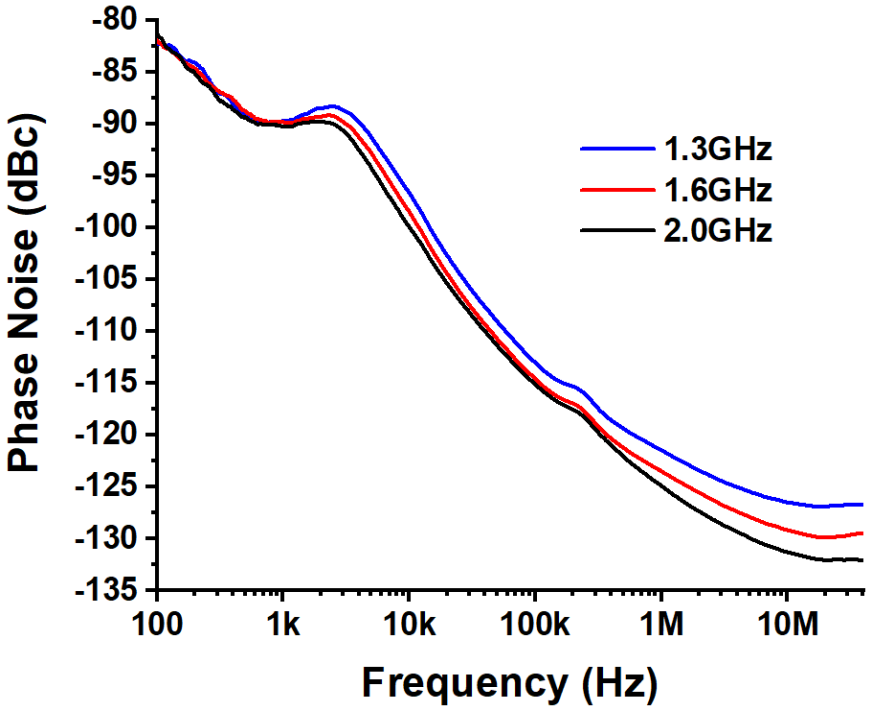


Figure 43. PN Plots for Various Frequencies

The power dissipation associated with these frequencies is plotted in Fig. 44.

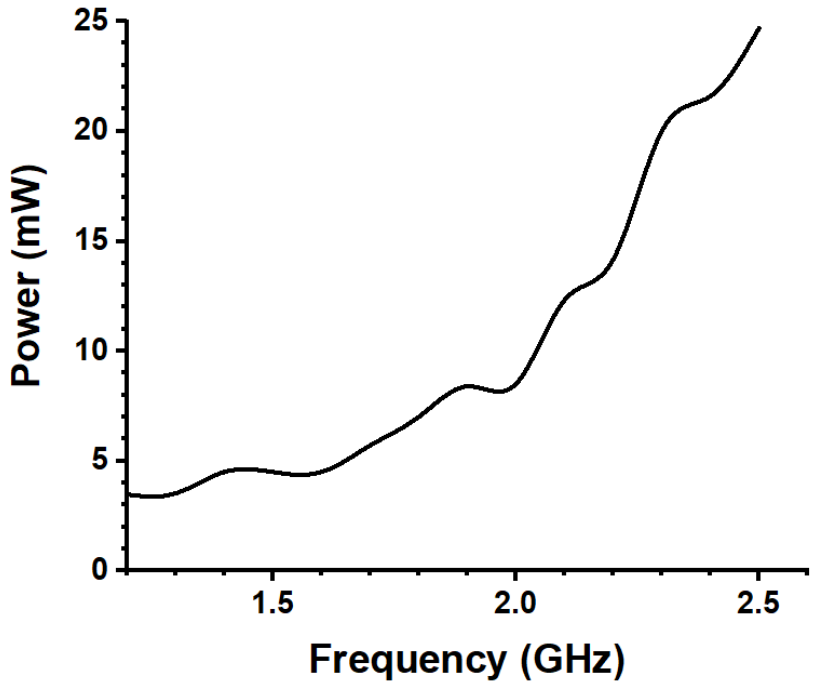


Figure 44. Power Dissipation vs. Frequency

It can be seen that the power increases quadratically as a function of frequency. This is due to primarily due to the dissipation of the ring oscillator, whose power is defined as

$$P = 2fCV^2$$

Additionally, this circuit requires a higher VDD to be able to generate higher frequencies. This relationship is also fairly linear. The combination of these relationships are responsible for the quadratic power relationship. Additionally, it can be seen that the power has significant periodic deviation from the ideal quadratic relationship. This is due primarily due to switching between VCO control codes, which causes discontinuities in the power dissipation.

By combining the noise and power measurements, the overall FOM for this PLL is -238.7, -241.9 and -242.7 dB at 1.3, 1.6, and 2GHz respectively. These PN profiles and figure of merits (FoMs) represent best in class performance.

To show that the presented circuit is capable of locking without the aid of an auxiliary loops, a plot of the output frequency versus time is included in Fig. 45. Due to limited measurement equipment capabilities, this plot is post-extracted simulation only data. However, this is sufficient empirical evidence to show that the presented PLL is capable of settling in a linear, second order manner. The particular case shown in Fig. 45 is generated by changing the reference frequency from 390MHz to 400MHz with N = 4. This results in a output frequency jump from 1560MHz to 1600MHz, and a settling time of approximately 75ns. While the actual settling time is a function of the reference frequency, the damping coefficient should be approximately equal for all operating conditions.

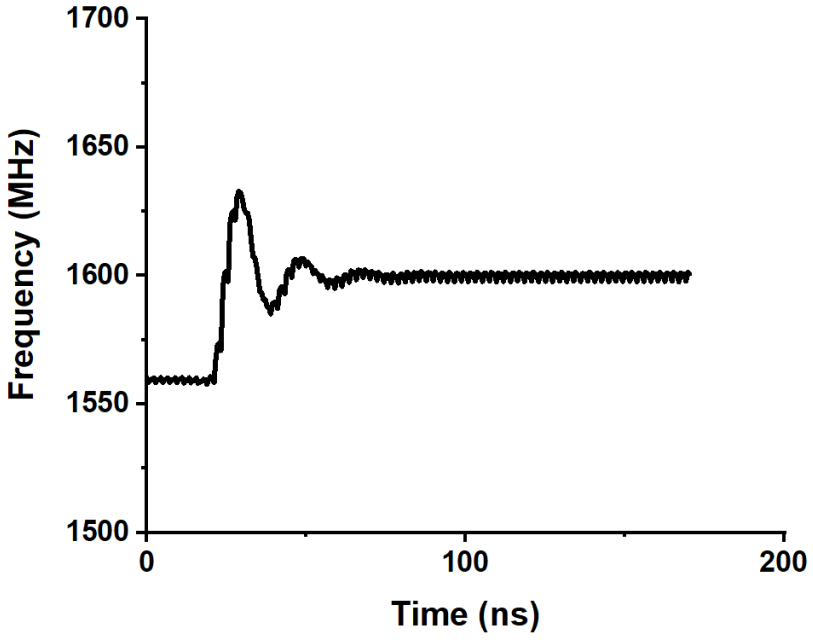


Figure 45. Simulated Settling Characteristics for N = 4

To show that the presented PLL architecture yields noise performance that is independent of N(No N^2 Noise), a plot of the in-band noise levels for various values of N is plotted in Fig. 46. It can be seen from this plot that the in-band noise shows no

significant dependence on N. This particular plot was generated at 1.6GHz, but similar performance is yielded across the entire frequency range.

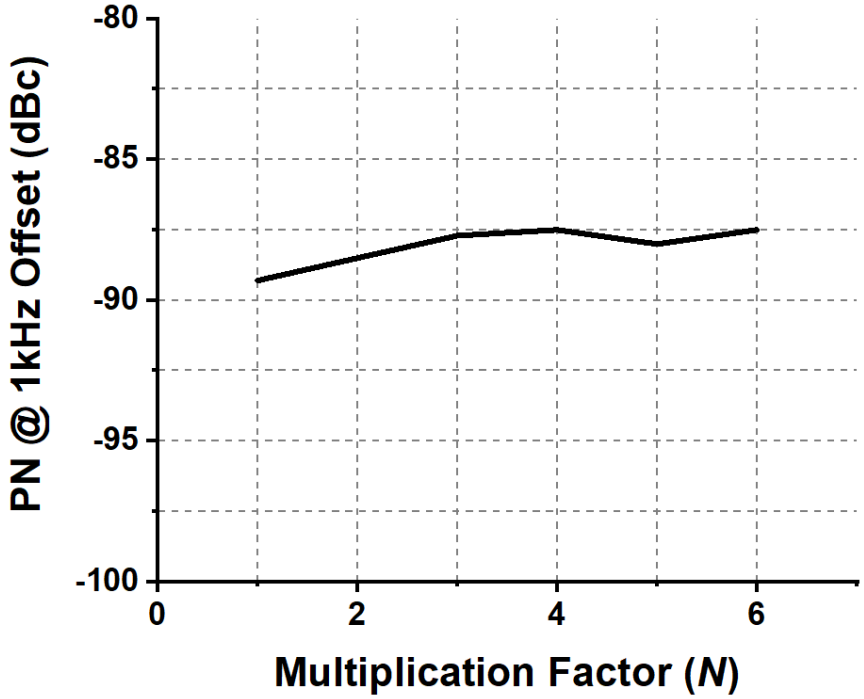


Figure 46. In-band Noise Level vs. N

A plot of the presented circuit's measured spectrum is included in Fig. 47. This spectrum is generated for an output frequency of 1.6GHz. The blue trace corresponds to the spectrum when N=1. As can be seen, the spectrum is free from any significant spurs. Superimposed on this plot is the spectrum resulting from N = 2 (red trace). It can be seen that this operating condition yields a pair of spurs with magnitude -46dBc located at an offset of fc/2. Similar spurious behavior is exhibited for larger values of N, but the offset location is fc/N.

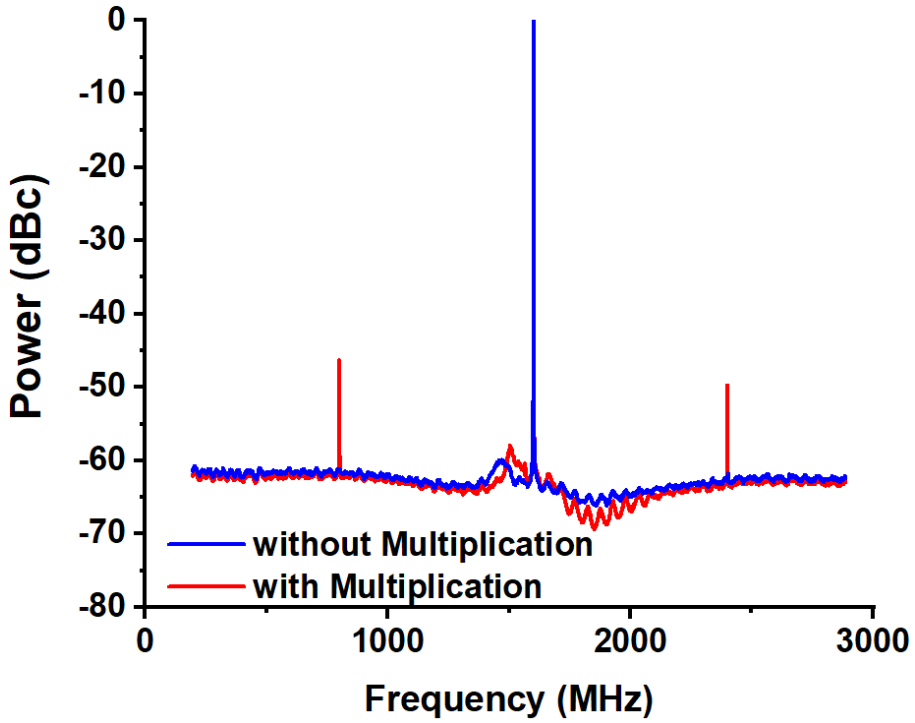


Figure 47. Spectrum with and without Integer-N Synthesis Enabled

Table 7 is replicated below in Table 8 with the measured specifications of the presented circuit included. As can be seen, the presented circuit demonstrates state of the art noise, area, power, frequency range and FoM.

COMPARISON TO PRIOR WORK

	[8]	[9]	[10]	[11]	[12]	[13]	[14]	This Work†
Technology	130nm	65nm	65nm	28nm	65nm	65nm	65nm	65nm
Topology	SSPLL	Active SSPLL	SSPLL w/ FeedForward	SSPLL	Switched Loop	Injection Lock	SSPLL	Sampled Filter
Oscillator Type	Multi-ring	Ring	Ring	Ring	SFT Ring	Ring	Ring	Ring
Supply Voltage (V)	1.3	1.2	0.94	1	1.2	1.1	1.2	0.9-1.2V
Active Area (mm^2)	0.21	0.0049	0.022	0.023	0.08	0.06	0.008	0.0066
Frequency (MHz)	800-1300	1100-2600	2000-2800	2.08-2.72	3000	0.96-1.44	2000-3200	1200-2500
Reference Spur (dBc)	-42*	-37	-55	-63	-71	-53	-64	-46
Integrated Jitter (fs)	571	720	633	248	357	185	422	250
Integration Bandwidth (Hz)	10k-100M	10k-100M	1k-100M	10k-100M	1k-80M	10k-40M	1k-100M	10k-40M
PN @ 1MHz (dBc)	-121.0	-114.4	-119.1	-125.4	-105.0	-113.5	-122.6	-124.8
Power (mW)	19	4.59	5.86	4.1	4.6	9.5	6.1	8.5
FoM (dB) +	-230.0	-236.2	-236.3	-246.0	-242.3	-244.9	-239.7	-242.7

† All results specified for 2.0GHz * Fractional Spur $+FoM = 10log_{10}(\frac{\sigma^2}{1s} \cdot \frac{P}{1mW})$

Table 8. Comparison to Prior Art

4.6. Conclusion

The presented PLL architecture emulates the noise performance of a subsampling PLL without the need for a sampling block within the phase detector. Furthermore, the presented architecture does not suffer from many of the issues associated with subsampling PLLs. Among these issues are aperture/pedestal errors, high frequency sampling, and variable current output charge pumps. Measurement results yield a FoM of -242.7dB, integrated jitter of 250fs, and PN of-124.8 @ 1MHz offset. These results are on par with the state of the art of all published state of the art ring oscillator based PLLs. Additionally, the lack of VCO sampling and auxiliary loop allows the presented circuit to have the lowest reported area of only 0.0066 mm^2.

The presented circuit allows for extremely low noise polyphase frequency synthesis. When combined with the other techniques proposed in this work, this helps enable modern communications via digital transmitter. Particularly, this lowered noise level aids in the transmission of low EVM waveforms, which is necessary for high density constellations such as 64 or 256 QAM.

It should be noted that the presented PLL architecture is compatible with all other techniques discussed in this work. Particularly, this PLL architecture could be used for the PLL described in Chapter 2. The presented PLL could also serve as the frequency synthesizer which drives the harmonic cancellation amplifier described in Chapter 3. Furthermore, the presented circuit is designed to be integrated with the dynamic range extension technique that is discussed in the following chapter. Specifically, the PLL discussed in this chapter is actually fabricated on the same die and actually is used as the synthesizer for that particular circuit.

CHAPTER 5

DELTA-SIGMA PHASE INTERPOLATION

5.1. Background

While Chapters 2 and 3 focused on extending the frequency reconfigurability of the ADT system, there are other specifications that must be taken into account. The focus of this chapter is to demonstrate the extremely high precision digital modulation that is needed to be viable for modern communications standards. Furthermore, it will be shown that this system is PVT invariant, which allows it to viable for a mass production scenario.

It was shown in Chapter 2, Section I that the phase resolution of a tapped delay line phase shifter is limited by the number of elements and their associated propagation delays. In a system not using a multi-stage phase upconversion process, as described in Chapter 2, section 2, a tapped delay line may expect to get as high as 5 bits of phase resolution. Unfortunately, this is not fine enough resolution to transmit the majority of modern communication standards, such as LTE, WLAN, etc. This is exacerbated by the fact that the pulsewidth-to-amplitude transfer function is sinusoidal. This nonlinearity means the distribution of possible amplitude points is non-uniform, and tends to cluster the majority of possible amplitudes towards full scale amplitude. To alleviate the lack of available quantizations, some form of interpolation – the generation of intermediate phases from known phases – is necessary.

Previous authors have augmented the tapped delay line structure with interpolation methods to achieve finer phase shifting resolution. The most common of these interpolation methods is resistive network interpolation as shown in Fig. 49. While

these methods do, in fact, increase the phase resolution, they add noise and require extreme attention to matching and calibration. For example, the interpolation network presented in [5] is ideally capable of increasing the phase resolution by a factor of 2 but requires over 7000 devices to be matched. This presents a serious problem for industrial acceptance as it causes low fabrication yield and adds significant time and money towards testing requirements.

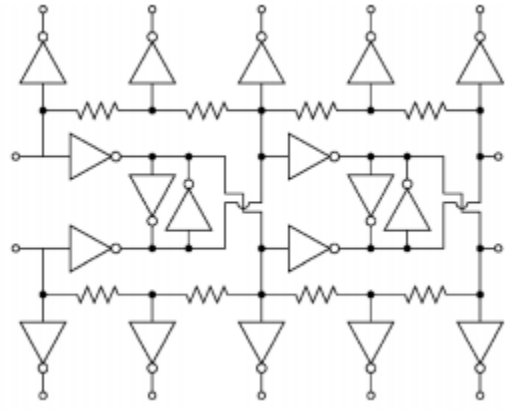


Figure 48. Resistive Interpolation [5]

It should also be noted that the existing methods only optimally function over a small frequency range. Though the authors frequently claim frequency ranges in excess of 1GHz, one can see that the phase resolution decreases as a function of frequency. [5] While this work does not intend to function over a wide range of frequencies, its all-digital nature lends itself nicely towards frequency agility and reconfigurability. The addition of frequency reconfigurability is expected to be the subject of future work on this project. A summary of the state of the art is provided in the following section

5.2. Current State of the Art

Table 9 provides a comparison of the current state of the art for phase interpolated polar modulation systems.

	[26]	[16]	[18]	[48]	[49]
EVM (dB)	-25	-25	-29	-26	-25
Frequency (GHz)	2.5	2.1	2	1.2	2.4
QAM	64	64	64	64	64
Bandwidth (MHz)	20	20	20	20	20
Technology	65nm	130nm	40nm	40nm	32nm

Table 9 – Summary of Prior Art

This table verifies the claims made in the previous section, namely that each of the previously demonstrated systems operate over a relatively small reconfiguration bandwidth.

Unfortunately, fabrication yields are not a frequently published specification for polar modulator systems. However, it is hinted at in previous works that the yields for such systems can be lower than one standard deviation (<60%) [50]. Regardless of the actual values of the yields for each of the systems noted above, it is expected that they

will not be sufficiently high to meet commercial demands, which regularly require upwards of 90% yield rate.

In [50] the authors presented the first published usage of a delta sigma (DSM) phase interpolator. [50] demonstrates only a high accuracy phase shifter, not a whole transmitter, but it presents the foundational theory upon which the following sections are based. A short summary of the results found in 10] is included below:

If a phase shifter has a limited resolution due to large quantization steps, it is possible to switch between possible phase quantizations at an oversampled rate, and in doing so, provide an effectively correct average phase. The rate at which the possible phases are alternated between is controlled by a simple Delta Sigma modulator. Detailed analysis of nonlinearity (DNL & INL) are derived, and the constituent circuit blocks needed to construct the system are presented. The achieved specifications of [50] are presented in Table 10.

Process	45nm
Carrier Frequency	1-3GHz
Area	0.15 mm^2
Modulation Scheme	GMSK
IBW	20MHz
ACLR	-51.6 dB
EVM	-33.5 dB
Power	34 mW

Table 10 – DSM Performance Summary

The work presented in this thesis operates using a similar concept to [50]. The main differences between these works are follows: This thesis presents a full modulator system, which necessitates multiple interpolators running in parallel, output networks, etc., whereas [50] contains only a single phase interpolator. Additionally, amplitude modulation is included in this modulator, whereas [50] is valid only for constant envelope systems. Lastly, this thesis moves the tapped delay line into the delta sigma's feedback loop, which allows the PVT sensitivity to be significantly reduced.

5.3. Theory

Since amplitude modulation in this system is accomplished via RFPWM, all that is needed in the system is two high resolution phase shifters and digital logic. To provide higher resolution phase shifting than is shown in previous works, this work presents a novel form of phase interpolation using full-loop DSM.

The fundamental premise of this work is to use the outputs of a ring oscillator, rather than simply cascaded delay units. When arranged as an oscillator, the circuit forces each node to have equivalent phase-distance to its adjacent nodes. This is, of course, assuming perfectly matched conditions. However, this is not unfeasible, since the ring oscillator being used in this work is only 5 stages. This smaller number of stages allows very simple matching. This oscillator can then be controlled via the PLL from Chapter IV, PLL as shown in Fig. 49, which automatically calibrates each stage to be the desired level of delay.

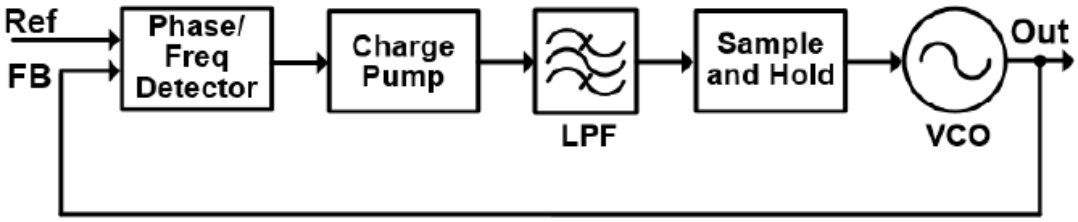


Figure 49. Simplified PLL Block Diagram

With a 5 stage differential VCO, 10 uniform phase shifts can be achieved (36° each) as shown in Fig 50. Resistive interpolation could yield even higher resolution, but this would require extensive matching networks as described previously. In order to interpolate the 36° phases into ~1° quantizations, this work also proposes the addition of a delta sigma architecture as shown in Fig. 51. A mathematical description of the architecture is provided in Fig. 52.

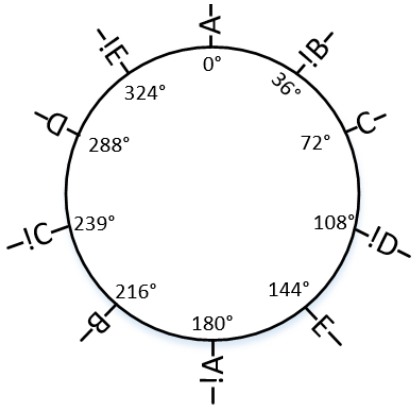


Figure 50. Phase Mapping of VCO

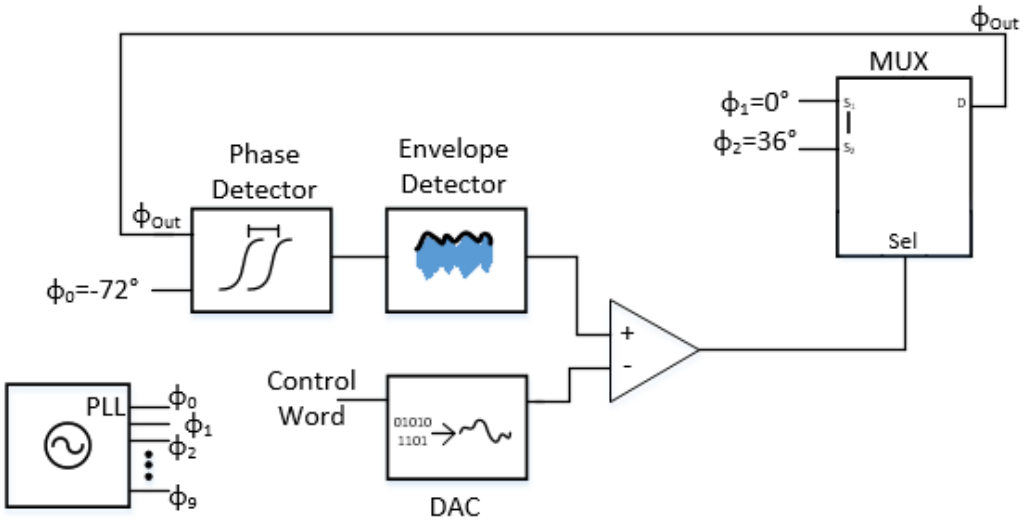


Figure 51. Delta Sigma Phase Modulator

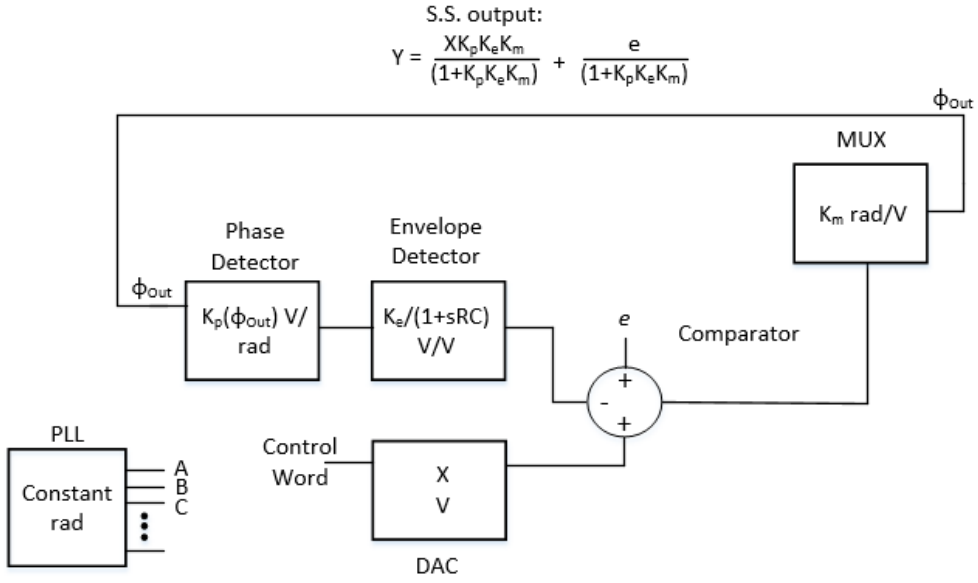


Figure 52. Transfer Functions of Interpolator Subblocks

The delta sigma modulator takes the output phase and detects its phase difference to a fixed reference. Depending on whether the average output phase is larger or smaller than desired, it switches between two reference phases (from the VCO). Switching

between these reference phases produces an effective average phase. The -72° at the input of the phase detector is chosen due to the dynamic range of the DAC and phase detector.

DSM schemes have been demonstrated before for averaging phase [50, 51]. However in all of them, the delta sigma is run open loop; if they want a phase half-way between the two references, they simply run a 50% duty cycle. To the author's knowledge, this would be the first demonstration of a closed loop DSM for phase modulation. Because this system is closed loop, it mitigates potential problems with offset or matching problems.

A less obvious consequence of using the DSM to interpolate the phase is that differences in the differential phase shift between the two phase shifters will cause a different duty cycle for each individual pulse. Since RF PWM fundamentally operates by changing the duty cycle to change the associated fundamental power, changing these duty cycles will change the effective amplitude. Intuitively, there are 4 permutations of the amplitude for any given pulse:

1. Phase 1 = 0°, Phase 2 = 0°
2. Phase 1 = 0°, Phase 2 = 36°
3. Phase 1 = 36°, Phase 2 = 0°
4. Phase 1 = 36°, Phase 2 = 36°

Since only duty cycle effects the amplitude, then options 1&4. And 2&3 are effectively the same as far as amplitude is concerned. This leaves the system with two possible amplitudes, which will be switched between in pseudo-random patterns. These

pseudo random patterns can be further controlled by adding correlation between the modulators, as shown in Fig. 53.

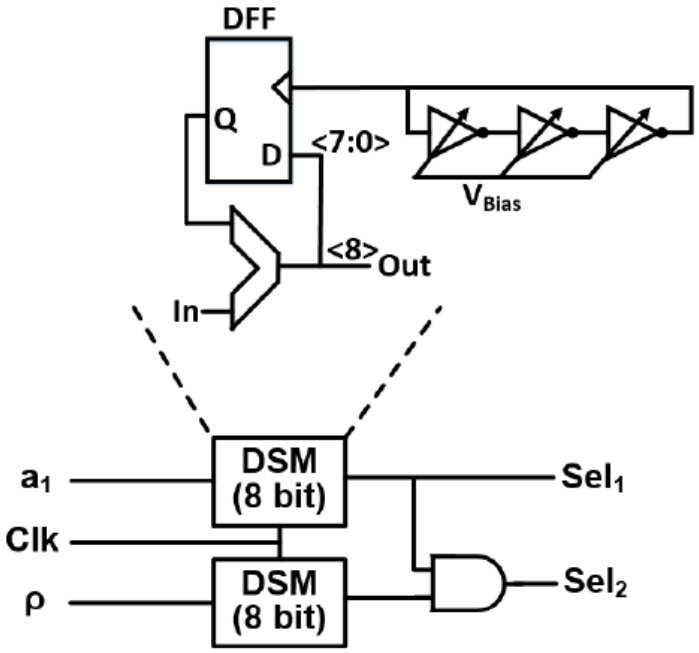


Figure 53. Correlated Modulators

In this arrangement, the average amplitude will simply be the average of the two possible amplitudes, normalized by the rate at which each condition is expected to occur. The rate at which each will occur is dependent on the duty cycle of the DSMs, which is a complex function of the relative distance between the two phases. For this reason, no closed form equation is provided in this section. A full derivation of the amplitude transfer function can be found in Appendix C. Despite the relative complexity of the transfer function, the achievable amplitude and phase values can be found using a simple Matlab model of the system and loaded into the FPGA to decode the IQ data to DSM codes. Since the output mapping has to occur regardless, the addition of this lookup table does not require any extra test or measurement beyond what is already required.

It should also be noted that this amplitude distortion naturally changes the RFPWM system into a BBPWM system at low amplitudes. Because the output of the AND gate is zero at or near 180° due to pulse swallowing, no pulses are produced when both phases are the same (i.e. Phase 1 = 0°, Phase 2 = 0° or Phase 1 = 36°, Phase 2 = 36°). However, when one pulse is 36° offset from the other, a 36° duty cycle pulse is outputted. This means that the whole system turns on and off the carrier at the duty cycle and frequency of the comparator – which is significantly lower in frequency than the carrier. This on-off switching allows the minimum duty cycle to be limited to 36°, which prevents pulse swallowing from occurring. Similar schemes could be enacted that would limit the duty cycle to an arbitrary pulsewidth other than 36° with additional circuitry. This mode is referred to as "swallowing mode" and is graphically shown in Fig. 54.a.

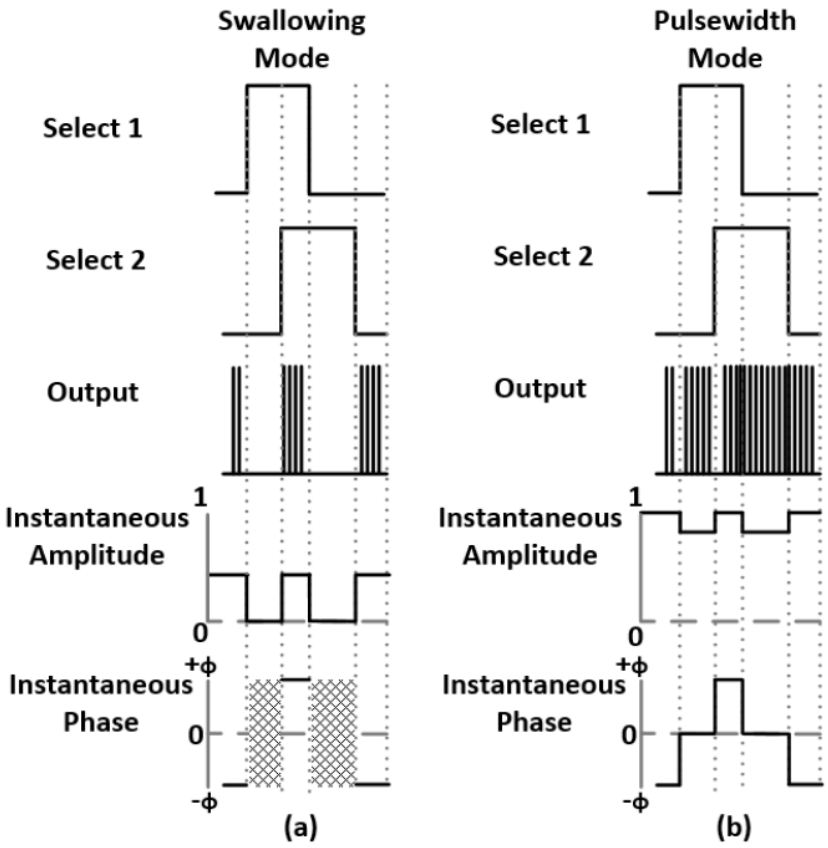


Figure 54. Graphical Example of Time Domain Waveforms in (a) Swallowing Mode and (b) Pulsewidth Mode

Using the correlation properties, it is also possible to provide phase shifting without corresponding amplitude modulation. This is accomplished by activating both DSMs simultaneously. An example plot of the possible trajectories as a function of the correlation coefficient, p, is shown in Fig. 55.

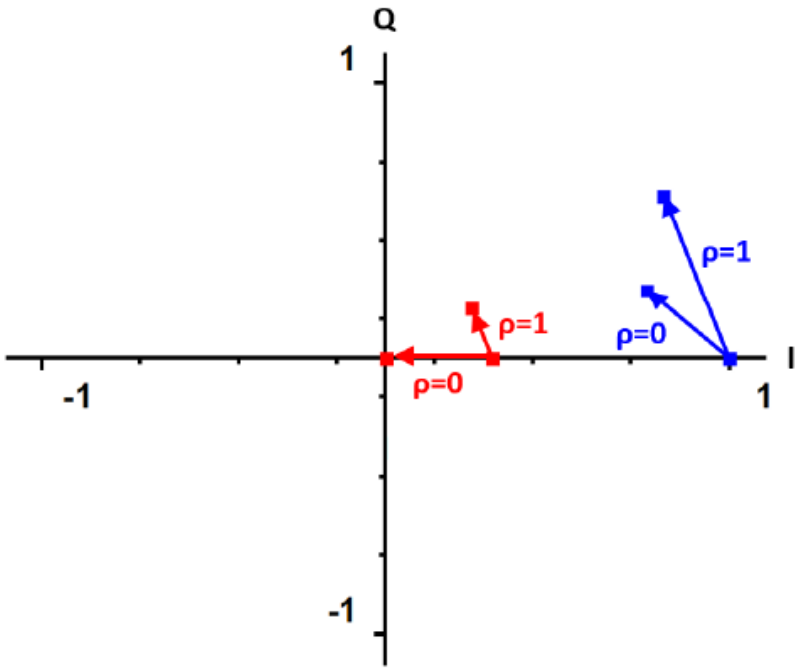


Figure 55. Potential I/Q Trajectories

By expanding out all possible I/Q trajectories over the entire Cartesian space, a map of the achievable constellation points can be generated. This mapping is shown in Fig. 56. While there are some deadzones, the possible I/Q vectors provide a fairly complete coverage of the I/Q plane.

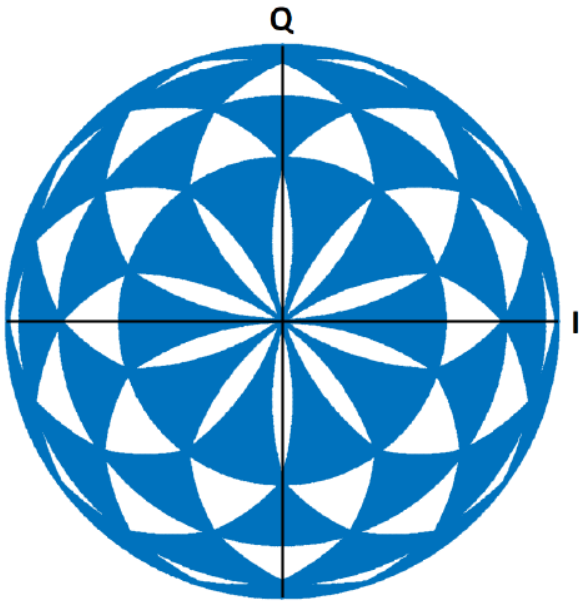


Figure 56. Possible Output Vectors with DSM Interpolation

This coverage is in stark contrast to what is ideally achievable by the same system without using DSM interpolation, which is shown in Fig. 57. Because of limited number of quantizations and relatively high pulse swallowing threshold, it can be seen that not even 16QAM constellations could be transmitted.

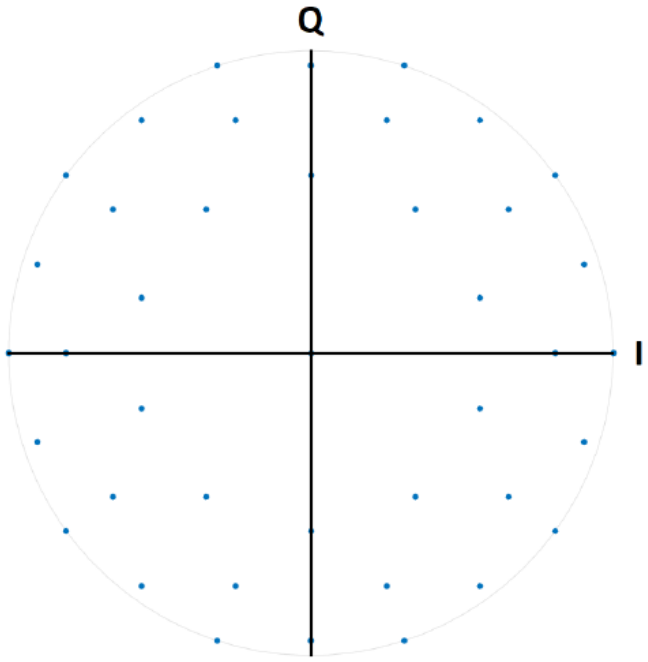


Figure 57. Possible Output Phases without DSM Interpolation

Using the possible output vectors shown in Fig. 56, a map of the best case 64QAM constellation using DSM interpolation is shown in Fig. 58. The blue dots represent the ideal points, while the red points represent the closest possible output. As can be seen, the constellation is nearly perfect, which leads to an ideally very small static quantization error.

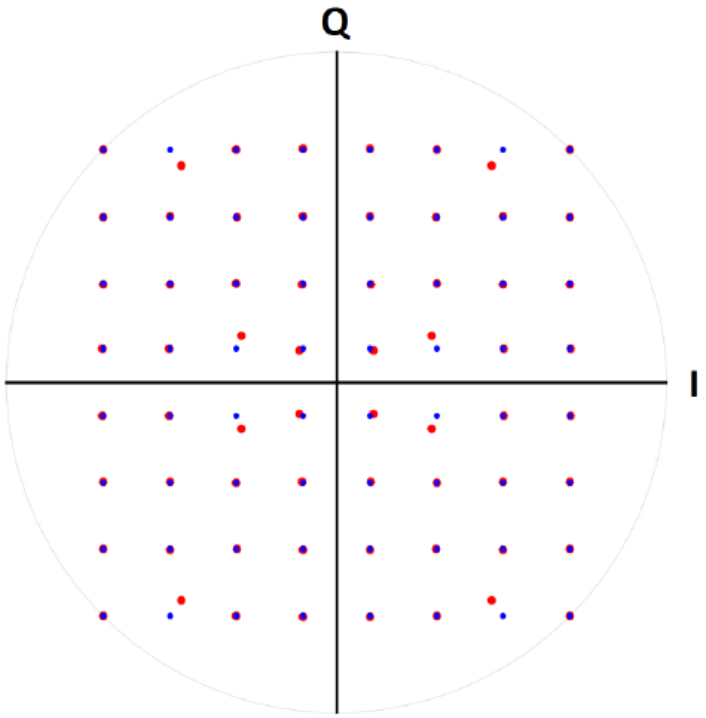


Figure 58. Achievable 64QAM Constellation using DSM Interpolation

One of the main problems typically associated with PLL-based phase shifters is their inherent narrowband operation. When phase modulation is applied before or during the loop, it requires the PLL to (re)lock before a symbols phase is valid. However, this topology does not suffer from these bandwidth concerns because the phase shifting is not included in the actual loop. Each node of the ring oscillator is tapped and multiplexed outside the loop. Therefore changing which of the node outputs is multiplexed out does not affect the locking characteristics of the loop. This implies that the bandwidth of this system is determined solely by the multiplexer and downstream logic. Since this work implements everything downstream of the PLL with standard cell digital logic, it is inherently capable of large instantaneous bandwidths. These potential bandwidths are expected to be significantly larger than the maximum of 20MHz that is required for WLAN. Furthermore, this allows design flexibility in the design of the PLL. Specifically,

the PLL's loop bandwidth can be adjusted to provide optimal in-band noise characteristics at the expense of settling time. The ultimate limiting factor for the system's potential bandwidth was the SPI, which was not able to exceed 700MHz, thus limiting the symbol rate to <5MHz.

There are some bandwidth tradeoffs with respect to EVM and dynamic range. While the minimum dynamic range is set by the minimum value of the modulators, the symbol must be transmitted in entirety during a finite period of time. During this time, there are a finite number of pulses, n. Since a non-zero symbol must have at least on pulse contained within its duration, the minimum amplitude is defined as A/n, where A is defined as the minimum non-swallowed pulse. However in order to lower EVM via averaging, it is recommended that the DSM repeat it's pattern at least 4 times within a symbol duration. The number of times that the DSM repeats it's pattern is a function of both the (used) DSM bit length, as well as the sampling frequency.

Unlike most DSM systems, there is no benefit to significant oversampling of the modulator. Since phase information is contained only in the edges of squarewaves, no marginal increase in sampled information is provided by sampling at a rate exceeding twice the carrier frequency. Furthermore, it was observed during design and simulation that sampling rates above half the carrier frequency yielded significant increase in the spur levels at the output. Thus, the DSM was designed to operate in the range of ¼ - ½ of the carrier frequency. As the maximum output frequency is approximately 2.4 GHz, the DSM must sample no faster than 1.2GHz.

Furthermore, the bandwidth degrades the achievable EVM of a system. For a given, static input, the DSM is expected to have a pattern time of

$\pm\frac{GCD(code,code_{max})}{f_{DSM}}$. If the symbol period is not an exact multiple of the pattern time, there is a partial period of the DSM pattern present in the duration of the symbol. Depending on where this partial pattern falls, there is a chance of having one higher or lower number of pulses than expected. During swallowing mode, this represents an amplitude error which can be expressed as

$$\epsilon = \frac{0.59BW}{a_1 \cdot f_{DSM}} \cdot rem(\frac{1}{BW}/\frac{1}{a_1 \cdot f_{DSM}}) \cdot a_1 f_{dsm}$$

Where rem is the remainder function. This can be further simplified to

$$\epsilon = 0.59BW \cdot rem(\frac{1}{BW}/\frac{1}{a_1 \cdot f_{DSM}})$$

Which leads to a normalized EVM value of

$$EVM = \frac{\epsilon}{A_{desired}} = \frac{BW}{a_1} \cdot rem(\frac{1}{BW}/\frac{1}{a_1 \cdot f_{DSM}}) .$$

It can be seen in the above equation t hat the EVM is proportional to the bandwidth of the transmitted symbol. This is similar to most modulators.

A similar degradation exists in the pulsewidth mode. Unlike the swallowing mode, where an extra pulse contributes amplitude error, the error of an extra puylse during pulsewidth mode primarily introduces phase error. Using similar analysis to the amplitude error derivation, it can be seen that the phase error in pulsewidth mode is expressed as

$$\epsilon_\phi = \frac{BW}{f_{DSM}} \cdot 36^\circ \cdot rem(\frac{1}{BW}/\frac{1}{a_1 \cdot f_{DSM}}) .$$

Which leads to an EVM of approximately

$$EVM = sin(\epsilon_\phi)$$

.

A full mathematical description of the system is omitted from the main text of this work. Readers are advised to reference Appendix C for the full derivation.

5.4. Implementation

To realize the system presented in the previous sections, a PLL-based phase shifter is designed in a 65nm bulk CMOS process with total dimensions equaling 1.5mm x 1.5mm. A custom board has been designed for verification and test, and uses a simplified SPI protocol to interface with the commercial FPGA evaluation board (KCU105). Two implementations were included in this tapeout: one analog closed loop, and the other a digital open loop solution. The analog solution shall be discussed first, followed by the digital solution.

The 5 stage ring oscillator is generated in a standard ring oscillator configuration [52], as shown in Fig. 59. This ring oscillator is then duplicated and placed in parallel, so that there are two identical VCOs placed adjacent to one another. Each corresponding node between the two oscillators is then connected via inverter as shown in Fig. 60. This forces the two oscillators to be exactly 180° out of phase from one another. Additionally, it also generates faster rise/fall times and lower overall noise. This oscillator is designed to have a smaller than average frequency gain to allow the circuit some noise immunity. Unfortunately, reducing the frequency gain of this block changes the transfer function and can cause noise to increase. The optimum solution is found experimentally.

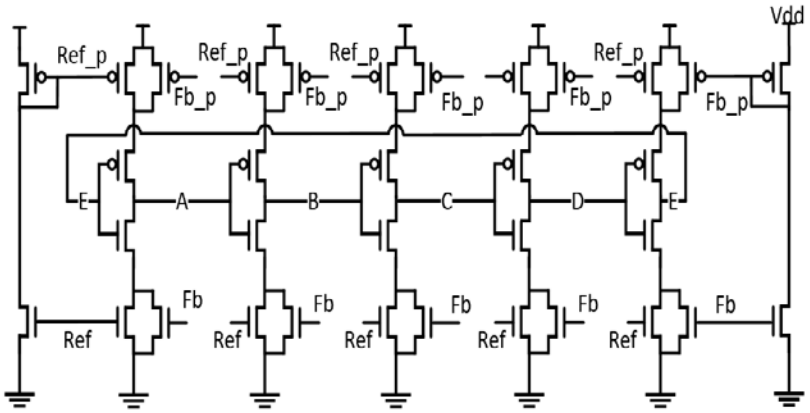


Figure 59. 5 Stage Ring Oscillator

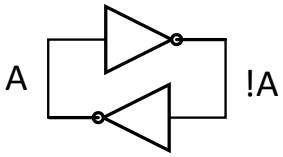


Figure 60 Edge Inversion Circuitry

The phase detector for the DSM's feedback loop is implemented as a simple XOR. This topology offers the smallest form factor, power dissipation, and input capacitance possible. When the output waveform is completely in phase, the XOR generates its minimum voltage, which would be 0. Correspondingly, the max average voltage would be when the signal is maximally out of phase, which would yield 2 times the maximal phase difference (relative to vdd). In the proposed system where the min and max phases at the output are 0 and 36 respectively, the range of the envelope detector's average output voltage would be 0-1/5 Vdd. However, the phase comparison of extremely small phases is problematic due to pulse swallowing (for any digital phase comparison, not just the XOR). So for the proposed system, it is actually much easier to work in a dynamic range of 72-102°. This can be accomplished by introducing a static -72° offset to the reference of the phase detector. Since the PLL already generates phase shifted

replicas of the clock at every 36°, this is easily accomplished by simply connecting a different PLL output to the input of the phase detector.

The most straightforward method of envelope detection for the XOR based phase detector would be simply to add a lowpass RC filter to the output of the XOR, as shown in Fig. 61.

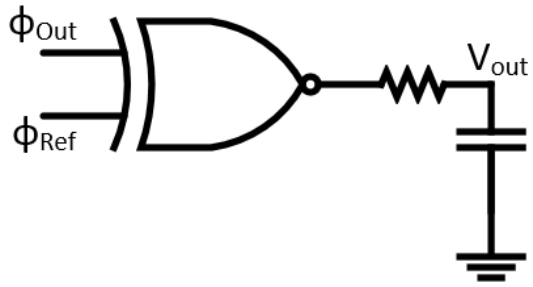


Figure 61. Simple Phase Detector Circuitry

This phase detector would effectively find the average (DC) value of the XOR based on its duty cycle. However, this limits the maximum voltage based on the maximum duty cycle, as discussed in section A. By changing the RC filter into a switched RC filter as in Fig 62, the system can provide DC gain. This gain relaxes the requirements of the comparator. The gain is determined by the ratio of resistors R1 and R2, and was optimized iteratively during co-design with the DAC and comparator.

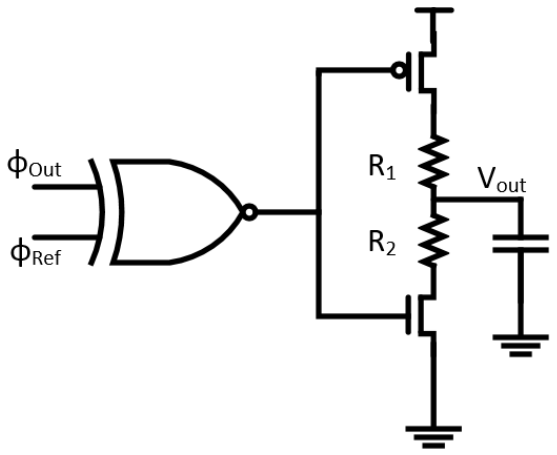


Figure 62. Phase Detector with DC Gain

The transfer characteristics of the topology shown in Fig. 62 is ideally identical to the topology shown in Fig. 61 over the intended range of input phases, with exception of a constant DC gain term, A. As such its transfer function would be

$$H(\phi) = \frac{A \cdot \Delta(\phi)}{1 + R_{eff} C s}$$

where R_{eff} is the effective resistance of the circuit.

With a constant phase offset between the two input signals, the steady state transfer function simplifies to

$$H(\phi) = A \cdot \Delta(\phi) .$$

The total (simulated) behavior of the envelope detector over an input range of 82-126ps (70°-110°) can be seen in Fig 63.

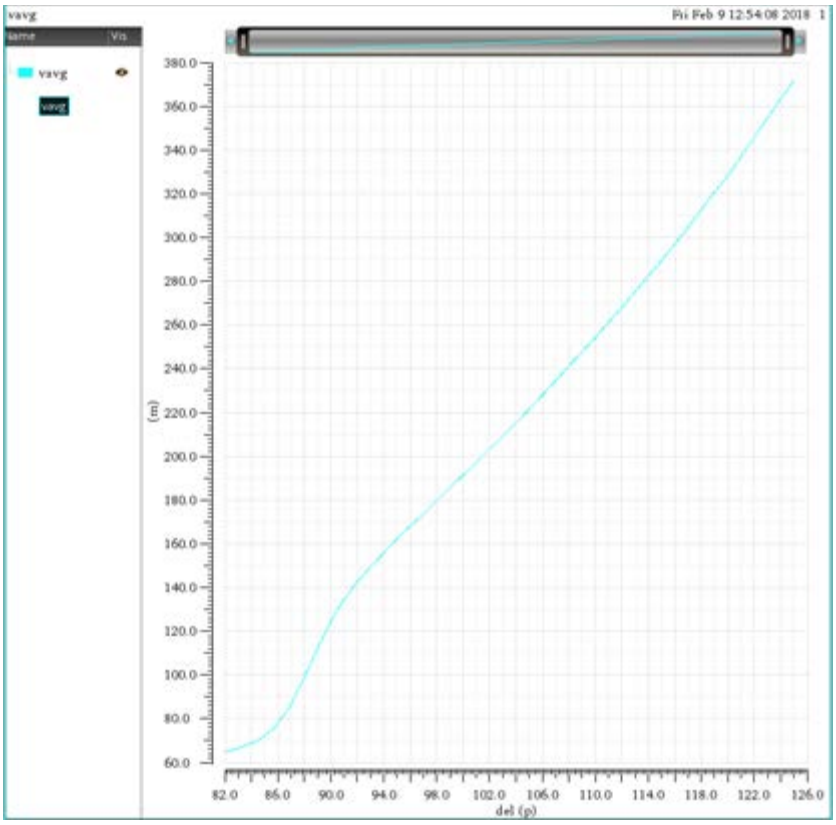


Figure 63. Simulated Phase Detector Output

These resistors should ideally be closely matched, otherwise there will be gain error. Though this may cause static errors, the output is still a linear function. Thus the DAC can be designed with extra dynamic range. As long as the dynamic range of the DAC is capable of covering all expected mismatches, the change in DC gain of the envelope detector results in no loss of resolution. The mismatch of the resistors need only be measured once in a quick calibration, and the DAC input codes can be adjusted accordingly. While this does constitute a calibration, it does not require circuit adjustment, only one-time input mapping. Furthermore, this calibration must be done for output mapping and DPD regardless, so no extra steps are added. A Monte Carlo simulation of resistor mismatches is provided in Fig. 64. This figure serves as an upper

bound for the expected errors, as the Monte Carlo is simulated for two independent resistors, with no matching techniques used.

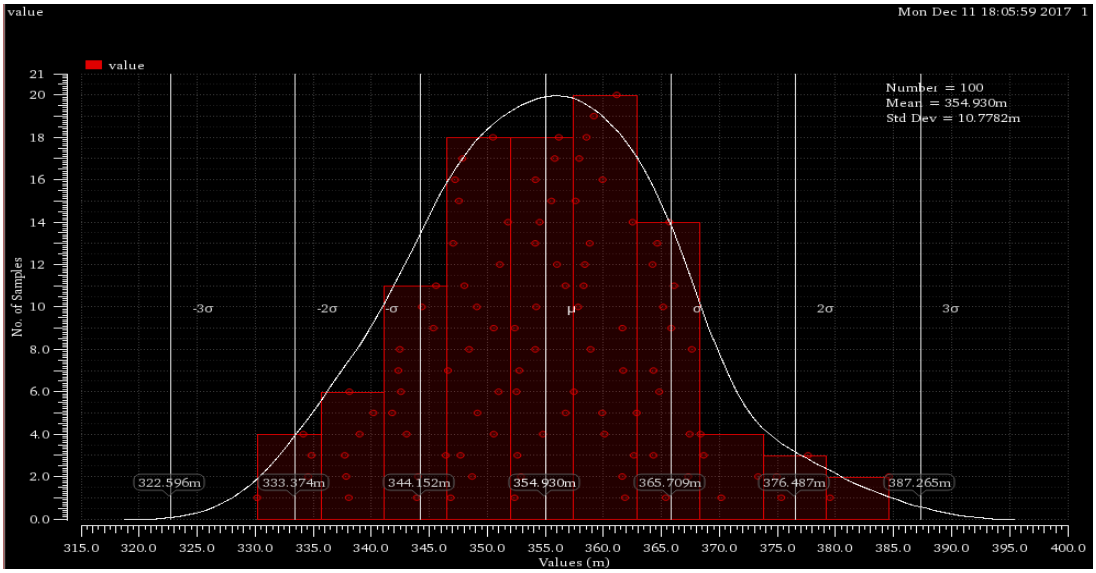


Figure 64. Worst Case Mismatch Error

As can be seen, the high end of the mismatch error results in a ~30mV change in output voltage. Thus, if the DAC is designed with a dynamic range with more than +/- 30mV extra dynamic range, no loss in resolution is expected. This dynamic range is, in fact, designed into the DAC, and as such Monte Carlo simulations confirm that no resolution is lost under small mismatched conditions.

To be able to maintain <1° resolution, the DAC must be able to sense the difference between the envelope detector's output at 1° increments. This sets a lower limit for the ENOB of the DAC. Specifically, the design aims for >36 quantizations over the dynamic range, as that allows for +/- 0.5° resolution. This corresponds to a minimum ENOB of approximately 5.2 bits.

Unlike most systems, there is actually an upper limit to the DAC resolution as well. The targeted application is WLAN, which has a carrier of 2.4GHz and a symbol rate of 20MHz. Thus there are 120 carrier pulses during each symbol. Since all the phase information in the digital pulse train is carried in the rising/falling edges, there are only 240 possible quantizations. This means any ENOB greater than 7.9 does not yield increased system performance. Realistically, the performance plateaus after only 6.9 ENOB as it is unlikely that the system can change a single edge without affecting its adjacent edge.

For this work, an 8 bit DAC is designed. This is significantly larger than what is needed for 36 quantizations. This extra resolution is implemented for two reasons. First, it allows some extra dynamic range to compensate for mismatch in the phase and envelope detectors. Secondly, it relaxes the specifications of the design. Realistically, the system should function within specification with an ENOB down to approximately 5-6 bits. By over designing the DAC by a factor of 2-3 bits, any small issues that arise from noise, non-linearity, layout, etc. can be disregarded. This DAC is implemented using a current steering topology as shown in Fig. 65.

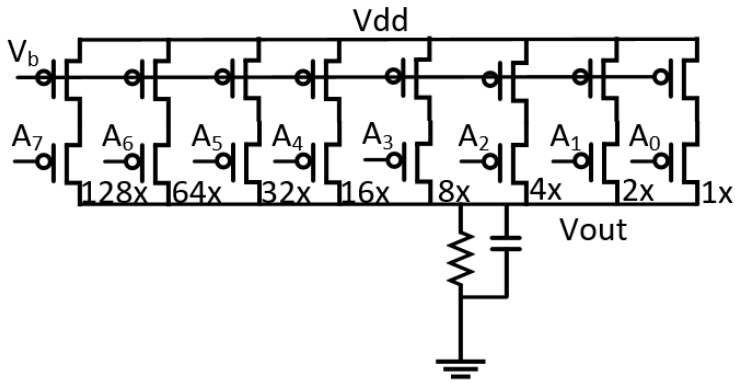


Figure 65. Current Steering DAC Topology

The comparator for this work has relatively relaxed specifications. It is desired that the circuit can detect voltage differences smaller than 1 LSB at as high of frequency as possible. However, the comparator serves to compare a ramp signal to a low frequency (effectively DC) signal. This ramp signal continues to increase until the comparator detects that it has surpassed the low frequency signal. Thus if the comparator offset prevents the detection of a small voltage difference, the ramp will continue to increase, thus pushing the difference above the offset level. While this changes the frequency at which the DSM switches, it does not change the overall duty cycle, so the resolution of the system does not suffer serious detriment.

The overall resolution, as limited by the comparator clocking is defined by the number of clocks that are present within each symbol. Similar to the upper limit of the DAC ENOB, a comparator clock frequency of greater than 2x the carrier frequency does not yield additional benefit. This is because each symbol only has 240 edges to contain phase information, so any clock samples above 240 will inevitably contain samples which contain no phase information. As stated before, it is difficult to change only one edge of the output signal without changing its adjacent edge as well due to glitches and other non-idealities. As such limited benefit is gained from clock frequency increases above ½ the carrier frequency. For this design, a clock frequency of approximately 1.6GHz (2/3 carrier) is chosen, but is adjustable over a wide range of frequencies. This adjustability will allow experimental verification of the upper and lower bounds qualitatively described in this section.

The comparator is designed using a standard latch based comparator [53] as shown in Fig. 66.

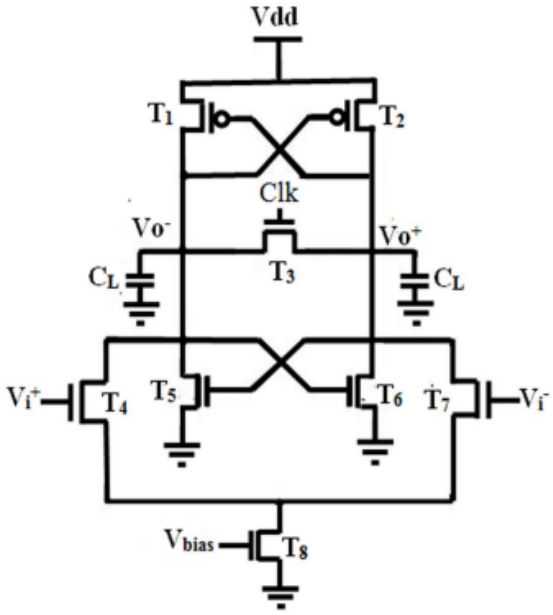


Figure 66. Latch Based Comparator

Unfortunately, this comparator does not work over the entire dynamic range of the DAC and envelope detector, as low DC values will de-bias the input pair. Ordinarily this would be fixed with traditional level shifters. But in this case, the previous stage relies on capacitive charge storage. This means that a traditional, low input impedance, level shifter would drain the capacitor and therefore not function correctly. To compensate for this, a PMOS input common source amplifier precedes each input pair, which maps the DC input levels to a DC range more conducive to the comparators operation (roughly 400-800mV). The PMOS gate input is a high impedance and can be lumped in with the previous stages output capacitance. There is some level of attenuation in these common source amplifiers, however since it is applied equally to both signals, it has a minimal effect on the operation aside from slightly exaggerating any offset errors, which has already been shown to be irrelevant to overall system functionality. These common source level shifters do need to be matched to one another, but this requires

relatively little effort, since there are only four devices, all of which are identical (aside from digital-ratio scaling) PMOS devices. Furthermore, small mismatches (on the order of a few %) will cause a static phase offset. While this is not a desirable condition, it does not necessarily reduce the resolution of the system, and can be largely mitigated in the output mapping calibration as described above.

The multiplexer in Fig. 52 (full system) is implemented with a standard digital mux preceded by a standard D flip flop. The flip flop is needed to prevent erroneous conditions at the output of the comparator from causing aberrant behavior in the switching of the output waveforms. Specifically, since the comparator has no hysteresis, it may oscillate if the DAC output voltage and the envelope detector output voltage are very similar. Clocking the output will prevent this oscillation from switching the output waveform rapidly, which could potentially cause unwanted noise or glitches to couple into the output waveform. Clocking the mux in this fashion also allows the researchers to independently test the effects of clocking speed on the phase accuracy and spectral characteristics. This allows the researchers to experimentally verify the mathematics used to formulate the DSM. After experimentation, the DSM clock can be adjusted and set as needed to meet required specifications. It is expected that this sampling clock will be independent of the PLL clock, meaning that no synchronization is required.

Monte Carlo simulations have been run for all devices that rely on matching. The system is designed in such a way that each block is tolerant of small device mismatches, and each block require matching minimal number of devices, which allows for high precision matching with minimal effort. The system has also been simulated across corners (SS and FF) and maintains all specifications under all conditions. Temperature is

not simulated in this work, since this system is very low power and is not expected to experience significant temperature fluctuations.

The digital solution is very similar to the analog solution. However, instead of measuring the output phase and comparing it to a reference, the digital solution simply switches the output multiplexer at a predetermined rate generated by a first order DSM. This architecture is shown in Fig. 7.

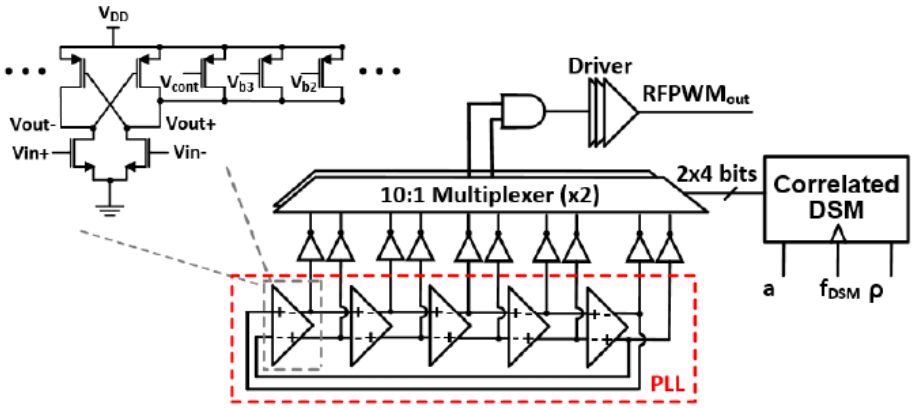


Figure 67. Open Loop Digital Implementation

The DSM block is a standard digital DSM, as shown in Fig. 8.

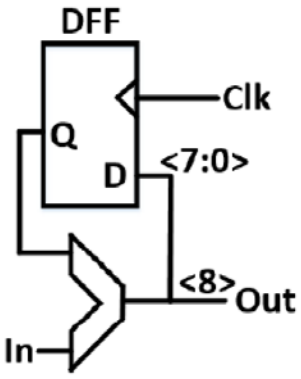


Figure 68. Simplified DSM Schematic

Because the digital implantation does not require the modulator to be in loop with the oscillator, nor contain analog components, it has a significantly improved PVT.

However, it does not have the jitter suppression mechanism that the analog implantation did via the output phase being measured. Fortunately, the experimental PLL discussed in chapter 4 worked extremely well, and generated integrated jitters on the order of 100s of fs. As such, there was not a significantly amount of jitter to be suppressed. Thus, the analog ceased to have any significant advantage over the digital implementation. Due to this, all results provided in the following section are solely for the digital implementation. The analog implementation yields similar results across the board, but requires significantly more calibration and bias signals, making a fair comparison difficult.

5.5. Results

The total power consumption of the presented circuit is approximately 23mW. Approximately 8.3mW and 4mW are consumed by the off-chip driver and frequency synthesizer respectively. This leaves a total of 10.4mW that is used by the delta sigma interpolator.

A plot of the achievable amplitudes from the DSM interpolator is included in Fig. 69.

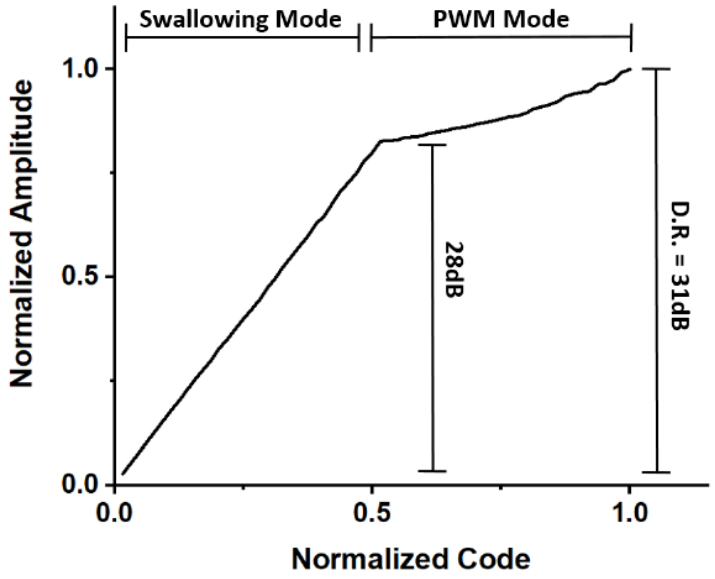


Figure 69. Amplitude Versus Input Code

As can be seen from the above figure, the swallowing mode is capable of extending the RFPWMs dynamic range by 28dB. In fact, there are an additional 16 dB of dynamic range that can be accomplished, however these datapoints are not included because they suffer from extremely high EVM and are therefore not suitable for use in a digital transmitter. Additionally, considering that the maximum output power is approximately 0dBm, the low end of the interpolators range (-47dBm) becomes increasingly difficult to measure accurately with the available lab equipment.

Furthermore, it can be seen in Fig. 69 that the swallowing mode demonstrates nearly perfect linearity. In fact, the measured linearity of this interpolation was below the measurement noise floor.

A plot of the spectrum resulting from a single tone transmission is included in Fig. 70. It can be seen that the output spectrum suffers from high spur levels, which is to be expected from a switching interpolator.

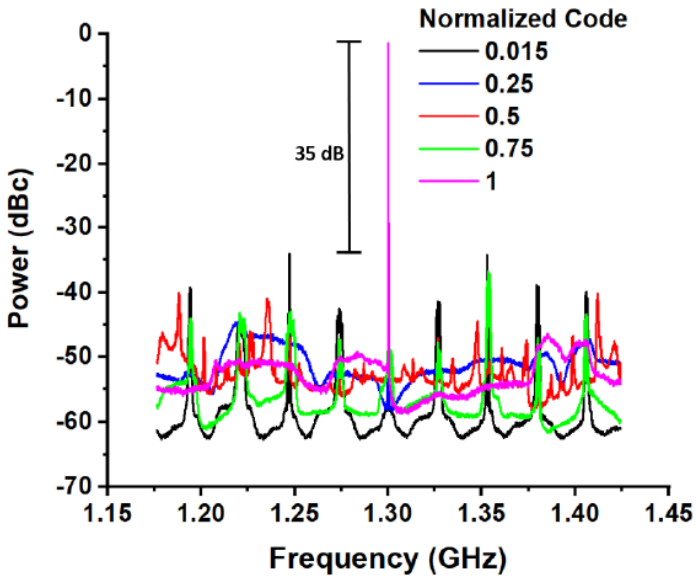


Figure 70. Single Tone Output Spectrum

The spacing of the spurs present in the output spectrum are dependent on the frequency of the DSM sampling, f_{DSM}. Specifically, it can be seen that no spurs occur within $\frac{\pm code_{max} \cdot f_{DSM}}{GCD(code, code_{max})}$, where $GCD(\cdot)$ represents the greatest common denominator function. This is true, so long as f_{DSM} does not exceed $\frac{f_{carrier}}{2}$, otherwise the frequencies will wrap around. This spacing prevents switching noise being superimposed on the passband of the signal. Furthermore, since this modulator is expected to be integrated with a downstream switch-mode power amplifier, it is assumed that the harmonic terminations/filtering at the output of the SMPA will take care of the far out spurs. If the spacing of the spurs too large for the intended bandwidth of the SMPAs output filtering, then the spurs can be pushed out further by truncating the DSM codes (setting LSBs to zero). The spacing will double for each LSB that is truncated, however the resolution of the interpolator will also be halved for each bit truncated. It is expected that the length of

the DSM code will be a design variable used by designers of future systems to optimize other design constraints such as filter quality factor.

A plot of the output spectrum when a 1Msym/s modulation is applied is included in Fig. 71. It should be noted that this plot also includes a raised cosine filter with $\beta = 0.3$ superimposed in post processing. This is because the transmitted data has no pulse shaping filter, and it is assumed that this will be added as part of the integration with the downstream SMPA. As can be seen, the spectrum shows minimal spreading. No additional DPD is needed to generate this spectrum. While the presented modulation circuits are capable of bandwidths in excess of 20MHz, the overall bandwidth is limited to less than 5MHz due to the SPI interface.

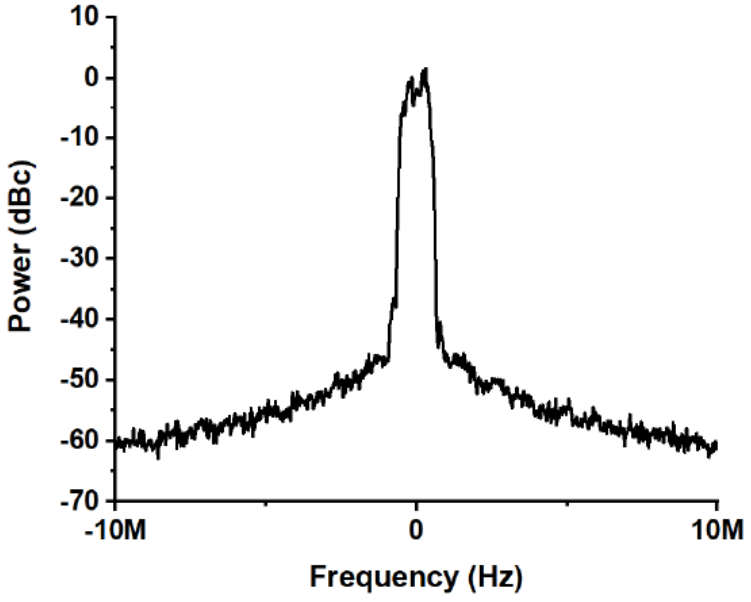


Figure 71. Output Spectrum with 1Msym/s Modulation

As can be seen, the presented circuit is has the largest ever reported dynamic range for a RFPWM system. This is done while maintaining state of the art specifications for power, area, frequency range, and EVM.

Due to measurement limitations, it was not possible to measure a full 64QAM demodulated constellation. However, a 16QAM constellation was able to be measured. The results are included in Fig. 72. The EVM of Fig. 72 is approximately -32.8, which is on par with state of the art publications.

Figure 38. Simulated constellation

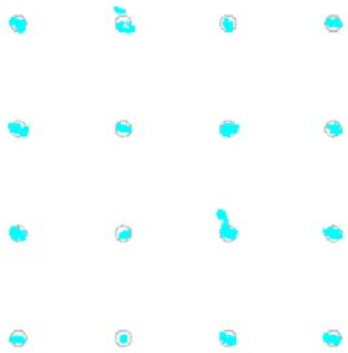


Figure 72. Measured Constellation

The EVM was also measured across swept carrier frequency. The results are shown in Fig. 73. As can be seen, the EVM is largely independent of the carrier frequency, which is to be expected as the DSM interpolation operation is theoretically independent of carrier frequency. These values are on par with the current state of the art, and are sufficient for most modern communications protocols.

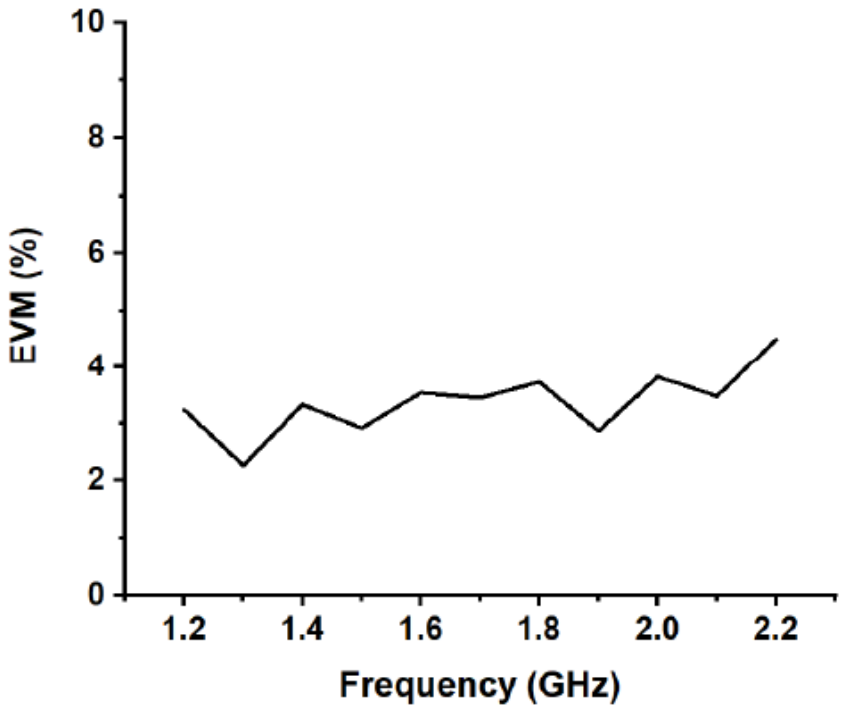


Figure 73. EVM vs. Frequency

A table of the measured results compared to prior art is presented in Table 11. As can be seen, the presented system has the largest dynamic range, smallest area, and lowest power consumption of other works in the area.

	[1]*	[4]	[5]	[6]	[3]	This Work
Technology	40nm	130nm	65nm	40nm	45nm	65nm
Topology	2-level RFPWM	Carrier Switching	3-level RFPWM	2-Level RFPWM	Delta-Sigma (PM only)	Delta-Sigma (AM & PM)
Dynamic Range (dB)	10.8†	23	6.4†	7.3†	0	31
Active Area (mm^2)	0.35	0.46	0.48	0.48	0.15	0.019
Frequency (GHz)	1-3	1.8-2.5	2.66	0.9-2.6	1-3	1.2-2.2
Spur Level (dBc)	-20	-28	Not Reported	Not Reported	-45	-35
EVM (dB)	-28	-25.5	-24.9	-29	-33.5	-32.8
Power (mW)	75	98	70	50	34	23

* All results specified for 1.2GHz † Peak to average power

Table 11. Comparison to Prior Art

5.6. Conclusion

It has been shown in this section that the presented circuit is capable of extending the dynamic range of a PWM based transmitter by 28dB. This is a sufficient dynamic range to transmit virtually any modern communication standard without any distortion issues. This solves one of the most important issues preventing the widespread adoption of digital transmitters for communications.

The lack of large number of interpolator elements allows the presented system to operate with extremely low area and power consumption. Additionally, since the interpolation is not done via device properties, it significantly reduces the potential for PVT sensitivity.

The presented dynamic range extension circuit is compatible with any digital pulsewidth modulation system, and therefore is interoperable with the circuits presented in Chapters 2-4.

CHAPTER 6

Conclusion

This work has shown four architectures that can be used in the development of wideband all digital polar transmitter systems. Each of these concepts addresses a specific issue that has prevented the widespread adoption of ADTs, specifically phase shifter's physical size constraints and frequency reconfigurability (Two-Point Phase Modulation), spurious emissions (Polyphase Harmonic Cancellation), high noise/EVM levels (sampled filter PLL), and limited dynamic range (Delta-Sigma Phase Interpolation). Additionally, each of the presented methods has a strong emphasis on reduced sensitivity to PVT and matching constraints. This emphasis allows for higher fabrication yield, increased ease/speed of design, and reduced verification and post-extraction requirements. The culmination of all of these techniques should allow an increased rate of industry adoption for ADTs.

REFERENCES

[1] S. Balasubramanian et al., “Ultimate transmission,” *IEEE Microwave Magazine*, vol. 13, no. 1, pp. 64-82, Jan. 2012.

[2] Grebennikov, N. Sokal and M. Franco, Switch-mode RF and microwave power amplifiers. Amsterdam: Elsevier/Academic Press, 2012.

[3] M. Nielsen and T. Larsen, "An RF Pulse Width Modulator for Switch-Mode Power Amplification of Varying Envelope Signals", *2007 Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, 2007.

[4] K. Grout, J. Kitchen, “Wideband Digital Wireless Transmitter Hardware for Controlling RF Switched-Mode Power Amplifiers” *Government Microelectronics Conference 2018*, 2018.

[5] P. Nuyts, P. Singerl, F. Dielacher, P. Reynaert and W. Dehaene, "A Fully Digital Delay Line Based GHz Range Multimode Transmitter Front-End in 65-nm CMOS", *IEEE Journal of Solid-State Circuits*, vol. 47, no. 7, pp. 1681-1692, 2012.

[6] A. Jerng and C. Sodini, "A Wideband ΔΣ Digital-RF Modulator for High Data Rate Transmitters", *IEEE Journal of Solid-State Circuits*, vol. 42, no. 8, pp. 1710-1722, 2007.

[7] J. Stauth and S. Sanders, "Pulse-density modulation for RF applications: The radio-frequency power amplifier (RF PA) as a power converter", *2008 IEEE Power Electronics Specialists Conference*, 2008.

[8] P. Nuyts, B. Francois, W. Dehaene and P. Reynaert, "A CMOS Burst-Mode Transmitter With Watt-Level RF PA and Flexible Fully Digital Front-End", *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 59, no. 10, pp. 613-617, 2012.

[9] J. McCue, B. Dupaix, L. Duncan, V. Patel, T. Quach and W. Khalil, "A time-interleaved multi-mode RF-DAC for direct digital-to-RF synthesis", *2015 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2015.

[10] J. McCue et al., "A Time-Interleaved Multimode RF-DAC for Direct Digital-to-RF Synthesis", *IEEE Journal of Solid-State Circuits*, vol. 51, no. 5, pp. 1109-1124, 2016.

[11] M. Mehrpoo, M. Hashemi, Y. Shen, R. van Leuken, M. Alavi and L. de Vreede, "A wideband linear direct digital RF modulator using harmonic rejection and I/Q-interleaving RF DACs", *2017 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2017.

[12] J. Xiao, et. al. “A 13-Bit 9GS/s RF DAC-based broadband transmitter in 28nm CMOS” *2013 IEEE Symposium on VLSI Circuits, 2013.*

[13] J. Walling et al., "A Class-E PA With Pulse-Width and Pulse-Position Modulation in 65 nm CMOS", *IEEE Journal of Solid-State Circuits*, vol. 44, no. 6, pp. 1668-1678, 2009.

[14] M. Park and M. Perrott, "A multiphase PWM RF modulator using a VCO-based opamp in 45nm CMOS", *2010 IEEE Radio Frequency Integrated Circuits Symposium*, 2010.

[15] B. Francois and P. Reynaert, "Reconfigurable RF PWM PA architecture for efficiency enhancement at power back-off", *2014 International Workshop on Integrated Nonlinear Microwave and Millimetre-wave Circuits (INMMiC)*, 2014.

[16] K. Cho and R. Gharpurey, "A Digitally Intensive Transmitter/PA Using RF-PWM With Carrier Switching in 130 nm CMOS", *IEEE Journal of Solid-State Circuits*, vol. 51, no. 5, pp. 1188-1199, 2016.

[17] H. Song and R. Gharpurey, "Digitally intensive transmitter employing RF pulse width modulation for IoT applications", *2015 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2015.

[18] S. Kulkarni, I. Kazi, D. Seebacher, P. Singerl, F. Dielacher, W. Dehaene and P. Reynaert, "Multi-standard wideband OFDM RF-PWM transmitter in 40nm CMOS", *ESSCIRC Conference 2015 - 41st European Solid-State Circuits Conference (ESSCIRC)*, 2015.

[19] P. Nuyts, P. Reynaert and W. Dehaene, Continuous-Time Digital Front-Ends for Multistandard Wireless Transmission. Springer, 2014.

[20] H. Song “VLSI Phased-Locked Loop Circuit Design” in Principles of VLSI Design 1st ed. [S.I.]: LULU COM, 2016. Pp331-344

[21] "3rd Generation Partnership Project; Technical Specification Group Radio Access Network; Evolved Universal Terrestrial Radio Access (E-UTRA); Base Station (BS) radio transmission and reception", 3GPP TS 36.104

[22] A. Azam, Z. Bai, W. Yuan, and J. S. Walling, "SCPA revolution: Linearization of multiphase SCPAs," in Proc. IEEE CICC, Austin, TX, USA, Apr. 2017, pp. 1–8.

[23] J. S. Walling and D. J. Allstot, "Linearizing CMOS switching power amplifiers using supply regulators," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 57, no. 9. pp. 497–501, Jul. 2010.

[24] R. Fano, "Theoretical limitations on the broadband matching of arbitrary impedances," *Journal of the Franklin Institute*, vol. 249, no. 1, pp. 57–83, 1950.

[25] K. Sessou and N. Neihart, "An Integrated 700–1200-MHz Class-F PA With Tunable Harmonic Terminations in 0.13-μm CMOS", *IEEE Transactions on Microwave Theory and Techniques*, vol. 63, no. 4, pp. 1315-1323, 2015.

[26] N. Kuo, B. Yang, C. Wu, L. Kong, A. Wang, M. Reiha, E. Alon, A. Niknejad and B. Nikolic, "A frequency-reconfigurable multi-standard 65nm CMOS digital transmitter with LTCC interposers", *2014 IEEE Asian Solid-State Circuits Conference (A-SSCC)*, 2014.

[29] W. Ye, K. Ma and K. Yeo, "2.5 A 2-to-6GHz Class-AB power amplifier with 28.4% PAE in 65nm CMOS supporting 256QAM", *2015 IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers*, 2015.

[30] J. Park, Y. Wang, S. Pellerano, C. Hull and H. Wang, "A CMOS Wideband Current-Mode Digital Polar Power Amplifier With Built-In AM–PM Distortion Self-Compensation", *IEEE Journal of Solid-State Circuits*, vol. 53, no. 2, pp. 340-356, 2018.

[31] A. Ba, et al, "A 2.4GHz class-D power amplifier with conduction angle calibration for –50dBc harmonic emissions," *IEEE Radio Frequency Integrated Circuits Symp*., pp. 239-242, June 2014.

[32] T. Sano et al., "13.4 A 6.3mW BLE transceiver embedded RX image-rejection filter and TX harmonic-suppression filter reusing on-chip matching network", *2015 IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers*, 2015.

[33] J. Fritzin, C. Svensson, and A. Alvandpour, "A class-D outphasing RF amplifier with harmonic suppression in 90 nm CMOS," *Proc. IEEE Eur. Solid-State Circuits Conf*., pp. 310–313, Sep 2010.

[34] J. A. Weldon, et al, "A 1.75-GHz highly integrated narrowband CMOS transmitter with harmonic-rejection mixers," *IEEE J. Solid-State Circuits*, vol. 36, no. 12, pp. 2003–2015, Dec. 2001.

[35] R. Shrestha, E. A. M. Klumperink, E. Mensink, G. J. M. Wienk, and B. Nauta, "A Polyphase Multipath Technique for Software-Defined Radio Transmitters," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 12, pp. 2681–2692, 2006.

[36] C. Huang, Y. Chen, T. Zhang, V. Sathe and J. Rudell, "A 40nm CMOS single-ended switch-capacitor harmonic-rejection power amplifier for ZigBee applications", *2016 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2016.

[37] S.-M. Yoo, B. Jann, O. Degani, J. C. Rudell, R. Sadhwani, J. S. Walling, and D. J. Allstot, "A class-G dual-supply switched-capacitor power amplifier in 65nm CMOS," *2012 IEEE Radio Frequency Integrated Circuits Symposium*, 2012.

[38] W. Yuan and J. S. Walling, "A multiphase switched capacitor power amplifier in 130nm CMOS," *2016 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2016.

[39] W. Yuan, V. Aparin, J. Dunworth, L. Seward, and J. S. Walling, "A quadrature switched capacitor power amplifier," *IEEE J. Solid-State Circuits*, vol. 51, no. 5, pp. 1200–1209, May 2016.

[40] M. S. Alavi, R. B. Staszewski, L. C. N. de Vreede, and J. R. Long, "A Wideband 2×13-bit all-digital I/Q RF-DAC," *IEEE Trans. Microw. Theory Tech*., vol. 62, no. 4, pp. 732–752, Apr. 2014.

[41] Z. Bai, W. Yuan, A. Azam, and J. S. Walling, ”A split-array, C-2C switched-capacitor power amplifier in 65nm CMOS,” *2017 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2017.

[42] S. Moallemi, K. Grout and J. Kitchen, "CMOS Power Drivers for Digital Transmitters: Challenges and Architectures," *Radio Wireless Week 2019*, 2019

[44] I. Sarkas, A. Balteanu, E. Dacquay, A. Tomkins, and S. Voinigescu, "A 45nm SOI CMOS Class-D mm-Wave PA with 10Vp-p differential swing", *2012 IEEE International Solid-State Circuits Conference*, 2012, pp. 88-90.

[45] H. Johansson, ”A simple precharged CMOS phase frequency detector”, *IEEE Journal of Solid-State Circuits*, vol. 33, no. 2, pp. 295-299, 1998.

[46] T. Seong, Y. Lee, S. Yoo, and J. Choi, “A −242-dB FOM and −71-dBc reference spur ring-VCO-based ultra-low-jitter switched-loop-filter PLL using a fast phase-error correction technique,” *2017 Symposium on VLSI Circuits*, 2017.

[47] H. Wang, O. Momeni, "A 9.6 mW Low-Noise Millimeter-Wave Sub-Sampling PLL with a Divider-less Sub-Sampling Lock Detector in 65 nm CMOS" *IEEE Radio Frequency Integrated Circuits Conference (RFIC)*, paper 3C-4, June 2019.

[48] Nuyts, P.A.J.; Reynaert, P.; Dehaene, W., "A fully digital PWM-based 1 to 3 GHz multistandard transmitter in 40-nm CMOS," *IEEE Radio Frequency Integrated Circuits Symposium (RFIC) 2013*, vol., no., pp.419,422, 2-4 June 2013.

[49] Ravi, A; et al., "A 2.4-GHz 20–40-MHz Channel WLAN Digital Outphasing Transmitter Utilizing a Delay-Based Wideband Phase Modulator in 32-nm CMOS," *IEEE J. Solid-State Circuits*, vol.47, no.12, pp.3184,3196, Dec. 2012

[50] H. Gheidi, T. Nakatani, V. Leung and P. Asbeck, "A 1–3 GHz Delta–Sigma-Based Closed-Loop Fully Digital Phase Modulator in 45-nm CMOS SOI", *IEEE Journal of Solid-State Circuits*, vol. 52, no. 5, pp. 1185-1195, 2017

[51] H. Gheidi, T. Nakatani, V. Leung, and P. M. Asbeck, “A wideband delta-sigma based closed-loop fully digital phase modulator in 45nm CMOS SOI,” *Proc. IEEE RFIC Symp.*, May 2016, pp. 158–161.

[52] J. Maneatis, "Low-jitter process-independent DLL and PLL based on self-biased techniques", *IEEE Journal of Solid-State Circuits*, vol. 31, no. 11, pp. 1723-1732, 1996.

[53] A. Majumder, M. Das, B. Nath, A. Mondal and B. Bhattacharyya, "Design of low noise high speed novel dynamic Analog Comparator in 65nm technology", *2016 26th International Conference Radioelektronika (RADIOELEKTRONIKA)*, 2016.

[54] V. Kroupa, Phase lock loops and frequency synthesis. Chichester: Wiley, 2005.

[55] J. Crawford, Advanced phase-lock techniques. London: Artech House, 2008.

APPENDIX A:

LIST OF PREVIOUS PUBLICATIONS

JOURNAL PUBLICATIONS

K. Grout, S. Moallemi and J. Kitchen, "Wideband Reconfigurable Switched Capacitor Power Amplifier Employing Polyphase Harmonic Cancellation", *IEEE Transactions on Circuits and Systems (TCAS I: Regular Papers)* [Submitted, in review]

K. Grout and J. Kitchen, "A RFPWM Modulator with 31dB Dynamic Range using Delta-Sigma Interpolation", *IEEE Transactions on Circuits and Systems (TCAS I: Regular Papers)* [To be submitted, October 2019]

K. Grout and J. Kitchen, "A Dividerless Ring Oscillator PLL with 250fs Integrated Jitter using Sampled Lowpass Filter", *IEEE Transactions on Circuits and Systems (TCAS II: Express Briefs)* [Submitted, in review]

S. Moallemi, P. Mehr, **K. Grout**, T Thornton and J. Kitchen, "Adaptive Power Control Using Current Adjustmentfor Watt-Level Power Amplifiers in CMOS SOI", *IEEE Transactions on Circuits and Systems (TCAS II: Express Briefs), 2019.*

CONFERENCE PUBLICATIONS

K. Grout and J. Kitchen, "Preservation of Phase Resolution with Wideband Integer-N Based Phase Modulators", *IEEE Radio Wireless Symposium (RWW)* 2020.

S. Moallemi, **K. Grout** and J. Kitchen, "CMOS Power Drivers for Digital Transmitters: Challenges and Architectures", *IEEE Radio Wireless Symposium (RWW)* 2019.

K. Grout and J. Kitchen, "Delta-Sigma based Polar Modulation Scheme for High PAPR Signals", *Government Microelectronics Conference (Gomac)* 2019.

K. Grout and J. Kitchen, "Wideband Digital Wireless Transmitter Hardware for Controlling RF Switched-Mode Power Amplifiers", *Government Microelectronics Conference (Gomac)* 2018.

K. Grout and J. Kitchen, "Analysis of Jitter on RFPWM Systems for All-Digital Transmitters", I*EEE 2018 Texas Symposium on Wireless and Microwave Circuits and Systems (WMCS)*, 2018.

S. Moallemi, **K. Grout** and J. Kitchen, "Transformer Based Power Combining for Outphasing Power Amplifiers", *IEEE 2018 Texas Symposium on Wireless and Microwave Circuits and Systems, 2018.*

WHITEPAPER PUBLICATIONS

K. Grout and J. Kitchen, "Use of Non-Reciprocal Devices for the Broadband Matching of Antennas", *National Science Foundation Proposal*, EECS Division, 2017.

PATENTS

K. Grout, "Correlated Delta-Sigma Interpolation for Dynamic Range Extension", Submitted to Skysong 2019

K. Grout, "Precharged PFD Utilizing Sampled Lowpass Filtering", Submitted to Skysong 2019

K. Grout, "Linearized Time Amplifier Architecture for Sub-Picosecond Resolution", United States Patent Pending 16415162, 2019

K. Grout, "Predictive Oversampling for PLL Bandwidth Extension", BAE SYSTEMS, Internal Trade Secret

APPENDIX B:

ALTERNATE PROOF OF RELATIVELY PRIME NUMBER RELATION

Uniformly quantized values within a cyclic space can be expressed as the set

$$\boldsymbol{\phi_{in}} = \{\mathbf{0}, \mathbf{1}, \mathbf{2}, \ldots \boldsymbol{k} - \mathbf{1}\},$$

Where $\boldsymbol{k}$ is the number of quantizations.

This set is the product of the cyclic abelian generator function

$$\boldsymbol{G} = <\boldsymbol{\phi}, *>$$

Such that the binary operator * is defined for arbitrary inputs $\boldsymbol{a}$ and $\boldsymbol{b}$ using the modulus function

$$\boldsymbol{a} * \boldsymbol{b} \equiv \boldsymbol{a^b} = (\boldsymbol{a} \cdot \boldsymbol{b}) \; \boldsymbol{mod} \; \boldsymbol{k}$$

A conversion function $\boldsymbol{F}$ can map the elements of group $\boldsymbol{G}$ to a group $\boldsymbol{H}$

$$\boldsymbol{F}: \boldsymbol{G} < \boldsymbol{\phi}, * > \rightarrow \boldsymbol{H} < \boldsymbol{\phi'}, * >$$

In the case of a scalar multiplication, $\boldsymbol{F}$ can be further expressed as

$$\boldsymbol{F}\big(\boldsymbol{\phi}(\boldsymbol{a})\big) = \boldsymbol{N} * \boldsymbol{\phi}(\boldsymbol{a})$$

For integer scalar $\boldsymbol{N}$ and arbitrary index $\boldsymbol{a}$ within the bounds of set $\boldsymbol{\phi}$.

Because $\boldsymbol{G}$ is an abelian group with closed binary operator, $\boldsymbol{H}$ must be a subgroup of $\boldsymbol{G}$.

Any subgroup $\boldsymbol{H}$ of a finite cyclic group $\boldsymbol{G}$ contains some element $\boldsymbol{b}$ if

$$\boldsymbol{H} = \{\boldsymbol{b^x} | \boldsymbol{x} \in \mathbf{Z}\}$$

Since $\boldsymbol{H}$ is generated by a mapping function acting on cyclic group $\boldsymbol{G}$, each element in $\boldsymbol{H}$ must be generated by some element, $\boldsymbol{a}$, in $\boldsymbol{G}$.

$$\boldsymbol{b} = \{\boldsymbol{a^s} | \boldsymbol{a} \in \boldsymbol{G}\}$$

For generator multiplier $\boldsymbol{s}$.

Because $\boldsymbol{N}$ was already defined as the generator multiplier, $\boldsymbol{N}$ can be substituted for $\boldsymbol{s}$.

Furthermore,

$$\boldsymbol{b^m = e \; iff \; (a^N)^m = e}$$

For some integer $\boldsymbol{m}$, where $\boldsymbol{e}$ represents the identity element of $\boldsymbol{G}$.

Since $\boldsymbol{H}$ is a cyclic subgroup of $\boldsymbol{G}$, and the result of m operating on $\boldsymbol{b}$ is identity, then $\boldsymbol{m}$ must be the order of the subgroup $\boldsymbol{H}$.

Since there are $\boldsymbol{k}$ elements in group $\boldsymbol{G}$, then

$$\boldsymbol{mk \; mod \; N = 0}.$$

If d is defined as the greatest common denominator of $\boldsymbol{N}$ and $\boldsymbol{k}$, then

$$\boldsymbol{d = uN + vk}$$

For some integers $\boldsymbol{u}$ and $\boldsymbol{v}$.

This yields the following identity

$$\boldsymbol{1 = u\left(\frac{N}{d}\right) + v(\frac{k}{d})}$$

Which implies that $\left(\frac{N}{d}\right)$ and $\left(\frac{k}{d}\right)$ are relatively prime.

Since

$$\boldsymbol{m\left(\frac{N}{d}\right) \; mod \; \left(\frac{k}{d}\right) = 0}$$

Then

$$\boldsymbol{m \; mod \; \left(\frac{k}{d}\right) = 0}$$

Thus

$$\boldsymbol{rem\left(\frac{ms}{k}\right) = 0}$$

By dividing top and bottom by $\boldsymbol{d}$, this can be rewritten as

$$\boldsymbol{rem\left(\frac{ms/d}{k/d}\right) = 0}$$

Since $\boldsymbol{H}$ must be the smallest subgroup of $\boldsymbol{G}$ containing $\boldsymbol{b}$, $\boldsymbol{H}$ must be the smallest order that fulfills these conditions. To minimize the order, $\boldsymbol{m}$ must be the smallest integer possible. Therefore

$$\boldsymbol{md/k = 1}$$

Which implies

$$\boldsymbol{m = k/d}$$

Thus the order of subgroup $\boldsymbol{H}$ is $\boldsymbol{k/d}$.

Therefore $\boldsymbol{F}$ is an isomorphic transform if and only if $\boldsymbol{d = 1}$.

As $\boldsymbol{d}$ is defined as the greatest common denominator of $\boldsymbol{N}$ and $\boldsymbol{k}$, then $\boldsymbol{F}$ is an isomorphic transform if and only if $\boldsymbol{N}$ and $\boldsymbol{k}$ are relatively prime. Otherwise, the order of $\boldsymbol{H}$ will be less than the order of $\boldsymbol{G}$, which implies F is a non 1:1 transform.

APPENDIX C:

DERIVATION OF DSM TRANSFER FUNCTION

It was shown in Chapter 1 that the amplitude of a RFPWM system is

$$\boldsymbol{A = \sin\left(\frac{\pi}{2} - \frac{\phi_1 - \phi_2}{2}\right)}.$$

And the phase is

$$\boldsymbol{\theta = \frac{\phi_1 + \phi_2}{2}}.$$

In the case of the DSM modulator discussed in Chapter 5, $\boldsymbol{\phi_1}$ and $\boldsymbol{\phi_2}$ can periodically be increased by 36°, or $\boldsymbol{\pi/5}$. In this case, variables $\boldsymbol{a_1}$and $\boldsymbol{a_2}$ can be defined that represent how often $\boldsymbol{\phi_1}$ and $\boldsymbol{\phi_2}$have a phase shift, normalized to 1. For example, a value of 0.5 for $\boldsymbol{a_1}$would imply that $\boldsymbol{\phi_1}$ would have a $\boldsymbol{\pi/5}$ shift imposed on it half of the time. By this definition, the average effective phase becomes

$$\boldsymbol{\theta = \frac{\phi_1 + \frac{(1 - a_1)\pi}{5} + \phi_2 + \frac{(1 - a_2)\pi}{5}}{2}}.$$

The amplitude is also affected by the phase modulation. If neither or both $\boldsymbol{\phi_1}$ and $\boldsymbol{\phi_2}$ have a shift added to them, then no change in amplitude occurs, yielding

$$\boldsymbol{A = \sin\left(\frac{\pi}{2} - \frac{\phi_1 - \phi_2}{2}\right)}.$$

However, if only one phase has a shift added to it, the amplitude becomes

$$\boldsymbol{A = \sin\left(\frac{\pi}{2} - \frac{\phi_1 + \frac{\pi}{5} - \phi_2}{2}\right)}.$$

Assuming $\boldsymbol{a_2}$ is zero, this would yield an effective average amplitude of

$$\boldsymbol{A = \sin\left(\frac{\pi}{2} - \frac{\phi_1 + (1 - a_1)\frac{\pi}{5} - \phi_2}{2}\right)}.$$

Substituting $\boldsymbol{a_2}$ for $\boldsymbol{a_1}$ would be the amplitude if $\boldsymbol{a_1}$ was fixed to 0 instead of $\boldsymbol{a_2}$.

However, there is no reason why one of the switching coefficients must be fixed to zero. A particularly useful case is when both $\boldsymbol{\phi_1}$ and $\boldsymbol{\phi_2}$ always have the same shift. In this case, the amplitude would again become

$$\boldsymbol{A = \sin\left(\frac{\pi}{2} - \frac{\phi_1 - \phi_2}{2}\right)}.$$

Since the pulsewidth is constant. However, the phase from such an arrangement would be

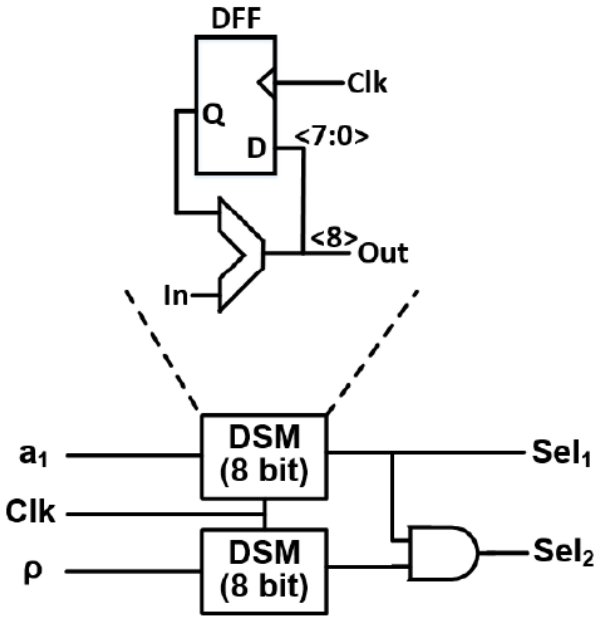
$$\boldsymbol{\theta = \frac{\phi_1 + \frac{2(1 - a_1)\pi}{5} + \phi_2}{2}}.$$

This indicates that the presented DSM architecture is capable of interpolating phase without affecting the amplitude.

However, the majority of the possible outcomes of the DSM system are where $\boldsymbol{a_1}$ and $\boldsymbol{a_2}$ are both non-zero, but not necessarily equal. To describe this type of situation, an additional variable, ρ, can be defined. a_2 can now be defined in terms of a_1 and ρ. In particular, a_2 is defined via the following algorithm

1. Set the output of the second DSM equal to the output of the first DSM
2. Override $(1 - \rho) \cdot 100\%$ of the second DSMs output's 1's with zeros

This algorithm can be easily accomplished via the circuit shown below.



With this algorithm for generating the select signals, the following amplitude will be generated

$$A = \sin\left(\frac{\pi}{2} - \frac{\phi_1 + \rho(1-a_1)\frac{\pi}{5} - \phi_2}{2}\right).$$

This can be seen as a weighted average between the amplitudes for when a_2 is fixed to zero and when a_2 is equal to a_1. Furthermore, the phase of such an arrangement would be

$$\theta = \theta'(1-a_1) + a_1(\theta' + \frac{\pi}{5}) \cdot (1-\rho) + a_1(\theta' + \frac{2\pi}{5}) \cdot (\rho)$$

Where θ' is defined as the nominal phase

$$\theta' = \frac{\phi_1 + \phi_2}{2}.$$

There is another region of interest in the transfer function. There exist some values of ϕ_1 and ϕ_2 such that there is a valid output, but that ϕ_1 and $\phi_2 - \pi/5$ would

yield a pulse that would be swallowed by downstream circuitry. This region of operation is referred in the body of this work as “swallowing mode” In this region, only pulses where neither or both phases are shifted yield an amplitude. When only one phase is shifted, the amplitude becomes zero. This yields an effective average amplitude is simply the amplitude of the valid pulse weighted by how often it happens. Specifically, when a_2 is set to zero ($\rho = 0$) then the amplitude can be expressed as

$$A = a_1 \sin\left(\frac{\pi}{2} - \frac{\phi_1 + \frac{\pi}{5} - \phi_2}{2}\right).$$

Which is completely linear due to the a_1 term moving to the front of the expression. Thus the presented system can generate waveforms with arbitrarily large linear dynamic ranges, limited solely by the minimum value of a_1, which is defined by the length of the DSM being used to modulate the phase. However, bandwidth and EVM limitations will put practical limits on the bounds of the dynamic range.