Energy-Detecting Receivers for Wake-Up Radio Applications

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Abstract

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In an energy-limited wireless sensor node application, the main transceiver for communication has to operate in deep sleep mode when inactive to prolong the node battery lifetime. Wake-up is among the most efficient scheme which uses an always ON low-power receiver called the wake-up receiver to turn ON the main receiver when required. Energy-detecting receivers are the best fit for such low power operations. This thesis discusses the energy-detecting receiver design; challenges; techniques to enhance sensitivity, selectivity; and multi-access operation.

Self-mixers instead of the conventional envelope detectors are proposed and proved to be optimal for signal detection in these energy-detection receivers. A fully integrated wake-up receiver using the self-mixer in 65 nm LP CMOS technology has a sensitivity of -79.1 dBm at 434 MHz. With scaling, time-encoded signal processing leveraging switching speeds have become attractive. Baseband circuits employing time-encoded matched filter and comparator with DC offset compensation loop are used to operate the receiver at 420 pW power. Another prototype at 1.016 GHz is sensitive to -74 dBm signal while consuming 470 pW. The proposed architecture has 8 dB better sensitivity at 10 dB lower power consumption across receiver prototypes.

Sensitivity and selectivity in an energy-detector first architecture is limited by characteristics of the front-end matching network. Further enhancement in sensitivity is proposed using the concept of interferer as LO, effectively operating as a direct down-conversion receiver. A wake-up receiver prototype in 0.13 μm CMOS operates at 550 MHz, consumes 220 nW from 0.5 V, and achieves a sensitivity of -56.4 dBm at a 400 kb/s chip rate using an 11-bit wake-up code. When a large interferer is present, the receiver operates in an interferer-enhanced mode, leveraging the interferer as a local oscillator to improve the sensitivity; in the presence of a -43.5 dBm interferer, a -63.6 dBm

sensitivity is achieved while consuming 1.1 μW. The architecture has 10 dB better selectivity for PM/FM interferer, but still gets blocked in the presence of a wide-band AM interferer.

Next, we propose a clockless continuous-time analog correlator to enhance the selectivity to such wide-band AM interferers. The architecture uses pulse-position-encoded analog signal processing with VCOs as integrators and pulse-controlled relaxation delays; it operates as a code-domain matched filter to de-spread asynchronous wake-up codes. A correlator prototype is designed in 65 nm LP CMOS technology, consumes 37 nW from 0.54 V, and performs code-domain filtering for an 11-bit Barker code. The receiver has -80.9 dBm sensitivity at 40 nW power consumption. A 5 dB improved selectivity to AM interference thanks to the correlator is demonstrated. This code-domain matched filtering also provides selectivity to unwanted codes to enable code-division multiple access (CDMA). A selective response to two different codes is presented, demonstrating CDMA for wake-up receivers.

Further enhancement in the link can be achieved using directional antennas, providing spatial gain and selectivity. However, increasing antenna directivity requires a high antenna aperture which is infeasible. Certain applications can leverage a nearby reflector to enhance the directivity. A proof-of-concept directional backscatter tag is proposed to act as a reflector. The tag uses multiple antennas acting as a reflectarray by configuring constant phase gradients depending on the direction of arrival (DoA) of the signal. The DoA is determined using RSSI measurements across different tag reflection configuration. A directional backscatter tag using a 3x3 antenna array with passive loads is implemented. It provides a 19 dB sensitivity enhancement resulting in an up to 3x increase in range compared to backscatter communications with a single antenna tag. This almost-passive tag can operate as a reflectarray for the wake-up receiver to enhance the link.

To sum up, scavenging energy has been studied widely for battery-less applications. However, the same energy and surrounding environment can be leveraged to enhance functionality (e.g. interferer as LO, using a reflector on a wall) to enhance low power operation. Innovations spanning both circuit and system architectures that leverage the ambient energy and environment to enable power-efficient solutions for next-generation wake-up radios are presented in this work.

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Chapter 1: Introduction

Remote sensors and devices will outnumber smartphones, accounting for more than half of all internet-connected things by 2020 [1]. The potential applications include smart factories and warehouses, smart homes, wearable health devices, smart cars, smart grids, and smart cities (Fig. 1.1). The requirements for these sensors such as battery life, bandwidth, radio range can vary across different applications. Most of the applications require these sensors and devices to be off the power grid, instead depending on batteries or harvested energy. With number of nodes predicted to rise orders of magnitude higher than smartphones, frequent maintenance including battery replacement is infeasible [2]. Thus, the devices need to be extremely energy efficient to extend the lifetime of these sensors.

A key hurdle is to sustain a wireless link with such sensors. Communication to the nodes can be power consuming to the order of $10's$ of mWs. E.g. a WiFi module consumes 3 mW [3] in standby mode, 214 mW in active receive mode and 660 mW in TX mode at 18 dBm transmit power. The corresponding receiver has a sensitivity of -98 dBm at 1 Mbps data rate. Similarly, a Bluetooth module consumes 29 mW in active receive mode, and 54 mW in active transmit mode at 3 dBm transmit power [4]. The receiver has a sensitivity of -92 dBm at 1 Mbps data rate. Here, a wake-up radio can serve as an important tool to substantially reduce the remote device power consumption and extend its battery life.

1.1 Wake-Up Radio

Wake-up is among the most efficient scheme which uses an always ON low-power receiver called the wake-up receiver to turn ON the main receiver when needed. The communication protocol is shown in Fig. 1.2. The sensor node has an always ON wake-up receiver, triggered by a

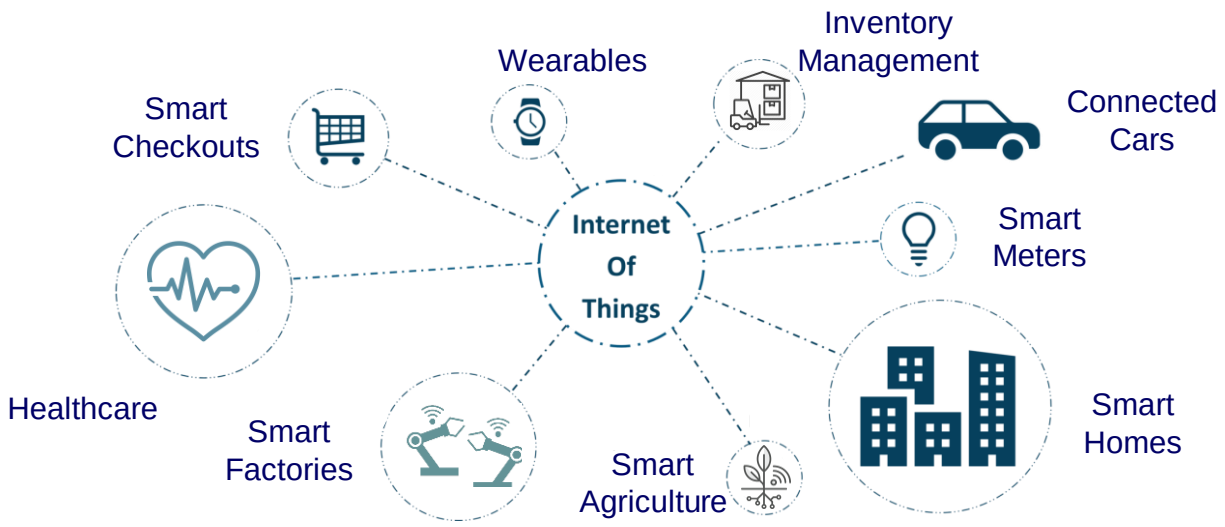


Figure 1.1: Different applications of a wake-up radio.

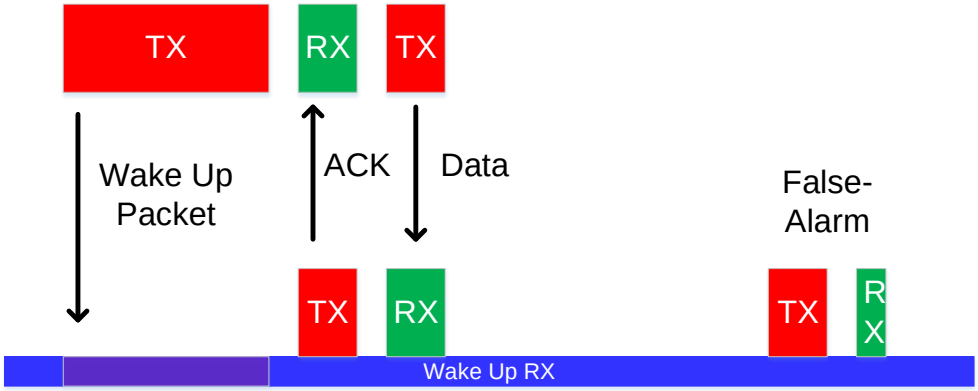


Figure 1.2: A generic wake-up radio communication protocol.

defined wake-up signature. Upon detecting the signature, the sensor node acknowledges the signal (ACK) and then turns ON the main receiver for receiving the data.

Message intervals vary for different applications and range from 24 hours to 10 minutes [1]. If a Bluetooth TX/RX is considered with a wake-up receiver, 100 bytes of data at 1 Mbps can be transmitted/received every hour at an average power consumption of 10 nW. Thus, the power consumption of the sensor node using a Bluetooth module can be reduced in the range of 60 nW to 500 pW depending on the desired message intervals. Next we discuss the key metrics for the design of a wake-up receiver and their impact on the system performance.

1.1.1 Wake-Up Latency

Wake-up receivers are generally designed to receive a desired signature for reliability. A typical 4-byte wake-up packet is described in [5] consisting of a 1-byte start frame, a 1-byte start sequence and a 2-byte ID. Wake-up latency can be $1-10$ msec for critical application like factory automation [6] or $0.1-1$ sec for a less-critical application like smart homes and warehouse. This leads to a minimum desired data-rate of 32 Hz to 32 kHz for a wake-up receiver depending on the application of interest.

1.1.2 False-Alarm Rate

Wake-up receivers should be designed to only trigger when a certain code is received. In worst scenario, the random noise in the receiver can lead to a received code, which is the same as a desired code. This leads to a false trigger since no such code was actually transmitted. This is known as a false alarm. It results in an unwanted TX and RX active time leading to a waste of power. In the event of a false wake-up, the main receiver then detects the absence of a frame and turns off. Typically the wake-up receiver should be designed for a false-alarm rate much less than the message rate for a sensor node. For a false-alarm rate of 1/Hr, 2-byte ACK and 2-byte RX using a Bluetooth module results in 370 pW of average power consumption. An even stringent power requirement would require a design for lower false-alarm rate or lower power consumption from the main transceiver.

1.1.3 Battery Lifetime

Sensor nodes are required to have at-least 10 years of lifetime without battery replacement, thus requires sufficient charge. Several applications can leverage ambient energy to recharge. A detailed survey was performed in [7] using credit-card sized solar cells in indoor settings. A typical available light energy of 1.1-2.9 J/cm^2/day was measured; assuming a 1% conversion efficiency, the available power is 1.3 $\mu W/cm^2$. Thus, an 80 μm x 80 μm photodiode can provide 6 nW power in an illuminated indoor light setting [8].

However, application like wireless implants in a human body might not allow the use of a battery or a photodiode. Energy harvesting through blood sugar is proposed in [9] for such applications. Energy in a single grain of sugar is enough to provide 6nW of power for a month.

Still, several deployment scenarios don't allow for recharge. High energy density *mm*-scale batteries have been an active area of research recently. A 2 mm Lithium-ion battery is proposed in [10]. Flexible and bio-compatible 2.25 mm x 1.7 mm Lithium-ion battery has been proposed in [11] with an energy density of 200 mWHr/cm^3. This *mm*-scale battery can provide 6 nW power for 10 years. Thus, different sources of energy for harvesting or battery operation can be used based on the environment where the node is being deployed.

1.1.4 Form Factor

Sensor nodes can vary in size, a credit-card size node might be feasible in a warehouse, but not on a key tracker. A small node requires higher operating frequency for a good air-to-antenna interface, e.g. a 5 cm, short-stub, electrically-small PCB antenna at 433 MHz has a peak antenna gain of −12.5 dBi [12], whereas, the corresponding gain for a 7 cm, long, folded-dipole antenna at 915 MHz is 0 dBi. The 2.4 GHz RF antennas used in [3] is 1.7 cm in length. For an even smaller form factor, the desired operating frequency need to be 5 GHz or even higher.

1.1.5 Range

A small form factor needs operation at higher frequency, but that comes at the cost of range. A 100 m free-space range has a 65 dB or 72 dB path loss at 433 MHz or 915 MHz. Assuming a 20 dBm transmit power, which satisfies TX power regulations for US and Europe in the ISM bands, the required receiver sensitivity for 915 MHz operation is −52 dBm. Non-ideal environment and multi-path fading affects the link, further path loss increases with increasing operation frequency. A −84 dBm sensitivity is required from the wake-up receiver to satisfy the requirements for WiFi [1].

Thus, different application requirements pose several constraints on the design as discussed above. Next, we discuss different RF wake-up receiver architectures and their performance trade-

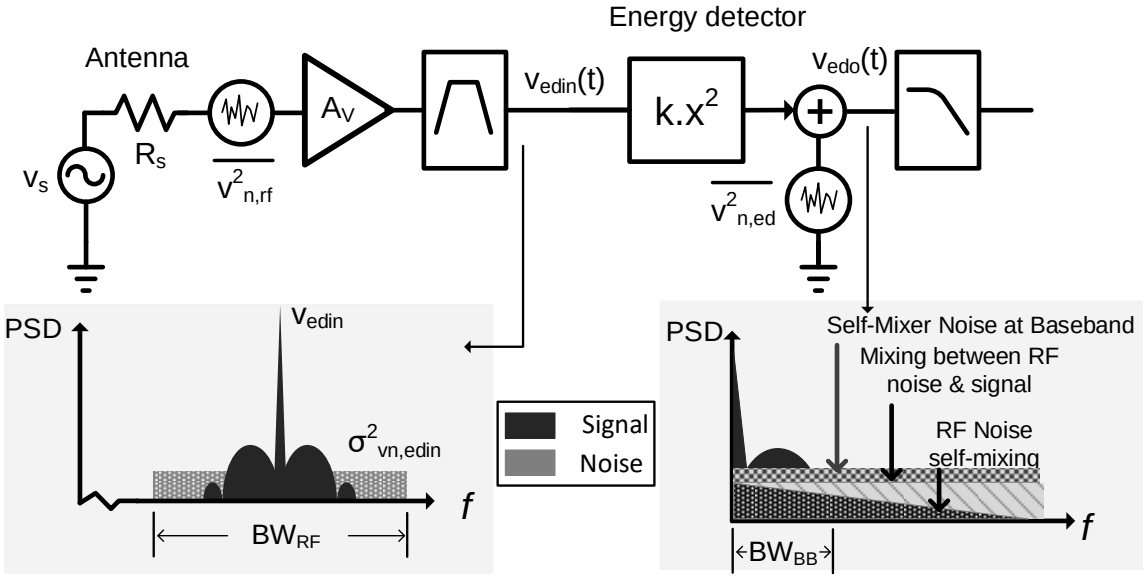


Figure 1.3: Noise contributions in energy-detector based wake-up receivers.

offs to satisfy the requirements.

1.2 Architectures for Sub-μW Radios

Conventional receivers including the direct down-conversion receiver can provide excellent selectivity and sensitivity, but at the cost of a power hungry local oscillator(LO). Direct down-conversion receiver architectures have been modified in prior works [13, 14] to reduce the power consumption, but they still consume $> 50\,\mu$W, largely due to the requirement of a crystal oscillator for frequency reference.

In the absence of an accurate local oscillator, several receiver architectures have been proposed, using a non-linear energy detector to down-convert the RF signal to baseband frequency. A generic block-diagram of an energy-detector based wake-up receiver is shown in Fig. 1.3 with noise contributions in the receiver. The receiver receives the signal from the antenna, with RF amplification A_v, followed by a filter with RF bandwidth BW_{RF}. The output of the filter is fed to an energy-detector to down-convert the RF signal to baseband.

The noise sources in the receiver architecture are also shown in Fig. 1.3. The noise from the antenna is filtered through the RF filter and fed to the energy detector. Due to the non-linear nature of the energy detector, the noise mixes with itself and appears at baseband, the noise also mixes with the input signal and appears as noise at baseband. A low RF bandwidth BR_{RF} is required to suppress the self-mixed noise from the antenna [15]. Noise is also added by the energy detector at the output. To suppress this noise, a high A_v is required from the RF front end.

These trade-offs lead to different receiver architectures shown in Fig. 1.4. An uncertain-LO receiver architecture (Fig. 1.4(a)) is proposed in [16] to mitigate the requirement of a crystal oscillator, however the ring oscillator still consumes 10's of μWs. The power consumption depends on the carrier frequency and the parasitic capacitance in different technology nodes. An energy-detection receiver with active-RF amplification using shifted limiters has been proposed in [17], but consumes $> 100\,\mu$W. Hence, RF amplification or local-oscillator (LO) generation consumes power of the order of $100\,\mu$W. This can be reduced to 100 nWs by duty-cycling the RF front end (Fig. 1.4(b)). Duty-cycled-RF front end with LO generation is explored in [18]. Duty-cycled-RF amplification is proposed in [19]. The corresponding trade-offs are explored in Section 1.2.1.

RF amplification or LO generation is difficult below 100 nW of power even with duty cycling at a reasonable latency of $\leq$1 sec, here passive RF front end with active energy detector (Section 1.2.2) or passive energy detector (Section 1.2.2) can be used when power consumption less than 10 nW is desired. Here, the sensitivity is limited by the noise from the energy detector due to the limited passive-RF gain available. Passive-RF front end with passive energy detectors (Fig. 1.4(c)) provide better signal-to-noise ratio(SNR) w.r.t. the active energy detectors (Fig. 1.4(d)) at low power, thus, they provide better sensitivity. Further, a pulsed input signal similar to the power-optimized waveforms (POW) used in [20] can improve the sensitivity for passive-RF ED-first wake-up receivers at the cost of higher power consumption and transmitter complexity. This is explored in Section 1.2.2.

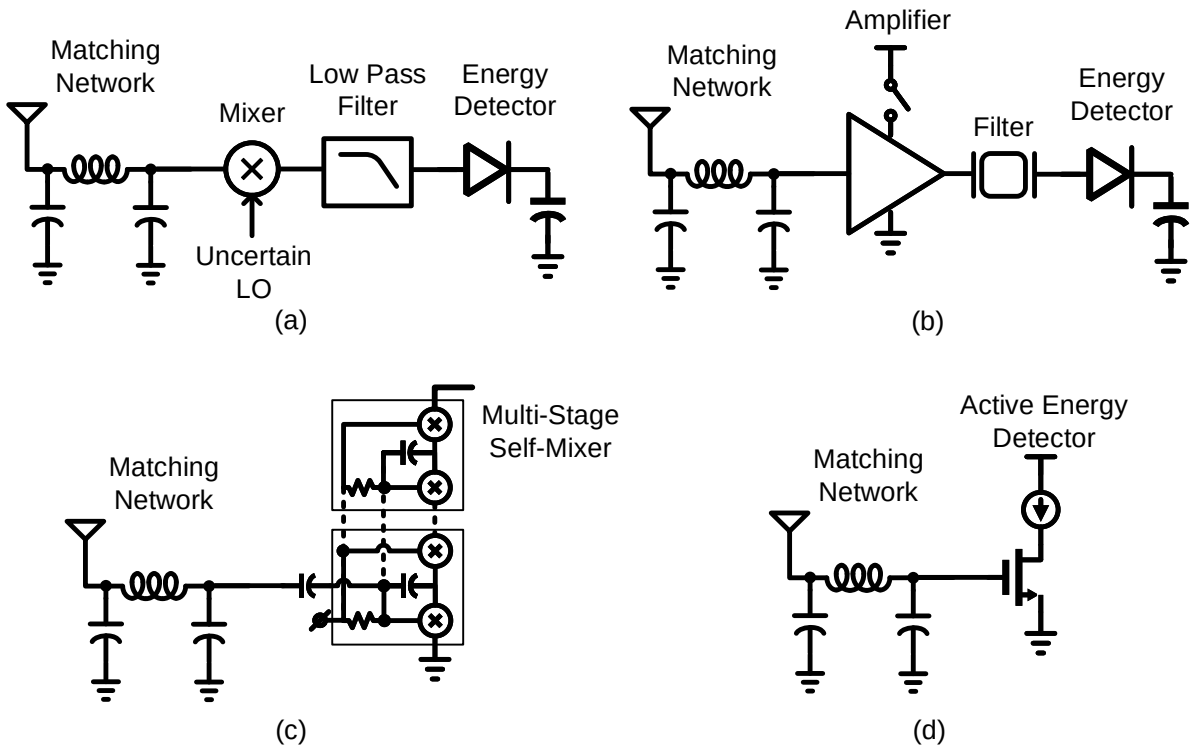


Figure 1.4: Wake-Up receiver RF front-ends using (a) an uncertain LO architecture; (b) a duty-cycled Active RF; (c) passive energy detector; and (d) an active energy detector.

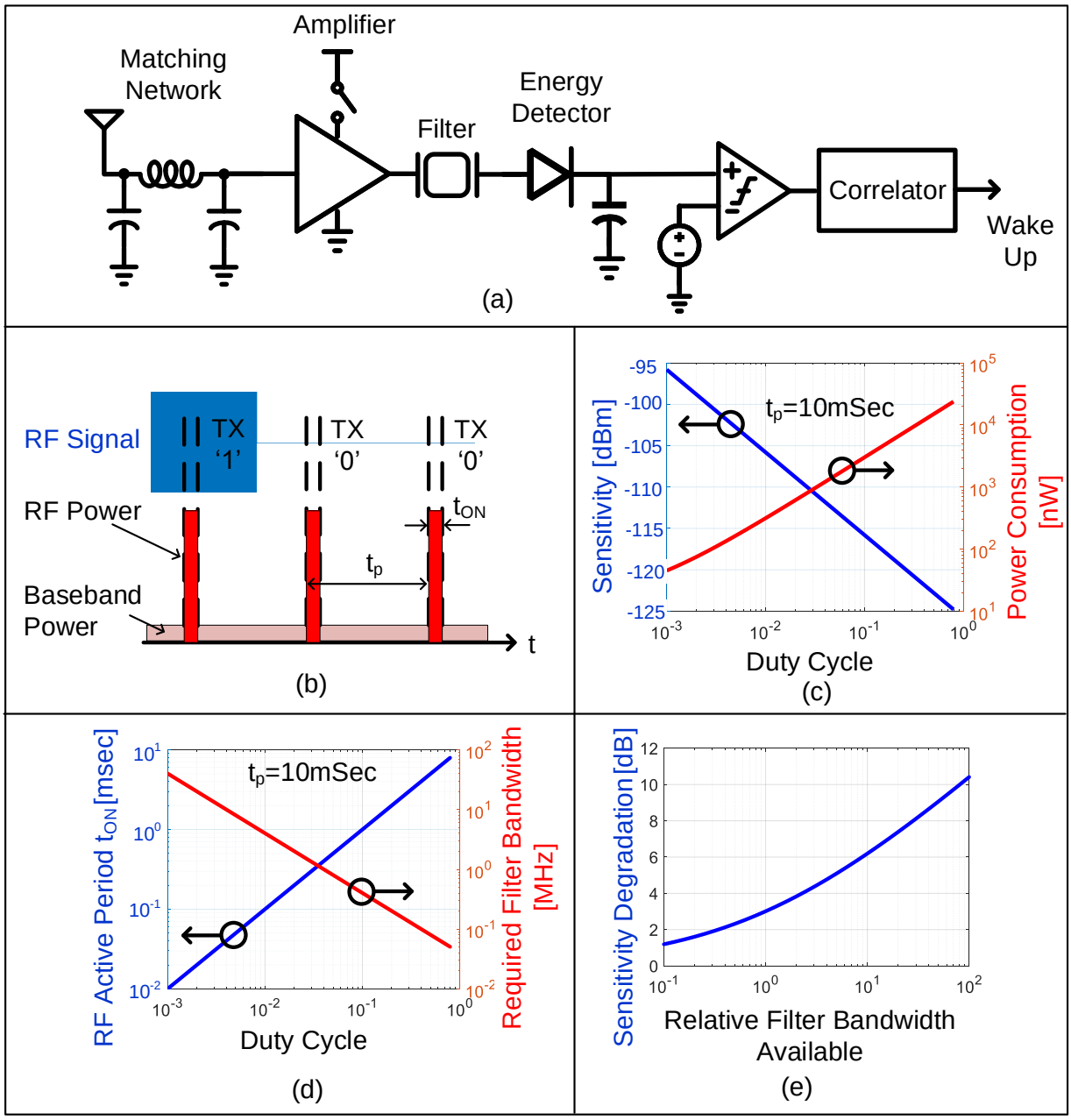


Figure 1.5: (a) A receiver architecture using a duty-cycled active RF amplification [19], (b) the operation principle and the power consumption profile for the receiver, (c) sensitivity and power consumption trade-off based on duty-cycle ratio t_{ON}/t_p assuming a very low RF front-end bandwidth BW_{RF}, (d) the required front-end RF filter bandwidth for a 3-dB degradation in sensitivity, and (e) the sensitivity degradation based on the excess RF filter bandwidth.

1.2.1 Duty-Cycled Active RF Amplifier

RF amplification consumes 100 μW of power at 900 MHz [21]. To reduce this power consumption, the amplifier can be duty cycled $1000x$ at bit-level to reduce the effective power consumption to 100 nW. Fig. 1.5(a) shows the receiver architecture proposed in [19]. The power consumption profile for the receiver is plotted in Fig. 1.5(b). Here, the RF amplifier is turned on for a period t_{ON} at an interval of time t_p (the bit period of the desired signal). This results in the amplifier duty-cycle ratio of t_{ON}/t_p.

Assuming that the RF filter bandwidth BW_{RF} is sufficiently low such that the noise mixed with the input signal dominates, the sensitivity for the receiver can be written as [15]:

$$P_{sens} = 8.k_B.T.NF.SNR_{min}/t_{ON} \tag{1.1}$$

where k_B is the Boltzmann constant, T is the absolute temperature, NF is the front-end amplifier noise factor and SNR_{min} is the minimum required SNR for successful signal demodulation. Assuming that the amplifier consumes P_{RF}, the power consumption is $P_{RF}t_{ON}/t_p$. The corresponding power and sensitivity trade-off with varying duty-cycle for $SNR_{req} = 12.4$ dB for an 11-bit code, $t_p = 10$ msec, $P_{RF} = 30\,\mu$W and $NF = 5$ dB is plotted in Fig. 1.5(c). The receiver can provide a sensitivity of -96 dBm at a power consumption of 30 nW for a latency of 110 msec for $t_{ON} = 10\,\mu$sec.

The receiver has a 3 dB degdaration in sensitivity when the RF filter bandwidth is such that the self-mixed noise from the RF front end is equal to the noise mixed with the input signal. This RF filter bandwidth is plotted in Fig. 1.5(d). The filter bandwidth required using expressions in [15] is $16.SNR_{req}/t_{ON}$, this requirement gets more stringent with higher duty cycle, and is not dependent on the RF carrier frequency. For a poorer filter available, the sensitivity degradation with increasing filter bandwidth relative to the desired bandwidth is plotted in Fig. 1.5(e).

Preamble Sampling

An alternative to bit-level duty cycled receiver is preamble sampling. Here, the receiver is duty cycled for detecting the preamble. Upon detection of the preamble, the receiver is turned on for a defined period to receive the wake-up code. A wake-up receiver with preamble sampling is proposed in [18] consuming 17 nW at −80 dBm sensitivity with a latency of 5 sec. The corresponding power consumption for a latency of 110 msec is 770 nW.

Thus, active RF front-end even with duty-cycling still consumes at-least 30 nW of power for less than 1 sec latency. The receiver architecture is best for battery operation, operation on a solar cell etc. where 100 nWs of power is easily available. Further reduction in power consumption and operation at higher carrier frequency will require operation in advanced technology nodes with higher f_T and high-Q inductors for tuned-RF amplification.

1.2.2 Passive RF Energy-Detecting Receivers

Energy-detecting (ED) receivers with a passive RF front end are promising for power consumption ≤10 nW. Most ED receivers consuming < 10 nW are implemented using an RF matching network to provide the passive gain A_v followed by an energy detector (Fig. 1.4(a,b)) [22, 23]. Here, the baseband signal processing can consume power less than 10 nW, and can even reduce to 10's of pWs depending on the required functionality. Dependence on the non-linearity of the transistor leads to poor sensitivity for such ED receivers [22]. Due to relaxed latency constraints for wake-up receivers, by exploiting the latency-sensitivity trade-off, ED receiver sensitivity has been improved in [24, 23, 25]. However, these implementations have optimum sensitivity for RF carrier frequencies less than 200 MHz, which are not suitable for the small form-factor nodes desired in ubiquitous deployment.

Energy detectors can be implemented using active or passive transistors. Active energy detectors using non-linearity of a common-source amplifier is used in [26, 24], however the sensitivity suffers due to the flicker noise and a poor conversion gain at low power. The trade-offs for active energy-detector based receivers are in Section 1.2.2. On the contrary, passive rectifiers with diode-

connected transistors are used to implement passive energy detectors. These perform better than the active counterparts due to the absence of flicker noise [23, 27].

Passive RF Front-End with Passive ED

The RF front-end for our proposed wake-up receiver architecture in [28] is shown in Fig. 1.6(a). Generally, it is assumed that zero-V_{TH} devices are required for achieving good conversion gain in diode rectifiers. This is a valid assumption for cold-startup in energy harvesting applications. This work proposes self-mixers in Chapter 3 as an alternative to mitigate the requirement with nominal power consumption. Further, the proposed self-mixers serve as an optimal energy detector for wake-up receivers to optimize sensitivity. The sensitivity trade-offs for this receiver is evaluated in Chapter 3 as well.

Here, we assume that the front-end passive gain is limited by the quality factor of the inductor Q_{ind} with an inductance of $L_{ind} = 1/(\omega^2 C_{in})$ is available, where ω is the RF angular frequency and C_{in} is the matching network load capacitance. The achievable sensitivity is evaluated in Chapter 3 and can be written as:

$$P_{sens}^2 = \frac{4k_B T R_{in,opt} SNR_{min}}{A_v^4 k_{ed}^2 R_s^2 t_p}. \tag{1.2}$$

where t_p is the bit period, $R_{in,opt} = Q_{ind}/(\omega C_{in})$, and $A_v = \sqrt{R_{in,opt}/(2R_s)}$.

The achievable sensitivity as a function of Q_{ind} at different RF frequencies for 100 bps data-rate with 110 msec latency, $SNR_{req} = 12.4$ dB is plotted in Fig. 1.6(b) for $C_{in} = 1$ pF. A -84 dBm sensitivity can be achieved for a 433 MHz operation for an inductor with a $Q_{ind} = 100$. The corresponding improvement in sensitivity for a reduced C_{in} at 2.4 GHz is shown in Fig. 1.6(c), again assuming an inductor with $L_{ind} = 1/(\omega^2 C_{in})$ and the desired Q_{ind} is available.

Thus the sensitivity is largely limited by the quality of the front-end matching network, it cannot be improved significantly for a similar latency.

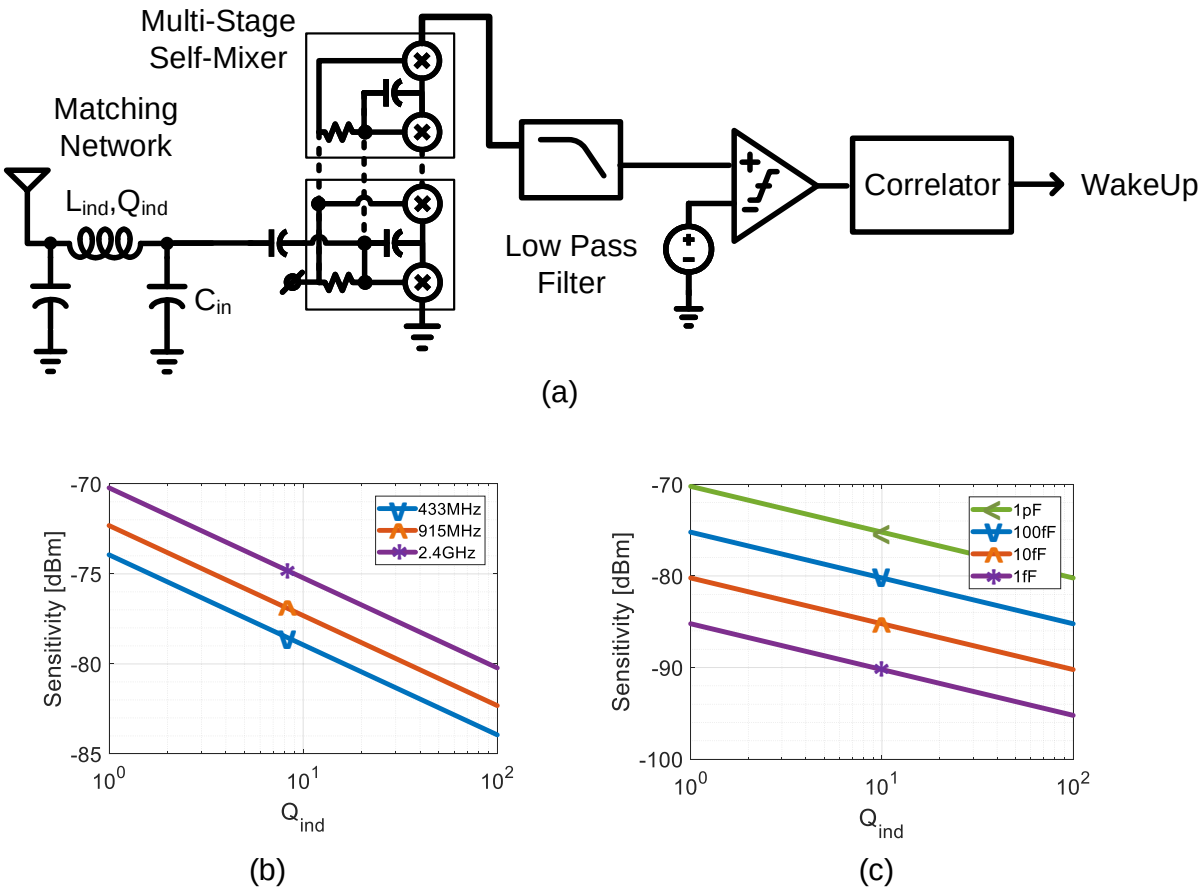


Figure 1.6: (a) Passive-RF energy-detecting receiver architecture using a self-mixer, (b) achievable sensitivity at different ISM band frequencies with increasing quality factor Q_{ind}, and (c) achievable sensitivity at 2.4 GHz with increasing quality factor Q_{ind} across different matching network load capacitors.

Pulsed Input Signal with Passive ED

Sensitivity is defined by the average incident power required to wake up a receiver. The power-optimized waveforms [20] carry most of the power in a small time window t_{pulse} for a bit-period t_p (Fig. 1.7(b)). The optimal receiver architecture to receive such a signal is shown in Fig. 1.7(a). Since the passive ED is non-linear, the RF to baseband conversion efficiency improves for a high peak-to-average power ratio(PAPR) signal. Thus, the sensitivity can be written as:

$$P_{sens,pulsed} = \sqrt{\frac{t_{pulse}}{t_p}} P_{sens} \tag{1.3}$$

where P_{sens} is defined by (1.2). The improvement in sensitivity as a function of t_p/t_{pulse} is plotted in Fig. 1.7(c) for $t_p = 10$ msec. The required SNR for false-alarm $\leq$1/Hr only changes by 1 dB for t_p/t_{pluse}=1000 due to increased number of samples at the input of the correlator, thus it doesn't significantly impact the sensitivity.

Passive RF Front-End with Active ED

For a passive energy detector, the noise contribution of the ED cannot be decreased to improve sensitivity(Chapter 3). However, that is not true for active energy detectors. For active energy detector based wake-up receiver shown in Fig. 1.4(d), the noise contribution from the energy detector can be reduced by increasing the power consumption. For an active ED, $i_{out} = k_{ed} v_{edin}^2$, where the voltage input to output current conversion gain constant $k_{ed} = I_{BIAS}/(2(nV_t)^2)$, here I_{BIAS} is the DC current, n is the sub-threshold slope coefficient and $V_t = k_B T/q$ is the thermal voltage. The noise current power spectral density is $2k_B T n I_{bias}/(nV_t)$. Compared to a passive RF front-end with passive ED, the current required for a similar sensitivity is $n^2 V_t^2/(2V_t R_s A_v^2)$, which leads to 3.6 μA current for A_v=20 dB. Sensitivity can further be improved with 0.5 dB/dB increase in current.

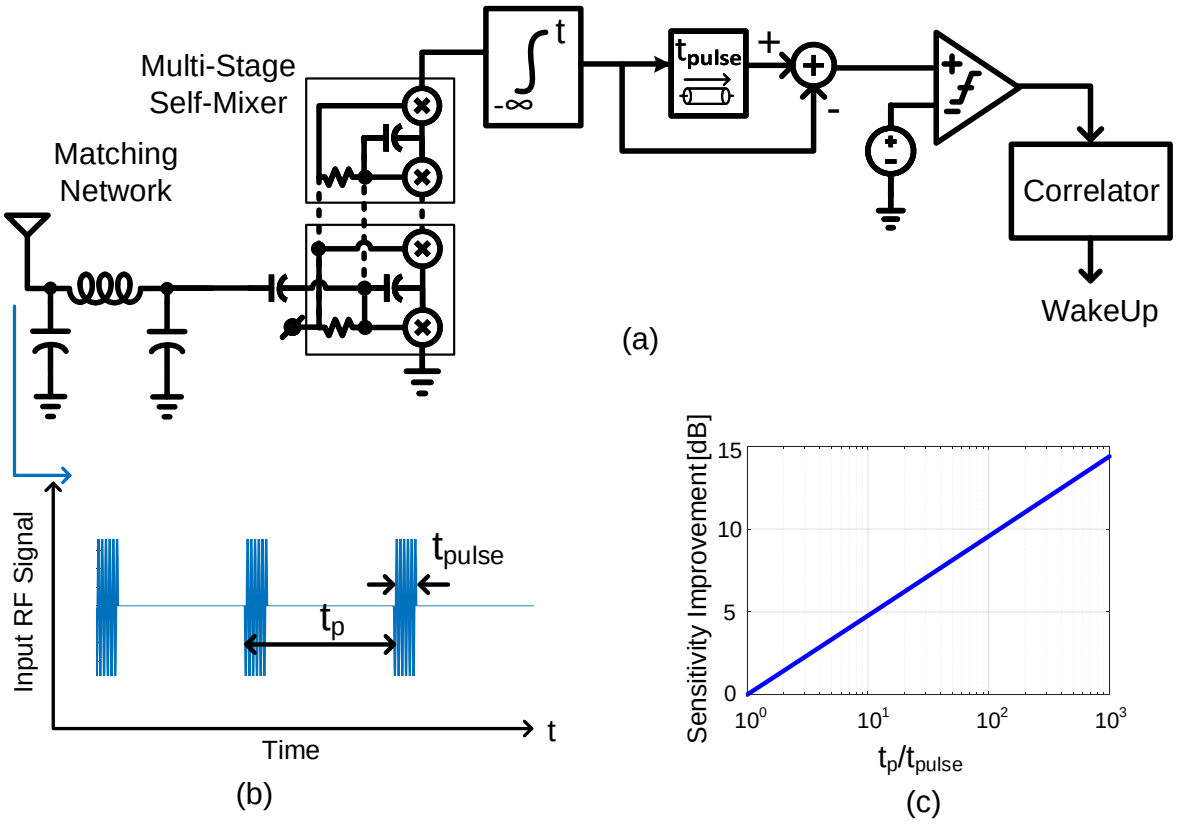


Figure 1.7: (a) Receiver architecture to receiver a pulsed-input signal, (b) an example of a pulsed-input RF signal with active time t_{pulse} for every bit period t_p, and (c) the improvement in sensitivity compared to the achievable sensitivity in Fig. 1.6 as a function of t_p/t_{pluse}.

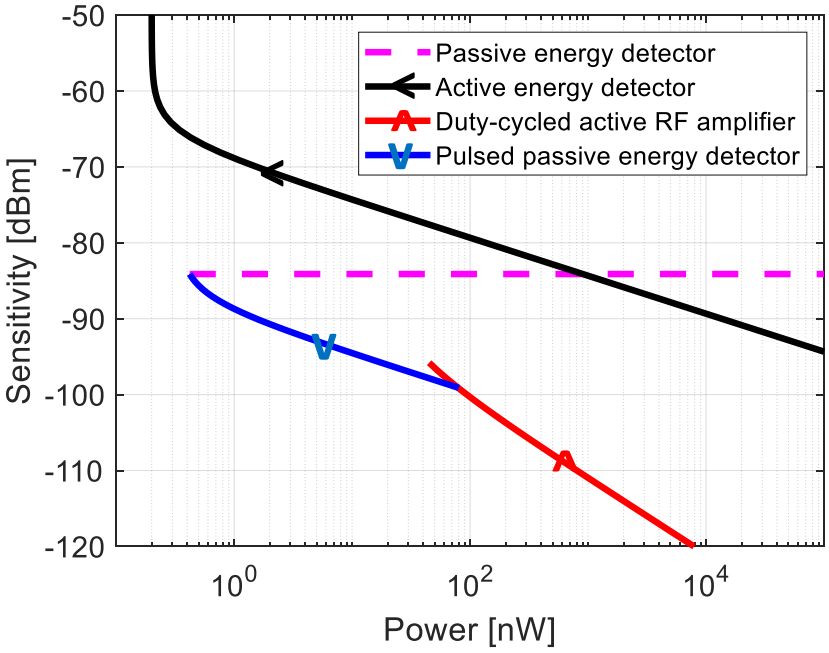


Figure 1.8: Performance trade-offs energy detector based wake-up receivers.

1.2.3 Performance Tradeoffs

The achievable sensitivity w.r.t. the power consumption for a 110msec latency and a passive voltage gain $A_v = 23\,\text{dB}$ is plotted in Fig. 1.8 for the wake-up receiver architectures discussed above. A 0.8 pW/Hz of power consumption is assumed (based on Sub-nW RX in Chapter 4) to evaluate the power-sensitivity trade-off for passive energy detectors with pusled RF input. At desired power consumption of ≤10 nW, passive-RF front end with passive energy detector is optimal for best sensitivity. At desired power consumption of ≥100 nW, duty-cycled RF amplifier with energy detector baseband, provides the best performance.

1.2.4 Selectivity in Energy-Detecting Receivers

While energy detectors down-convert the RF signal to baseband with minimal power, the down-converted baseband signal spectrum at frequency f_{bb} is a function of inter-mixing of the signals with $\Delta f = f_{bb}$ in the input spectrum. Therefore, the energy detector receiver exhibit no frequency-domain selectivity. The spectral dependence on Δf is exploited in a transmitted LO architec-

ture [17], where the transmitted signal is spread across frequency with a fixed Δf. This improves resilience to narrowband AM interference, but the performance degrades with increasing bandwidth of the interferer. The narrowband interferers can also be treated as LO to downconvert the RF signal to an IF frequency, this improves the selectivity as well as sensitivity for the wake-up receiver(Chapter 5).

For resilience to wideband AM interference, high-Q filters are required before the energy detector. The front-end RF matching network doesn't provide sufficient selectivity at high carrier frequency e.g. in [23], an off-chip transformer operating at 433 MHz provides a 3-dB RF bandwidth of 11 MHz. Thus a SAW filter or a MEMS filter is desired to provide channel selectivity in future.

Frequency-domain selectivity is not available from a ED-first receiver architecture without the front-end RF filter, but code-domain selectivity can still be achieved using an analog correlator at baseband. This is explored in Chapter 6. The code-domain selectivity also enables code-division multiple access(CDMA) using orthogonal codes in the same frequency band. This CDMA operation is also demonstrated in Chapter 6.

An alternative to RF front-end is using Ultrasound for communication. Here, since the carrier frequency is very small, the channel selectivity is provided by the ultrasound transducer itself. Ultrasound has been studied for wake-up applications [29, 30] but the transducers have poor transmit efficiency and the sound waves does not penetrate through walls, thus, it is best suited for applications with short ranges. Here, we will limit our analysis to RF wake-up receivers.

1.3 Thesis Organization

This chapter has discussed the challenges in designing a low-power sensor node, requirements for a wake-up receiver, and a brief discussion on the performance trade-offs in designing a wake-up receiver using energy-detecting front end. Chapter 2 further carries an in-depth noise analysis for these energy-detecting receivers with passive-RF front end and derives the requirements from the matching network and the energy detector for achieving the best performance.

Chapter 3 proposes different self-mixer architectures to serve as optimal energy detectors and discusses the design trade-offs. Chapter 4 presents the design of a fully integrated sub-nW wake-up receiver in 65 nm LP CMOS technology employing time-encoded matched filter and comparator with DC offset compensation loop.

For the sub-nW receiver proposed in Chapter 4, sensitivity and selectivity is limited by the front-end design. Chapter 5 proposes the use of interferer as LO to enhance both the sensitivity and the selectivity of the receiver, however, the receiver still gets blocked in the presence of a wideband AM interferer.

In Chapter 6, a clock-less continuous-time analog correlator is proposed which has multi-fold advantages. The correlator provides code-domain selectivity to improve rejection to AM interference. A clock-less architecture with code-domain matched filtering enhances the sensitivity as well. A selective response to two different codes is presented, demonstrating asynchronous CDMA for wake-up receiver application.

Further enhancement in the link is achieved using directional antennas to provide spatial gain and selectivity. A proof-of-concept directional backscatter tag is proposed in Chapter 7, which can be used with the sensor node to act as a reflectarray antenna with enhanced sensitivity and spatial selectivity.

Lastly, we conclude the thesis by highlighting the contributions and discussing directions for future work.

Chapter 2: Noise Analysis for Energy-Detecting Receivers

Energy-detecting receivers use a high-Q RF L-C matching network to provide high passive gain followed by an energy detector for sensing the RF signal (Fig. 2.1). Designing high-Q RF L-C matching networks is difficult at higher carrier frequencies due to increased losses, and as a result the receiver sensitivity often degrades. Thus, optimizing the RF front-end design is critical to maximize sensitivity.

Here, we'll assume an ideal RF front end as shown in Fig. 2.1 to evaluate the impact of the noise from the antenna and the energy detector. Next, we use an ideal rectifier as a passive energy detector, to evaluate the sensitivity as a function of front-end passive gain from the matching network and desired channel bandwidth. Non-idealities due to finite Q-factor of the inductor are introduced to evaluate the practical range of passive gains available, limiting the achievable sensitivity. The chapter concludes by defining the requirements on the energy detector given the front-end matching network to optimize sensitivity.

2.1 Noise Analysis

Fig. 2.1 shows the noise model for an ED receiver with a passive RF front end. The antenna is represented as a voltage source with a source resistance R_s of 50 Ω and is matched to the energy detector using a matching network with a passive gain A_v at frequency f_{rf}, leading to a 3-dB bandwidth BW_{RF}, and a noise factor N_{MN}. The energy detector is assumed to have an input resistance $R_{in,ed}$ with a conversion gain constant k_{ed}. Since the energy detector is non-linear, we evaluate the signal-to-noise ratio (SNR) at the output of the energy detector.

Assuming a continuous-wave RF signal with power P_{in} incident on the antenna with a radiation resistance R_s, resulting in an RF input signal $v_{in}(t)$. The root-mean-square (RMS) signal received

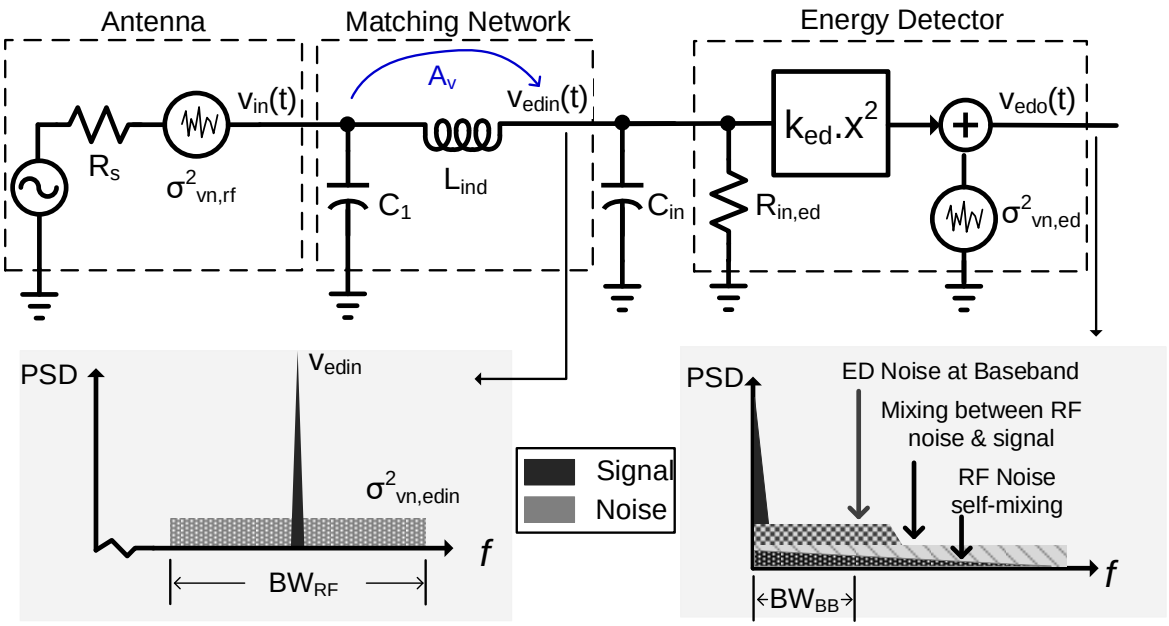


Figure 2.1: Small-signal model including noise sources for an ED receiver; the spectra of signal and noise at the input and the output of the energy detector are also shown.

from the antenna is $v^2_{in,rms} = P_{in}R_s$. The matching network provides a passive voltage gain A_v. At the output of the matching network, the signal is $v_{edin}(t) = v_{in}(t)A_v$. The input noise from the antenna gets band-pass filtered by the matching network leading to an input-referred noise variance of $\sigma^2_{vn,rf} = k_B T R_s BW_{RF}$ where k_B is the Boltzmann constant and T is the absolute temperature. The input signal spectrum in the presence of white noise is in Fig. 2.1.

Thus, the noise at the input of the energy detector $v_{n,edin}(t)$ has a variance $\sigma^2_{vn,edin} = \sigma^2_{vn,rf}A^2_v N_{MN}$. The output of the energy detector is $v_{edo}(t) = k_{ed}(v_{edin}(t) + v_{n,edin}(t))^2$. Fig. 2.1 also shows the spectra of the signal and noise components at the output of the energy detector. The signal at the output of the energy detector, $v_{edo}(t)$, is:

$$v^2_{edo,rms} = k^2_{ed}v^4_{edin,rms} = A^4_v k^2_{ed} P^2_{in} R^2_s \tag{2.1}$$

Using the results from noise and sensitivity analysis for ED receivers proposed in [15], the power spectral density (PSD) at the output of the energy detector due to signal mixed with noise and the

noise mixed with itself as a function of baseband frequency f is:

$$PSD_{vn,edo} = \frac{2k_{ed}^2 v_{edin,rms}^2 \sigma_{vn,edin}^2}{BW_{RF}/2} + \frac{k_{ed}^2 \sigma_{vn,edin}^4 2(BW_{RF} - f)}{BW_{RF}^2} \quad 0 \leq f \leq BW_{RF} \tag{2.2}$$

Here, the first term is due to mixing of signal with noise, and second term is due to self-mixing of the noise at f_{rf}. Further, let's assume that the energy detector adds noise $\sigma_{vn,ed}^2$ at baseband. Assuming that BW_{RF} is much larger than BW_{BB}, the total noise variance at the output is:

$$\sigma_{vn,edo}^2 = 2k_{ed}^2 \sigma_{vn,edin}^2 \left(\frac{BW_{BB}}{BW_{RF}}\right) \left(2v_{edin,rms}^2 + \sigma_{vn,edin}^2\right) + \sigma_{vn,ed}^2 \tag{2.3}$$

the first term is due to mixing of the $v_{edin}(t)$ with $v_{n,edin}(t)$, the second term is due to self-mixing of the $v_{n,edin}(t)$ at RF, and $\sigma_{vn,ed}^2$ represents the noise added by the energy detector. The SNR at the output of the ED can be found from:

$$\frac{1}{SNR} = \frac{\sigma_{vn,edo}^2}{v_{edo,rms}^2} = \frac{4k_B T BW_{BB} N_{MN}}{P_{in}} \left(1 + \frac{k_B T BW_{RF} N_{MN}}{2P_{in}}\right) + \frac{\sigma_{vn,ed}^2}{A_v^4 k_{ed}^2 P_{in}^2 R_s^2} \tag{2.4}$$

2.2 Passive Energy Detector Model

A conventional energy detector using a diode-connected transistor is shown in Fig. 2.2(a). The energy detector has an RF input signal v_{edin}, with a baseband output v_{edo}. Assuming the transistor in weak-inversion and operating in the linear region with drain-to-source potential $V_{ds} \approx 0$, a symmetric weak-inversion body-referenced equation for the drain-to-source current is [31]:

$$I_{ds} = I_s (W/L) e^{(V_{gb}/nV_t)} (e^{(-V_{sb}/V_t)} - e^{(-V_{db}/V_t)}) \tag{2.5}$$

where $V_t = k_B T/q$ is the thermal voltage, I_s is the saturation current, W and L are the width and the length of the channel. Assuming the baseband signal generated across drain and source due to second-order non-linearity is small and equal to v_{edo}, $v_{gb} = v_{edin}$; $v_{sb} = v_{edo}$; $v_{db} = v_{edin}$. For small

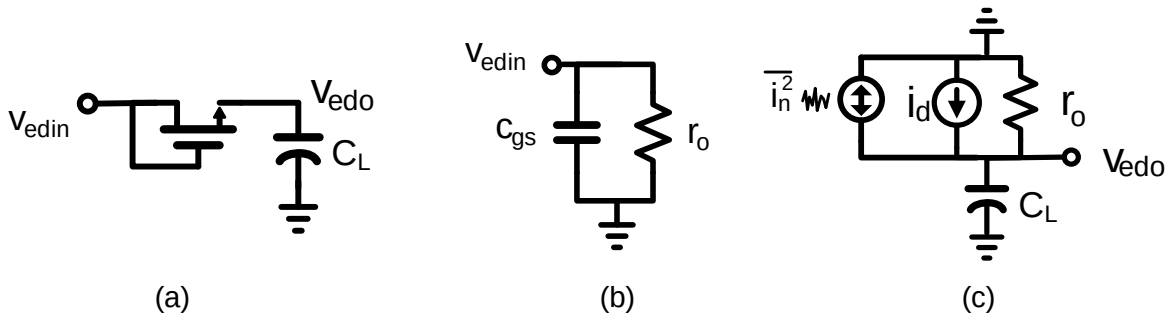


Figure 2.2: (a) An energy detector using a diode connected transistor, (b) the equivalent small-signal model at f_{rf}, and (c) the equivalent small-signal model at baseband frequency.

v_{edin}, using the Taylor series expansion and neglecting the higher order terms:

$$I_{ds} = K\left(\frac{v_{edin} - v_{edo}}{V_t}\right) + K\left(\frac{v_{edin}}{V_t}\right)^2\left[\frac{2-n}{2n}\right] \tag{2.6}$$

where $K = I_s(W/L)$. This leads to the equivalent small-signal model at baseband shown in Fig. 2.2(c), the first term is proportional to the drain-to-source potential $v_{db} - v_{sb}$ and can be represented as a resistor $r_o = V_t/K$, and, the second term can be represented as an i_d current source:

$$i_d = K\left(\frac{v_{edin}}{V_t}\right)^2\left[\frac{2-n}{2n}\right] \tag{2.7}$$

Assuming that the load capacitor C_L act as open at baseband, the baseband current should be zero. Thus:

$$v_{edo} = \left[\frac{2-n}{2n}\right]\frac{v_{edin}^2}{V_t} = k_{ed}v_{edin}^2 \tag{2.8}$$

where $k_{ed} = (2-n)/(2nV_t)$. At f_{rf}, capacitor C_L is assumed as a short, thus the input impedance is the channel resistance r_o in parallel with the gate-to-source capacitance c_{gs} as shown in Fig. 2.2(b). The output impedance at baseband is also equal to the channel resistance r_o. For transistors operating in the weak-inversion linear region, the channel behaves as a resistor of value $r_o = 1/g_{ds}$ [31]

and the noise variance can be written as

$$\sigma^2_{vn,ed} = 4k_B T R_{in,ed} BW_{BB} \tag{2.9}$$

Note that the input resistance at f_{rf} is $R_{in,ed} = r_o$, also equal to the baseband output resistance $R_{out,ed} = r_o$. Thus, the output noise is directly coupled to the input resistance through the transistor channel.

2.3 Sensitivity Analysis

Here, we use the characteristics of a passive energy detector derived in Section 2.2 and the noise analysis carried out in Section 2.1 to determine the sensitivity of these energy-detection receiver. Here, we assume that the minimum required SNR is SNR_{min}.

2.3.1 Antenna noise mixed with itself dominates

If the self-mixing noise dominates at the output of the ED, using (2.4):

$$SNR = \frac{P_{in}^2}{2.N_{MN}^2 (k_B.T)^2 .BW_{RF}.BW_{BB}} \tag{2.10}$$

The sensitivity can be written as $P_{sens} = N_{MN}(K_B T)\sqrt{2BW_{RF}BW_{BB}SNR_{min}}$.

2.3.2 Antenna noise mixed with input signal dominates

If the RF noise mixed with signal dominates, the output noise using (2.4) is:

$$SNR_{out} = \frac{P_{in}}{4N_{MN}(k_B T)BW_{BB}} \tag{2.11}$$

$$P_{sens} = 4.N_{MN}(k_B T)BW_{BB}SNR_{min} \tag{2.12}$$

At a baseband bandwidth of 1MHz, $SNR_{min} = 12.4\,\text{dB}$, $N_{MN} = 2$ results in a sensitivity of $-92.4\,\text{dBm}$. If the baseband noise is negligible compared to the noise at the input, the sensitivity becomes independent of A_v and k_{ed}.

2.3.3 Noise added by the energy detector dominates

If the baseband noise dominates the output, using (2.4) and (2.9):

$$SNR_{out} = \frac{A_v^4 k_{ed}^2 P_{in}^2 R_s^2}{4k_B T R_{in,ed} BW_{BB}} \tag{2.13}$$

$$P_{sens}^2 = \frac{4k_B T R_{in,ed} BW_{BB} SNR_{min}}{A_v^4 k_{ed}^2 R_s^2}. \tag{2.14}$$

Further, for a matching network converting R_s to $R_{in,ed}$ with a passive gain of A_v, $R_{in,ed} = r_o = R_s A_v^2$ hence:

$$P_{sens}^2 \propto \frac{R_{in,ed} BW_{BB}}{A_v^4 k_{ed}^2} \propto \frac{BW_{BB}}{A_v^2 k_{ed}^2} \tag{2.15}$$

Hence, sensitivity only improve 0.5 dB/dB with increase in passive gain or 0.5 dB/dB decrease in data rate. Using (2.1),(2.4),(2.9) and (2.8), maximum achievable sensitivity is evaluated for the receiver assuming $N_{MN} = 2$, $SNR_{req} = 12.3\,\text{dB}$, and sub-threshold slope coefficient n=1.3. Fig. 2.3 shows the empirically calculated sensitivity of the receiver with increasing passive gain from matching network at different desired data rates. At low passive gains (region 1), $\sigma_{vn,ed}^2$ dominates the noise, thus, the last term in (2.4) dominates and the sensitivity improves for an increase in passive gain. At high passive gains (region 2), the noise due to mixing of signal $v_{edin}(t)$ with noise $v_{vn,edin}(t)$ dominates, thus, sensitivity becomes independent of A_v. For practical passive gains of 10-40 dB, (2.14) can be used to evaluate the sensitivity of the receiver. Note that this analysis is carried out for a continuous-wave signal at the RF input. The results may differ for a modulated input signal.

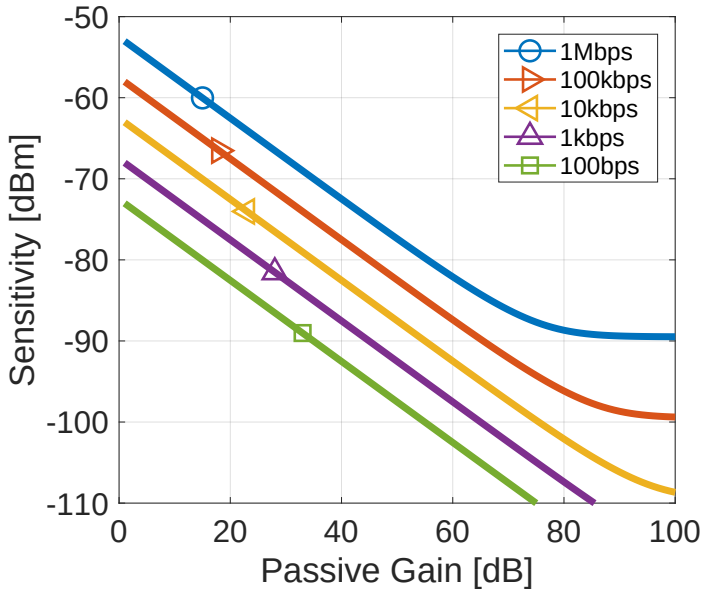


Figure 2.3: Sensitivity of the energy-detector receiver for increasing passive gain from the matching network at different desired data rates for a 12.3 dB SNR required at the output of the energy detector.

2.4 Limited Front-End Passive Gain

Fig. 2.3 suggests that a high passive gain will provide a better sensitivity for the receiver. But, the achievable passive gain from the matching network is limited due to the finite Q-factor of the inductor. Additionally, with increasing frequency f_{rf}, the quality of the inductors degrade due to the reduced skin depth and more pronounced proximity effect.

The maximum achievable A_v depends on the load being driven. Let's assume the matching network sees a load resistance of $R_{in,ed}$ in parallel with capacitance C_{in}. Typically, C_{in} is a combination of the capacitances from the off-chip inductor, package, bond-wire, on-chip electrostatic discharge (ESD) circuit, and energy detector.

Assuming that an inductor with value $L_{ind} \approx 1/(\omega_{RF}^2 C_{in})$ is available with a self-resonance frequency much higher than $\omega_{RF}/(2\pi)$, the passive gain from the matching network at an angular

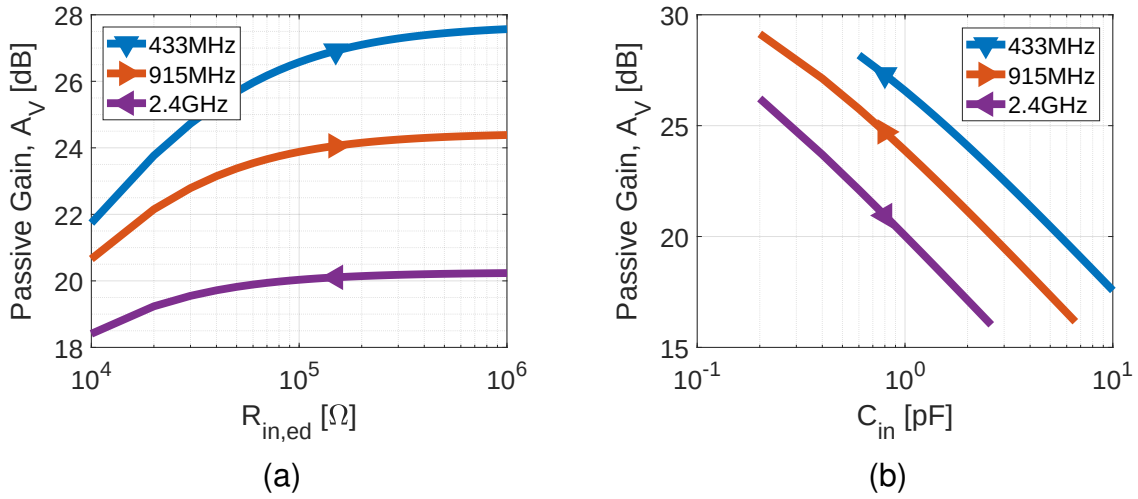


Figure 2.4: (a) Passive gain variation with the input resistance at an C_{in} = 1 pF; (b) Passive gain variation with input capacitance at an $R_{in,ed}$ = 100 kΩ at different ISM band frequencies for an inductor Q=80.

frequency ω_{RF} can be written as:

$$A_v = \sqrt{\frac{R_{in,ed}}{R_s}} \Bigg/ \sqrt{\left(1 + \frac{\omega_{RF} R_{in,ed} C_{in}}{Q_{ind}}\right)} \tag{2.16}$$

where $Q_{ind} = \omega_{RF} L_{ind} / R_{ind}$ is the quality factor of the inductor in the matching network. Fig. 2.4a shows the A_v for a Q_{ind} of 80 for different ISM band frequencies; for a fixed C_{in} of 1 pF, the achievable A_v increases with increasing $R_{in,ed}$, but once $R_{in,ed} > 100$ kΩ, A_v has only a weak dependence on $R_{in,ed}$ due to the dominating losses in the matching network. Thus, $R_{in,ed}$ is required to be $\approx 100\,\text{k} - 1\,\text{M}\Omega$. Fig. 2.4b shows the degradation in A_v with increasing C_{in} for a fixed $R_{in,ed}$ of 100 kΩ. A small C_{in} is desired to maximize A_v. Thus, a sufficiently high $R_{in,ed}$ and a low C_{in} are desired from the energy detector. With increasing frequency, for a fixed C_{in}, A_v degrades further as evident from Fig. 2.4. Hence a reduction in load capacitance is necessary for operation at higher RF carrier frequencies to achieve high A_v.

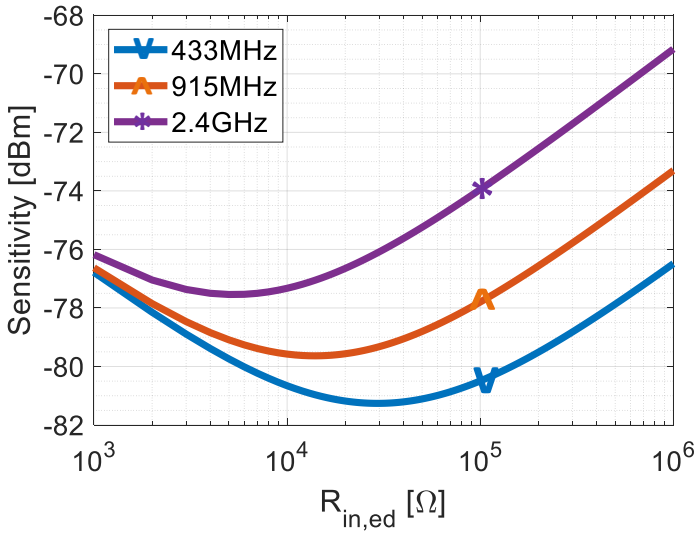


Figure 2.5: Achievable receiver sensitivity for a continuous-wave RF input signal as a function of the self-mixer input resistance $R_{in,ed}$ assuming Q_{ind}=80, C_{in}=1 pF, BW_{BB}=200 Hz, SNR_{req}=12.4 dB.

2.5 Optimizing for Sensitivity

The achievable passive gain saturates due to the finite Q-factor of the available inductor. Therefore, there is a limit to the enhancement in sensitivity with increasing passive gain as plotted in Fig. 2.3. Here, we evaluate the best sensitivity achievable for a continuous wave signal at the input of the receiver.

Using (2.16) and (2.14):

$$SNR_{edo} \propto \frac{A_v^4}{R_{in,ed}} \propto \frac{R_{in,ed}}{R_s^2} \Bigg/ \left(1 + \frac{\omega_{RF} R_{in,ed} C_{in}}{Q_{ind}}\right)^2 \tag{2.17}$$

The sensitivity for a C_{in} of 1 pF, a Q_{ind} of 80, an SNR_{req} of 12.4 dB, an NF of 1.2 dB and an BW_{BB} of 200 Hz is plotted in Fig. 2.5 for different ISM band frequencies. The optimal $R_{in,ed}$ for maximizing sensitivity can be written as:

$$R_{in,opt} = Q_{ind}/(\omega_{RF} C_{in}) \tag{2.18}$$

E.g., for a Q_{ind} of 80 and a capacitance C_{in} of 1 pF at 434 MHz, the optimal $R_{in,ed}$ for the energy detector is 30 kΩ. Operating the receiver with $R_{in,ed} = R_{in,opt}$ degrades the SNR by 6 dB. This leads

to a receiver sensitivity degradation of 3 dB compared to the ideal sensitivity plotted in Fig. 2.3.

Therefore, an energy detector with an input resistance of $R_{in,opt} = Q_{ind}/(\omega_{RF}C_{in})$ is desired to achieve optimal sensitivity from a passive-RF energy detector receiver. Next, self-mixers are proposed to achieve the desired $R_{in,opt}$ while adding minimal contribution to C_{in}.

Chapter 3: Self-Mixers

Sensitivity analysis in Section 2.5 demonstrates that a high input resistance $R_{in,ed}$ is not the optimal design for best sensitivity. A desired $R_{in,ed}$ is dependent on the front-end matching network losses for best sensitivity. For e.g. an inductor quality factor Q_{ind} of 200 requires the energy detector with an input capacitance of 1 pF to have $R_{in,ed}$ of 83 kΩ at 2.4 GHz operation. The nominal-V_t transistors available in 65 nm LP CMOS technology has a channel resistance of 100 MΩ which is much higher than the required operating resistance. One approach is to increase the W of the transistors, but, a 100x reduction in $R_{in,ed}$ require a 100x W/L, leading to 100x increase in input capacitance, again degrading the front-end matching network. Here, a self-mixer provides extra degree of freedom to reduce the impedance without increase in capacitance and no degradation in conversion gain constant. This chapter describes several designs of the self-mixer derived from the conventional envelope detectors and proves the optimality of the self-mixer to be used as energy detectors for wake-up receivers.

3.1 Self-Mixer Operation Principle

Gate-biased self-mixers are derived from a conventional envelope detector by introducing an AC coupling capacitor and providing a DC bias potential, V_{G_B}, at the gate e.g. self-mixer in Fig. 3.1b is derived from an envelope detector circuit in Fig. 3.1a. This gate bias slightly forward biases the channel, while still operating the transistor in the weak-inversion, linear region. Fig. 3.1c shows the equivalent small-signal model at an RF input frequency, assuming the capacitors C_C and C_L are sufficiently large to act as a shorts at RF.

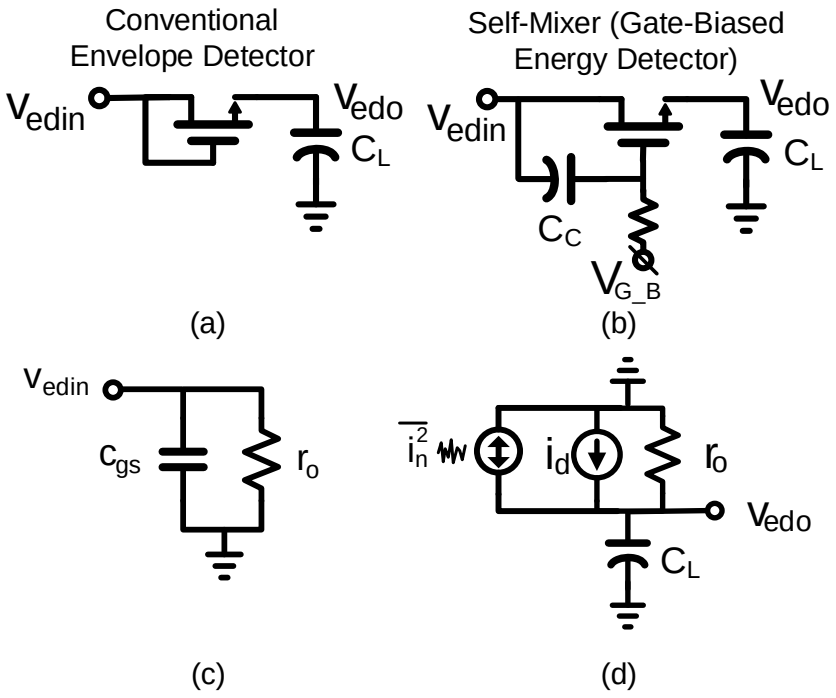


Figure 3.1: (a) A conventional envelope detector, (b) one-stage self-mixer, (c) self-mixer small-signal model at RF frequency, (d) and the small-signal model at baseband frequency.

3.1.1 Achieving High Enough Resistance

Fig. 3.2a shows the varying input resistance $R_{in,ed} = r_o$ and capacitance $C_{in,ed} = c_{gs}$ with V_{G_B} for a one-stage self-mixer consisting of a single transistor with $(W/L) = (1\,\mu/60\,\text{n})$ in a 65 nm LP CMOS process, where:

$$R_{in,ed} = r_o = \frac{V_t}{K} = \frac{V_t}{I_s}\frac{L}{W}e^{-V_{G\_B}/(nV_t)} \tag{3.1}$$

The simulated $R_{in,ed}$ at zero bias is >100 MΩ, which is sufficiently large compared to the requirements in 2.5; it can be easily reduced since $R_{in,ed}$ decreases exponentially with increasing V_{G_B}.

3.1.2 Minimizing Capacitance

The input capacitance $C_{in,ed}$ for the one-stage self-mixer is dominated by the transistor's gate-to-source capacitance c_{gs}. Using minimum-sized transistors keeps the capacitance low; a $1\,\mu/60\,\text{n}$

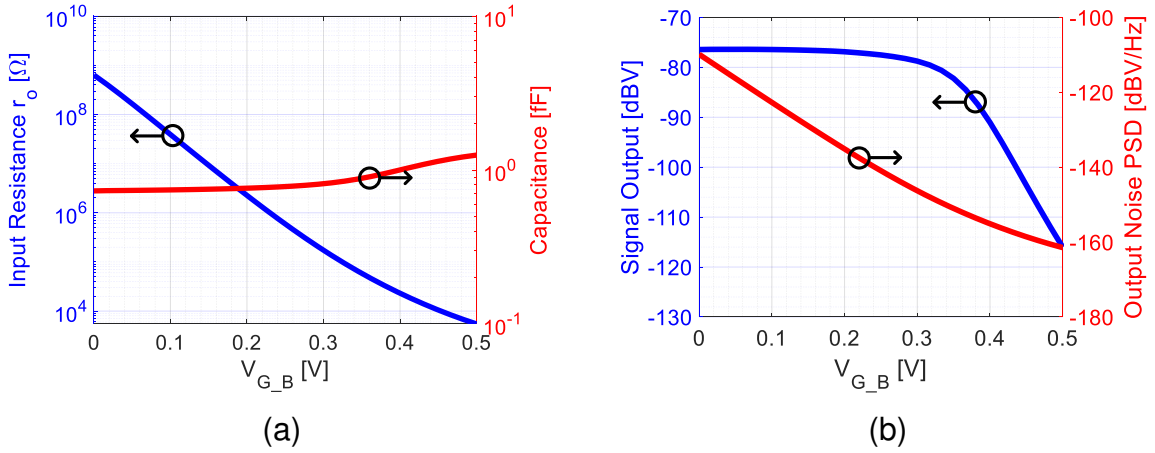


Figure 3.2: (a) ED input resistance, capacitance and (b) conversion gain at 5mV RF input signal and noise power spectral density at 100 Hz with increasing V_{G_B}.

transistor contributes a capacitance of 1 fF.

3.1.3 Conversion Gain and Noise of the Self-Mixer

Conversion gain for a conventional envelope detector was derived in Section 2.2. The equivalent self-mixer will have the same conversion gain at $V_{G\_B} = 0$. Fig. 3.2b shows the varying output for a 5 mV peak RF input to the self-mixer for increasing V_{G_B}; v_{edo} remains constant in weak-inversion, and there is practically no signal reduction due to forward biasing the channel.

Since the transistor is operating in the weak-inversion, linear region, the power spectral density (PSD) of the output noise of the self-mixer can be written as $4k_BTR_{out,ed}$ where $R_{out,ed}$ is equal to the channel resistance r_o for a one-stage self-mixer. Fig. 3.2b also shows the exponential drop in PSD at 100Hz for the self-mixer with increasing V_{G_B}, demonstrating the direct dependence on the channel resistance r_o.

Therefore, with increasing V_{G_B}, the self-mixer noise contribution at baseband can be reduced while keeping the conversion gain constant and the input capacitance low. This maximizes the signal-to-noise ratio (SNR) at the output of the self-mixer.

3.1.4 Satisfying Requirements for Optimal Sensitivity

Section 2.5 derives the input impedance desired from a passive energy detector for optimal sensitivity. A minimum input capacitance is desired, and an $R_{in,ed} = R_{in,opt}$ is calculated based on the input capacitance, operating frequency and the matching network losses. A self-mixer, using V_{G_B} minimizes the input capacitance, gives a tuning control to set $R_{in,ed} = R_{in,opt}$ while not affecting the conversion gain. Thus, a self-mixer serves as an optimal energy detector for passive energy-detection receivers.

Further sensitivity enhancement can be achieved by increasing the conversion gain constant k_{ed} for the self-mixer. A single-ended multi-stage self-mixer and a differential-in differential out self-mixer are presented here and compared based on the conversion gain and the contribution to the input capacitance.

3.2 Single-Ended RF Input Self-Mixer

A single-ended RF input self-mixer is designed based on a multi-stage Dickson charge pump in Fig. 3.4 by providing a bias potential V_{G_B} at the gate of each transistor. Transistors operate in two different configurations, in config. 1 RF signal v_{edin} is AC coupled at the drain, whereas, in config. 2 v_{edin} is AC coupled at the source and the gate. Next, we evaluate the conversion gain for both configurations.

3.2.1 Operation of a Single-Stage Self-Mixer

Fig. 3.3(a) and (b) shows the operation of 1-transistor self-mixers in config. 1 and config. 2 respectively.

For config. 1, assuming a baseband drain-to-source potential generated as v_{edo}: $V_{gb} = V_{G\_B}$; $V_{sb} = 0$; and $V_{db} = v_{edin} + v_{edo}$. Using the drain-to-source current 2.5:

$$I_{DS} = I_s \frac{W}{L} e^{V_{G\_B}/(nV_t)} \left(1 - e^{-(v_{edin}+v_{edo})/V_t}\right) \tag{3.2}$$

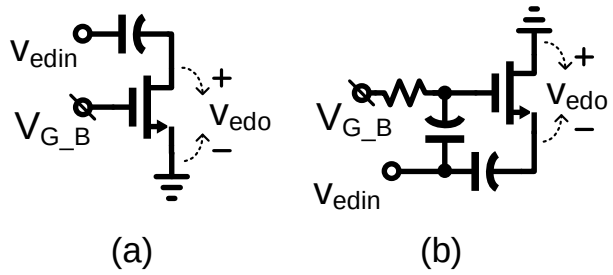


Figure 3.3: 1-stage self-mixer configurations for a single-ended self-mixer design.

Using Taylor series expansion and neglecting the 3^{rd} order or higher terms:

$$I_{DS} = I_s \frac{W}{L} e^{V_{G\_B}/(nV_t)} \left(\frac{v_{edin} + v_{edo}}{v_t} - \frac{v_{edin}^2}{2v_t^2} - \frac{v_{edo}^2}{2v_t^2} - \frac{v_{edin} v_{edo}}{v_t^2} \right) \tag{3.3}$$

Assuming capacitor C_C is open at baseband, equating the baseband current to zero gives:

$$v_{edo} = \frac{(v_{edin})^2}{2V_t} = k_{ed1}(v_{edin})^2 \tag{3.4}$$

For config. 2: $V_{gb} = V_{G\_B} + v_{edin}; V_{sb} = v_{edin} - v_{edo}; V_{db} = 0$; following the same steps as above gives:

$$I_{DS} = I_s \frac{W}{L} e^{V_{G\_B}/(nV_t)} \left(1 + \frac{v_{edin}}{nV_t} + \frac{v_{edin}^2}{2n^2V_t^2} \right) \left(\frac{v_{edo} - v_{edin}}{v_t} + \frac{v_{edin}^2}{2v_t^2} + \frac{v_{edo}^2}{2v_t^2} - \frac{v_{edin} v_{edo}}{v_t^2} \right) \tag{3.5}$$

Again, equating the baseband current to zero gives:

$$v_{edo,1t} = i_d r_o = \frac{(2-n)(v_{edin})^2}{2nV_t} = k_{ed1}(v_{edin})^2 \tag{3.6}$$

These two configurations are cascaded to form a multi-stage self-mixer. On average, the output of an each stage at baseband can be written as:

$$v_{edo} = \frac{v_{edin}^2}{2nV_t} \tag{3.7}$$

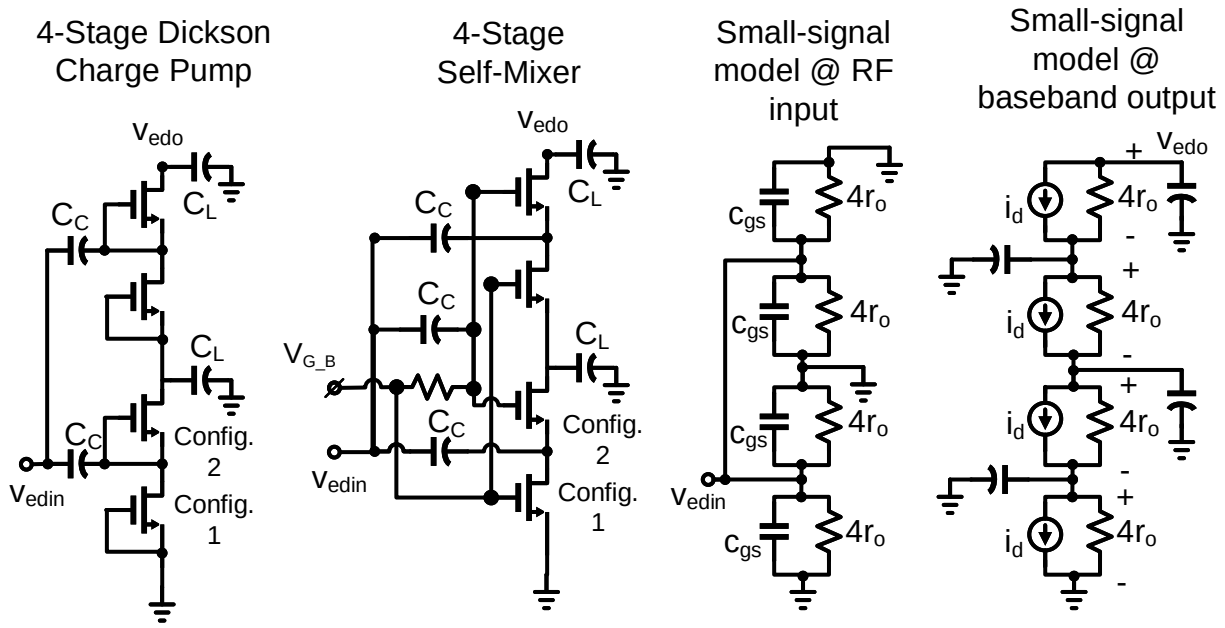


Figure 3.4: Different operating configuration of transistors in a multi-stage self-mixer inspired from Dickson charge pump.

3.2.2 Multi-Stage Self-Mixer

A 4-stage self-mixer is shown in Fig. 3.4 derived from a 4-stage Dickson charge pump. Small-signal model at RF and baseband frequency is also shown. Multiple stages appear in parallel at RF, thus the input resistance of the N-stage self-mixer at RF is r_o/N. The model doesn't have multi-stage closed loops at baseband, therefore the loading is capacitive. For N-stages the baseband output is:

$$v_{edo} = k_{ed} v_{edin}^2 = N \frac{(v_{edin})^2}{2nV_t} \tag{3.8}$$

where the conversion constant k_{ed} is $N/(2nV_t)$. Multiple stages appear in series at baseband, thus the output resistance is $N.r_o$; therefore $R_{out,ed} = N^2 R_{in,ed}$. The output noise PSD in the signal bandwidth of interest is then $PSD_{vn,ed} = 4k_B T N^2 R_{in,ed}$.

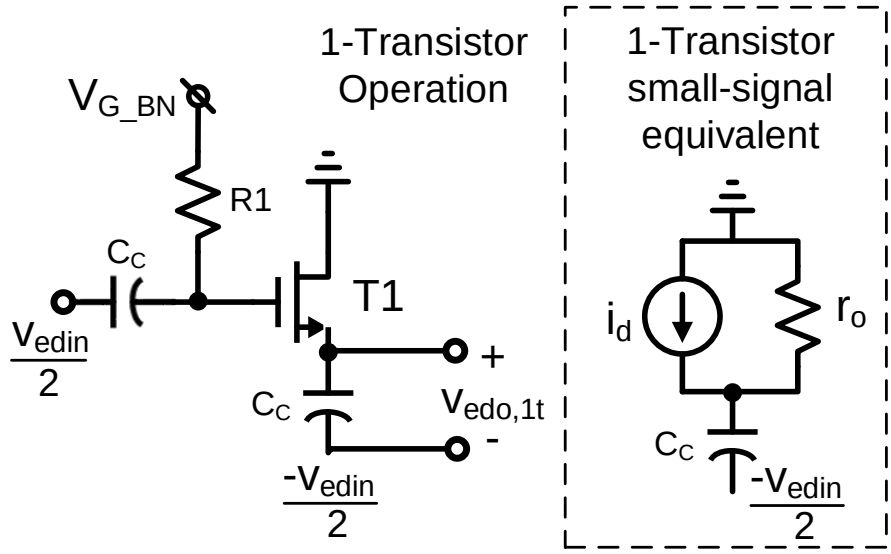


Figure 3.5: One-transistor self-mixer operation and it's small-signal model equivalent.

3.3 Differential RF Input Self-Mixer

3.3.1 Operation of a 1-Transistor Self-Mixer

Fig. 3.5 shows the operation of a one-transistor self-mixer circuit implemented with an NMOS T1. The drain of T1 is grounded. Capacitors C_C are assumed to act as shorts at RF and opens at baseband. The source is floating, so the source has the same DC potential as the drain. The DC bias at the gate of T1 is V_{G_BN} and RF signals $v_{rf} = v_{edin}/2$ and $-v_{rf} = -v_{edin}/2$ are AC coupled to the gate and source respectively. Assuming the baseband signal generated across drain and source due to second-order non-linearity is small, $V_{gb} = V_{G\_BN} + v_{rf}$; $V_{sb} = V_{edo,1t} - v_{rf}$; $V_{db} = 0$. For small v_{rf}, using the Taylor series expansion and neglecting the higher order terms:

$$I_{ds} = K\left(\frac{v_{rf} - V_{edo,1t}}{V_t}\right) + K\left(\frac{v_{rf}}{V_t}\right)^2\left[\frac{2+n}{2n}\right] \tag{3.9}$$

where $K = I_s(W/L)e^{V_{G\_BN}/(nV_t)}$. This leads to the equivalent small-signal model at baseband shown in Fig. 3.5, the first term is proportional to the drain-to-source potential $V_{db} - V_{sb}$ and can

be represented as a resistor r_o, and, the second term can be represented as an i_{ds} current source:

$$r_o = \frac{V_t}{K} = \frac{V_t}{I_s}\frac{L}{W}e^{-V_{G\_BN}/(nV_t)} \tag{3.10}$$

$$V_{edo,1t} = i_{ds}r_o = \left[\frac{2+n}{2n}\right]\frac{(v_{rf})^2}{V_t} = k_{ed1}(v_{rf})^2 \tag{3.11}$$

Fig. 3.6 shows a complete stage of the self-mixer combining a PMOS (T3, T4) and an NMOS (T1, T2) pair. A common-mode voltage V_{CM} is provided at the drain of T3 and T4. The corresponding gate bias voltage for PMOS transistors is V_{G_BP}. In the presence of an RF signal, a drain-to-source potential is generated across all transistors. As the current polarities for PMOS and NMOS transistor are opposite, the voltage across T3 and T1 gets added and the observed output potential across 1-stage at baseband can be written as:

$$v_{edo} = \frac{(2+n)}{4nV_t}v_{edin}^2 \tag{3.12}$$

3.3.2 Characteristics of a Multi-Stage Self Mixer

The self-mixer stages can be cascaded into a multi-stage mixer; Fig. 3.7 shows the proposed multi-stage self-mixer architecture. Cascading stages don't form any closed loops, hence the loading is capacitive. The common-mode potential V_{CM} is provided at the drain of the middle stage. For N-stages the conversion equation for self-mixer becomes:

$$v_{out} = k_{ed}v_{edin}^2 = N\left[\frac{2+n}{4n}\right]\frac{(v_{edin})^2}{V_t} \tag{3.13}$$

and the conversion constant k_{ed} for the N-stage self-mixer is $N(2+n)/4nV_t$. For a sinusoidal input signal v_{edin}, the

The N stages appear in parallel at RF and in series at baseband. Hence, the differential input resistance at RF is $R_{in} = r_o/N$, while the differential output resistance at baseband is $R_{out} = Nr_o$, and

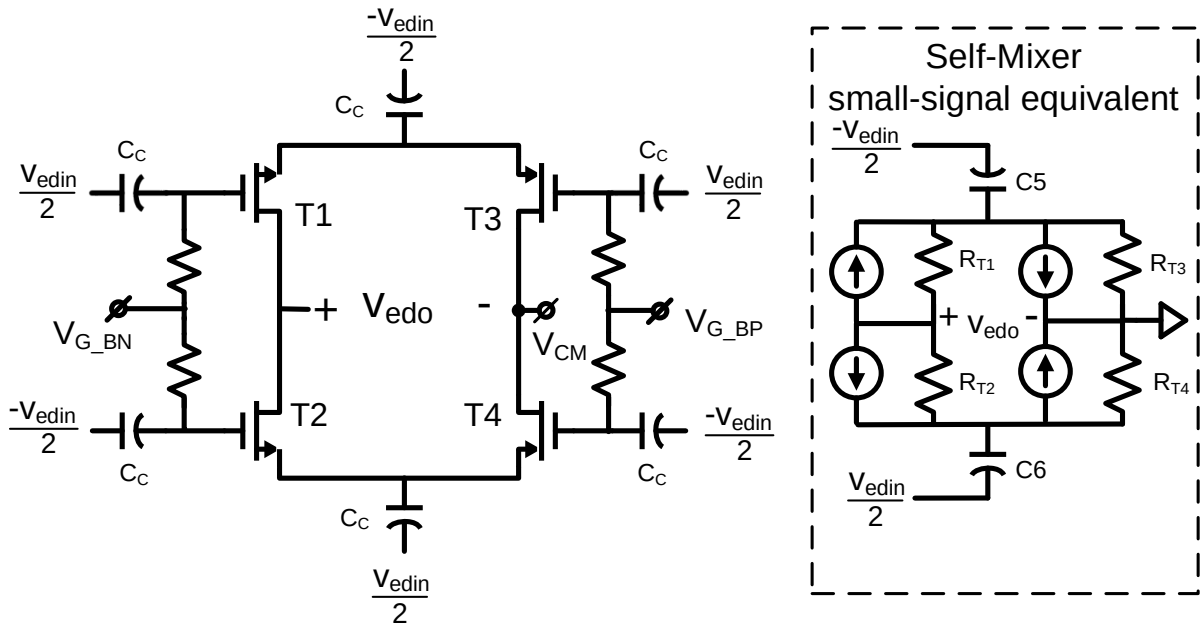


Figure 3.6: One-stage self-mixer circuit and its small-signal equivalent by combining an NMOS pair and a PMOS pair one-transistor self-mixer shown in Fig. 3.5.

thus $R_{out} = N^2 R_{in}$. The output noise variance of the self-mixer is then $\sigma^2_{vn,ed} = 4K_B T N^2 R_{in} BW_{BB}$.

3.3.3 Biasing Circuit

The bias potentials V_{G_BP} and V_{G_BP} for biasing the self-mixer transistors T1, T2, T3 and T4 are generated by comparing a replica of these transistors with a 10 MΩ poly-resistor used in a 2nA PTAT current reference circuit as shown in Fig. 3.8. This PTAT current reference biases transistors T9 and T10 to set the desired resistance. The generated DC potentials V_{G_BP} and V_{G_BP} for NMOS and PMOS pair respectively sets the resistance of T1, T2, T3, and T4. This current-controlled biasing technique makes the self-mixer resilient to process and temperature variations.

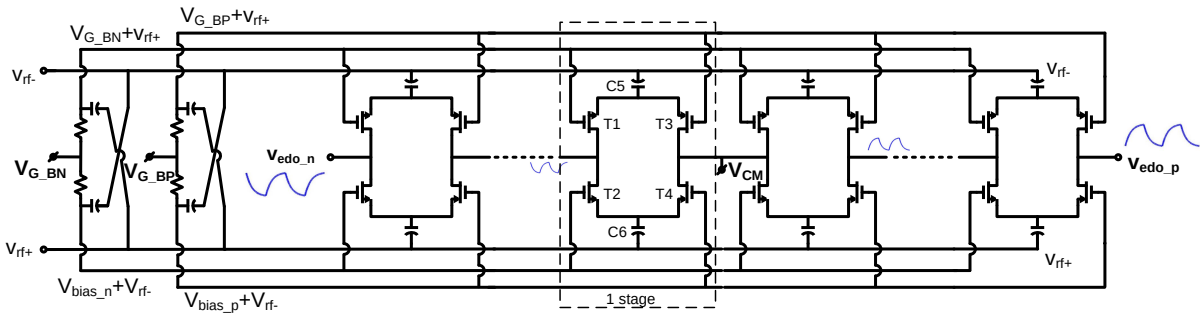


Figure 3.7: Proposed multi-stage self-mixer architecture by cascading a 1-stage self-mixer shown in Fig. 3.6. Here, $v_{rf} = v_{edin}/2$

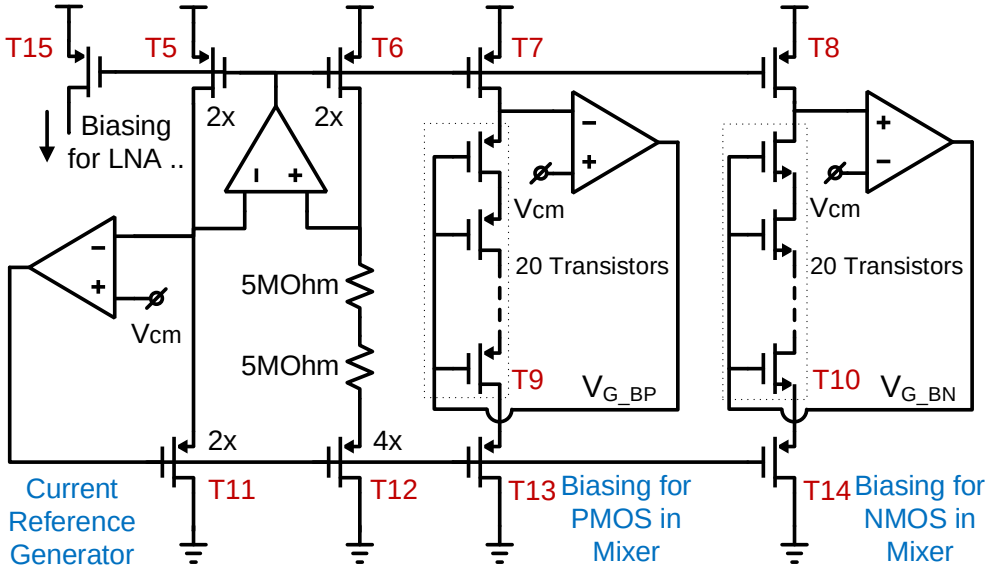


Figure 3.8: Biasing circuit generating V_{bias_p} and V_{bias_n} for self-mixer (Fig. 3.7) and PTAT current reference for baseband circuits.

3.4 Impact of Multiple Stages

3.4.1 Sensitivity

The signal-to-noise ratio at the output of the self-mixer using (2.13) and (3.13) is:

$$SNR_{edo} = \frac{1}{4K_BTBW_{BB}}\left[\frac{2+n}{4n}\right]^2 \frac{A_v^4 P_{in}^2 R_s^2}{R_{in}V_t^2} \tag{3.14}$$

Both signal power and noise power increases in proportion to N^2. Thus, the ratio is independent of the number of stages used. Therefore, the increased number of stages doesn't improve the sensitivity. However, it does provide an additional baseband gain without any power consumption, this helps in reducing the power consumption of the baseband circuits.

3.4.2 Bandwidth

With increasing number of self-mixer stages, the offered bandwidth decreases. The self-mixer can be treated as an RC transmission line, where the resistance $R_{tx} = R_{in,ed}.N$ and the capacitance $C_{tx} = C_C$. The step input to output transfer function for a transmission line with an open circuit load is the error function [32]:

$$v_{edo}(t) = v_{edo} erf\left(\frac{N\sqrt{R_{tx}C_{tx}}}{2\sqrt{t}}\right) \tag{3.15}$$

Thus, the equivalent bandwidth is $0.46/(N^2 R_{tx}C_{tx})$. With increasing number of stages, the available baseband bandwidth reduces.

3.4.3 Baseband Power Consumption

The output signal is $\propto N$, therefore, multiple stages can be treated as providing passive gain before the baseband. This passive gain relaxes the noise requirements and reduces the active power consumption of the baseband circuits.

3.5 Comparison Between Different Self-Mixers

Fig. 3.9 shows the conversion-gain constant k_{ed} for different 1-stage self-mixer architectures. The differential-in differential-out self-mixer provides a 3 dB better conversion constant compared to the single-ended self-mixer architecture. The conversion gain for all self-mixer designs improve for slight increase in the channel length due to improvement in the sub-threshold slope constant n. For channel length ≥100 nm, the improvement in conversion gain k_{ed} is minimal.

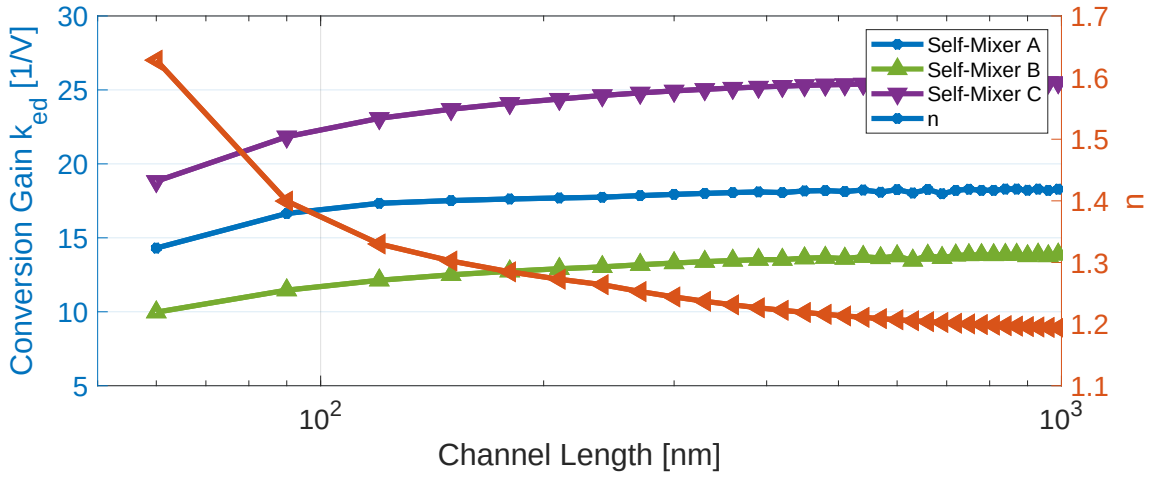


Figure 3.9: Simulated conversion gain constant k_{ed} as a function of the channel length for self-mixer A and B shown in Fig. 3.3 and self-mixer C shown in Fig. 3.6 implemented in 65 nm CMOS LP technology.

Theoretically, n cannot be reduced below 1, leading to a sub-threshold slope of 60 mV/decade. Recent work on Nanowire FET's [33] proposes an achievable sub-threshold slope of 6 mV/decade and can be promising for future designs.

Chapter 4: A Sub-nW Wake-Up Receiver using Self-Mixer

Wake-up receivers with a high-Q RF L-C matching network to provide high passive gain followed by an energy detector for sensing the RF signal can operate at less than 10 nW. The previous chapter discussed the requirement of a self-mixer for optimizing such a receiver front end. This chapter uses this proposed front end to outline the design of a sub-nW wake-up receiver.

The differential self-mixer architecture requires a balun for implementation and can be lossy, here a single-ended RF input self-mixer architecture is used. The receiver implementation uses a 65 nm CMOS technology to reduce the input capacitance to 44 fF compared to a 144 fF input capacitance for a differential RF input self-mixer in 0.13 μm CMOS technology [34]. This chapter discusses the performance of three different prototypes operating at 151 MHz, 434 MHz and 1.016 GHz.

4.1 Receiver Architecture

Fig. 4.1 shows the proposed wake-up receiver architecture. In this work we are assuming an 11-bit wake-up code is OOK modulated at data-rate f_{DATA} = 100 bps on an RF carrier. The receiver has a high-Q LC matching network followed by a multi-stage gate-biased self-mixer (Section 4.2). The multi-stage gate-biased self-mixer has a low input capacitance, and minimizes the added noise while not affecting the conversion gain. The output of the self-mixer is amplified using a current-reuse inverter-based voltage amplifier. Time-encoded clocked integration using clock-triggered voltage-controlled delay lines (VCDL) is used to implement a matched filter for the rectangular-bit shape (details in Section 4.3.3) to reduce baseband noise. The outputs of the clocked VCDLs are compared using a phase-frequency detector (PFD); the PFD UP/DOWN output pulses drive a Set-Reset latch. This effectively implements a comparator or a 1-bit ADC for the time-encoded

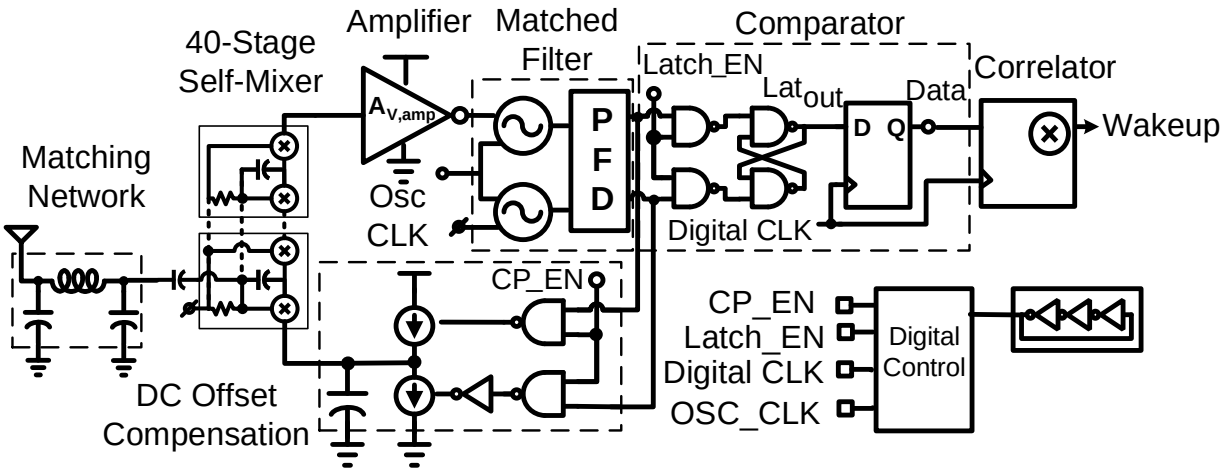


Figure 4.1: Proposed architecture using self-mixers and a baseband consisting of a matched filter, DC offset compensation and comparator implemented with time-encoded analog signals followed by a correlator.

signal.

The comparator is clocked at a sampling rate $f_s = 2f_{DATA}$ and this 2x oversampling eliminates the need for a clock-and-data-recovery circuit (CDR) for clock synchronization [23, 24].

The PFD output pulses are also fed back to the self-mixer reference node via a charge pump. This creates a first order, low bandwidth, delay-locked loop (Section 4.3.5) to reject the DC signal due to any DC offsets introduced by the baseband signal processing circuits or due to a continuous-wave interferer at the receiver input.

4.2 Front-End Design using Self-Mixer

Let's assume the RF input signal, $v_{in}(t)$, is AM modulated signal at a carrier frequency f_{RF} and is incident on an antenna with a radiation resistance R_s. The root-mean squared (RMS) voltage signal at the antenna is $v^2_{in,RMS} = P_{in}R_s$ where P_{in} is the received signal power.

The L-C matching network amplifies this voltage with a passive voltage gain $A_v = v_{edin}/v_{in}$. This A_v depends on the load resistance $R_{in,ed}$ and the capacitance C_{in}. Typically, C_{in} is a combination of the capacitances from the off-chip inductor, package, bond-wire, on-chip electrostatic

discharge (ESD) circuit, and self-mixer or energy detector. Assuming that an inductor with value $L_{ind} \approx 1/(\omega_{RF}^2 C_{in})$ is available with a self-resonance frequency much higher than $\omega_{RF}/(2\pi)$ and an available quality factor Q_{ind}, the optimal $R_{in,ed}$ using (2.18) is $R_{in,ed} = Q_{ind}/(\omega_{RF} C_{in})$ E.g., for a Q_{ind} of 80 and a capacitance C_{in} of 1 pF at 434 MHz, the optimal $R_{in,ed}$ for the self-mixer is 30 kΩ. The passive gain from the matching network is then $A_v = \sqrt{R_{in,ed}/(2R_s)}$.

4.2.1 Conversion Gain and Noise of the Self-Mixer

The conversion gain and noise for a single-ended RF input self-mixer is evaluated in Chapter 3. The conversion gain constant k_{ed} is $N/(2nV_t)$. The output noise PSD is also evaluated in Chapter 3 and can be written as $PSD_{vn,edo} = 4k_B T N^2 R_{in,ed}$.

The receiver sensitivity for a continuous-wave RF input signal as a function of self-mixer $R_{in,ed}$, matching network A_v, baseband noise-figure NF, required SNR_{req} and baseband sampling rate f_s is:

$$\begin{aligned} Sensitivity|_{dBm} = &\frac{1}{2}(SNR_{req}|_{dB} + NF|_{dB}) - A_v|_{dB} \\ &+ 10log\left[\sqrt{\frac{4k_B T R_{in,ed} f_s (2nV_t)^2}{R_s^2}}\Bigg/ 1mW\right] \end{aligned} \tag{4.1}$$

4.2.2 Gate-Leakage Compensation and Biasing Circuit

Fig. 4.2 shows the implementation of the self-mixer and the baseband amplifier. The source of the self-mixer, V_{EDREF}, is floating and connected to a 20 pF capacitor that is driven by a charge pump; this creates a DC feedback loop that will be discussed in Section 4.3.5. The output of the self-mixer, $v_{ed,bbo}$, is connected to the baseband-amplifier NMOS transistor M_{A1}. The self-mixer operates in the linear region, and the DC gate potential of M_{A1} is the same as DC potential at V_{EDREF}.

The DC gate bias V_{G_B} of the self-mixer leads to a gate-to-drain leakage current. If uncompensated, this current would increase the potential V_{EDREF}, negating the effect of gate-biasing. Fig. 4.2

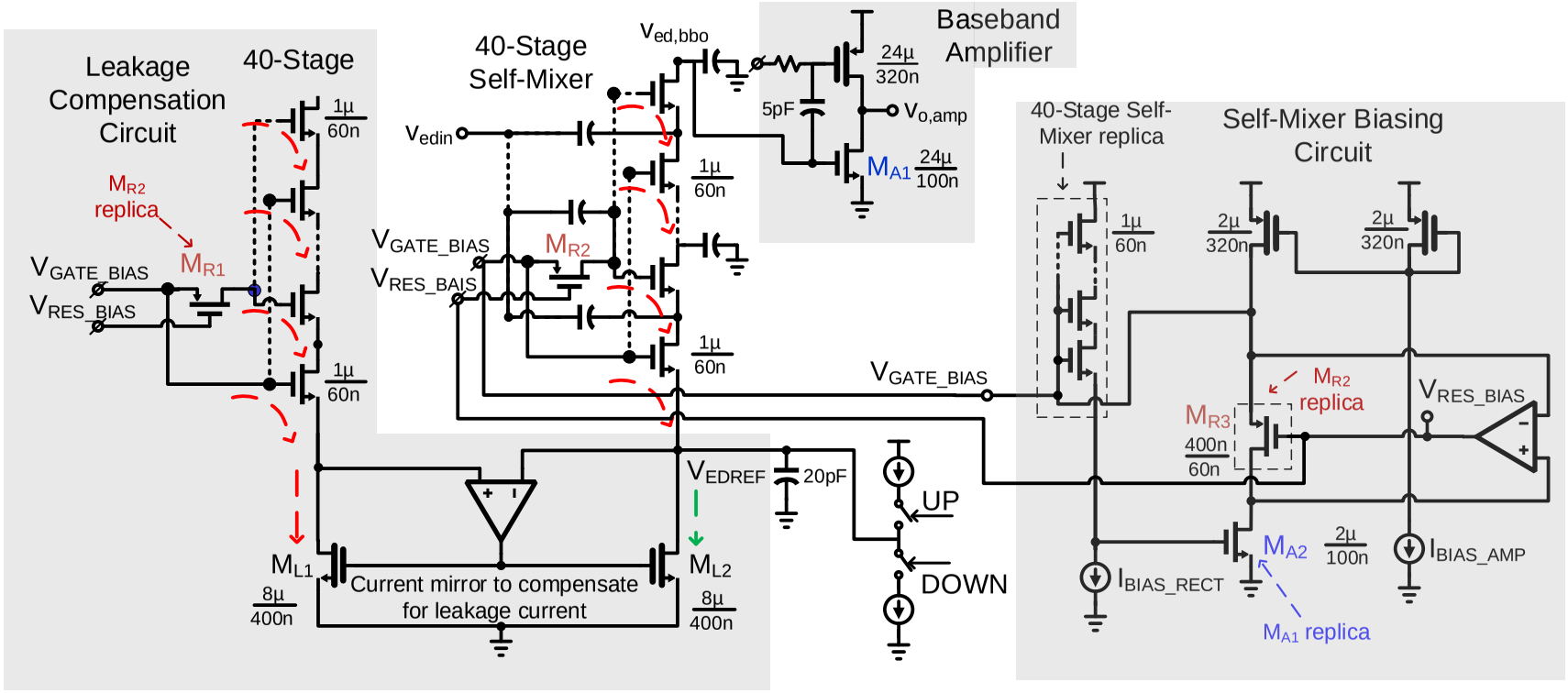


Figure 4.2: Self-mixer and baseband amplifier design, self-mixer biasing circuit and self-mixer gate-leakage compensation circuit details. Here, transistors $M_{R1} - M_{R3}$ operate as resistors.

shows the leakage-compensation circuit where a replica self-mixer (without C_C and C_L) is used to sense the leakage current using transistor M_{L1}; this current is mirrored to M_{L2} and compensates for the leakage in the self-mixer. A varying V_{EDREF} can change the leakage current. Therefore, the operational amplifier in the leakage-compensation circuit keeps track of the potential V_{EDREF} on the replica self-mixer circuit for accurate current mirroring.

Fig. 4.2 also shows the biasing circuit to generate V_{G_B} and V_{RES_BIAS}. A replica of the NMOS transistor M_{A1} is M_{A2}. A series of 40 transistors are used with each transistor the same size as in the 40-stage self-mixer to keep track of the threshold variations. This is operated as a source follower with a drain current source of I_{BIAS_RECT}. The current source I_{BIAS_AMP} sets the gate-to-source potential for M_{A2}. The current source I_{BIAS_RECT} sets the potential V_{G_B}. This current-controlled biasing technique makes the self-mixer resilient to voltage and process variations.

Transistor M_{R2} is biased as a resistor for AC-coupling the RF signal in the self-mixer. A replica transistor M_{R3} is used to generate the bias potential V_{RES_BIAS} for setting the resistance of M_{R2}.

4.3 Receiver Prototype Implementation

Fig. 4.3 shows the transistor-level implementation details of the wake-up receiver chip that was implemented in 65 nm LP CMOS.

4.3.1 RF Front End

Three receivers were prototyped operating at 151.25 MHz, 434.4 MHz and 1.016 GHz using the matching network design in Fig. 4.3 with the component values below:

Frequency	L_{ind}	Inductor Details	C_1
151.25 MHz	1 μH	26 AWG Cu 13 turns	30 pF
434.4 MHz	111 nH	132-10SM Coilcraft	14 pF
1.016 GHz	27 nH	0908-SQ Coilcraft	3.3 nH

The Q-factor of the capacitors degrades with increasing frequency. For the 1.016 GHz prototype, we use a matching network with 3.3 nH inductor instead of the capacitor C_1 to reduce losses. The

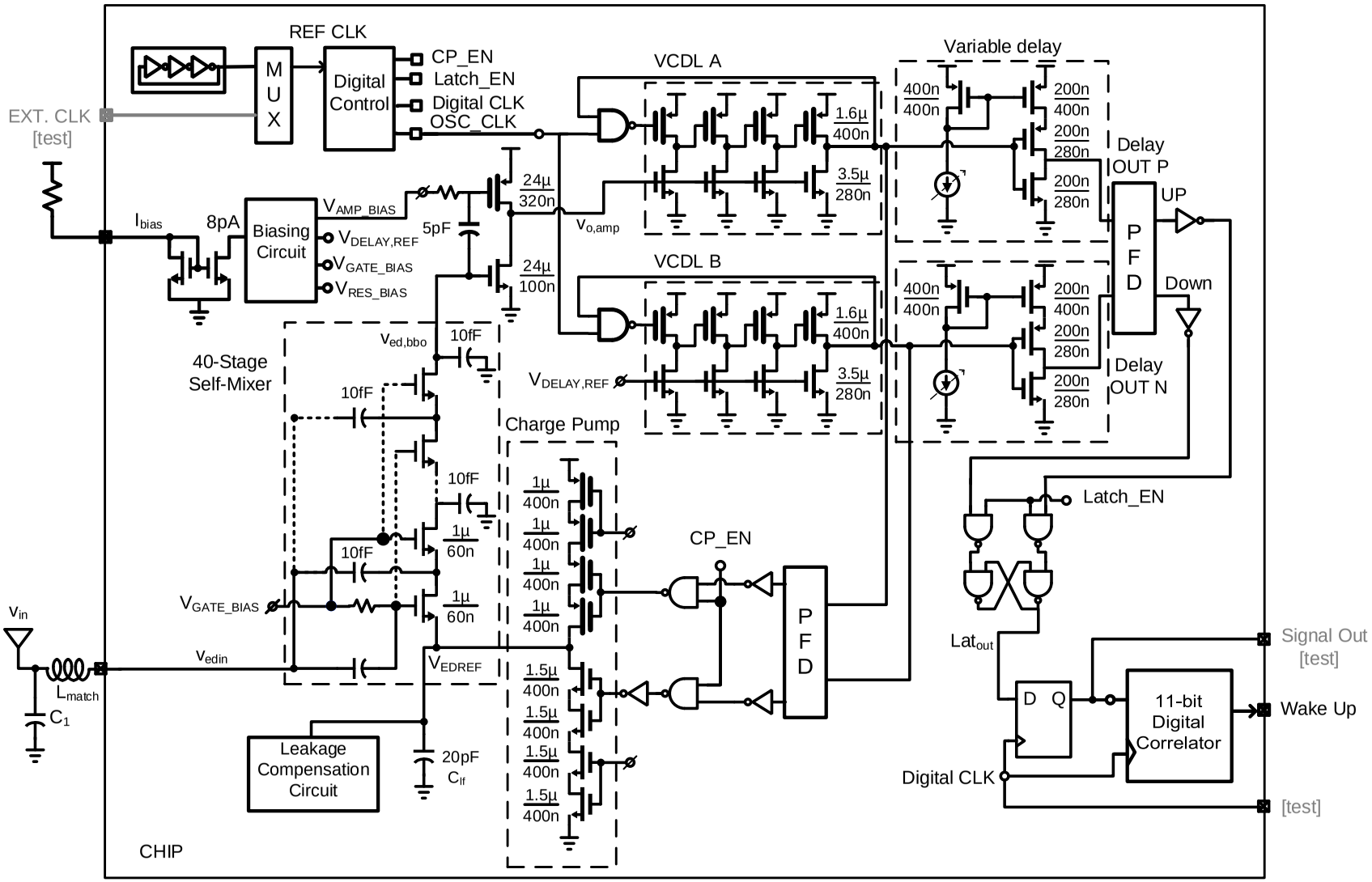


Figure 4.3: System architecture with self-mixer, voltage-controlled delay lines (VCDL), charge-pump, variable delay including transistor-level implementation details.

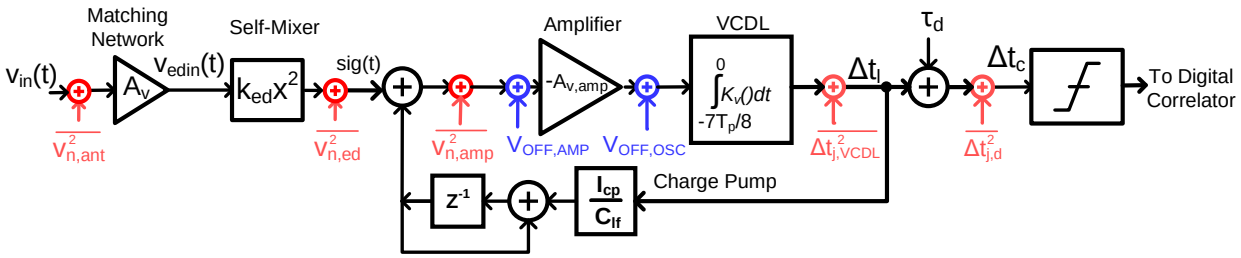


Figure 4.4: Multi-domain model of the proposed receiver with added DC offsets and noise from the receiver chain.

output of the matching network is connected to the 40-stage self-mixer with an $R_{in,ed}$ of 200 kΩ at 151 MHz and 434.4 MHz and 50 kΩ at 1.016 GHz. The source of the multi-stage self-mixer $V_{edref} = V_{EDREF} + v_{edref}(t)$ is connected to a delay-locked loop (DLL) discussed in Section 4.3.5.

4.3.2 Baseband Voltage Amplifier

The self-mixer output, $v_{ed,bbo}$, is amplified by gain $(-A_{v,amp})$ of 26 dB using a current-reuse baseband amplifier with output $v_{o,amp}(t)$ (Fig. 4.3). Its input-referred noise is $2kTn/(g_m)$; assuming $n = 1.2$ and $g_m/I_d = 29$, an $I_d = 370$ pA, the amplifier NF compared to the self-mixer output noise ($R_{in,ed} = 200$ kΩ) is 1 dB while the power consumption is only 150 pW at 0.4 V. The PMOS transistor is current biased using a current mirror with AC coupling while the NMOS transistor is biased through the DC feedback loop created by the DLL discussed in Section 4.3.5. Additionally, the DLL provides a high-pass response in the signal path and rejects the low-frequency flicker noise added by the amplifier.

4.3.3 Baseband Signal Processing with Time-Encoded Signals

The sensitivity optimization carried out in Section 2.5 optimizes the noise power spectral density for optimal SNR, but the integrated noise power needs to be minimized before digitization. Wake-up receivers generally use a 1-bit comparator. For such a comparator, a windowed integrator serves as a matched filter to optimally filter the baseband signal to receive a rectangular bit shape.

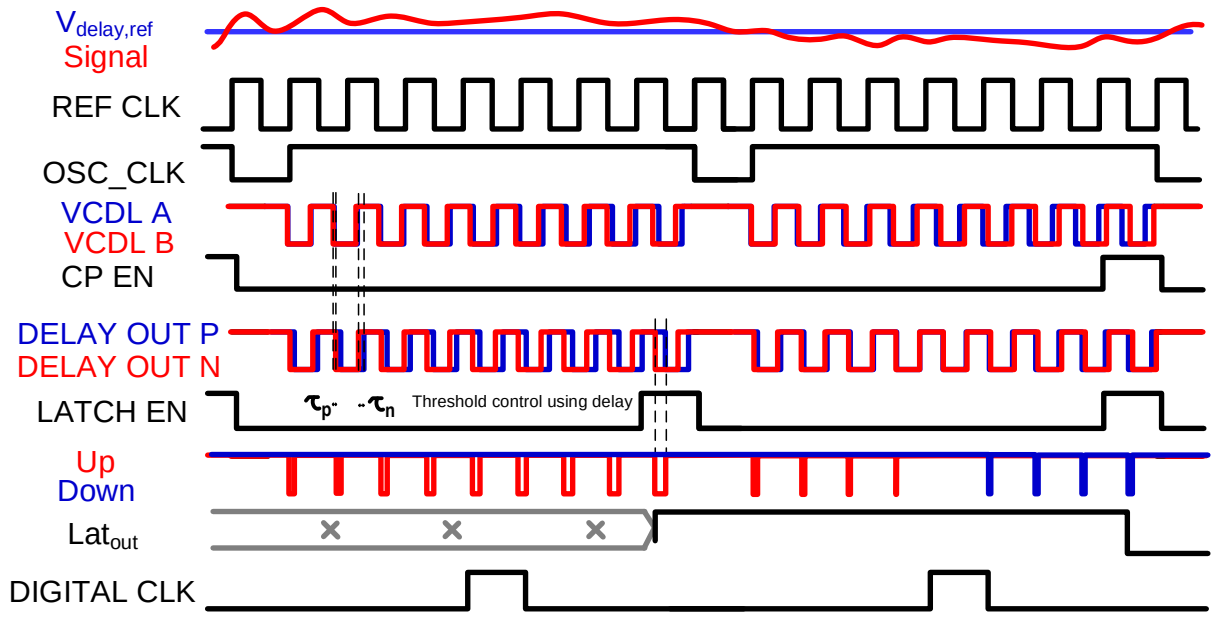


Figure 4.5: Operation of the Integrator and comparator using time-encoded signals with VCDLs, SR latch and current starved inverter delay cells.

Windowed Integrator using a Voltage-Controlled Delay Line and Time-Encoded Signals

A windowed integrator implementation using time-encoded analog signals was proposed in [35] for power-efficient ADCs, and can be adapted to be used as a matched detector for the rectangular bit shape; it filters the high-frequency baseband noise and ensures that the noise bandwidth is f_s to optimize the SNR before sampling.

Two voltage-controlled delay lines (VCDLA and VCDLB) (Fig. 4.3) with clocked feedback realize a V-to-T signal conversion and time-encoded integration. The operation principle is illustrated in Fig. 4.5. The rising-edge of the OSC_CLK triggers oscillation in VCDLs, with the frequency controlled by its respective input voltage, $V_{o,amp}$ and $V_{DELAY,REF}$. At the falling-edge of OSC_CLK, the relative position of the edges in VCDLs has the information of the output phase (relative delay), effectively integrating the input signal when OSC_CLK is 'high'. For an OSC_CLK time period T_p, the VCDLs integrate the signal for a time of $7T_p/8$ and remain in reset mode for the rest of the period. This is ensured by deriving the OSC_CLK from an 8x REF_CLK generated

using an on-chip current-starved ring oscillator. Assuming the DC output of the amplifier is set as $V_{DELAY,REF}$ using the DC feedback for the DLL(Section 4.3.5), the difference of the output pulse widths of the two VCDLs is:

$$\Delta t_l[kT_p] = \int_{(k-7/8)T_p}^{kT_p} K_{vco}T_{vco}v_{o,amp}(t)dt \tag{4.2}$$

where K_{vco} is the voltage-to-frequency conversion gain and $T_{vco} = 1/f_{vco}$ is the time period when VCDLA is operated as a VCO, and k is the index for the discrete-time samples. In z-domain:

$$\Delta t_l(z) = \frac{-7}{8}A_{v,amp}K_{vco}T_{vco}T_p\frac{V_{edref}(z)}{z} + sig(z) \tag{4.3}$$

where $sig(z)$ is the Z-transform of the discrete samples $sig[kT_p]$ given by [36]:

$$sig[kT_p] = -A_{v,amp}K_{vco}T_{vco}\int_{(k-7/8)T_p}^{nT_p} v_{edo}(t))dt \tag{4.4}$$

This will be used to evaluate the time-domain response of the DLL in Section 4.3.5.

Comparator for Time-Encoded Signals

At the end of the OSC_CLK 'high' pulse, Δt_l is measured using phase-frequency detector (PFD). The relative pulse-widths of the UP/DOWN pulses provides a measure if $\Delta t_l \geq 0 | \Delta t_l \leq 0$. These UP/DOWN pulses trigger an SR-latch to operate as a comparator. The output of the SR-latch is sent to an 11-bit digital correlator discussed in Section 4.3.4.

A non-zero threshold for the comparator needs to be set for a low false-alarm rate. The DLL(Section 4.3.5) sets $\Delta t_l = 0$ at the output of the VCDLs. Additional current-starved inverter delay cells in the signal and reference path with a different delay (τ_N and τ_P) are added in each branch after VCDLs to set the threshold. The required threshold for false alarm $< 1/Hr$ is evaluated in Section 4.4.4.

4.3.4 Digital Correlator

The receiver does not do data-clock recovery but uses 2x oversampling to receive the wake-up code [23, 24]. As a result, either the even or the odd samples will be aligned with the incoming data signal. The on-chip 100 pW 11-bit sliding-window digital correlator skips every alternate bit and thus correlates with the most reliable data. D-flipflop shift registers keep the last twenty-two samples, XOR gates multiply the received code with the desired wake-up code, and a 4-bit full-adder sums the XOR outputs; the adder output is then compared with a correlation threshold.

4.3.5 Delay-Locked Loop for DC Feedback

$\Delta t_l[kT_p]$ is also sensed using a separate PFD and is fed back to the reference input of the self-mixer using a charge pump with a load capacitor C_{lf} as shown in Fig. 4.3. The loop sets $\Delta t_l = 0$ at DC, thus forming a delay-locked loop. This sets the amplifier output DC potential equal to V_{EDREF}, which then biases the voltage amplifier as well.

The charge-pump output can be written as $v_{edref}[kT_p] = v_{edref}((k-1)T_p) + I_{CP}\Delta t_l(kT_p)/C_{lf}$, where I_{CP} is the charge-pump current of 1 pA and C_{lf} is a load capacitor of 20 pF. This feedback loop is enabled for every alternate sample for a time of $T_p/8$ at the end of integration cycle controlled by CP_EN in Fig. 4.5. The discrete-time operation of the DLL [37] justifies the use of a Z-domain model for analysis (see Fig. 4.4). The Z-domain transfer function from $sig(z)$ to $\Delta t_l(z)$ is:

$$\frac{\Delta t_l(z)}{sig(z)} = \frac{1 - z^{-1}}{1 - (1 - G_{loop})z^{-1}} \tag{4.5}$$

where loop gain: $G_{loop} = (7T_p/8)A_{v,amp}K_{vco}T_{vco}I_{CP}/C_{lf}$. The transfer function represents a high pass filter with a cutoff frequency of $f_s/100$, with f_s=200 Hz in this prototype.

The theoretical and measured response of the receiver at the output of the VCDLs to the desired wake-up code of "11100100110" is shown for a receiver prototype operating at 1.016 GHz in Fig. 4.6. It shows a DLL settling time of 50 mSec, which limits the number of consecutive '1's in the wake-up code to three; if the code requires more consecutive '1's, RZ-encoding or Manchester

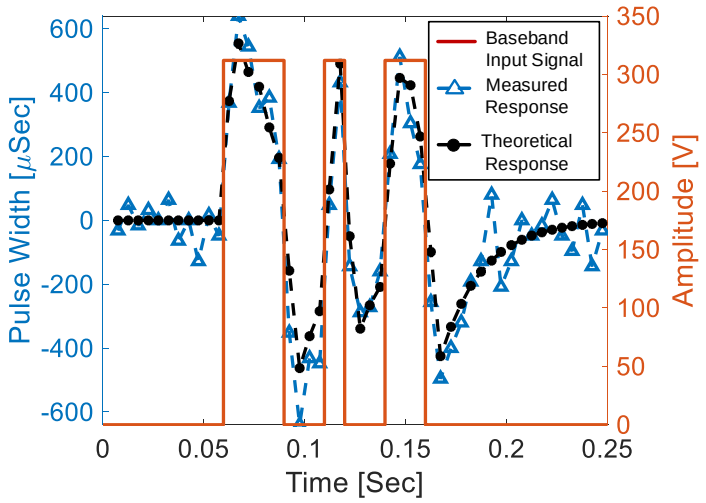


Figure 4.6: Theoretical and measured receiver transient response for a −75 dBm RF input signal modulated with the baseband input signal for the 1.016 GHz prototype.

encoding can be used [1].

Stability

The region of convergence (ROC) is defined by $|z| > |(1 - G_{loop})|$. For a causal and stable LTI system, the ROC must extend the outermost pole to infinity and must include the unit circle $|z| = 1$. Therefore, G_{loop} must be less than 1. This sets the charge-pump current I_{CP} and capacitance C_{lf}.

Offset Cancellation

The amplifier and the VCDLs add random DC offsets modeled as $V_{OFF,AMP}$ and $V_{OFF,OSC}$ in Fig. 4.4. The charge pump in the feedback loop creates a zero at DC, so that the DC offsets are rejected. Thanks to this baseband offset cancellation, very small transistors can be used in the VCDLs, even though they introduce larger mismatches, and the VCDLs can operate with only 50 pW each.

4.4 Power Consumption Limit

Achieving a low baseband noise figure sets a minimum power consumption from the baseband, given the self-mixer design. We now discuss the power consumption limits for the baseband blocks based on the noise contribution of the 40-stage self-mixer with $R_{in,ed} = 200\,\text{k}\Omega$.

In the multi-domain model in Fig. 4.4, the self-mixer noise at the output is $\overline{v_{n,ed}^2}(f)$, the input-referred amplifier noise is $\overline{v_{n,amp}^2}(f)$, and the VCDL and delay cell added jitter is modeled as $\overline{\Delta t_{j,VCDL}^2}$ and $\overline{\Delta t_{j,d}^2}$ respectively. The baseband noise factor referred to the self-mixer can then be written as:

$$NF_{edref} = 1 + \frac{\overline{v_{n,amp}^2}}{\overline{v_{n,ed}^2}} + \frac{\overline{\Delta t_{j,VCDL}^2}}{\overline{\Delta t_{j,ed}^2}} + \frac{\overline{\Delta t_{j,d}^2}}{\overline{\Delta t_{j,ed}^2}} \tag{4.6}$$

where $\overline{\Delta t_{j,ed}^2}$ is the jitter contribution due to self-mixer at the output of the VCDL. The noise PSD for the self-mixer is given by $\overline{v_{n,ed}^2}(f) = 4k_BTR_{out,ed}$. This is integrated by the VCDL for a period $7T_p/8$, thus ignoring the effect of high-pass filter due to the loop, $\overline{\Delta t_{j,ed}^2} = (7T_p/8)K_{vco}^2T_{vco}^2A_{v,amp}^2 4k_BTR_{out,ed}$.

4.4.1 Noise Contribution of the Amplifier

Assuming an amplifer current consumption of $I_{D,AMP}$, the associated g_m is $I_{D,AMP}/(nV_t)$. Thus, the input-referred noise contribution from the current-reuse amplifier is:

$$\frac{\overline{v_{n,amp}^2}}{\overline{v_{n,ed}^2}} = \frac{nV_t\gamma}{2I_{D,AMP}R_{out,ed}} \tag{4.7}$$

For $R_{out,ed} = 320\,\text{M}\Omega$, the amplifier requires 313 pA of current for a 10% contribution in noise.

4.4.2 Jitter Contribution from the Voltage-Controlled Delay Line

A VCDL implemented using a gated ring oscillator is used for analysis as shown in Fig 4.3. Assuming $I_{D,1}$ to be the current for each stage in the ring oscillator, the total oscillator power

consumption can be written as:

$$P = N_{osc} I_{D,1} V_{DD} \tag{4.8}$$

where N_{osc} is the number of stages in the ring oscillator and V_{DD} is the oscillator supply. Assuming f_{vco} as the operating frequency of the ring oscillator, which can be written as:

$$f_{vco} = I_{D,1}/(2\eta N_{osc} q_{max}) \tag{4.9}$$

where $I_{D,1}$ is the current in a single stage, q_{max} is the maximum change in charge during a transition for each stage in the oscillator and η is a proportionality constant close to 1.

Further assume Γ is the time-varying impulse sensitivity function (ISF) defined for one period for each stage in the ring oscillator [38]. An approximate value of the RMS of Γ is [39]:

$$\Gamma_{RMS} = \sqrt{\frac{2\pi^2}{3\eta^3}} \frac{1}{N_{osc}^{1.5}} \tag{4.10}$$

The VCDL is used to integrate for a period of $7T_p/8$ (see Section 4.3.3), so the integrated jitter at the end of the clock period can be computed using the jitter analysis in [38]:

$$\overline{\Delta t_{j,VCDL}^2} = \frac{1}{2 f_{vco}^2} \frac{\overline{i_n^2}/\Delta f}{q_{max}^2} \Gamma_{RMS}^2 \frac{7T_p}{8} \tag{4.11}$$

The drain current noise spectral density in weak-inversion saturation region is given by:

$$\frac{\overline{i_n^2}}{\Delta f} = 4kT\gamma g_m = \frac{4kT\gamma I_d}{nV_t} \tag{4.12}$$

Now, combining (4.9), (4.10) and (4.12), we obtain:

$$\overline{\Delta t_{j,VCDL}^2} = \frac{4kT\gamma\pi^2}{2\eta n V_t I_{D,1}} \frac{7T_p}{8} \tag{4.13}$$

Thus, the baseband amplifier input referred noise contribution from the VCDL is:

$$\frac{\overline{\Delta t^2_{j,VCDL}}}{\overline{\Delta t^2_{j,ed}}} = \frac{\gamma \pi^2}{2\eta n V_t I_{D,1OSC} K^2_{vco} T^2_{vco} A^2_{v,amp} R_{out,ed}} \tag{4.14}$$

For a 10% noise contribution from the VCDL, using a simulated $K_{vco}T_{vco} = 24\,/\mathrm{V}$, $A_{v,amp} = 20$, $n = 1.4$, the one-stage current required is 13 pA. Please note that the noise analysis is performed to get an estimate of the order of magnitude of the power consumption. The exact analysis may vary at such low-power operation.

4.4.3 Jitter Contribution from the Delay Cells that Control the Comparator Threshold

Current-starved delays that control the comparator threshold add extra jitter as well. For a τ_d delay operating with a current $I_{D,DEL}$ using a PMOS current mirror in weak-inversion, saturation region, the jitter is $\overline{\Delta t^2_{j,d}} = 4kT\gamma\tau_d/(I_{D,DEL}nV_t)$.

Assuming the delay threshold required by the delay cell is $M\sqrt{\overline{\Delta t^2_{j,ed}}}$, where M is a scaling constant, the jitter added by the delay cell compared to the jitter added by the self-mixer can be written as:

$$\frac{\overline{\Delta t^2_{j,d}}}{\overline{\Delta t^2_{j,ed}}} = \frac{4kT\gamma M}{I_{D,DEL}nV_t\sqrt{\overline{\Delta t^2_{j,ed}}}} \tag{4.15}$$

We evaluate the required value of M next for low false alarms. Here, assuming $M = 10$, for a 10% noise contribution from the delay cell, the current consumption required is 430 fA. Therefore, the delay cell doesn't add much jitter compared to the jitter contribution from the self-mixer.

4.4.4 Threshold Requirement for Low False Alarm

The comparator threshold needs to be set sufficiently large so that there is a low probability to trigger a false wake-up. We now evaluate the required threshold for keeping the false alarm rate less than a desired rate; in this work we have targeted a rate less than $1/Hr$.

The false-alarm probability is the probability that the comparator output is the desired wake-

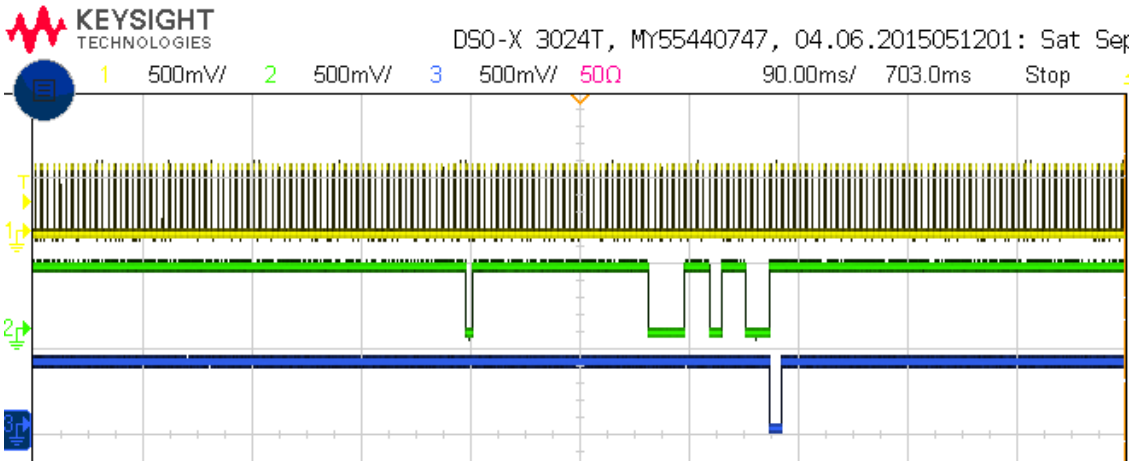


Figure 4.7: Time-domain response to a −79 dBm wakeup signal for 434 MHz receiver prototype demonstrating appropriate threshold for low false alarm $< 1/Hr$.

up code due to the noise present in the receiver. Assuming the receiver sampling rate of f_s, the total number of bits received in an hour are $3600 f_s$. Let H be the number of '1's in a wake-up code. For x-bit error tolerance in the correlator, the total number of false positives generated are $\approx 3600 f_s {}^{H}C_x P^{H-x}$ where P is the probability of comparator output to be '1'. Here, we assume that the probability of receiving a '0' is close to 1 for simplicity. Therefore, P is required to be less than $(1/(3600 f_s {}^{H}C_x)^{1/(H-x)})$ for a false alarm rate $< 1/Hr$. For $f_s = 200\,\mathrm{S}/s$, a desired 11-bit wake-up code "11100100110" received with 1-bit error tolerance, the required P is 4.7%. Assuming a Gaussian noise distribution, the corresponding threshold required is $\tau_d = 1.7\sigma = 1.7\sqrt{\Delta t_{j,ed}^2}$. Thus M is 1.7 in (4.15). Fig. 4.7 shown the response of the receiver to a −79 dBm wake-up signal for 434.4 MHz receiver prototype. Here, the comparator is falsely triggered once in 150 samples, demonstrating appropriate threshold setting for low false alarm rate.

4.4.5 SNR Required to Achieve a Desired Missed Detection Ratio

We can now evaluate the SNR required at the input of the comparator for successful detection of a wake-up code based on the comparator threshold derived above for a given false-alarm rate. For an x-bit error tolerance, the receiver must miss at-least $(x+1)$ bits for missing a wake-up signal. Assuming the probability of missing $(x+2)$ bits or more in a code will be low compared to missing

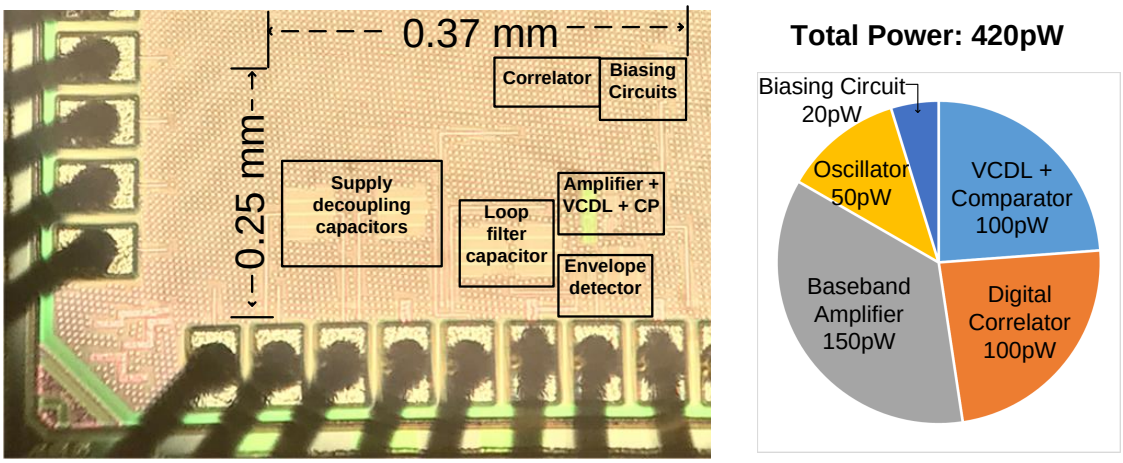


Figure 4.8: DIE micrograph and power consumption distribution for receiver prototype at 434 MHz.

only $(x+1)$ bits, the probability of missed detection is $\approx {}^{H}C_{x+1}P_1^{x+1}$, where P_1 is the probability of a missed bit. For a required missed-detection ratio (MDR) of 10^{-3}, with $N = 6$, and 1-bit error tolerance, P_1 is required to be 0.008, requiring the input signal of the comparator to be 2.4σ above the threshold. Therefore, a total signal amplitude of 4.1σ is required for signal detection, thus requiring a 12.3 dB SNR at the input of the comparator.

4.5 Measurement Results

The micrograph for the 65 nm LP CMOS chip is shown in Fig. 4.8. Wake-up receivers have been built at 151.25 MHz, 434.4 MHz, and 1.016 GHz using three chips with the appropriate matching networks. The measured input reflections, S_{11}, are shown in Fig. 4.9a, with 3-dB bandwidths of 4 MHz, 10 MHz, and 35 MHz. The passive gain achieved from the matching network couldn't be measured due to the high-impedance node at the load. The power consumption for the three receivers operated from 0.4 V measured using an 8.5-digit multimeter is 370 pW, 420 pW, and 470 pW. The breakdown of the power consumption across the various receiver blocks is shown in Fig. 4.8 for the 434 MHz receiver.

An RF carrier OOK-modulated with a 100 bps "11100100110" wake-up code was fed into the receivers to measure the MDR for varying input signal power (Fig. 4.9b); a sensitivity of −79 dBm,

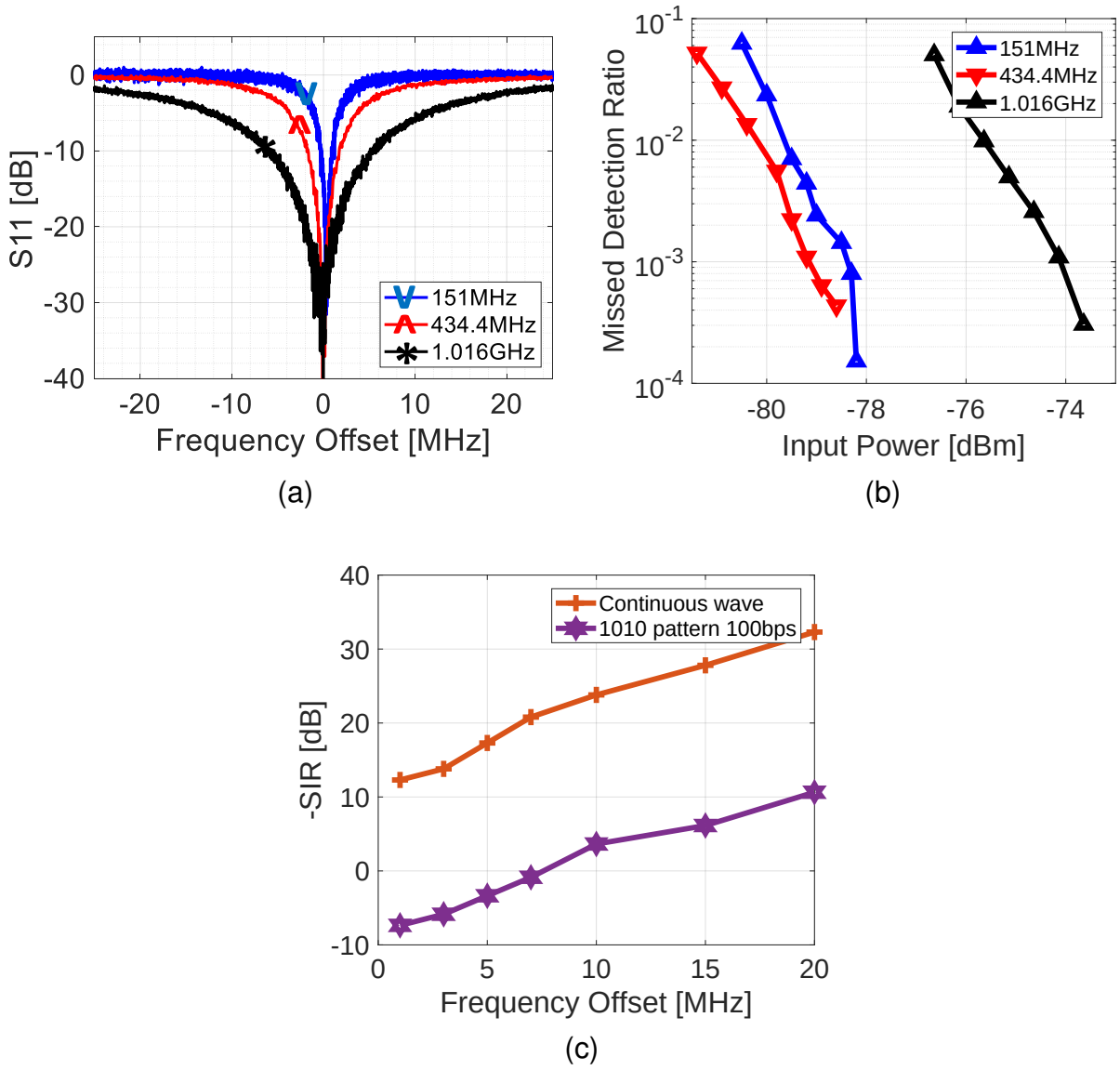


Figure 4.9: (a) Input reflection at 434 MHz and 151 MHz; (b) Missed detection ratio for the receiver at 434 MHz; (c) and Signal-to-interference rejection ratio at 434 MHz for a continuous as well as a worst case AM interferer.

−79.2 dBm, and −74 dBm is achieved for an MDR of $< 10^{-3}$. The 1.016 GHz prototype requires an $R_{in,ed} \approx 10\,\text{k}\Omega$ to achieve the best sensitivity, but the added baseband amplifier noise couldn't be reduced further due to increased flicker noise at higher current consumption. In future work, the receiver can be redesigned for optimal operation at higher frequencies.

The signal-to-interference ratio (SIR) to maintain an MDR of 10^{-3} is measured with the desired signal at −77 dBm (Fig. 4.9c). An in-band interferer overlapping with the desired signal in baseband is generated by 100% OOK modulating an RF carrier with a "1010"-pattern at 100 bps; for this AM interferer, the SIR is −3.7 dB, and 5.8 dB at 3 MHz offset for the 151.25 MHz and the 434.4 MHz receivers; the DLL does not offer rejection to this AM interferer. For a continuous-wave interferer at 3 MHz offset, the SIR is as good as −23.3 dB and −13.8 dB for the 151.25 MHz and 434.4 MHz receivers, thanks to the additional 20 dB rejection by the DLL; the maximum rejection is limited by the dynamic range of the DLL charge pump.

Table 4.1 shows the comparison with the state-of-the-art wake-up receivers. We normalize sensitivity to latency as in [24, 34] for comparison. The receiver provides >8 dB better sensitivity at 434 MHz and 1.016 GHz, and a 3 dB better sensitivity at 151.25 MHz, all at 10 dB lower power consumption compared to the prior art. The figure of merit (Fig. 4.10) is at least 11 dB better than other receivers.

4.6 Conclusions

A wake-up receiver architecture is presented using a multi-stage gate-biased self-mixer and a matched-filter baseband realization using time-encoded signals. A 65 nm LP CMOS receiver chip using a 40-stage MOS RF self-mixer has been presented. Three receiver prototypes at 151.25 MHz, 434.4 MHz and 1.016 GHz have been demonstrated with a −79 dBm, −79.2 dBm, and −74 dBm sensitivity for a missed-detection ratio $< 10^{-3}$ and a 110 ms latency, while consuming 370 pW, 420 pW, and 470 pW from 0.4 V. Sensitivity is largely limited by the front end losses in the matching network. The receiver doesn't provide any selectivity to in-band AM interference even when the interferer operates at a different channel frequency. The next chapter explores a modified

Table 4.1: Comparison between different receiver architectures for IoE

		ISSCC'17	ISSCC'18	SSCL'18	**This Work**	CICC'17	ESSCIRC'17	ISSCC'18	**This Work**	RFIC'17	**This Work**
Frequency range		f_{RF} <200MHz				400MHz < f_{RF} < 600MHz				f_{RF} > 1GHz	
Features		Active Rectifier	Auto-threshold compensation	Pseudo-balun ED	Self-Mixer +DLL	Differential Self-Mixer	Active Rectifier	Auto-threshold compensation	Self-Mixer +DLL	High-Q FE Co-design	Self-Mixer +DLL
Tech Node		180 nm	130 nm	180 nm	65nm LP	130 nm	180 nm	130 nm	65nm LP	65 nm	65nm LP
Frequency	[MHz]	113.5	151.8	109	151.25	550	405	433	434	2400	1016
Modulation		OOK	OOK	OOK	OOK	OOK	OOK	OOK	OOK	OOK	OOK
Chip Rate	[kbps]	0.3	0.2	0.033	0.1	400	0.3	0.2	0.1	2.5	0.1
Code Length		16-bit	16.5-bit	6-bit	11-bit	11-bit	16-bit	16.5-bit	11-bit	32-bit	11-bit
Power	[nW]	4.5	7.4	6.1	0.37	222	4.5	7.4	0.42	365	0.47
Passive Gain	[dB]	25	NR	30.6	26	19	18.5	NR	26	N/A	21
Sensitivity	[dBm]	-69	-76	-80.5	-79	-56.4	-63.8	-71	-79.2	-61.5	-74
Latency	[mSec]	53.5	82.5	180	110	0.0275	53.3	82.5	110	12.8	110
In Band SIR [3MHz off]											
AM Jammer	[dB]	-4	-4	-5	-3.6	-2	4	N/A	5.8	N.R.	N/A
Continuous Wave	[dB]	-11	-30	-5	-23.3	-13	-28	N/A	-14	-19.1	N/A
Normalized Sensitivity[1]	[dBm]	-75.4	-81.4	-84.2	-83.8	-79.2	-70.2	-76.4	-83.4	-71.2	-78.8
FoM[2]	[dB]	-159	-163	-166	-177	-146	-154	-158	-178	-136	-171.2

1. Normalized Sensitivity = Sensitivity + 5.log[Latency/1s]

2. FoM = Normalized Sensitivity + 10.log[Power/1W]

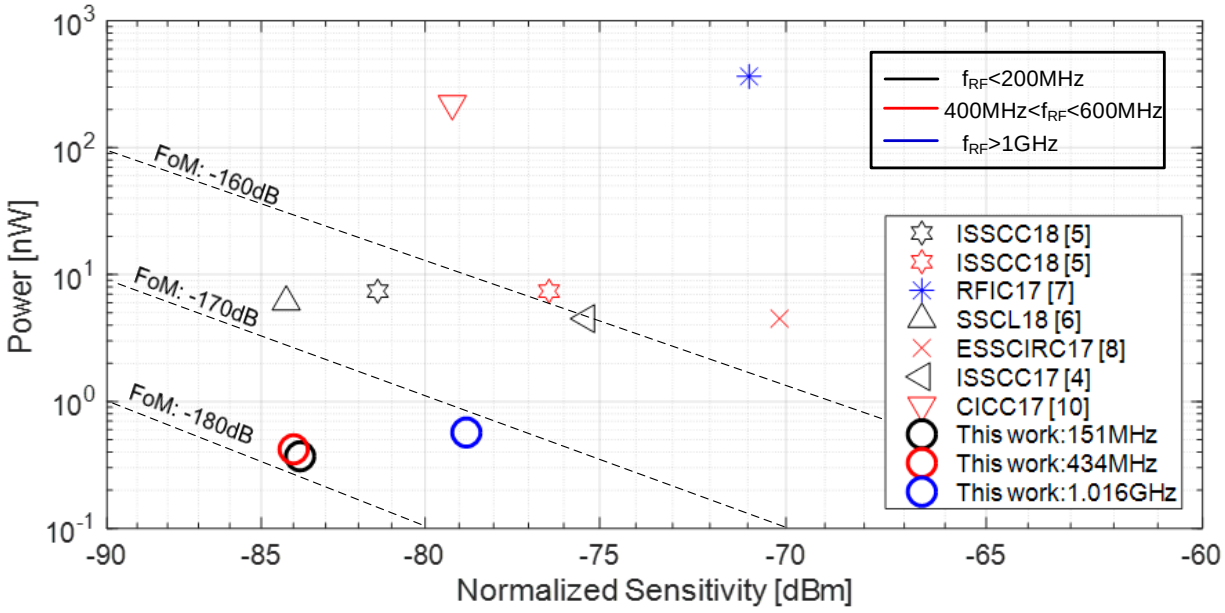


Figure 4.10: Receiver performance comparison to the state of the art using normalized sensitivity and FoM described in [24, 34].

receiver architecture to enhance the sensitivity and the selectivity further.

Chapter 5: Enhancing Sensitivity and Selectivity in Passive-RF Energy-Detecting Receivers

The previous chapter discussed a sub-nW wake-up receiver suitable for relaxed latency of the order of 100 msec. However, the receiver architecture didn't offer any selectivity to in-band AM interference. Here, we discuss a receiver architecture for applications with critical latency, and offer a solution for improving sensitivity as well as selectivity to interference using the concept of interferer as LO. The receiver is designed in 0.13 μm CMOS technology, it uses a passive RF front end with a differential-RF input self-mixer as discussed in Chapter 3. The receiver consumes 222 nW with -56.4 dBm sensitivity at 550 MHz for a 27.5 μsec latency. Using an interferer enhanced mode, the receiver consumes 1.1 μW, it improves the sensitivity with 1 dB/dB increase in the interferer power while providing a 10 dB improved selectivity to narrowband interferers.

5.1 Interferer as LO

Let's assume there is a wanted signal $v_{wanted}(t)$ with amplitude A and OOK-modulated with a data signal $m_{sig}(t)$, which is a sequence of '1's and '0's at a 400 kbps chip rate, and an interferer $v_{int}(t)$ with amplitude B and an amplitude modulation of $m_{int}(t)$ and a phase modulation of $\phi_m(t)$:

$$v_{wanted}(t) = Am_{sig}(t)sin(\omega_{sig}t) \tag{5.1}$$

$$v_{int}(t) = B(1 + m_{int}(t))cos(\omega_{int}t + \phi_m(t)) \tag{5.2}$$

The input to the self-mixer is: $v_{edin} = (v_{wanted} + v_{int})$. The output of the self-mixer then has three components:

$$\begin{aligned} v_{sig,bb} = k_{ed} v_{wanted}^2 &= k_{ed} A^2 m_{sig}^2(t)/2 \\ v_{int,bb} = k_{ed} v_{int}^2 &= k_{ed} B^2 (1 + m_{int}(t))^2/2 \\ v_{mix,if} = k_{ed} v_{wanted} v_{int} &= k_{ed} AB m_{sig}(t)(1 + m_{int}(t)). \\ & \quad sin((\omega_{sig} - \omega_{int})t - \phi_m(t)) \end{aligned} \tag{5.3}$$

where $v_{sig,bb}$ and $v_{int,bb}$ are located close to DC, whereas $v_{mix,if}$ appears at an IF frequency of $\omega_{if} = \omega_{sig} - \omega_{int}$. Fig. 5.1a shows the simulated output signal strengths in the presence of a -60 dBm RF input signal for an increasing level of an interferer with amplitude B. At low interferer powers, where the 4th order harmonics in the self-mixer remain small, $v_{int,bb}$ is $\propto B^2$ and rises 2 dB/dB, $v_{mix,if}$ is $\propto B$ and rises 1 dB/dB whereas $v_{sig,bb}$ remains constant.

Next, we discuss the enhancement in receiver performance based on the type of interferer present at an ω_{if} offset.

5.1.1 Operation with a Continuous-Wave Interferer

Let's assume v_{int} is a constant amplitude sine wave (i.e. $m_{int}(t) = 0$ and $\phi_m(t) = 0$). Fig. 5.3a shows the corresponding spectra at the input and output of the self-mixer. Now, v_{int} acts as LO and mixes with v_{wanted} to generate a copy of the desired signal at the IF frequency as $v_{mix,if}$ while $v_{int,bb}$ is a signal at DC, typically larger than $v_{sig,bb}$. To receive this signal, the proposed receiver architecture is shown in Fig. 5.2. When no strong interferer is present, the baseband signal is amplified and low-pass filtered and then sliced in the *low-frequency (LF) Path*. When the interferer is present, the receiver can operate in an interferer-enhanced mode using the *high-frequency (HF) path,* where the desired signal appears as $v_{mix,if}$ at a low IF in the mixer output. The HF path high-pass filters, amplifies and slices the mixer output and performs an envelope detection to demodulate the signal in this mode. Signal $v_{mix,if}$ increases 1 dB/dB increase in interferer power, whereas, the

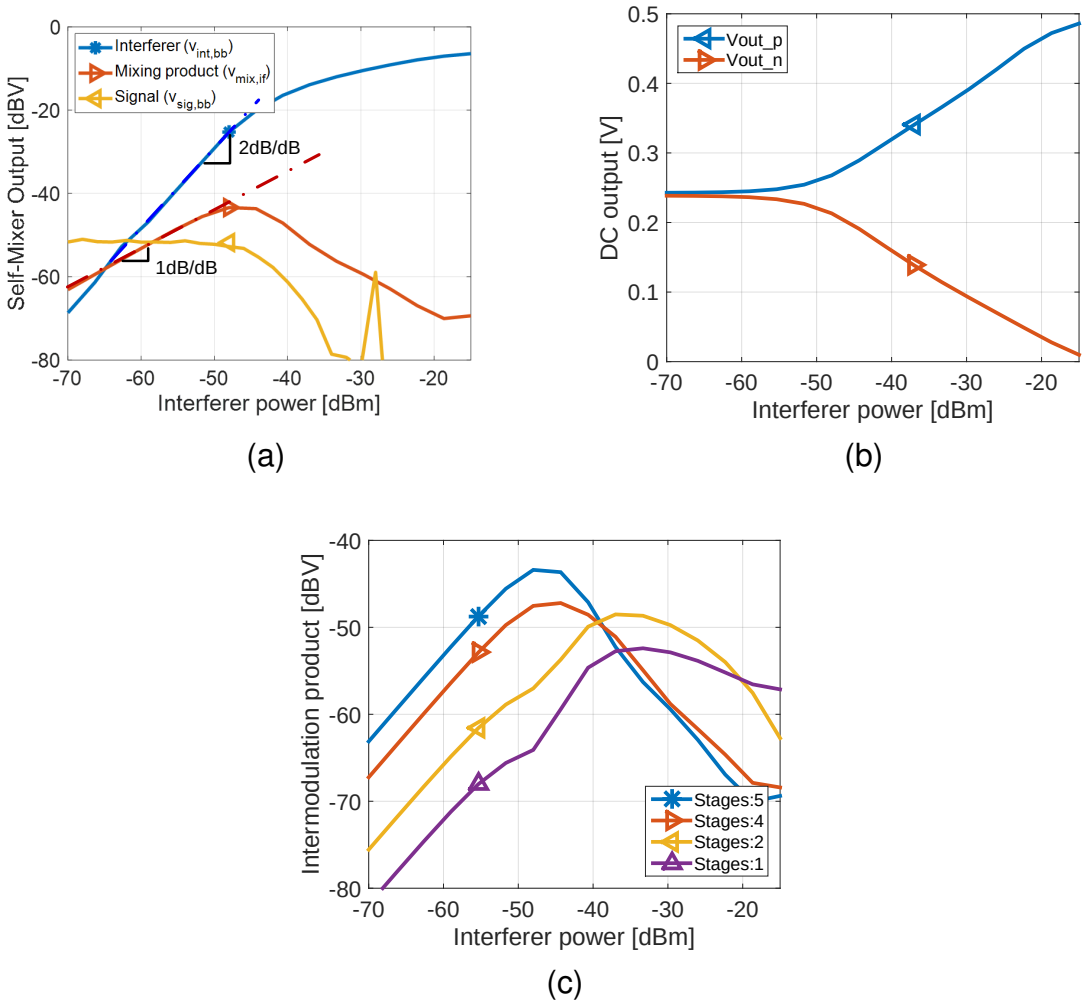


Figure 5.1: For an increasing continuous-wave interferer level at 2MHz offset; (a) the simulated level of the components in the self-mixer output for with a −60 dBm 400 kbps OOK input signal present; (b) the simulated DC-operating points at nodes V_{out_p} and V_{out_n} for self-mixer in Fig. 3.7; (c) and the simulated mixing product $v_{mix,if}$ at different number of stages in the self-mixer in Fig. 3.7.

noise from the self-mixer remains constant. Thus, the sensitivity of the receiver in the HF path improves by 1dB for 1dB increase in the interferer power.

5.1.2 Operation with a PM/FM Interferer

For a strong PM/FM interferer, $m_{int}(t) = 0$, but $\phi_m(t) \neq 0$. However, $v_{sig,bb}$ and $v_{int,bb}$ are independent of $\phi_m(t)$. The $v_{mix,if}$ now carries the amplitude modulation of the signal and the phase

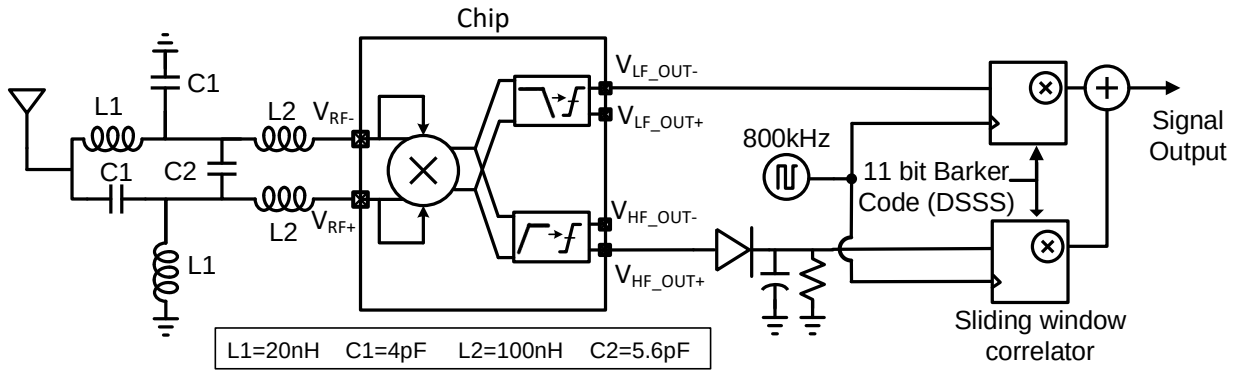


Figure 5.2: Proposed receiver architecture implemented using the proposed multi-stage self-mixer and with an additional HF-path (bottom) for the interferer-enhanced operating mode with enhanced sensitivity and selectivity.

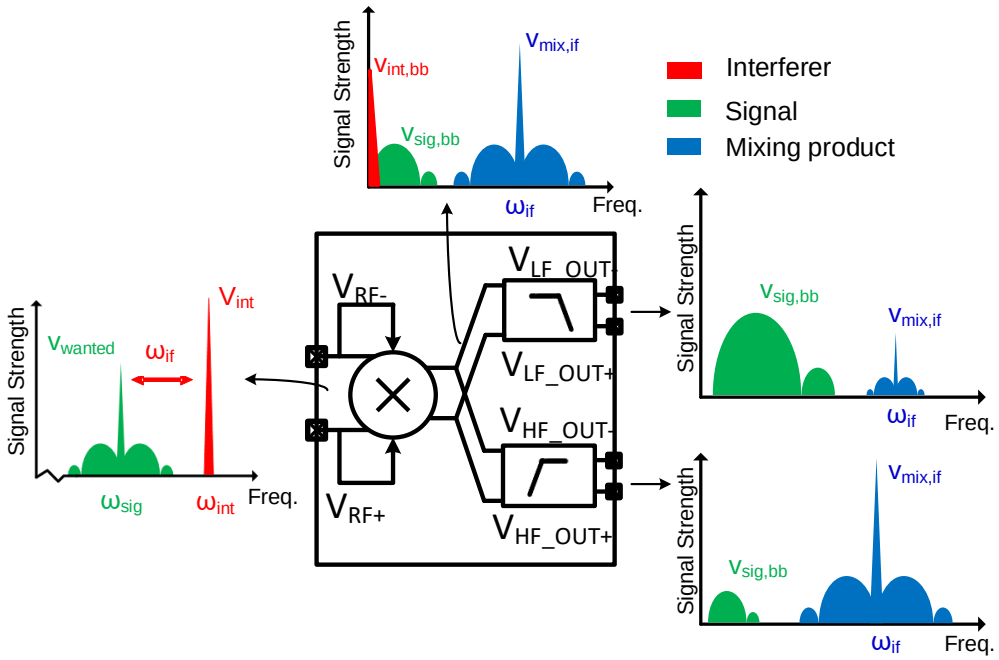
modulation of the interferer. Therefore, the $v_{mix,if}$ is demodulated using envelope detector in the HF path (Fig. 5.2), to make it insensitive to the phase modulation of the interferer. Hence, the receiver treats a PM/FM interferer as a narrowband carrier and has the performance as described above for the signal in the presence of a narrowband carrier.

5.1.3 Operation with an AM Interferer

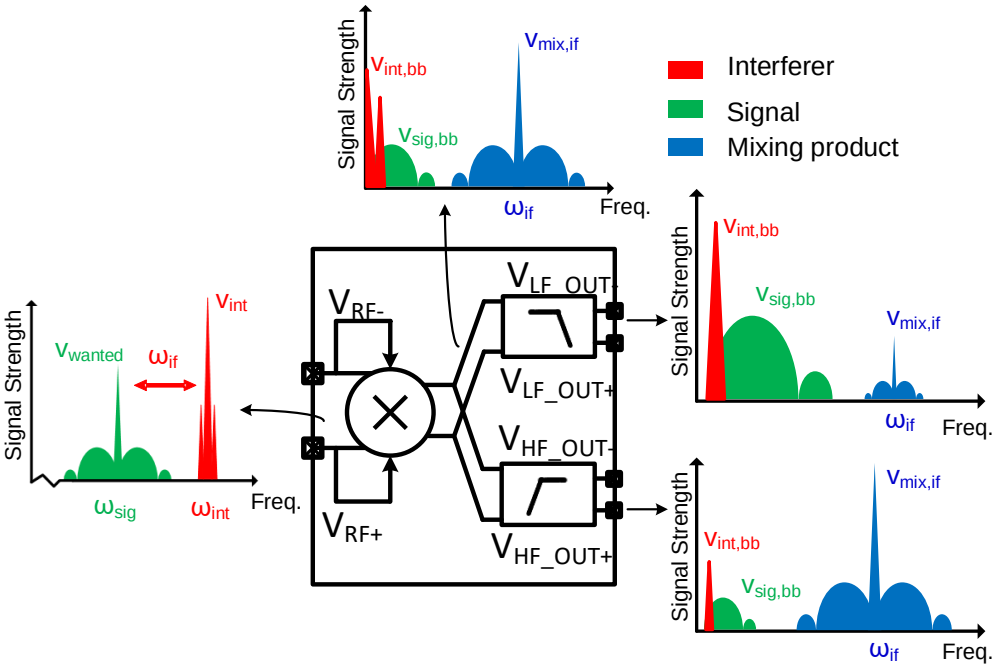
For an AM interferer, $m_{int}(t) \neq 0$ and the spectra at the input and the output of the self-mixer are shown in Fig. 5.3b. The frequency content of the signal $v_{int,bb}$ can overlap with the content of $v_{sig,bb}$ and for a strong AM interferer the LF-path gets blocked.

Let's evaluate the impact on $v_{mix,if}$ in the HF-path. The signal $m_{sig}(t)$ is a random stream of '1's and '0's (middle waveform in Fig. 5.4). For an AM interferer with low-modulation index, i.e. $m_{int}(t) \ll 1$, the $v_{mix,if}$ will have an IF frequency $(\omega_{sig} - \omega_{int})$ output in the presence of '1', and no signal in the presence of '0' (bottom waveform in Fig. 5.4). This signal is then amplified with a limiting amplifier to remove the unwanted AM modulation of $m_{int}(t)$ and the desired signal is retrieved using envelope detection at the IF frequency (Fig. 5.2). For increasing modulation index or modulation frequency of the AM interferer, the rejection of $v_{int,bb}$ through the HPF decreases, and hence the SIR degrades.

The sub-nW receiver in Chapter 4 and the LF path of the proposed receiver get blocked in the



(a)



(b)

Figure 5.3: Signal spectra in the receiver when (a) a narrowband carrier at an offset frequency ω_{if} and (b) an AM interferer at an offset frequency ω_{if} is present

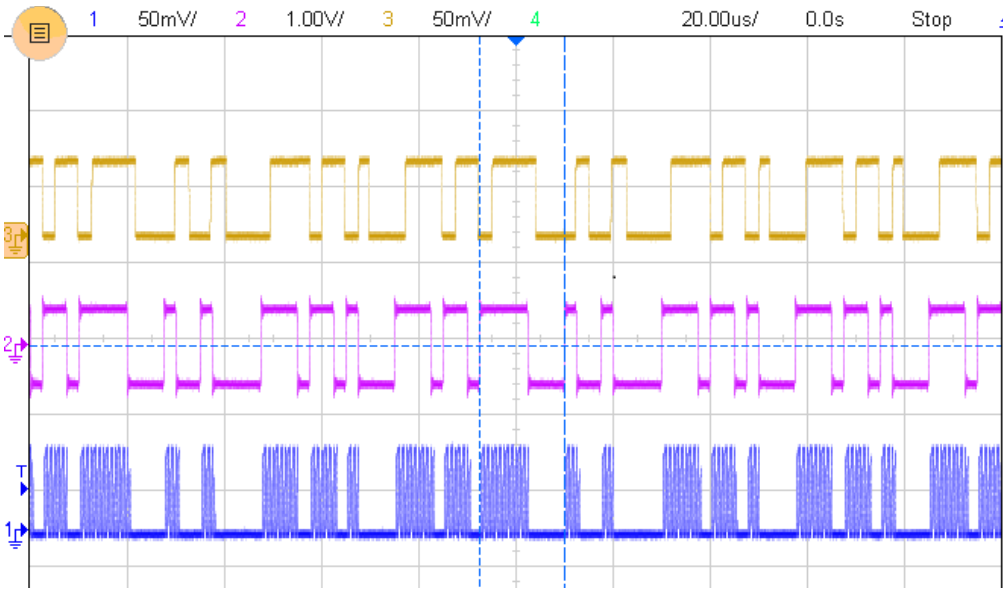


Figure 5.4: Random 1-0 transmitted data pattern (middle); the LF signal (top) reflects the same pattern; the HF output (bottom) shows the same pattern on a 2 MHz IF carrier in the presence of a 10% AM interferer at 2 MHz offset.

presence of AM interferers, but the interferer-enhanced operation via the HF path enables signal demodulation in the presence of AM interferer as well. Additionally, thanks to the improved conversion gain, the sensitivity is improved in the interferer-enhanced operation.

5.1.4 Potential Interferers to the Receiver

To assess the types of interferers possibly present in practical applications, we review the signals associated with the protocols in the 915 MHz ISM band. LoRa, Sigfox, and Weightless-P employ phase or frequency modulation. ZigBee describes channels at 2 MHz spacing with 40 kbps BPSK, 250 kbps O-QPSK, and 250 kbps ASK modulation [40] in this band. To evaluate the impact of an interferer on the receiver, we will present the measured performance of the receiver in the presence of PM, FM and AM modulated interferers in Section 5.3.

5.1.5 Limitations on Enhanced Sensitivity

As the interferer power increases, $v_{int,bb}$ increases, as shown in Fig. 5.1a. For an interferer stronger than -45 dBm, $v_{int,bb}$ is strong enough to change the DC operating point of the self-mixer,

as shown in Fig. 5.1b, thus reducing the effective gate-to-source potential for T1 in Fig. 3.5. This leads to an increase in r_o, and, as a result, a reduction in the bandwidth of the self-mixer and a decrease in the conversion gain for the mixing product $v_{mix,if}$, which limits the enhancement in sensitivity. This is illustrated in Fig. 5.1c where a 2-stage self-mixer has stronger mixing product output than a 5-stage self-mixer for a −30 dBm interferer because of the higher bandwidth offered. For the current prototype, the operation of sensitivity enhanced mode is limited for interferers between −56 dBm and −30 dBm. In future prototypes, the DC potential at V_{out_p} (Fig. 5.1b) can be sensed and used to select the number of stages to be used in self-mixer. At higher interferer powers, the signal can be tapped after fewer stages. This will increase the range of interferer powers over which sensitivity enhancement is obtained.

5.2 Receiver Architecture and Implementation

The receiver front end (Fig. 5.2) first converts the 50 Ω antenna impedance into a 100 Ω differential impedance using a 4-element passive balun with L1=20 nH and C1=4 pF, which is then matched to the self-mixer's input resistance of 25 kΩ using a 3-element matching network with C2=5.6 pF and L2=100 nH having a Q-factor of 30 at 550 MHz. Ideally this offers a 26 dB passive voltage gain, however, the simulated passive voltage gain with finite-Q is 19 dB. RF-to-baseband down-conversion is implemented on-chip with the architecture shown in Fig. 5.5. The differential input capacitance at the RF input of the packaged chip comprises package (including bond-wire), ESD and self-mixer capacitances which are 165 fF, 65 fF and 188 fF respectively. Two-bit on-chip trim capacitors have been included to fine tune the matching network to the desired RF frequency. The matching network is followed by the 10-stage self-mixer presented in Section 3.3.1. When no strong interferer is present, the baseband signal is amplified and low-pass filtered and then sliced in the LF Path. When the LF path is blocked by interference, the receiver operates in an interferer-enhanced mode using the HF path. The operation of the HF path using an interferer as LO is discussed in detail in Section 5.1. The HF path high-pass filters, amplifies and slices the mixer output and performs an envelope detection to demodulate the signal in this mode. The outputs of the

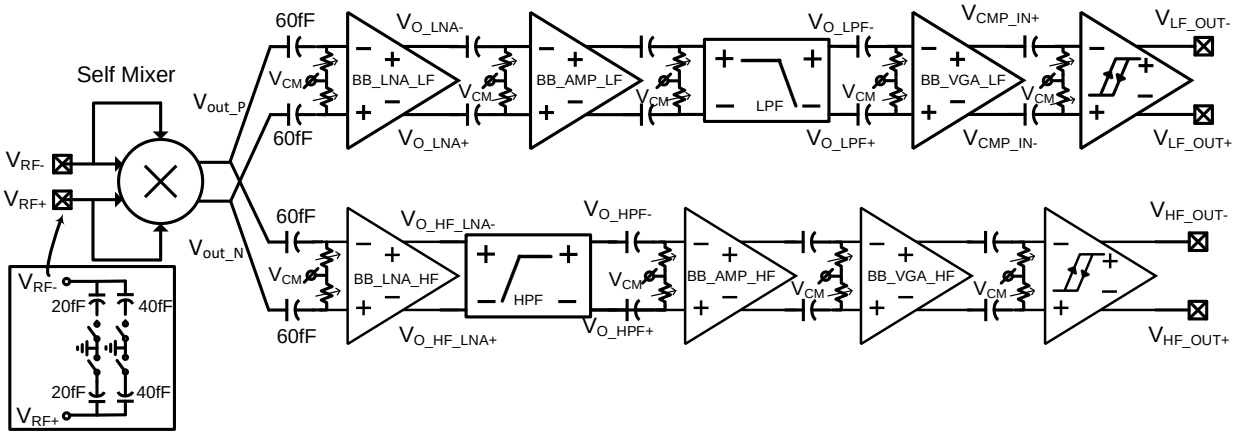


Figure 5.5: Proposed on-chip receiver implementation with LF path (top) and HF path (bottom), 2-bit on-chip input capacitance tunability is provided for the matching network.

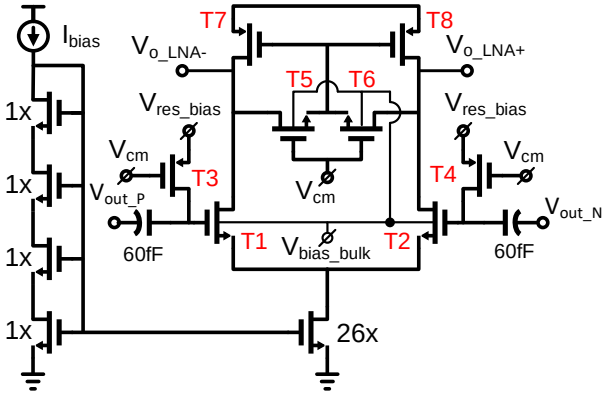
LF and HF paths are correlated off-chip with the Barker-code using a sliding-window correlator.

5.2.1 Baseband Implementation - LF-Path

During regular operation of the receiver, the LF-path demodulates the signal with a baseband LNA and a low-pass filter that filters inter-modulation products at the self-mixer output.

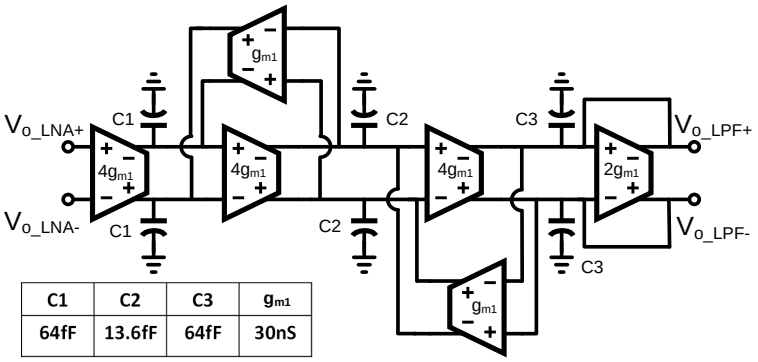
BB-LNA

The baseband LNA (Fig. 5.6a) is implemented as a common-source differential amplifier. Body biasing techniques [41] control the V_{TH} variations of the NMOS transistors T1,T2,T5, and T6, allowing the operation of the LNA at 0.5 V. The LNA consumes 215 nA, and has $\leq$ 2 dB noise figure w.r.t. the output impedance of the self-mixer. Minimum-sized transistors are used to achieve the desired bandwidth at low power, hence the amplifier has a high DC offset. Therefore, it is AC-coupled to the self-mixer using PMOS transistors (T3, T4) in linear region as 250 MΩ resistors, providing a 10 kHz high-pass cutoff. Since the desired signal is spread across 400 kHz bandwidth using the 11-bit Barker-codes, there is no information loss at DC. Transistors T5 and T6 are used as resistors for common-mode feedback.



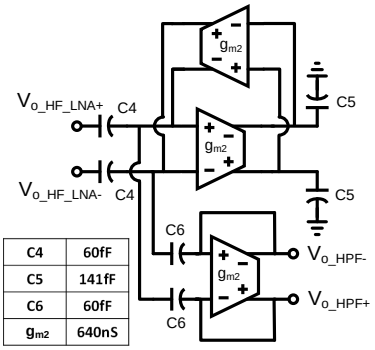
	BB_LNA_LF	BB_AMP_LF, BB_AMP_VGA	BB_LNA_HF, BB_AMP_HF, BB_VGA_HF
T1,2	2.8u/0.12u	1.12u/0.12u	2.8u/0.24u
T7,8	1.12u/1.5u	0.56u/0.12u	2u/0.24u
T3,4	0.28u/1u	0.28u/1u	0.28u/1u
T5,6	0.28u/0.12u	0.28u/0.12u	0.28u/0.12u
Ibias	2nA	0.4nA	5nA

(a)



C1	C2	C3	g_{m1}
64fF	13.6fF	64fF	30nS

(b)



C4	60fF
C5	141fF
C6	60fF
g_{m2}	640nS

(c)

Figure 5.6: (a) Circuit implementation of the baseband amplifiers, with sizing table for the different instantiations; (b) third order g_m-C Chebyshev low-pass baseband filter with 1 MHz cut-off frequency using C1=C3=64 fF, C2=13.6 fF and a unit g_m of 30 nS; (c) third order g_m-C Chebyshev high-pass baseband filter with 1 MHz cut-off frequency using C4=C6=60 fF, C5=141 fF and a unit g_m of 640 nS.

LPF

A third-order, current-biased, g_m-C, 500 kHz, Chebyshev low-pass filter (Fig. 5.6b) for 400 kbps data rate is used in the LF path to reject the mixer output products beyond 1 MHz. MOS-capacitors are used for the small capacitors C1, C2 and C3. The gm-cell circuit topology is similar to the one used for LNA. Since, $g_m = I_d/(n.V_t)$ in weak inversion, a PTAT current source provides a constant g_m. This keeps the LPF cutoff constant across temperature to the first order. The LPF is followed by a variable-gain amplifier with similar topology as the LNA. The variable gain is implemented using 3-bit programmable common-mode feedback resistors implemented with T5 and T6. The receiver chain has 60 dB gain followed by a hysteresis comparator. Overall, the on-chip LF path consumes 222 nW from a 0.5 V supply. The digital demodulation at baseband is performed off-chip. Based on simulations for D-flip-flop power consumption at 500 kHz, we estimate it would consume 25 nW when implemented on-chip.

5.2.2 Circuit Implementation - HF-Path

The HF-path is designed to demodulate the signal using the mixing product $v_{mix,if}$. Assuming the receiver has a front-end bandwidth of 11 MHz, as demonstrated in [23] for a 433 MHz carrier frequency, and the desired signal is in the center, then the HF path requires a bandwidth of 5.5 MHz to demodulate the signal from the mixing product $v_{mix,if}$.

BB-LNA

The BB-LNA in the HF-path also uses the topology shown in Fig. 5.6a and has a 5 MHz bandwidth. Since the self-mixer has a bandwidth of 500 kHz, the signal strength and noise power spectral density observe a 20 dB/dec roll-off beyond 500 kHz. To support lower noise and a 5 MHz bandwidth, the baseband LNA in the HF path consumes 500 nA.

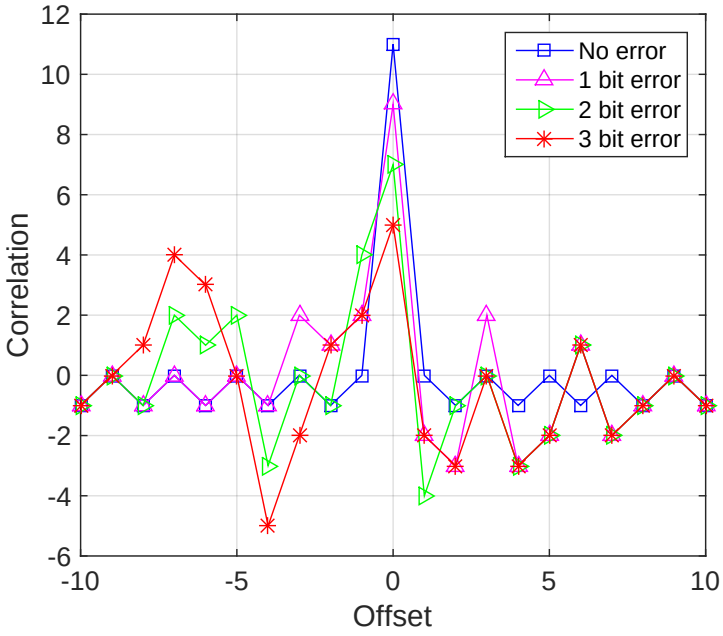


Figure 5.7: Correlation between an ideal Barker code and a received Barker code with 1-bit, 2-bit and 3-bit errors at different code offsets. A 3-bit error leads to a symbol error with a correlation of -5.

HPF

The BB-LNA is followed by a third-order, 1MHz, Chebyshev g_m-C high-pass filter (Fig. 5.6c) to reject any down-converted AM interferer in the baseband. MOS-capacitors are used to implement C4, C5 and C6 with low capacitance values. The signal is then further amplified using baseband amplifiers, each a replica of the BB-LNA consuming 500 nA, with a power consumption dictated by the required 5 MHz baseband bandwidth. A hysteresis comparator is used to slice the signal $v_{mix,if}$. Overall, the HF-path consumes 1.1 μW from 0.5 V.

5.2.3 Digital Demodulation and Correlation with the Barker Code

The Barker codes have correlation very close to a δ function. The auto-correlation is 11 when the codes are aligned and reduces to $\leq |1|$ at any other bit offset. Hence, the Barker code helps to identify the signal in the presence of an interferer as well. Fig. 5.7 shows the correlation between an ideal 11-bit Barker code and a received Barker code with 1-bit, 2-bit and 3-bit errors. Barker

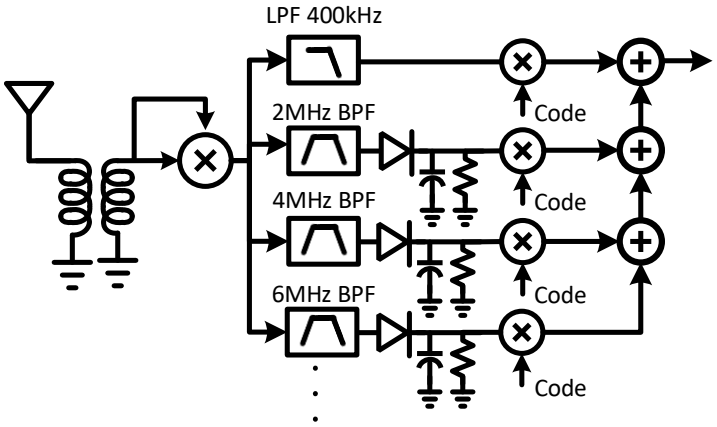


Figure 5.8: System architecture for operation in the presence of multiple interferers.

codes with 2-bit error can be demodulated, however a 3-bit error leads to a symbol error. Thus, the receiver demodulator uses a correlation threshold of 7 to identify the signal.

For the current receiver prototype, the outputs of the LF and the HF path signals have been digitized using an oscilloscope and the HF path IF-frequency output was demodulated to baseband by counting the number of pulses. The correlation with Barker-code was performed in Matlab using a sliding window correlator. We suggested the use of clock and data recovery (CDR) in [42], however 2x oversampling is used in [24] and can be used here as well, obviating the need for a CDR. An architecture for the digital baseband in future implementations is shown in Fig. 5.2. A rectifier is used to demodulate the HF path output from IF-frequency to baseband. The DC level on the AC coupling capacitors C9 and C10 of the self-mixer is used as an indicator of the presence of large interference and a trigger to turn on the HF path. The outputs of the LF and the HF path are then correlated with the 11-bit Barker code using a sliding window correlator. The output of the correlators can then be combined using an OR operation to get the desired demodulated data or the wake-up signal.

5.2.4 Operation in the Presence of Multiple Interferers

So far, the analysis has been performed for a single interferer to explore the opportunity of interferer enhanced sensitivity. The performance in the presence of multiple interferers can be

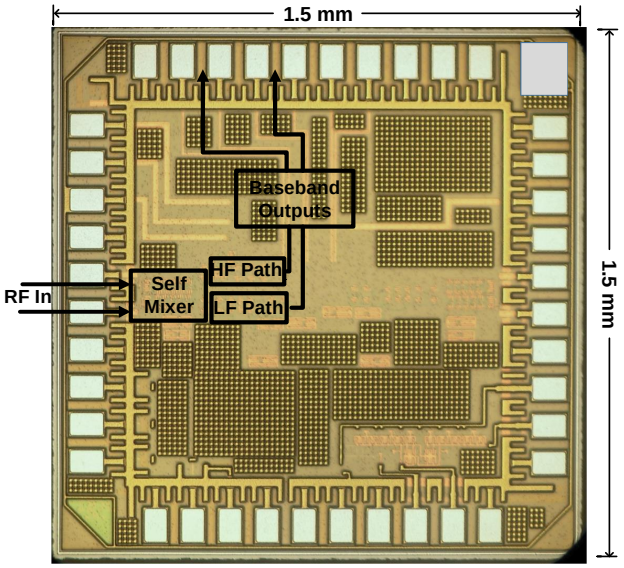


Figure 5.9: Chip micrograph implementing the receiver prototype with an area of 0.2mm^2 in 130nm technology node.

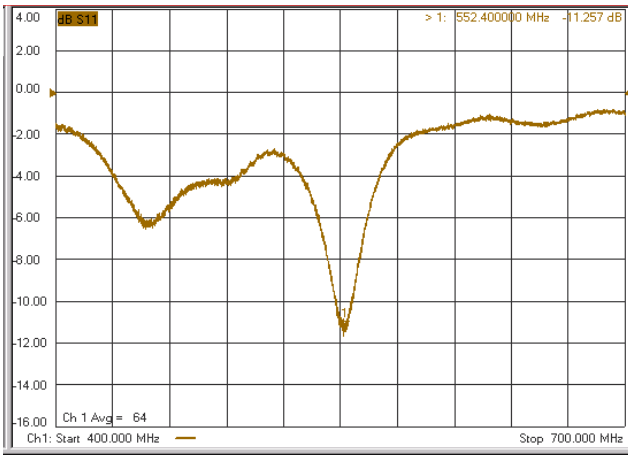


Figure 5.10: Measured S11 of the designed energy-detection receiver, the receiver has a -4 dB RF bandwidth of 36 MHz.

improved by using the architecture shown in Fig. 5.8. It uses multiple IF filters with a 400 kHz bandwidth located at different IF-frequencies, followed by a correlator-bank to look for the availability of the desired signal.

5.3 Experimental results

The chip micrograph of the receiver prototype fabricated in a 130nm CMOS technology is shown in Fig. 5.9. The receiver was packaged in a QFN-40 package and mounted on an FR4 PCB which contains the 0402 components for the passive-gain matching network (see Fig. 5.2). The Q-factor of inductor L2 in Fig. 5.2 is 30, which limits the achievable simulated passive gain to 19 dB[1]. The receiver architecture was targeted to operate in the 433 MHz and 915 MHz ISM bands. Due to the relatively high parasitic capacitors in the 130 nm technology node that was available for prototype fabrication, the prototype receiver operates up to a maximum frequency of 550 MHz and we report experimental results for this highest frequency. The receiver S11 was measured to evaluate the performance of the matching network. The receiver achieves a -4 dB bandwidth of 36 MHz at a 550 MHz (Fig. 5.10). To evaluate the sensitivity and selectivity in regular and interferer-enhanced operation, we used an RF input signal generated by 100% modulating a 550 MHz carrier with a pseudo random data sequence encoded with 11-bit Barker as $m_{sig}(t)$.

5.3.1 Regular Operation through the LF Path

The output of the LF path was sampled with an oscilloscope and correlated with the input $m_{sig}(t)$. The bit-error ratio is plotted in Fig. 5.11. The receiver achieves a sensitivity of -56.4 dBm for a 400 kHz chip rate with 11-bit wake-up code. The measured sensitivity is 3 dB poorer than the calculated sensitivity in Fig. 2.3 assuming the simulated passive gain of 19 dB; this is possibly due to the additional losses in the FR4 PCB substrate.

Next, for a desired signal of -53.4 dBm, the interferer power is increased until the BER degrades to 10^{-3}, the resulting signal-to-interferer power ratio (SIR[2]) is measured for a 250 kHz-PM interferer with a sinusoidal phase deviation of π. The LF path provides an SIR of -12.3 dB, -13.8 dB and -16.5 dB for an interferer located 1 MHz, 3 MHz and 5 MHz away from the signal. The measured SIR for an AM-modulated interferer with 50% modulation depth and varying mod-

[1] Due to the high impedance RF input at the chip, it is very difficult to measure the passive gain so we are relying on the simulated gain.

[2] More negative SIR signifies tolerance to stronger interferer.

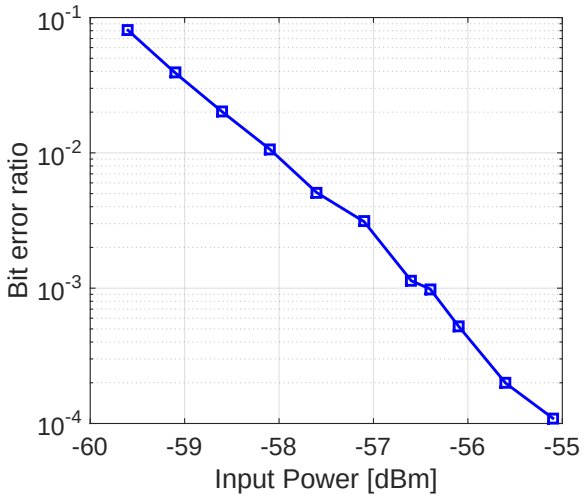


Figure 5.11: Bit error ratio for varying input signal strength in regular operation through the LF path in the absence of interferers.

ulation frequencies and located 2 MHz away from the signal is shown in Fig. 5.12b. The receiver has −2 dB SIR for a 400 kHz AM interferer. Thus, in the presence of an AM-modulated interferer, the LF path gets blocked.

5.3.2 Interferer-Enhanced Operation through the HF Path

The output of the HF path is at an IF-frequency; for the current prototype, the number of pulses were counted to detect a presence of '1'. Fig. 5.12a shows the improvement in sensitivity as a function of the power of the continuous-wave interferer. As discussed in Section 5.1, the sensitivity improves by 1dB per dB increase in the interferer power. A peak sensitivity of −63.6 dBm at a BER of 10^{-3} was achieved at an interferer power of −43.5 dBm while consuming 1.1 μW, beyond which the sensitivity starts to degrade. This is consistent with the maxima for mixing product in Fig. 5.1a.

Further, the SIR was evaluated with an interferer at a 2 MHz offset and different modulation types. For −53.4 dBm signal, Fig. 5.12b shows the SIR in the presence of a PM interferer with a phase deviation of π and an FM interferer with a frequency deviation of 100 kHz. The receiver provides a −23 dB SIR for PM/FM interferers. This limits the operation of sensitivity enhanced mode upto an interferer power of −30 dBm, confirming the simulations as discussed in Sec. 5.1.5.

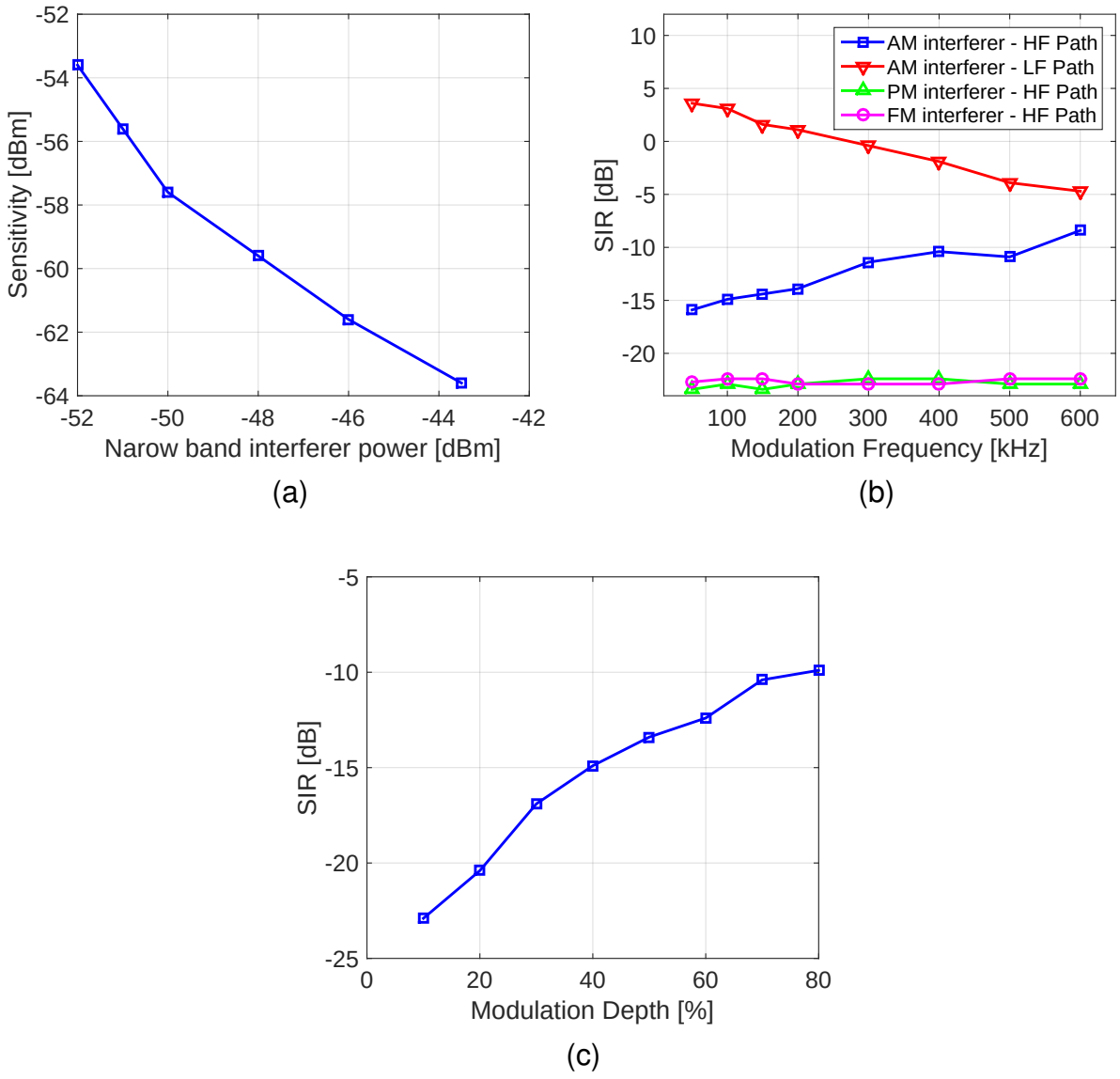


Figure 5.12: (a) Sensitivity improvement in the interferer-enhanced operating mode through the HF path in the presence of a 250 kHz-PM interferer, sensitivity degrades with interferer power >-43 dBm; (b) signal-to-interferer ratio (SIR) for AM, PM, and FM interferers with varying modulation frequency of the interferer; (c) SIR for an AM interferer with a 250 kHz modulation bandwidth and varying modulation depth.

Fig. 5.12b also shows the degradation in SIR for increasing modulation frequency of a 50% AM interferer as analyzed in Sec. 5.1.3. The corresponding degradation w.r.t. the modulation depth at a modulation frequency of 250 kHz is shown in Fig. 5.12c. The receiver provides an SIR of -10 dB, -23.4 dB, and -22.9 dB for an AM interferer, a PM interferer and an FM interferer respectively at

400 kbps chip rate.

5.4 Conclusion

The chapter proposed a receiver architecture to utilize an interferer to an advantage. When the interferer is used as an LO, the sensitivity and selectivity of the wake-up receiver can be enhanced. However, the enhancement is limited in the presence of a wideband interferer. Next chapter, we attempt to improve the performance of the receiver in the presence of such wideband interferers.

Chapter 6: CDMA using Continuous-Time Analog Correlator

Chapter 4 discussed a sub-nW wake-up receiver, but the receiver didn't offer any selectivity to AM interference and the sensitivity was limited by the losses in the front end. To improve the sensitivity and selectivity, interferer was treated as LO in Chapter 5. However, the performance still degrades in the presence of a wideband interferer. Here, we propose an analog correlator to improve the selectivity to a wideband AM interference, as well as enable code-division multiple access for simultaneous wakeup of different sensor nodes.

ED wake-up receivers use OOK modulation and typically use a wake-up code 10 to 32 bits long. Standard receiver designs [23, 34, 25, 28] use a *clocked, digital correlator* after the baseband comparator to detect the wake-up code, requiring synchronization with the incoming signal or 2x oversampling. The block diagram for the wake-up receiver architecture proposed in Chapter 4 is shown in Fig. 6.1a. Briefly revisiting the architecture, it uses a high-Q front-end matching network to provide passive RF voltage gain driving a multi-stage self-mixer. The baseband amplifies and filters the signal and then performs a 1-bit A/D conversion using a comparator, clocked at twice the data rate for asynchronous reception. A clocked, digital correlator checks for the presence of the desired wake-up code. The prototype has 10 MHz of RF bandwidth for a 434 MHz operation and a -14 dB signal-to-interference rejection ratio (SIR) for a continuous-wave interferer. However, for an interferer with in-band AM modulation, the SIR is 5.8 dB and the receiver doesn't provide any selectivity. Therefore, the challenges posed by the architecture include limited sensitivity, no selectivity to AM interference and clock recovery.

These challenges can be addressed by performing correlation in the analog domain before A/D conversion (Fig. 6.1b). The *continuous-time (CT), clockless analog correlator* [43] before the baseband comparator performs matched filtering (MF); this eliminates the synchronization challenges and improves output signal-to-noise ratio (SNR) and thus sensitivity; it also provides

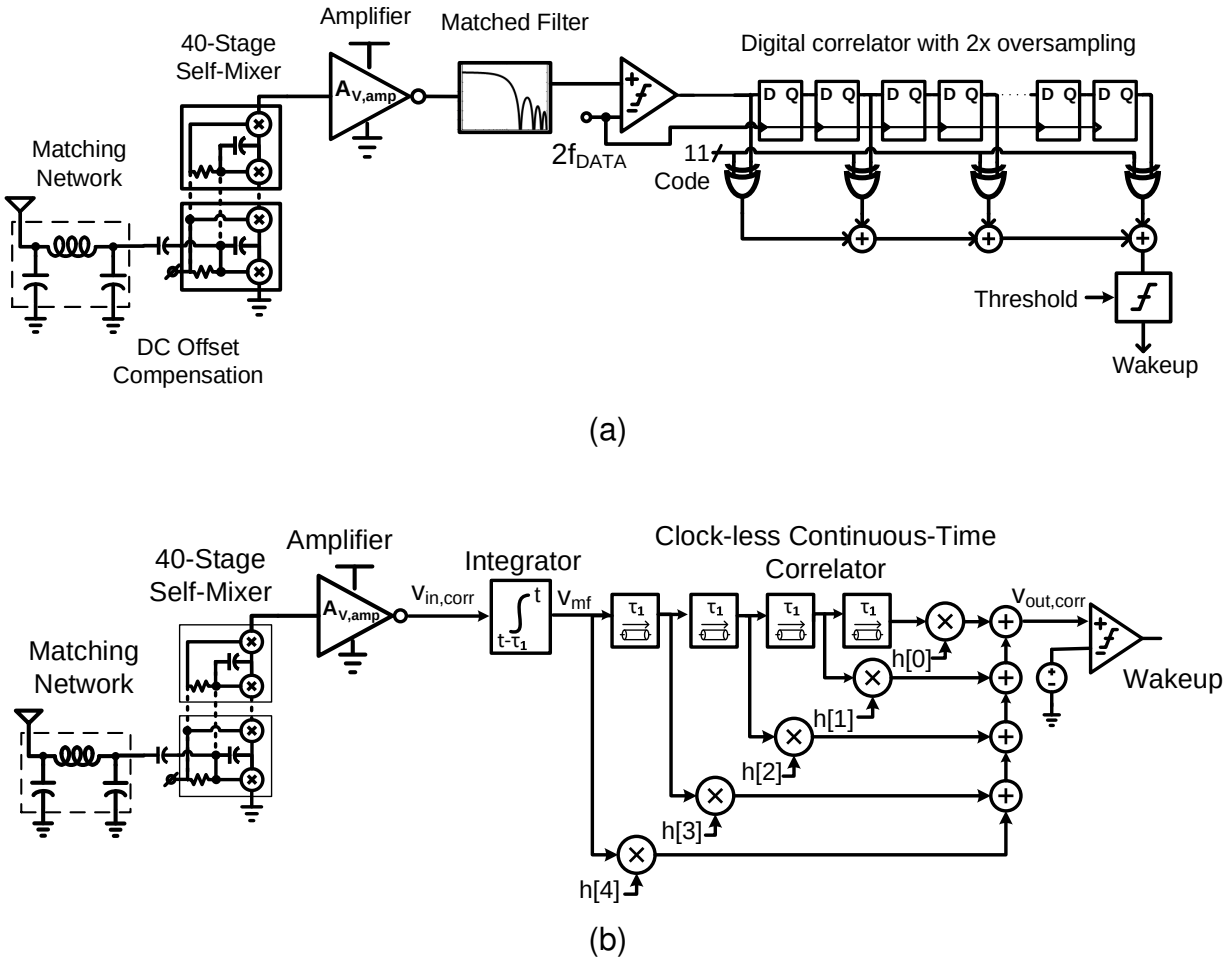


Figure 6.1: A wake-up receiver architecture with (a) a digital correlator proposed in [28], (b) an analog correlator.

code-domain filtering for enhanced selectivity and can suppress AM interference.

This code-domain filtering further enables asynchronous code-division multiple access (CDMA) operation for wake-up receivers. The wake-up codes can be treated as direct sequence code-division multiple-access (DS-CDMA) signals. A matched filter is optimal to receive such DS-CDMA signal [44]; the implementation includes multipliers to multiply with the code sequence and integrators to integrate it for the duration of the signal [45]. Next, we discuss the advantage of using an analog correlator instead of a digital correlator before exploring the architecture to implement the analog correlator.

6.1 Clockless, Analog Correlators vs Clocked, Digital Correlators

A receiver using a digital correlator digitizes the signal before correlation [28]. Instead, an analog correalator 6.1b implements a matched filter for the entire code before thresholding. This provides several advantages/disadvantages as discussed below.

6.1.1 Processing Gain

The output, $v_{out,corr}$, of an ideal N-bit correlator with rectangular bits with a period of τ_1 can be written as:

$$v_{out,corr}(t) = \int_{\tau=-N\tau_1}^{0} v_{in,corr}(t-\tau)\ h[\tau]\ d\tau \tag{6.1}$$

where $v_{in,corr}(t)$ is the input signal, and $h[\tau]$ is a piecewise linear function representing the correlation coefficients. $h[\tau]$ is defined for N time periods corresponding to the correlation sequence. Fig. 6.2 shows the operation of an analog correlator for a 5-bit Barker code. Assuming the signal uses '1', '-1' encoding, during integration of the signal for N-bits, the signal adds in magnitude while the noise adds in power, thus the analog correlator provides a processing gain of $10log(N)$ for the SNR. Instead, if the signal uses '1', '0' encoding, assuming the number of '1's in the code is L, the corresponding processing gain is $10log(L)$.

A digital correlator instead only uses a matched filter for just one bit. A coding gain can

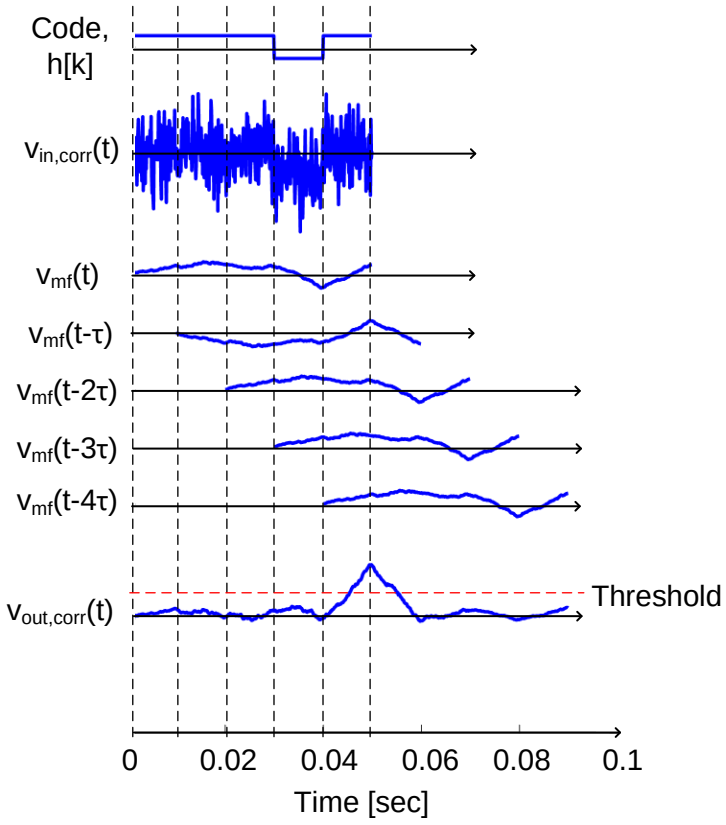


Figure 6.2: Operation of a 5-bit analog correlator in Fig. 6.1b to improve the sensitivity of the receiver.

be achieved by tolerating a few bit errors in the code, leading to a lower required SNR at the comparator input as discussed in Section 6.1.3. The processing gain without the coding gain is 0 dB.

6.1.2 Code-Domain Selectivity

Fig. 6.3 shows the response of a digital correlator and an analog correlator for the desired 5-bit Barker code, an undesired code $h_{int}[k]$ '1,-1,1,-1,1' and the superposition of both the Barker code and $h_{int}[k]$. Here, $h_{int}[k]$ act as an AM interferer, and the digital correlator gets blocked. The analog correlator response to $h_{int}[k]$ gives the residual cross-correlation, which can be treated like analog white Gaussian noise (AWGN). This is acceptable as the first-order approximation due to the wide-band quasi-white spectra of the spreading sequence typically used [46]. If the interferer

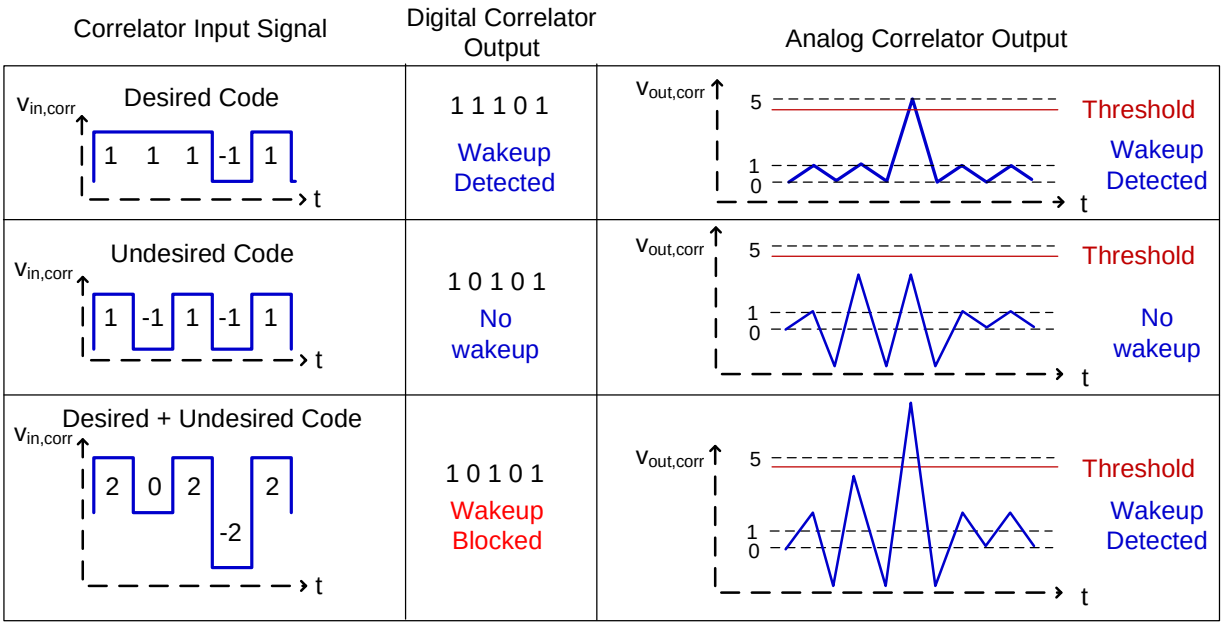


Figure 6.3: Response of a digital correlator and an analog correlator for a desired 5-bit Barker code, an undesired code '1,-1,1,-1,1' and a superposition of both.

$h_{int}[k]$ is orthogonal to the spreading sequence, the interferer will appear an noise at the output of the correlator, with a suppression of $10log(N)$ or $10log(L)$. Fig. 6.3 shows the successful operation of an analog correlator even in the presence of an unwanted code.

6.1.3 Required SNR for MDR $\leq 10^{-3}$

The SNR required to achieve a missed-detection ratio (MDR) of 10^{-3} using a digital correlator is analyzed in [47]. E.g., an 11-bit code '11100100110' at 100 bps with 2x oversampling and 1-bit error tolerance has a required SNR of 12.3 dB at the comparator input for a false-alarm rate $\leq$1/Hr.

For an analog correlator, let's assume a data rate of 100 bps, hence a bit period $\tau_1 = 10$ msec, and a required false-alarm rate $\leq$1/Hr and an MDR $\leq 10^{-3}$. This is equivalent to a receiver with a sampling rate of $f_s = 1/\tau_1$. Equivalently, for $3600 f_s$ samples in an hour, probability of a comparator triggered due to noise is $P(1|0) \leq 1/(3600 f_s)$. Thus, the required comparator threshold is 4.6σ where σ is the root-mean square (RMS) noise at the correlator output. The signal needs to be 3.1σ above the threshold for successful detection with an MDR $\leq 10^{-3}$. The required SNR at the

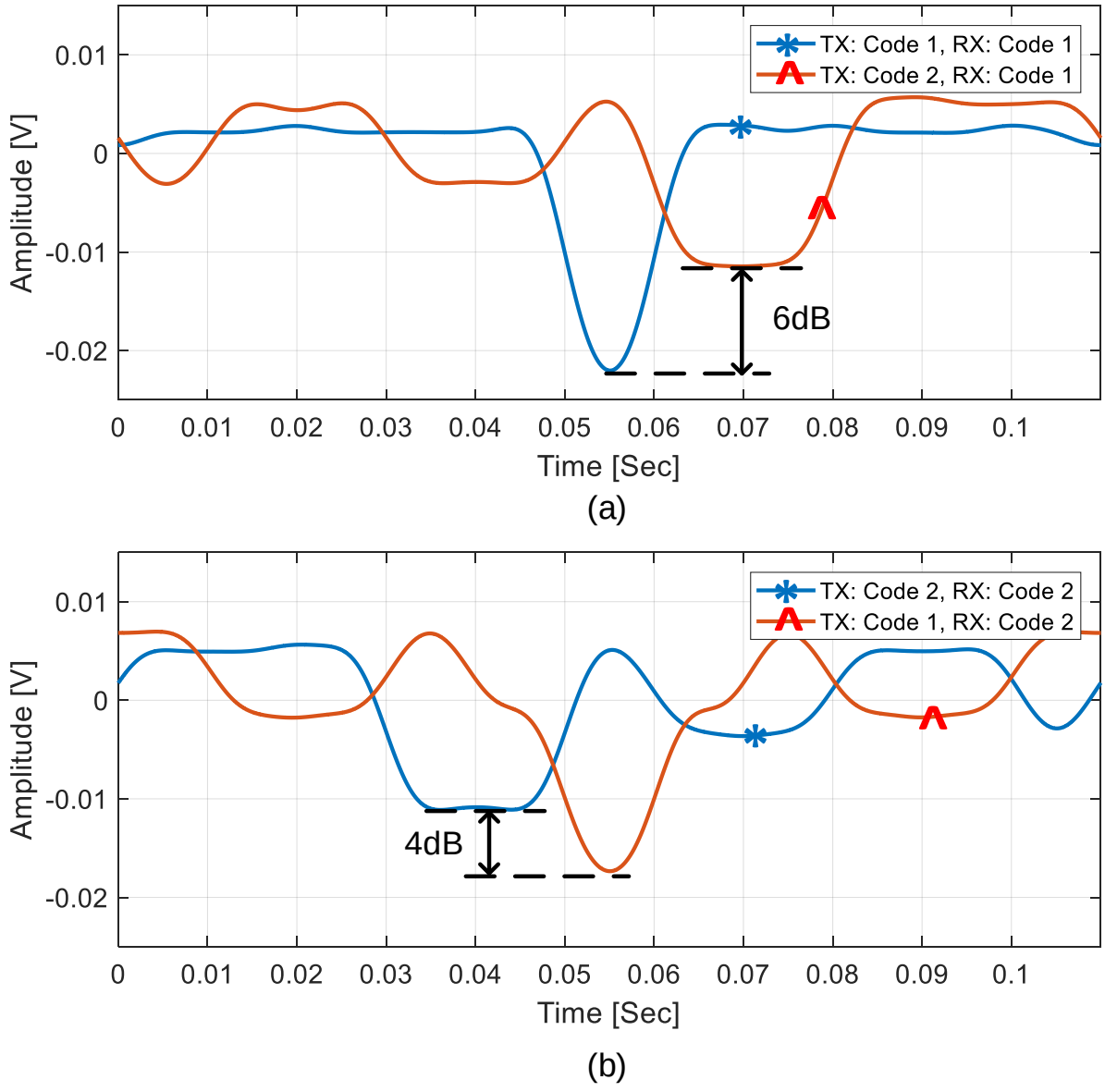


Figure 6.4: Simulated responses of the analog correlator to <code1> and <code2>, when configured to receive (a) <code1> and (b) <code2>. Here <code1> is '11100010010' and <code2> is '11111001101'.

correlator output is then 17.7 dB.

6.1.4 Code-Division Multiple Access

Suppression to unwanted code using the analog correlator is explained in Section 6.1.2. This can be used to provide code-domain selectivity, enabling code-domain multiple access. Fig. 6.4 shows the response of an analog correlator to two different codes <code1>: '1110010010' and <code2>: '11111001101' with '1', '-1' encoding when the correlator is configured to receive (a) <code1> and; (b) <code2>. The correlator has a 6 dB suppression for <code2> when receiving <code1> and a 4 dB suppression to <code1> when receiving code2. Ideally, the suppression should be $10log(N)$ where $N = 11$, but, the codes are not entirely orthogonal to each other. Due to the nonorthogonality of the practical spreading sequences, DS-CDMA receivers suffers from the near-far problem as well [46]. However, this is not an issue when the same transmitter is transmitting to several wake-up nodes.

Low cross-correlation sequences for asynchronous CDMA reception are explored in [48]. Gold sequences are proposed for the same in [49]. There are $2^l - 1$ Gold-codes in a family depending on the seeds where l is the length of the shift register to generate an m-sequence leading to Gold codes. The length of the Gold sequences is $g = 2^l - 1$. For well chosen sequences, the cross-correlation in Gold-codes is $2^{(l+1)/2} + 1$ and the self-correlation is $2^l - 1$. This requires 31-bit long sequences ($l = 5$) to have a 10 dB suppression to unwanted code. The output SNR degradation with increasing number of users is shown in [46] for a 31-bit long gold sequence. The SNR drops to 13 dB for receiving two users simultaneously with equal transmit power. Thus, for CDMA reception, the system performance is multiple-access interference (MAI) limited, and channel utilization is correspondingly low. With the need to support numerous users in future, an optimal multi-user receiver requires a bank of matched-filters followed by a Viterbi algorithm for maximum likelihood sequence estimation. For wake-up receivers, we want the receiver complexity to be minimal. Alternative is to reduce the total mean square error (MSE) at the receiver output, alleviating the problem of noise enhancement. Adaptive techniques to minimize the mean square error (MMSE)

has been described in [46]. This work demonstrates the performance of an 11-bit matched filter implementation for DS-CDMA reception. The receiver can be adapted for complex algorithms based on the system requirements in future.

6.2 CT Analog Correlator Circuit Implementation

The ideal correlator response to an N-bit sequence given by (6.1) can be rewritten as:

$$v_{out,corr}(t) = \sum_{k=1}^{N} \int_{\tau=-k\tau_1}^{(1-k)\tau_1} v_{in,corr}(t-\tau)h[\tau]d\tau \tag{6.2}$$

$$= \int_{\tau=-\tau_1}^{0} \left(\sum_{k=1}^{N} v_{in,corr}(t-k\tau)h[k\tau] \right) d\tau \tag{6.3}$$

This requires integration, delays and adders. Implementation using discrete-time signal processing involves an ADC, a digital-signal-processing (DSP) unit and a clock generator. This requires synchronization with the input signal. E.g., a bank of 260 256-bit long recycling integrated correlators were implemented for receiving a 256-bit code in [50] due to lack of synchronization with the input signal.

For true *clockless* analog correlators, continuous-time analog delays are needed (Fig. 6.1b); at very high frequencies analog delays can be implemented with transmission-line sections, but these are infeasible at baseband frequencies. For an analog signal encoded in time domain, e.g., with pulse-position modulation (PPM) or pulse-width modulation (PWM), digital-style delays can be utilized to realize the CT delays. Clock-less CT signal processing using a CT ADC and DAC and digital-style delays has been used to implement analog FIR filters in [51]. Pulse-frequency modulation (PFM) with digital delays are used in [52, 53], but, the DSP used doesn't provide the matched-filter operation. Here, we use PFM encoding using voltage-controlled oscillator (VCO), and design the DSP to provide matched-filtering and the FIR response required for the analog correlator. Next, we describe the operation of a 1-bit matched filter.

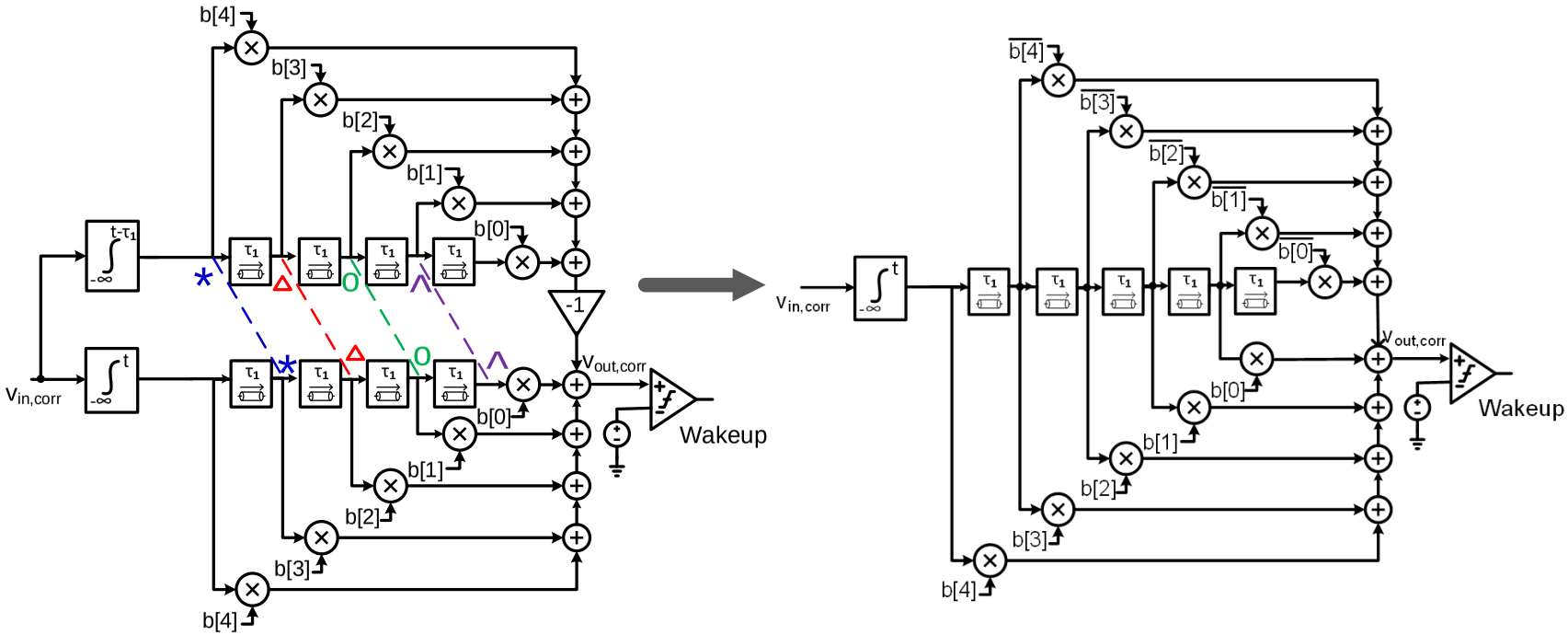


Figure 6.5: Equivalent block diagram of a 5-bit analog correlator as in Fig. 6.1b, $\int_{-\infty}^{-\tau_1}$ can be tapped from $\int_{-\infty}^{0}$ with a delay τ_1.

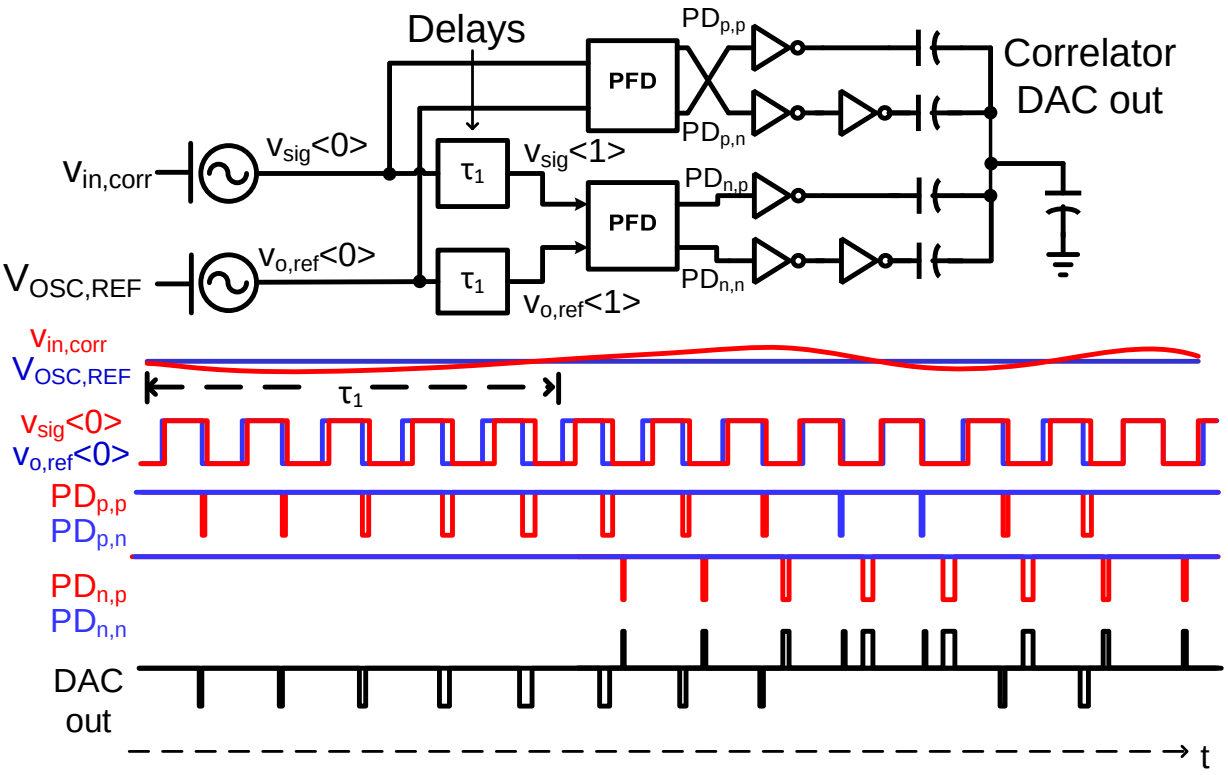


Figure 6.6: Implementation and operation of a matched filter for 1-bit rectangular pulse.

6.2.1 Matched Filter for a Single Rectangular Bit

The ideal analog correlator response in (6.3) can also be written as:

$$v_{out,corr,1}(t) = \int_{-\infty}^{0} \sum_{k=1}^{N} v_{in,corr}(t - k\tau)h[k\tau]d\tau - \int_{-\infty}^{-\tau_1} \sum_{k=1}^{N} v_{in,corr}(t - k\tau)h[k\tau]d\tau \tag{6.4}$$

The equivalent block diagram is in Fig. 6.5. Since, $\int_{-\infty}^{-\tau_1}$ can be tapped from $\int_{-\infty}^{0}$ with a delay τ_1, it results in a compact block diagram, operating as a matched filter while also providing the FIR response for the desired code. Here, the integrator can be implemented using VCO, the output digital signal can be delayed using latch-based delays, the digital signals can be correlated to code and summed using a capacitor DAC.

Fig. 6.6 shows the implementation of a 1-bit matched filter (N=1). The front end of the correlator consists of VCOs with center frequency f_0, the sig-VCO converts the input signal into pulse frequency modulated (PFM) output and a ref-VCO serves as a reference signal with frequency f_0. The pulse output position at v_{sig} <0> relative to the pulse positions at $v_{o,ref}$ <0> gives the integral output $\int_{-\infty}^{t} K_{vco}(V_{in,corr}(\tau) - V_{OSC,REF})d\tau$ where K_{vco} is the voltage-to-frequency conversion gain of the VCO. The relative pulse positions are compared with a phase-frequency detector (PFD) and fed to an adder implemented using capacitor-DAC to convert the signal back to voltage domain.

The output pulses of the VCOs are also delayed using latch-based delay cells with delay τ_1 and the relative position is again evaluated using a PFD. The output is subtracted using the capacitor-DAC. This provides a CT windowed integrator response for a window of time τ_1 set using the delay cell.

6.2.2 Matched Filter for an 11-Bit Code

The architecture for an 11-bit matched-filter is shown in Fig. 6.7. N delay elements in Fig. 6.6 are cascaded to keep track of $v_{in,corr}$ for the past $N\tau_1$ duration. CT delay implementation is discussed in detail in Section 6.3.5. At the input and the output of each τ_1 delay, a PFD is used to evaluate the relative position of pulses. The outputs of the twenty-two PFDs are sent to a capacitor-DAC to implement eleven matched filters for 11-bit code. A weighted sum is performed using the capacitor-DAC with weights as the correlator coefficients h[τ], implemented by swapping the input signals to the PFDs.

Assuming a sinusoidal input signal with frequency f_{in}, and a peak amplitude A, the spectral description of a PFM encoded signal is evaluated in [53]. The spectrum has strong signals at $kf_0 \pm mf_{in}$ with signal strength relative to the desired signal given by:

$$\frac{S(kf_0 \pm mf_{in})}{S(f_{in})} = \frac{2f_0}{\Delta f_p} J_m\left(\frac{k\Delta f_p}{f_{in}}\right)\left(1 \pm \frac{mf_{in}}{kf_0}\right) \tag{6.5}$$

where $J_m(\frac{k\Delta f_p}{f_{in}})$ is the Bessel function of the first kind of order m and $\Delta f_p = AK_{vco}$ is the peak

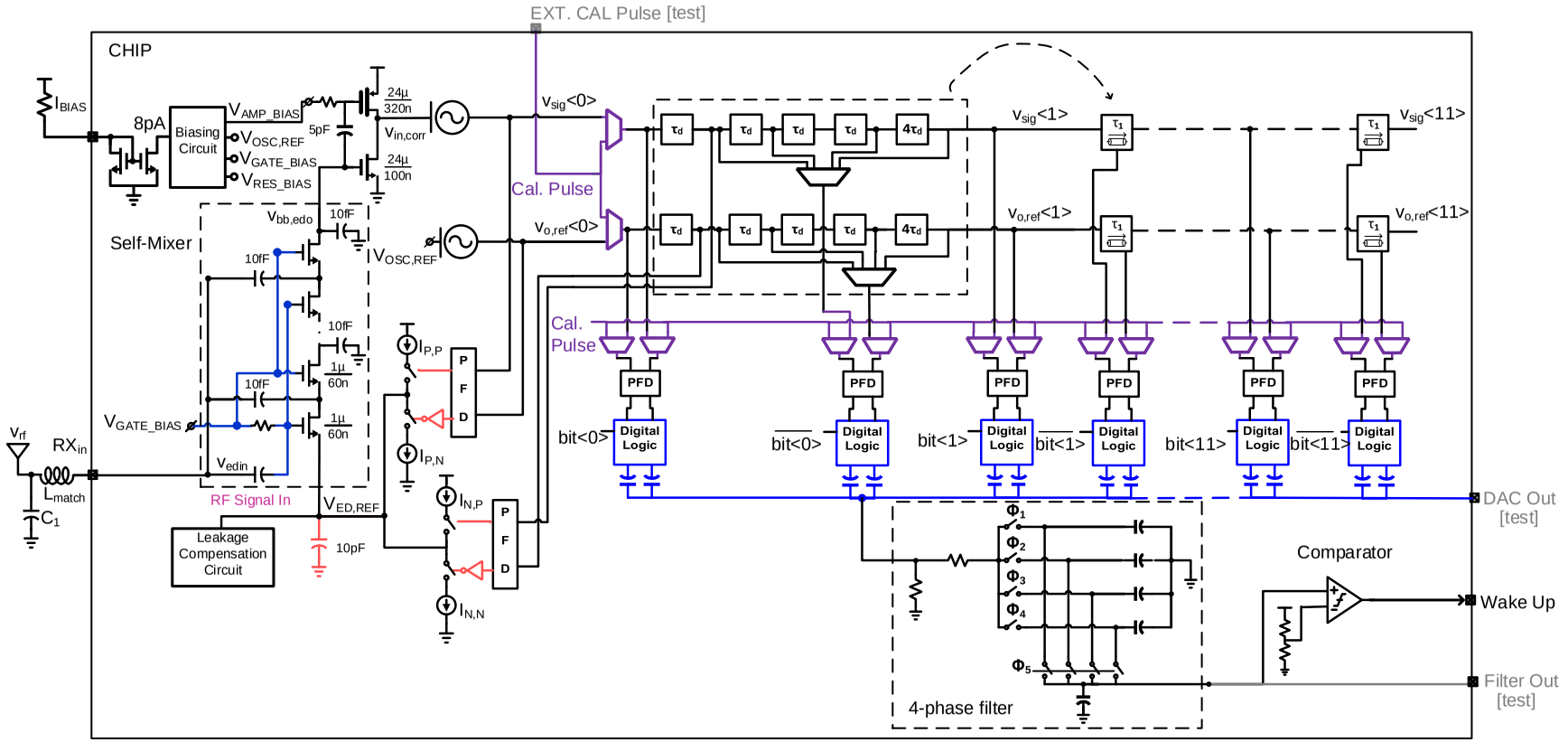


Figure 6.7: Energy-detector wake-up receiver with a clockless analog correlator for matched filtering; the DC feedback loop through the gate-biased self-mixer and part of the baseband provides automatic biasing.

frequency deviation at the output of the VCO. The correlator DAC output is a weighted sum of PFD pulses containing these spurious signals and need to be rejected. A 4-phase filter uses the 4-phases of the ref-VCO controlled by $V_{OSC,REF}$ to sample the DAC output and averages the output over one VCO period to suppress the outputs at f_0 and its harmonics. The output of 4-phase filter is then $v_{out,corr}(t)$.

6.3 System Implementation

Fig. 6.7 shows the wake-up receiver implementation using an 11-bit analog correlator. The RF front end consists of a matching network followed by a gate-biased self-mixer [47]. Its output is amplified using a one-stage current-reuse amplifier that drives the analog correlator. The output of the correlator is fed to a comparator that decides if the receiver should wake up.

The sig-VCO and ref-VCO need to be frequency locked; their outputs are compared with a PFD and fed back to the self-mixer reference $V_{ED,REF}$ with a charge-pump (CP) for DC feedback. We use a second PFD-CP driven by delayed VCO outputs to create a zero for stabilizing this second-order feedback loop.

6.3.1 RF Front End

The receiver front end has an off-chip matching network with the 132-10SM inductor L_{ind}=111nH available from Coilcraft and capacitor C_1=14 pF providing a passive voltage gain A_v of 26 dB at 450.8 MHz RF frequency. The matching network is followed by a self-mixer proposed in [47], it serves as an optimal energy detector by maximizing the conversion gain while minimizing the noise contribution. A 40-stage self-mixer is used with an input resistance $R_{in,ed} = 200\,\text{k}\Omega$. The source of the self-mixer V_{EDREF} is connected to a charge-pump for DC feedback discussed in Section 6.3.4.

6.3.2 Baseband Voltage Amplifier

The output of the self-mixer $v_{ed,bbo}$ is amplified using a current-reuse baseband amplifier by gain ($-A_{v,amp}$) of 26 dB with a 1 dB baseband noise figure relative to the noise contributed by the self-mixer. The PMOS transistor is current biased using a current mirror with AC coupling while the NMOS transistor is biased through the DC feedback loop (Section 6.3.4). The output $v_{in,corr}(t)$ is sent to the correlator. Additionally, the feedback loop also provides a high-pass response in the signal path and rejects the low-frequency flicker noise added by the amplifier.

6.3.3 Voltage Controlled Oscillators

The output of the voltage amplifier is fed to a signal VCO for PFM encoding. A reference VCO with frequency f_0 is used with control voltage $V_{OSC,REF}$ to serve as a pulse-position reference for the signal VCO. Average frequency of the signal VCO is locked f_0 using a PLL (Section 6.3.4). This sets the DC potential at $V_{in,corr}$ equal to $V_{OSC,REF}$. 4-phase current-starved ring oscillators are used operating at 1.1 kHz with $K_{vco} = 25\,\text{kHz}/V$. The available four-phases will be used to implement a filter (Section 6.3.7) to suppress the correlator DAC output at f_0 and its harmonics.

6.3.4 Phase-Locked Loop

On an average, the signal VCO need to be locked to the reference VCO for glitch-free operation of the correlator. This is ensured using a phase locked loop. The outputs of the VCOs are compared to a PFD and fed to a charge pump (I_{cp}) driving a 10 pF capacitor. The loop has two poles at angular frequency $\omega = 0$, and needs to be compensated for stability. The VCO outputs are delayed using τ_d digital delay (Section 6.3.5), fed to another PFD with the inputs swapped. The Up/Down pulses drive another charge pump (cI_{cp}), where c is a scaling constant $0 \leq c \leq 1$. This introduces a zero, and stabilizes the loop. The equivalent s-domain model is shown in Fig. 6.8. The CP and loop-filter feedback gain is:

$$I_{cp}\left[\frac{1 - ce^{-j\omega\tau_d}}{j\omega C_{lf}}\right] \tag{6.6}$$

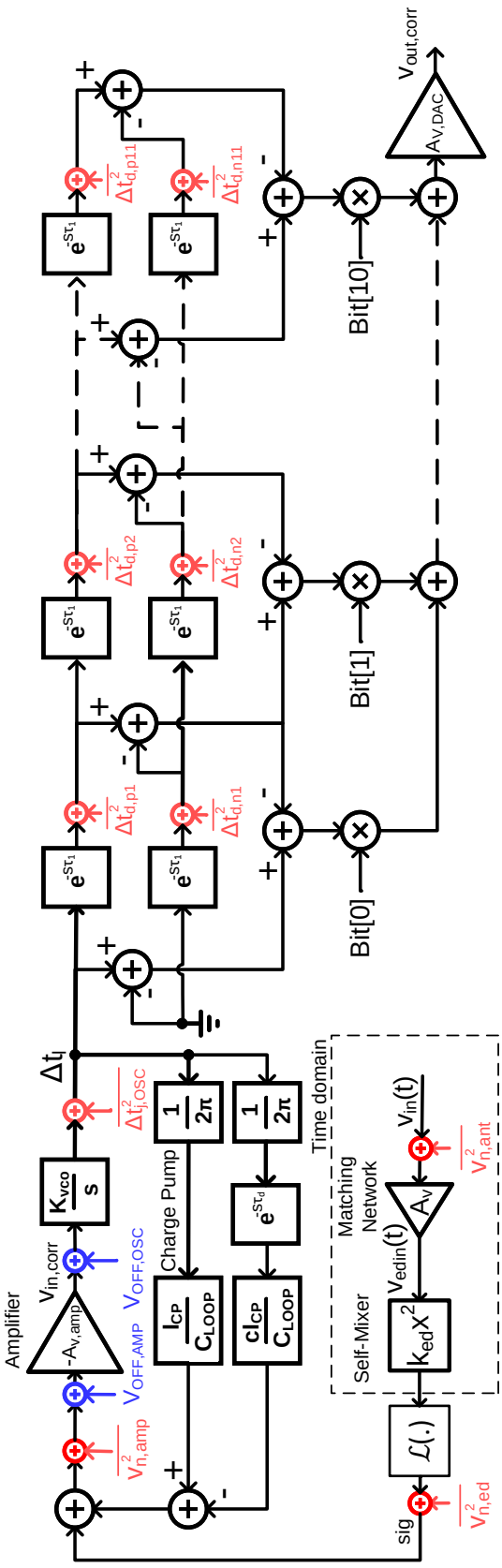


Figure 6.8: Mixed-domain model with modeled noise and DC offsets for the receiver architecture in Fig. 6.7.

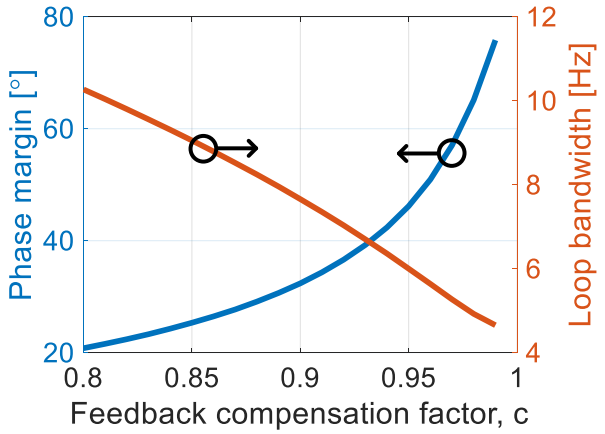


Figure 6.9: Phase margin and loop bandwidth achieved using delay based compensation for a varying c.

Equivalently the integral and proportional terms can be written as:

$$H_{cp,lf}(j\omega) = \frac{1-c}{j\omega C_{lf}} + \frac{c|sin(\omega\tau_d)|}{\omega C_{lf}} \angle \left(\frac{-\omega\tau_d}{2}\right) \tag{6.7}$$

Now, the loop gain can be written as:

$$H_{loop}(j\omega) = -A_{v,amp} \frac{K_{vco}}{j\omega} \frac{I_{cp}}{2\pi} H_{cp,lf}(j\omega) \tag{6.8}$$

The achievable phase margin and loop bandwidth for $I_{cp} = 2\,\text{pA}$, τ_d=1.5 msec for varying compensation factor c is in Fig. 6.9. The receiver has a 30° phase margin and 8 Hz loop bandwidth for $c = 0.9$.

6.3.5 Delay Cell Design

The outputs of the VCOs are fed to the delay lines to implement the analog correlator described in Section 6.2. The delay line consists of eleven delay elements of τ_1 delay each. Each τ_1 implementation (Fig. 6.7) consists of 8 τ_d delay cells cascaded in series. Further, each delay element τ_d consists of 3 granular τ_g delay cells as shown in Fig. 6.10. An input falling edge sets the SR latch

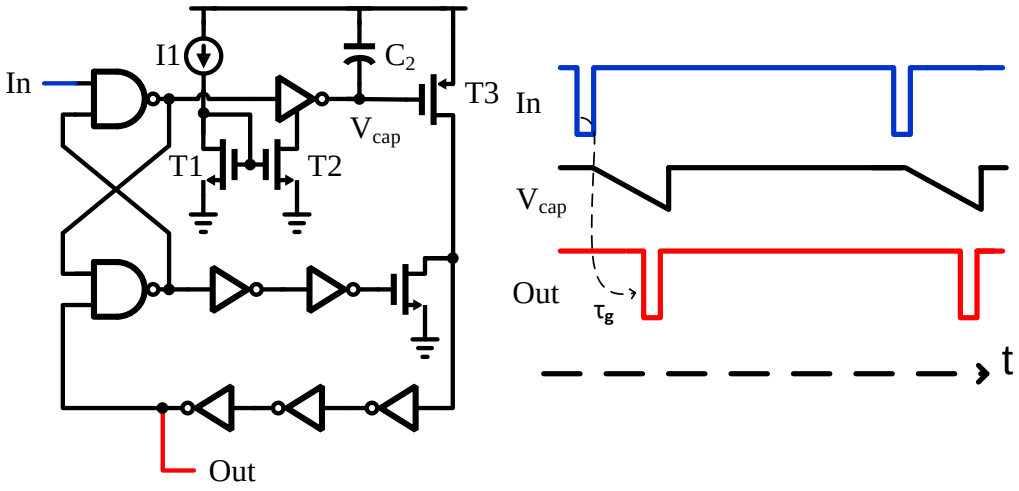


Figure 6.10: Unit delay cell implementation providing a delay of τ_g

to discharge C_2, until it reaches threshold to turn transistor T3 on. Once T3 is triggered, it delivers a falling edge pulse at the output and resets the latch. The delay τ_g is controlled by current mirror T1 and T2, MIM-cap C_2 and transistor T3 threshold.

Variations in transistors are controlled using current mirror trimming. The delay cell takes an input digital pulse and produces a similar output pulse after a delay τ_g. The delay is controlled by the current mirror using transistors T1 and T2 and capacitor C_2. MIM-caps are used for C_2 to minimize process variations, however nA current mirrors are less reliable. All delay elements for each τ_1 delay implementation are mirrored from the core current mirror with 6-bit trimming to provide a 30% tuning range to account for current mirror and delay cell mismatches. The core current mirror also has a 50% tuning range to set the average delay of all the delay elements. The delay cell calibration to set the delays is described in Section 6.3.6.

The minimum pulse width (τ_{pulse}) required for the input pulse is decided by the setup time of the latch. The maximum pulse width should be less than the delay of the unit cell. Therefore, the input-pulse instantaneous frequency must be less than $(1/(\tau_g + \tau_{pulse}))$. For $\tau_1 = 10$ msec, $\tau_g = 416\,\mu$sec. This leads to a maximum input-pulse frequency of 2.3 kHz. Due to the variations in the current mirrors controlling the delay cells and the added jitter, f_0 is set to 1.1 kHz.

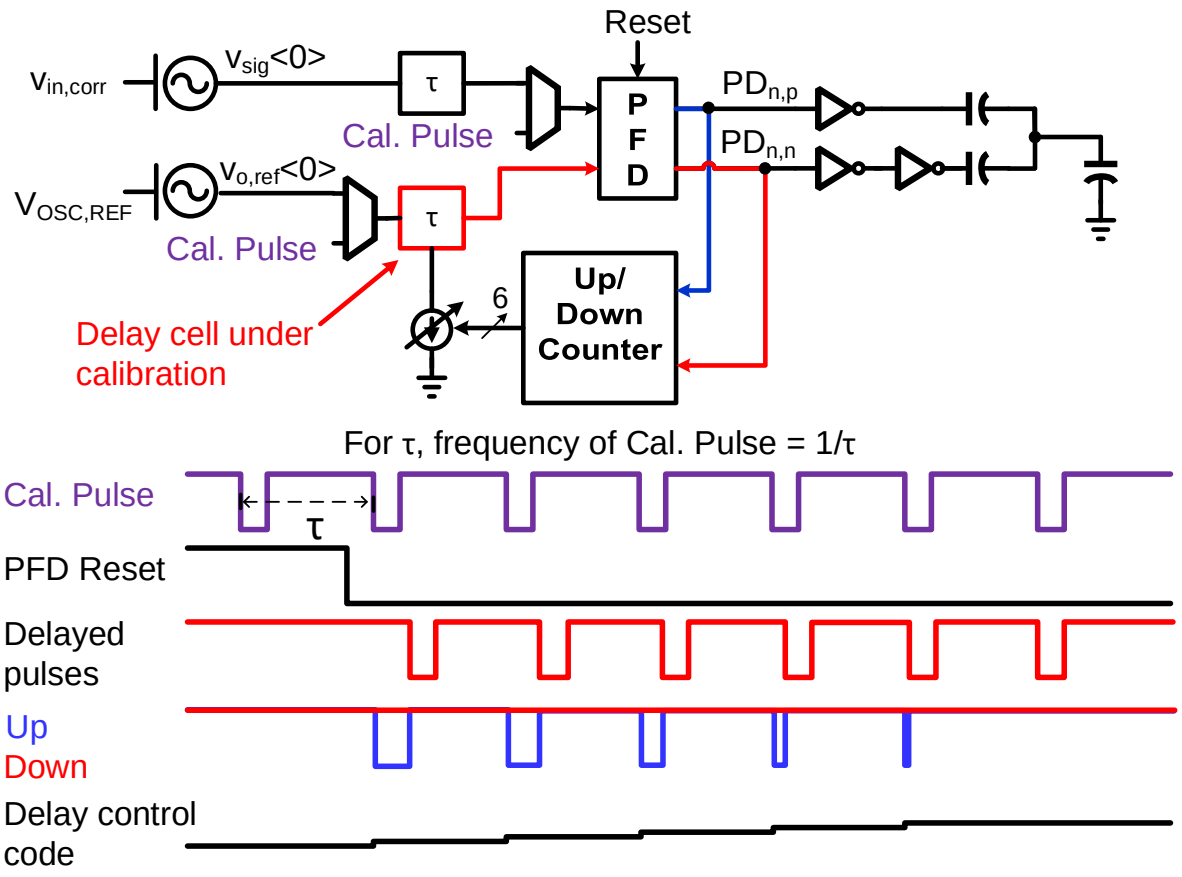


Figure 6.11: Calibration mechanism for delay cells.

6.3.6 Delay-Cell Calibration

Each delay element τ_l has a 6-bit trimming register to account for mismatches. The calibration process to set the delays is shown in Fig. 6.11. The VCOs in the receiver architecture are bypassed to feed falling edge pulses (Cal_Pulse) at the input of the delay line with a pulse frequency of $1/(\tau_l)$. E.g. to calibrate a τ_l delay cell in the reference delay line, the VCO output is bypassed and a Cal_Pulse is fed at the input of the delay cell. The corresponding delay element in the signal path is bypassed, instead, Cal_Pulse is fed. Thus, the PFD at the output of the delay cells compare τ_l to the period of the Cal_Pulse. The Up/Down pulses provides the feedback to increase/decrease the delay control code to set the delay.

6.3.7 Four-Phase Filter

The output of the correlator DAC has the strong signal components at f_0 and its harmonics, this needs to be filtered out. In [54], multiple VCO phases and averaging using delays are used. Here, multiple VCO phases will require additional delay lines, which is area inefficient. For a delay based averaging, frequency f_0 can change, which can lead to a poor rejection. Instead we use four-phases ϕ_{1-4} of the f_0 with 20% duty-cycle to sample the signal at the output of the correlator DAC, a series resistor is used to provide a low-pass frequency response, a non-overlapping phase ϕ_5 with 5% duty-cycle is used to average the four samples. This filtered output $v_{out,corr}(t)$ is sent to a comparator for detecting wake-up.

A dynamic latched comparator clocked at frequency f_0 from the ref-VCO is used to compare the correlator output to detect the wake-up signal. The correlator is set at a threshold of $-20\,\text{mV}$ for a false-alarm rate $\leq$ 1/Hr.

6.4 Design Considerations in the Receiver and Correlator

We discussed the code requirements for an ideal asynchronous CDMA wake-up receiver in Section 6.1.4. The non-ideal components such as noise, non-linearity, variations over process, voltage and temperature can impact the performance. Below, we discuss the effect of these on the performance of the proposed receiver.

6.4.1 Noise

The noise sources in the receiver are shown in Fig. 6.8. The noise from the antenna $\overline{v^2_{n,ant}}$ doesn't dominate the passive-RF energy-detector receivers [34]. The added noise from the self-mixer $\overline{v^2_{n,ed}}$, the amplifier $\overline{v^2_{n,amp}}$ and the VCO $\overline{\Delta t^2_{j,OSC}}$ gets low-pass filtered in the correlator. The total noise contributed by these sources at $v_{out,DAC}$ is 4mVrms. The noise of each delay in the correlator is modeled as $\overline{\Delta t^2_{d,<p|n><1-1|>}}$ and appears at the output of the correlator DAC. The noise considerations in the delay-cell design are detailed in [53]. The noise contribution from the delay

cells has to be kept low compared to the front-end noise, which accounts for most of the power consumption in the correlator. The measured RMS jitter for 1.25 msec, 10 msec and 110 msec delay using the delay cells is 0.43%, 0.26% and 0.17% respectively. This suggests the presence of a correlated noise in the delay cells due to the common current source used. The RMS jitter added due to the delay cells is then $\sqrt{\Sigma_{k=1}^{11}\overline{\Delta t^2_{d,<p|n><k>}}} = 190\,\mu$Sec. The measured noise at $v_{out,DAC}$ due to the delay cells is 3.2 mVrms. The total measured RMS noise at $v_{out,DAC}$ is 5.2 mVrms.

6.4.2 VCO Frequency

We calculated the maximum frequency of operation for a VCO in Section 6.3.5 based on the delay cell granularity as 2.3 kHz. This suggests a tolerable peak pulse position deviation of 217 μSec, but the pulse position jitter added by the delay cells is itself 190 μSec. To reduce the possibility of cycle slipping, say once every hour, the probability of a glitch should be $\leq 1/(3600 f_0)$. Assuming a Gaussian jitter profile, the operating frequency has to be less than 500 Hz. Thus, noise in the delay cells must be reduced in future prototype for a glitch free operation.

Additionally, the correlator DAC output has spurious signals with relative strength to the wanted signal given by (6.5). The spurs are a strong function of the input amplitude as well as the ratio f_{in}/f_0. These spurs can cause in-band distortion when f_0 gets closer to f_{in} [53]. For a correlator input signal of 3 mV and $f_{in}/f_0 = 0.14$, the signal-to-distortion ratio (SDR) is 30 dB. For an 11-bit correlation code, 30 dB SDR is sufficient, but when using a longer code, the input signal amplitude or bandwidth needs to be reduced further for proper operation.

6.4.3 Delay Drift

The correlator processing gain can change when τ_1 changes due to process, temperature and supply voltage variations. The simulated processing gain for <code1> is 5 dB for '1' '0' encoding and 11 dB for '1' '-1' encoding. The variation of the processing gain with delay drift for '1' '-1' encoding and '1' '0' encoding is shown in Fig. 6.12a. The correlator has a 1 dB degradation in the processing gain for a 5% drift in the delay τ_1. To tolerate higher drift in delays, either

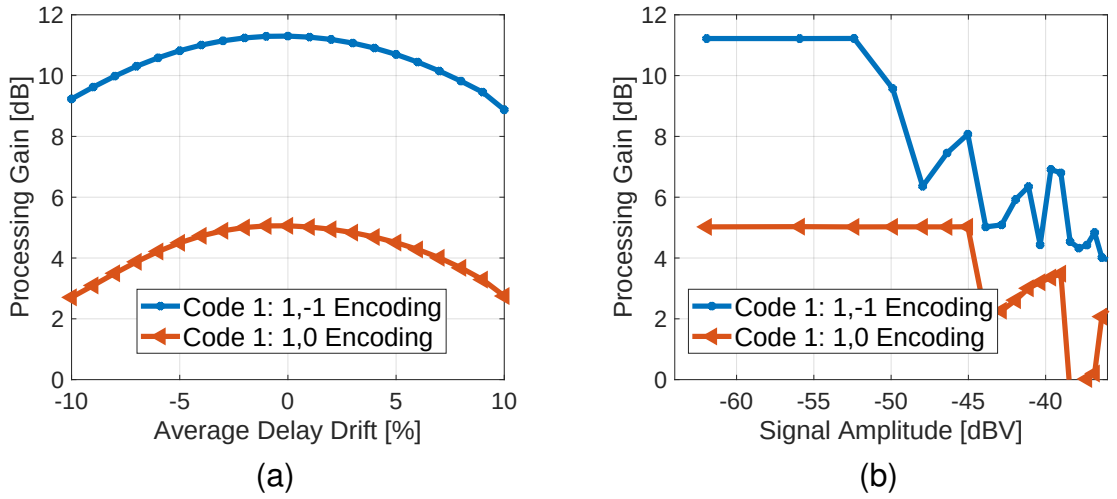


Figure 6.12: The correlator processing gain degradation w.r.t. (a) variation in delay τ_1, (b) increasing input signal strength.

a temperature compensated oscillator on-chip or a crystal reference can be used. During large temperature changes, these can be switched on as a reference for re-calibration of the delay cells.

6.4.4 Dynamic Range

The outputs of the PFDs saturate with increasing input signal due to the limited maximum pulse position difference which is limited to the VCO period $1/f_0$. Processing gain degradation with increasing input signal strength for '1' '-1' encoding and '1' '0' encoding is shown in Fig. 6.12b. The simulated processing gain degrades for signal higher than -52 dBV for '1' '-1' encoding and -45 dBV for '1' '0' encoding. For a 10 dB SNR at the correlator output, the correlator requires a '1' '0' encoded 1mV peak input (measurements discussed below), thus the dynamic range of the correlator is 15 dB.

If needed, UP/Down counters at the output of the PFDs controlled by the states in the PFD can be used in future designs to enable multi-level digital output [51], to further enhance the dynamic range.

6.4.5 Non-Linearity

Sources of non-linearity in the delay cell and VCO encoder are discussed in [53]. Non-linearity in the correlator can impact the rejection to unwanted codes and can be critical when longer codes are used, it doesn't impact the performance for the 11-bit correlator implementation presented here.

6.5 Measurement Results

The matching network is designed to operate at 450.8MHz, it has a 3-dB RF bandwidth of 10 MHz. The corresponding S11 is in Fig. 6.15a. Next we measure the performance of the wake-up receiver for a Barker wake-up code '11100010010'.

6.5.1 Correlator Characteristics

The delay cells are calibrated with delay $\tau_1 = 10$ msec to receiver a 100 bps '11100010010' Barker code. Next, a 450.8 MHz RF signal modulated with a sinusoidal AM signal with a frequency f_{in} is fed to the input of the receiver. Frequency f_{in} is swept from 10 Hz to 400 Hz; $v_{in,corr}$ and $v_{out,corr}$ are measured to evaluate the frequency response. Fig. 6.13 shows the ideal and measured frequency response. The correlator has a Sinc filter response due to windowed integration in addition to the spectral characteristics of the code. As expected, the measured response starts to deviate from its ideal behavior at higher frequencies when f_{in} gets closer to f_0.

6.5.2 Wake-Up Receiver Sensitivity and Selectivity

Next, the comparator threshold is set to -20 mV (5.8σ) and an RF signal modulated with the 50% RZ-OOK encoded 11-bit Barker code with '1', '0' symbols is applied to measure the sensitivity. The receiver response to -79.3 dBm wake-up code sent every 200 mSec is shown in Fig. 6.14a. The missed-detection ratio (MDR) is measured to be 10^{-3} for -80.9 dBm input signal.

Next, signal-to-interference ratios (SIRs) are measured for a 100 bps OOK modulated '1010' pattern AM interferer and a continuous-wave interferer by measuring the noise equivalent power at

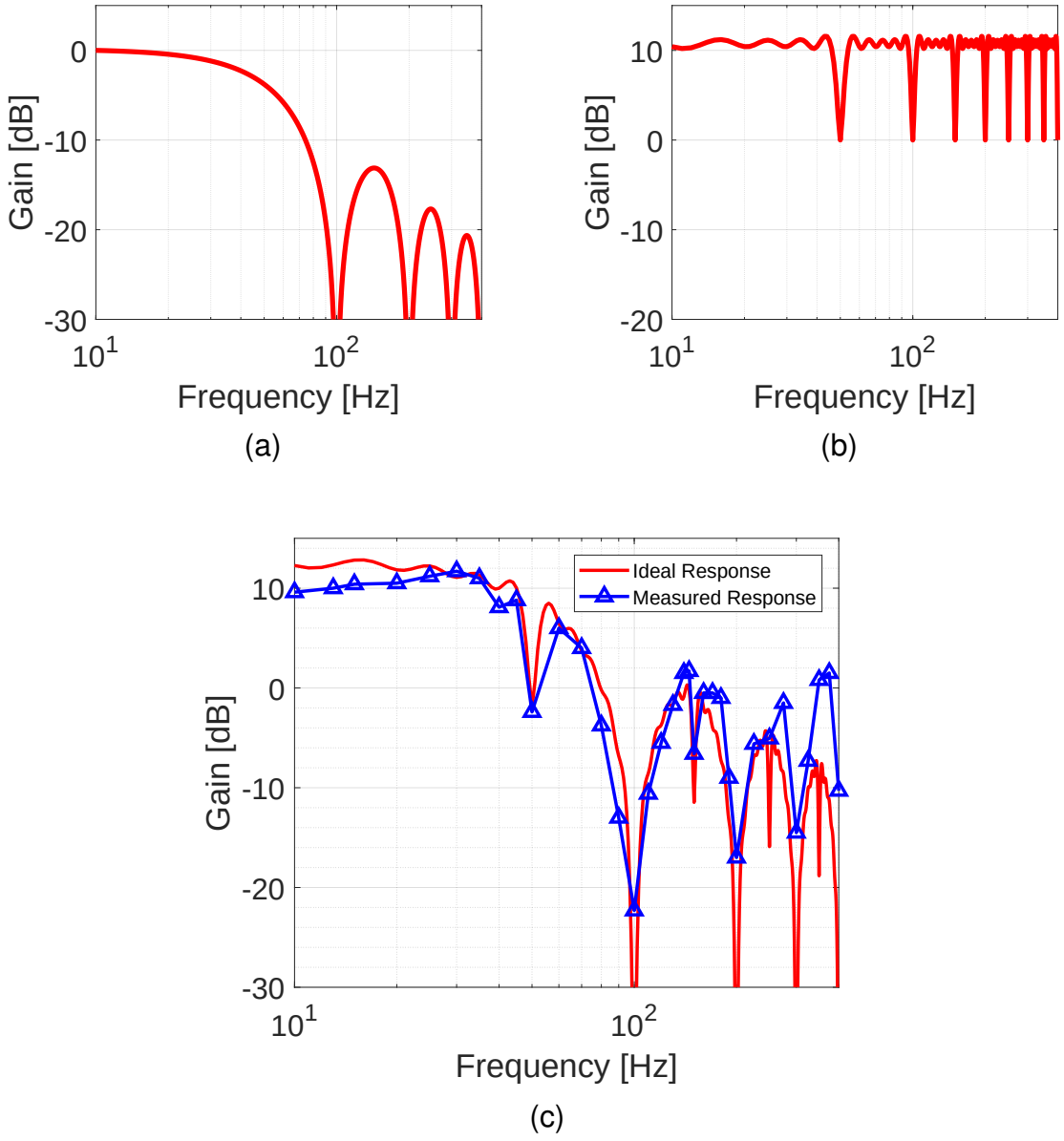
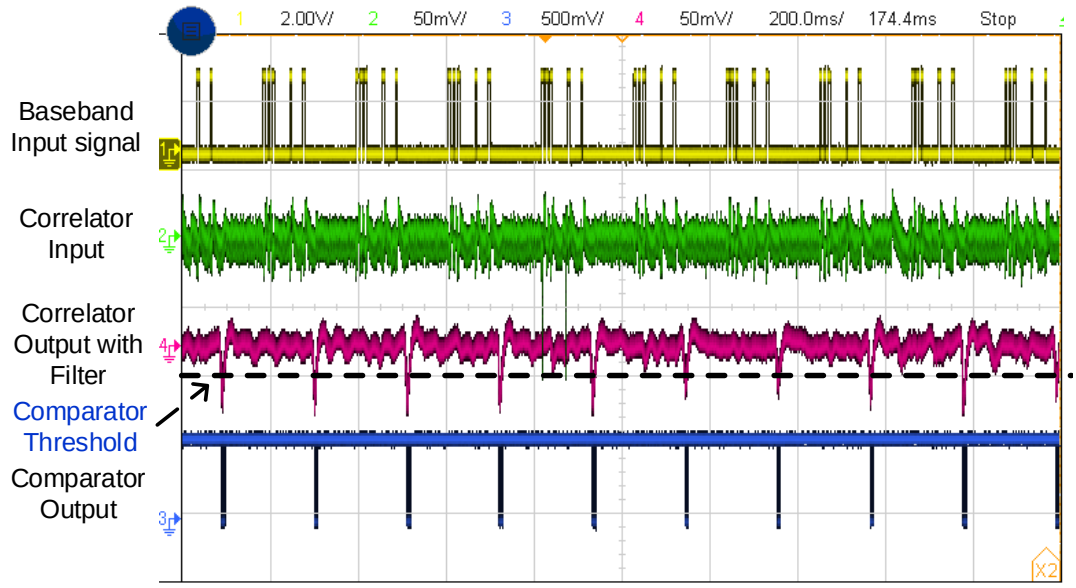
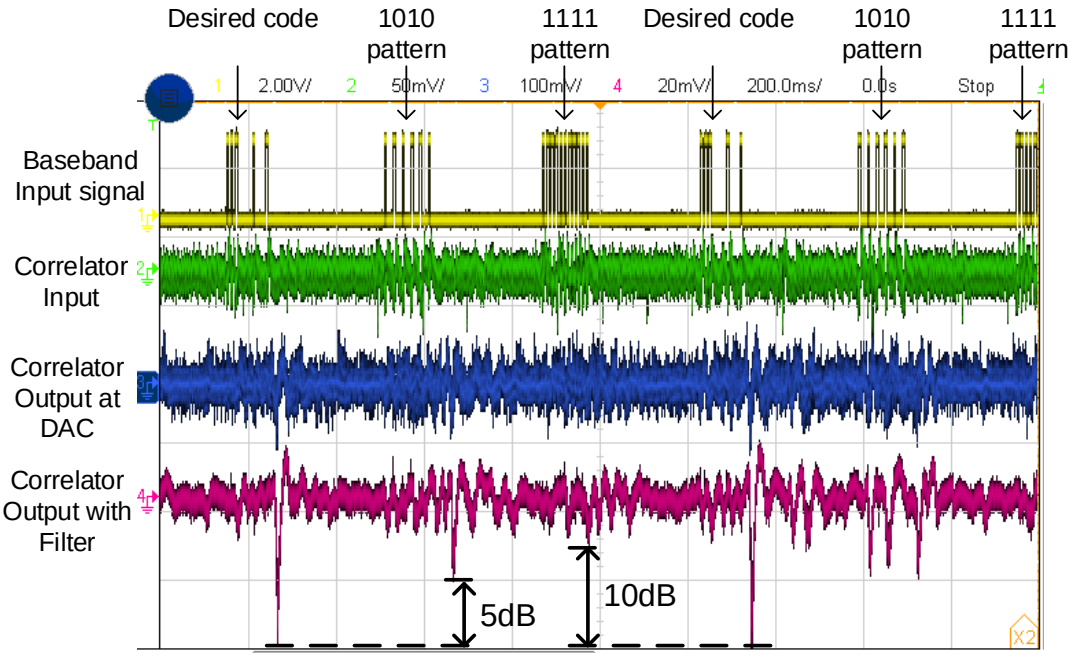


Figure 6.13: (a) 1-bit matched filter ideal frequency response; (b) spectral characteristics of the 11-bit Barker code; and (c) ideal vs measured frequency response of the implemented 11-bit matched filter.

the output of the correlator filter (Fig. 6.15c). The corresponding SIRs are 1.1 dB and −29.7 dB at a 3 MHz offset. Next, the rejection of unwanted 50% RZ-OOK encoded 11-bit codes with '1','0' symbols is measured. Fig. 6.14b demonstrates that the correlator provides a 5 dB rejection to the '10101010101' code and >10 dB rejection to '11111111111' code.



(a)



(b)

Figure 6.14: (a) Receiver response to the wake-up Barker code '11100010010' sent every 220 msec with the comparator threshold at −20 mV; (b) receiver response to the desired wake-up Barker code, '10101010101' code and to a '11111111111' code at 100 bps chip rate (comparator output not shown due to limited channels available on the oscilloscope). All codes use 50% RZ-OOK modulation.

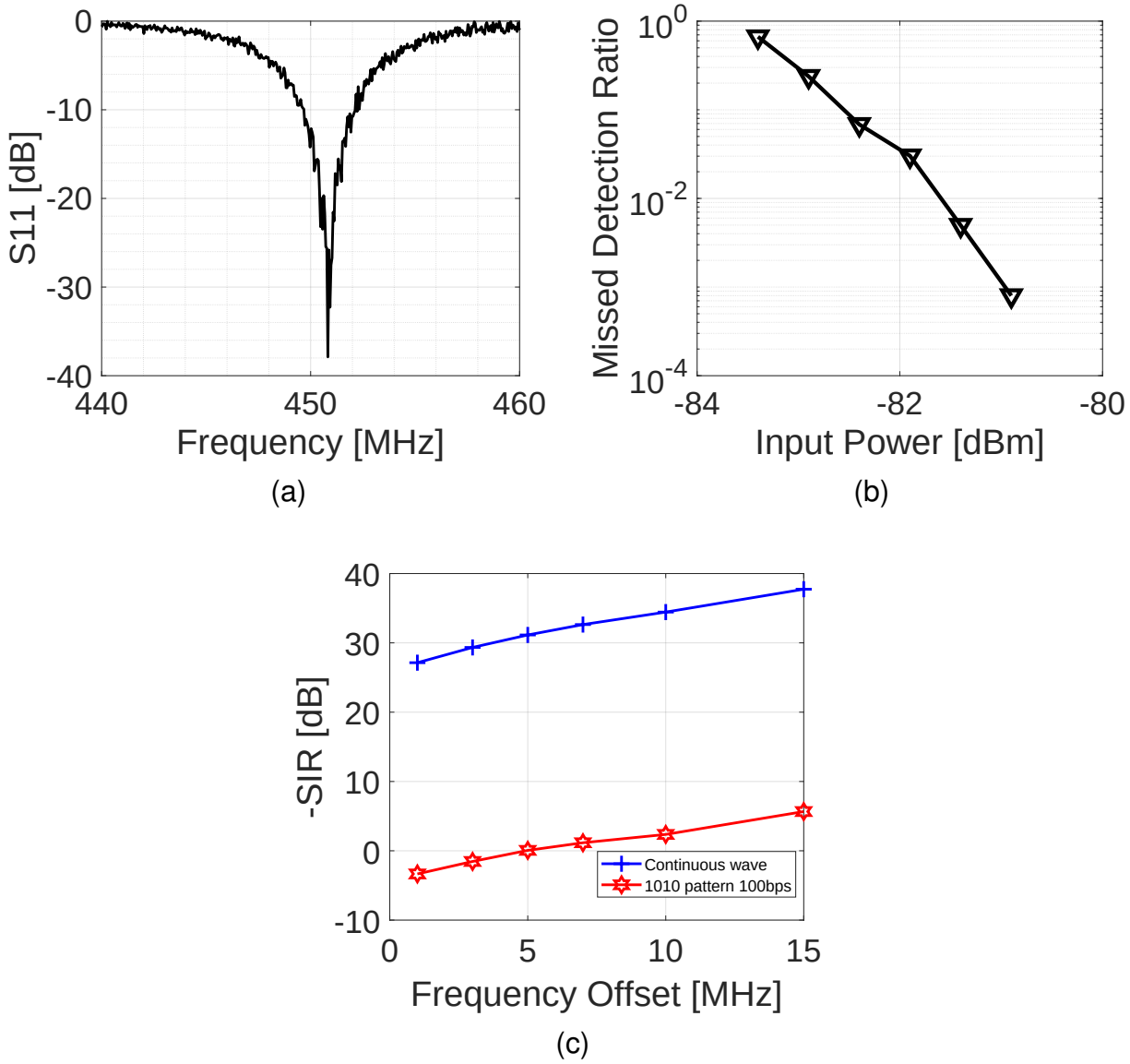


Figure 6.15: Measured wake-up receiver performance (a) RF Input reflection; (b) Missed-Detection Ratio at 450.8 MHz; (c) Signal to Interference Ratio for a continuous wave and a '1010' pattern AM interferer.

6.5.3 CDMA Operation

Here, to maximize the rejection to unwanted code in the correlator, we use RZ-OOK encoded 11-bit codes with '1','-1' symbols. We use <code1>:'11100010010' and <code2>:'11111001101' as in Fig. 6.4. First, the correlator is configured to receiver the <code1>, and <code1> is sent to the receiver, repeated every 110 msec. The time-domain response averaged over 50 responses to suppress the noise is shown in Fig. 6.16a. Next, <code2> is sent to the receiver with the same configuration. Fig. 6.16a shows a 5.5 dB rejection to <code2>. Similarly, the receiver is configured to receive <code2> and the response to <code2> and <code1> are measured. Fig. 6.16a shows a 4.5 dB rejection to <code1>.

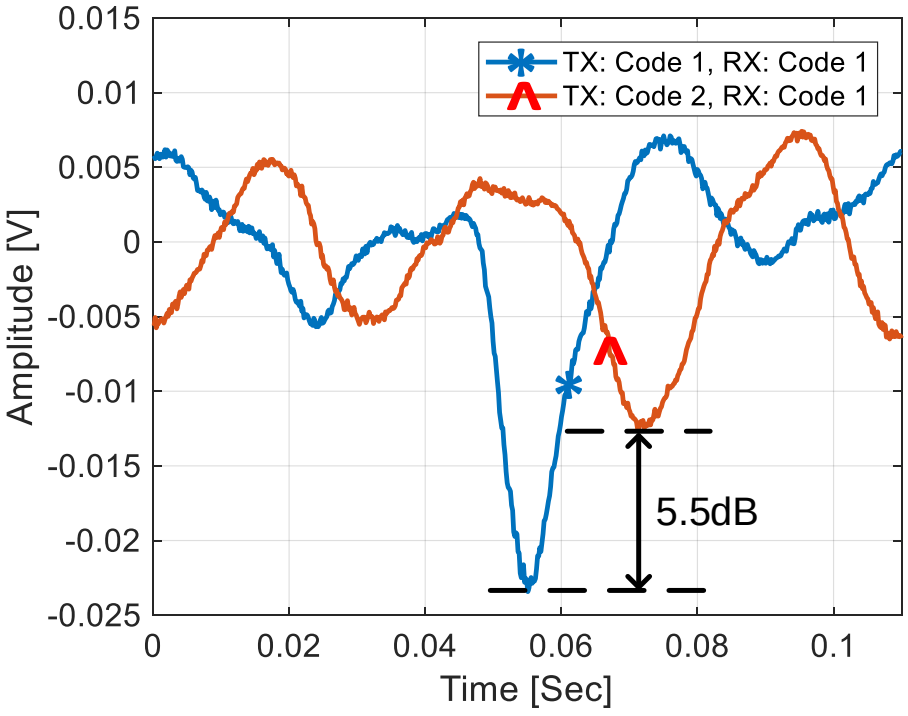
Next, a combination of <code1> and <code2> are sent to the receiver and response of the receiver for desired code of either <code1> or <code2> is measured. Fig. 6.17 demonstrates that the correlator output crosses the threshold in the presence of a wanted code and successfully rejects an unwanted code. This demonstrates code-domain multiple access for wake-up receivers.

6.5.4 Comparison to the State of the Art

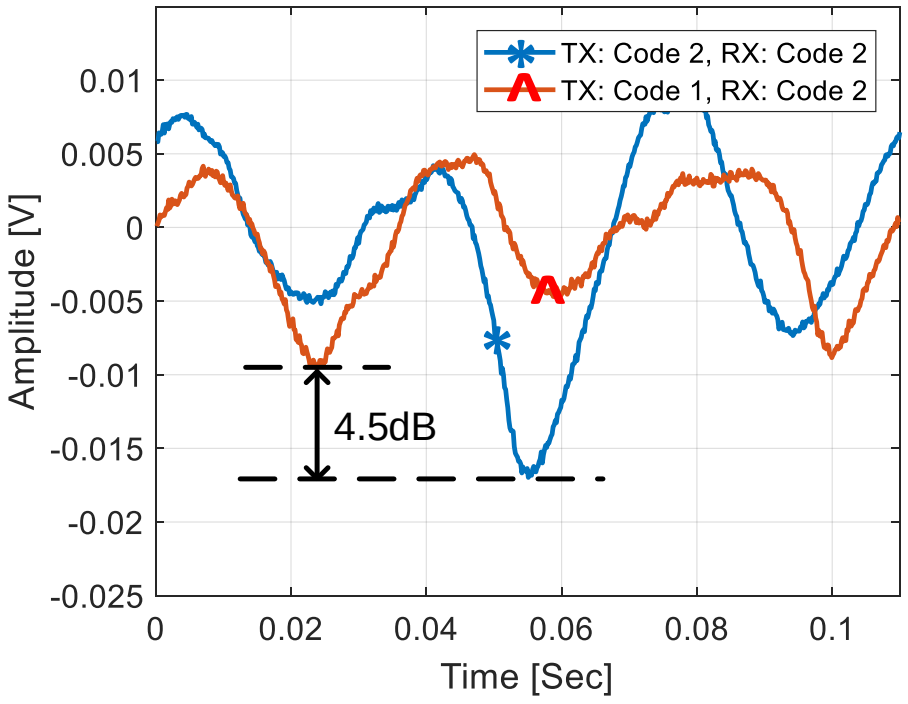
The receiver die (Fig. 6.18) uses an area of 0.15 mm^2 and consumes 40 nW with the correlator using 0.11 mm^2 and consuming 93% of the power. Comparison to the state-of-the-art wake-up receivers is tabulated in Table 6.1. Compared to the wake-up receiver using a digital correlator [47], the receiver has 2 dB better sensitivity, 5 dB better rejection to a worst-case AM interfer and 15 dB better rejection to a continuous-wave interferer, however this comes at a cost of 100x power consumption. More importantly, the receiver supports simultaneous wake-up of multiple nodes using different codes at a nominal power of 40 nW.

6.6 Conclusions

A continuous-time analog correlator using pulse-position encoding has been presented that is used as a code-domain matched filter to improve the sensitivity and selectivity of a wake-up



(a)



(b)

Figure 6.16: (a) Receiver selectivity to <code1>, averaged over 50 responses; (b) Receiver selectivity to <code2> averaged over 50 responses.

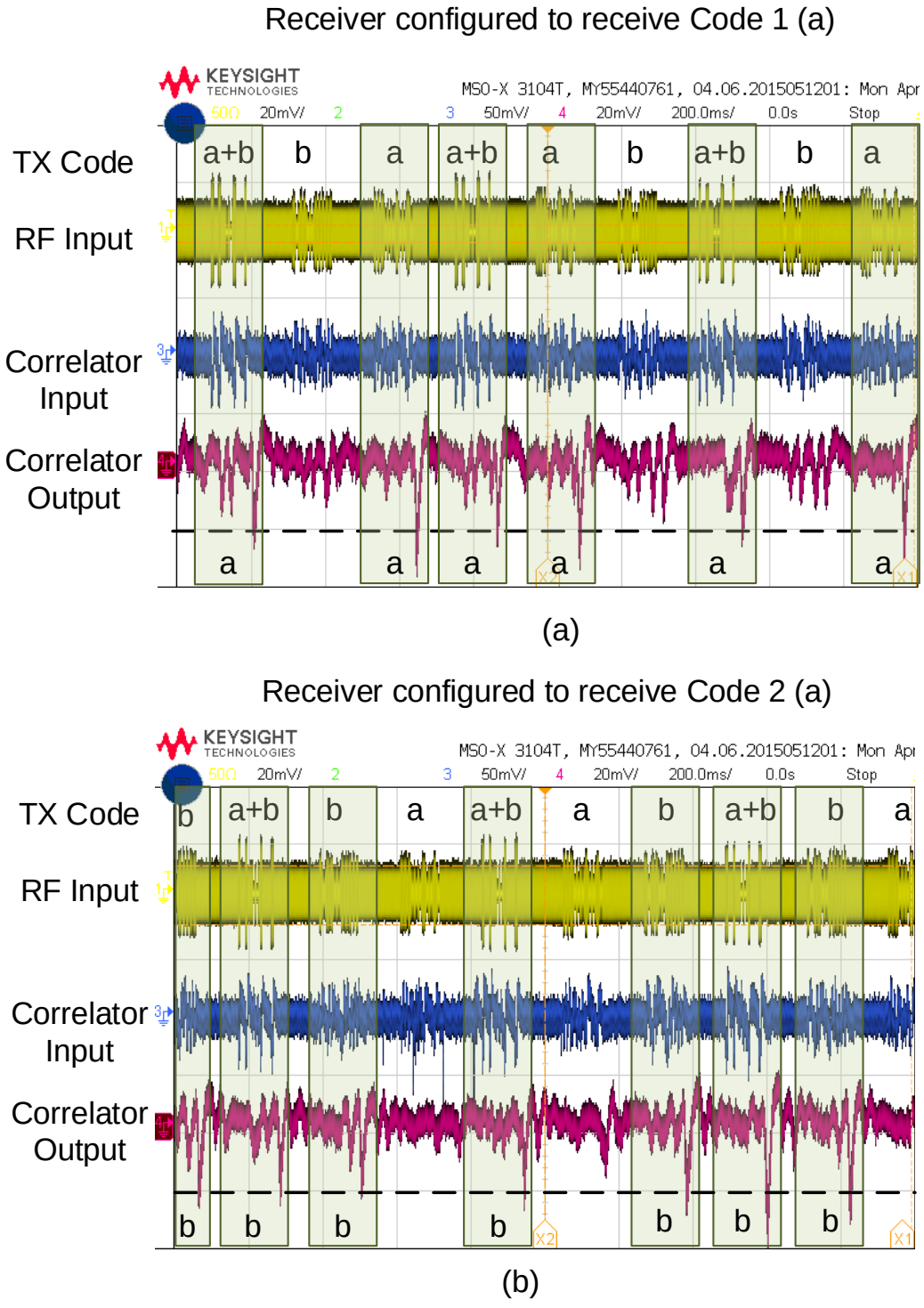


Figure 6.17: Receiver response for receiver configured to receive (a) <code1>; (b) <code2>.

Table 6.1: Comparison with the state-of-the-art ED wake-up receivers operating at > 400 MHz

	ISSCC'16	RFIC'17	CICC'17	ESSCIRC'17	ISSCC'18	ISSCC'19	**This Work**
Key Features	30-Stage Rectifier	Rectifier-Antenna Co-design	Self-Mixer	Active Rectifier	Passive Rectifier	Self-Mixer	**CT-Analog Correlator**
CMOS Tech. Node (nm)	65	65	130	180	130	65nm	**65nm**
Correlator	Digital	Digital	Digital	Digital	Digital	Digital	**Analog**
Frequency (MHz)	2400	2400	550	405	433	434	**450.8**
Chip Rate (kbps)	8.2	2.5	400	0.3	0.2	0.1	**0.1**
Code-length (bit)	31	32	11	16	16.5	11	**11**
Power (nW)	236	365	222	4.5	7.4	0.42	**40**
Passive Gain (dB)	NR	NR	19	18.5	NR	26	**26**
Sensitivity (dBm)	-56.5	-61.5	-56.4	-63.8	-71	-79.1	**-80.9**
Latency (msec)	3.8	12.8	0.0275	53.3	82.5	110	**110**
Circuit Area (mm^2)	0.25	1.1	0.2	6	1.95	0.05	**0.15**
Modulation	OOK	OOK	OOK	OOK	OOK	OOK	**RZ-OOK**
In-band SIR(3MHz away)							
Square wave AM interferer	NR	NR	NR~	4*	NR	5.8	**1.1**
C-Wave Interferer	NR	-19.1	-14	-28	NR	-14	**-29.67**
Normalized Sens.# (dBm)	-68.6	-71	-79.2	-70.2	-76.4	-83.9	**-85.7**
FoM^ (dB)	-134.9	-135.4	-145.7	-153.7	-157.7	-178.0	**-159.7**

~Not reported for a square-wave AM jammer

*For a PRBS AM interferer

#Normalized Sens.=Sensitivity + 5log(Latency/1s)

^FoM=Normalized Sens. + 10log(Power/1W)

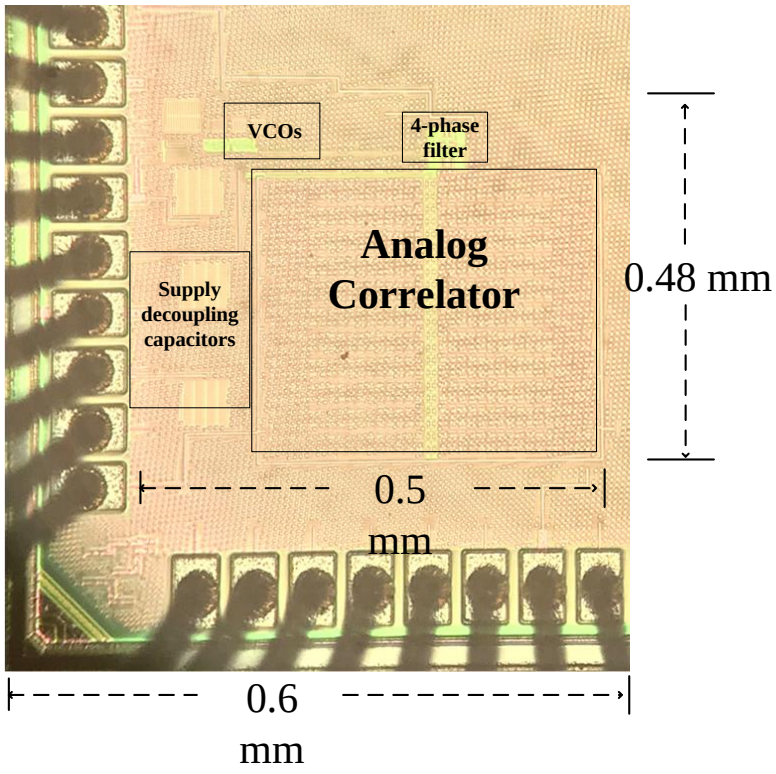


Figure 6.18: Chip micrograph implemented in 65 nm LP-CMOS technology.

receiver. The architecture is entirely asynchronous, mitigating the requirement for clock recovery. The 450 MHz receiver prototype designed in 65 nm CMOS-LP technology consumes 40 nW from 0.54 V, and demonstrates code-domain filtering for an 11-bit Barker code. The wake-up receiver using the analog correlator has a −80.9 dBm sensitivity with 2 dB enhanced sensitivity and 5 dB improvement in selectivity thanks to the correlator. Selective response of the receiver to different desired codes with rejection to an undesired code is presented to demonstrate CDMA operation.

Chapter 7: Directional Backscatter Tags

The thesis so far has focused on the design of a very low-power receiver while adding reliability to the link. But, the achievable sensitivity might still not be enough for several applications. Here, spatial gain as generally used in reflectarray antennas can be used to improve the link. This chapter will describe the design of a multi-antenna directional backscatter tag. The tag can be used on a wall as a directional reflector to achieve multi-path gain for spatial gain and selectivity. The tag can also be used as a transmitter for relatively longer range RFID applications such as in automated car parking.

Backscatter modulation is gaining traction to connect billions of everyday objects at low power, enabling ubiquitous sensing and computing capability [55, 56]. Fundamentally, the range of backscatter communications is limited since the path loss $\propto d^4$. Recently the range of backscatter transmission has been increased by decreasing the data rate to as low as 50 bps [57, 58]. However, low data rates might not be feasible for several latency critical applications [59]. In Fig. 7.1 a backscatter communication setup [55] is shown where the transceiver in the reader transmits the signal to and receives the reflected signal from the tag simultaneously. A single antenna backscatter tag reflects the signal back in all directions, but the signal of interest is only in the direction of the reader. We use a multi-antenna tag to backscatter a directional beam to the reader; e.g., using 3x3 array can provide a 19 dB sensitivity enhancement and an up to 3x increase in range [60].

Gains for multi-antenna tags using pinhole diversity has been analyzed theoretically in [61], but measurement results in [62] suggest that it provides very small gains for LOS backscatter channels. Phase conjugation techniques have been used to transmit the signal back in the DoA [63]. These transceivers implement DoA detection using phased array processing and use the conjugate of the received phases for the transmit antenna array. A retrodirective array phase modulator (RAPM) has been proposed in [64] for a linear antenna-array RFID tag using transmission lines.

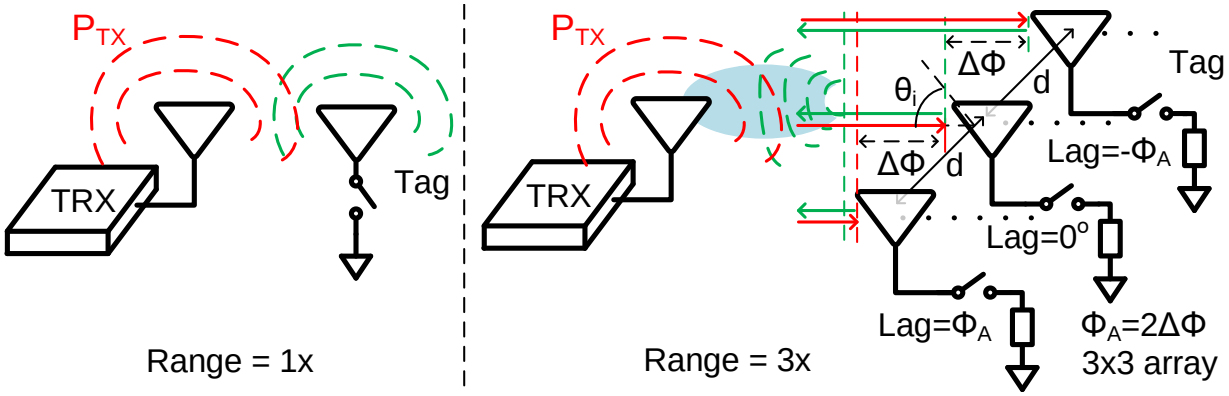


Figure 7.1: Traditional backscattering with a 1-antenna tag vs proposed directional backscattering with a 3x3 antenna-array tag, that can provide a 3x range.

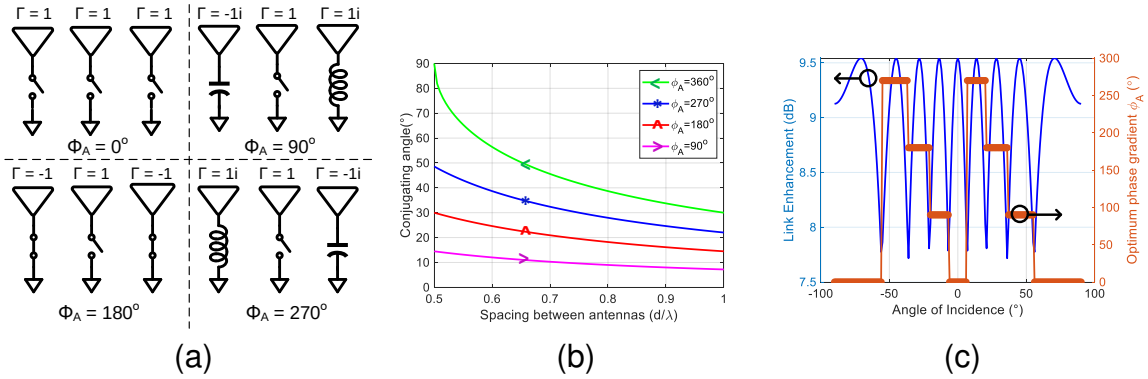


Figure 7.2: Analysis of a 3x1 antenna array for backscattering: (a) Available phase-gradient (ϕ_A) configurations using standard QPSK loads; (b) Calculated conjugating angle for different ϕ_A w.r.t. antenna spacing; (c) Evaluated maximum link budget enhancement for a 3x3 antenna array in the horizontal plane and the corresponding required phase gradient ϕ_A thanks to directional backscattering w.r.t. angle of incidence, θ_i, using 0.53λ antenna spacing.

Extending RAPM to a 2D array requires crossing transmission lines, which is practically infeasible. We demonstrate a compact phase conjugation technique for backscatter modulation on a 2D array, thus achieving maximum directivity in the DoA. Sec. 7.1 describes the operation principle for directional backscatter. Sec. 7.2 outlines the design of a compact, low power 3x3 directional backscatter tag as a proof of concept. The measurement setup and experimental results are discussed in Sec. 7.3.

7.1 Directional Backscatter Tag

The incoming RF signal is reflected back by the backscatter antenna with different phase lags depending on its load. Using open, short, inductive and capacitive loads a backscatter QPSK modulator has been implemented for a single antenna tag [55]. In the proposed multi-antenna tag, each antenna can switch between these loads for QPSK modulation, while the same loads are also used to create a directional backscattered signal.

7.1.1 Directional Backscattering in a Linear Array

Let's first assume a linear array of 3 antennas with an antenna spacing of d (Fig. 7.1). For an incident signal at an angle θ_i, when operating in the far field, incident waves with wavelength λ received by adjacent antennas have a phase difference of $\Delta\phi = 2\pi.d.sin(\theta_i)/\lambda$. To reflect the signal back in the DoA, the reflected signal must have a phase difference of $-\Delta\phi$. Thus, the loads of adjacent antennas need to provide an extra phase difference of $\phi_A = -2\Delta\phi$. If the phase lag of the middle antenna is $\phi_r = 0°$, the other two antennas require a phase lag of ϕ_A and $-\phi_A$. Using the four standard QPSK loads, the phase gradient ϕ_A can be 0°, 90°, 180° and 270° (Fig. 7.2a). For these values of ϕ_A, the corresponding angle of incidence (conjugating angle) at which the backscatter tag achieves maximum directivity of the reflected signal in the DoA is plotted in Fig. 7.2b for increasing spacing between the antennas. By using an antenna spacing of 0.53λ, evenly spaced conjugating angles of 15°, 30°, 45° and 60° can be obtained.

7.1.2 Directional Backscattering in an NxN Array

For an NxN array, assuming the required horizontal and vertical phase gradients are ϕ_A and ϕ_B, the required phases for $(i, j)^{th}$ antenna in the array is $\phi_{ref}(i, j) = (i-(N+1)/2)\phi_A + (j-(N+1)/2)\phi_B$. The tag needs to determine the gradients ϕ_A and ϕ_B using DoA estimation (discussed in Sec. 7.1.4). An NxN array can provide N^4 times the link enhancement (e.g., 19 dB for a 3x3 array), thus N times the range. For $\phi_B = 0$, the backscatter tag directivity is plotted at $\theta_i = 0°, 30°, 45°, 60°$

using the corresponding ϕ_A in Fig. 7.3 for a 3x3 array. The directivity improves by 9 dB for the conjugating angles. For $\phi_B = 0$, the maximum achievable array factor is plotted w.r.t. the angle of incidence θ_i in Fig. 7.2c. Limiting the loads to the four QPSK loads leads to a quantization error in ϕ_A and a degradation of up to 2 dB in the array gain.

7.1.3 Directional Backscattering with QPSK modulation

By changing the reference phase ϕ_r, while maintaining the phase gradients ϕ_A and ϕ_B, QPSK modulation can be implemented with directional backscattering. For a baseband signal mapped to a QPSK phase $\phi_m(t)$, the required phase for the $(i, j)^{th}$ antenna is $\phi(i, j, t) = \phi_{ref}(i, j) + \phi_m(t)$.

7.1.4 Compact DoA Estimation using RSSI

For an incoming wave at an angle of incidence θ_i, any two adjacent antennas in a 3x1 linear array receive signals $V_1(t) = A.sin(\omega.t)$ and $V_2(t) = A.sin(\omega.t + \phi)$ where $\phi = 2\pi.d.sin(\theta_i)/\lambda$. Adding the signals in-phase (Fig. 7.4a) provides a measure of $2.A.cos(\phi/2)$ which allows to detect θ_i. The sum of the two signals normalized with the received power on one antenna is plotted as $RSSI_1$ in Fig. 7.4b. However, $RSSI_1$ is symmetric w.r.t. $\theta_i = 0$. The sign of θ_i can be evaluated using the derivative of $RSSI_1$, measured by connecting inductor in parallel to either antennas (Fig. 7.4a) and subtracting the received signal strengths: $RSSI_2 - RSSI_3$ is plotted in Fig. 7.4b. DoA can be successfully estimated over a range of θ_i from $-60°$ to $60°$. For $|\theta_i| > 60°$, $RSSI_1$ is less than -13 dB and the required phase gradient, $\phi_A = 0°$.

7.2 Design of a Proof-of-Principle Demo System

To demonstrate the principles of directional backscattering communications, we designed a directional backscatter tag on a PCB using off-the-shelf RF components and with baseband backscatter modulation implemented on a micro-controller (Fig. 7.5). A full-duplex transceiver for the reader has been implemented on a software-defined radio (USRP) to transmit the carrier and receive the backscattered signal.

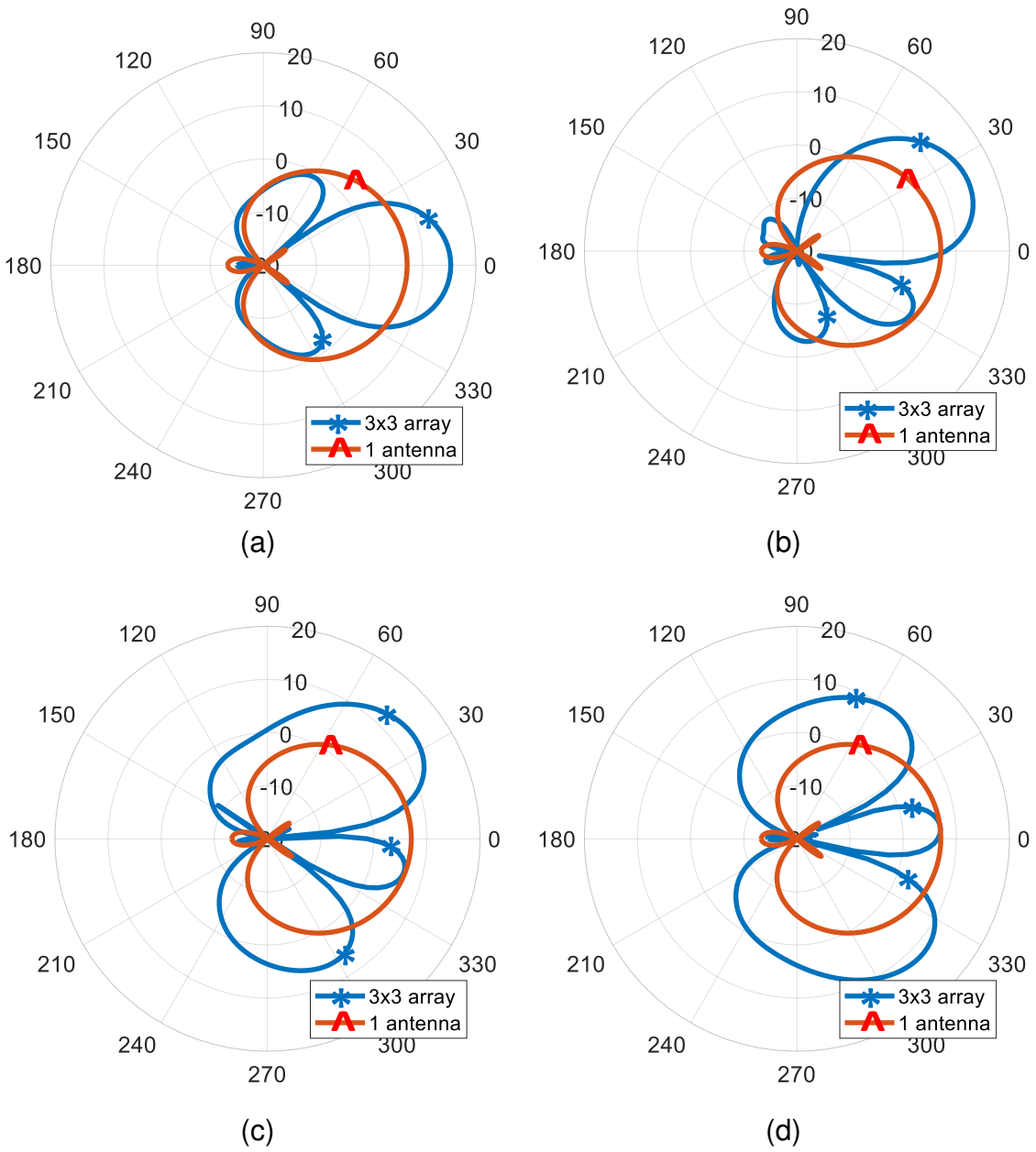


Figure 7.3: Simulated directivity enhancement using 3x3 array tags in the horizontal plane with angle of incidence and the corresponding phase gradient (ϕ_A) of (a) 0°, 0°, (b) 30°, 180°, (c) 45°, 270° and, (d) 60°, 0°.

7.2.1 Tag Hardware

A 3x3 antenna array using patch antennas sized 3 cm by 3.8 cm with 6.5 cm center to center spacing was designed at 2.45 GHz on 31 mil-thick ISOLA 370HR substrate (Fig. 7.6). SMD 3 nH 0201 inductor and 1.3 pF 0402 capacitor are used for load modulation. An SP5T switch

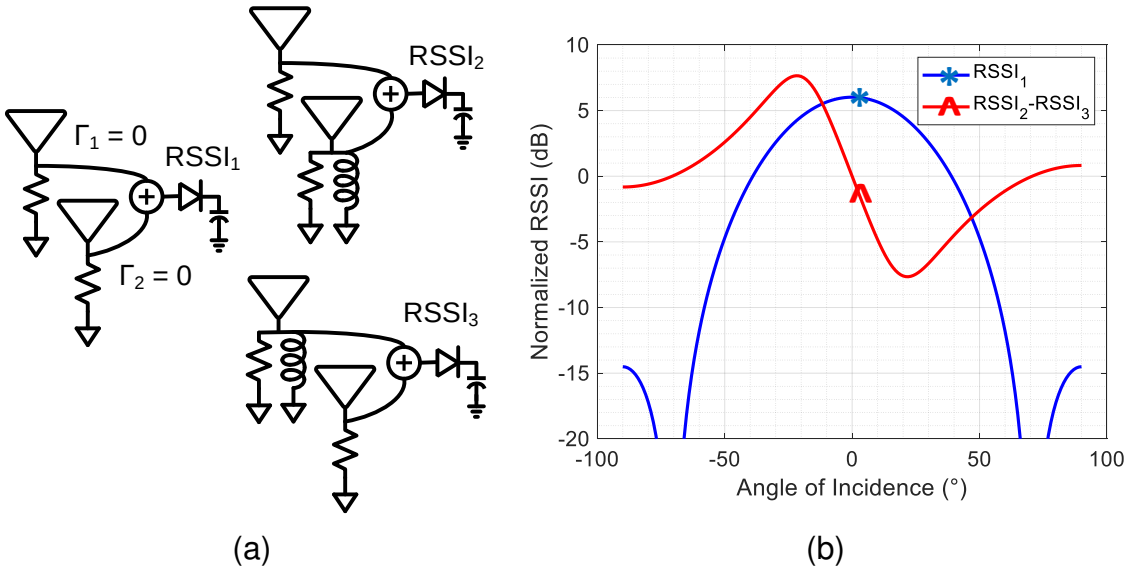


Figure 7.4: Direction-of-arrival estimation in the tag over a range of $|\theta_i| < 60°$: (a) adjacent antenna configurations for RSSI measurements; (b) calculated $RSSI_1$ provides the estimate of $|\theta_i|$, calculated $RSSI_2 - RSSI_3$ provides the sign of θ_i, the angle of incidence. For $|\theta_i| > 60°$, phase gradient is 0°.

(SKY13415) is used to switch the antenna load for load modulation and determining the DoA. A power combiner (SP-2U2+) is used to add signals from two antennas in phase. A power detector (LT5538) is used to detect the received signal strength from the power combiner. 10-bit ADCs on Teensy 3.6 MCU are used to digitize the output of the power detector. Detecting the DoA, DoA mapping to the required phase gradients, QPSK modulation, and generation of control signals for switches on each antenna is implemented on the same MCU.

7.2.2 Full-Duplex Reader Transceiver using USRP

A USRP B-210 SDR has been used to implement a full-duplex transceiver (Fig. 7.5) using the reader architecture in [55]. The TX1 channel transmits a 2.45 GHz signal and the RX1 channel receives the backscattered signal. One Wifi antenna is used for transmit and one for receive. The antennas have an isolation of 25 dB at 2.45 GHz. Further, RF cancellation provides 34dB rejection for the coupled TX1 signal to the RX antenna. The coupled carrier is further rejected using DC blocking and high-pass FIR filters at baseband.

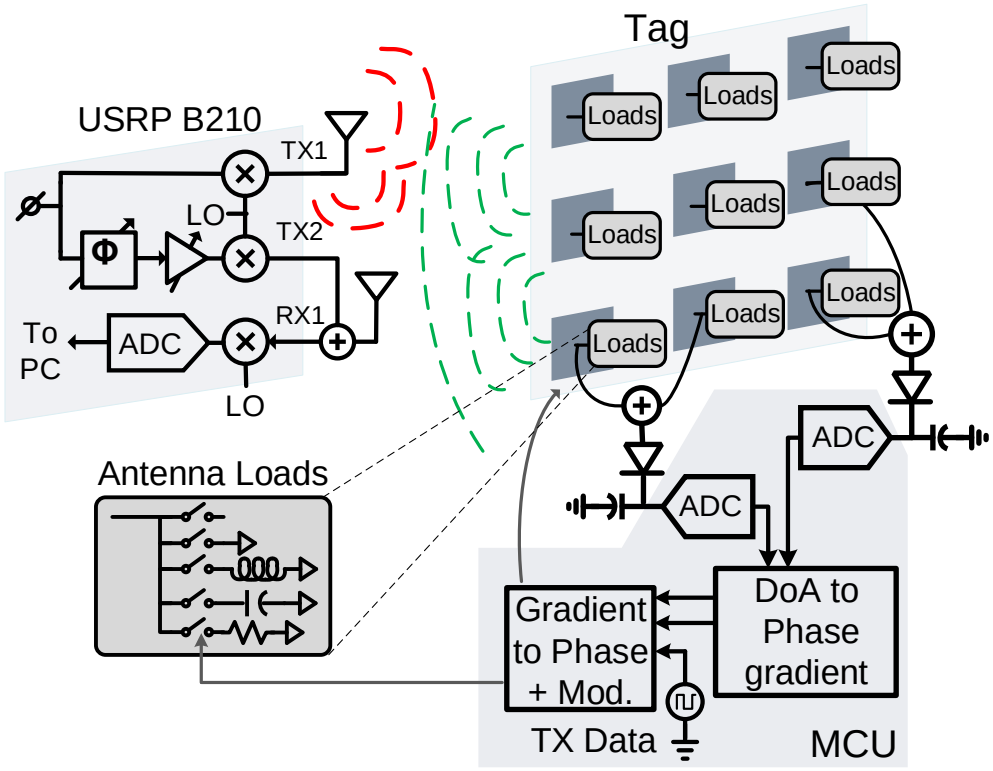


Figure 7.5: Diagram of the proof-of-principle prototype of a 3x3 directional backscatter tag and reader.

7.3 Measurement Setup and Results

Fig. 7.6 shows the setup for over-the-air measurements to evaluate the radiation pattern for backscatter tags. The backscatter tag is mounted on a rotator with a protractor to keep track of the angle of arrival. The tag is kept at a distance of 1 meter ($\approx 8\lambda$) from the TRX antennas. This results in around 80 dB path loss for the backscatter signal. A 15 dBm RF carrier is transmitted while the RX antenna is connected to the spectrum analyzer to measure the backscattered signal. As per the analysis, the measurements are carried out in the horizontal plane with vertical phase gradient, $\phi_B = 0°$.

First, to evaluate the operation of a single antenna tag, only the middle antenna of the backscatter tag was modulated with a 20 kHz BPSK signal, and the signal generator frequency was swept from 2 GHz to 3 GHz. The center frequency of operation for the antenna was found to be shifted to 2.33 GHz. Next, the reader transmits a 15 dBm signal at normal incidence and only the middle tag

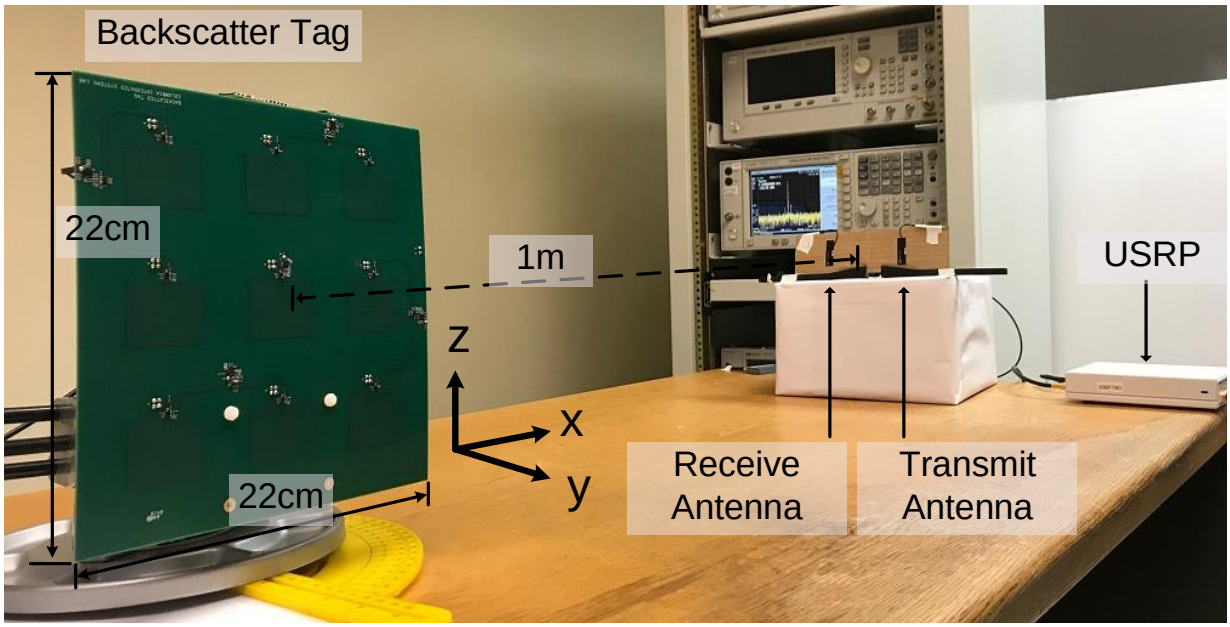


Figure 7.6: Measurement setup with the 3x3 2.45 GHz backscatter tag turned to a 90° angle of incidence for better visibility.

antenna is BPSK modulated. The received BPSK signal has a strength of −79.1 dBm (Fig. 7.7a). A strong carrier is present due to the coupling from the TX antenna. To measure the enhancement in the link budget from directional backscattering, the 3x3 array is BPSK modulated with $\phi_A = 0°$, $\phi_B = 0°$, receiving a −59.1 dBm signal (Fig. 7.7b), thus providing a 20 dB enhancement in the link, providing an up to 3x increase in range. The improvement is slightly higher than expected due to gain mismatch in the antennas.

Then, to evaluate the conjugating angles as described in Sec. 7.1.1, the tag is rotated with 2.5° steps in the horizontal plane, and the received signal strength is measured across angle of incidence for single antenna as well as a 3x3 array with horizontal phase gradient $\phi_A = 0°$, 90°, 180°, and 270°. The results are plotted in Fig. 7.8. For most angles of incidence, the 3x3 array achieves a 19 dB improvement in the link when using the appropriate ϕ_A for the specific DoA. As predicted in Fig. 7.2c, the conjugating angles are measured to be 0°, −70° and 70° for $\phi_A = 0°$; −15° and 40° for $\phi_A = 90°$; −30° and 30° for $\phi_A = 180°$; −40° and 15° for $\phi_A = 270°$. The results are slightly shifted from the directivity plots in Fig. 7.3 due to the reduced carrier frequency resulting

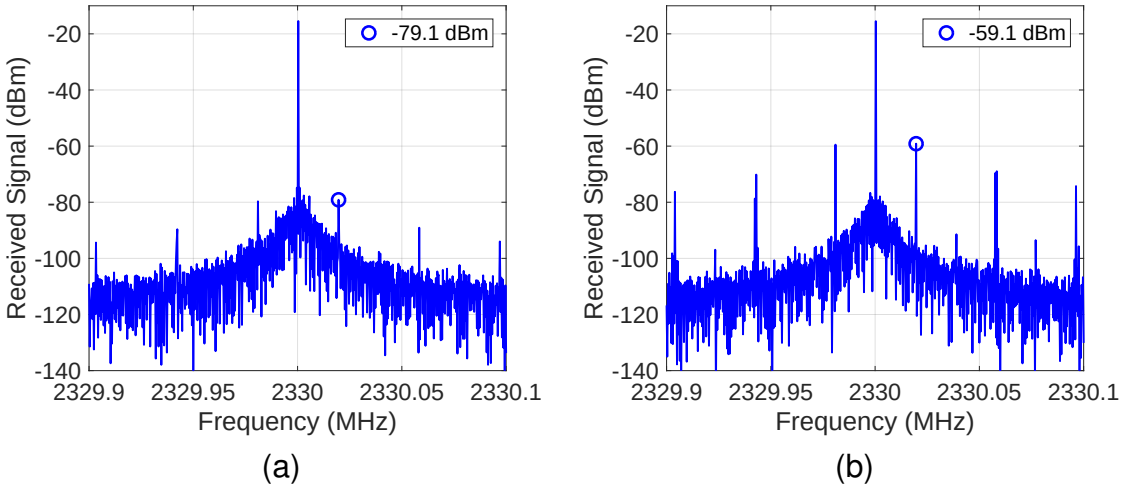


Figure 7.7: Received backscattered signal spectrum with normal incidence using (a) one antenna backscatter, (b) 3x3 array with 0° phase gradient (ϕ_A).

in a 0.51λ antenna spacing rather than the designed specification of 0.53λ.

The angle of arrival estimate using the proposed DoA measurement is shown in Fig. 7.9a. The measurements were taken with tag at a distance of 40 cm from the TRX antennas to avoid possible SNR degradation due to interference. The measured angle has an 8° RMS error due to mismatch between paths connecting antennas to the power combiner. A 5° error in DoA estimate is acceptable with minimal degradation in sensitivity. In the current setup, the measured results for $|\theta_i| > 45°$ are unreliable due to the presence of strong out-of-band interferers.

Next, the 3x3 antenna array was QPSK modulated with $-45°$ angle of incidence and a phase gradient of $\phi_A = 270°$. The backscattered signal was received using the USRP and the signal constellation is plotted in Fig. 7.9b, demonstrating a QPSK link with directional backscattering. Some constellation distortion is observed, probably due to the signal dependent gain in the antenna switches.

7.4 Future Work

Compared to traditional backscattering in Fig. 7.1, using an NxN antenna array at the reader with an NxN tag will provide N^3 increase in range. For the same setup, assuming area constrained

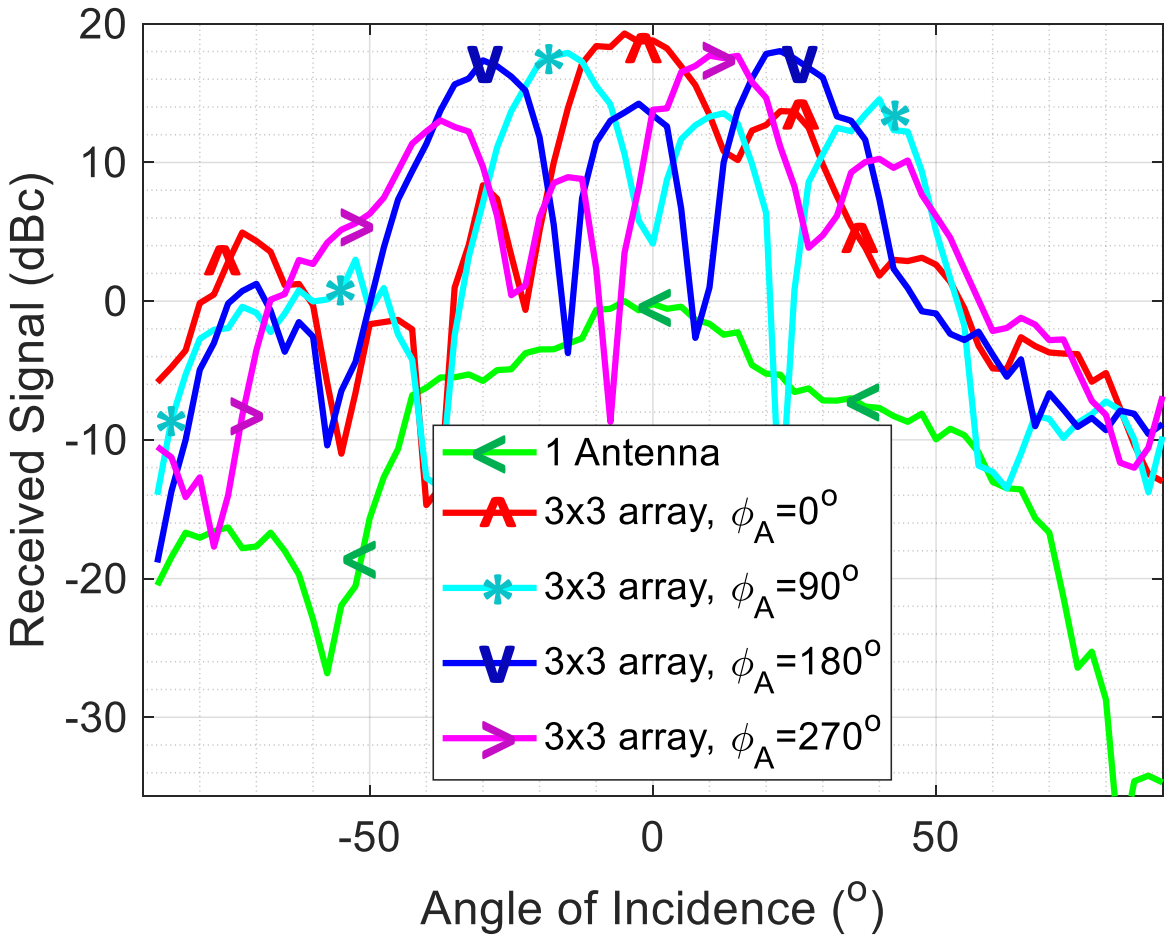


Figure 7.8: Received backscattered signal strength at the reader receiver versus angle of incidence(w.r.t. x-axis) with tag rotated in the xy plane for different phase-gradients (ϕ_A) configurations in the 3x3 tag; the signal strength is relative to the peak signal received for a single-antenna tag.

applications, using N times the carrier frequency with antenna aperture similar to 1x1 array improves the range $\sqrt{N^3}$ times. Increasing the number of antennas and antenna loads will allow higher order modulations with narrower beams for more efficient data transfer or security from unwanted readers. By implementing custom RF chips, the proposed tag can be operated at ultra-low power e.g., using energy-detection receiver architecture of [42]. DoA estimation performance can be improved by mitigating interference using band select filters or spread spectrum techniques. Lastly,

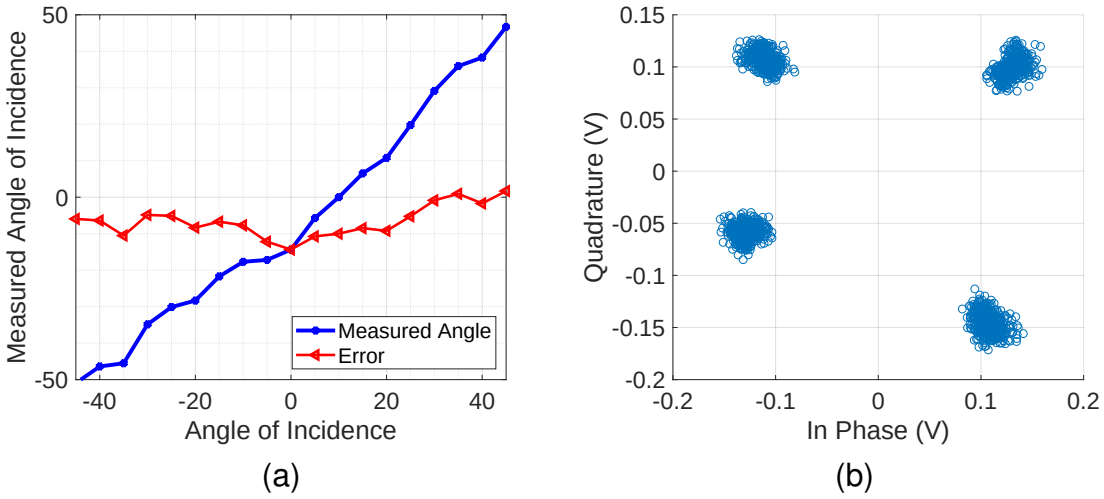


Figure 7.9: (a) Measured angle of incidence, (b) Constellation plot for QPSK modulation using a directional backscatter tag with 90° phase gradient.

RF switches will be characterized for selecting loads to reduce distortion. Such ultra-low-power operation with DoA functionality will enhance the use of tags for navigation and localization applications.

7.5 Conclusions

We proposed the use of phase gradients in multi-antenna tags to realize directional backscattering to significantly improve the range of backscatter communications. The gradients can be created using standard antenna loads from QPSK backscatter modulation. A low-power DoA estimation technique is proposed based on RSSI measurements with different antenna load configurations. Directional backscatter with QPSK modulation using a 3x3 antenna-array tag is demonstrated in a proof-of-concept system at 2.33 GHz, providing a 19 dB link enhancement, promising an up to 3x increase in range. The measured RMS error in the DoA estimation is better than 8°, sufficient for a 30° beamwidth.

Chapter 8: Conclusion and Future Directions

In the final chapter of this thesis, the scope and depth of the research work is revisited, and its scientific contributions are highlighted. Suggestions for future research in the area of low-power transceivers are outlined.

Summary

This thesis discussed the challenges in designing low-power receivers using energy detectors. The thesis starts with noise-analysis for passive-RF front end with energy detector. The requirements lead to self-mixers which operate as optimal energy detectors for power consumption below 100 nW. Using the self-mixer, a sub-nW wake-up receiver architecture is proposed, providing the optimal sensitivity based on the losses in the front end.

For passive-RF energy-detector receivers, the sensitivity is limited by the front-end losses and the selectivity is limited by filtering at RF frequency. Here, the use of interferers as LO is proposed to enhance both the sensitivity and the selectivity of the receiver, but the performance is still limited in the presence of a wide-band AM interferer. To improve the selectivity to interference, a clock-less continuous-time analog correlator is proposed which provides code-domain selectivity. Additionally, the clock-less analog correlator mitigates the need for synchronization with the input signal.

The energy detector receivers don't provide any in-band frequency-domain selectivity, thus multiple access is difficult. Here, the proposed analog correlator serves as a DS-CDMA matched filter to enable simultaneous wakeup signatures using different codes at the same carrier frequency.

The link for the energy-detector receivers can further be enhanced by using directive antennas e.g. reflectarrays. A low-power directional backscatter tag using passive load-modulation tech-

nique is proposed which can act as a directional reflector to enhance the directivity of the receive antenna. These passive tags can be placed on the walls, bridges or other existing infrastructure around the receiver. Here, advanced algorithms need to be devised to localize the receiver for such links to achieve best performance.

Contribution to Literature

To improve the sensitivity of the passive-RF energy-detector receiver:

- We propose self-mixers a.k.a. gate-biased energy detectors which operate as optimal energy detectors for passive-RF front end and provides better SNR compared to active energy detectors for less than 100nW power consumption.
- We propose continuous-time analog correlator which provides better conversion gain than a digital correlator for improved sensitivity.
- We propose the use of interferer as LO, to further improve the sensitivity in the presence of a strong narrow-band interferer.
- Directional backscatter tag is proposed which can operate as a reflectarray to improve the directivity of the receive antenna in suitable environments.

To improve the selectivity of the passive-RF energy-detector receiver:

- We propose the use of interferer as LO which provides improvement in selectivity to modulated interferers.
- The performance using an interferer as LO degrades in the presence of a wideband AM interferer. A continuous-time analog correlator is proposed to suppress these AM interferers and improve the selectivity.

Further, to enable multiple access, the continuous-time analog correlator is proposed to enable code-division multiple access for simultaneous wake-ups in the same frequency bands.

Recommendations for Future Work

The passive-RF energy-detector receivers are limited in sensitivity by the losses in the front end and the achievable conversion gain constant k_{ed}. A high sub-threshold slope is desired for an improved conversion gain. Recent work on Nanowire FET's [33] proposes an achievable sub-threshold slope of 6mV/decade and can be promising for future designs.

We proposed techniques to improve selectivity for energy-detector receivers, however, the best way to achieve this selectivity is to use an RF filter in the front end. The selectivity can be enhanced by using a channel select filter e.g. using MEMS. But, the requirements get more stringent with increasing carrier frequency. For higher carrier frequency, the front-end losses increase, thus the sensitivity will degrade further when using a passive-RF front end. Here, the use of duty-cycled active-RF amplification with the energy detector receivers can improve the performance.

Apart from application to energy-detector based wake-up receivers, the self-mixers can also be used for energy harvesting. A successful signal detection is dependent on $v_{ed,out}^2/r_{out}$ (since the noise is directly proportional to r_{out}), this is equivalent to the output power available from the self-mixer as well. Thus, self-mixers doesn't just serve as optimal energy detectors, but are also an optimal RF to DC power converters for low input signals.

The continuous-time analog correlator can additionally be used for synchronization purposes. The 1-bit clock-less matched filter for a rectangluar bit can be used in the baseband for clock-less matched filtering without analog-to-digital conversion. The wide-band linear continuous-time digital delays used for the analog correlator design can also serve as true time delays for phased arrays.

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