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Qifeng Lu, Ce Zhou Zhao, Chun Zhao, Steve Taylor, and Paul R. Chalker

Investigation of Anomalous Capacitance-Voltage Behavior Caused by Interface Dipoles and the Effect of Post-Metal-Annealing

Qifeng Lu[1, a)], Ce Zhou Zhao[2, b)], Chun Zhao[3], Steve Taylor[1] and Paul R. Chalker[4]

[1]*Department of Electrical Engineering and Electronics, University of Liverpool, Liverpool L69 3GJ, UK.*
[2]*Department of Electrical and Electronic Engineering, Xi'an Jiaotong-Liverpool University, Suzhou 215123, China*
[3]*Nano and Advanced Materials Institute, Hong Kong University of Science and Technology, Kowloon, Hong Kong, China*
[4]*Center for Materials and Structures, School of Engineering, University of Liverpool, Liverpool L69 3GH, UK*

[b)]Corresponding author: cezhou.zhao@xjtlu.edu.cn
[a)]Qifeng@liverpool.ac.uk

Abstract. Anomalous capacitance-voltage (CV) behavior was observed in MOS devices with zirconium oxide gate dielectrics using pulse CV technique. The relative positions of up and down CV traces measured by pulse technique were opposite to those by conventional CV measurement. This unusual phenomenon cannot be inconsistently explained by charge trapping and de-trapping mechanisms. Therefore, a hypothesis related with interface dipoles was proposed. With regard to the formation of the interface dipole, it may be related to the oxygen density difference between the high-*k* layer and native SiO_x layer. In addition, this anomaly was sensitive to growth temperature as well as post-metal-annealing process. However, after annealing in either nitrogen or forming gas ambient, the relative positions of up and down CV curves measured by the pulse technique were consistent with those obtained by conventional CV measurement.

Keywords: Anomalous capacitance-voltage, MOS, $Zr(NMe_2)_4$

INTRODUCTION

With the continuous scaling down in Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs),SiO_2 based devices have reached their physical limitation. When the thickness of the SiO_2 gate dielectric is below 1.4 nm, the electron tunneling effects and leakage current become serious obstacles for the device reliability [1]. The replacement of SiO_2 with high-*k* dielectrics (dielectric constant larger than that of SiO_2, 3.9)is a solution to the challenge. In MOSFET technology, SiO_2 was replaced by a hafnium-based high-*k* material in 2007 [2].When the high-*k* material is used, a smaller equivalent oxide thickness (EOT) is obtained compared to SiO_2 gate dielectric with same physical thickness [3].In other words, the gate dielectrics with small EOT can be obtained without the expense of an increase of the leakage current by the employment of high-*k* material. Therefore, a number of high-*k* materials, HfO_2, ZrO_2, Y_2O_3 and their silicates, have been widely researched [4,5]. Among various high-*k* candidates, ZrO_2 has attracted a great amount of attention due to its relatively large dielectric constant (*k*~25) and relatively wide band gap (~5.0 eV) [6, 7].However, the significant concentrations of defects in high-*k* dielectrics have been proved to result in the instability of devices, such as flat-band voltage shift. In order to characterize these defects comprehensively, a number of techniques have been proposed to investigate the reliability, degradation, device lifetime, defect loss, electron trapping and de-trapping, interface states etc. [8-12]. One of the popular techniques, termed as pulse capacitance-voltage (CV) technique, is able to characterize the dielectric thin films in several hundred micro seconds. Due to the fast characterization speed of the pulse CV technique, less de-trapping process occurs before accomplishment of the measurement. Therefore, more traps are extracted compared with

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conventional methods, e.g., measured by Agilent 4284A LCR meter. However, an anomalous behavior in CV curves characterized via pulse CV techniques has drawn significant attention, when applied to metal gate MOS devices [13, 14, 15].When analyzing the MOS devices with ZrO_2 gate dielectrics, the relative positions of up and down traces measured by a pulse CV technique are opposite to those observed using a conventional CV measurement (by LCR meter) and this phenomenon cannot be consistently explained by trapping and de-trapping of the charges. One possible hypothesis relating to interfacial dipoles, that successfully explains most of abnormal features in the experiment, has been proposed afterwards [14]. Nevertheless, the effects of deposition and annealing conditions on the abnormal CV behavior are seldom explored and reported.

In this work, ZrO_2 gate dielectrics deposited under various temperatures and annealed in different conditions were researched. The interface dipoles, which present at the ZrO_2/SiO_x interface, were found to be sensitive to the deposition and annealing conditions. An interesting correlation between deposition as well as annealing temperature and CV curves shift, which provides a reference for the properties of the high-*k* thin films characterized by pulse technique, will be discussed in the paper.

EXPERIMENTAL DETAILS

N-type silicon wafers with resistivity of 1-10 Ω cm, cleaned using the Radio Corporation of America cleaning procedure, were used as the substrates. After cleaning, zirconium oxide thin films were deposited at 150 °C, 200 °C, and 250 °C using 150 ALD cycles of $Zr(NMe_2)_4$ and water vapor. The temperature for zirconium precursor was 130°Cand the 50 °C deionized water (DI water) was served as the oxygen source. The aluminum gate electrodes with a diameter of 0.3 mm and thickness of 500 nm were deposited by E-beam evaporation. The backside was deposited with aluminum as well after the treatment of a diluted HF solution to form ohmic back contact. Each sample was cut into three pieces, of which two were annealed in nitrogen and forming gas (FG) ambient, respectively, for 30 minutes at 350 °C. The pieces were labeled as "as-deposited", "N_2", and "FG" samples, respectively. The conventional and pulse CV characteristics were investigated using an Agilent 4284A precision LCR meter and a developed pulse CV system. All of the electrical measurements were performed in the dark, at room temperature with a Faraday Cage surrounding the wafer prober.

RESULTS AND DISCUSSIONS

The pulse CV measurement system was developed and implemented to probe the MOS capacitor sample and its system structure chart is shown in Fig.1. The MOS capacitor can be modeled as a resistor (high resistance) connected with a capacitor in parallel as shown in the inset of Fig.1.The current flowing through the capacitor and resistor were i_C and i_R, respectively. A function generator was used to input a pulse voltage (v_g)for the sample and the signal was monitored by channel one(v_{CH1}) of an oscilloscope. The related current through the sample (i_{total}) was amplified by a current amplifier and then monitor by channel two (v_{CH2}). The detailed working principle and the approach to the CV characteristics have been discussed in our previous research output [3].

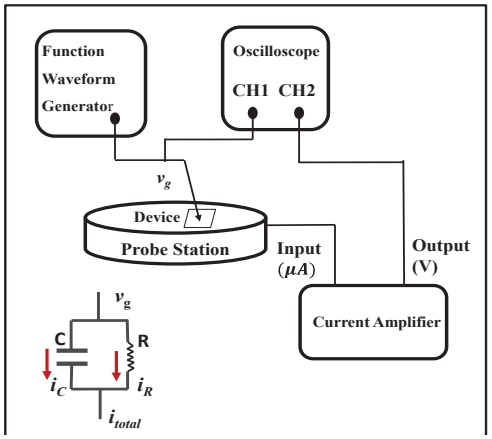

FIGURE 1. Pulse capacitance-voltage (CV) measurement system structure chart.

Before the characterization of MOS devices with high-*k* dielectrics, a SiO_2 MOS sample was used to test the reliability of the system. Figure 2(a) showed the original Voltage-Time (VT) data from both channel one and channel two of the oscilloscope. The pulse CV characteristic given in Fig.2 (b) was calculated using the following formula based on the VT data in Fig.2 (a) [3].

$$v_{\mathrm{CH2}} = A \cdot C \cdot \frac{dv_g}{dt} + A \cdot \frac{v_g}{R}$$

In addition, a conventional CV test was employed to compare with the new pulse CV technique. From Fig.2 (b), there was no clear shift for both pulse and conventional CV test. This is due to that there were no significant traps located in the oxide layer of the thermal SiO_2 MOS system. Furthermore, the pulse CV and conventional CV results matched consistently vertically. Therefore, it can be concluded that the pulse CV system was suitable for MOS capacitance measurement.

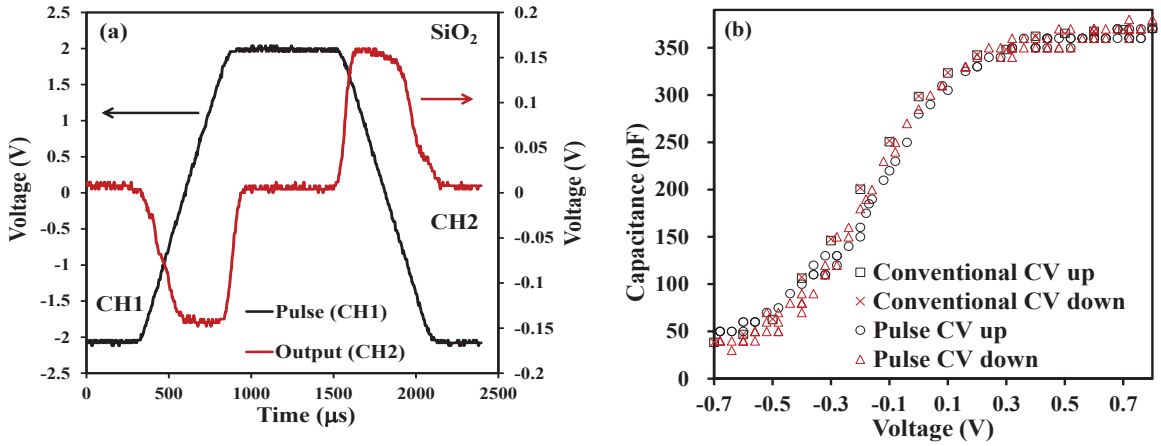

FIGURE 2. (a)Voltage (V) *versus* time (μs) and (b) Capacitance (pF) *versus* voltage (V) for the SiO_2 MOS sample.

The CV traces of the as-deposited sample with the ZrO_2 dielectric deposited at 200 °C measured by the Agilent 4284A (labeled as conventional CV) and the developed pulse CV system (labeled as pulse CV)were shown in Fig.3. From the comparison of the CV curves measured by the pulse technique and the conventional method, a distinct difference was observed. The down trace of CV characteristics was positively shifted with reference to the up one extracted from conventional method, while the shift became negative in the results from the pulse technique. For convenience in the following discussion, the positive shifts of down traces with respect to the up one was defined as the positive loop width, otherwise, it was defined as negative loop width. With regard to the hysteresis observed in the conventional CV curves, it was attributed to trapping and de-trapping of charges in the oxide [12]. However, the opposite shift directions of the CV curves in conventional and pulse technique cannot be consistently explained by the trapping/de-trapping of the charges. In order to explain this anomalous behavior, a model relating to the response of interface dipoles was proposed as shown in Fig.4.With regard to the formation of the dipoles, it was discussed by Kita et al [13].The orientation of the dipoles was randomly directed. d_2 and d_3 with angles of α and β, respectively, were half of the dipole separations for up and down pulse CV measurement. The effect of the dipoles on the positions of CV traces was divided into two parts, perpendicular to the interface and parallel to the interface, and only the part perpendicular to the interface accounted for the loop width. In the conventional measurement, the dipoles exactly followed the change of the oxide field induced by the DC bias and no significant change in dipole separation occurred. In addition, the conventional CV was only used as the reference position, so the direction of the dipoles in HFCV was not considered and d_1 was the distance of the dipole further from the high-*k*/SiO_x surface. However, in the pulse CV measurement (sweeping from negative to positive), the electric field across the capacitor stretched the dipoles at the negative bias. Then, when a fast voltage pulse swept from negative to positive, the dipole separation remained unchanged due to the lag in dipole response. Consequently, a positive shift of the up trace was observed, because the negative ends of the dipoles were closer to and the positive ends ($d_2\cos\alpha$) were further from the Si/SiO_x interface compared with the case (d_1) in the conventional measurement. A similar mechanism was operative when the pulse voltage swept from positive to negative and a negative shift of the down trace was observed consequently ($d_3\cos\beta < d_2$).

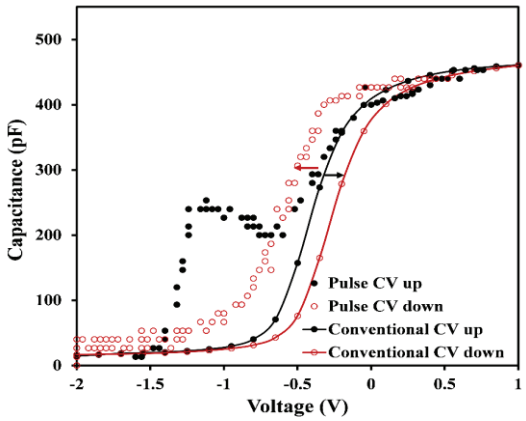

FIGURE 3. CV characteristics for an as-deposited ZrO_2 film deposited at 200 °C measured by an Agilent 4284A LCR meter and a pulse CV system. The applied peak-to-peak voltages were 3 V for both pulse and conventional method. In pulse measurement, the rising edge was 400 μs and a pulse width of 800 μs was used to minimize the effect of charge trapping.

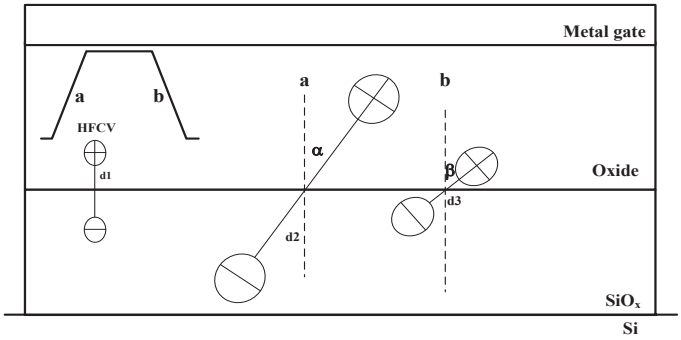

FIGURE 4. The separation of interface dipoles for the as-deposited sample during conventional measurement, under pulse voltage sweepingfrom negative to positive and from positive to negative.

From the above discussion, it was clear that an anomalous CV behavior attributed to the response of interface dipoles was observed for as-deposited samples when the pulse CV measurement was implemented. With respect to the samples annealed in FG ambient for 30 minutes at 350 °C, the CV behavior was illustrated in **Error! Reference source not found.** (a). The sample annealed in nitrogen ambient showed the similar CV behavior (not shown here).There was a zero loop width measured with a pulse width of 800 μs and an applied VPP of 3 V for both samples. In addition, the up traces extracted from both samples using the pulse CV technique were identical with those extracted from the conventional measurements (not shown in the figures). However, under the same measurement conditions, the as-deposited one showed a negative loop width. From these results, it seemed that the abnormal CV behavior was observed to be suppressed after either FG or N_2 annealing. This behavior may be due to suppression of the pulse-voltage-induced change of dipole separation, which contributed to the shift of the CV curves. However, a positive shift of down trace with the increase of pulse width (pulse width 10000 μs) was still observed. These changes of loop width were mainly attributed to captured electrons induced by the positive stress applied on the gate electrode. The longer the pulse width, the more charges were supplied into the traps from the substrate. This in turn led to more trapped charges and more positive shift of the down CV trace. Apart from the post-metal-annealing, the deposition temperature also impacted on the loop width of pulse CV traces for the MOS devices. Since the effect of interface dipoles was largely related to the annealing process rather than the ambient, only the loop width extracted from FG samples were demonstrated representatively to compare with those from as-deposited ones. From the changes of loop width for as-deposited samples, it was clear that loop width decreased with increasing of deposition temperature e.g. -0.2 V -0.15 V, and -0.125 V for 150 °C, 200 °C, and 250 °C, respectively. After annealing, the loop width became negligible for the samples deposited at 200 °C and 250 °C, while it still remained negative (-0.16 V) for the 150 °C sample, which implied that it was more difficult to suppress the effect of interface dipoles for thin films deposited at lower temperatures.

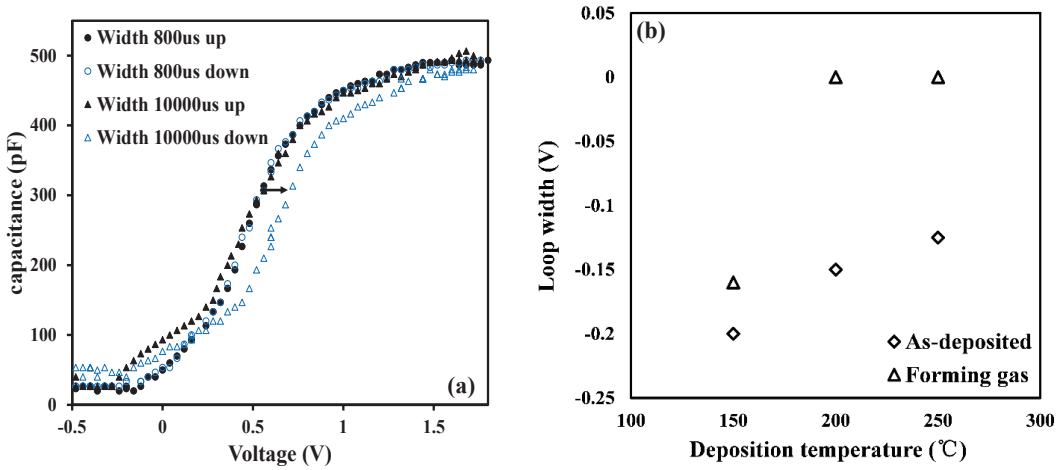

FIGURE 5. (a) Pulse CV characteristics of the samples annealed in forming gas ambient. The pulse technique was performed with various pulse times at a constant rising edge of 400 μs. (b) The comparison of loop width before and after annealing for the samples with various deposition temperatures. All the loop widths were extracted from the pulse CV curves with the rising edge of 400 μs and pulse width of 800 μs.

CONCLUSION

In this research, an anomalous CV characteristic was observed, in which the relative positions of up and down traces measured by pulse CV technique were opposite to those by conventional methods. The down trace of conventional CV curves was positively shifted with reference to the up trace, while the shift became negative for pulse CV curves. This unusual phenomenon cannot be inconsistently explained by charge trapping and de-trapping mechanism. Therefore, a hypothesis related with interface dipoles was proposed. In addition, the loop width, related to the interface dipoles, was highly dependent on the deposition temperature as well as post-metal-annealing process. The effect of dipoles was suppressed and the relative positions of CV characteristics measured by the pulse technique were consistent with those obtained by the conventional method when the samples were annealed in either FG or nitrogen ambient at 350°C for 30 minutes.

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