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Ultrasonic Additive Manufacturing using Feedstock with Build-in Circuitry for 3D Metal Embedded Electronics

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Abstract

Embedded electronics and sensors are becoming increasingly important for the development of Industry 4.0. For small components, space constraints lead to full 3D integration requirements that are only achievable through Additive Manufacturing. Manufacturing metal components usually require high temperatures incompatible with electronics but Ultrasonic Additive Manufacturing (UAM) can produce components with mechanical properties close to bulk, but with the integration of internal embedded electronics, sensors or optics. This paper describes a novel manufacturing route for embedding electronics with 3D via connectors in an aluminium matrix. Metal foils with printed conductors and insulators were prepared separately from the UAM process thereby separating the electronics preparation from the part consolidation. A dual material polymer layer exhibited the best electrically insulating properties, while providing mechanical protection of printed conductive tracks stable up to 100℃. General design and UAM process recommendations are given for 3D embedded electronics in a metal matrix.

1 Introduction

Embedded electronics and systems have developing into a multi-billion dollar industry over the past decade and is continuing to grow as more technologies become available [1]. For the automotive industry, 30% of the cost of a car is accounted for by embedded electronics [2] and the first satellite with 3D printed embedded electronics has been sent into orbit [3]. Furthermore, encapsulated sensors for high temperature environments [4] and medical instrumentation are being developed [5]. However, electronics manufacturing requires multiple highly specialized processing steps and is incompatible with most manufacturing processes of mechanical components. For this reason, electronic components are traditionally manufactured separately and subsequently bolted onto the component to form a product with both the functionality of the electronics and the mechanical part. Further integration of the electronic and structural part is, however, possible if the PCB is removed and the conductive tracks and electronic components are printed or placed directly on the structural material. This has led to the development of Additively Manufactured 3D

electronics in polymers [6,7], but due to the high processing temperatures it has so far not been possible to form 3D electronics in metal parts.

Ultrasonic additive manufacturing (UAM) is a hybrid sheet lamination manufacturing technology that enables the fabrication of metal parts through subsequent and repeated additive and subtractive steps [8]. In the UAM process, thin metal foils are bonded layer-by-layer during the ultrasonic metal welding (UMW) step, and the desired shape is given to the part by periodic CNC machining. During the bonding, a sonotrode is rolling over the foil stack while vibrating at a pre-set ultrasonic frequency and amplitude and applying pressure. The result is the formation of a solid state bond between the metal foils [9,10], but at temperatures less than 200℃ for aluminium alloys [11], which is well below the mel ting point of the metal, and is compatible with many polymers. Additionally, the heat dissipates quickly so the overall thermal load is low [12,13]. In the foil-foil interface the metal undergoes plastic metal flow during bonding, which enables composite metal matrix structures with embedded functionality such as optical fibres [14,15], shape memory alloy fibres [16,17], magnetostrictive and shape memory materials for embedded sensing applications [18] as well as smart switches for structural antennas [19]. The low UAM processing temperature has enabled embedding of printed conductive tracks [20] and thermal sensors [21] into CNC machined pockets of a UAM fabricated substrate. Screen printed electric insulators and conductive paths have also been partially embedded without the need for milled pockets [22–24].

In the conventional UAM process the metal foils are ultrasonically welded and then milled but a recently proposed “form-then-bond” approach suggests that the order of the welding and milling steps can be inverted [25]. It was shown that by using the “form-then-bond” approach it is possible to create cavities to encapsulate electronic components by stacking multiple foils with pre-milled features. In this study, we show that additional pre-treatments such as pocket formation and electronics printing can be applied to the foils to create structures with extra functionality. Additionally, a manufacturing method is presented for the fabrication of through-hole via for 3D embedded electronics as shown in Fig. 1. Printed electrical tracks are preferred over solid conductors as printed tracks can be shaped arbitrarily including bending in 3D. The study is divided in three stages: stage one demonstrates the feasibility of using pre-prepared foils with electrically insulating materials; stage two delves deeper into embedding strategies that have a minimal effect on the final resistance of the embedded printed conductive tracks; stage three investigates methods of creating structures with through-hole via for 3D integration of electronic components. Combined, this manufacturing process shows the building blocks needed for 3D electronics embedded in a metal matrix.

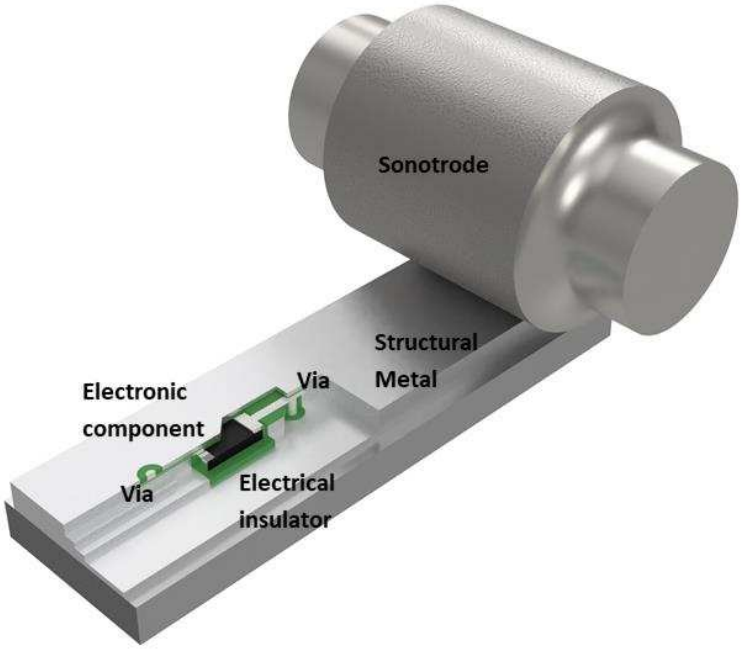

Fig. 1 Illustration of an electronic component (black) with conductive through-hole via and electrical insulators (green) embedded in the metal matrix by the Ultrasonic Welding Process.

2 Materials and methods

For the sample preparation the following steps were used: electrochemical etching of pockets in the aluminium foil, application of the insulating layer into the pockets, printing conductive tracks on the electrical insulator, placing electronic component onto a UAM fabricated aluminium substrate and encapsulation using ultrasonic welding of the pre-treated foils. As part of the investigation a range of different polymer insulators, layering strategies and welding strategies were tested as detailed below.

2.1 Electrochemical etching of aluminium foils

Indentations, 40 µm deep, in the 100 µm thick aluminium foils (Al 3003-H18) were created by masking the foils with a lacquer (MICCROShield, Tolber Chemical Division) and patterning a rectangle 4.8 mm wide and 50 mm long with a CO2 laser marker system (Synrad Inc., 10 W max. power, 10.6 µm wavelength) as illustrated in Fig. 2(a). The prepared foils were then electrochemically etched in an acid solution (66% wt. phosphoric acid, 15% wt. sulfuric acid, 3% wt. ethylene glycol, 16% wt. water) at 80℃ and a curren t density of 100 mA/cm^2 for 6 min. The foils were decreased prior to masking and between each processing step.

2.2 Application of insulating layers and dispensing conductive tracks

The etched trenches were filled manually with polymer insulator and levelled using a doctor blade (see Fig. 2(b)). Three electrically insulating polymer pastes were selected based on

their relative hardness and elasticity. The three insulating polymers were given an abbreviation TP (Gwent Electronic Materials Ltd., D2080121P12), TS1 (Creative Materials Inc., 104-38) and TS2 (Technic Inc., 520 Series), where TP and TS highlight the polymer is a thermoplastic or thermoset, respectively (Table 1). The polymers were cured according to the manufacturer recommendations (Table 1). The coating process was repeated twice for TP to accommodate for the shrinkage of the paste during curing.

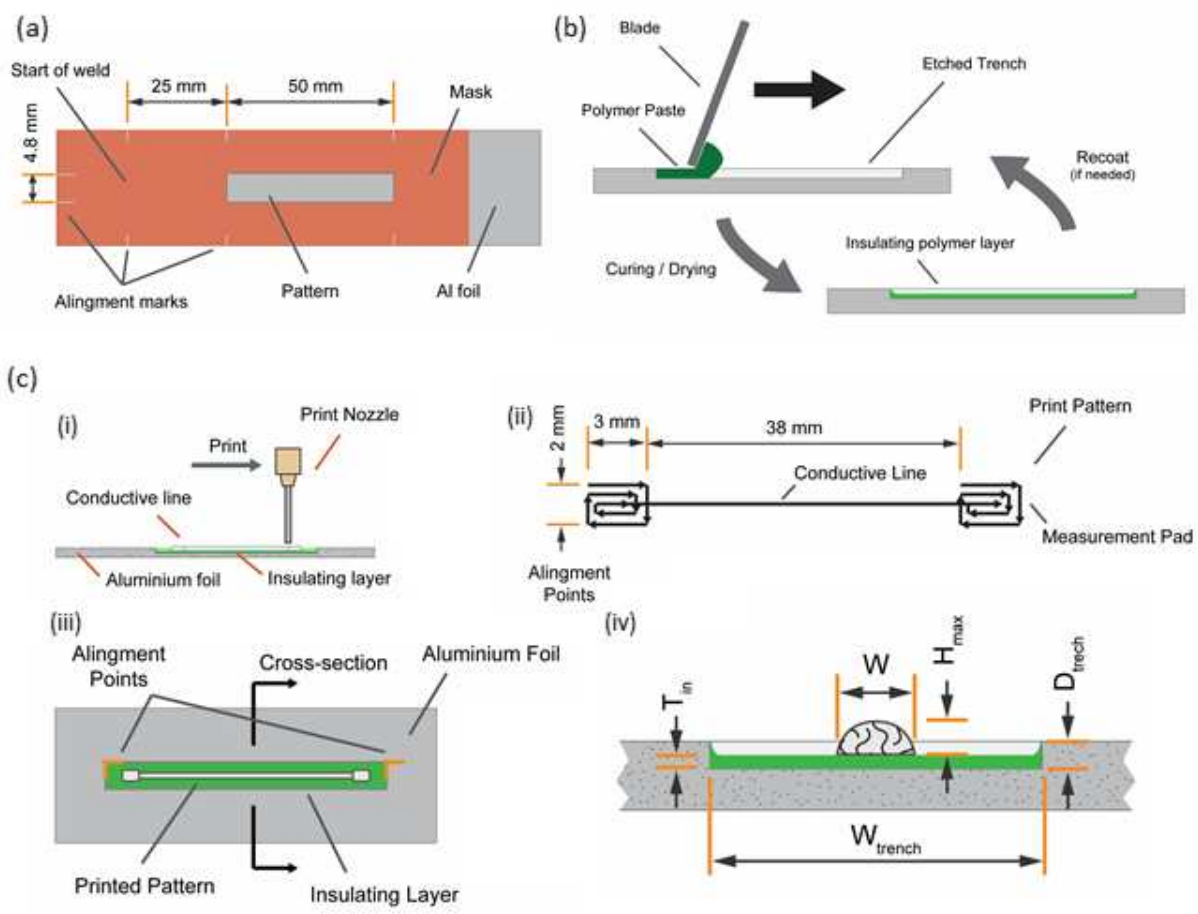

Fig. 2 (a) Mask pattern for electrochemical etching. (b) Doctor blade coating of polymer insulators in aluminium trench. Coating repeated one or more times with the same or different insulator. (c) The conductive paste printing (i) with print track (ii)sample positioning (iii) and cross-section with dimensions of interest (iv).

The conductive tracks were dispensed on the polymer insulator using a pneumatic Musashi Shotmaster 500 system (Musashi Engineering Inc., Japan, nozzle diameter 220 µm, pressure 175kPa, Speed 3 mm/s, print gap 90 µm, pitch 250 µm). The print pattern used for this stage of experimentation is shown in Fig. 2(c). The main conductor consists of a single conductive line (38 mm long) and two measurement pads. Multiple print passes were used to create the print pads. The material used for the conductive tracks was a silver based conductive paste Gwent C2110817D5 (code name Ag-TP). After syringe dispensing, the tracks were cured in a box oven at 150℃ for 30 minutes.

Table 1 Material properties and post processing of the three electrically insulating polymers.

	TP	TS1	TS2
Manufacturer	Gwent Electronic Materials Ltd.	Creative Materials Inc.	Technic Inc.
Product Code	D2080121P12	104-38	520 Series
Type	1-part thermoplastic	1-part thermoset	2-part thermoset
Colour	White	Clear	Green
Viscosity	9-14 Pas [2]	N/A	N/A
Solids Content	47-48 %	N/A	N/A
Volume Resistivity	N/A	$1 \cdot 10^{11}$ *Ωcm*	$2.6 \cdot 10^{16}$ *Ωcm*
Dielectric Constant	N/A	3.9 @ 60 Hz	4.00 @ 50 Hz
Curing Conditions	150°C for 15 min in box oven	120°C for 10 min in box oven	150°C for 45 min in box oven

2.3 Dual-material polymer insulator

Etched aluminium trenches were filled with the base insulating material (i.e. either 3 coatings of TP or 1 coating of TS2) using a doctor blade and cured in a box oven at 150℃ for 15 -45 min. Then, the foil preparation was concluded following two alternative approaches. In the first approach (“coat-then-print”, Fig. 3(a)), a layer of TS1 was first deposited, and then a conductive pathway was dispensed onto the cured TS1 over-coating layer and thermally cured at 150 ℃ for 30 min. The second approach (“print-then-coat”, Fig. 3(b)) involved the dispensing of the conductive pathway directly onto the TP or TS2 sub-layer and, after the conductive track was cured in the oven, the coating of the whole structure with a layer of TS1 using a doctor blade. The printed tracks were encapsulated using the “face-up” approach described in next section. Resistance measurements were taken before and after UAM welding. Three samples were prepared for each material and each coating approach, resulting in 12 samples in total.

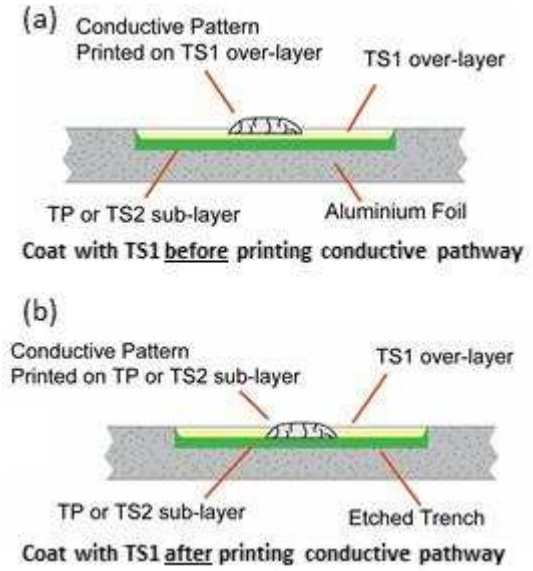

Fig. 3 *Illustration of the "coat*-then-*print" (a) and "print*-then-*coat" (b) manufacturing* approaches.

2.4 Encapsulation of conductive tracks and weld orientation

Foils prepared with either conductive tracks and insulating polymer or just insulating polymer were prepared (step 1, Fig. 4) before ultrasonically welding the first foil to the aluminium substrate (step 2, Fig. 4). Subsequently, the second foil was manually aligned to the first foil using alignment marks and ultrasonically welded (step 3, Fig. 4). The order of welding the two foils was investigated, as it would result in the conductive track either "face-up" towards the sonotrode or "face-down" away from the sonotrode. In both cases three samples were fabricated. The top layer was subsequently removed using a sharp blade to take resistance measurements. In all experiments the aluminium foils and base plate were mechanically clamped to the anvil at one end. The UAM process parameters used for all UAM bonding were Amplitude = 18 µm, Force = 1600 N, Speed = 30 mm/s, T = room temp.).

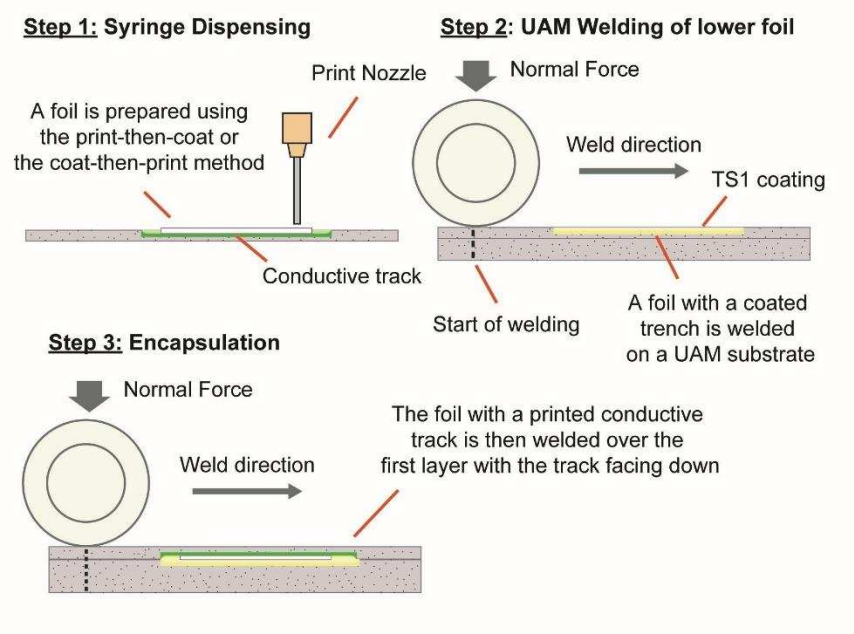

Fig. 4 The UAM welding process for encapsulation.

2.5 Through-hole via

Samples were prepared with the TP & TS1 material combination and both through-hole via in the top foil and substrate were examined. The mating foils were coated with two layers of TS1, similarly to the previous experimental stage. The two alternative sample preparation approaches are described in detail below. Three samples were prepared this way using each method.

For the via in the top foil approach, shown in Fig. 5 (a), the foil with the conductive track was ultrasonically welded onto a UAM fabricated substrate. Then a mating foil with two pre-drilled via and coated with insulating material was placed on top of the previous layer, aligned and welded, encapsulating the conductive track. The via on the mating foil was prepared using the following steps: first, two layers of TS1 were dispensed in the etched trench and cured. Then two through holes of diameter ⌀ 2.0 mm were manually drilled, using progressively larger diameter drill bits (⌀ 0.8, 1.2, 1.6 and 2.0 mm). Then, the sidewalls of the holes were manually coated with two layers of TS1 insulating material by applying a small quantity of material with a doctor blade. Finally, an opening was drilled on the coated via using a ⌀ 0.8 mm drill bit.

A similar methodology was used to prepare the samples using the via in substrate approach (Fig. 5 (b)), where the mating foil was first welded onto a UAM fabricated substrate. Then through-holes with nominal diameter ⌀ 2 mm were drilled on the centre axis of the coated trench, using progressively larger drill bits as before. In order to avoid the creation of

protruding features, a chamfer was added to the holes using a ⌀ 2.8 mm drill bit. Finally, the holes were coated with three layers of TP and one layer of TS1, cured and an opening was drilled using a ⌀ 0.8 mm drill bit. A dual insulating material coating was used for the via on the substrate as it provided with a more reliable insulating coating. Aluminium foils with printed conductive tracks were prepared using the print-then-coat method and the TP & TS1 material combination, as described previously. The mating foils were coated with TS1 and the samples were prepared using the both the face-up and the face-down approaches.

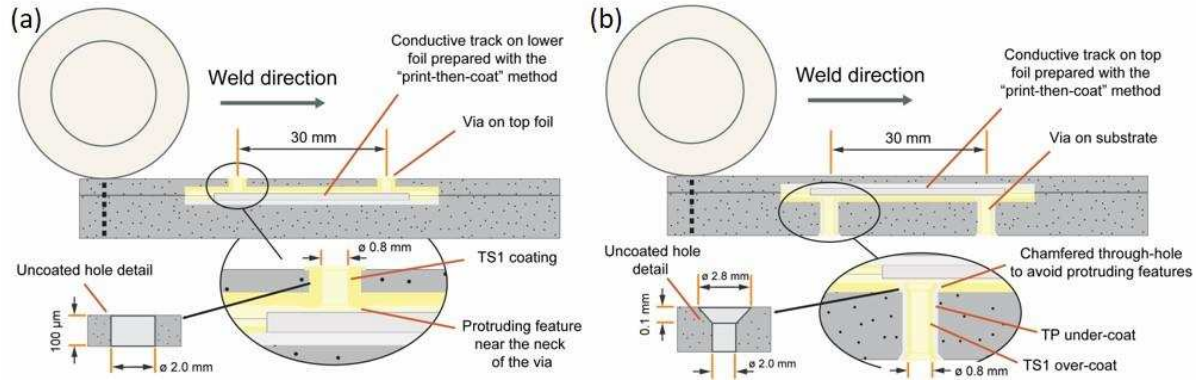

Fig. 5 Encapsulation process with via on the top foil (a) and encapsulation process with via on the substrate (b).

2.6 Thermal stability

The behaviour of a sample prepared using the face-down approach was examined at elevated temperatures. The resistance of the embedded conductive track was first measured at room temperature using the Fluke multimeter. Then the temperature of the sample was increased by placing it on a preheated hot plate (IKA C-MAG HS7). The initial temperature of the hotplate was 50℃ and it was increased every 5 minutes by 10℃ until the sample failed. Every 5 minutes the resistance of the track was measured, and the sample was examined for shorting, by measuring the resistance between the track and the aluminium matrix, and any other modes of failure. The temperature of the hotplate was controlled by an integrated thermocouple (IKA ETS DS thermocouple) and the temperature of the sample was verified using an external K-type thermocouple.

2.7 Embedded SMT resistor

For the embedding of the resistor, the face-down approach was followed as illustrated in Fig. 6. A surface mount technology (SMT) resistor (TE Connectivity CRG1206 series, nominal dimensions 3.1 x 1.65 x 0.55 mm) was placed on the top foil and was welded face-down over a coated substrate with a milled pocket. The following process was used to prepare the top layer: first, foils with etched trench were coated with three layers of TP insulator and

cured. Two conductive tracks were then dispensed along the centre axis of the trench. A gap of 2 mm was left between the two tracks. While the tracks were still wet, the SMT resistor was placed on this gap and it was kept in place when the conductive adhesive was solidified during thermal curing. Finally, the whole structure (i.e. the conductive track and the resistor) was coated with a layer of TS1 and then its resistance was recorded using both the Keithley 2425 tabletop multimeter and the Fluke 177 handheld multimeter. The lower layer was prepared by first welding an etched and coated with TS1 aluminium foil onto a UAM fabricated substrate. Then a pocket (nominal dimensions of 6.2 mm by 3.8 mm and 1.0 mm depth) was manually milled onto the substrate using a ⌀1.5 mm ball-end cutting tool. The pocket was then coated with three layers of TP and one layer of TS1 insulator. Two via were added to the substrate using the method described in the previous section.

After testing the coated pocket for shorting (the vertical edges of the pockets were critical locations for the creation of short circuits), the top layer was placed on the substrate, aligned and UAM welded. The resistance of the embedded structure was then measured using a Fluke 177 handheld multimeter. Two additional aluminium foils were then UAM welded onto the substrate, to examine the effect of welding additional layers, and the resistance of the structure was then measured again.

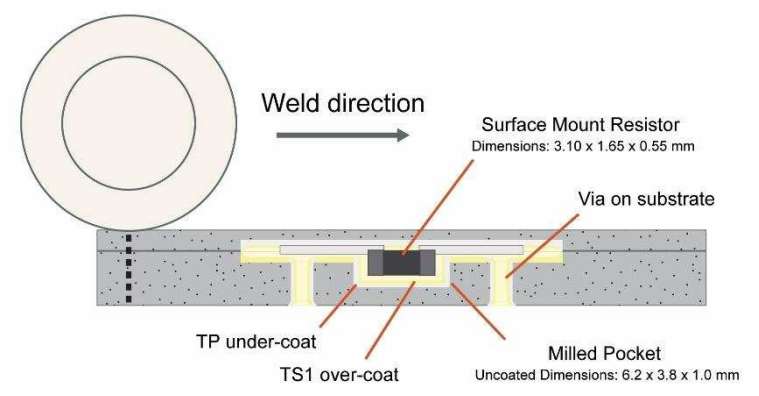

Fig. 6 Encapsulation process for embedding the SMT resistor.

2.8 Characterisation

Resistance measurements were taken before and after encapsulation using the Keithley 2425 tabletop multimeter and handheld 4-point probes. Profile line scans were taken using a stylus based Talysurf CLI system.

3 Results and discussion

3.1 Dual layer polymer insulator

Initial experiments on the three electrically insulating polymers TP, TS1 and TS2 (see supplementary information) showed that TS1 excels in the areas that TP and TS2 perform poorly and underperforms in the areas that TP and TS2 perform well. For example, TS1 is excellent at protecting the conductive tracks mechanically but provides a poor printing surface and a poor electrical insulation. In contrast TP and TS2 provide a good printing surface and electrical insulation but does not protect the conductive tracks well during UAM processing. For this reason, the possibility of combining different insulating materials with overall improved characteristics was examined.

For the dual layer polymer insulator either TP or TS2 were used as a reliable electrically insulating layer and the elastic TS1 was used on top of these to protect the conductive tracks from the UAM process. Two approaches were used; “coat-then-print” where both the insulating polymer layers were applied before the conductive tracks were printed, and “print-then-coat” where the second layer of insulating polymer was applied after the conductive track was printed Fig. 3).

The insulating coating of all samples prepared for this experimental stage survived the UAM welding process without any evidence of failure, confirming the hypothesis that the TS1 coating will act as a protective layer to the TP sub-layer (see Table 2). Also, no shorting was observed between the conductive tracks and the aluminium matrix, during either the UAM welding of the lower foil or the encapsulation step. An example of a prepared “printed-then-coated” foil before and after UAM welding is presented in Fig. 7. The printed tracks retained their original shape during the welding step, but traces of the conductive and insulating material were transferred onto the sonotrode during treatment.

Table 2 Summary of resistance response of conductive tracks prepared with different coating methods. The errors represent the Standard Deviation.

Material Combination	**Coating Method**	**Initial Resistance R_i [Ω]**	**Resistance after Welding R_w [Ω]**	**Relative increase R_w/R_i**
TS2 & TS1	Coat-then-print	3.203 ± 0.021	108.96 ± 4.73	34
TP & TS1	Coat-then-print	2.857 ± 0.021	20.45 ± 0.73	7.15
TS2 & TS1	Print-then-coat	0.693 ± 0.002	54.21 ± 0.44	78
TP & TS1	Print-then-coat	0.802 ± 0.017	4.182 ± 0.145	5.22

It was expected from the initial results, that the conductive tracks printed on the TS1 material would exhibit a higher resistance than the tracks printed onto TP or TS2 and then coated.

Indeed, the as-printed resistance of the tracks fabricated using the “print-then-coat” approach was three to five times lower than the resistance of the tracks produced with the “coat-then-print” approach. Also, the initial resistance of the tracks printed on TS2 and TP using the same coating approach were comparable.

After welding, the resistance of the tracks treated using the “print-then-coat” approach was also two to five times lower than the resistance of the tracks fabricated using the “coat-then-print” approach, for the same insulator combination. These observations suggest the following two conclusions: i) the TS1 coating acts as a protective layer for the conductive tracks prepared with the “print-the-coat” approach and ii) the different response of the conductive tracks is caused by the different material properties of TP and TS2. These two points are discussed below.

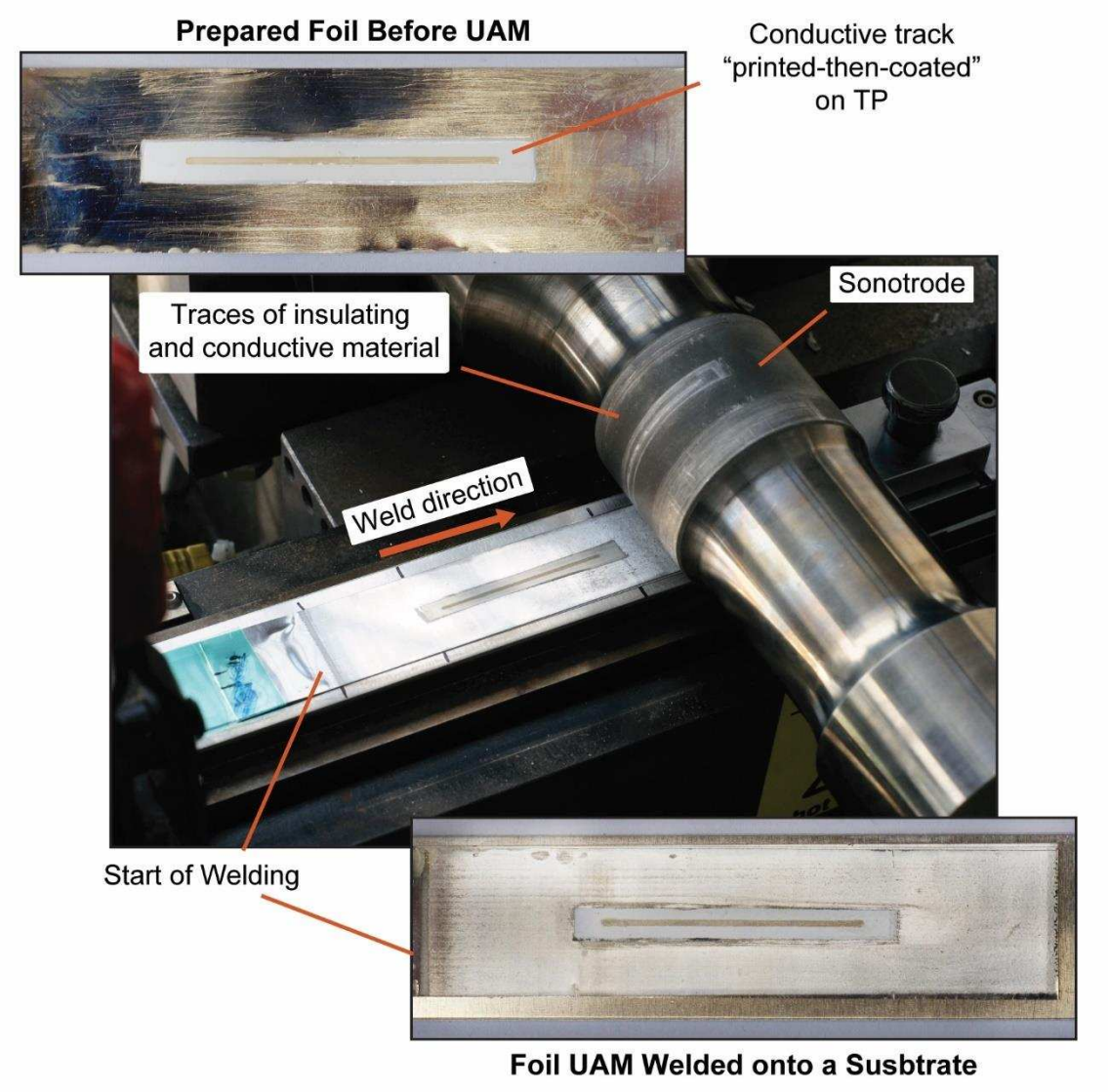

Fig. 7 Example of UAM welding of a foil coated with TP+TS1 and using the print-then-coat approach.

3.1.1 Polymer protective layer for conductive tracks

The way that the TS1 layer acts as a protective layer for the conductive track is shown in Fig. 8. Line scans were taken of a sample prepared using the “print-then-coat” approach during three different steps of the fabrication process: after the deposition and curing of the conductive track, after the application of the TS1 coating layer and after UAM welding. The top of the as-printed printed conductive track protrudes approx. 5-10 μm above the top surface of the foil. After UAM welding though, the top surface of the aluminium foil, the insulating coating and the top of the conductive track are almost level. This suggests that sonotrode came in direct contract with the top of the conductive track (this is also confirmed by the traces of insulating and conductive material observed on the surface of the sonotrode presented in Fig. 7). The surface of the aluminium foil and the conductive track appear considerably rougher compared to their untreated state. The surface of the insulating layer though appeared mostly unaltered, suggesting that the TS1 coating deformed elastically and returned to its original shape after the load has been removed. The work absorbed by TS1 has reduced the total ultrasonic energy input in the conductive track and has partially attenuated the ultrasonic oscillations. Also, since a portion of the conductive track is encapsulated under the top layer of the TS1 coating, it did not come in direct contact with the sonotrode, and it was less affected by the ultrasonic energy and rolling of the sonotrode. The TS1 over-coat protected in a similar way the TP under-layer also and prevented the cracking of the insulating layer.

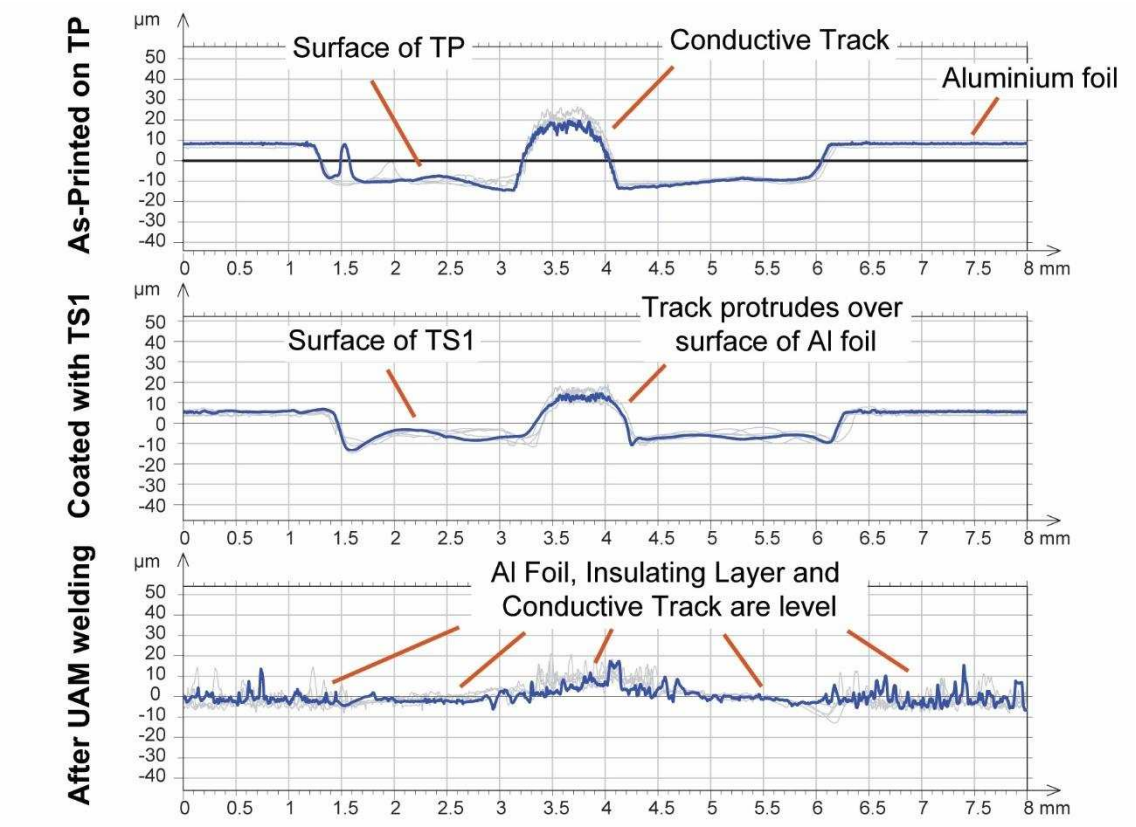

Fig. 8 Surface morphology of a typical sample prepared with the print-then-coat approach during the different sample preparation steps.

3.1.2 The effect of polymer choice on conductive track resistance increase

After UAM encapsulation the samples prepared with TS2 resulted in a much larger resistivity increase than the ones prepared with TS1 as shown previously. The difference could either be due to mechanical deformation or ultrasound degradation. The top view and a micrograph of a cross-section along the width of representative welded samples of both material combinations are presented in Fig. 9. The tracks printed on either TP or TS2 do not differ substantially in dimensions after the UAM welding step. In fact, the measured average width of the tracks was almost identical, while the average height of the tracks after welding printed on TS2 was 2 µm larger on average than the height of the tracks printed on TP (measurements were taken by examining three cross-sections of representative samples). For this reason, the dimensions of the tracks were not the cause of the observed large difference in the relative resistance increase of the samples printed on TP or TS2.

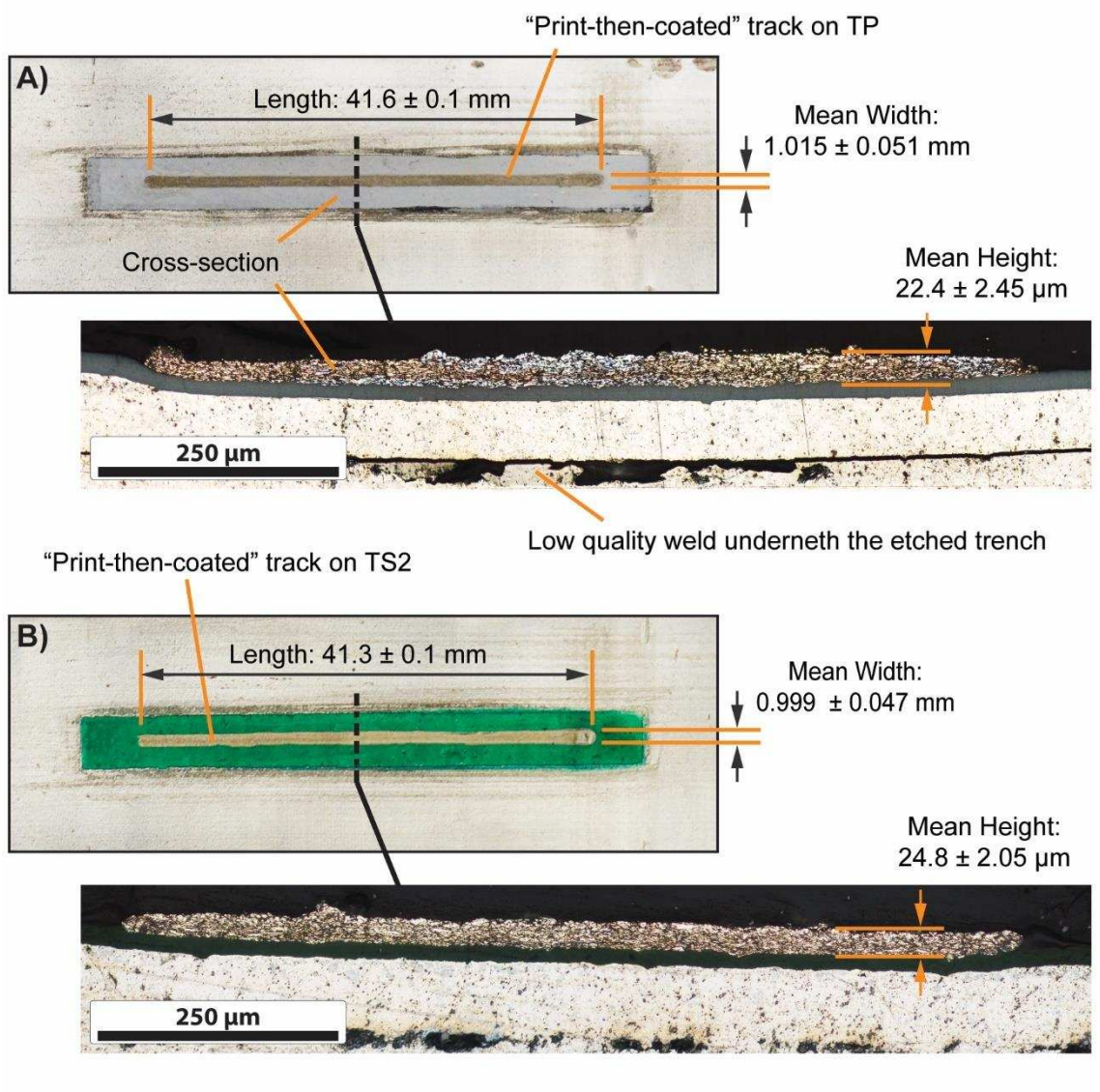

Fig. 9 Top view and cross-section of typical samples prepared with the print-then-coat approach and with A) TP & TS1 material combination and B) TS2 & TS1 material combination.

The difference in the relative resistance increase was instead attributed to the different physical properties of the two insulating materials TP and TS2. We have previously shown that the total ultrasonic energy input in the conductive material increases the resistivity of the printed tracks after welding almost linearly [16]. Changes in the absorbed energy can therefor affect the increase in electrical resistance after UAM. When the ultrasonic wave reaches the boundary between the conductive track and the insulating polymer, part of the energy is absorbed depending on the acoustic properties of the polymer. Qualitatively, TS2 has a much lower hardness than TP and thus is expected to have a lower modulus of elasticity. This indicates, that the ultrasonic wave may travel through these materials with a different velocity. Thus, the percentage of the ultrasonic energy that is absorbed in the interface of the conductive material and the insulator may vary between TP and TS2. As a

result, the conductive track is exposed to a higher ultrasonic energy for one of the insulating polymers, and thus its resistivity increases by a larger amount.

3.2 Encapsulation of conductive tracks and weld orientation

To determine the optimal process for the encapsulation of conductive tracks, two approaches were examined: 1) the conductive track “face-up” towards the sonotrode during welding or 2) “face-down” away from the sonotrode. The electrical resistance was measured for each process step and the results are summarized in Table 5.

Table 3 Summary of resistance measurements of samples encapsulated with the face-up and face-down approaches. The errors represent the Standard Deviation.

	Initial Resistance R_i [Ω]	**Resistance after Welding R_w [Ω]**	**Resistance after Encapsulation R_e [Ω]**
Welded face-up	0.802 ± 0.020	4.182 ± 0.145	4.408 ± 0.020
Welded face-down	0.725 ± 0.015	N/A	0.837 ± 0.010

The samples prepared using the “face-down” approach exhibited resistance increase of only 15%, while the resistance of the sample welded “face-up” was approx. 5 times higher compared to their initial value, (only 5% of this increase was caused during the encapsulation process though.) The main cause of the electrical resistance of the conductive tracks is therefore the direct exposure to the ultrasonic energy/sonotrode and not from the elongation of the foil.

A representative sample for each case was sectioned along its width and viewed under the optical microscope. Dark field micrographs of the area near the conductive track are presented in Fig. 10. The micrographs illustrate the flow of the TS1 material around the conductive track. In both cases, the TS1 layer was deformed around the track during loading. This deformation partially absorbed the ultrasonic energy, protecting the tracks and preventing the degradation of their electrical conductivity.

From the micrographs, the cross-sectional area and dimensions of the encapsulated tracks were measured. It was observed the encapsulation did not alter the dimensions of the tracks. Thus, the resistivity of the tracks after encapsulation was calculated to be 292.5 ± 28.2 x 10^{-5}·Ωcm and 60.9 ± 5.4 x 10^{-5}·Ωcm for the “face-up” and “face-down” samples respectively. This shows that there was only minimal increase of resistivity of the conductive tracks encapsulated “face-down” (less than 1%), demonstrating the superiority of this embedding method. (The conductive paste supplier states an ideal volume resistivity of 7.5 x 10^{-5}·Ωcm but we were not able to achieve this even before welding).

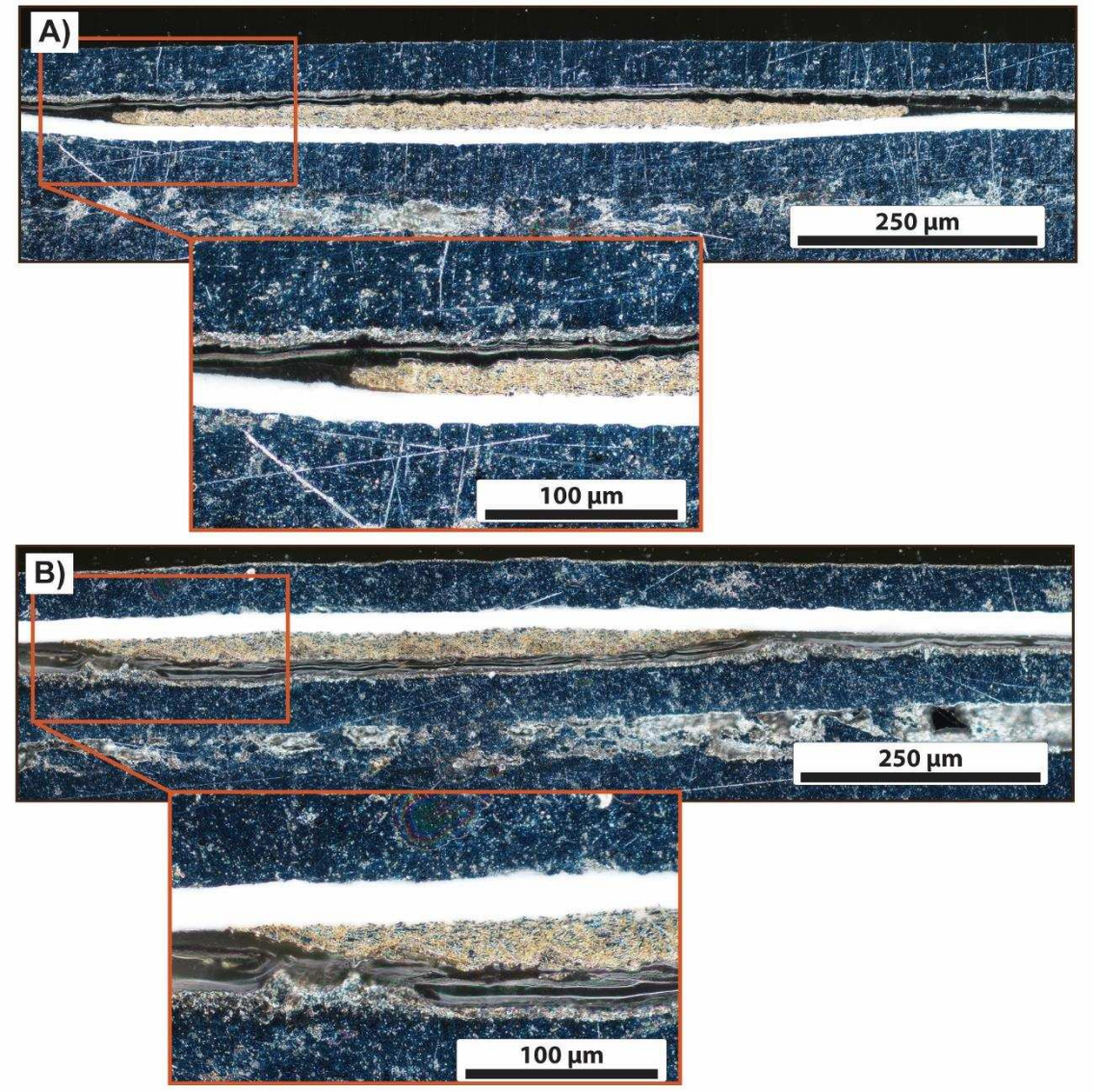

Fig. 10 Cross-sectional view (in dark field) along the width of typical encapsulated conductive tracks prepared with the A) face-up approach and B) the face-down approach.

3.3 Through-hole Via

Vertical via enables the creation of 3D structures and the interconnection between the embedded circuitry with their environment. The resistance of the embedded tracks was measured before and after encapsulation. The initial resistance of the “as-printed” tracks, their resistance after welding (for the “face-up” approach) and their resistance after encapsulation are presented in Table 4. All tracks were embedded successfully without any sign of shorting.

The tracks embedded using the “face-up” approach (i.e. the samples with via on the top foil) exhibited a significant increase in resistance during the encapsulation step compared to the tracks that were embedded “face-up” but did not have a via. The resistance of the former was tripled during the encapsulation step, while the resistance of the later was almost

unchanged. On the other hand, the final resistance of the tracks that were welded face-down (i.e. the samples that had the via on the substrate) increased only marginally and was almost identical to the resistance of the tracks prepared with the same approach but with no via.

Table 4 Summary of resistance measurements of samples with via during encapsulation. The errors represent the Standard Deviation.

	Initial Resistance R_i [Ω]	**Resistance after Welding R_w [Ω]**	**Resistance after Encapsulation R_e [Ω]**
Via on top foil	0.746 ± 0.021	4.721 ± 0.096	12.47 ± 3.42
Via on substrate	0.769 ± 0.015	N/A	0.87 ± 0.19

The observed increase in resistance of the tracks embedded “face-up” was thought to be a result of the direct contact of the sonotrode with the exposed areas of the conductive tracks near the via, and not due to deformation during encapsulation. This was tested by subjecting an already welded face-up sample to a second run of the UAM treatment by running the sonotrode over the track for a second time, using the same processing parameters. This yielded a fivefold increase to its resistance (from approx. 4.5 Ω to 25 Ω), confirming the hypothesis. A cross-sectional view of an encapsulated via shows that material moving during the UAM process can form potential point failures Fig. 11.

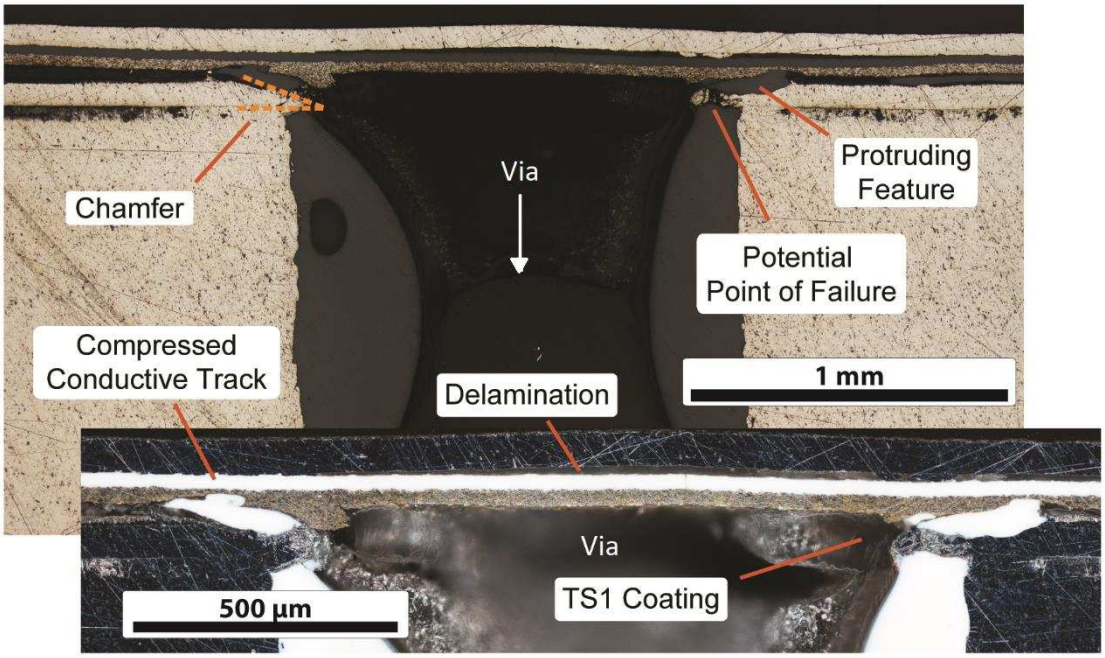

Fig. 11 Cross-sectional view (bright field and dark field) along the length of a typical sample with via on the substrate.

3.4 Temperature Stability

The temperature stability of the embedded conductive tracks was tested up to 120 ℃ by slowly raising the temperature and periodically measuring the resistance. In Fig. 12 the measured electrical resistance as a function of time and temperatures is shown.

The electrical resistance was relatively stable (less than 10% variation) up to 100 ℃ , whereas after that threshold it dropped abruptly and at 120 ℃, the sample shorted due to the softening of the polymer insulator.

The thermal stability indicate that the embedded tracks are functional even at elevated temperatures that meet the requirements of most applications. The embedded tracks can be used without any interference with the metal matrix at temperatures up to 60℃, and with some interference at temperatures up to 100℃ and limited exposure.

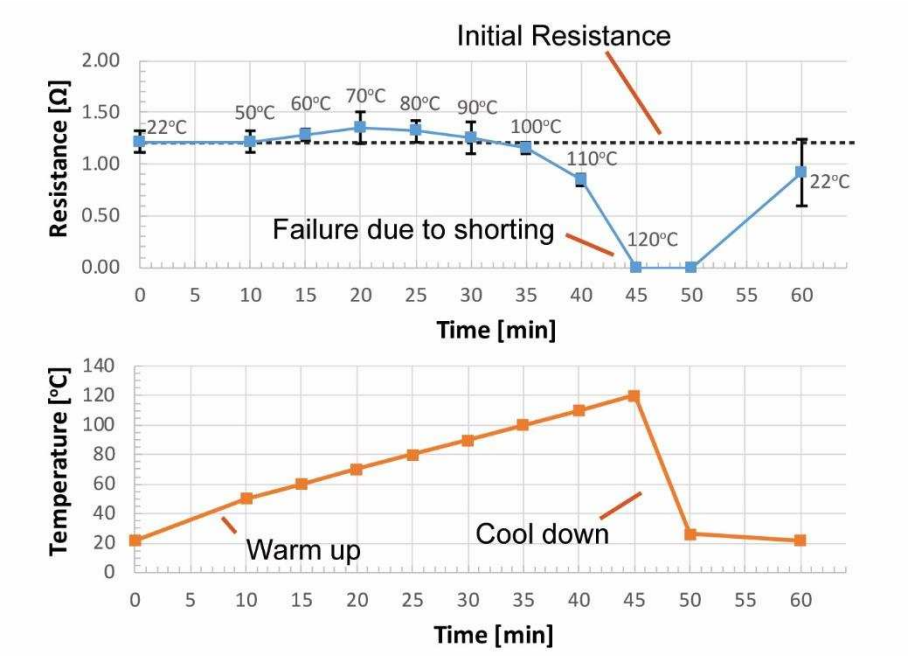

Fig. 12 Resistance response of embedded conductive track and the associated thermal load as a function of time.

3.5 3D Embedded Electronics

An SMT resistor was successfully embedded with 3D through via interconnects in the metal matrix by UAM welding. A cross-section of the embedded resistor is given in Fig. 13. A close-up of the resistor in higher magnification and in dark field is also given in the same figure.

The resistance of the electronic circuitry (i.e. the resistor placed on the printed conductive track) did not change during embedding: its initial resistance was 997.8 ± 0.1 Ω, while after encapsulation its resistance was 998.2 ± 0.6 Ω.

Two additional foils were then welded over the sample, to study the weld recovery. The welding of the additional layers did not affect the resistance of the embedded structure. The small gap between the SMT resistor and the substrate results in UAM welding over an unsupported area, which impedes the quality of welding on the subsequent layers, as can be seen in the micrograph in Fig. 13. Weld recovery can be improved by better manufacturing tolerances minimizing the gap between SMTs and substrate. In future developments further protection of the SMTs by polymer encasing may also be required to avoid components dislodging and improve reliability.

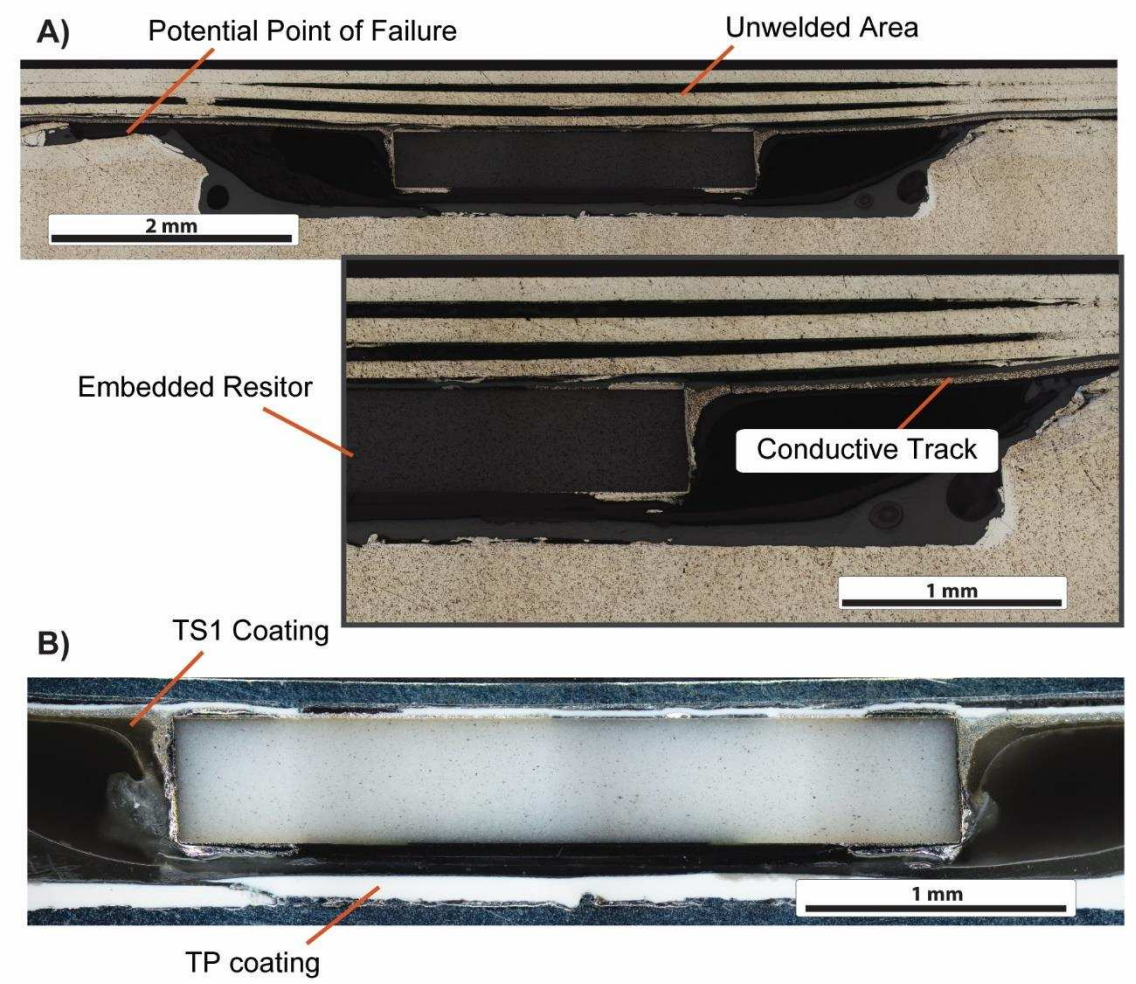

Fig. 13 Micrograph of a sample with a successfully embedded resistor, cross-sectioned along its length a) bright field micrograph b) dark field micrograph.

3.6 Design Recommendations

Following extensive experimental research on embedding printed electronics and SMTs in a metal matrix by UAM, several design and process recommendations can be reached.

1) The electrically insulating material must be soft to protect printed electronics during UAM, while providing reliable electrical insulation and a printable surface.

Alternatively, a dual layer combination of soft and hard electrical insulating materials can be used.

2) Both printed conducting and insulating materials must be cured/able to withstand similar temperatures.
3) The dimensions of the embedded cavities for conductive tracks and SMTs must be kept to a minimum to ensure good welds below the cavities and weld recovery above the cavities. When embedding multiple components, individual connected cavities are therefore preferable to one large cavity. No gaps can be present below the embedded SMTs and should be minimized around the SMTs to improve weld recovery.
4) Avoid sharp edges in close contact with printed electronics i.e. chamfer all vias.
5) During processing avoid contact between sonotrode and electronic elements such as printed conductive tracks and SMT components, as it can cause damage to the electronics.
6) The SMTs should be bonded well to the foils e.g. by a polymer to avoid component detachment.
7) Use the minimum ultrasonic power that creates a successful weld, as a high ultrasonic power degrades the printed conductors [24].
8) Use a foil alignment system for best cavity accuracy and edge definition [25].

4 Conclusion

Electronics fully embedded in a metal matrix has so far not been possible due to the high temperatures associated with manufacturing metal parts. Ultrasonic AM offers a low temperature alternative to metal manufacturing and previous initial studies have indicated that printed conductors, electrical insulators and electrical components are able to survive the ultrasonic AM process. This study investigated the requirements for extending the electronic integration into the 3rd dimension and the effect of material and processing choices. A dual layer electrically insulating barrier was developed by combining a hard and a soft polymer, which both protected the conductive tracks and provided reliable insulation. The least damage to the conductive tracks was achieved when applying the insulating layers and printing the conductive tracks directly onto the metal foil, thus using the form-then-bond method, and then bonding foils face-down to avoid contacting the sonotrode. The encapsulated conductive tracks were fully stable at temperatures up to 60℃ and with small variations up to 100℃.

This study demonstrates a fully encapsulated surface mount component within a metal matrix with vertical through hole connectors, which can serve as building blocks for future 3D metal encapsulated electronics. This enables hybrid processing where electronic, optical and thermal functionalities can be fabricated outside the UAM machine but subsequently becoming a structural part of the component. By repeating and automating the process, entire 3D electronic circuits could be embedded into metal structures, enabling the creation of intelligent structural electronics for industry 4.0.

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