Charge model of four-terminal 2D semiconductor FETs

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1. Abstract

A charge model for four-terminal two-dimensional (2D) semiconductor based field-effect transistors (FETs) is proposed. The model is suitable for describing the dynamic response of these devices under time-varying terminal voltage excitations.

2. Introduction

Since the emergence of graphene, over a surprisingly short period of time, an entire new family of 2D materials have been discovered. Some of them have been recently used as channel materials in FETs, being promising candidates to replace and/or augment silicon and III-V compound semiconductors in the near future. In this context, the development of electrical models for 2D-FETs is essential to help in interpreting the experimental results; allowing to assess their digital and/or RF performance through benchmarking against other existing technologies and eventually providing guidance for circuit design and circuit-level simulations.
Several compact models for three-terminal FETs based on graphene and related 2D materials have been recently published encompassing both static and dynamic regimes [1]–[3]. However, the dynamic regime has been so far described by a charge model derived for bulk MOSFETs [4] that fails to capture the specific physics of 2D semiconductors. This charge model is based on a parameter that provides a continuum transition between the linear and saturation regimes of the transistor. This approximated model has been used, for example, for 2D-FETs considering a weak-inversion situation where the net channel charge is assumed to be linear along the channel [1]. In addition, it has also been applied for graphene FETs by approximating the net charge in the channel with compact expressions valid for materials with a bandgap [2], [3].
Based on a recently published compact drain current model for 2D semiconductor FETs [5] that considers Fermi-Dirac statistics and drift-diffusion transport, we present a quasi-static model of the terminal charges of four-terminal 2D-FETs shown in Fig. 1. To guarantee charge conservation, a Ward-Dutton linear charge partition scheme has been used. Together with the drain current model in [5], a large-signal model could be developed combining both models as a tool for simulating the electrical behaviour of 2D-FET based circuits.

3. Results

The compact charge model derived for bulk MOSFETs [4] and later used for 2D-FETs in [1] is benchmarked against numerical calculations performed with our 2D charge model for the device described in Table 1. We have considered a small back gate capacitance coupling as compared to the top gate, i.e., $C_{bb} << C_{bt}$, so that the four-terminal device can be considered as a three-terminal device and therefore, is directly comparable to the results provided in [1]. The net charge along the channel, evaluated with our model, is shown in Fig. 2 for different drain biases. We have compared the charge associated to each terminal for both low and high drain biases: (1) V_{ds} = 0.1 V where the channel charge is linear along the channel (blue solid line in Fig. 2) and (2) V_{ds} = 0.5 V, where the channel charge is no longer linear along the channel (green solid line in Fig. 2). Although in case (1) the charge model derived for bulk MOSFETs follows the numerical results (Fig. 3), in case (2) the results bring to light that the model derived for bulk MOSFETs is not appropriate to describe accurately the charge associated to each terminal of a 2D-FET, especially at high bias (Fig. 4). Specifically, in case (2), the charge model in [1] would underestimate the current contribution in the dynamic regime computed as the time derivative of terminal charges at an operational bias point.

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References

[1] S. V. Suryavanshi and E. Pop, *J. Appl. Phys.*, **120**(22), pp. 1–10, 2016.
[2] Han Wang, *et al.*, *IEEE TED*, **58(**5), pp. 1523–1533, May 2011.
[3] S. Rakheja, *et al.*, IEEE TNANO., **13**(5), pp. 1005–1013, Sep. 2014.
[4] Y. Tsividis, *Operation and modeling of the MOS transistor*, 2nd ed. New York ; Oxford: Oxford University Press, 1999.
[5] E. G. Marin *et al.*, *IEEE TED*, **65(**3), pp. 1239–1245, Mar. 2018.

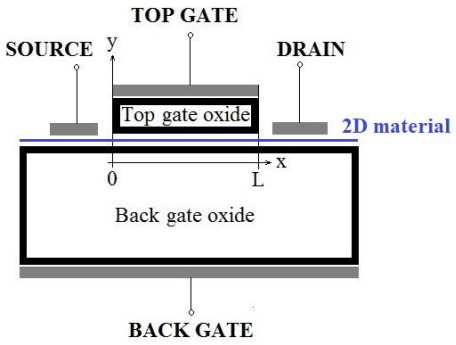

Fig. 1. Cross section of a four-terminal field-effect transistor where a 2D semiconductor material plays the role of the active channel. The electrostatic modulation of the carrier concentration in the channel is achieved via a double-gate stack consisting of top and back gate dielectrics and corresponding metal gates.

Table 1. Input parameters of a WSe_2-based FET. The meaning of the input parameters is explained in [5]. T is the temperature, g_s and g_v are the spin and valley degeneracies, respectively; m^*_v is the valence band effective mass, μ represents the effective carrier mobility at low fields, L is the channel length, C_{bt} and C_{bb} are the top and back geometrical barrier capacitances, respectively; and V_s and V_b are the source and back gate biases, respectively.

Input parameter	Value	Input parameter	Value
T	300 K	L	1 µm
g_s	2	C_{bt}	0.63 µF/cm^2
g_v	1	C_{bb}	0.13 nF/ cm^2
m^*_v	$0.44m_0$	V_s	0
μ	300 cm^2/Vs	V_b	0

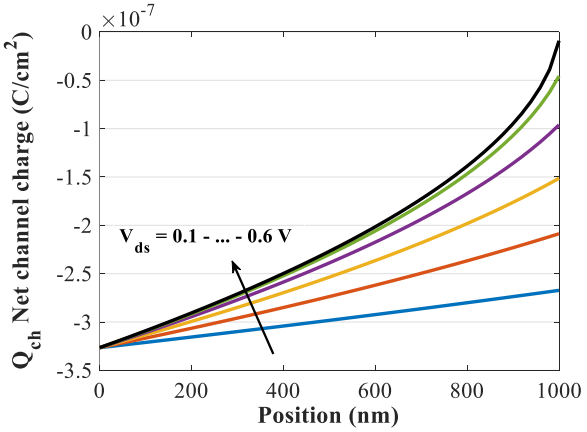

Fig. 2. Net charge along the channel for different drain biases at V_{gs} = 0.5 V. For low drain biases, Q_{ch} can be approximated by a straight line along the channel.

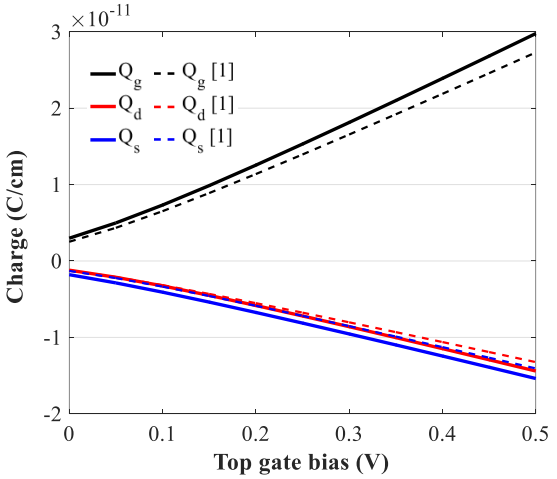

Fig. 3. Charge associated to each terminal normalized to the channel width vs. top gate bias for V_{ds} = 0.1 V. Solid lines represent the outcome of our numerical charge model and dashed lines represent results using the charge model for bulk MOSFETs presented in [4] and used in [1] for 2D-FETs.

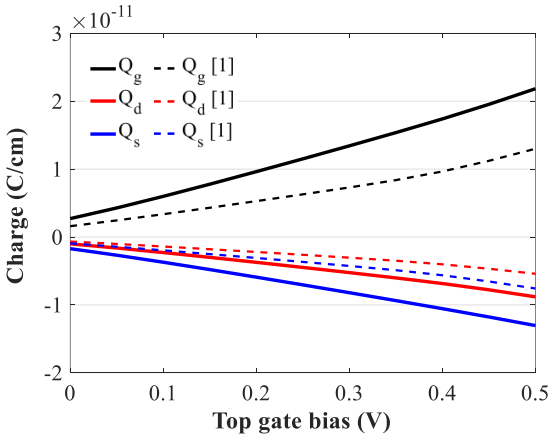

Fig. 4. Charge associated to each terminal normalized to the channel width vs. top gate bias for V_{ds} = 0.5 V. Solid lines represent the outcome of our numerical charge model and dashed lines represent results using the charge model for bulk MOSFETs presented in [4] and used in [1] for 2D-FETs.