# Feasibility of Novel Low-cost Deca-Nanometer Vertical MOSFETs for Radio Frequency Application

Thesis submitted in accordance with the requirements of the

**Department of Electrical Engineering and Electronics**

**University of Liverpool**

## Doctor in Philosophy

**Author: Lizhe Tan**

**Supervisor: Stephen Hall**

**October 2008**

“ Copyright © and Moral Rights for this thesis and any accompanying data (where applicable) are retained by the author and/or other copyright owners. A copy can be downloaded for personal non-commercial research or study, without prior permission or charge. This thesis and the accompanying data cannot be reproduced or quoted extensively from without first obtaining permission in writing from the copyright holder/s. The content of the thesis and accompanying research data (where applicable) must not be changed in any way or sold commercially in any format or medium without the formal permission of the copyright holder/s. When referring to this thesis and any accompanying data, full bibliographic details must be given, e.g. Thesis: Author (Year of Submission) "Full thesis title", University of Liverpool, name of the University Faculty or School or Department, PhD Thesis, pagination.”

# Abstract

The vertical MOSFET (VMOSFET) is a strong contender for low operating power devices on the ITRS road map, which is presently at the 65 nm technology node. VMOSFETs have already found applications in the power device market and also shown feasibility as both digital and analogue/RF devices. The proposed VMOSFETs are CMOS technology compatible and can be fabricated with a channel length down to sub-0.1 μm without the need for expensive deep submicron lithography. This provides an opportunity to fabricate high-performance RF blocks with a low cost process and integrate them with digital ones. On the other hand, VMOSFETs suffer from much higher parasitic capacitances which limits its operation frequency. They can also suffer from severe short channel effects which shift the threshold voltage and increase the off-current.

Previous research has demonstrated the feasibility of some novel concepts to address the above limitations: overlap parasitic capacitance by fillet local oxidation (FILOX) and short-channel effect by junction stop (JS). In this work, I have investigated in detail, the properties of devices with the above features through experimental, analytical and numerical modelling studies. Furthermore, device performances at RF frequency have been measured and analysed. Finally, a set of compact model parameters has been extracted targeting on the 100nm short channel device with FILOX using EKV model approach.

Through the characterisation and numerical simulation of the VMOSFET-JS, we have investigated electrical anomalies and relevant underling physics in different parts of the device through analytical model study and parameters fitting. Numerical simulation also showed the individual impact of symmetrical and asymmetrical junction depths with regard to charge sharing and drain induced barrier lowering (DIBL) which allowed further improvement in the device design, in particular, the possibility of allowing lower body doping and hence higher channel mobility and on-current. It is also shown that there is a critical junction depth above which the JS effect on SCEs reaches its maximum.

FILOX technology has been incorporated into ultra-thin pillar capacitors and assessed by C-V and I-V characterisation. Feasibility for incorporating FILOX into fully-depleted VMOSFET structures is demonstrated. Low levels of leakage current were observed. A VMOSFET-FILOX incorporating a retrograde channel has been designed and fabricated. Theoretically the new design brings increased on-current while maintaining the off-current level. A number of anomalies in experimental devices are explored.

A surface potential based analytical model for source series resistances has been developed. The model shows good agreement with the source series resistance extracted from the 2D simulations using the Z parameters method. Suggestions are made to address

the series resistance limitation on cut-off frequency, $f_T$ which is shown to be related to FILOX thicknesses and associated process conditions.

Cut-off frequency characterisation has shown that VMOSFET-FILOX with frame gate has only half the $f_T$ of double gate contact which is shown to be able to achieve a maximum $f_T$ of 8.6 GHz. The effects on $f_T$ of bias, channel length, width and FILOX thickness have been investigated in some detail. 3D simulation studies address performance including the influence of corners on the electrical characteristics. The numerical simulation calibrated with the process has suggested the best $f_T$ can be achieved can reach 30.5GHz for a 60nm FILOX. Device simulation also suggests that if the junction abruptness is improved to an ITRS requested level for a 50nm channel length, the peak $f_T$ can be boosted to 99.4GHz. Therefore, an almost three-generation-hop in RF performance that can be achieved using a 0.35μm lithography stepper compared to the advanced lateral MOSFETs at the same lithography technology node.

The extraction of the EKV parameters, which model both DC and AC performances, has been conducted using the VMOSFET-FILOX devices with a double gate contact. In the process, some modelling issues have been raised. The problems of realising a truly 'long channel device' for model fitting in contrast to the good fitting for the short channel model and device variations for S-parameters fitting highlight challenges in the compact modelling of vertical MOSFETs. Finally, suggestions to improve process steps are made in order to refine the device performance in accordance with RF requirements.

## *ACKNOWLEDGEMENT*

*During these four years of taking apart of this project, I have received much support from many wonderful people no matter who are near or far away from me. Without them, it would not be possible for me to accomplish this journey. I would like to take this opportunity to share my endless joyfulness and more importantly to say "Thank you" to them.*

*I would like to express my deepest gratitude to is Prof. Steve Hall who has guided and inspired me since the beginning of the project and always kept the flame lighting in these four years. Not only being great in supervision on solving the problems met during research, despite of being busy with dealing with the administrative and teaching duties for the Department as required by the role of the head of department, his encouragement and substantial support to the young generation of engineers is also most helpful and memorable. I am very grateful for his support and trust in all kinds.*

*I would like to express my sincere gratitude to Prof. Peter Ashburn, Dr. Mohammad M. Al Hakim and Dr. Enrico Gili from the team in University of Southampton for kindly providing the samples and comments on my work. Our cooperation has been a wonderful experience and formed such an important part of the project. Also I would like to acknowledge deeply Sean Connor and Arnaud Bousquet from MHS for allowing me to access their workstation and assist me in the laboratory.*

*I also would like to express my sincere gratitude to my dear colleagues in the research group. Many thanks to Mr William Davey for sharing the same office and lots of wonderful laughs. Many thanks to Dr. Yi Lu and Dr. Ivona Z. Mitrovic for their professional knowledge, useful discussions and suggestions on looking into the problems. Many thanks to Mr Paul Wakinson and Mr Kevin Molloy for their important technical assistance in the labs and office. Many thanks to Mrs Jacqueline Cowan for her kind concern every time I came to the office. It has been a great privilege and a treasured experience for me to study in the Electrical Engineering and Electronics Department, University of Liverpool.*

*Last and most importantly, I dedicate the thesis to my parents Zaixi Tan, Jianfu Li and my fiancée Sui Liu. Many thanks to them for their support in a numerous ways and their understanding on the fact that I could not always be with them during these years. Without their love and care, this thesis is not possible. Of course, I must thank all my friends who have been giving me encouragement and support in the last four years.*

# Content Table

Abstract....I
Acknowledgement ....III
Contents....IV
List of Figures....VIII
List of Tables....XIII
List of Symbols ....XIV
List of Acronyms....XVIII

**Chapter 1.** Literature Review ....1

1.1 Market Value of RF Applications ....2
1.2 Trend of RF Device Research....4
1.2.1 III-V Transistors.... 4
1.2.2 SiGe HBT BiCMOS.... 6
1.2.3 CMOS Technology....8
1.3 Si Based Vertical MOSFETs....12
1.4 Vertical MOSFETs in this Project....20
1.5 Summary....25

**Chapter 2.** Theory Consideration .... 28

2.1 Introduction.... 29
2.2 Basic Current-Voltage Characteristics in Long Channel MOSFETs.... 29
2.2.1 Universal Drain-Current Model....30
2.2.2 I-V Characteristics in the Linear and Saturation Region....32
2.2.3 I-V Characteristics in the Sub-threshold Region.... 34
2.3 Short Channel Effect....35
2.3.1 Charge Sharing and Drain Induced Barrier Lowering....35
2.3.2 Sub-threshold Degradation....39
2.3.3 Channel Length Modulation and Velocity Saturation....39
2.4 Avalanche Breakdown....41
2.5 Off-State Drain-source Leakages.... 41
2.6 Gate Oxide Leakage Mechanisms.... 43

2.7 RF Performance Figure of Merit........................................................ 46
2.8 MOSFET RF Equivalent Circuit........................................................ 49

**Chapter 3.** Characterisation and Numerical Modelling of Vertical MOSFETs with a Junction Stop........................... 51

3.1 Current-Voltage Characterisation ........................................................ 52
3.1.1 Sample Preparation........................................................ 52
3.1.2 Comparison of Transfer Characteristics........................................................ 54
3.1.3 Comparison of Output Characteristics and Substrate Currents.......... 60
3.2 Carrier Conduction Mechanisms in Gate Oxide........................................................ 65
3.3 Device Modelling and Calibrations........................................................ 67
3.3.1 Simulation Structure Construction........................................................ 68
3.3.2 Calibration of Sub-threshold Region........................................................ 69
3.3.3 Calibration of Off-Current Regime and GIDL........................................................ 71
3.3.4 Calibration of On-Current........................................................ 73
3.4 Summary........................................................ 74

**Chapter 4.** Short Channel Effects in Vertical MOSFETs with a Junction stop ........................................................ 76
4.1 Introduction ........................................................ 77
4.2 Junction effects on CS and DIBL in A Conventional VMOSFET............ 78
4.3 Junction Depth Design in a VMOSFET-JS........................................................ 81
4.4 Discussion........................................................ 85
4.4.1Drain Junction Depth Effects on CS........................................................ 86
4.4.2 Drain Junction Depth Effects on DIBL........................................................ 89
4.5 Summary........................................................ 90

**Chapter 5.** VMOSFETs with Novel Structures........................ 92

5.1 Ultra Thin Pillar Vertical MOSFET with FILOX........................................................ 93
5.1.1 Technology Description........................................................ 94
5.1.2 Capacitance-Voltage Measurements........................................................ 96
5.1.3 Other Capacitor Properties........................................................ 100
5.2 VMOSFET-FILOX with a Retrograde Body........................................................ 104
5.2.1 Analytical Model........................................................ 104
5.2.2 Numerical Model........................................................ 108
5.2.3 Device Characterisation........................................................ 113
5.3 Summary........................................................ 120

**Chapter 6.** Series Resistance in VMOSFETs with FILOX......... 123

6.1 Introduction........124
6.2 Analytical Model of the Bottom Junction Resistance........125
6.2.1 Analytical Model for Accumulation Resistance, $R_{acc}$........126
6.2.2 Analytical Model for Spreading Resistance, $R_{sp}$........130
6.2.3 Analytical Model for $R_{sh1}$ in Parallel with $R_{acc3}$........133
6.2.4 Discussions on Series Resistance in Bottom Junction and Top Junction
........134
6.3 $R_d$ and $R_s$ Extraction using an RF-Impedance Technique........135
6.3.1 Technique Description........136
6.3.2 The Effect of FILOX Thickness on $R_d$ and $R_s$........138
6.3.3 The Effect of Drain/Source Implantation and RTA on $R_d$ and $R_s$........143
6.4 Summary........144

**Chapter 7.** $f_T$ Characterisation........146

7.1 Calibration and De-Embedding........147
7.2 $f_T$ Characterisation of Second Batch VMOSFET-FILOX........151
7.2.1 $f_T$ Extraction Technique........151
7.2.2 The Effect of Contact Resistance on $f_T$........153
7.2.3 The Effect of Biases on $f_T$........154
7.2.4 The Effect of Gate Types on $f_T$........157
7.2.5 The Effect of Channel Length and Channel Width on $f_T$........159
7.2.6 The Effect of FILOX Thickness on $f_T$........162
7.2.7 Corner Effects........163
7.2.8 50nm Ideal Device Simulation........164
7.4 Summary........165

**Chapter 8.** EKV Modelling........167

8.1 Introduction........168
8.2 Data Acquisition........168
8.3 Extraction Strategy........169
8.4 Parameter Extraction........170
8.5 Summary........181

**Chapter 9.** Conclusions & Suggestions for Future Work............185

9.1 Conclusions........................................................................186

9.2 Suggestions on Future Work................................................... 192

Reference List..................................................................................197

Appendix A....................................................................................... 206

Appendix B....................................................................................... 210

Appendix C....................................................................................... 212

Appendix D....................................................................................... 214

Appendix E....................................................................................... 215

Appendix F....................................................................................... 220

# List of Figures


1.1 (a) Wireless application coverage (b) established and emerging markets. 3
1.2 Block diagram of a typical base station. 4
1.3 Cross sectional diagram of npn GaAs HBT. 6
1.4 Cross sectional diagram of GaAs/AlGaAs HEMT. 6
1.5 Cross sectional diagram of SiGe HBT by IBM. 8
1.6 Cross sectional diagram of SiGe HBT based BiCMOS by IBM. 8
1.7 Cross sectional diagram of a typical Si LDMOS. 9
1.8 Cross sectional diagram of a typical SOI. 10
1.9 Basic structures of a Si based planar double gate, planar gate-all-around, FinFET, vertical MOSFETs with double gate and surrounded gate. 13
1.10 Cross sectional diagram of selectively grown epitaxial p type VMOSFET. 14
1.11 (a) Simulated electron concentration for delta local doping; (b) corresponded doping profile along the pillar height at the surface. 14
1.12 Overlap capacitance reduced by depositing SiO2/PolyGate/SiO2 layers in a selective epitaxy grown VMOSFET. 15
1.13 SiGe source VMOSFET for parasitic bipolar effect reduction. 16
1.14 First reported ion-implanted defined vertical MOSFET with a GAA structure. 17
1.15 First reported ion-implanted defined ultra-thin-body vertical MOSFET with a double gate structure. 18
1.16 TEM picture of the gate oxide at the pillar corners featuring different surface orientations. (a) 10 nm oxide thickness at the (001) sidewall (b) 14 nm oxide thickness at the (011) sidewall; (c) 12 nm oxide thickness at the $11\sqrt{2}$ sidewall. 18
1.17 Brief fabrication process of the ultra-thin-vertical-channel MOSFET. 20
1.18 Fabrication process of an ion implanted Vertical MOSFET with a Fillet Local Oxidation (FILOX). 21
1.19 Fabrication process of an ion implanted Vertical MOSFET with a Junction Stop structure (JS). 24
2.1 Basic structure of an nMOSFET. "Y" direction is along the channel; "X" direction is perpendicular to the channel. 30
2.2 The electric field contours in a lateral MOSFET with a gate bias above threshold voltage and with low drain bias. 37
2.3 Potential and band diagram along the channel where the magnitude and the position of minimum surface potential determine these values for the source barrier height. 37
2.4 Drain/source junction leakage mechanism in deep sub-micron. 42
2.5 Band diagram of direct tunneling mechanism. 43
2.6 Band diagram of Fowler-Nordheim mechanism tunneling. 45
2.7 A simplified two port network of a MOSFET at RF. 48
2.8 Equivalent circuit of a MOSFET at RF frequency range. 50
3.1 Vertical MOSFET structure with a junction stop beneath the poly-Si drain contact. 53

3.2 Transfer characteristics of devices in split # 1: W=32um. 55
3.3 Transfer characteristics of devices in split # 3: W=52 um. 55
3.4 Transfer characteristics of devices in split# 5: W=52 um. 55
3.5 Transfer characteristics of devices in split#6: W=27 um. 56
3.6 Transfer characteristics of devices in split#7: W=27 um. 56
3.7 Transfer characteristics of devices in split#8: (a) & (b) W = 27 um with a high $V_T$ ; (c) & (d) W = 27 um with a low $V_T$. 56
3.8 Comparison of (a) $V_T$ and (b) $I_{on}/I_{off}$ in DoT and SoT modes in different process splits. 58
3.9 (a) Comparison of sub-threshold slope in SoT and DoT; (b) Assistant diagram showing high interface states density induced on the top of the pillar due to Poly-Si gate over-etching. 60
3.10 Output characteristics of a device in split# 1 W=32um. 60
3.11 Output characteristics of a device in split#3 W = 27 um. 61
3.12 Output characteristics of a device in split#5 W=52 um. 61
3.13 Output characteristics of a device in split#6 W=27um. 61
3.14 Output characteristics of a device in split#7 W=27 um. 62
3.15 Output characteristics of a device in split#8 W = 27 um. 62
3.16 Comparisons of IBVGS curves for both DoT and SoT modes for all the splits with varying drain biases.63
3.17 Comparison of breakdown voltage and the ratio of maximum body current in DoT and SoT modes. 65
3.18 Gate to body oxide current vs. gate bias; tox=3nm; area=2.1x10-9m-2; the source and drain electrodes were set to be floating. 66
3.19 Temperature dependence of the gate to body oxide leakage. 67
3.20 3D view of a surround gate VMOSFET-JS structure; W= 30μm. 68
3.21 2D view of VMOSFET-JS structure with a 70nm channel length. 68
3.22 Transfer characteristics of fabricated device compared to the partially fitted device simulation apart from on-current region. L= 70nm, $t_{ox}$=3.0nm, $N_a=3.0\times10^{18}cm^{-3}$. 70
3.23 (a) Reciprocal temperature dependence of the large-area drain diode leakage for different values of reverse bias. The doping level in a drain junction at the pillar top is squared in (b). 71
3.24 Band diagram of electron tunnelling in the drain junction surface region under high negative gate bias. 72
3.25 Simulated on-current vs. measured on-current. $V_{GS}$=2.5V 74
4.1 (a) Charge sharing and (b) DIBL as a function of bottom junction depth for a VMOSFET and a conventional lateral MOSFET. 79
4.2 Simulations of DIBL and CS as a function of reducing drain junction depth in a vertical MOSFET with a junction stop (VMOSFET-JS). 82
4.3 DIBL as a function of body doping for VMOSFETs and VMOSFET-JSs. The devices are simulated in DoT configuration with a symmetrical drain/source junction depth of 30nm. 82
4.4 $I_{off}$ as a function of Ion for VMOSFET and VMOSFET-JS devices with different body doping levels. 83
4.5 (a) Cross-section of the simulated devices showing the cut line along which the source electric field was simulated (b) Absolute source junction field as a function of distance along the source for VMOSFET and VMOSFET-JS devices with 60nm and 15nm source junctions. 85
4.6 Simulated potential contours in a VMOSFET-JS device with asymmetrical drain and source junctions. 87

4.7 Conduction band energy (cut line shown in Fig 7) as a function of distance along the channel for MOSFET-JS devices with different drain junction depths ($X_{jd}$). 87
4.8 Minimum surface potential and channel depletion region width as a function of drain junction depth for a MOSFET-JS device simulated with $V_{DS}$=50mV and $V_{GS}$=1V in DoT configuration. 88
4.9 Conduction band energy as a function of distance along the body surface for VMOSFET-JS devices with different drain junction depths ($X_{jd}$). 89
5.1 Process flow for fabrication of TiN surround-gate, ultra-thin pillar. 95
5.2 SEM cross-section through a vertical edge of a pillar capacitor test structure. 95
5.3 Test structure of surrounded gate pillar capacitor (fully depleted device); $t_{ox}$ = 8.0nm, $t_{FILOX}$ = 8.3nm. 95
5.4 Test structure of a pillar bottom capacitor where HSW: the height of a pillar. 96
5.5 C-V characteristics of ultra-thin pillar capacitors with (a) 8nm vs. 37nm FILOX; (b) 16nm vs. 24nm. 97
5.6 Gate oxide leakage current as a function of magnitude of gate bias on 20 nm ultra-thin pillar capacitors are with different FILOX thicknesses. 98
5.7 Mechanic stress in 20 nm ultra-thin pillar capacitors with 10nm and 40nm thick FILOX. 99
5.8 C-V characteristics of ultra-thin pillar capacitors with four different pillar thicknesses. FILOX thickness is 37 nm. 99
5.9 HF and LF curves for Pillar Bottom (PB) device with TiN gates. 100
5.10 (a) Magnified LF & HF curves for the pillar bottom device; (b) Schematic diagram of the influence of oxide charge in the LOCOS; (c) Frequency dependent upturn. 100
5.11 Gate current vs. gate bias of the PT capacitor with the Fowler-Nordheim plot included. 103
5.12 Total VT shift as a sum of CS and DIBL vs. $W_{dm}$. 105
5.13 (a) Schematic diagram of an ideal retrograde body; (b) $W_{dm}$ decreases with Ws; (c) VT shift due to SCE decreases with Ws. 106
5.14 Key steps for retrograde body doping process. 110
5.15 Boron doping profile comparison along the body depth (cut line 1) using different implantation conditions. 111
5.16 Net doping profile along cut line 1 after 45KeV and 45o RB implantation 10s 1100 °C RTA. 111
5.17 Transfer Characteristics under low and high drain biases for devices with (a) uniform body with a doping level of $5x10^{17}cm^{-3}$; (b) retrograde body with a doping profile varies from of $4.8x10^{17}cm^{-3}$ to $1x10^{18}cm^{-3}$ with Wdm; (c) uniform body with a doping level of $1x10^{18}cm^{-3}$ 112
5.18 Linear plot of transfer characteristics under low and high drain biases among the three devices. 112
5.19 Comparison of body doping profiles from the process simulation along the body depth (cut line 1). 112
5.20 Layout structure of a GAA with double gate contacts and P+ ring area surrounding the device. 114
5.21 Threshold voltages measured from the RB, DGC and P ring devices under SoT mode, with comparison to a uniform body DGC, P ring device. 114
5.22 (a) VT extraction from the IDVG curves under low drain bias at varied body biases using linear extrapolation method; (b) Calculated average body factors fitted to characterized body factors in low and high body bias region. 116
5.23 On-currents of double gate contact devices for SoT and DoT modes. 116
5.24 (a) Transfer characteristics under low and high drain biases in a sample device; (b) DIBL values for DoT

and SoT in the rest of the devices. 118

5.25 Measured (a) output characteristics; (b) Substrate current vs. gate bias under different drain biases for DoT and SoT. 118

5.26 (a) Simulation structure of a non-uniform body doping device; (b) the body doping profile along the cut line in the pillar varies from $6x10^{18}cm^{-3}$ to $1x10^{17}cm^{-3}$. 119

5.27 Simulated transfer characteristics under high and low drain biases with a 110 mV high DIBL for the DoT mode. 120

5.28 (a) Direct tunnelling current is observed in the gate to body oxide with $t_{ox}$=2.6nm (b) Direct tunnelling current is observed in the gate to source overlap region with $t_{FILOX}$ = 36 nm. 120

6.1 Current conduction path in VMOSFET-FILOX under a) $V_{DS}$=0.1V $V_{GS}$=1.5V; b) $V_{DS}$=1.5V $V_{GS}$=1.5V; L=100nm;FILOX=40nm. 125

6.2 A VMOSFET-FILOX structure with an equivalent circuit of the series resistance; L=100nm. 126

6.3 Series resistance in the overlap region of the (a) bottom and (b) top junction. 126

6.4 Accumulation layer in the junction depletion region. 127

6.5 $R_{acc1}$ vs.$V_{GS}$. 130

6.6 Spreading resistance geometry: α is the spreading angle and is determined by the geometry parameters. 131

6.7 $R_{sp}$ vs. $V_{GS}$. 132

6.8 $R_{acc2}$ vs. $V_{GS}$. 132

6.9 $R_{acc3}$ vs. $V_{GS}$. 133

6.10 Racc1, Rsp, Rtotal vs. $V_{GS}$ of the bottom junction. 134

6.11 The simplified equivalent circuit of a MOSFET. 136

6.12 $-\omega$/Im(Z22) vs. $\omega^2$ of the sample at $V_{GS}$=2V with frequency from 100MHz to 9GHz. 139

6.13 Extracted and analytical $R_s$ vs. $V_{GS}$ frequency FILOX=40nm, 0o S/D implant, 40s RTA, $V_{DS}$=0V. 139

6.14 $R_d$, $R_s$ vs. $V_{GS}$, 0o S/D implant, 40s RTA, $V_{DS}$=0V. 140

6.15 (a) FILOX Encroachment above the bottom junctions from thinnest and thickest cases(b) Doping profile at junction boundary under FILOX thicknesses of 50nm and 60nm for top junction. 141

6.16 $I_{on}$, $f_T$ vs. FILOX thickness; $V_{DS}$=$V_{GS}$=1.0 V. 142

6.17 $R_d$, $R_s$ vs. $V_{GS}$ for cases of a) 0 degree s/d implant, RTA=10s; b) 15 degree s/d implant, RTA=10s; c) 0 degree s/d implant, RTA=40s; all with FILOX=40nm, $V_{DS}$=0V. 143

7.1 RF Layout with ten identical devices connected in parallel where source pad is tied to body using a ring type contact; drain and source pads are deposited separately within the ring. 147

7.2 (a) 2D schematic diagram; (b) 3D diagram of an open dummy structure for pad parasitic de-embedding. 148

7.3 Smith chart: the frequency response of S11 (blue) and S22 (red) as frequency increases from 1GHz to 20 GHz. 149

7.4 Pad parasitic circuitry without inductive components but with capacitive components only. 149

7.5 Comparison of (a) Y11, Y12, Y21, Y22 and (b) S11, S12, S21, S22. 153

7.6 Comparison of Y-parameter before de-embedding ($Y_{total}$) and after de-embedding ($Y_{sub}$). 150

7.7 Technique A: $f_T$ extracted from the unit current gain axis with the -20dB/dec roll-off line from h21 vs.

frequency curves. fT≈7.8 GHz when $V_{GS}$ = 1.2V, $V_{DS}$ = 1.5 V 152

7.8 Technique B: $f_T = |h_{21}| \cdot freq$ where fT=7.75 GHz when $V_{GS}$= 1.2V, $V_{DS}$ = 1.5 V. 152

7.9 Contact layout of a VMOSFET-FILOX with a poly-gate covering the entire pillar sidewall of the pillar and the periphery area on the top. 153

7.10 (a) $f_T$ vs. $V_{GS}$ extracted from numerically simulated VMOSFET with 40nm and 60nm thick FILOX; (b) $f_T$ comparison of the fabricated device and the numerical model with/without Radd (c) IDVG comparison of the above two cases. 155

7.11 $f_T$ vs. $V_G$ of a double gate contact VMOSFET with L=100nm, W=30um, $t_{FILOX}$=40nm. 156

7.12 (a) Simulated total gate-drain/source overlap capacitance and gm vs. gate bias; (b) Simulated $f_T$ vs. gate bias; $V_{DS}$=1.5V. The on-current has been calibrated. 156

7.13 $f_T$ comparison of double gate contact and frame gate devices and (a) a channel length of 100nm (b) a channel length of 150nm. 40nm thick FILOX 157

7.14 Structures of double gate contact and frame gate devices for 3D simulation. 158

7.15 Overlap capacitance comparison of double gate and frame gate contact devices with structures shown in Fig 7.14. 158

7.16 $f_T$ comparison of devices with 40nm FILOX, between 100nm channel length and 150nm channel length for both (a) double gate contact (b) frame gate contact. 159

7.17 $g_m$ comparison of devices with 100nm channel length and 150nm channel length using a double gate contact. 160

7.18 $f_T$ comparison of devices with different channel width for (a) double gate contact; (b) frame gate. 40nm FILOX, 100nm channel length. 161

7.19 $f_T$ comparison of devices with and without increased active area. 40nm FILOX, 100nm channel length. 161

7.20 $f_T$ comparison of double gate contact devices with different FILOX thicknesses. 30um width, 100nm channel length. 162

7.21 Drain current comparison of double gate contact devices with different FILOX thicknesses from (a) measurement (b) simulation. 30um channel width, 100nm channel length. 163

7.22 Conduction current density contour at the body corner regions in (a) the device with poly-Si gate surrounding the corner; (b) the device without poly-Si gate surrounding the corner. 163

7.23 Transfer characteristics of devices with/without corner with $V_{DS}$=1.5V where no significant improvement on the on currents by corners is spotted W=4um. 164

7.24 (a) Doping profile along the drain, channel and source in a simulated VMOSFET with 50nm channel length and 40nm FILOX; (b) Extracted $f_T$ vs. gate bias. 165

8.1 Transfer characteristics under $V_{DS}$=1.5V and 1.0V from DGC devices with 40nm FILOX and 30um channel width in the four wafers. 169

8.2 EKV model parameters extraction strategy. 170

8.3 COX extraction by fitting the accumulation region in high frequency C-V plot for a large planar gate oxide capacitor (Line – Simulation data; Symbol – Experiment data). 171

8.4 VTO, GAMMA, KP, E0, E1, EKA extraction by fitting the simulation and measurement in (a) linear graph of IDVG; (b) log graph of (a); (c) gm; all with VDS=50mV. 172

8.5 ZC and THC extraction from measured and fitting (a) IDVG and (b) gm through a auto-optimiser tool kit; VDS=1.5V. 173

8.6 DL, RLX, ETAD, LETAD and NCS extraction through fitting of measured and simulated IDVG and gm curves of the short channel device with VDS=0.05V (a) - (b) and VDS=1.5V (c) - (d) . 174

8.7 Measured and simulated output characteristics and output resistance curves of the short channel device after extraction of UCRIT, LAMBDA. 175

8.8 Comparison of measured and simulated IDVG curves of long device using the RLX extracted from the short device in (a) log scale (b) linear scale. 176

8.9 On-currents comparison of the long and the short devices to the simulated short device. Use the same RLX that is extracted from the long device fitting. 177

8.10 Fitting of the measured and simulated output characteristics of the long channel device. 178

8.11 (a) Reasonably good fitting of IDVG with VDS=1.5V in the long channel device after using the velocity saturation and SCE related parameters from the short device; (b) fitting of gmVG with VDS=1.5V. 179

8.12 Fitting of (a) S11, (b) S12, (c) S21, (d) S22 parameter curves of the short channel device with $V_{GS}$=0, 0.5V,1.0V, 1.5V 2.0V, 2.5V and $V_{DS}$=50mV, 0.5V,1.0V, 1.5V. ($V_{DS}$ sweeping orders not) 180

9.1 A brief process flow for fabrication of an ultra-thin body VMOSFET structure. 195

# List of Tables

3.1 Summary of splits of jS batch devices 54

3.2 Electrical charactersitics parameters of JS batch devices 57

3.3 Breakdown voltage and ratio of maximum body current in DoT and SoT 64

5.1 FILOX thickness vs. gate oxide Thickness in UTP capacitors 98

5.2 Designed key step conditions summary of RB device fabrication 111

5.3 Device parameter comparison of the three cases 113

6.1 $C_{ov}$ at $V_{GS}$=1.0V vs. FILOX thickness 142

6.2 $R_d$, $R_s$ vs tilt angle, RTA time with $V_{GS}$=2V 144

8.1 Extracted DC Parameters using EKV model 183

8.2 Physics modelled vs. un-modelled 184

9.1 Performance comparison among the simulated UTVMOSFET and fabricated VMOSFETs with single gate and double gate contacts 195

# List of Symbols

| | |
|---|---|
| $A_G$ | - gate area [$m^2$] |
| A | - oxide carrier tunnelling variable I [$e^2$/JsV] |
| Aa | - constant for electron tunnelling rate for GIDL I [$V^{-2}s^{-1}m^{-1}$] |
| Bb | - constant for electron tunnelling rate for GIDL II [$Vm^{-1}$] |
| B | - oxide carrier tunnelling variable II [$eV^{0.5}$/Js] |
| $C_{ox}$ | - oxide capacitance per unit of area [F/$m^2$] |
| $C_{acc}$ | - accumulation capacitance [F] |
| $C_{ds}$ | - drain-to-source parasitic capacitance [F/m] |
| $C_{dm}$ | - channel depletion region capacitance induced by the gate [F/m] |
| $C_{gs}$ | - gate-to-source parasitic capacitance [F/m] |
| $C_{gd}$ | - gate-to-drain parasitic capacitance [F/m] |
| $C_{it}$ | - interface-trap induced capacitance [F/m] |
| $D_{it}$ | - interface traps/states density [$cm^{-2}$] |
| $E_c$ | - energy level of the conduction band [eV] |
| $E_f$ | - Fermi energy level [eV] |
| $E_{Fn}$ | - electrons quasi Fermi level [eV] |
| $E_{Fp}$ | - holes quasi Fermi level [eV] |
| $E_g$ | - semiconductor band gap = 1.12eV in Si |
| $E_i$ | - Fermi level in intrinsic silicon [eV] |
| $E_v$ | - energy level of the valence band [eV] |
| $E_{trap}$ | - difference between the trap energy level and the intrinsic Fermi level [J] |
| $\varepsilon_v$ | - vacuum permittivity=8.85x10-14 [F/m] |
| $\varepsilon_{ox}$ | - dielectric constant of silicon dioxide = $3.9 \cdot \varepsilon_v$ |
| $\varepsilon_{si}$ | - dielectric constant of silicon = $12 \cdot \varepsilon_v$ |
| $f_T$ | - cut-off frequency [Hz] |
| $f_{max}$ | - maximum oscillation frequency [Hz] |
| $g_m$ | - transconductance [A/V] |
| $g_{ds}$ | - output conductance [A/V] |
| $G_{max}$ | - Maximum Power Gain |
| $G_{BBT}$ | - band to band tunneling generation rate [$m^{-3} s^{-1}$] |
| $h_{21}$ | - transistor current gain |
| $h_p$ | - Planck's constant [eVs] |
| $I_B$ | - body current [A] |

$I_D$ - drain current [A]

$I_{DS}$ - drain-source current [A]

$I_{Dsat}$ - drain current at saturation condition [A]

$I_G$ - gate current [A]

$I_{on}$ - on-state drain current of a MOSFET [A]

$I_{off}$ - off-state drain current of a MOSFET [A]

$J_{n,diff}$ - diffusion current density in n type inversion layer [A/m$^2$]

$J_{n,dift}$ - drifted current density in n type inversion layer [A/m$^2$]

k - Boltzmann constant (=8.617x10$^{-5}$eV/K)

L - channel length [m]

$L_{diff}$ - characteristics slope of the Gaussian curvature region [m]

$l_{ext}$ - distance between $N_d$ and $N_{dmax}$ in junction boundary region [m]

$m_e$ - the free electron mass (= 9.1 x 10$^{-31}$ kg)

m - body-effect coefficient

n - electron concentration in inversion layer [m$^{-3}$]

$n_i$ - intrinsic carrier concentration [m$^{-3}$]

$n_o$ - the carrier density conducting through the oxide [m$^{-3}$]

$N_a$ - acceptor doping concentration [m$^{-3}$]

$N_d$ - donor doping concentration [m$^{-3}$]

$N_{ox}$ - fixed charge in oxide [m$^{-3}$]

$N_{it}$ - interface trap density [m$^{-2}$]

$Q_{acc}$ - accumulation layer charge per unit area [C/m$^2$]

$Q_d$ - depletion charge per unit area [C/m$^2$]

$Q_{inv}$ - inversion charge per unit area [C/m$^2$]

$Q_{it}$ - interface trapped charge per unit area [C/m$^2$]

$Q_s$ - total charge per unit area in silicon [C/m$^2$]

$Q_{ox}$ - equivalent oxide charge density per unit area [C/m$^2$]

$R_d$ - drain resistance per width [Ω·m]

$R_s$ - source resistance per width [Ω·m]

$R_{acc}$ - accumulation resistance per width [Ω·m]

$R_{sp}$ - spreading resistance per width [Ω·m]

$R_{sh}$ - sheet resistance per width [Ω·m]

$R_{co}$ - contact resistance per width [Ω·m]

$R_{ch}$ - channel resistance per width [Ω·m]

s - second [s]

Ss - sub-threshold swing or inverse sub-threshold slope [V]

S - Scattering parameter

$\tau$ - transit time for a carrier to travel through the channel [s]

| | |
|---|---|
| $t_{inv}$ | - inversion layer thickness [m] |
| $t_{acc}$ | - accumulation layer thickness [m] |
| $t_{ox}$ | - oxide thickness [m] |
| $t_{FILOX}$ | - fillet local oxidation thickness [m] |
| T | - absolute temperature [K] |
| V | - quasi-Fermi potential for electrons along the channel [V] |
| $V_G$ | - gate voltage [V] |
| $V_B$ | - body voltage [V] |
| $V_D$ | - drain voltage [V] |
| $V_{DS}$ | - drain-to-source voltage [V] |
| $V_{Dsat}$ | - drain-to-source voltage at saturation condition [V] |
| $V_{BD}$ | - breakdown Voltage [V] |
| $V_{fb}$ | - flat band voltage [V] |
| $V_G$ | - gate voltage [V] |
| $V_{GB}$ | - gate/body voltage [V] |
| $V_{GD}$ | - gate/drain voltage [V] |
| $V_{GS}$ | - gate/source voltage [V] |
| $V_{ox}$ | - voltage across oxide [V] |
| $V_S$ | - source voltage [V] |
| $V_{SB}$ | - source/body voltage [V] |
| $V_T$ | - threshold voltage [V] |
| $W_{dm}$ | - minimum channel depletion region width under the gate of a short-channel MOSFET at the threshold condition [m] |
| $W^o_{dm}$ | - long channel depletion region width under the gate at the threshold condition [m] |
| $W_d$ | - channel depletion region width under the gate [m] |
| $W_s$ | - low doped surface width [m] |
| $W_{dep}$ | - lateral depletion region width in drain/source junction [m] |
| Z | - impedance Parameter |
| Y | - admittance parameter |
| $\xi_c$ | - critical field for velocity saturation [Vm-1] |
| $\xi_{max}$ | - maximum electric field in the depletion region [V/m] |
| $\xi_n$ | - lateral electric field in inversion layer [V/m] |
| $\xi_{ox}$ | - electric field across oxide [V/m] |
| $\xi_s$ | - vertical electric field in the semiconductor [V/m] |
| $\upsilon_{sat}$ | - saturation velocity [m/s] |
| V | - channel quasi-Fermi potential [V] |
| $\Phi_B$ | - barrier height for electrons [eV] |

$\Phi_{PF}$ - energy level of a trap in a Poole-Frenkel site [eV]

$m_{ox}$ - carrier effective mass at the conduction band edge in oxide [kg]

$m_e$ - free electron mass [kg]

$\lambda$ - early voltage parameter [$V^{-1}$]

$\mu_{eff}$ - effective electron mobility [$m^2/V$-s]

$\mu_{ox}$ - carrier mobility in oxides [$m^2/V$-s]

$\mu_b$ - carrier mobility in the bulk of the junction [$m^2/V$-s]

$\rho$ - resistivity [cm]

$\tau$ - transit time for an electron to travel from source to drain in the channel [s]

$\tau_o$ - electron lifetime [s]

$\psi_i$ - the intrinsic Fermi level [V]

$\psi_{bi}$ - built-in voltage of a pn-junction [V]

$\psi_s$ - surface potential [V]

$\psi_{min}$ - minimum surface potential [V]

$\psi_B$ - difference between Fermi level and intrinsic level in p type material [V]

$\omega$ - angular frequency [rad/s]

$X_j$ - junction depth [m]

$X_{jd}$ - drain junction depth [m]

# List of Acronyms

$\alpha$ - current spreading angle
CLM - channel length modulation
CS - charge sharing
DIR - direct tunnelling
DoT - drain on top
DUT - device under test
DGC - double gate contact
DIBL - drain induced barrier leakage
FG - frame gate contact
FILOX - fillet local oxidation
JS - junction stop
GIDL - gate induced drain leakage
$N_{dmax}$ - maximum doping level in a junction
PB - pillar bottom
PT - pillar top
RTA - rapid thermal annealing
RB - retrograde body
SILC - stressed induced leakage current
SoT - source on top
SCE - short channel effect
UTP - ultra thin pillar
VMOSFET- vertical metal-oxide-silicon field effect transistor

# Chapter 1

# Introduction and Literature Review

## 1.1 The Market Value of RF Applications

"The wireless telegraph is not difficult to understand. The ordinary telegraph is like a very long cat. You pull the tail in New York, and it meows in Los Angeles. The wireless is the same, only without the cat."

- Albert Einstein, 1938

70 years ago, Einstein's description of the wireless telegraph, an old fashioned word which today translates to "radio frequency", may have already portrayed an image that it should not be too difficult a task for people to understand the concept of wireless communication products. Manipulation of the products should not be more difficult than pulling a cat's tail. Indeed, along with the many years development of the semiconductor industry, wireless communication in the forms of products and services have penetrated into peoples' daily work and life with a tremendous growth rate. Nowadays, wireless/RF applications have become a necessity for most electronic products. As many customer surveys have suggested, the market for wireless/RF applications of which the main areas are illustrated in Fig 1.1, is now huge. The latest report in 2008 (Millward Brown) on consumer awareness of wireless technologies has suggested that in Mainland China, Germany, Japan, Taiwan, US and the UK, 85% of consumers recognize Bluetooth, and for others such as Wi-Fi: 53%, Wireless technology Wireless USB: 57%, IrDA: 53%. Wireless Local Area Network (WLAN) is now capable of reaching virtually every corner of the world. WLAN worldwide service revenues were projected to reach $9.5 Billion by 2007 and the looming global rollout of WiMAX will push its way into 3G market and generate $53 billion in mobile revenue in 2011 (Alexander Resources). It can further be quantified that excluding the market value of other communications, semiconductor

wireless/RF products have become the 2nd largest market only after data processing electronics. In 2007, the total viable market of the entire wireless/RF industry reached $47 billion. The market also has grown steadily every year in size and product variety extending the accessibility worldwide e.g. wireless-chip market has outpaced wireline-chip market in 2007 (The Linley Group).

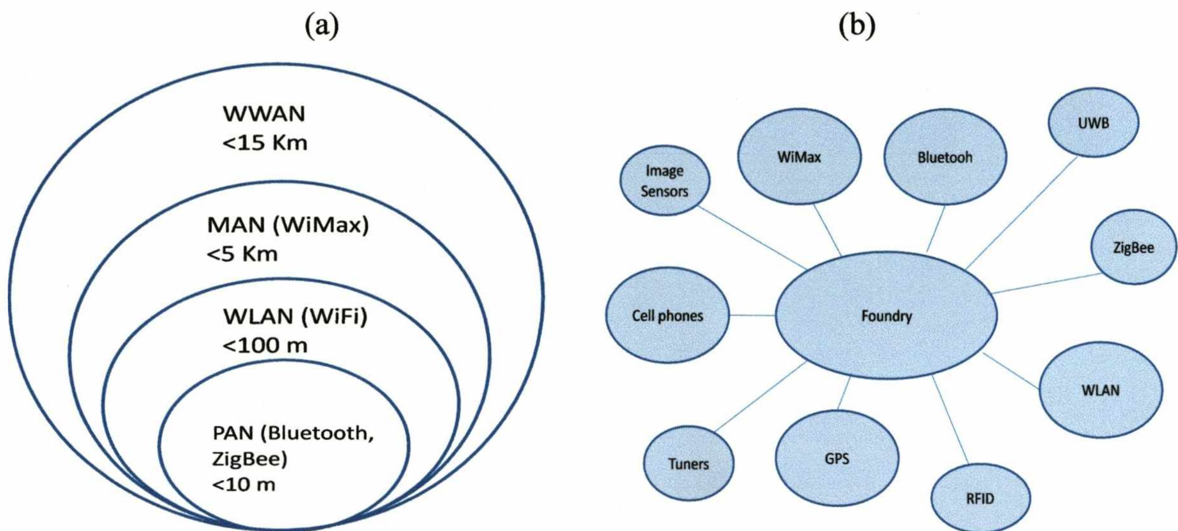



Fig 1.1 (a) Wireless application coverage (b) established and emerging markets [1].

From the technology point of view, the increasing deployment of wireless networks has been pushed by the demand for higher data transmission rate. In order to maintain this technology push of faster transmission speed, the industry is required to make large investments in infrastructure hardware. The base station for wireless signals, which serves as an interface between the antenna for broadcasting the signal and the fixed line telecommunication backbone, is one of the important infrastructure components. Since the power amplifier is also recognized to be the most expensive portion of the capital expenses in a base station, technology that can reduce the complexity and cost of these components is of great interest to the wireless industry. In the base station architecture, the power amplifier is an important block as illustrated in Fig 1.2, with transistor devices serving as core components inside [2]. All together with other semiconductor components, they serve

the purpose of boosting the strength of the RF signals to a level essential for consumers to access the wireless applications over long distance. Similarly transistor devices are also the core components in RF power amplifier for RF blocks in handset devices. Therefore an incredible amount of research has been undergoing in the field of wireless/RF circuits and the related semiconductor components.

This project is largely motivated by the drive for more cost-effective transistors with better RF performance, which especially benefit the medium and small semiconductor companies. The scope of this thesis is focusing on the investigation of the feasibility of CMOS process compatible Vertical MOSFET (VMOSFET) for RF applications. In the next section, variants of RF transistors and their development over the last a few decades will be reviewed.

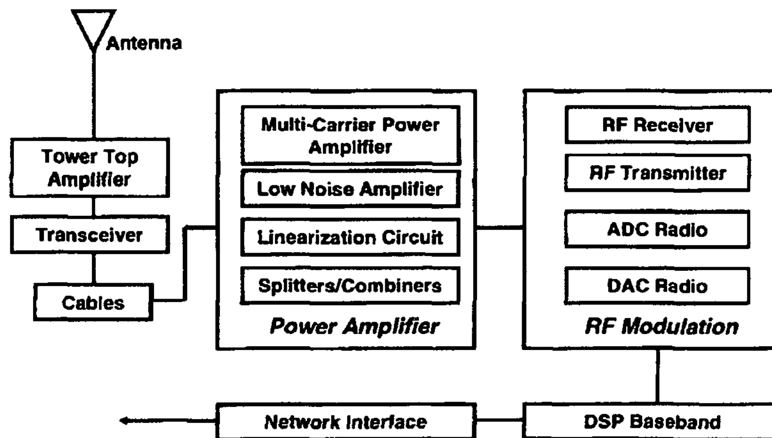



Fig 1.2 Block diagram of a typical base station [2].

## 1.2 The Trend of RF Device Research

### 1.2.1 III-V Transistors

About 15 years ago, the field of RF transistors has been clearly dominated by III-V (e.g. GaAs based) Heterojunction bipolar transistor (HBTs) and HEMT-FET transistors. Even

now GaAs HBT technology (an advanced structure is shown in Fig 1.3) is still currently in widespread use for cell phones. In GaAs technology, the electron mobility and saturated electron velocity are higher than those of Si thus improving the high frequency performance. A further major advantage of GaAs technology over Si, is the ability to form a good semi-insulating substrate which in turn brings a considerable reduction in losses at frequencies in the high GHz regime. The best GaAs HBT shows maximum frequencies of oscillation $f_{max}$ in excess of 200GHz while the cut-off frequency $f_T$ is limited to about 150GHz. [3] The basic structure of a GaAs/AlGaAs HEMT is demonstrated in Fig 1.4. The basic operation of the GaAs depletion-mode FET such as high electron mobility transistor (HEMT) is very similar to that of the JFET. The device consists of a barrier junction controlled by the gate electrode. Through changing the negative bias on the gate the output current conducting across the base also changes therefore inducing a changing current between two ohmic contacts. Heterojunctions are used with a highly-doped wide-band-gap n-type donor-supply layer (AlGaAs) and a non-doped narrow-band-gap channel layer with no dopant impurities (GaAs) to boost electron mobility in the channel. The electrons situated in the n-type AlGaAs thin layer are transferred into the GaAs layer thereby forming a depleted AlGaAs layer. The different band-gap materials form a quantum well in the conduction band on the GaAs side where the electrons can move quickly without colliding with any impurities because the GaAs layer is undoped. This feature enables the transistors which can operate at significantly high frequencies typically over 500GHz. It should be noted that currently GaAs HEMTs are the most widespread commercial GaAs-based RF FETs. However, a major disadvantage is that the substrate of GaAs wafers is not a good thermal conductor and thus has to be thinned for optimum performance in power amplifier applications. Furthermore GaAs is more fragile than silicon resulting in a relatively lower yield of GaAs ICs than the silicon based IC and as a consequence, higher fabrication cost. The fabrication process allows realization of very fast transistors with

"relatively" cheap GaAs substrates but still more expensive than Si. Si is also more abundant and this, together with the relative ease of scaling wafer diameters, leads to lower cost of substrates and processing. Also similar to MESFET devices, the DC operation of GaAs HEMTs is depletion mode thus requiring both positive and negative supply rails which makes it less popular in circuit design.

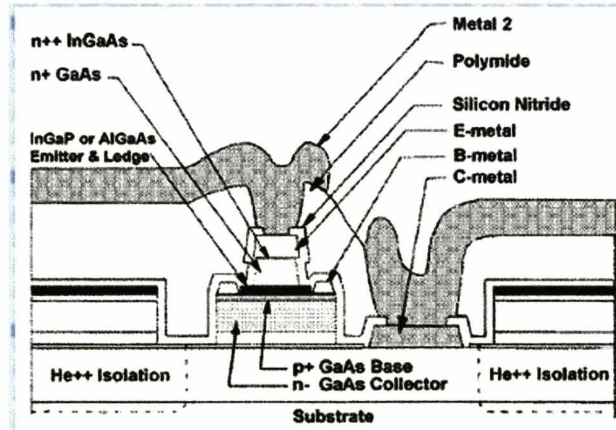



Fig 1.3 Cross sectional diagram of npn GaAs HBT [4].

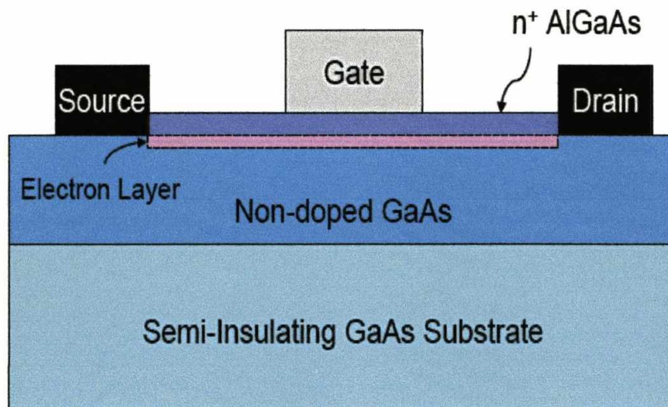



Figure 1.4 Cross sectional diagram of GaAs/AlGaAs HEMT.

## 1.2.2 SiGe HBT BiCMOS

The recent development of RF transistors has formed a comprehensive answer to the question of "Why has the Si based technology become the preference in the RF devices

industry". Compared to compound semiconductor such as GaAs, silicon is the richest natural resource that is abundant on the Earth's crust. Alternatively speaking the economy of scale available to the silicon industry has consisted of a solid precondition of the adoption of silicon. Secondly, silicon dioxide has been seen to be one of the best insulators for device application and can been easily incorporated onto silicon circuits. GaAs does not form a stable insulating layer which precludes the realisation of the enhancement mode devices required to make CMOS. The third major advantage for Si technology to be become a mainstay of wireless/RF industry is that it benefits from the well-developed and thus mature applications of bipolars and MOSFETs devices in digital circuits. In the field of bipolar, SiGe HBT has already been accepted to satisfy the requirements for making high speed transistors which can be applied in the rapid growing communication market.

The concept of combining silicon and germanium into an alloy in the silicon bipolar was developed largely, by IBM. An example of cross-section of a SiGe HBT is shown in Fig 1.5. Comparing to CMOS devices, BJT devices offer the advantages of excellent noise performance and an improved transconductance. Furthermore, for RF low-noise amplifiers, SiGe HBT circuits occupy one-quarter to one-third of the area of CMOS circuits of equivalent functionality [5]. It was also found that for wireless/RF communications circuits, SiGe HBT consumes much less power than CMOS to achieve the same level of performance due to excellent noise performance and an improved transconductance [6]. The real strength of SiGe lies in its ability to integrate analogue, RF and digital on a single chip using existing CMOS foundries. The SiGe BiCMOS process allows enhancement of CMOS performance by the addition of SiGe HBTs. A representative structure of SiGe BiCMOS is shown in Fig 1.6. The fastest SiGe HBTs have greater than 370 GHz cut-off frequency and greater than 350 GHz maximum oscillation frequency [3]. However, the drawback is that fabrication cost of BiCMOS technology is high and also large area is always needed for the digital part.

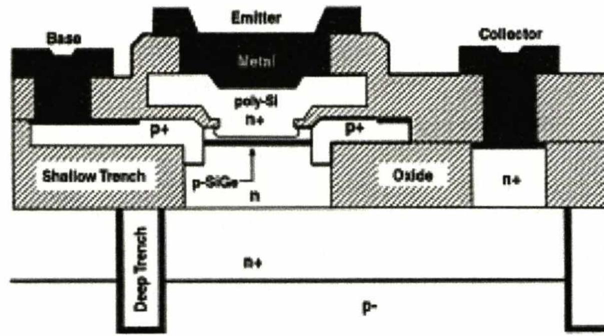



Fig 1.5 Cross sectional diagram of SiGe HBT by IBM.

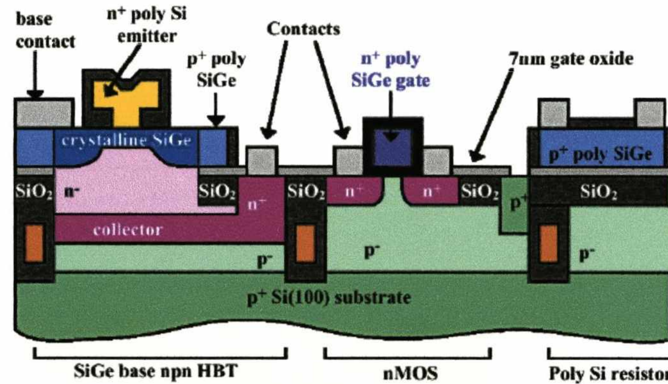



Fig 1.6 Cross sectional diagram of SiGe HBT based BiCMOS by IBM.

## 1.2.3 CMOS technology

In the past, MOSFETs were considered as slow devices because the electron mobility in Si is lower than that in GaAs; meanwhile the shortest gate length that can be achieved in MOSFETs was always longer than GaAs MESFET. However, continuous aggressive scaling of feature size not only made the MOSFETs smaller, but also much faster, so as to become qualified as good RF devices. With sub-100nm channel length, $f_T$ and $f_{max}$ are above 200 GHz for MOSFET technology [7]. Today, consumers demand wireless/RF systems to be low-cost, power efficient and reliable. High-level integration has proven in practice to be an effective way to reduce cost and achieve compactness simultaneously for high volume applications leading to entire systems on a single chip using CMOS

technology [7]. However, it has proved difficult to achieve good power amplifiers (PA) in Si. Presently, PAs with III-V compound semiconductors are still the most commonly used devices from the view of manufacturer due to lack of competition from the Si based side. In order to breakthrough this bottleneck for making wireless product fabrication more cost effective, the final challenge is now to integrate the PA, transceiver IC, digital baseband and power management module on a single silicon chip.

Next, silicon MOS devices for Pas are investigated and reviewed. Si LDMOS technology was primarily developed for RF power application [8]. A typical structure is demonstrated in Fig 1.7. The original motivation for LDMOS is to produce short channel devices that could be immune to low breakdown voltage by spatially separating the n+ drain to gate control using a lightly doped drain extension area which is often called the drift region. The limited current drivability due to long channel length and high series resistance in the LDD region have limited LDMOS transistors to an operation frequency below 5GHz. Its fabrication process is similar to standard CMOS but with added fabrication steps and hence cost.

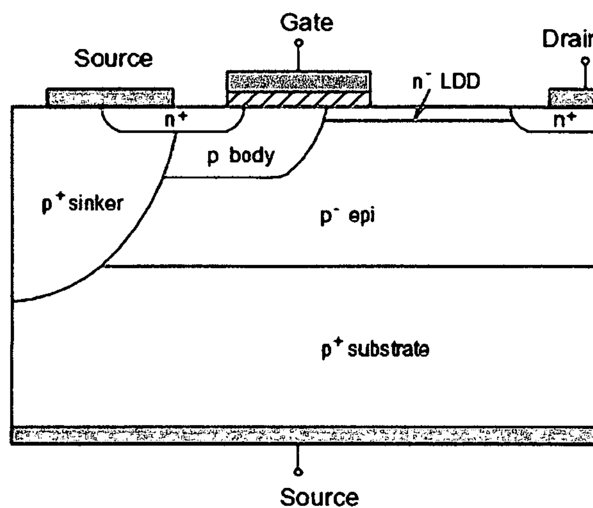


Fig 1.7 Cross sectional diagram of a typical Si LDMOS.

Silicon-on-Insulator (SOI) technology has gained momentum for RF application based on advantages associated with the high resistivity substrate which also results in low noise

and provides good linearity in low noise amplifier (LNA) circuits [9]. The ease of integrating SOI with high-resistivity substrates, normally higher than 1000 ohms-cm, reduces substrate noise coupling and losses allowing designs of on-chip inductors and varactors with more than 60% improvement in the quality factor, Q. This allows further reductions of 60% in power consumption for RF blocks. It also benefits from reduced parasitic capacitance and leakage current. A cross-sectional diagram of basic SOI is demonstrated in Fig 1.8. However, the disadvantages of floating body effects and the additional cost to eliminate them, together with the high cost and limited availability of substrates, have made SOI-CMOS technology less popular than bulk CMOS which so far has the best performance-to-cost ratio of all the device technology contenders for wireless/RF application.

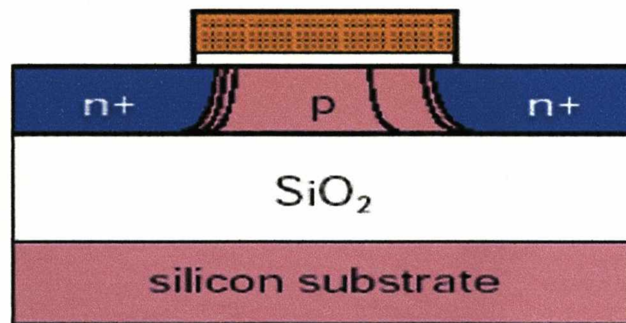



Fig 1.8 Cross sectional diagram of a typical SOI.

CMOS was originally invented purely for digital integrated circuits and in turn drives the scaling for CMOS dimensions and increasing of the intrinsic speed of high performance Micro-processor Units. The scaling road map for all physical and electrical parameters is described in the International Technology Roadmap for Semiconductor (ITRS) [10]. The ITRS has recently revised its projection for targeted printed gate length for MOSFET in high-performance logic circuit for 2003 from 80nm in 1999 to 65nm in 2003 and for 2007 the value finally has reached 42nm. Continuous MOSFET scaling has simultaneously increased the number of transistors in the increasingly complex integrated logic circuits

while reductions in device size continue. For example, in the beginning of 2008, the Intel Tukwila Micro Process Unit has reached 2 billion transistors per chip with a mainstream frequency of 2GHz compared to 2300 transistors in Intel 4004 with a speed of 1MHz in 1971 [11].

Needless to say, also benefiting from the annual scaling, wireless/RF integrated circuits implemented in CMOS are making a strong appearance. Therefore combined with significant performance improvements in the digital part, CMOS has become the dominant technology that is believed the best vehicle at present time to realise an entire system on a single chip at a reasonable cost.

However, a significant limiting factor of conventional CMOS for RF applications is associated with packaging because any parasitic PCB, packaging or bondwire in combination with ESD protection network and packaging pin capacitances will strongly degrade RF signals. From the technology point of view, in the past a major factor in compromising MOSFET RF performance was the relatively low on-current drivability and high parasitics such as gate-drain/source overlap capacitance, gate resistance, drain/source resistances and losses to the substrate.

Double gate (DG) and gate all around (GAA) technology offer the best solutions to control short-channel effects, increase the channel width and hence boost the on-current drivability. However, both the planar DG and GAA MOSFET [12, 13] require very complex fabrication processing which limits their integration within a standard CMOS process flow. Using a FinFET structure, double gate devices can be realised with a CMOS compatible process [14]. However, one drawback is that to achieve good gate to channel electrostatic coupling, the width of the silicon fins needs to be a fraction of the channel length of the devices which requires advanced sub-lithographic techniques. The devices also suffer from inhenertly high series resistance which can severely limit on-current. Defining the MOSFET in a vertical Si pillar was considered to be a very effective way to

avoid the need for exacting fabrication processes while retaining DG/GAA structure as the vertical pillar is itself a natural structure for double/surround gate architectures. Simplified views of the above mentioned structures are shown in Fig 1.9 to allow comparison. Secondly, as scaling of ordinary planar MOSFET now faces significant technology challenges, vertical MOSFETs with a channel length defined by non-lithographic methods provides further opportunities for cost reduction. There are three other main implications that make this technology attractive for RF and especially power applications. First, by defining the channel length vertically, significant increase of the packing density is allowed due to smaller footprint of each device. This feature has been exploited in Dynamic Random Access Memory (DRAM) technology where maximum packing density is a key factor. Secondly, by reducing the pillar width to the range of channel region depletion region width, partially/fully depleted devices can be achieved which can provide excellent short channel effect control, similar to the ultra-thin-body SOI MOSFET and FinFET. Lastly, despite defining MOSFET vertically, other pocket, retrograde channel and even high K dielectric technologies are still compatible within the fabrication process allowing potential for further improvements in device performance.

## 1.3 Si Based Vertical MOSFET

The recent development of vertical MOSFETs (VMOSFET) has been largely driven by two factors observed by the industry, firstly the potential as a strong non-classical CMOS contender in continuing the ITRS roadmap in 21$^{st}$ century and secondly the potential for applications in low standby power and RF devices market due to its low cost process and compatibility with CMOS technology. From the point of view of technology, the recently reported VMOSFETs can be mainly classified into two types according to the two different

fabrication processes in defining the channel and source/drain regions, namely by epitaxy and ion-implantation respectively.

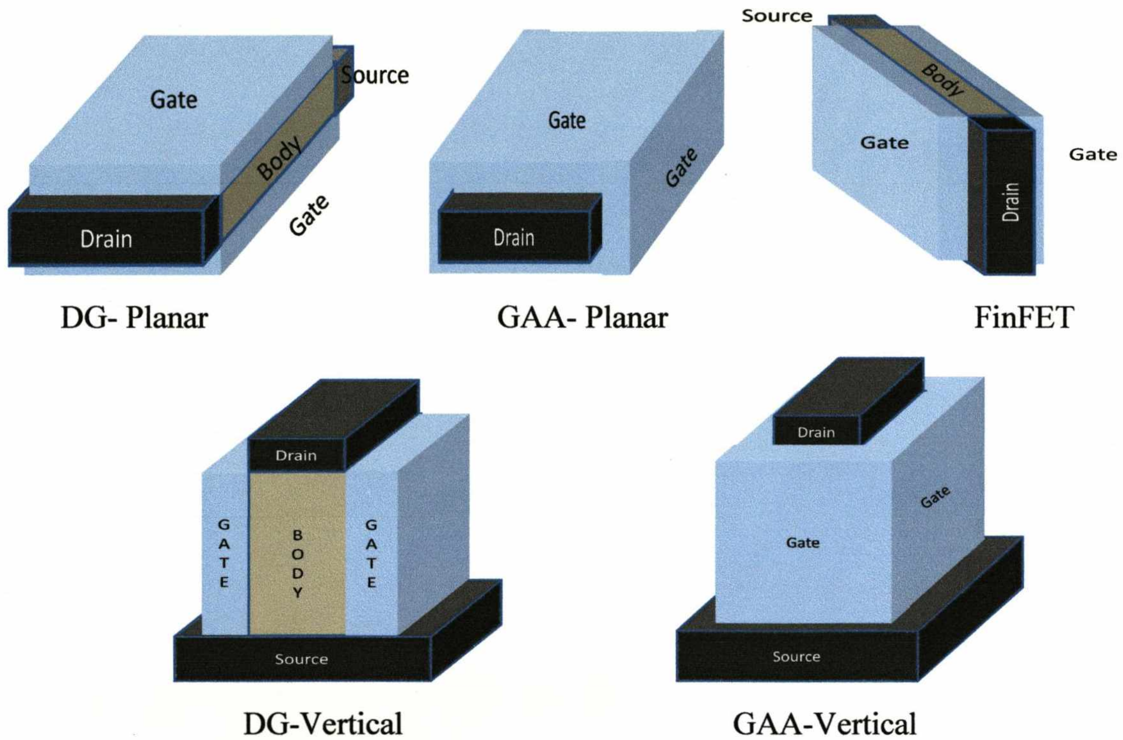



Fig 1.9 Basic structures of a Si based planar double gate, planar gate-all-around, FinFET, vertical MOSFETs with double gate and surrounded gate.

A classical epitaxially grown VMOSFET with channel length down to 70nm was reported in [15]. The channel length was precisely defined by the thickness of a silicon film using Reduced/Low-Pressure Chemical Vapour Deposition (RP/LPCVD) A cross sectional diagram of the first sub 100nm epitaxial vertical MOSFET is shown in Fig 1.10 where the thickness of the P-doped layers were chosen to provide final channel length after reactive ion etching to form the pillar. It was reported that without utilizing silicided junctions and channel engineering, the vertical pMOSFET attained a $f_T$ of 4GHz for a channel length of 130nm with uniformly doped body. Further experiments using similar process but defining channels on sidewalls with different orientations suggested that the

current in the <100> is 1.4 times higher than that in <110> [16]. The sidewall interface quality was enhanced by the deposition and etching of a sacrificial oxide layer before the

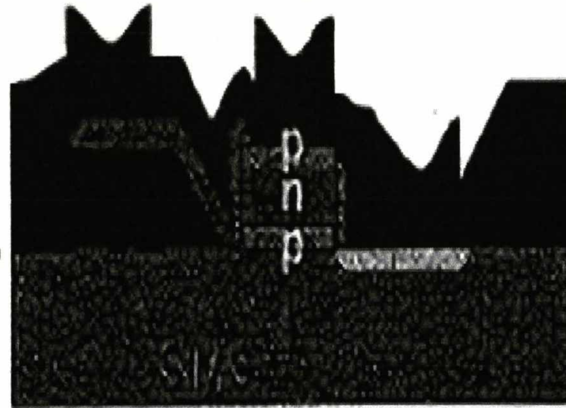



Fig 1.10 Cross sectional diagram of selectively grown epitaxial p type VMOSFET [12].

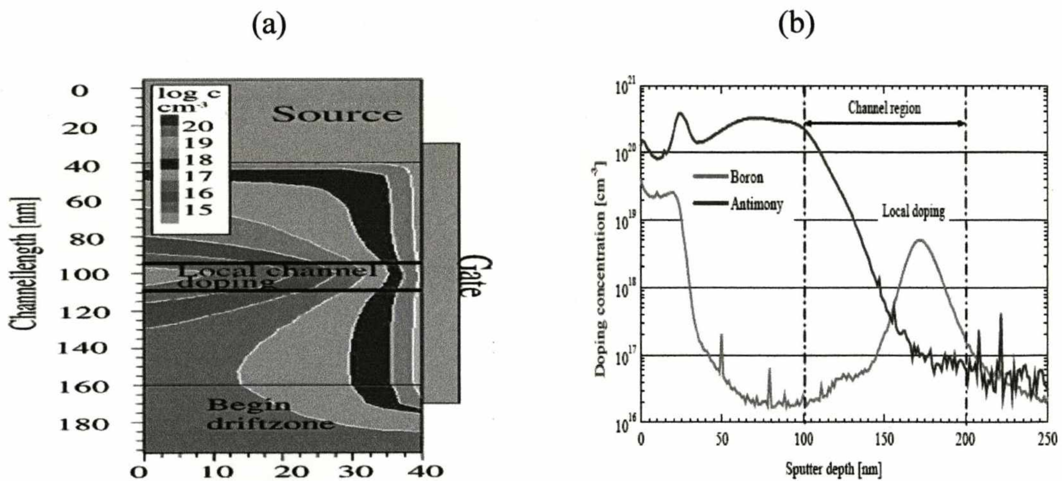



Fig 1.11 (a) Simulated electron concentration for delta local doping; (b) corresponded doping profile along the pillar height at the surface [17].

gate oxide growth. However, this device suffers from severe parasitic phenomena such as short channel effect (SCE), floating body effect and high gate-drain/source overlap capacitance.

In order to suppress the SCE without compromising on-current, a technology was later reported using Molecular Beam Epitaxy (MBE) instead of LPCVD to grow a highly doped thin layer in the center of the body as a "junction field stopper" while maintaining

homogenously doped channel region confined to the $Si/SiO_2$ interface [17, 18]. The doping profile of the delta region is shown in Fig 1.11. Compared to the entirely homogeneously doped body, this delta doping profile maintains the benefit of high mobility but also reduces hot carrier effects due to the reduced average drain electric field along the channel and thus improves the breakdown voltage and reliability. However, the application of this device in RF applications is limited because of the large overlap capacitance between the gate and the drain/source. A selective epitaxy method solves this problem by depositing the poly gate layer previously to the selective epitaxial growth of the p+np+ junctions therefore reducing the overlap regions [19]. The final structure of this sandwiched gate stack with the selective epitaxial grown body is shown in Fig 1.12. Because floating body effects still remain an important issue inducing severe parasitic bipolar effect in the aforementioned epitaxial devices, a SiGe source layer was developed to suppress hole accumulation and delay avalanche breakdown [20]. The SiGe layer is shown with the device in Fig 1.13. For an ultra short channel device, especially with p type channel, SiGeC layers were also seen as important technology to suppress the dopant diffusion from the drain and source, which would lead to a severe bulk punch through [21].

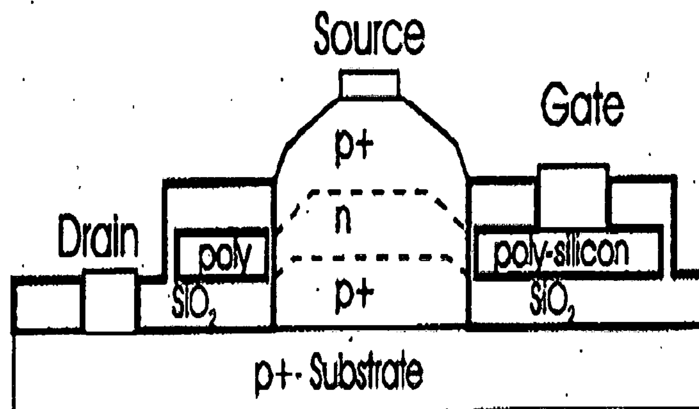



Fig 1.12 Overlap capacitance reduced by depositing SiO2/PolyGate/SiO2 layers in a selective epitaxy grown VMOSFET [16].

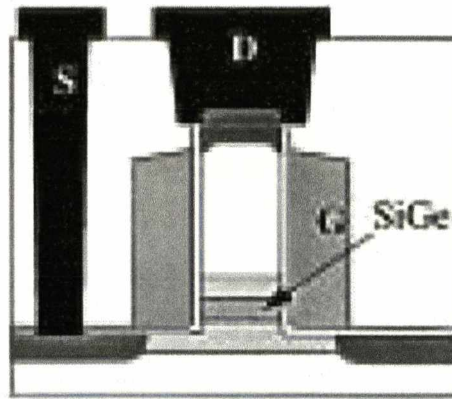



Fig 1.13 SiGe source VMOSFET for parasitic bipolar effect reduction [17].

The suppression of overlap capacitance for the epitaxial VMOSFET has also been addressed by a replacement gate process [22]. In that work, after etching of the dummy gate, the poly gate was self-aligned with the previously grown channel and therefore the overlap region was significantly reduced. In the device, the junction depth could be controlled by solid source diffusion (SSD). However, shallow junctions were still difficult to form because of the high thermal budget required for annealing. A process for threshold voltage adjustment involving only a borosilicate glass (BSG) film has been reported in [23] to allow the Si body surface doped accordingly, thus precluding the poly gate doping. The main drawbacks of using epitaxial deposition to define channel length, however, are expensive fabrication cost, poor compatibility with mainstream CMOS planar technology and thus low throughput.

VMOSFETs fabricated through an etching and implantation process were first introduced in 1991 [24] where unlike previous epitaxial processes, the channel, drain and source regions are defined by ion-implantation. The structure is shown in Fig 1.14 where a gate all around architecture was also first applied to vertical MOSFETs. In the process, a p-type well region was first formed on the (100) plane of the silicon substrate for defining the threshold voltage through boron implantation. This resulted in a nearly constantly doped substrate region for a depth of 2μm. The pillar was then formed by etching followed by a

sacrificial oxidation step to remove surface damage. The entire pillar, including the channel length was then covered by a thermally grown gate oxide and etched n type polysilicon gate. Drain and source region implantation was then carried out and the process was finished with contact hole formation and aluminium metallization. This kind of process has the advantages of simplicity and full compatibility with conventional planar CMOS technology. Moreover, other performance enhancement processes such as surround gate for higher drain current drivability, body floating effect suppression, short channel effect and gate overlap capacitance reduction have been successfully integrated without using additional epitaxy steps. The etch-implantation defined vertical MOSFETs with double gate adopted similar process and suggested that it was possible to achieve narrow pillar width for better channel control [25] which is shown in Fig 1.15.

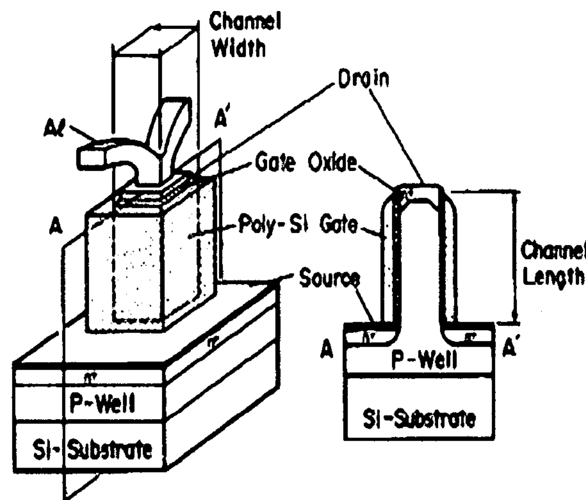



Fig 1.14 First reported ion-implanted defined vertical MOSFET with a GAA structure [24].

Advanced lithography techniques have later also been adopted to fabricate ultra-thin body with sub-50nm ridge thickness with a better quality [26, 27]. The on-current in such implanted devices can be enhanced by incorporating Ge ion implantation into the channel region followed by solid phase expitaxial regrowth [28]. As a result, the enhanced drive current is attributed to higher hole mobility in the SiGe channel. Furthermore, a narrow

band-gap source by incorporating a SiGe layer [29] at the pillar bottom proved an effective solution to suppress the floating-body effect due to the more efficient removal of charge

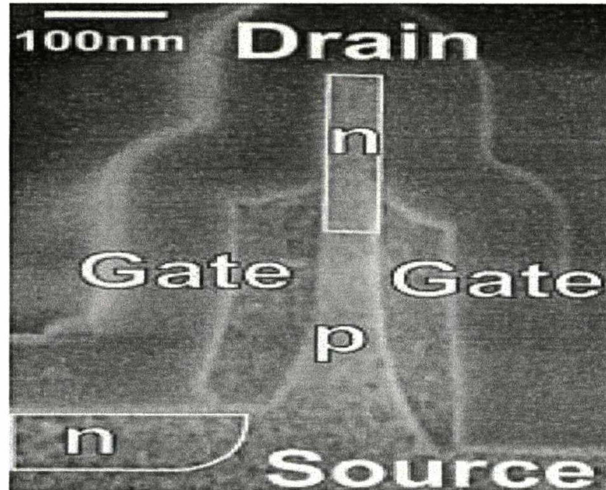



Fig 1.15 First reported ion-implanted defined ultra-thin-body vertical MOSFET with a double gate structure [25].

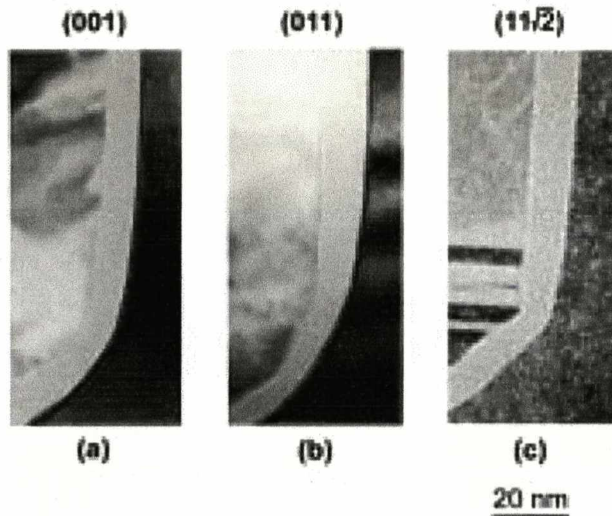



Fig 1.16 TEM picture of the gate oxide at the pillar corners featuring different surface orientations. (a) 10 nm oxide thickness at the (001) sidewall (b) 14nm oxide thickness at the (011) sidewall; (c) 12nm oxide thickness at the $11\sqrt{2}$ sidewall [30].

(holes) and less electron back injection into the body compared to conventional VMOSFET [30]. The impact of the sidewall interface orientations on the gate oxide thickness, interface state density and effective electron mass thus the inversion layer mobility, was examined in [31] where it was shown these parameters depend strongly on

the shape and orientation of the trench sidewalls. The orientation dependent oxide thicknesses are compared in Fig 1.16.

The issue of high overlap capacitance in implanted VMOSFET was addressed by using a simple self-aligned process which is less complicated than the reversed gate formation and replacement gate processes for epitaxial channel devices [32]. However, the performance of these devices was degraded by the onset of short channel effects and limited by the fact that only the overlap gate capacitance at the pillar bottom can be reduced. One proposed solution to address short channel effects was to implant a graded channel doping which has high doped end near the source [33]. In this way, the source junction barrier is enhanced that provides suppression of drain field penetration and also bulk punch through. The lightly doped drain end channel serves to increase the carrier mobility and reduce the impact ionization rate. The disadvantage of this approach is that the highly doped source end channel may have the high band to band leakage to be the device must also be biased in source on top mode to allow aforementioned benefits to be realized. A solution to address the large overlap capacitance at both top and bottom of the pillar was proposed in [34] where a poly-Si mask was used to protect the top encroaching oxide from being overetched. Therefore the remaining oxide thickness further reduced the overlap capacitance at the pillar top. More recently, an ultra thin vertical channel nMOSFET process that can improve on current and simultaneously address the short channel effect and part of the overlap capacitance was reported in [35] with an outline of the key process steps illustrated in Fig 1.17. In this device, a SiN isolation layer was used to limit the overlap capacitance regions between the top drain region and the replacement gate but the LDD drain region self-aligned underneath the gate in the vertical body still suffers from a high overlap capacitance. At the same time, the ultra thin body efficiently suppresses the SCE with the aid of a gate adjusted threshold voltage by using boron-doped poly-$Si_{0.5}Ge_{0.5}$ material and shallow junction depths which were naturally defined by the width of the

ultra-thin body. However, it also brought the problems of high series resistance due to the contact interface and ultra-shallow junction depth. Also it has poor sidewall interface quality because of the difficulty of incorporating the sacrificial oxide layer.

## 1.4 VMOSFETs in this Project

In this project, the advantage of adapting the cost-effective CMOS compatible process is maintained when fabricating Si based vertical MOSFETs defined by implantation and etch. In addition, two techniques have been integrated into the process to address the main VMOSFET draw backs, namely the large gate overlap capacitances and severe short channel effects. In previous research, a local and self-aligned oxidation process known as fillet localised oxidation (FILOX) serves to increase the oxide thickness in the gate overlap

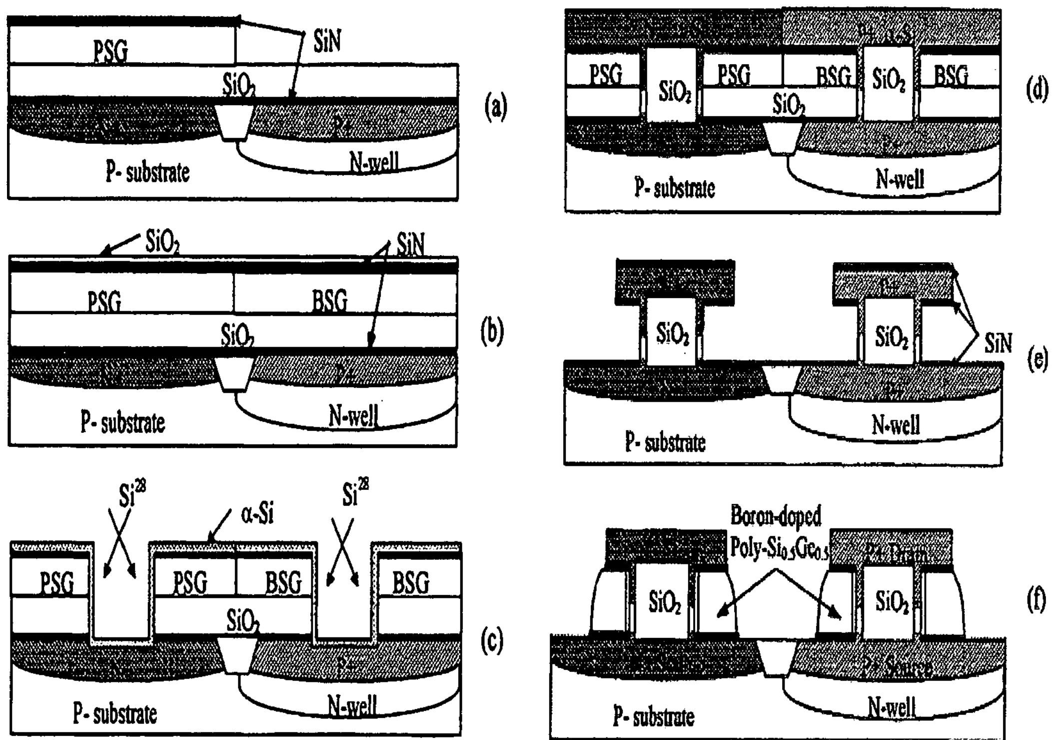



Fig 1.17 Brief fabrication process of the ultra-thin-vertical-channel MOSFET. (a) Field isolation, As/P/$BF_2$ implants, $SiO_2$ deposition, and phosphosilicate glass (PSG) formation; (b) borosilicate glass (BSG) formation; (c) Trench etching; (c) Trench etching; (d) α-Si deposition, As/$BF_2$ implants and annealing; (e) drain patterning (f) Gate formation [34].

region thus reducing the overlap capacitances both at the pillar top and bottom, was reported [36-38]. Later on, a junction stop (JS) architecture, or "dielectric pocket", was proposed by Donaghy and Hall et al. [39] which allows formation of a shallow top junction. Experimental devices were reported in [40, 41].

Fig 1.18 shows a simplified flow of the FILOX process produced by simulation [42]. As described in [34], the initial wafers were p-type <100> which were then implanted with boron followed by a drive-in annealing in dry and wet ambient for 10 and 30 minutes respectively. A light field photo-resist layer was spun onto the wafer to protect future pillar areas. After hard-baking the wafers, the pillars were anisotropically etched using HBr. The photo-resist was then removed in a plasma asher. In the following steps a thin pad oxide layer was grown and a thick nitride layer was deposited. The active area was defined using a lithography process where thick LOCOS was grown at a high temperature in a hydrogen/oxygen ambient. The nitride fillet was left on the vertical pillars after the nitride and the pad oxide was anisotropically etched. The fillet local oxidation was then performed

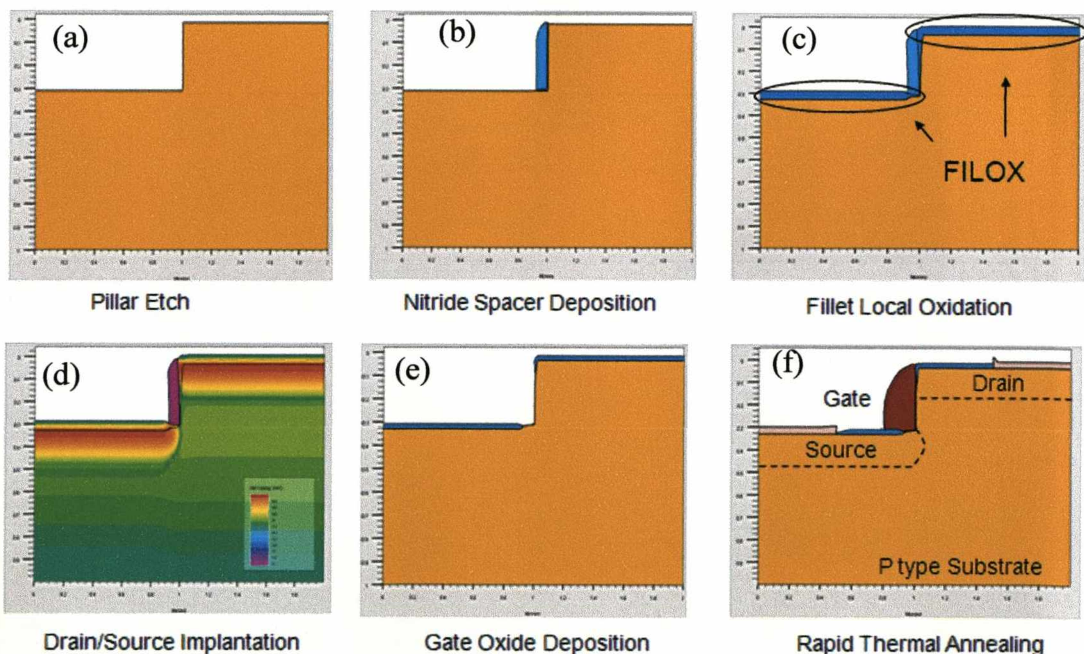



Fig 1.18 Fabrication process of an ion implanted Vertical MOSFET with a Fillet Local Oxidation (FILOX).

at a high temperature in a hydrogen/oxygen ambient allowing the oxide to become viscous. Through this self-aligned process, unlike defining oxide by lithography, the FILOX does not need to take into account any alignment tolerance and can thus grow closer to the channel without affecting the channel area. A P+ type contact ring was then implanted to contact the substrate from the surface. It was followed by drain/source implantation of arsenic where the implantation tilt angle could vary from 0 degree to 7 degree depending on the needs. During the angled implantations, four times of repeats with directions of north, south, east, west were needed to avoid shadowing effect that could prevent the dopants to reach the pillar bottom. In the next stage, the nitride fillets were removed in orthophosphric acid along with the remaining pad oxide, using HF dip etch solution for 40 second to leave the silicon sidewalls exposed. After an RCA clean, the gate oxide was grown on the pillar sidewalls. A thick, in-situ phosphorous doped polySi layer was deposited to form a uniformly doped gate. After an anisotropic poly-Si etch, the poly-Si fillets surrounding all vertical surfaces were left followed by the poly-Si removal mask lithography and isotropic silicon etch where the poly-Si filets were thinned. A rapid thermal anneal (RTA) was performed to activate implanted dopants. Finally, contact windows were etched and the probe pads and the metal tracks were deposited. Characterisation showed that for a device with 100nm channel length, 3nm gate oxide thickness and body doping of $2x10^{18}cm^{-3}$ an on-current of 100 uA/um with a off-current of $5x10^{-12}$ A/um was achieved. More importantly, the gate overlap capacitance can be reduced up to two times compared to conventional devices without FILOX if an initial 60nm FILOX have encroached into top and bottom side of the pillar.

In the design of VMOSFET with a JS, the junction stop is located between the drain and the body of the device that allows formation of shallow top junction and prevents the penetration of drain dopant into the pillar centre. The introduction of a junction stop was first proposed in a lateral MOSFET [43] as an alternative to pocket ion implantation in

order to suppress short channel effects. In this approach, the conventional pocket is substituted by buried dielectric spacers allowing uttermost part of drain/source extended as shallow junctions.

The incorporation of both a junction stop and an epitaxial layer in vertical MOSFET has its channel length defined by dry etched pillar height and the epitaxially deposited by an undoped silicon layer between the body and the polysilicon drain of the device. A time-controlled oxide over-etch provides a recessed junction stop which permits the seeding of the epitaxial channel. The fabricated vertical MOSFET with an epitaxial channel and junction stop by Takashi at all [44] indicates the possibility of this approach in providing reasonable device performance for the on-current and SCE. At the other hand however, this process also introduces a high level of complexity into the fabrication. The growth of the epitaxial channel of the device is difficult to control because of the differing orientations of sidewalls and substrate. Moreover, epitaxial growth is a low-throughput process.

A simpler approach was reported by the same team [40, 41]. The complexity is largely reduced by establishing the connection between the drain and the body of the device by a thin polysilicon spacer. At the same time the channel is free from epitaxy and simply defined by the height of the pillar and out-diffusion of the vertical junction depth from the polysilicon. The fabrication process is illustrated in Fig 1.19.

First, the 600nm thick LOCOS was used in order to define the active area of the devices on a p-type body which was formed by boron ion implantation ($5x10^{14}cm^{-2}$, 50keV), followed by a drive-in anneal. Then the junction stop layer was grown by dry thermal oxidation to a thickness of 10-20nm. A 300nm thick amorphous silicon layer was deposited by low pressure chemical vapour deposition (LPCVD). The native oxide from the pillar sidewall was removed by a short wet etch in hydrofluoric acid. An undoped amorphous silicon layer was deposited by LPCVD at 560°C in order to form the spacer

connection between the poly drain the silicon body. This is a standard, high throughput CMOS process step. The channel was then defined by anisotropic dry etch in a HBr plasma where the length was controlled by timing the dry etch. After this, a 6nm sacrificial oxidation was done at 800°C and then was selectively removed by wet etch in hydrofluoric acid to eliminate the dry etch damage from the silicon surface. Another sacrificial LTO layer was then deposited to protect the channel from the drain/source ion implantation.

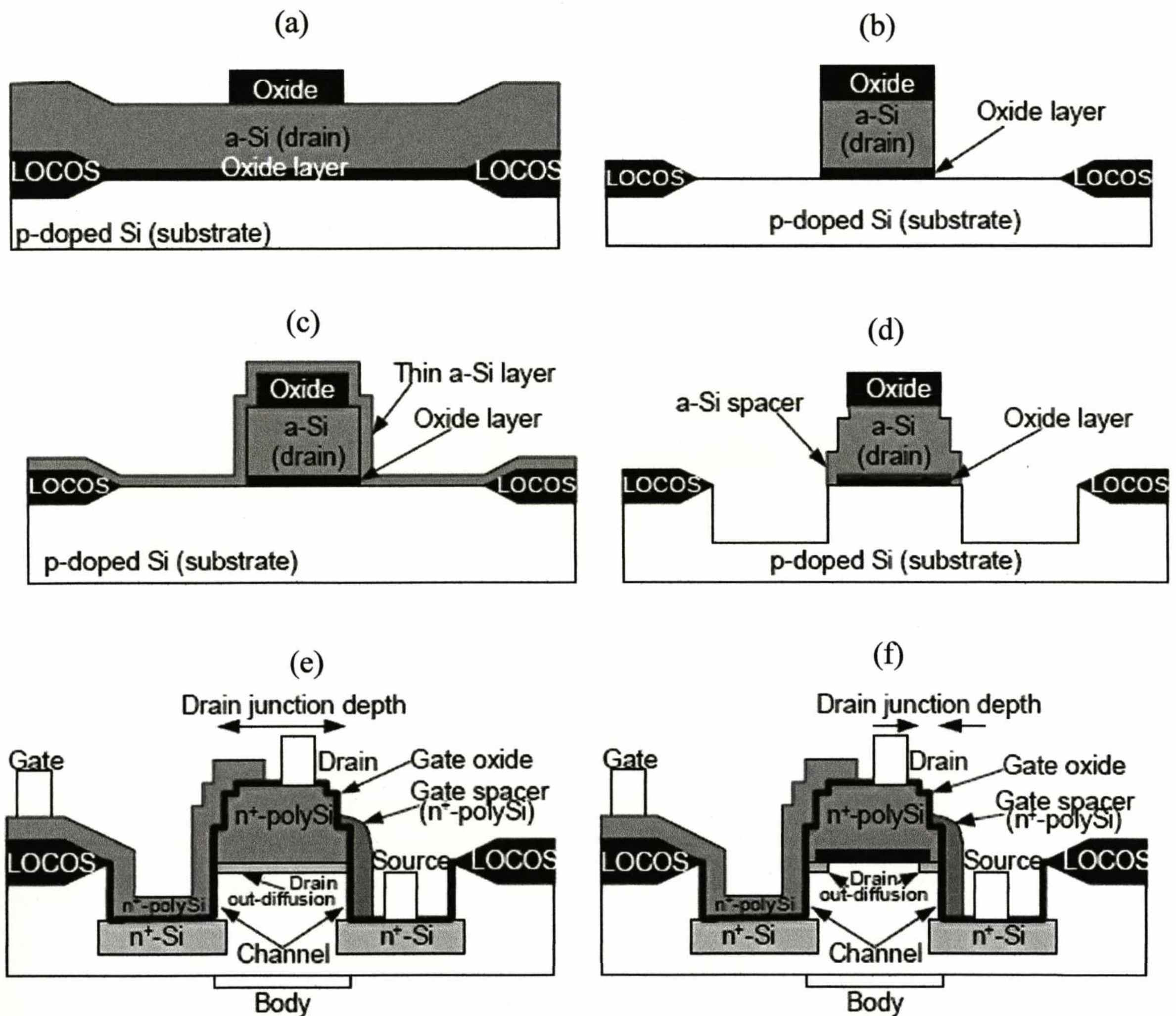



Fig 1.19 Fabrication process of an ion implanted Vertical MOSFET with a Junction Stop structure (JS) [32].

Then the sacrificial oxide layer was removed together with the LTO hard mask by wet etch in hydrofluoric acid. A 3nm gate oxide was thermally grown at 800°C followed by deposition of 100nm thick poly-Si layer, which was doped by tilted phosphorus ion

implantation. The poly-Si gate was then dry etched followed by realisation of contacts. Finally RTA (Rapid Thermal Annealing) at 1050°C for 20 sec was performed for dopant activation. The process finished with standard back end metallization process.

## 1.5 Summary

Nowadays, wireless networks have reached almost every corner of the world through cell phone network, WiFi, Bluetooth, GPS and other forms. In the semiconductor industry, the wireless-chip has overtaken the wire line-chip market in 2007 and is still growing with an increasing rate annually driven by the demand for more advanced wireless technology, for example 3G. Although silicon bipolar RF transistors were predominantly used until 1995, silicon RF MOSFETs have now become the dominating force in the market and have completely displaced bipolar in network base-stations. The trends of being more cost-effective and hence capable to integrate with the digital block have further made CMOS compatible Si RF devices relatively more attractive compared to GaAs HBT and HEMT, SiGe HBT, SOI, LDMOS and SiGe BiCMOS. In principle, vertical MOSFETs offer the potential to replace advanced planar devices whilst maintaining its advantage of cost effectiveness. Two fabrication routes have been reported. The first one is to use selective epitaxy to grow the required layer sequence. The interface between the epitaxial layer and the mask for epitaxy is used as the active area. The second method is to define the drain-channel-source by implantation. The sidewall of pillars is used as the active area. The literature has suggested that vertical MOSFET defined by ion-implantation and etch offers the best route for process compatibility and also for maximizing the RF performance to cost ratio. Innovations have been applied to the conventional VMOSFET structure, such as

surround gate, junction top and FILOX architecture, to enhance device performance and suppress inherent disadvantages.

In this project, the essential goal is to examine the feasibility of CMOS technology compatible vertical MOSFETs developed based on the previously proposed technologies developed by collaboration between Liverpool and Southampton Universities, for RF applications. The measurement and analysis results of this collaboration will be discussed and presented in this thesis

In Chapter 2, the theory of long and short channel MOSFETs along with some concepts associated with RF aspects and compact modelling are described. The characterisation of experimental VMOSFETs with a junction stop (VMOSFET-JS) followed by related device simulation studies to explain the results, are presented in Chapter 3. In Chapter 4, the influence of the junction stop (JS) for suppressing SCEs in a sub-100nm channel length device is studied using numerical simulation, in some detail. The simulation study provides physical insight into the influence of junction depth on SCEs, in particular for the case of the asymmetric junctions inherent in vertical devices. In Chapter 5, the feasibility for integrating ultra-thin body and retrograde body with FILOX technology are examined. Chapter 6 investigates the influence of drain and source series resistance on $f_T$ in short channel VMOSTFETs with FILOX (VMOSFET-FILOX). An analytical model is developed and compared with numerical simulations. Proposals are made for modifications to the fabrication process to mitigate high series resistances. In Chapter 7, the $f_T$ characteristics of second batch VMOSFET-FILOXs with a range of layouts are measured across the wafers. A maximum $f_T$ of 8.6GHz was found while the simulation suggested that the $f_T$ can go up to 30.5GHz. Factors that limit the $f_T$ in these devices are found to arise from contact resistance, large overlap capacitance in frame gate design and high junction sheet resistance. These are indentified with the assistance of process-generated 2D and 3D numerical models. Simulation also shows that with 0.35μm

lithography stepper, up to three-generation-hop in $f_T$ can be ultimately achieved with VMOSFETs if 50nm channel length is targeted using the junction abruptness required by ITRS road map. In Chapter 8, the extraction of EKV model parameters for both DC and AC aspects on a double gate contact VMOSFET-FILOX with a 100nm channel length is presented with some modelling issues identified and discussed. The thesis is concluded in Chapter 8 which also contains suggestions for further work.

# Chapter 2

# Theoretical Considerations

## 2.1 Introduction

The underlying theory for MOSFET operation, oxide conduction mechanisms and RF performance merits, are presented in this chapter to provide the necessary context for the interpretation of associated work on device characterisation, analytical, numerical and compact modelling. Particular attention is given to the short channel effects in MOSFETs as these are studied in some detail in later chapters for both device design and also interpretation of experimental results. Theory regarding to oxide conduction is also important as it prepares for characterisation on devices where there are particular challenges in realising good quality gate oxides on the etched, vertical pillars which constitute the device channels. The principles of device RF performance assessment and modelling are also introduced through the RF figures of merit, $f_T$, $f_{max}$ and the device equivalent circuit at RF.

## 2.2 Basic Current-Voltage Characteristics in Long Channel MOSFET

In a long, n-channel MOSFET, when no voltage is applied to the gate, there is no current flowing between the drain and source. Under these conditions, the MOSFET acts like two back-to-back diodes with only a low level of drain junction related leakage current. When a sufficiently large positive voltage is applied to the gate, the silicon surface is inverted into n-type which forms a conducting channel between the n+ source and drain. The gate voltage induces minority carriers into the inversion layer while the drain voltage

establishes a lateral electric field which causes charge to drift along the channel. The basic structure of MOSFET operation in inversion is illustrated in Fig 2.1.

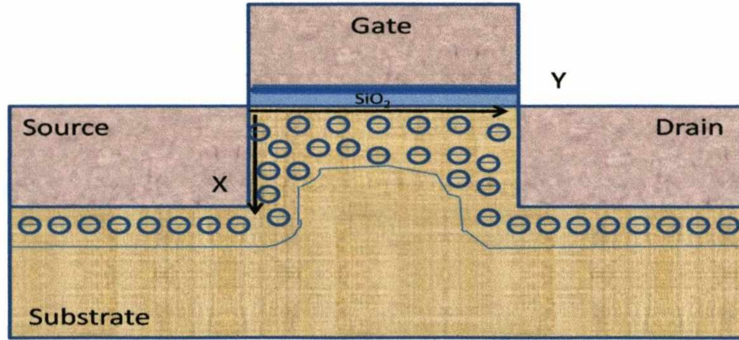



Fig 2.1 Basic structure of an nMOSFET. "Y" direction is along the channel; "X" direction is perpendicular to the channel.

## 2.2.1 Universal Drain-Current Model

The inversion layer in an n-channel MOSFET can be considered as homogeneous n-type silicon with an average, free-electron volume density, n. By neglecting any hole current component, the drift current density in the inversion layer under a lateral electric field $\xi_n$ gives

$$J_{n,drift} = q \cdot n \cdot \xi_n \cdot \mu_{eff} \qquad \text{Eq. 2.1}$$

where q is electronic charge equal to $1.6\text{x}10^{-19}$ C, $\mu_{eff}$ is an effective electron mobility in the inversion layer.

If the carrier concentration is not uniform along the channel, carriers will diffuse under the influence of the concentration gradient. The diffusion current density is

$$J_{n,diff} = k \cdot T \cdot \mu_{eff} \cdot \frac{dn}{dY} \qquad \text{Eq. 2.2}$$

where Y is the lateral distance along the inversion layer, k is Boltzmann's constant, T is the absolute temperature.

The total current density in the inversion layer from the source to the drain is the sum of the drift and diffusion current densities:

$$J_n = q \cdot n \cdot \xi_n \cdot \mu_{eff} + k \cdot T \cdot \mu_{eff} \cdot \frac{dn}{dY} \qquad \text{Eq. 2.3}$$

Hole current and the generation and recombination currents are assumed to be negligible in the channel region due to the very low level of majority carriers in the vicinity of the channel.

By considering the electrostatic effect of the lateral electric field (Y direction only), an expression for the drain current density can be derived using the 1D Poisson equation. Then the current density is related to quasi-Fermi potential V as in [45]:

$$J_n = -q \cdot n \cdot \mu_{eff} \cdot \left(\frac{d\psi_s}{dY} - \frac{k \cdot T}{q \cdot n} \cdot \frac{dn}{dY}\right) = -q \cdot n \cdot \mu_{eff} \cdot \frac{dV}{dY} \qquad \text{Eq. 2.4}$$

where $\psi_s$ is the surface potential and V is the quasi-Fermi potential for electrons along the channel.

The general drain current model assumes a gradual channel approximation (GCA) which first considers that the variation of the electric field along the channel is much larger than the corresponding variation perpendicular to the channel. This allows the use of Poisson's equation in the 1D form, to derive the inversion layer charge density. The inversion charge can then be associated with the gate bias by considering the continuity of the displacement vector across the gate oxide/substrate boundary. In the following derivations, the source electrode is taken as connected to the body electrode and also to ground. By integrating equation 2.4 with respect to the drain bias,

$$I_D = \mu_{eff} \cdot \frac{W}{L} \cdot \int_0^{V_D} [-Q_{inv}(V)] dV \qquad \text{Eq. 2.5}$$

where W is the channel width, L is the effective channel length, $\mu_{eff}$ is the effective mobility which is a function of vertical and lateral electric field and is assumed to be constant along the channel, $V_D$ is the bias applied to the drain electrode, $Q_{inv}(V)$ represents the inversion layer charge density which varies along the channel.

It is further assumed that the inversion layer charge is located at the silicon surface as a sheet of charge and there is no potential drop or band bending across the inversion layer:

the so-called charge-sheet approximation [45]. After the onset of the inversion layer at $\psi_S = 2\psi_B + V$, considering $Q_{inv}(V) = Q_s(V) - Q_d(V)$ the drain current can then be expressed as

$$I_D = \mu_{eff} \cdot \frac{W}{L} \cdot \int_0^{V_D} [-(Q_s(V) - Q_d(V))] dV \qquad \text{Eq. 2.6}$$

where $Q_S$ is the total charge density per unit area in the substrate side induced by the gate, $Q_d$ is the depletion region charge density per unit area under the gate,

$$Q_s = -C_{ox}(V_G - V_{fb} - 2\psi_B - V) \qquad \text{Eq. 2.7}$$

where $C_{ox}$ is the gate oxide capacitance per unit area, $V_{fb}$ is the flatband voltage; $2\psi_B$ is the Fermi potential condition for the onset of surface inversion.

The depletion region charge density under the gate can be related to the surface potential at the threshold voltage condition using

$$Q_d = -qN_a W_{dm}^0 = -\sqrt{2\varepsilon_{si} q N_a (2\psi_B + V)} \qquad \text{Eq. 2.8}$$

where $N_a$ is the acceptor density in the silicon substrate; $W_{dm}^0$ is the long channel depletion region width under the gate at the threshold condition; $\varepsilon_{si}$ is dielectric constant of silicon. Equation 2.6 is integrated with the above definitions for $Q_s$ and $Q_d$, the drain current is related to the gate and the drain voltages as follows:

$$I_D = \mu_{eff} \cdot \frac{W}{L} \cdot C_{ox}[\left(V_G - V_{fb} - 2\psi_B - \frac{V_D}{2}\right) V_D - \frac{2\sqrt{2\varepsilon_{si} q N_a}}{3C_{ox}} [(2\psi_B + V_D)^{\frac{3}{2}} - (2\psi_B)^{\frac{3}{2}}]] \qquad \text{Eq. 2.9}$$

## 2.2.2 I-V Characteristics in the Linear and Saturation Regions

The equation 2.9 can be expanded into a power series in $V_D$. Keeping the first two terms, a good approximation to the drain current is given by

$$I_D = \mu_{eff} \cdot \frac{W}{L} \cdot C_{ox}[\left(V_G - V_{fb} - 2\psi_B - \frac{\sqrt{2\varepsilon_{si} q N_a 2\psi_B}}{C_{ox}}\right) V_D - \frac{m}{2} V_D^2] \qquad \text{Eq. 2.10}$$

The three terms following $V_G$ can be grouped as the threshold voltage

$$V_T = V_{fb} + 2\psi_B + \frac{\sqrt{2\varepsilon_{si}qN_a 2\psi_B}}{C_{ox}} \qquad \text{Eq. 2.11}$$

m is the body effect coefficient which typically lies between 1.1 and 1.4.

$$m = 1 + \frac{\sqrt{\varepsilon_{si}qN_a/4\psi_B}}{C_{ox}} \qquad \text{Eq. 2.12}$$

m can be expressed as a sub-threshold slope factor Ss which is defined as the voltage to produce an increase in $I_D$ of one decade; that is, $Ss = m\frac{kT}{q}\ell n(10)$. Thus Ss describes the sensitivity of drain current to gate bias below threshold voltage and is usually expressed as mV/decade.

If the applied drain voltage, $V_D$ satisfies the condition: $V_D \ll V_G - V_T$, then the drain current can be simplified to

$$I_D \approx \mu_{eff} \cdot \frac{W}{L} \cdot C_{ox}(V_G - V_T)V_D \qquad \text{Eq. 2.13}$$

that is, there is a linear relationship between drain current and voltage for a given gate voltage. This explains why this regime of operation can be termed 'ohmic'.

The drain current saturates in value when the drain bias is increased such that a condition where the charge density at the drain end of the channel is zero occurs. This corresponds to a condition of zero vertical electric field in the oxide near to the drain end of the device. Analytically, the condition occurs when the product of quasi-Fermi potential at the drain end and the body factor, $m \cdot V_D$, equals to or higher than $V_G - V_T$. Further increase of the drain voltage does not further increase the drain current as predicted by equation 2.10 but in fact predicts a decrease in current after $V_D = \frac{V_G - V_T}{m}$. This condition is unphysical and in reality, the charge to voltage relationship does not behave as equation 2.10 for $V_D > \frac{V_G - V_T}{m}$. The additional drain voltage drops across the depletion region at the drain end of the channel. So when the drain current saturates, equation 2.10 reaches its maximum at ($V_D = \frac{V_G - V_T}{m}$) and thereafter becomes independent of $V_D$ as shown in Eq.2.14:

$$I_D = \mu_{eff} \cdot \frac{W}{L} \cdot C_{ox} \frac{(V_G - V_T)^2}{2m} \qquad \text{Eq. 2.14}$$

where $V_G$ can be related to the surface potential $\psi_s$ through

$$V_G = V_{fb} + \psi_s + \frac{\sqrt{2\varepsilon_{si} q N_a \psi_s}}{C_{ox}} \qquad \text{Eq. 2.15}$$

Eq.2.15 arises from the consideration of the continuity of the displacement vector across the oxide/semiconductor boundary (see also the derivation of equation 2.5) and also using Poisson's equation to relate the semiconductor electric field to the surface potential. It can be seen from equation 2.15 that increasing the gate bias causes the surface potential to increase hence increasing the drain current.

## 2.2.3 I-V Characteristics in the Sub-threshold Region

The charge in the substrate can also be related to the surface potential by solving Poisson's equation [45] and applying Gauss's law to give:

$$-Q_s = \varepsilon_{si}\xi_s = \sqrt{2\varepsilon_{si} kTN_a}\,[\frac{q\psi_s}{kT} + \left(\frac{n_i}{N_a}\right)^2 e^{\frac{q(\psi_s - V)}{kT}}]^{1/2} \qquad \text{Eq. 2.16}$$

where $\xi_s$ is the vertical electric field in the semiconductor and $n_i$ is the intrinsic carrier density. The first term in the square bracket arises from the depletion charge density while the second term, is from the free charge density.

When the device is operating in the sub-threshold region, it is assumed that the free charge density is relatively small. The total substrate charge density, which is also the inversion layer charge density, can be expressed as

$$Q_{inv} = -\sqrt{\frac{\varepsilon_{si} q N_a}{2\psi_s}} \left(\frac{kT}{q}\right)\left(\frac{n_i}{N_a}\right)^2 e^{q(\psi_s - V)/kT} \qquad \text{Eq. 2.17}$$

Therefore substituting $Q_{inv}$ into equation 2.5, the drain current in the sub-threshold region is obtained as;

$$I_D = \mu_{eff} \cdot \frac{W}{L} \cdot \sqrt{\frac{\varepsilon_{si} q N_a}{2\psi_s}} \left(\frac{kT}{q}\right)^2 \left(\frac{n_i}{N_a}\right)^2 e^{\frac{q\psi_s}{kT}} (1 - e^{\frac{-qV_D}{kT}}) \qquad \text{Eq. 2.18}$$

The surface potential is related to gate bias by equation 2.15.

For $\psi_B < \psi_s < 2\psi_B$, $V_G$ is seen to obey a linear relationship with $\psi_s$ with gradient given by the body factor, m. $I_D$ can then be related to the gate bias by an exponential term.

$$I_D \propto e^{\frac{qV_G}{mkT}} \qquad \text{Eq. 2.19}$$

## 2.3 Short Channel Effects

### 2.3.1 Charge Sharing and Drain Induced Barrier Lowering

The essential effect caused by shortening of the transistor channel length, is that the penetration of the lateral electric field from the drain and source increases the magnitude of the surface potential along the channel region or alternatively, it reduces the barrier height for carrier injection into the channel. In the sub-threshold regime, the mobile carrier density in the channel under the gate is negligible compared to the ionized acceptor concentration, $N_a$ in the depletion region therefore the vertical electric field is mainly determined by $N_a$. The influence of the vertical and lateral electric field can be interpreted by examining the two-dimensional Poisson's equation (2.20 and 2.21) which describes the potential and field relationship to charge in the depletion region. The vertical direction X and lateral direction Y are marked out in Fig 2.1,

$$\frac{d^2\psi(Y,X)}{dX^2} + \frac{d^2\psi(Y,X)}{dY^2} = \frac{qN_a}{\varepsilon_{si}} \qquad \text{Eq. 2.20}$$

Or

$$\frac{d\xi_s}{dX} + \frac{d\xi_s}{dY} = \frac{qN_a}{\varepsilon_{si}} \qquad \text{Eq. 2.21}$$

where $\xi_s$ is the vertical electric field in the depletion region under the gate.

The first part of equation 2.20 and 2.21 on the left hand side is controlled by the gate field in the vertical direction while the second part is controlled by the source-drain field in the lateral direction. Consequently in the short channel MOSFET, the barrier height at the source can be reduced further by the lateral field and not only by the vertical field induced from the gate-source bias.

The charge sharing effect (CS) is related to the lowering of the threshold voltage by the contribution of the built-in potentials of source and drain junctions, to the depletion region under the gate, at low drain bias. The physical picture is that under very low drain bias, the built-in potential of the drain and source depletion regions contribute about equally to the depletion region under the gate. This is demonstrated by Fig 2.2 where the arrows represent the electric field strength. For a shorter channel length, the laterally supported depletion regions constitute a greater portion of the total depletion region under the gate. As a result, less gate bias is needed to support the depletion region with the consequence that the threshold voltage is reduced.

The shift of the threshold voltage is due to the charge sharing between the gate and drain/source. However, the division of depletion charge between the gate and the source and drain is somewhat arbitrary. The short channel sub-threshold theory states that the minimum surface potential along the channel determines the minority injection rate and also the minimum depletion region width under the gate at the threshold condition $W_{dm}$. The minimum surface potential can be found at the channel location corresponding to $W_{dm}$ and therefore is also the location of the maximum source barrier height as depicted in the band diagram of Fig 2.3.

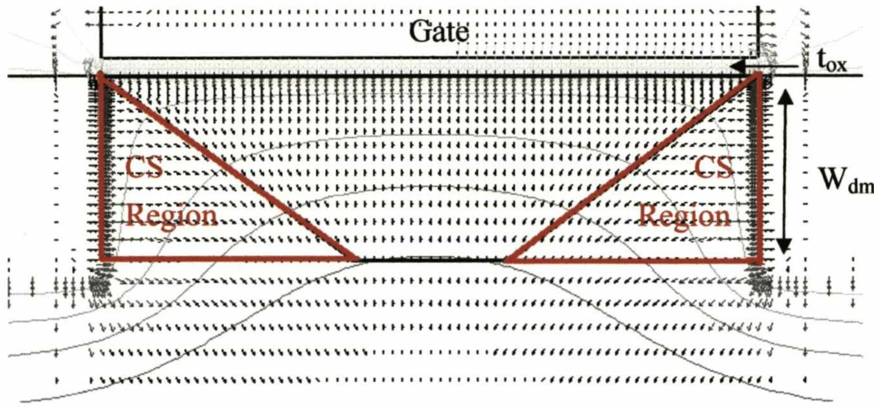



Fig 2.2 The electric field contours in a lateral MOSFET with a gate bias above threshold voltage and with low drain bias. The charge sharing (CS) effect is defined in a symmetric-junction structure, where the triangle regions are depletion charges supported by the drain and source alternatively reducing the gate supported depletion charge which is seen to shrink to a trapezoid region.

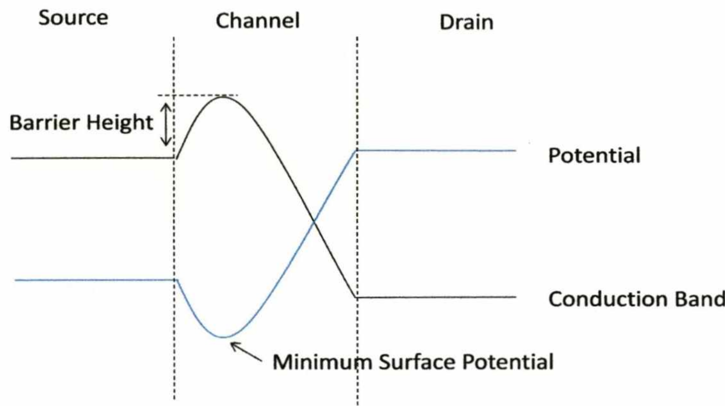



Fig 2.3 Potential and band diagram along the channel where the magnitude and the position of minimum surface potential determine these values for the source barrier height.

Therefore the threshold voltage shift is considered in terms of a shift of the minimum surface potential $\Delta\psi_{min}$. By differentiating equation 2.15, an expression for the factor m, can be obtained in the form:

$$\frac{\partial V_G}{\partial \psi_{min}} = 1 + \frac{3t_{ox}}{W_{dm}} = m \qquad \text{Eq. 2.22}$$

where $W_{dm}$ is labelled in Fig 2.2. It is defined as equal to $\sqrt{\frac{2\varepsilon_{si}\psi_{min}}{qN_a}}$ in this case. The factor of 3 in equation 2.22 arises from the ratio of the dielectric constants of semiconductor and oxide. If $\psi_{min}$ is not known, the value of $W_{dm}$ can still be estimated iteratively with

relation to the long channel depletion region width $W_{dm}^{o}$, channel length and oxide thickness according to the equation 2.23, as presented in [46].

$$\frac{W_d}{W_{dm}^{o}} = 1 + 4\left(\frac{W_{dm}^{o}}{W_d+3t_{ox}}\right)\left(\frac{\sqrt{\psi_{bi}(\psi_{bi}+V_D)}}{\psi_s^{o}}\right)e^{-\pi L/2(W_d+3t_{ox})} \quad \text{Eq. 2.23}$$

The product of the shift of the minimum surface potential due to the lateral field which is in the square bracket in Eq. 2.24 and body factor, m, gives a useful expression for the threshold voltage shift due to the influence of the lateral electrical field [46],

$$\Delta V_T = \left[\frac{24t_{ox}}{W_{dm}+3t_{ox}}\sqrt{\psi_{bi}(\psi_{bi}+V_D)}e^{-\pi L/2(W_{dm}+3t_{ox})}\right]\cdot m \quad \text{Eq. 2.24}$$

where $\psi_{bi}$ is the p-n junction built-in potential.

Because of the exponential factor in equation 2.23, the threshold shift is very sensitive to the factor $W_{dm}$. As a 'rule of thumb', to avoid excessive short channel effects, the value of channel length should be at least 2-3 times that of $W_{dm}$. The charge sharing effect is quantified by subtracting the threshold voltage in the short channel device to that of the long channel device, typically with $V_D$=50mV.

Under the off-condition, the source barrier height prevents carrier injection from the source over the barrier. When the drain bias is high, however, the minimum surface potential is further increased; hence the source barrier height is, in turn, lowered to the same degree. This latter effect is referred to as drain-induced barrier lowering (DIBL). The consequent shift in threshold voltage caused by this drain field penetration can be estimated from equation 2.23 by substituting a large $V_D$.

Alternatively, the DIBL can be evaluated from the gate voltage shift in the transfer characteristics of high drain biases of 1V at zero gate bias and low drain bias of 50mV at a gate bias for the same sub-threshold drain current.

## 2.3.2 Sub-threshold Slope Degradation

In the short channel device, the sub-threshold slope factor term, Ss is modified to better model the short channel effects and is given by equation 2.25. The term in the square bracket describes the degradation of the surface potential variation sensitivity to the gate bias , as presented in [46].

$$Ss \approx 2.3m\frac{kT}{q}\left[1 + \frac{11t_{ox}}{W_{dm}} e^{\frac{-\pi L}{2(W_{dm}+2t_{ox})}}\right] \qquad \text{Eq. 2.25}$$

The above equation shows the sensitivity of Ss to the variation of the minimum surface potential which dictates the value of $W_{dm}$.

## 2.3.3 Channel Length Modulation and Velocity Saturation

As the drain-source voltage $V_{DS}$, is increased beyond the saturation voltage $V_{DSAT}$, the surface channel starts to pinch-off at the drain end and then moves towards the source end as $V_{DS}$ is increased. The voltage difference $V_D$ - $V_{DSAT}$ is dropped across the region between the saturation point and the drain. The effective channel length is shortened by a fraction, $\Delta L$. which is the distance between the pinch-off (saturation) point and the drain end. $\Delta L$ is referred to as the degree of channel length modulation (CLM) by the drain voltage. The voltage difference $V_D$ - $V_{DSAT}$ is dropped across the region between the saturation point and the drain. The drain current is then increased by a factor of $(1 - \Delta L/L)^{-1}$.

$$I_D = \frac{I_{DSAT}}{1-(\frac{\Delta L}{L})} \qquad \text{Eq. 2.26}$$

Where $I_{DSAT}$ is the current at the voltage $V_{DSAT}$. The drain current above $V_{DSAT}$ continues to increase as a result of the decreasing effective channel length with increasing drain bias.

Short channel MOSFETs also experience a lowering of saturated drain current as a result of the saturation of the carrier velocity. When the field strength along the surface is low enough, the carrier velocity increases with the electric field strength according to Ohm's Law. When the field strength becomes comparable to or greater than a critical field, $\xi_c$ the velocity of the carriers no longer increases with field but saturates at a constant level, $\upsilon_{sat}$ which is related to $\xi_c$ by

$$\xi_c = \frac{\upsilon_{sat}}{\mu_{eff}} \qquad \text{Eq. 2.27}$$

In order to maintain a constant saturation velocity, the effective mobility needs to decrease with increasing electric field strength so that the saturation drain current no longer obeys equation 2.14, rather it becomes

$$I_D = \frac{\mu_{eff}}{1+\frac{\mu_{eff} V_D}{\upsilon_{sat} L}} \cdot \frac{W}{L} \cdot C_{ox} \frac{(V_G - V_T)^2}{2m} \qquad \text{Eq. 2.28}$$

where $\mu_{eff}$ is lowered by a factor of $1 + \frac{\mu_{eff} V_D}{\upsilon_{sat} L}$ to account for the velocity saturation effect.

As a result, velocity saturation tends to lower the drain saturation current and this lowering effect becomes more significant as the channel length is scaled further. Additionally, the drain current reaches saturation at a lower value of $V_D$ in the short channel device than in a long channel device as a result of velocity saturation. The above velocity saturation phenomenon is restricted to the drift-diffusion model, which treats carrier transport in thermal equilibrium with the silicon lattice. However, the drift-diffusion model breaks down under sufficiently high field because a fraction of carriers may acquire kinetic energy higher than kT as a result of non-localized scattering. So it is possible that the carrier velocity exceeds $v_{sat}$ and this is a phenomenon known as velocity overshoot.

## 2.4 Avalanche Breakdown

When the electric field in the drain region exceeds mid-$10^5$ V/cm, impact ionization takes place close to the drain, leading to an abrupt increase of drain current. The breakdown process happens when carriers gain sufficient kinetic energy from the field as they move along the channel and collide with bound majority carriers in the drain side of the channel, to generate secondary electrons and holes. The generated minority carriers add to the drain current while the majority carriers flow through the body to the substrate contact. The current flow through the bulk substrate resistance induces a potential drop which serves to reduce the threshold voltage and hence increases the channel current which in turn, increases the breakdown current. The forward bias can also significantly forward-bias the source junction to allow carriers to be injected into the substrate. A fraction of these will be collected by the reverse-biased drain. Thus a positive feedback process is initiated. In effect, a parasitic bipolar transistor appears in parallel with the MOSFET. Breakdown often results in permanent damage to the MOSFET as large amounts of hot carriers are injected into the oxide particularly in the gate-to-drain overlap region.

## 2.5 Off-state Drain-source Leakage

When a deep sub-micron MOSFET is biased in the off-state, there are four major mechanisms contributing to the total drain-source leakage. A schematic diagram showing these leakage currents is illustrated in Fig 2.4.

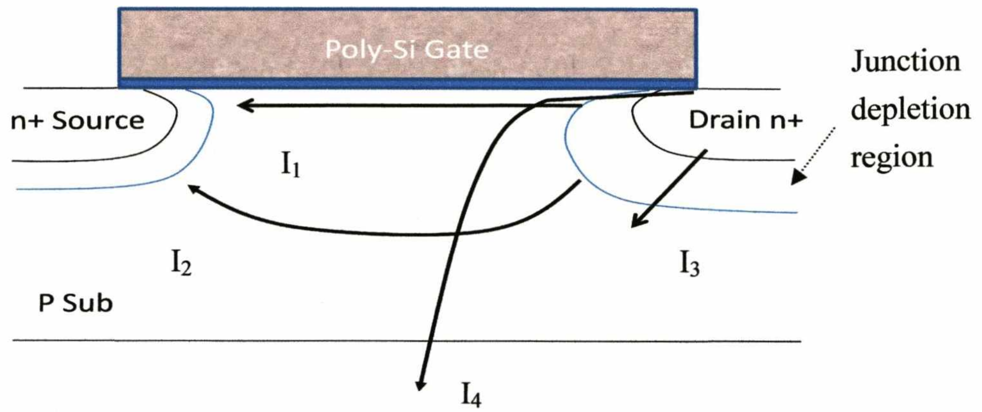



Fig 2.4 Drain/source junction leakage mechanism in deep sub-micron

The current $I_1$ is the sub-threshold conduction and the $I_2$ represents the bulk-punch-through [47]. The diode leakage current $I_3$, has the two components, namely electron-hole pair thermal generation in the depletion region [48] and also electron tunnelling from the p-region into the n-region if both regions are heavily doped [45]. The band-to-band or Zener tunnelling occurs when the electric field across a reverse-biased p-n junction approaches $10^6$V/cm causing a significant number of electrons to tunnel from the valence band in the p-region to the conduction band of the n-region. A further leakage mechanism arises for the case of increasing negative gate bias as the electric field underneath the gate oxide in the overlap drain depletion region also increases causing a narrowing of the associated depletion region width. In this region, the probability of band-to-band tunnelling of electrons becomes higher due to the intensified field strength, and consequently the drain current is seen to increase with gate bias. This extra leakage that is intensified by the vertical gate field, is termed gate induced drain leakage, GIDL ($I_4$) [48, 49]. GIDL is an important mechanism in determining the storage node discharging in the DRAM trench transistors [50]. The basic model of GIDL, which was proposed by [51], is based upon equation 2.29,

$$I_D = Aa \cdot \xi_{max} e^{-\frac{Bb}{\xi_{max}}} \qquad \text{Eq. 2.29}$$

where Aa and Bb are the constants associated with the effective mass and the energy band gap, $\xi_{max}$ is the maximum electric field within the gate induced depletion region at the Si/$SiO_2$ interface in the proximity of the drain junction.

## 2.6 Gate Oxide Leakage Mechanisms

There are two prevalent carrier conduction mechanisms in the $SiO_2$ namely direct tunnelling and Fowler-Nordheim injection. The dominant conduction mechanism is dependent on the dielectric thickness, trap density, and electric field strength.

In modern deep sub-micron devices, gate oxide thickness have been scaled into the sub 3.5nm region and the gate leakage level is consequently much larger than that in thicker oxides. The dominant oxide conduction mechanism in ultra-thin oxide is the direct tunnelling of electrons [52] as illustrated in the band diagram of Fig 2.5 which shows electrons tunnelling through the oxide from the inversion layer to the metal electrode.

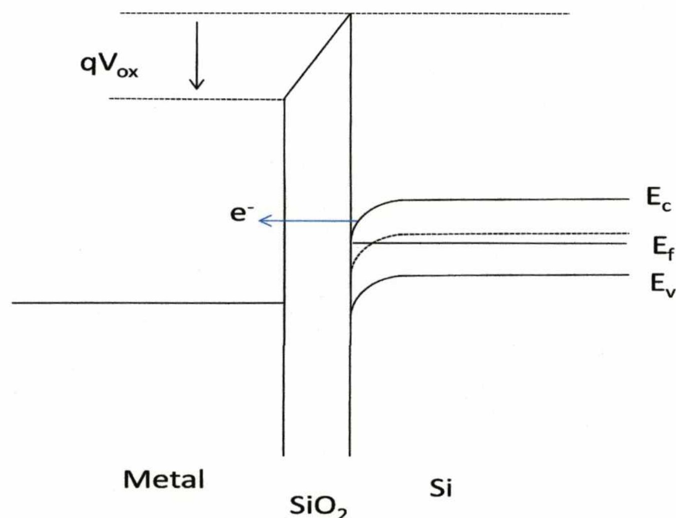



Fig 2.5 Band diagram of direct tunneling mechanism.

The tunnelling current is determined by the electric field, oxide barrier height and the carrier effective mass in the oxide. The magnitude of the tunnelling current does not have a

direct relationship to the carrier density in the electrodes: the silicon side in this case. This is because the rate of electron tunnelling from the potential well is very small compared to supply capability. This allows a direct evaluation of the quantum mechanical probability without considering the carrier supply [53], to produce the following expression:

$$I_{DIR} = A_G A \xi_{ox}^2 \exp\left[\frac{-B\left[1-(1-\frac{qV_{ox}}{\Phi_B})^{3/2}\right]}{\xi_{ox}}\right] \quad \text{Eq. 2.30}$$

where $A_G$ is the gate area, $\xi_{ox}$ is the oxide electric field that can be related to gate bias by subtraction of the surface potential, $V_{OX}$ is the oxide voltage, $\Phi_B$ is the barrier height for electrons for emission from semiconductor to dielectric. A and B are variables related carrier tunnelling in oxide as listed below, for the case of injection from a metal electrode:

$$A = \frac{q^3 \frac{m_e}{m_{ox}}}{8\pi h_p \Phi_B} = \frac{1.54x10^{-6} \frac{m_e}{m_{ox}}}{8\pi h_p \Phi_B} \quad \text{Eq. 2.31}$$

$$B = \frac{8\pi\sqrt{2m_{ox}\Phi_B^3}}{3qh_p} = 6.83x10^7 \sqrt{\frac{m_{ox}}{m_e}\Phi_B^3} \quad \text{Eq. 2.32}$$

where $h_p$ is Planck's constant, $m_e$ is the free electron mass, $m_{ox}$ is the carrier effective mass at the conduction band edge in oxide, m is the free electron mass, and the following assumptions are made: $\Phi_B$=3.2 eV and $\frac{m_e}{m_{ox}} = 0.35$.

For thicker oxide, the probability of carriers tunnelling through the entire potential barrier height becomes very low, but given a sufficient high electric field, they are still able to tunnel through the narrow part of the trapezoid shape energy barrier into the conduction band of the oxide. This latter mechanism is named Fowler-Nordheim conduction and is further explained with the aid of Fig. 2.6.

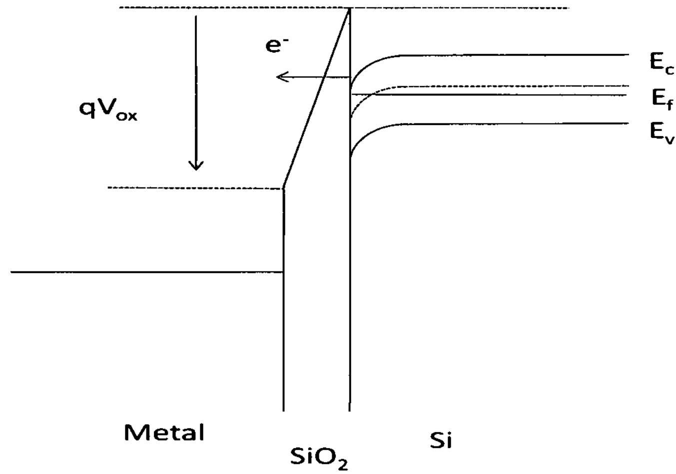



Fig 2.6 Band diagram of Fowler-Nordheim mechanism tunnelling (Note that carriers tunnel mainly from the inversion layer).

For Fowler-Nordheim tunnelling, the analytical model can be expressed as

$$I_{FN} = A_G A \xi_{ox}^2 \exp\left(\frac{-B}{\xi_{ox}}\right) \qquad \text{Eq. 2.33}$$

A and B are as expressed in equation 2.31 and equation 2.32. Note that A and B are appropriate for tunnelling from a metal electrode. Tunnelling from semiconductor inversion or accumulation layers requires consideration of sub-bands in those regions and gives rise to different expressions for the constants. However, in fact, the absolute values of the constants are of similar magnitude, as pointed out by Weinberg [53].

Besides direct tunnelling and Fowler-Nordheim conduction, which are one-step tunnelling processes, carriers can tunnel through the dielectric by multi-step paths; the so-called trap-assisted tunnelling (TAT). The TAT mechanism is often known as stressed induced leakage current (SILC) and is generally present under low gate bias in a dielectric which has been pre-stressed by high field. The consequence of repeated stressing is that more traps are created allowing conditions for multi-path tunnelling of carriers. An analytical model is presented in [54] where the energy difference between the conduction band in the dielectric and the energy level of the trap is needed for detailed calculations.

## 2.7 RF Performance Figures of Merit

This investigation of Si-based vertical MOSFET for radio frequency circuit applications involves an assessment of the suitability of fabricating devices with good DC performance using standard CMOS compatible process as well as the suitability of the device performance from the RF point of view. CMOS compatibility is a pre-condition in the design of a fabrication process scheme. In a PA circuit design stage, the device efficiency, gain, noise and linearity are the most common metrics to consider. The efficiency can be optimized by adopting dynamic bias, voltage and load during the circuit design [55], but should also be taken into account where maximum current and power gain and minimum power consumption are targeted.

The second important figure of merit is the gain of device, which is closely related to the efficiency, whereby increasing the gain brings the possibility of achieving higher efficiency. On the other hand, the possible highest frequency to obtain useful gain is determined by two commonly used figures of merit: the gain-bandwidth product, $f_T$ and the maximum oscillation frequency $f_{max}$. The $f_T$ is the frequency when the current gain falls to unity while $f_{max}$ measures the frequency when the power gain fails to unity. The derivation of the analytical expressions of the above two figures of merit is described below.

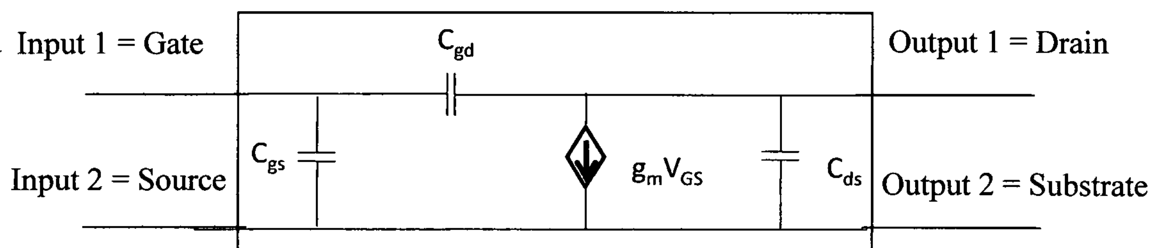



Fig 2.7 A simplified two port network of a MOSFET at RF.

In the RF operation regime, a MOSFET can be represented by a two-port network as shown in Fig 2.7 where the simplified equivalent circuit of the intrinsic part is contained in the box. It is considered here that the influence of the substrate network is negligible and the effect of parasitic resistances ($R_d$, $R_s$) are already accounted for in the transconductance parameter, $g_m$. Hybrid (h) parameters are needed when the current amplifier property is required at the output. The h-parameters can be extracted from a two-port network which is used to represent a device. Knowledge of the parameter $h_{21}$ is of most importance as it defines the input and output current gain of the transistor at a specific input frequency and in terms of the admittance parameters $Y_{11}$ and $Y_{21}$ as defined in equation 2.33 below. Consequently, $h_{21}$ can be expressed analytically as a function of $g_m$, gate-to-source capacitance $C_{gs}$ and gate-to-drain capacitance $C_{gd}$ with help of admittance parameters $Y_{11}$ and $Y_{21}$ through equation 2.34 to equation 2.37.

$$h_{21} = \frac{I_{out}}{I_{in}} = \frac{Y_{21}}{Y_{11}} \qquad \text{Eq. 2.34}$$

$$Y_{11} = \left.\frac{I_1}{V_1}\right|_{V_2=0} = j\omega C_{gs} + j\omega C_{gd} \qquad \text{Eq. 2.35}$$

$$Y_{21} = \left.\frac{I_2}{V_1}\right|_{V_2=0} = -g_m + j\omega C_{gd} \qquad \text{Eq. 2.36}$$

If the operation frequency satisfies the condition, $\omega = 2\pi f \ll \frac{g_m}{C_{gd}}$

$$|h_{21}| = \left|\frac{Y_{21}}{Y_{11}}\right| \approx \frac{g_m}{\omega(C_{gs}+C_{gd})} \qquad \text{Eq. 2.37}$$

when $h_{21}$ falls to unity, then the corresponding frequency can be defined as:

$$f_T \approx \frac{g_m}{2\pi(C_{gs}+C_{gd})} \qquad \text{Eq. 2.38}$$

The $f_T$ is proportional to the transconductance $g_m$, and reciprocally to gate to drain/source overlap capacitances. The transconductance, $g_m$ in the saturation region of MOSFET operation can be expressed using equation 2.39 where $V_T$ and $\lambda$ take into account the drain/source charge sharing, DIBL, and CLM phenomenon while $\mu_{eff}$ and $\upsilon_{sat}$ take into account the velocity saturation phenomenon.

$$g_m = \frac{\mu_{eff} C_{ox} \frac{W}{L}(V_{GS}-V_T)(1+\lambda V_{DS})}{1+\frac{\mu_{eff} V_{DS}}{\upsilon_{sat} L}} \quad \text{Eq. 2.39}$$

The $g_m$ can be further linked to the saturated drain source current and expressed as

$$g_m \approx \sqrt{2\mu_{eff} C_{ox} \frac{W}{L} I_{DS}} \quad \text{Eq. 2.40}$$

and the transconductance $g_m$ in the linear region of operation can be expressed as

$$g_m = \mu_{eff} C_{ox} \frac{W}{L} V_{DS} \quad \text{Eq. 2.41}$$

When the device operates in the saturation region, the reciprocal of $2\pi f_T$ can be also defined as the transit time $\tau$, associated with electrons travelling from source to drain in the channel. The transform of $f_T$ to $\tau$ is outlined in equation 2.42 where the following conditions are considered (1) $C_{gs}$ dominates among the parasitic capacitance components (2) $C_{gs} \approx \frac{2}{3} LWC_{ox}$ (3) $V_{GS}$-$V_T$=$V_{DS}$

$$\tau = \frac{1}{2\pi f_T} \approx \frac{C_{gs}}{g_m} = \frac{\frac{2}{3}LWC_{ox}}{\frac{W}{L}\mu_{eff}C_{ox}(V_{GS}-V_T)} = \frac{3L}{2\mu_{eff}\frac{V_{GS}-V_T}{L}} \sim \frac{L}{\upsilon_{sat}} \quad \text{Eq. 2.42}$$

Alternatively, the value of cut-off frequency $f_T$, can be obtained from the frequency response of current gain, $h_{21}$, which can be expressed by the S parameters.

$$h_{21} = \frac{-S_{21}}{(1-S_{11})(1+S_{22})+S_{12}S_{21}} \quad \text{Eq. 2.43}$$

The $h_{21}$ method allows extraction of $f_T$ from a plot of the $h_{21}$ parameter versus frequency on log-log scales. A line with slope of -20dB/dec can be fitted by linear regression to each roll-off curve and the intercept on the frequency axis yields $f_T$.

The figure of merit $f_{max}$ is defined as the frequency when the Maximum Available power Gain (MAG) $G_{max}$ reaches unity according to Mason's unilateral power gain definition. Note that the maximum power gain of a device is defined as the power gain delivered when both input and output ports are matched to the impedance of the source and load, respectively. $G_{max}$ can be expressed using Y parameters as indicated below [56].

$$G_{max} = \frac{1}{4} x \frac{|y_{21} - y_{12}|^2}{(Re(y_{11})Re(y_{22}) - Re(y_{21})Re(y_{12}))} \quad \text{Eq. 2.44}$$

In accordance with the experience of circuit designers, $f_T$ and $f_{max}$ need to be 10 times and 15 – 20 times the operating frequency respectively to guarantee that the design will satisfy the targeted gain over a specific high frequency range [57].

Based on a small-signal equivalent circuit and under the assumption of negligible losses through the substrate network, the analytical expression of $f_{max}$ can also be expressed as follows [58, 59, 60]

$$f_{max} = \frac{f_T}{2\sqrt{(2\pi R_g f_T C_{gd} + g_{ds}(R_g + R_s)}} \quad \text{Eq. 2.45}$$

where $R_g$ is the gate resistance, $R_s$ is the series resistance related to source junction and $g_{ds}$ is the output conductance.

The $f_{max}$ parameter is generally more dependent on layout than $f_T$ as the gate resistance plays an important role. The value of $R_g$ depends on (a) the distributed resistance of polysilicon (b) the metal to poly contact resistance. A significant reduction of gate resistance is achieved when the gate is connected by more than one contact.

The $f_T$ and $f_{max}$ parameters are both affected by the values of the drain and source series resistance which serve to limit the DC bias current and so in turn, the value of transconductance $g_m$. It is worthwhile to note that $f_{max}$ is more sensitive to $R_s$ than is $f_T$ because of the additional contribution of $R_s$ in determining the denominator term of equation 2.44.

## 2.8 MOSFET RF Equivalent Circuit

When the MOSFET device operates up to high frequencies, the characteristics such as the unity current and power gains start to degrade. This degradation arises as the intrinsic channel region of the device experiences a non-quasi-static effect (NQS) [61] which affects

the transconductance. More importantly the extrinsic parasitic components of the device have a significant impact in limiting the $f_T$ and $f_{max}$ values at high frequencies. Thus from the modelling point of view, to accurately describe the device performances in the RF frequency range, it is important to model accurately both the intrinsic and extrinsic components of the device. The basic characteristics of the intrinsic part has been briefly introduced in the above sections, while the extrinsic parasitics can be represented by the resistance, capacitance, diode components in the equivalent circuit as shown in Fig 2.8. These components such as gate resistance, source/drain series resistance, gate overlap capacitances and the substrate network can be extracted through the analysis of the small signal parameters characterised from the two-port network [62]. The extraction of series resistance using small signal parameters will be further discussed in Chapter 6.

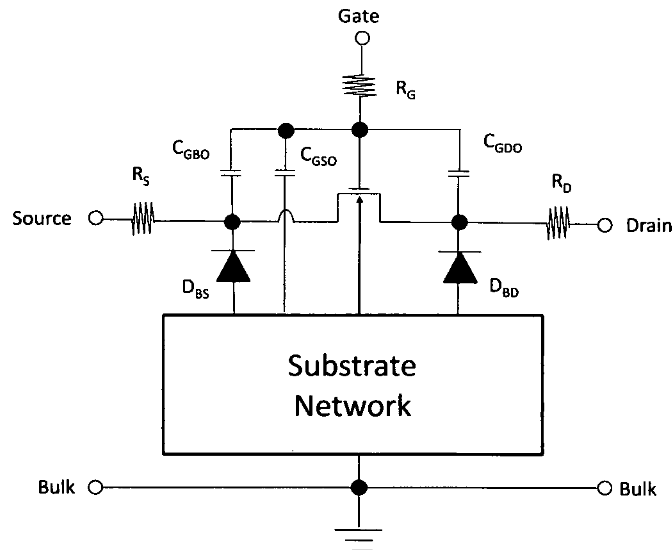



Fig 2.8 Equivalent circuit of a MOSFET at RF frequency range.

# Chapter 3

# Characterisation and Numerical Modelling of Vertical MOSFETs with a Junction Stop

# 3.1 Current-Voltage Characterisation

## 3.1.1 Sample Preparation

The general fabrication process of vertical MOSFETs with a junction stop structure and its novelty is described and summarized in section 1.4. In this chapter, the DC electrical characteristics of the VMOSFET-JS fabricated in different process conditions with channel lengths down to 70nm are investigated. Device simulation was performed in order to quantify some physics related device parameters and establish a numerical model that can be used for short channel effect studies.

The junction stop structure is reviewed in Fig 3.1 where a shallow junction vertical transistor can be realized by incorporation of an oxide cap or junction stop (JS). This structure is referred to as 'VMOSFET-JS'. The shallow drain junction is created by out-diffusion from an n-doped polysilicon drain through a self-aligned polysilicon spacer. The junction stop structure brings a number of advantages and importantly, allows formation of a shallow junction at the pillar top which in turn to mitigate the problems of charge sharing (CS) and DIBL. The JS structure prevents junction dopant penetration into the centre of the pillar, which could exacerbate bulk punch through. The channel length is defined by anisotropic dry etch and a connection is established between the drain and the body of the device by a thin polysilicon spacer. The poly-drain spacer width at the drain-body connection part is limited by the polysilicon layer thickness.

To thoroughly study the electrical characteristics of VMOSFET-JS devices, the transfer characteristics and the output characteristics were measured using a H4155B parameter analyzer. The carrier conduction as a function of gate bias condition in the gate to drain/body/source oxides was assessed from measurements conducted with the Hewlett-

Packard IV rig where the delay time of each DC sweep step was 0.4s and the rise time was 0.02s.

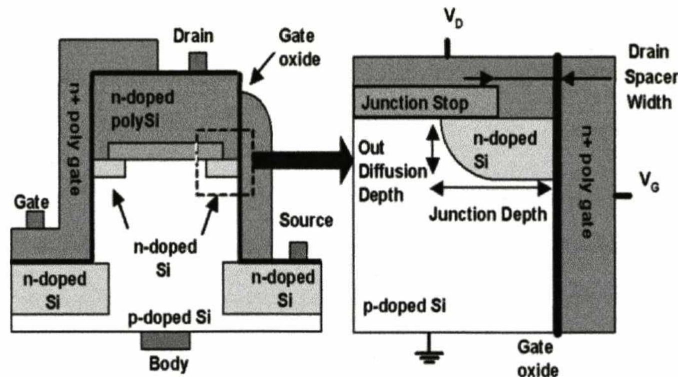



Fig 3.1 Vertical MOSFET structure with a junction stop beneath the poly-Si drain contact.

In order to study the impact of the channel length and drain spacer width parameters of the JS devices, the process designated for further IV investigation was divided into 4 splits (#1, 3, 5, 6) where with the same channel length, drain spacer width varies from 50 nm to 30 nm, while, with the same spacer width, the channel length varies from 130nm to 70nm. Process split #3 featured, a thinner junction stop of nominally 10nm. In process split #7, devices were fabricated with a 6nm thick sacrificial oxide which was thermally grown at 800°C on the pillar sidewall and then selectively removed by wet etch in hydrofluoric acid in order to eliminate dry etch damage, which can cause high interface state density. Process split # 8 had no junction stop layer but only an amorphous Si drain on the pillar top to allow comparison of the electrical property of devices with and without the JS structure. Therefore in split #8, devices have a drain junction out-diffused from the amorphous drain all over into the pillar top. The key conditions of interest for research presented in this section are shown in the table 3.1.

Table 3.1 Summary of Splits of JS batch devices

| Process Split | JS Thickness (nm) | Drain Spacer Width (nm) | Channel Length (nm) | RTA Temperature °C |
|---|---|---|---|---|
| 1 | 20 | 50 | 130 | 1050 |
| 3 | 10 | 30 | 130 | 1050 |
| 5 | 20 | 50 | 70 | 1050 |
| 6 | 20 | 30 | 70 | 1050 |
| 7* | 20 | 50 | 130 | 1050 |
| 8 | Control Device ( No JS ) | | 250 | 1050 |

*Sacrificial oxidation was grown and etched before gate oxide growth

### 3.1.2 Comparison of Transfer Characteristics

The reliability of the fabrication process of VMOSFET-JS devices is justified by successful reproduction of similar transfer and output characteristics among different devices on the same wafer from the different process splits. Two examples of the transfer characteristics from two separate devices in each process splits are plotted in Fig 3.2 – 3.7 to allow comparison. The transfer characteristics were measured with drain biased at 1.0V and 0.1V in drain-on-top (DoT) mode which applies to the case when the drain is assigned to the top of the vertical pillar and source-on-top (SoT) mode to the case when it is assigned to the bottom contact. The same characteristics are stable and repeatable after several gate bias sweeps. Note that "W", represents the channel width of the measured device.

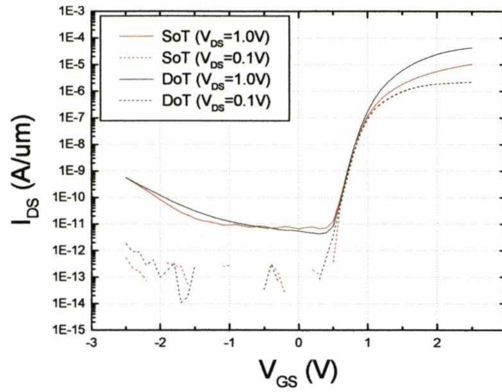



Fig 3.2 Transfer characteristics of devices in split # 1: W=32um

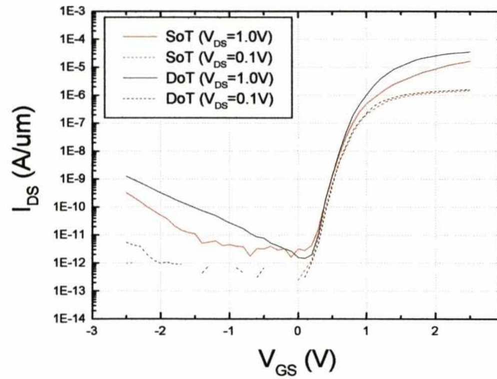



Fig 3.3 Transfer characteristics of devices in split # 3: W=52 um

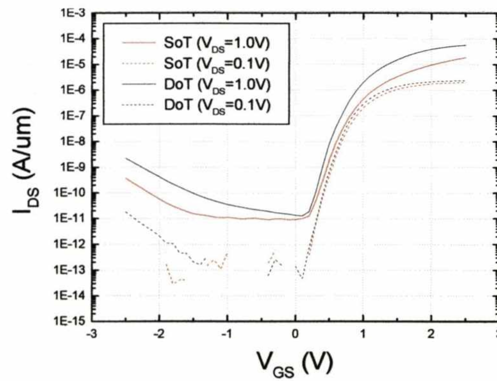



Fig 3.4 Transfer characteristics of devices in split# 5: W=52 um

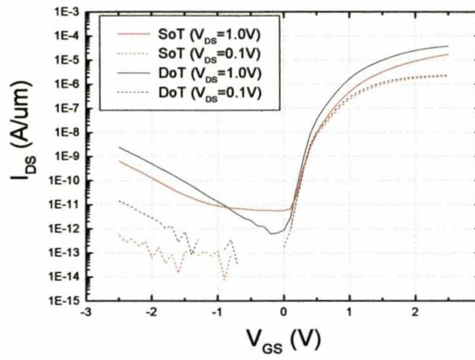



Fig 3.5 Transfer characteristics of devices in split#6: W=27 um

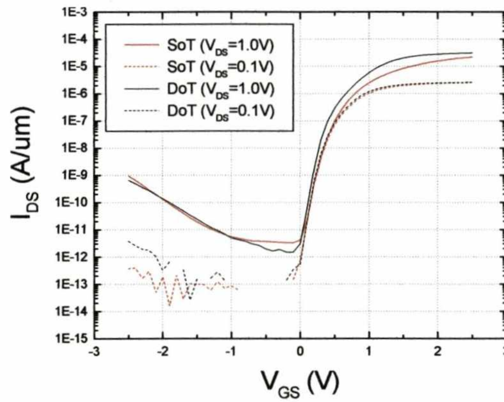



Fig 3.6 Transfer characteristics of devices in split#7: W=27 um

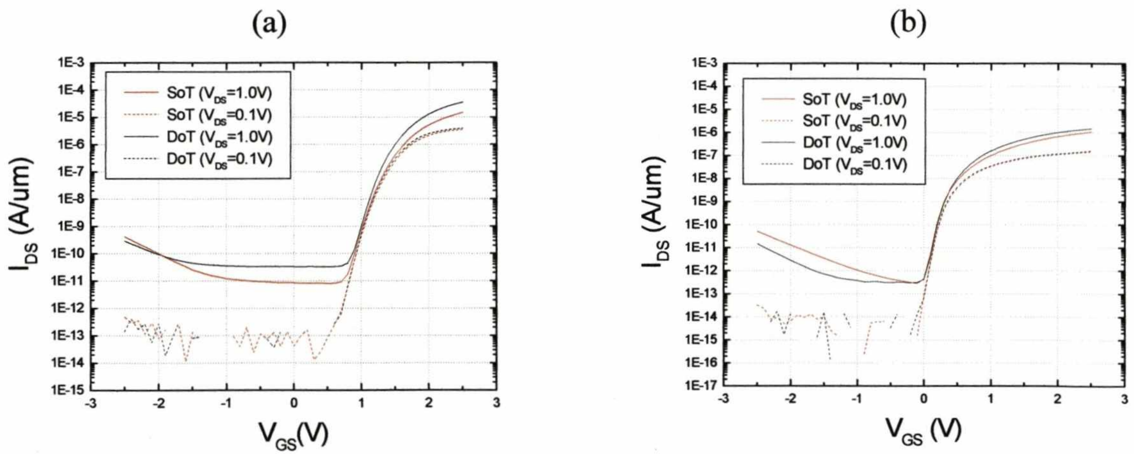



Fig 3.7 Transfer characteristics of devices in split#8: (a) W = 27 um with a high $V_T$; (b) W = 27 um with a low $V_T$.

The above transfer characteristics allow extraction of some DC parameters such as threshold voltage $V_T$, on-current, off-current, drain induced barrier lowering (DIBL), and sub-threshold slope, Ss, for $V_{DS}$=0.1V and $V_{DS}$=1.0V. The electrical characteristics of the

best devices with the highest $I_{on}$ per channel width from each individual split are used for parameter extraction and comparison. The results of threshold voltage, on/off-current, sub-threshold slope Ss for both DoT and SoT are listed in table 3.2. On-current is the drain current taken at $V_{DS}$=1.0V and $V_{GS}$=1.5V while off-current is the drain current taken at $V_{DS}$=1.0V and $V_{GS}$=0V. The devices with nominally 250nm channel length in split #8 have two categories of characteristics measured: one has high threshold voltages and the one has low threshold voltages. Note that all the devices have nominally a body doping/substrate level of $3x10^{18}cm^{-3}$ and gate oxide thickness of 3nm. The characterised on-currents show that the best value of 20 uA/um was found in split #7. However it is still 26 times lower than the ITRS data at the 70nm technology node due to a combined effect of its high body doping and additional series resistance. The simulation from an ideal structure assuming no additional series resistance effect shows that the on-current should have a value of 380 μA/μm that is about 18 times higher than the best characterized $I_{on}$. Further investigation of $I_{on}$ rectification by the additional resistance is discussed in section 3.3.5. The cause of this resistance is thought to be due to a thin native oxide layer residing between the polysilicon drain and silicon body.

Table 3.2 Electrical charactersitics parameters of JS batch devices

| | **$V_T$ (V)** | | **$I_{on}$ (uA/um)** | | **$I_{off}$ (pA/um)** | | **Ss (mV/dec) ($V_{DS}$=1.0V)** | |
|---|---|---|---|---|---|---|---|---|
| | DoT | SoT | DoT | SoT | DoT | SoT | DoT | SoT |
| Split 1 | 1.1 | 1.1 | 6.02 | 1.83 | 5.43 | 6.47 | 100 | 100 |
| Split 3 | 0.95 | 0.95 | 10.98 | 3.17 | 1.57 | 3.17 | 117 | 117 |
| Split 5 | 0.78 | 0.83 | 15.9 | 2.8 | 8.89 | 4.78 | 118 | 155 |
| Split 6 | 0.95 | 0.95 | 10 | 3.0 | 1.54 | 8.98 | 117 | 158 |
| Split 7 | 0.7 | 0.7 | 20.3 | 8.4 | 3.0 | 4.04 | 89 | 89 |
| Split 8 (a) | 1.28 | 1.28 | 1.42 | 0.53 | 11.5 | 8.3 | 102 | 118 |
| Split 8 (c) | 0.48 | 0.5 | 11.6 | 0.7 | 377.8 | 156.7 | 102 | 118 |

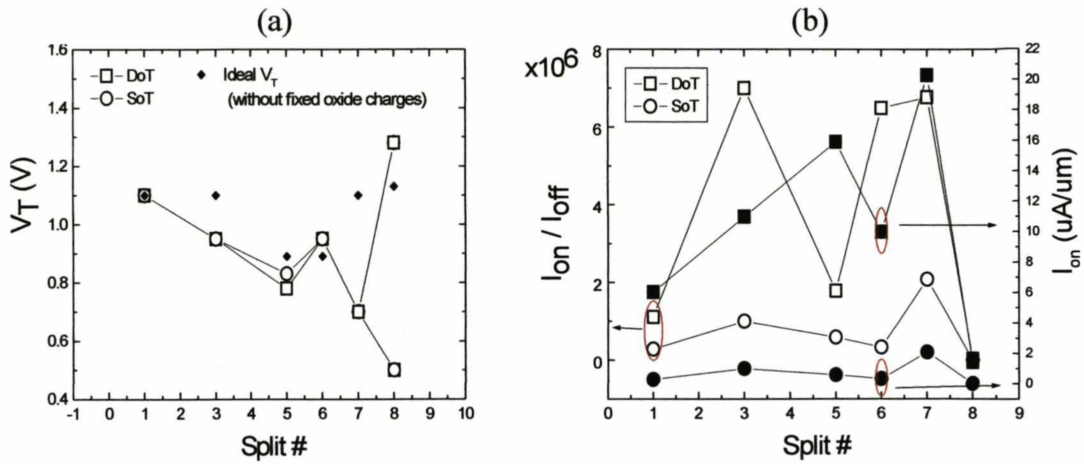



Fig 3.8 Comparison of (a) $V_T$ (b) $I_{on}/I_{off}$ in DoT and SoT modes in different process splits.

The comparisons of $V_T$s and $I_{on}/I_{off}$ ratios are illustrated in Fig 3.8 (a) and (b). In Fig 3.8 (a), for devices in split # 1 (L=130nm), the $V_T$ under low drain bias is 90mV higher than the ideal values estimated from the bulk MOSFET threshold voltage calculator in the road map calculation tool kit MASTAR [63] where charge sharing effect on $V_T$ is taken into account. In the calculation 50nm junction depth and the defaulted fitting parameters for charge sharing effect, effective channel length were used. For devices in the splits # 3, 7 (L=130nm) the $V_T$s are 60.4mV and 309.8mV less than the ideal value respectively. The main reason for this significant shift could be explained by the presence of negative gate oxide charge or a shorter than expected channel length. Note that the latter explanation could arise from over-etching of the reduction of the pillar height. The long channel devices in split # 8 (250nm) were divided into two groups: one with a high $V_T$ which is 0.15 V higher to the ideal value of 1.13V; the other one with a value of around 0.5V. Note that the ideal devices with 130nm, 250nm and long channel lengths have almost the same $V_T$s due to high body doping. For the second group of devices, a level of $4.5 \times 10^{12}$cm$^{-2}$ of positive fixed gate oxide charge or a channel reduction of 193nm is needed to account for the 0.63V reduction in $V_T$ from its expected value. On the other hand, for the short channel devices in split # 5 and 6 (L=70nm), $V_T$s are either lower or higher than the expected

values. If not considering channel length variation, this shift indicates the presence of positive and negative gate oxide charge of the order of mid-$10^{11}cm^{-2}$. Such a level of oxide charge is feasible in these experimental devices made with a non-optimised process.

In Fig 3.8 (b), it is shown that the $I_{on}/I_{off}$ ratios in DoT are significantly higher than that in SoT due to a higher $I_{on}$. The asymmetry of $I_{on}$ in DoT and SoT is caused by the additional resistance that is connected in series to the top junction. Further analysis is deferred to section 3.3.6. The comparisons of sub-threshold slopes in SoT and DoT under $V_{DS}$=1.0V is illustrated in Fig 3.9 (a). An extra Ss degradation is observed clearly in SoT mode for splits # 5, 6, 8. These phenomena are almost certainly associated with the presence of higher interface state density at the pillar top regions of the sidewalls that cause Ss higher in SoT than in DoT. Before the final metal deposition and RTA, a polysilicon gate track etch is necessary to allow the gate spacer to surround the pillar without covering the entire pillar top. However, over-etching of the polysilicon can cause the top segment of the thin gate oxide exposed during the gate etch and plasma damage is induced on it especially at the top of the pillar. As a result, a high level of interface state density $D_{it}$ can be present in the top region of the pillar. A diagram is plotted in Fig 3.9 (b) to assist the explanation where the top gate oxide is exposed to plasma damage. The pillar bottom segment is immune to the damage due to un-etched segment of the polysilicon gate. In split # 7 where sacrificial oxidation was used to passivate surface prior to gate oxide growth, the Ss for both SoT and DoT are low due to the fact that the interface trap density was largely eliminated.

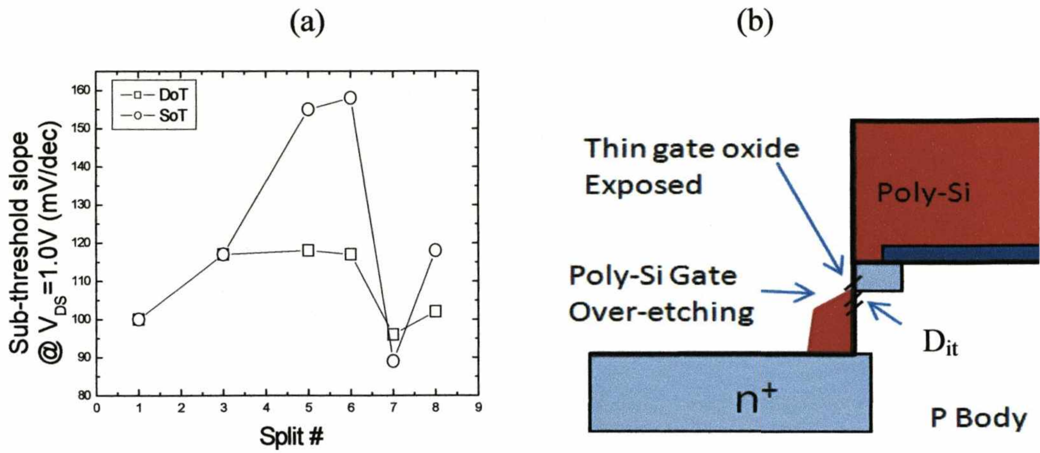



Fig 3.9 (a) Comparison of sub-threshold slopes in SoT and DoT; (b) indication of the location of the high interface states density induced during the Poly-Si gate over-etching.

## 3.1.3 Comparison of Output Characteristics and Substrate Currents

The output characteristics of devices which were chosen for data collection in the last section are shown in Fig 3.10-3.15 where the gate bias is varied from 0 to 2.4V in 0.4 V steps. The strong asymmetry in linear and saturation currents for SoT and DoT modes at high gate bias is explained as due to the presence of additional series resistance at the top junction as previously discussed. Further detailed analysis will be presented in section 3.3.6.

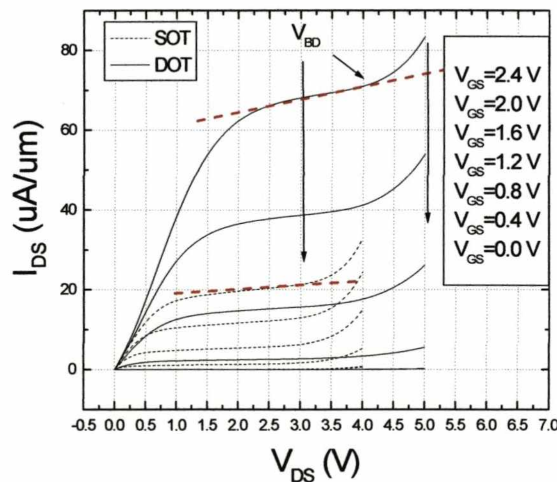



Fig 3.10 Output characteristics of a device in split# 1 W=32um.

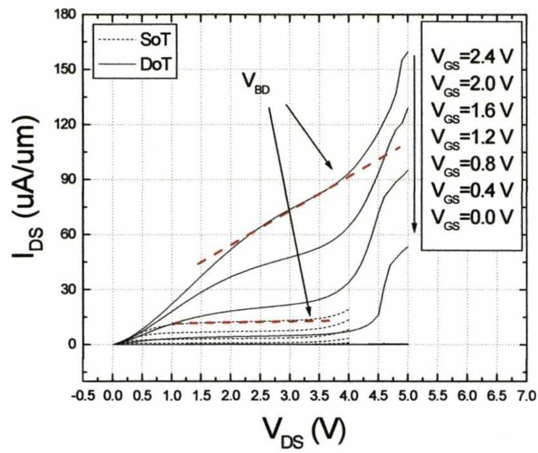



Fig 3.11 Output characteristics of a device in split#3 W = 27 um.

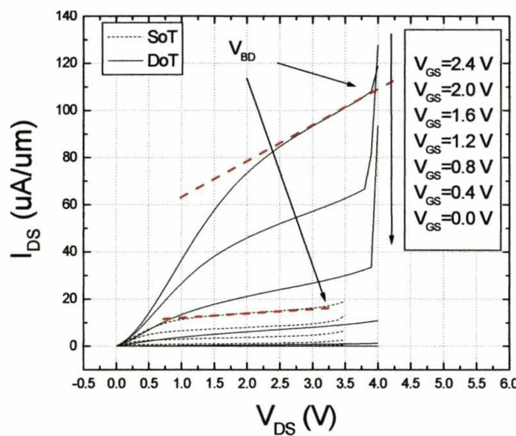



Fig 3.12 Output characteristics of a device in split#5 W=52 um.

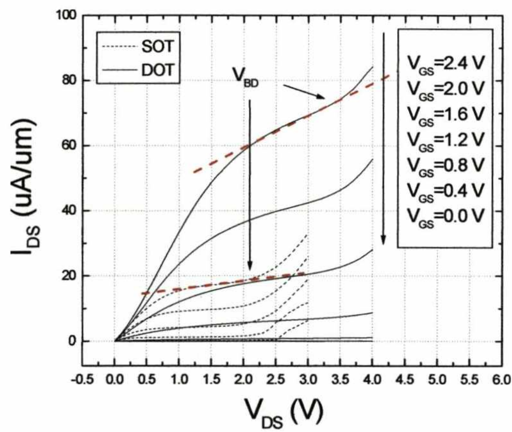



Fig 3.13 Output characteristics of a device in split#6 W=27um.

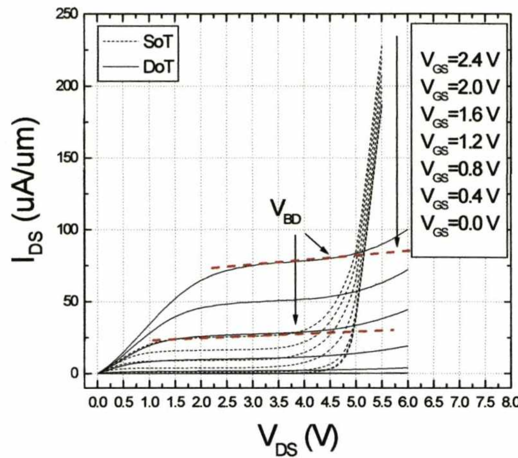



Fig 3.14 Output characteristics of a device in split#7 W=27 um.

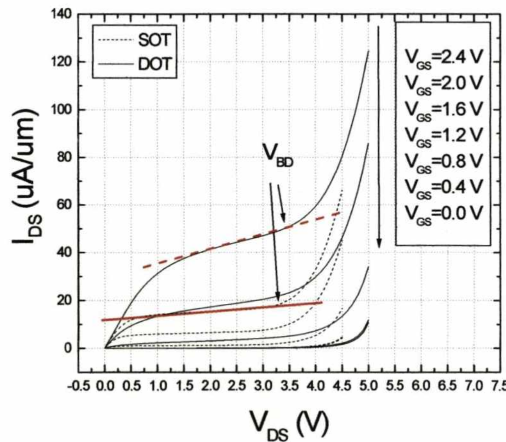



Fig 3.15 Output characteristics of a device in split#8 W = 27 um.

The other striking feature of the output characteristics is the asymmetry of breakdown voltage $V_{BD}$ in SoT and DoT modes where $V_{BD}$ in SoT is always lower than in DoT. The breakdown phenomenon is caused by avalanche impact ionization by the hot carriers at the drain end where a hot electron induces other electron and holes pairs. The holes flow into the body thus the substrate and form the body current. The body current at high drain bias serves as an indicator of the avalanche impact ionization. The body current is measured as a function of gate bias with different drain biases in both SoT and DoT modes and is shown Fig 3.16 (a) – (f) for all the splits.

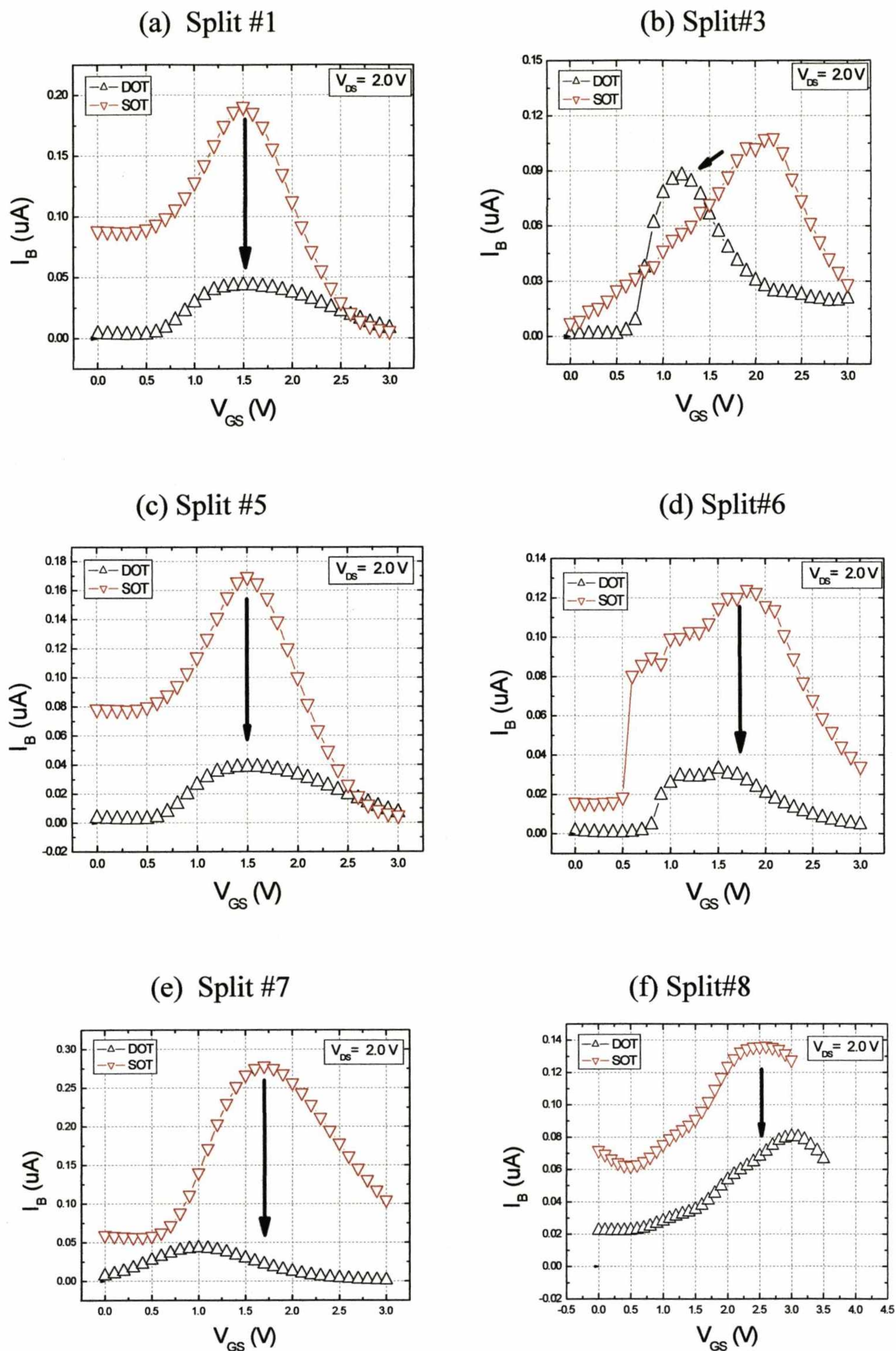



Fig 3.16 Comparisons of $I_B V_{GS}$ curves for both DoT and SoT modes for all the splits with varying drain biases.

Both values of avalanche breakdown voltage $V_{BD}$ and maximum body current $I_{BMAX}$ in SoT and DoT modes of all the cases are listed in table 3.3. Note that $V_{BD}$ is defined at a drain-source voltage where saturated drain current starts to increase dramatically due to impact ionization with $V_{GS}$=2.4V.

Table 3.3 Breakdown voltage and ratio of maximum body current in DoT and SoT

| Split # | Breakdown Voltage (V) | | $I_{BMAX}$ (uA/um) | |
|---|---|---|---|---|
| | DoT | SoT | DoT | SoT |
| 1 | 4.1 | 3.0 | 0.043 | 0.19 |
| 3 | 3.7 | 3.2 | 0.029 | 0.036 |
| 5 | 3.9 | 2.9 | 0.038 | 0.17 |
| 6 | 3.5 | 2.2 | 0.03 | 0.124 |
| 7 | 4.75 | 3.75 | 0.043 | 0.28 |
| 8 | 3.5 | 3.2 | 0.08 | 0.136 |

The values of $V_{BD}$ and ratio of maximum body currents of the two modes under different drain biases are illustrated in Fig 3.17 (a) and (b) for all the splits. The $V_{BD}$ asymmetry between the two modes reaches its maximum in split # 5 and minimum in split # 3 and 8. Note that split # 3 has a 10nm thick junction stop and the split # 8 has no junction stop. The rest of the splits have 20nm thick junction stop that sufficiently screens the drain field penetrate into the top of the pillar resulting in much weaker avalanche impact ionization in DoT than SoT where no junction stop is present at the pillar bottom. The relative symmetry of the body current for DoT and SoT in split 3 # devices suggests an ineffective junction stop as a result of a tail of drain dopant penetrating into the centre of the pillar to form the deep top junction. This is a similar situation to that of the control devices in split # 8 where the impaction ionization at the drain end is not suppressed giving similar $V_{BD}$ irrespective of DoT or SoT.

The weak junction stop suppression of impact ionization in split # 3 and 8 is also evident by comparing the $I_{BMAX}$ in SoT and DoT ratios to the rest splits. The lowest values are found for split # 3 and 8 indicating the least asymmetry of maximum body current in the two modes therefore a weak or absence of the junction stop suppression on impact ionization at the pillar top.

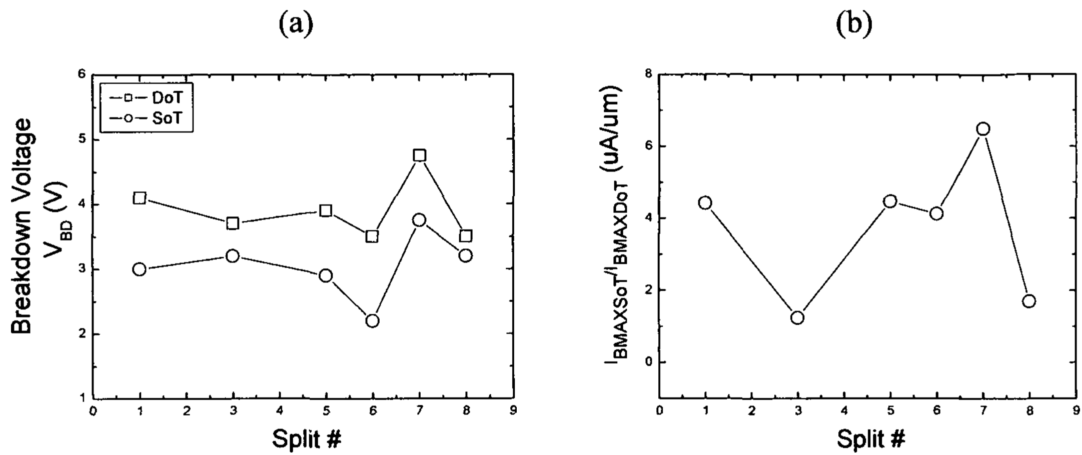



Fig 3.17 Comparison of breakdown voltage and the ratio of maximum body current in DoT and SoT modes.

## 3.2 Carrier Conduction Mechanism in Gate Oxide

Before the deposition of the polysilicon gate of the VMOSFET-JS devices, a 3nm thin gate oxide was thermally grown covering the entire device surface. Consequently the oxides between the polysilicon gate and body/drain/source regions all have equal thickness. Two-terminal current-voltage measurements have been taken between gate and body electrodes with the maximum of the gate bias below |2.5V| in order to avoid an electric field strength of 10MV/cm that could cause the oxide to break down. Typical gate to body oxide leakage measurements with floating drain and source electrodes are represented by symbols and shown in Fig 3.18. The overlap of the data indicates the reproducibility of the measurement among the four devices on the wafers.

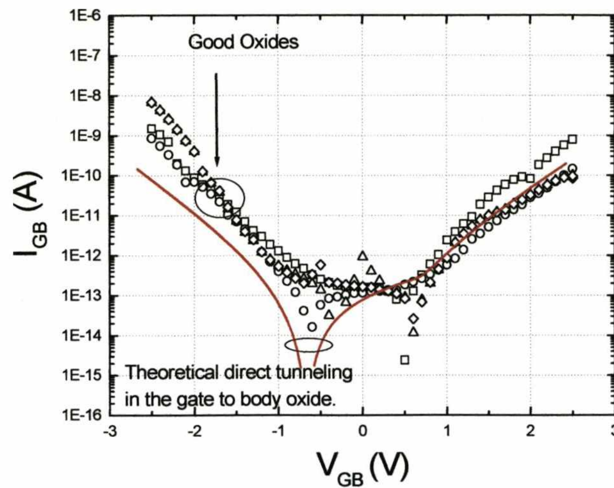



Fig 3.18 Gate to body oxide current vs. gate bias; $t_{ox}$=3nm; area=$2.1x10^{-9}m^{-2}$; the source and drain electrodes were set to be floating.

In Fig 3.18, the data represented by the symbols shows a low current level which varies from $1x10^{-14}$ A to $1x10^{-8}$ A as the gate bias sweeps up to positive and negative 2.5V. In such thin oxide, it is presumed that direct tunnelling dominates the carrier conduction mechanism [52]. This can be confirmed by the fact that low level $I_{GB}$-$V_{GB}$ characteristics demonstrates a good functional fit to the direct tunnelling theory expressed in equation 2.28 where the surface potential in the silicon surface is also taken into consideration. The theoretical model is represented by the red line in Fig.3.18. Note that the higher current in the negative gate bias region compared to that predicted by the theory, is attributed to the likelihood of a lower barrier height for electrons when injected from the poly-Si gate into the oxide due to field intensification at interfacial roughness. The dominant DT mechanism can also be confirmed by the fact that this tunnelling current has weak dependence on temperature which varies from 15°C to 70°C. Results are shown in Fig 3.19.

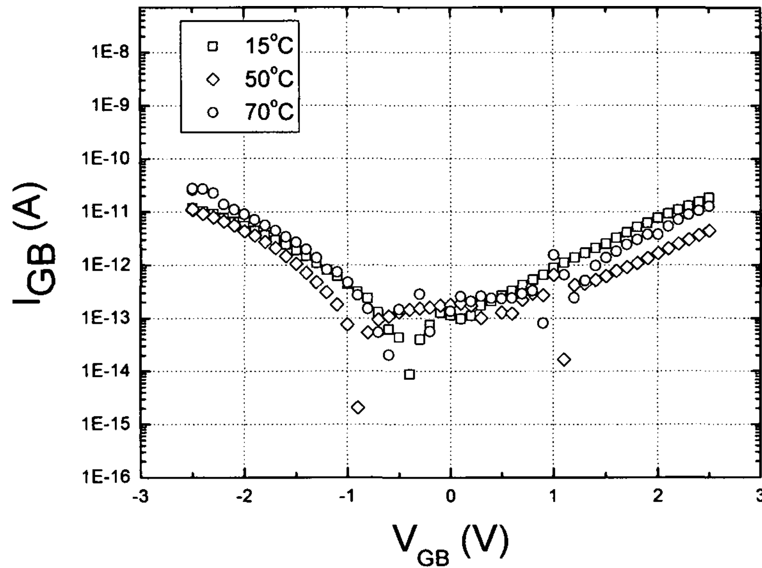



Fig 3.19 Temperature dependence of the gate to body oxide leakage.

The tunnelling carrier oscillation at the low field region is caused by the partial reflection of the wave function of the tunnelling electrons at the interface with the oxide. This reflection from all boundaries in the oxide leads to an additional item when calculating the tunnelling probability using the WKB model [64].

## 3.3 Device Modeling and Calibration

A general fitting of the numerical model and the experimental device transfer and output characteristics was conducted allowing further understanding of device properties such as fixed gate oxide charge, interface state density and series resistances. In addition, this physically based fitting of the numerical model allows for a reliable simulation study into short channel effects which are the key points of interest in the design of the junction stop structure.

### 3.3.1 Simulation Structure Construction

Fig 3.20 illustrates a 3D view of a surround gate VMOSFET-JS structure where the channel width is 30 μm. To avoid complex computation, a 2D cross-sectional structure which is shown in Fig 3.21 was used for device simulation. In accordance to the structure of a fabricated device in split #6 observed from the SEM cross sectional diagram of the pillar, the simulation structure has a channel length of 70nm [65]. The gate oxide has a nominal thickness of 3.0nm. The channel width in the 2D simulation is taken conventionally, as 1um. The junction stop thickness is 20nm. The top and bottom junction depths are both 30nm with the body doping set to be around $3x10^{18}cm^{-3}$ accordingly. The peak of the drain junction doping level is $1x10^{20}cm^{-3}$.

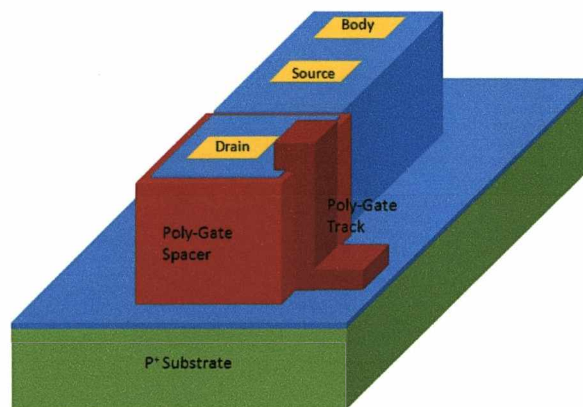



Fig 3.20 3D view of a surround gate VMOSFET-JS structure; W= 30μm.

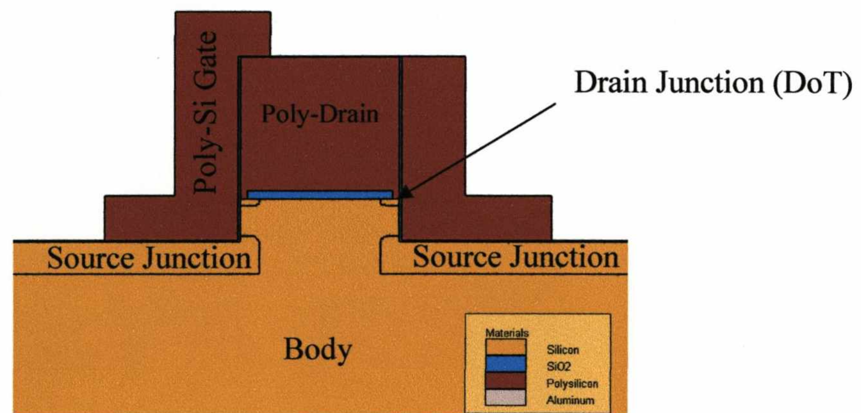



Fig 3.21 2D view of VMOSFET-JS structure with a 70nm channel length.

## 3.3.2 Calibration of the Sub-threshold Regime

The simulation study was conducted to attempt fits with the measured transfer characteristics under low and high drain biases and results are shown in Fig 3.22. The simulated sub-threshold region characteristics are calibrated with the experimental data by fitting two device parameters namely the threshold voltage $V_T$ and the sub-threshold slope parameter, Ss. The threshold voltage equation is:

$$V_T = V_{fb} + 2\Psi_B + \frac{\sqrt{4\varepsilon_{si} q N_a \Psi_B}}{C_{ox}} + \frac{Q_{ox}}{C_{ox}} \qquad \text{Eq. 3.1}$$

Where $V_{fb}$ is the flatband voltage, $N_a$ is the body doping, $C_{ox}$ is the gate oxide capacitance per unit area, $\Psi_s$ is the surface potential, $Q_{ox}$ is negative fixed oxide charge. As the first four parameters are kept constant $Q_{ox}$ is adjusted to fit the calculated and simulated $V_T$. The lateral shift gives the extraction of $Q_{ox}$ to be $2.9\text{x}10^{12}$ $cm^{-3}$. In this case, DoT mode is used. The effect of the interface state density ($D_{it}$) on threshold voltage is omitted from equation 3.1. The sub-threshold current is related to body factor m in a relationship as expressed in equation 2.19 where m also determines the subthreshold slope Ss. m can alternatively be expressed as below instead of equation 2.12

$$m = 1 + \frac{C_{dm} + C_{it}}{C_{ox}} \qquad \text{Eq. 3.2}$$

where $C_{dm}$ is the channel depletion region capacitance induced by the gate:

$$C_{dm} = \frac{\varepsilon_{si}}{W_{dm}} \qquad \text{Eq. 3.3}$$

and the interface-trap capacitance:

$$C_{it} = \frac{d|N_{it} q|}{d\Psi_s} \qquad \text{Eq. 3.4}$$

The sub-threshold slope is expressed by the following equation:

$$Ss = \frac{\ln(10) mkT}{q} = 60m\left(\frac{T}{300}\right) \text{mV/decade} \qquad \text{Eq. 3.5}$$

The interface state density is a function of the body factor, m. Therefore, by fitting the simulated sub-threshold slope to experimental value for $V_{DS}$=50mV, the interface state density can be estimated. As a result, after fitting Ss, an acceptor-like interface state $D_{it}$ along the channel was extracted to be $1x10^{12}cm^{-2}$. For ease of modelling, the main influence of states was indicated by one discrete trap energy level (state) placed at a energy depth of 0.3eV from the conduction band edge in the energy band gap. When the gate bias sweeps approaches the measured $V_T$ and fills this trap with an electron, the presence of the new state then shifts the simulated sub-threshold slope to a more positive direction so to fit the measured curve as shown in Fig 3.22. The sub-threshold region of the simulated transfer characteristic with $V_{DS}$=1V, is slightly shifted to a lower bias region due to the presence of 70mV DIBL which is not observed in the measured data. The channel length of the device might be underestimated from the ideal value of 100nm in the absence of DIBL.

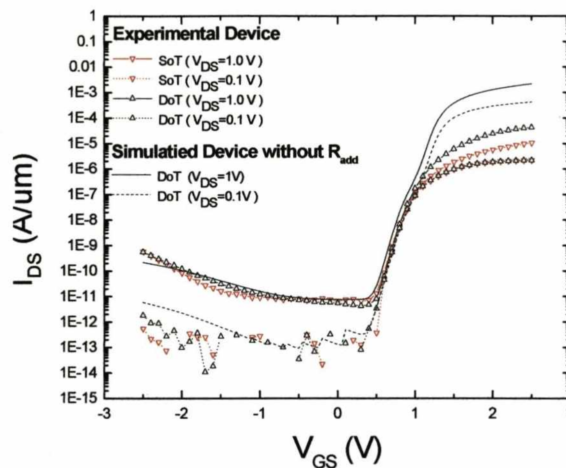



Fig 3.22 Transfer characteristics of fabricated device compared to the partially fitted device simulation apart from on-current region. L= 70nm, $t_{ox}$=3.0nm, $N_a$=$3.0x10^{18}cm^{-3}$.

### 3.3.3 Calibration of the Off-Current Regime and GIDL

In the low negative gate bias region -0.75V<$V_{GS}$<0.3V, the off-current is insensitive to the gate bias but dependent on the drain bias. The experimental work shows that the drain junction diode is also temperature insensitive especially in the conditions of relatively high drain bias and low temperature as illustrated in Fig 3.23 (a) with the junction doping profile in (b). This provides the evidence of the band-to-band tunnelling as the dominating junction leakage mechanism. The weak temperature dependence also suggests that the thermal generation does not have the dominating role in the given condition as it is stronger temperature and carrier life time sensitive. However the weak temperature dependence shown is mostly-likely attributed to traps assisted tunnelling [54].

(a) (b)

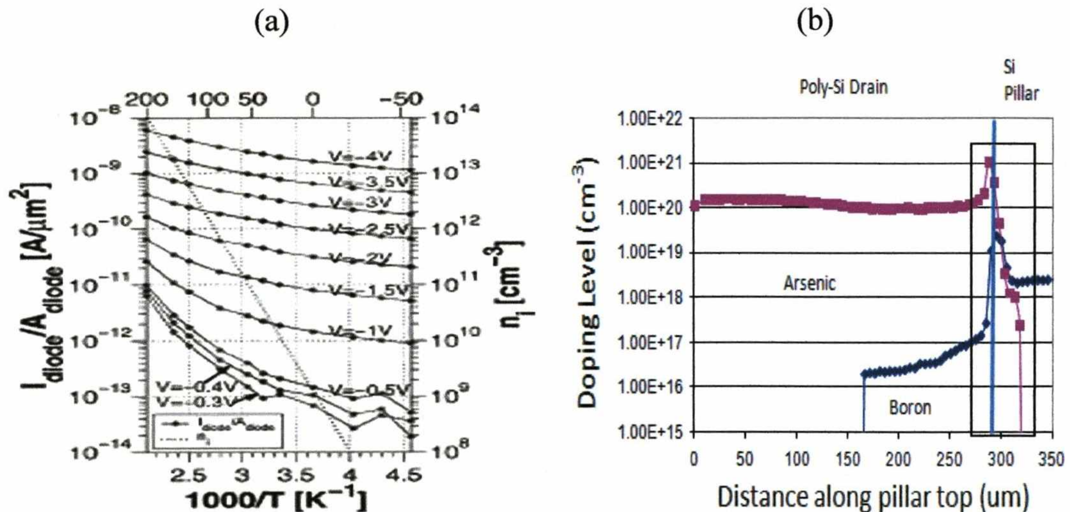



Fig 3.23 (a) Reciprocal temperature dependence of the large-area drain diode leakage for different values of reverse bias. The doping level in a drain junction at the pillar top is squared in (b). [66]

In the high negative gate bias region, the surface potential in the drain-gate overlap region increases further due to the increasing vertical field from the higher gate bias. As a result the surface band-bending eventually exceeds the silicon band gap $E_g$ (1.12V) and bends further with increasing gate bias. The band diagram at the junction surface in the Si drain side is illustrated in Fig 3.24. Consequently with the presence of increasing electric

field strength, more electrons are able to tunnel from the drain valence band to the drain conduction band, thus generating an electron-hole pair. Both carriers are swept away by the high drain electric field and thereafter holes are collected by the body contact and electrons are collected by the drain contact. The dependence of band-to-band tunnelling rate on the increasing field has been developed in [67]. The band-to-band tunnelling rate in the GIDL model directly determines the GIDL current density as expressed by the equation 2.29. The simulation fit indicates the presence of band-to-band tunnelling in the JS device drain-substrate junction but with very low tunnelling rate which needs to be 1000 times lower than the default model. This further indicates that the junction boundary doping is not abrupt and in fact gradually varies from $1\text{x}10^{20}\text{cm}^{-3}$ to $3\text{x}10^{18}\text{cm}^{-3}$ within 30nm which can be observed in Fig 3.23 (b).

## 3.3.4 Calibration of the On-Current

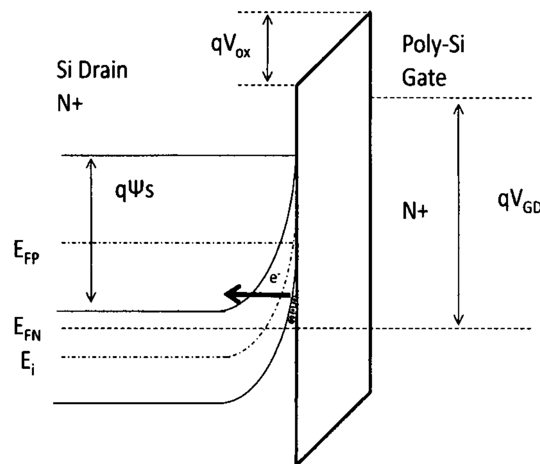



Fig 3.24 Band diagram of electron tunnelling in the drain junction surface region under high negative gate bias.

In the on-current region of the measured device, a striking aspect of the experimental transfer characteristics which has also demonstrated in other devices section 3.1.2, is that the on-current in DoT mode is much higher than SoT whilst in the other operating regimes it almost overlaps. This suggests the presence of additional series resistance in the top

junction. It is likely to be due to the presence of a thin unintentional native oxide layer beneath the polysilicon drain spacer and the silicon body. To further justify this hypothesis, an external resistance, $R_{add}$ is added to the drain contact. As a result, reasonable agreement can be obtained between simulation and experimental on-current at $V_{GS}$=2.5V in the high gate bias region for SoT mode with $R_{add}$ of the order about 80kΩ/um. By simulating the on-current in DoT, a severe limitation of current is apparent Despite that, the trend of on-current asymmetry in DoT and SoT modes can still be observed similar to that of the measured device. The lower on-current in SoT mode is because of the fact that the effective gate-source voltage as the additional resistance causes the intrinsic source contact to become positively biased. This bias also leads to a threshold voltage increase due to the body effect; both effects leading to less current drivability. The above variation of the source-gate effective voltage can be understood with assistance from a schematic diagram of the series resistances connection shown in Fig 3.25 for SoT mode. The on-current asymmetry can also be explained by the asymmetry of $V_T$ under high drain bias: 1.15V in DoT and 1.3V in SoT. In order to eliminate this additional resistance, a cleaner interface could be obtained, either by depositing the spacer layer in a cluster tool after an in-situ surface clean or by using a high dose silicon ion implantation with a large tilt angle to break up the native oxide layer. It can be concluded that except for the on-current region, the fitting is reasonably good therefore a SCE simulation study can be conducted as long as the on-current region is avoided.

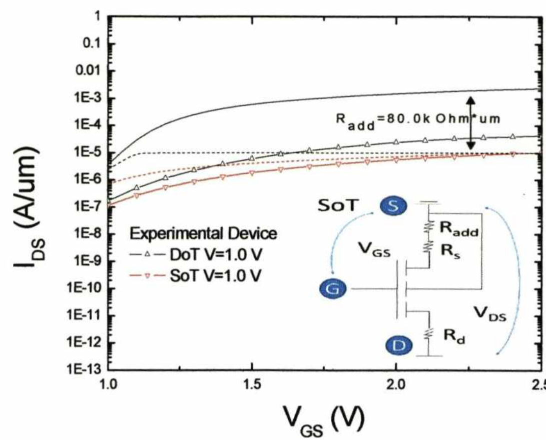



Fig 3.25 Simulated on-current vs. measured on-current: at $V_{GS}$=2.5V for SoT mode, they agree with each other; Both the simulated and measured on-currents give evidence of a lower value of current in SoT than in DoT modes. This is compatible with the presence of the additional resistance connected to the top junction region.

## 3.4 Summary

In this chapter, the DC characteristics of VMOSFETs with a junction stop structure, were examined experimentally and numerically. The JS serves to suppress bulk punch through and also allows acts as a hard mask to allow formation of a shallow top junction. The threshold voltages of most of the devices differ from the ideal, in a manner consistent with either gate oxide fixed charges or channel length variation. Through comparison of the transfer characteristics of devices on different process splits, the asymmetry of on-current in SoT and DoT modes was observed for all the devices. The presence of a parasitic series resistance at the top junction is a likely cause of the asymmetry. The experimental on-currents show that the best value is still 26 times lower than the ITRS value at the same technology node. The sub-threshold slopes for $V_{DS}$=1V in the devices of split # 5, 6, 8 show higher degradation for SoT compared to DoT mode due to the presence of a high level of interface-state density along the pillar sidewalls at the pillar top, as a result of over-etching of the polysilicon gate. The higher substrate current in split # 1,5,6,7 (20nm JS thickness) is observed in SoT mode than DoT mode suggesting that the

presence of JS effectively suppresses the impact ionization at the top junction. In the split # 3 (10nm JS thickness) and # 8 (no JS) the substrate current difference between SoT and DoT modes is not so big due to the absence of the JS. Moreover, in these devices, the breakdown voltages are smaller in SoT again pointing to the beneficial effects of the JS. The direct tunnelling mechanism was observed to dominate the gate oxide leakage for regions between the gate and drain, body and source. The DT mechanism dominance of the leakage in the 3nm oxide was proven by the functional fitting of direct tunnelling theory to the experimental data and also its weak dependence on temperature.

A 2D numerical simulation was conducted with the Atlas Silvaco simulation package and an attempt was made for calibration with the fabricated devices. The models underlying non-classical phenomena were carefully selected for simulating the carrier energy and transportation statistics more accurately in a 70nm device. The fitting of the simulation to experimental data in different transistor operational regimes provided a brief understanding of device properties such as fixed oxide charge, interface-state density, junction boundary doping abruptness, band-to-band tunnelling rate near the top junction and anomalously low on-current. The simulation further served to confirm the likely presence of a parasitic series resistance in the top junction which is the cause of low on-current and asymmetry between SoT and DoT modes. Modifications to the process were suggested, to avoid this parasitic resistance.

# Chapter 4

# Short Channel Effects in Vertical MOSFETs with a Junction Stop

## 4.1 Introduction

A fundamental problem of vertical MOSFETs is inherently deep junctions that exacerbate short channel effects (SCEs). In the last chapter electrical characteristics of fabricated vertical MOSFET with junction stop (JS) were explored. It is evidently that JS serves to suppress the impact ionization at the top junction. The formation of the junction stop is realized by a self-aligned oxide region which is formed at the pillar top and acts as a diffusion barrier for shallow junction formation. In this chapter the work of [39], [40] is extended and a comprehensive study of the effects of asymmetric junction depths on short channel effects (SCEs) in vertical MOSFETs is presented. The benefits of using a JS structure in vertical MOSFETs for improving SCEs immunity are demonstrated by simulations which show clearly the effect of the top junction on SCEs and bulk punch-through. The JS structure allows the formation of a shallow drain junction, thus mitigating the problems of SCEs namely the charge sharing effect (CS) and drain induced barrier lowering (DIBL). The JS also reduces the propensity for single transistor latch, which is related to deep junctions, as well as preventing drain dopant encroachment in the middle of the pillar, which would further exacerbate bulk punch-through. Finally, the JS reduces the drain-substrate parasitic capacitance.

In [39] the electrostatic influence of the JS in a device without significant out-diffusion from the drain contact was explored. In that case, the JS oxide influenced significantly the electrostatics of the drain region, although a very low thermal budget process would be required to minimize out-diffusion. In [68], the impact of JS on SCE has been observed experimentally from a p-type 50nm device. However, the underlying physics associated with junction depth is not fully explained. In this work, specific role of the junction stop and associated out-diffused drain region which is controlled to produce a shallow top

junction is explored in some detail. According to the general guidelines for junction depth in the roadmap [69], SCEs deteriorate with increasing junction depth. Nevertheless, little work is reported into the underlying physics. In section 4.2 therefore, numerical simulation is used to present a detailed analysis of junction depth leverage on SCEs in VMOSFETs. The study is also relevant to conventional lateral MOSFETs with symmetric junction depths. The advantages of the VMOSFET-JS are quantified in section 4.3, where it is demonstrated, how to design the junction stop architecture to suppress SCEs and bulk punch-through. The results show that with a shallow drain junction formed by a JS, the charge sharing can be improved by more than 50mV and the DIBL by nearly 50mV for a 70nm channel length and a body doping of $1x10^{18}cm^{-3}$. Furthermore, the incorporation of a JS allows a reduction of the body doping in a VMOSFET-JS whilst maintaining similar SCEs to a VMOSFET, thus improving the on-current. The limit of the influence of junction depth on both charge sharing and DIBL is considered in Section 4.4.

## 4.2 Junction effects on CS and DIBL in A Conventional VMOSFET

A vertical n-MOSFET with a deep top junction spanning over the pillar top and a lateral n-MOSFET are compared for a body doping of $1x10^{18}cm^{-3}$, a channel length of 70nm and a gate oxide thickness of 2nm. The VMOSFET has a constant top junction depth which is 250nm. The bottom junction depth was varied from 5nm to 100nm, with an abrupt junction doping profile. The fixed oxide charge, interface trap densities, and band-to-band tunneling rate are defined using the semi-calibrated values from the previous study. The CS (charge sharing) was evaluated from the threshold voltage shift, $\Delta V_T$ at

$V_{DS}$=50mV. The threshold voltage was extracted using the linear extrapolation method under low drain bias (50mV) and $\Delta V_T$ was then given by the deviation from the long channel value. The DIBL was evaluated from the gate voltage shift in transfer characteristics of high drain biases of 1V at zero gate bias and low drain bias of 50mV at a gate bias for the same sub-threshold drain current.

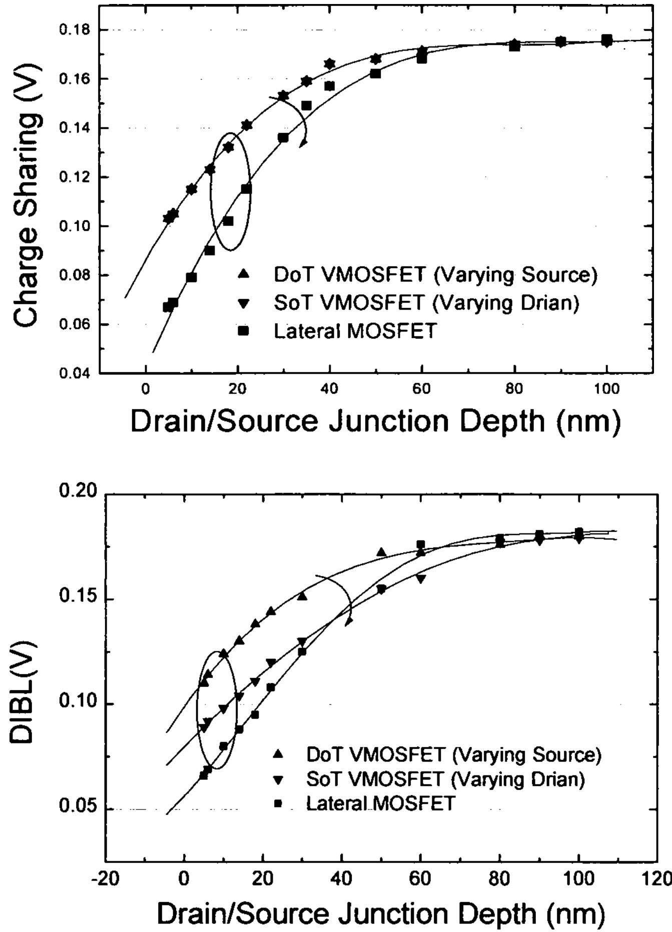



Fig 4.1 (a) Charge sharing and (b) DIBL as a function of bottom junction depth for a VMOSFET and a conventional lateral MOSFET. Three cases are compared: (1) a VMOSFET in DoT configuration; (2) a VMOSFET in SoT configuration; (3) a conventional lateral MOSFET with identical drain and source junction depths. The devices were simulated with $V_{DS}$=50mV and $V_{GS}$=1V for charge sharing and $V_{DS}$=1V and $V_{GS}$=0V for DIBL.

As highlighted in [70, 71, 72], one of the unique characteristics of a VMOSFET with an implanted source and drain is the natural asymmetry of the junctions, with a deep top junction usually covering the whole pillar width. The bottom junction is variable and

dependent on lateral dopant diffusion. Because the junction depth has become an important parameter in controlling the threshold voltage shift due to SCEs, it is worthwhile making a comparison between vertical devices with asymmetric junctions and lateral devices with symmetric junctions with regard to CS and DIBL. In order to investigate the effect of junction depth on the SCEs only, the uniform body doping level was set to be $1\text{x}10^{18}\text{cm}^{-3}$ in the simulations and an abrupt junction was utilized. For the VMOSFET, the top junction spans the top of the 250nm wide pillar and is therefore very deep. The bottom junction depth is defined by the extent of the lateral encroachment of the bottom junction beyond the edge of the vertical pillar.

Fig 4.1 shows CS and DIBL as a function of bottom junction depth for a VMOSFET and a conventional lateral MOSFET. The smaller DIBL and CS values for the conventional lateral MOSFET indicate the superiority of using symmetrical junctions. However, the DIBL curve for the case of variable drain junction depth in SoT configuration, illustrates a similar behaviour to that of the symmetrical structure. All three curves also show similar limiting behaviour at large drain/source junction depths for both DIBL and CS. The physical reason behind the latter phenomenon is analyzed in some detail in section 4.4. For the case of varying source junction depth, the source junction has less influence on the DIBL than the drain junction. Consequently it can be pointed out that in vertical MOSFETs, it is more desirable to have a shallow drain junction on top of the pillar. The SoT configuration gives better DIBL than the DoT configuration. However, good control of both CS and DIBL is desirable for both configurations and this is explored in the next section.

## 4.3 Junction Depth Design in a VMOSFET-JS

A vertical MOSFET with a shallow top junction is achieved using the proposed junction stop architecture illustrated in Fig 3.1. The aim of this proposed JS architecture is to assess the benefits of a shallow drain junction in VMOSFETs using a CMOS compatible process. This approach also brings the advantage of forming a relatively symmetrical structure which is also important for pass transistor implementation in circuits. The drain spacer width, the gap between the JS and the gate oxide depicted in Fig 3.1 is found to be a critical in defining the junction depth. In the simulations of the VMOSFET-JS, the drain spacer width is varied from 3nm to 80nm yielding a drain junction depth in the range 5nm to 100nm. The junction stop has a thickness of 20nm. Simulation results of SCEs are shown in Fig 4.2 for devices biased in the DoT configuration with different JS spacer widths and therefore different drain junction depths. The devices have a body doping of $1 \times 10^{18} cm^{-3}$ and a 30nm source junction depth. The results indicate that when the drain junction depth exceeds 50-60nm (drain spacer width of around 30nm), the JS loses electrical influence on the SCEs and the device behaves as a 'conventional' vertical MOSFET. When the drain junction depth is reduced to 20nm, the CS and the DIBL are reduced by nearly 50mV.

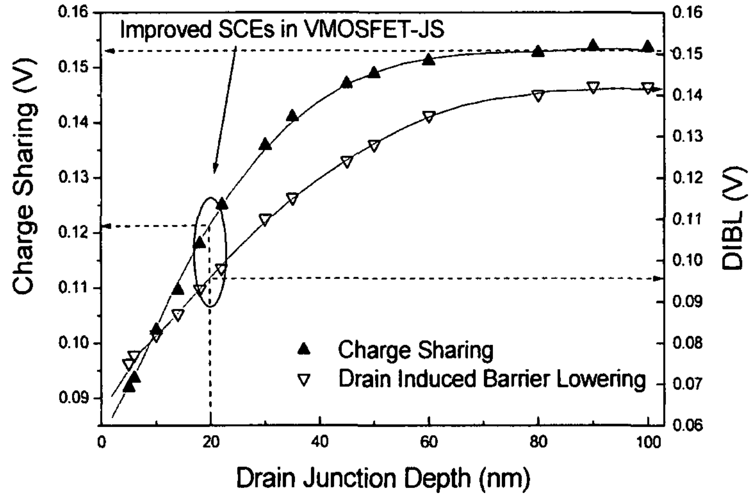



Fig 4.2 Simulations of DIBL and CS as a function of reducing drain junction depth in a vertical MOSFET with a junction stop (VMOSFET-JS). Improved SCEs are obtained for shallower drain junctions. All the devices are biased in DoT configuration, with a body doping of $1\times10^{18}cm^{-3}$ and a source junction depth of 30nm.

A further advantage of the JS is that it allows the channel doping to be decreased. Fig 4.3 shows simulations of DIBL for VMOSFETs with and without a JS in the DoT configuration, as a function of body doping. In this case, the JS devices have symmetric drain/source junction depths which are both 30nm. It is observed that a VMOSFET with a

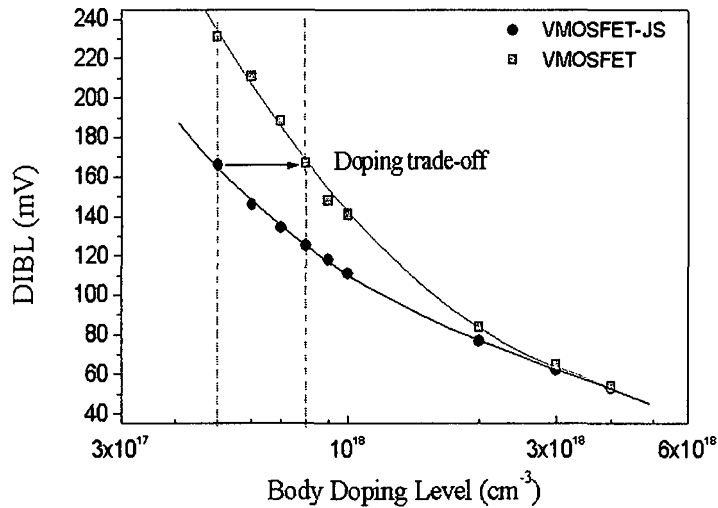



Fig 4.3 DIBL as a function of body doping for VMOSFETs and VMOSFET-JSs. The devices are simulated in DoT configuration with a symmetrical drain/source junction depth of 30nm.

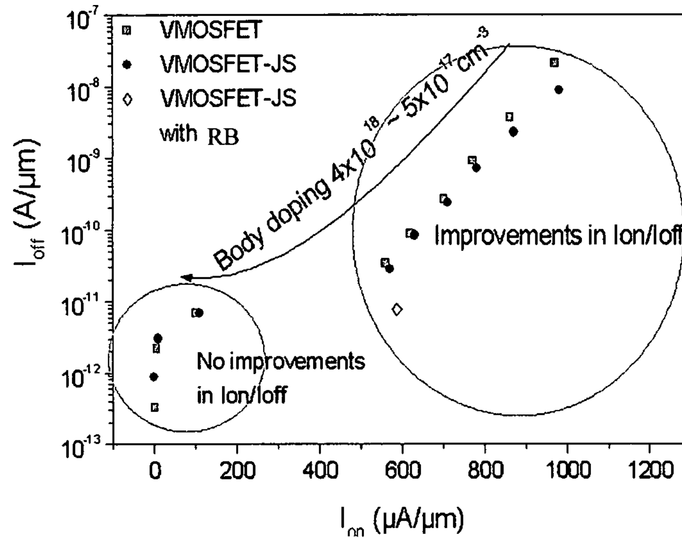



Fig 4.4 $I_{off}$ as a function of Ion for VMOSFET and VMOSFET-JS devices with different body doping levels. The arrow shows the direction of increasing body doping. Also shown is a point for a retrograde body VMOSFET-JS (VMOSFET-JS with RB) with a channel doping of $5\times10^{16}cm^{-3}$ and a body doping of $4\times10^{18}cm^{-3}$.

body doping of $7x10^{17}cm^{-3}$ demonstrates a DIBL value of 166mV, but the same value can be achieved with body doping of $5x10^{17}cm^{-3}$ if a JS is incorporated.

The simulation results above have demonstrated the increasing efficacy of the JS on DIBL control in devices with lower body doping. Lower channel doping yields higher channel mobility, thus a doping trade-off can be enabled to enhance the $I_{on}/I_{off}$ ratio. Note that $I_{on}$ was taken at $V_{DS}=V_{GS}=1.0V$. The benefits are shown in Fig 4.4 where $I_{on}$ vs. $I_{off}$ is plotted for both VMOSFETs and VMOSFET-JSs. For high body doping (left hand side of the graph) the JS provides little improvement in the $I_{on}/I_{off}$ ratio, but at low body doping (right hand side of the graph) the JS gives a significant improvement in the $I_{on}/I_{off}$ ratio. For body dopings of $5.0x10^{17}cm^{-3}$ and $6.0x10^{17}cm^{-3}$ the JS gives improvements in $I_{off}$ of 58.7% and 37.8% respectively for a given $I_{on}$. Note in the fabricated device shows a much lower $I_{on}$ due to a high body doping and large series resistance caused by the native oxide grown between the poly drain and the silicon body.

As described in [73], the JS process also facilitates integration of a retrograde channel. To investigate the benefits of a retrograde channel, a VMOSFET-JS with a highly doped

body ($4x10^{18}cm^{-3}$) and a low doped channel ($5x10^{16}cm^{-3}$) has been simulated. The drain and source junction depths are both 30nm. The $I_{on}/I_{off}$ level for this structure is shown by the diamond symbol in Fig 4.4, with a value of 586 μA/um for $I_{on}$ and 7.64 $x10^{-12}$A/um for $I_{off}$, which compares with values of 0.2 μA/um and 3.3 $x10^{-13}$ A/um for the equivalent device without a retrograde channel. The advantage of the JS-retrograde channel structure is clear, in that it enables a further increase in $I_{on}$ for a slightly increased $I_{off}$ by enhancing the channel mobility without significantly degrading the SCEs and bulk punch-through.

The electrical influence of the JS on bulk punch-through is illustrated by simulating the transverse electric field strength along the source junction as shown by the cut line in Fig 4.5 (a). The simulated field strength at the source junction which has a direction against the field from the drain is shown in Fig 4.5 (b). The transverse electric field is simulated along the source junction for VMOSFET and VMOSFET-JS devices with deep and shallow source junctions. The junction stop suppresses bulk punch-through by screening the electric field penetration from the drain contact and so reducing the depletion region encroachment from the drain. This is apparent from the increase in the absolute value of the source junction electric field in the JS structure compared to the conventional structure. Higher field strength at the source junction in the JS structure means a higher source

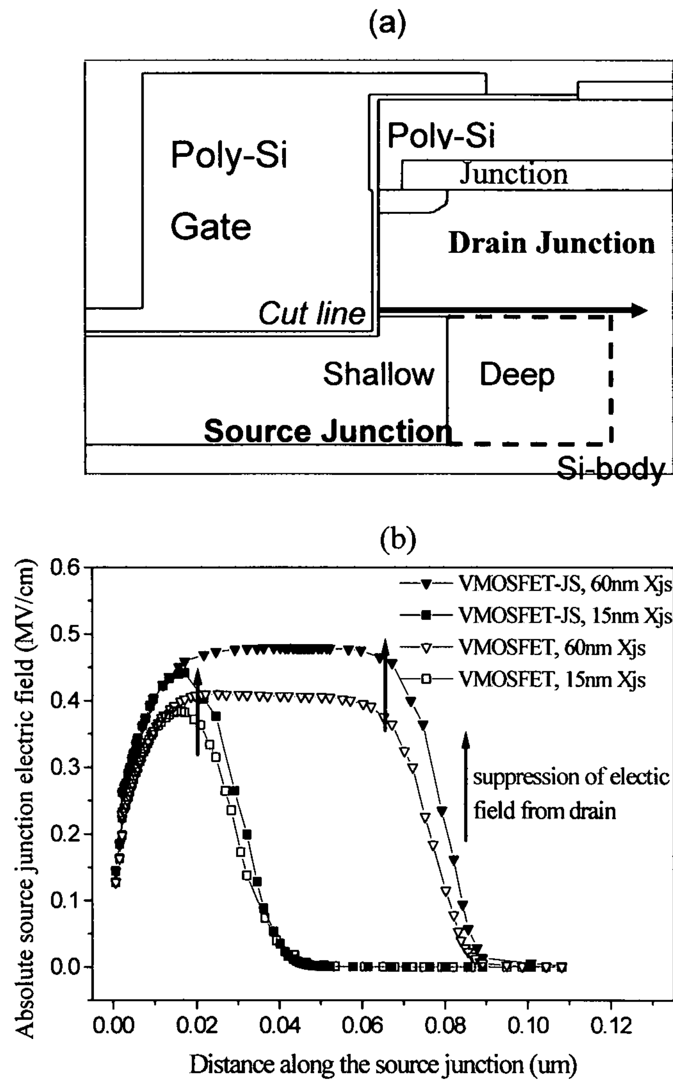



Fig 4.5 (a) Cross-section of the simulated devices showing the cut line along which the source electric field was simulated (b) Absolute source junction field as a function of distance along the source for VMOSFET and VMOSFET-JS devices with 60nm and 15nm source junctions. The device was biased in DoT configuration with $V_{DS}$=1V and $V_{GS}$=50mV.

barrier against minority carrier injection in the bulk region and thus a better immunity against bulk punch-through.

## 4.4 Discussion

Numerical and analytical studies [74, 75, 46, 76] have been reported that use simplified expressions for short channel effect modeling and recently, associated scaling trends have been summarised in [77]. In a recent report on modeling SCEs in small geometry lateral

devices [78], the influence of junction depths was investigated whereby the channel depletion region width was fixed by an "undoped" channel region. The influence of various channel depletion widths was included in the study of [79] by modeling the sub-threshold region using the voltage transform (VDT) approach. Here, the study is further extended to clearly define the critical point where SCEs become insensitive to the variation of the drain junction depth in the case of a VMOSFET-JS with various channel depletion region widths.

### 4.4.1 Drain Junction Depth Effects on CS

Firstly the charge sharing effect which arises due to the built-in potentials of the junctions in the channel region is considered. The dependence of CS on drain junction depth, $X_{jd}$ was shown in Fig 4.2. It is difficult to define accurately the shared regions geometrically, as shown in Fig 4.6, where a 70nm VMOSFET-JS with a bodying of $1x10^{18}cm^{-3}$ is simulated. For this reason changes in the surface potential are considered instead. The minimum surface potential determines the minority carrier injection rate into the channel, therefore the shift of minimum surface potential $\Delta\psi_{min}$ determines the threshold voltage shift. It is informative therefore to investigate the shape of the channel surface potential by plotting the conduction energy band diagram and results are shown in Fig 4.7 (a). Note that the simulated device has a structure as described in Fig 4.6 with a various top junction and a fixed bottom junction; it was biased at $V_{DS}$=50mV and $V_{GS}$=1V with zero substrate bias. Also the drain is assigned to the top of the pillar. By comparing the conduction band diagrams for deep and shallow drain junctions, it is observed that for junctions with depths that are comparable to or greater than a critical point, the surface conduction bands overlap. Shallower junctions are then very sensitive to variation in

junction depth. The minimum space surface potential, $\psi_{min}$ against drain junction depth is plotted in Fig 4.8. It is apparent that increasing junction depth degrades the charge sharing effects, with saturation of the effect at about $X_{jd}$ = 52nm. This critical value is defined as the point where 90% of the maximum $\Delta V_T$ is reached.

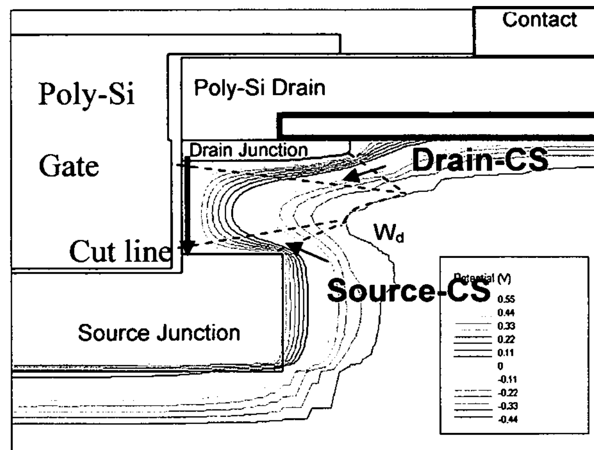



Fig 4.6 Simulated potential contours in a VMOSFET-JS device with asymmetrical drain and source junctions. The device has a top junction depth of 50nm, a bottom junction depth of 30nm and a body doping level of $1x10^{18}cm^{-3}$. The drain and source controlled charge sharing regions (CS) are also defined at a low drain bias (50mV).

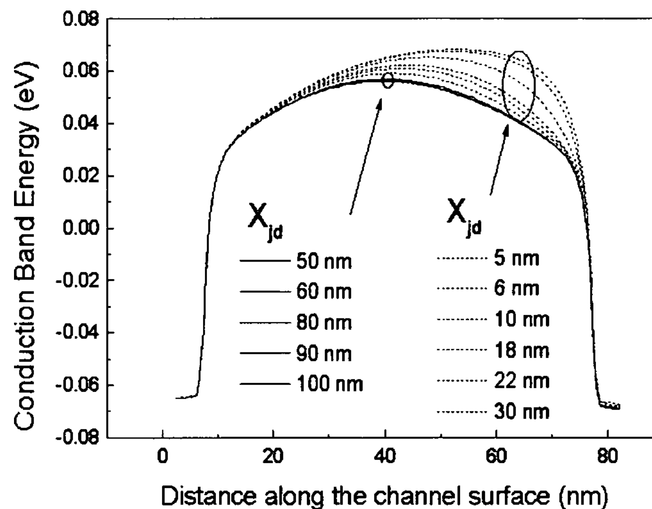



Fig 4.7 Conduction band energy (cut line shown in Fig 7) as a function of distance along the channel for MOSFET-JS devices with different drain junction depths ($X_{jd}$).

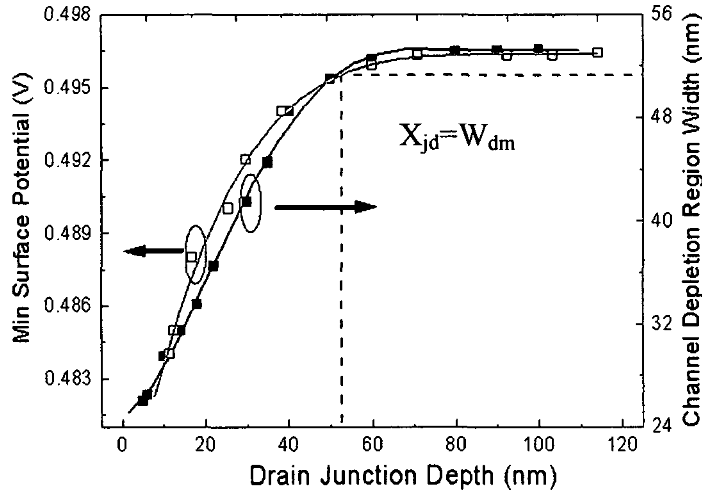



Fig 4.8 Minimum surface potential and channel depletion region width as a function of drain junction depth for a MOSFET-JS device simulated with $V_{DS}$=50mV and $V_{GS}$=1V in DoT configuration.

The dependence of channel depletion width on drain junction depth is also shown in Fig 4.8. In the region before the channel depletion region width reaches a constant value, the relationship between $X_{jd}$ and $W_{dm}$ can be summarized with the analytical expression shown below.

$$W_{dm} \approx \frac{10}{1 + 0.2 \cdot X_{jd}} \cdot X_{jd} \qquad \text{Eq. 4.1}$$

Therefore the ratio of $W_{dm}$ to $X_{jd}$ decreases as $X_{jd}$ increases. After the critical point, where the $X_{jd}$ has a depth equal to $W_{dm}$, the variation of $W_{dm}$ becomes independent of $X_{jd}$.

The critical point can be physically understood in terms of the varying channel depletion region edge with assistance from Fig 4.6. As the junction depth increases, the channel depletion region expands until a critical point is reached when further increase of $X_{jd}$ exceeds $W_{dm}$. At this point, $X_{jd}$ no longer affects the surface potential and thus the geometry of the channel depletion region. As a result, the triangular charge sharing area in Fig 4.6 stays constant and consequently the threshold voltage shift also stays constant.

## 4.4.2 Drain Junction Depth Effects on DIBL

The simulated drain induced barrier lowering (DIBL) values show a similar behaviour to that of CS. This was illustrated in Fig 4.2 where the influence of the drain junction depth on DIBL also reaches a critical point after which the DIBL effect saturates. This result is consistent with that of the simulation study in [79] for the case of an undoped retrograde channel region.

The junction effect on DIBL shows the movement of the critical point to a higher value (62nm) than that for CS. This is caused by the lateral encroachment of the drain field with drain bias which increases the value of minimum surface potential $\psi_{\min}$ and therefore the maximum channel depletion region width. As the drain junction depth increases, the position of $\psi_{\min}$ in the channel moves towards the source, as shown in Fig 4.9 and the band diagrams eventually overlap indicating the saturation of the influence of junction depth.

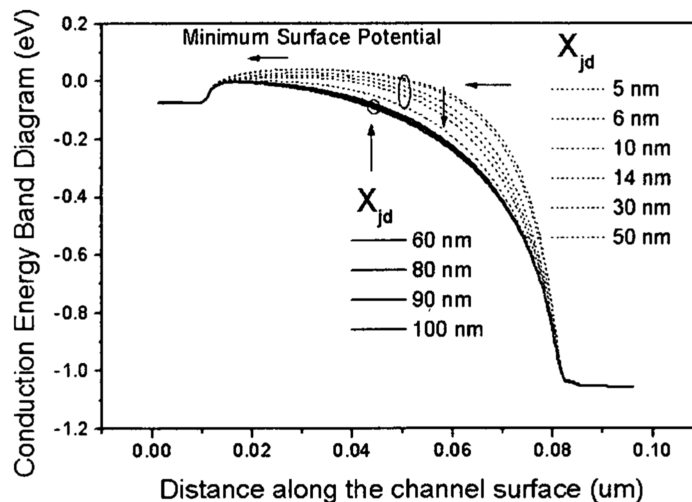



Fig 4.9 Conduction band energy as a function of distance along the body surface for VMOSFET-JS devices with different drain junction depths ($X_{jd}$). The device was simulated with $V_{DS}$=1V and $V_{GS}$=50mV in DoT configuration.

The limit of the influence of junction depth on both CS and DIBL suggests that for a VMOSFET-JS design in a particular technology node, a shallower drain junction in the deep depth regime (above $W_d$) allocated by the spacer width does not necessarily improve the SCEs. Therefore an analytical concern on relating the drain spacer width to depletion region width is required for future VMOSFET-JS design.

In the other hand, some reports such as [80] suggest that if $X_j$ is included into the scaling rule as an empirical element in determining characteristic channel length then the improvement in short channel immunity by using shallow junctions essentially means a longer effective gate length. For the junction depth itself, some other experimental data showed that short channel immunity is insensitive to junction depth if an effective gate length is used instead of a physical length of the poly-crystalline silicon gate [81]. However, these analyses are normally not straight forward for device design purpose.

## 4.5 Summary

In this chapter, short channel effects in VMOSFETs have been systematically studied using 2D numerical simulation. It is shown that the naturally occurring asymmetry of the junctions is detrimental to the control of SCEs. The study also indicates the advantage of employing a drain-on-bottom configuration for the suppression of DIBL. The junction stop structure provides significantly better SCE control and bulk punch-through immunity compared to the conventional vertical device. The simulation results also have indicated that it is possible to provide a trade-off between the junction stop and body doping to reduce DIBL which can lead to an improved $I_{on}/I_{off}$ ratio. Furthermore, the inclusion of a retrograde channel in the JS structure gives a further significant improvement in the device $I_{on}/I_{off}$ performance. In a VMOSFET with a junction stop, it is important to control

accurately the drain spacer width which is the key parameter for controlling the depth of the top junction. The effect of drain junction depth on SCEs in VMOSFET-JS devices is also investigated in some detail. A critical point has been defined at which the SCEs saturate with increasing drain junction depth. As a result, this study has provided a methodology for optimizing the junction depths of VMOSFET-JS devices.

# Chapter 5

# VMOSFETs with Novel Structures

## 5.1 Ultra Thin Pillar Vertical MOSFET with FILOX

Thin body multi-gate devices are promising for scaling CMOS devices into the nanoscale regime. Vertical transistors are one approach for the implementation of multi-gate CMOS, because double or surround gates can easily be incorporated, enabling increased packing density at a defined lithographical node as compared to standard CMOS transistors. Introduced in Chapter 1, a simple self-aligned process was proposed to reduce the parasitic capacitance in vertical MOSFETs using nitride spacers on the sidewalls of the vertical pillar and a local oxidation. This Fillet Local Oxidation (FILOX) process delivered a five times reduction in overlap capacitance compared with devices without the FILOX process.

In the past, the FILOX process was applied to very thick pillars, where the generation of stress by the nitride spacer and the local oxidation was not an issue. However for ultimate scaled CMOS, very thin pillars are required to provide a fully depleted body, which gives improved electrostatic control over the channel and hence improved short-channel effects. In this case, stress arising from the nitride spacer and the local oxidation would be a major concern on the viability of the technology. In this chapter, a technology which is able to reduce the overlap capacitance in ultra-thin pillar vertical MOSFETs is investigated. The technology is demonstrated by the fabrication of ultra-thin pillar (UTP) capacitors with a TiN surround gate. Electrical characterisation of the capacitors is performed in UTP pillar capacitors and planar test capacitors.

### 5.1.1 Technology Description

Fig. 5.1 shows a schematic of the process flow for the fabrication of the ultra-thin pillar capacitors with a TiN surround gate which are fabricated by our collaborators at the Southampton University. Pillars with thicknesses down to 20 nm were defined using electron beam lithography and an anisotropic etch was used to create the ultra-thin pillars (b). A thin, stress-relief oxide was then grown and a silicon nitride layer deposited by chemical vapor deposition and anisotropically etched to expose the stress relief oxide on the horizontal surfaces and to leave nitride spacers on the sidewalls of the pillars (c). Local oxidation was performed for different times to give FILOX oxide thicknesses in the range 8-40 nm (d). After removal of the nitride spacers by wet etching, a thermal gate oxide was grown and a TiN layer was deposited and anisotropically etched to create the surround gate (e). Fig 5.2 shows an SEM cross-section through the vertical edge of a completed pillar capacitor test structure. The FILOX oxide can be seen on the horizontal surface at the bottom of the pillar and the TiN surround gate can be seen on the pillar sidewall.

Each UTP capacitor test structure incorporates 200 ultra-thin pillars with surround gate, as shown schematically in Fig 5.3. Each pillar has a width of 10 μm and a height of about 0.22 μm. The arrangement allows the capacitance to be measured from the vertical gate metal to the substrate and includes the influence of any encroachment by FILOX. The gates are deposited along vertical sidewalls only. Two sets of capacitors were tested, where one has varying FILOX thicknesses and the other one has varying pillar thicknesses. The "pillar bottom" (PB) planar capacitor test structure is illustrated in Fig. 5.4 where the gate covers the entire planner and perpendicular area. According to the geometries, the area for UTP was estimated to be 50,262 $um^2$ while for PB the area is 50,907 $um^2$.

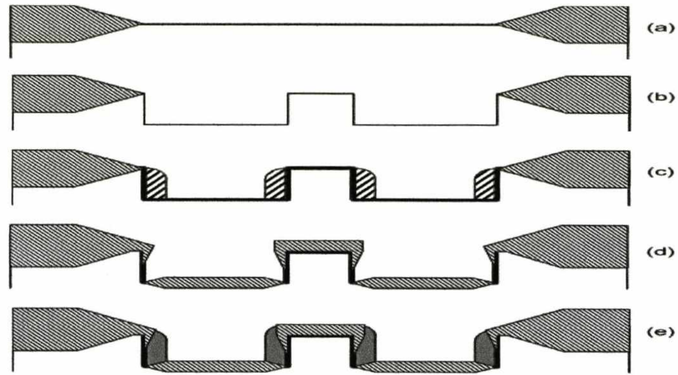



Fig 5.1 Process flow for fabrication of TiN surround-gate, ultra-thin pillar. [82]

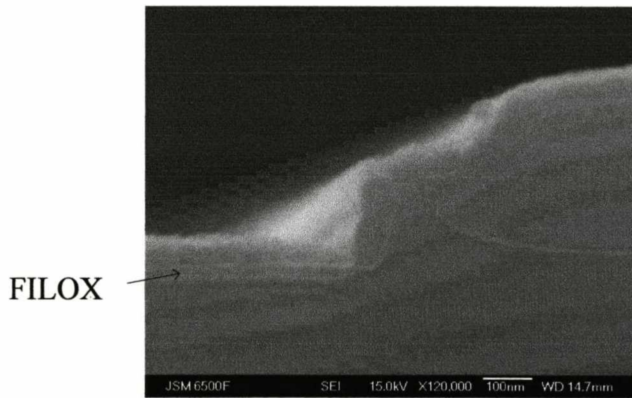



Fig 5.2 SEM cross-section through a vertical edge of a pillar capacitor test structure. [82]

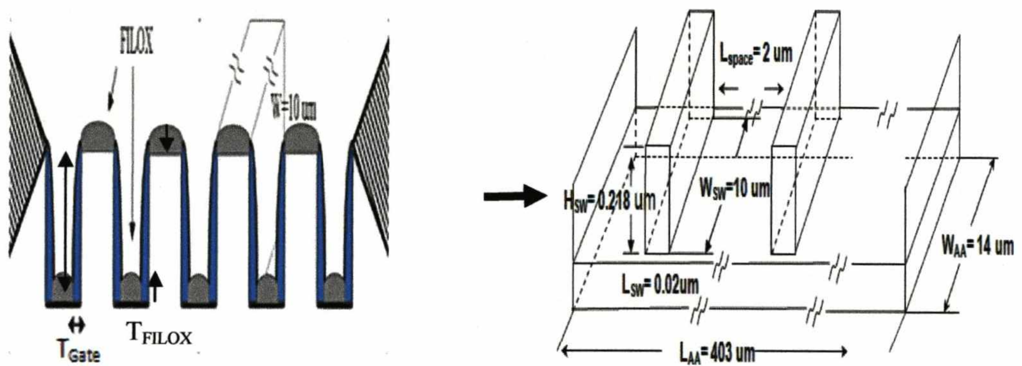



Fig 5.3 Test structure of surrounded gate pillar capacitor (fully depleted device); $t_{ox}$ = 8.0nm, $t_{FILOX}$ = 8.3nm.

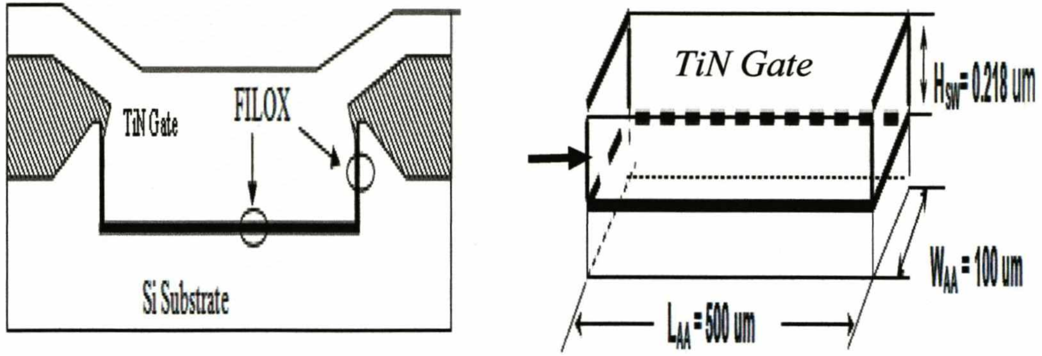



Fig 5.4 Test structure of a pillar bottom capacitor where $H_{SW}$: the height of a pillar.

## 5.1.2 Capacitance-Voltage Measurements

It is shown in Fig 5.5 that the 20 nm thick UTP capacitors with 8 nm thin FILOX exhibit recognizable C-V characteristics. However, the 20 nm thick pillar capacitors with 16nm, 24nm and 37 nm thick FILOX show less reasonably behaved C-V characteristics where the flat band voltage and the $C_{min}$ are different in the low(quasi-static) and high frequency curves. The reason is unclear. The lack of saturation in accumulation is likely due to the impact of leakage in these small value capacitors. The gate oxide thickness varies in a manner dependent on the FILOX thicknesses and the associated oxide encroachment under the gate, known as the bird's beak. The average gate oxide thicknesses enhanced by encroachment were estimated from $C_{acc}$ from C-V plots, as approximately 8nm, 10nm, 13nm and 15nm corresponding to FILOX thickness of 8nm, 16nm, 24nm and 37nm respectively. The FILOX thicknesses were informed by ellipsometry and SEM [82]. The oxide leakage for UTP capacitors fabricated by different FILOX processes is shown in Fig 5.6. Electron injection is from the gate electrode. It is observed that for devices with four different FILOX thicknesses, the leakage levels are of the order 1 pA until the leakage level becomes visible at circa 6-7 MV/cm, apart from the 37nm thick sample. The upturn in oxide

leakage current at the high gate bias is seen to reduce with the increasing thickness of FILOX, leading to an increasing average gate oxide thickness. However, for the device with 37 nm FILOX thickness, the leakage current becomes evident at a lower gate voltage and in fact almost coincides with the curve for the device with 8 nm FILOX at the same gate bias. Both leakage currents reach a level of 10 nA at 8 V. The cause of this increasing oxide leakage may be related to a dislocation-induced leakage path [83]. Dislocations could arise as a result of mechanical stress induced by the FILOX process, as suggested from early research where the trace of silicon dislocation due to the stress is clearly seen in TEM [36]. A thicker FILOX will almost certainly generate more mechanical stress than thinner ones. The simulation in Fig 5.7 shows that the stress level along a cut line through a 40nm thick FILOX is over 30 times that of the 10nm thick FILOX near the pillar bottom region. In addition, the stress effect is likely to be the cause of the degradation in yield of working 20 nm ultra-thin pillar capacitors. The yield drops from 80% for 20 nm FILOX to 50% for 37 nm FILOX.

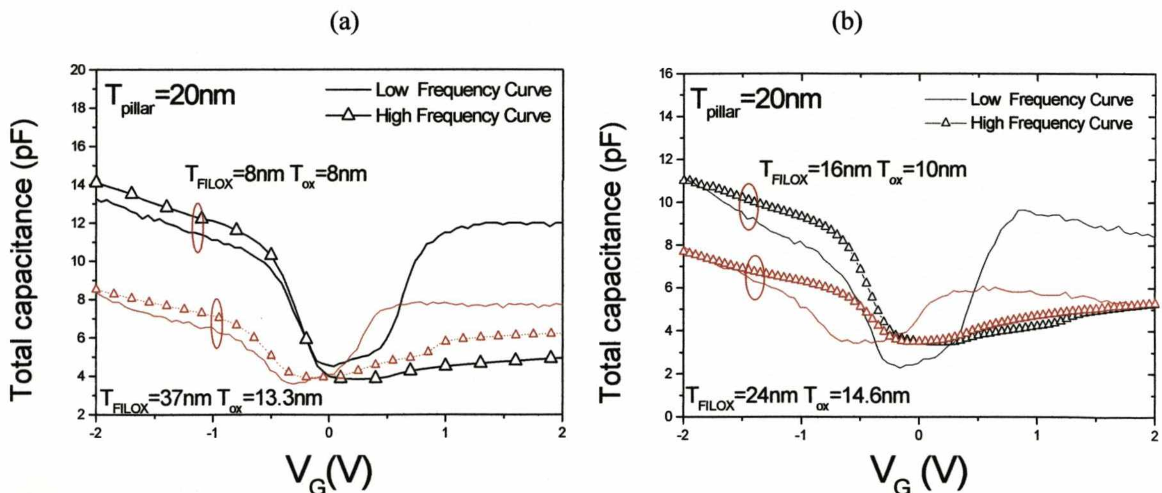



Fig 5.5 C-V characteristics of ultra-thin pillar capacitors with (a) 8nm vs. 37nm FILOX; (b)16nm vs. 24nm ($T_{pillar}$, $T_{FILOX}$, $T_{FILOX}$ represents the pillar, FILOX, average oxide thickness respectively. HF, LF represents the high, quasi-static state C-V curves respectively.)

Despite the above stress-related issue, ultra-thin pillar capacitors with 37 nm FILOX with various pillar thicknesses show a consistency in C-V characteristics as illustrated in Fig 5.8. This provides evidence that the FILOX process has been successfully applied to ultra-thin pillar devices without significantly degrading the electrical performance in thin pillar capacitors and indicates the potential of the technology.

Table 5.1 FILOX Thickness vs. Gate Oxide Thickness in UTP capacitors

| $T_{FILOX}$ (nm) | Average $T_{ox}$ (nm) |
|---|---|
| 8 | 8 |
| 16 | 10 |
| 24 | 14.6 |
| 37 | 13.3 |

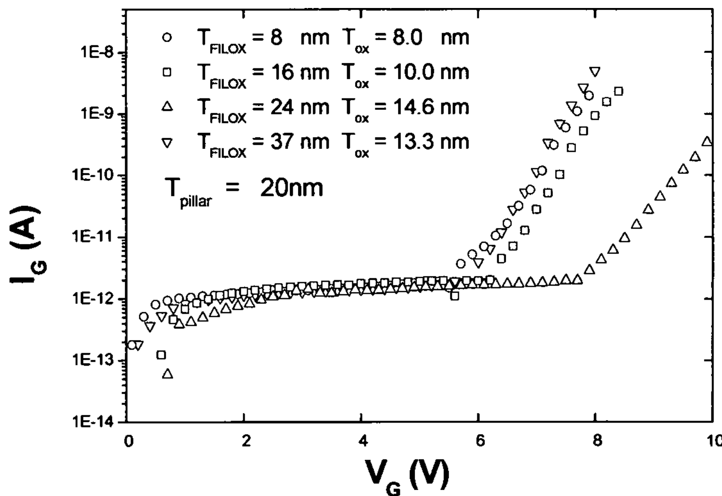



Fig 5.6 Gate oxide leakage current as a function of magnitude of negative gate bias on 20 nm ultra-thin pillar capacitors are with different FILOX thicknesses.

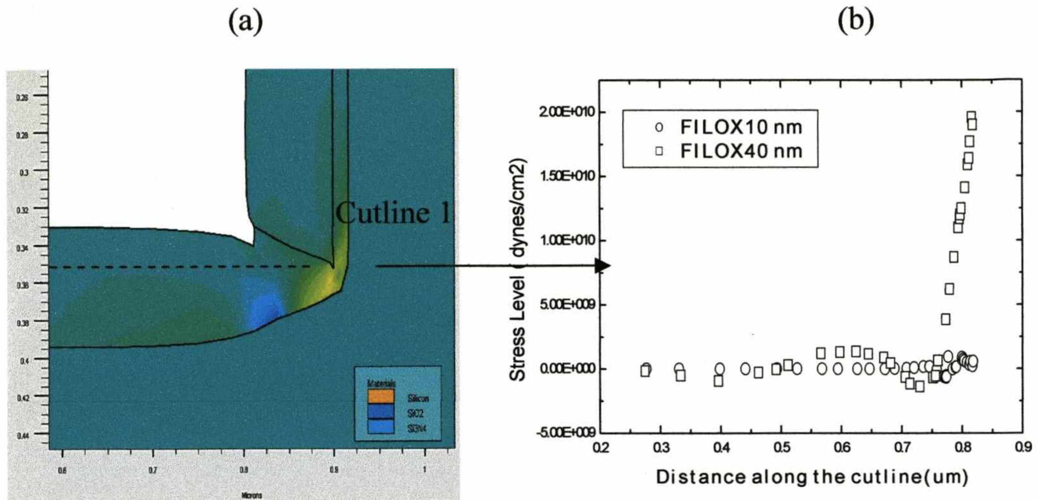



Fig 5.7 Mechanic stress comparison in 20 nm ultra-thin pillar capacitors with 10nm and 40nm thick FILOX.

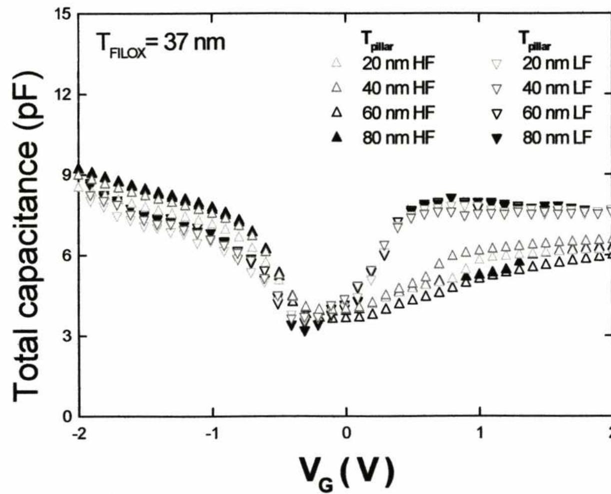



Fig 5.8 C-V characteristics of ultra-thin pillar capacitors with four different pillar thicknesses. FILOX thickness is 37 nm.

### 5.1.3 Other Capacitor Properties

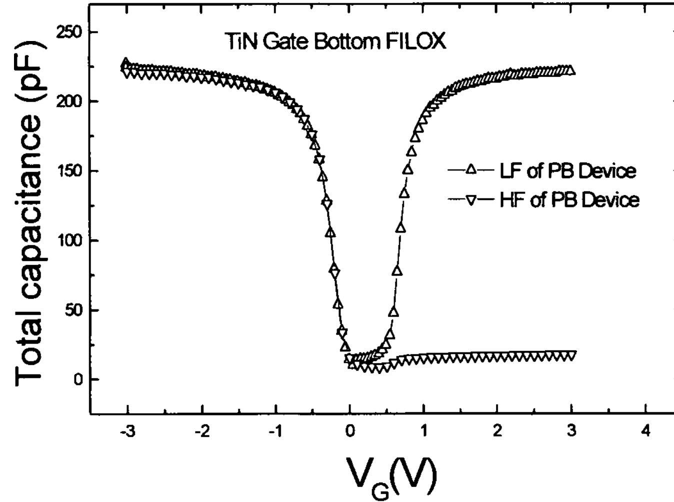



Fig 5.9 HF and LF curves for Pillar Bottom (PB) device with TiN gates.

Fig 5.9 illustrates the HF, LF curves of Pillar Bottom Devices with structures shown in Fig 5.4. The slight frequency dependence of the $C_{acc}$ is consistent with the influence of series resistance [84]. The nominal FILOX oxide thickness of 8.3nm, is used to calculate a device area of 5,4000 $um^2$. Because the FILOX thickness was assessed by ellipsometry, the accuracy of the oxide thickness on the planar surface of 8.3nm is considered to be reliable. Thus, compared to the expected area of 50,262 $um^2$, the effective area of the device should be increased by about 7%. It is suspected that the enlargement of the effective total area is due to edge effects associated with the LOCOS.

Using the quasi-static state curve of the UB sample illustrated in Fig 5.9, the $C_{min}$ and $C_{max}$ iteration method was used to find the doping density according to:

$$N_a = \frac{4}{A_G^2}\frac{kT}{q^2}\frac{1}{\varepsilon_o \varepsilon_s}\left[\frac{1}{C_{min}} - \frac{1}{C_{max}}\right]^{-2} \ln\left(\frac{N_a}{n_i}\right) \qquad \text{Eq. 5.1}$$

where $C_{min}$ and $C_{max}$ can be determined from the quasi-static state C-V plot; $A_G$ is the device area for the pillar bottom device.

The quasi-static state C-V plot indicates $C_{max}$ = 220 pF and $C_{min}$ = 8.7pF which is the capacitance when the device just enters the inversion regime, before the upturn. After four rounds of iteration, the substrate doping was found to be 3.3 x $10^{14}$ $cm^{-3}$. This is in good agreement with the 3-4x$10^{14}cm^{-3}$ which is generated from the nominal substrate resistivity of 17-33 ohm·cm.

The upturn anomaly on the HF curve in the inversion regime of the PB device is magnified in Fig 5.10(a). This is likely to be due to the well-known effect of peripheral inversion regions caused by oxide positive fixed charge in the LOCOS. Fig 5.10 (b) shows the cross-sectional diagram of the capacitance with increased active area due to this effect. This additional inversion region allows the AC signal to modulate minority carrier electrons around the edge of the active area. Therefore the effective active area for the capacitance is increased, resulting in an increase in $C_{inv}$ even with a high frequency signal. The effect is exacerbated by the low substrate doping of circa 3x$10^{14}cm^{-3}$. Further evidence of the additional inversion layer is proven in Fig 5.10 (c) by the frequency response of the high frequency C-V curves among which lower frequency signal allows more inversion capacitance to be added to the total capacitance. Due to the larger area of inversion capacitance, the C-V curve at 10 KHz testing frequency has a similar behaviour as the one at quasi-static state as shown in Fig 5.8.

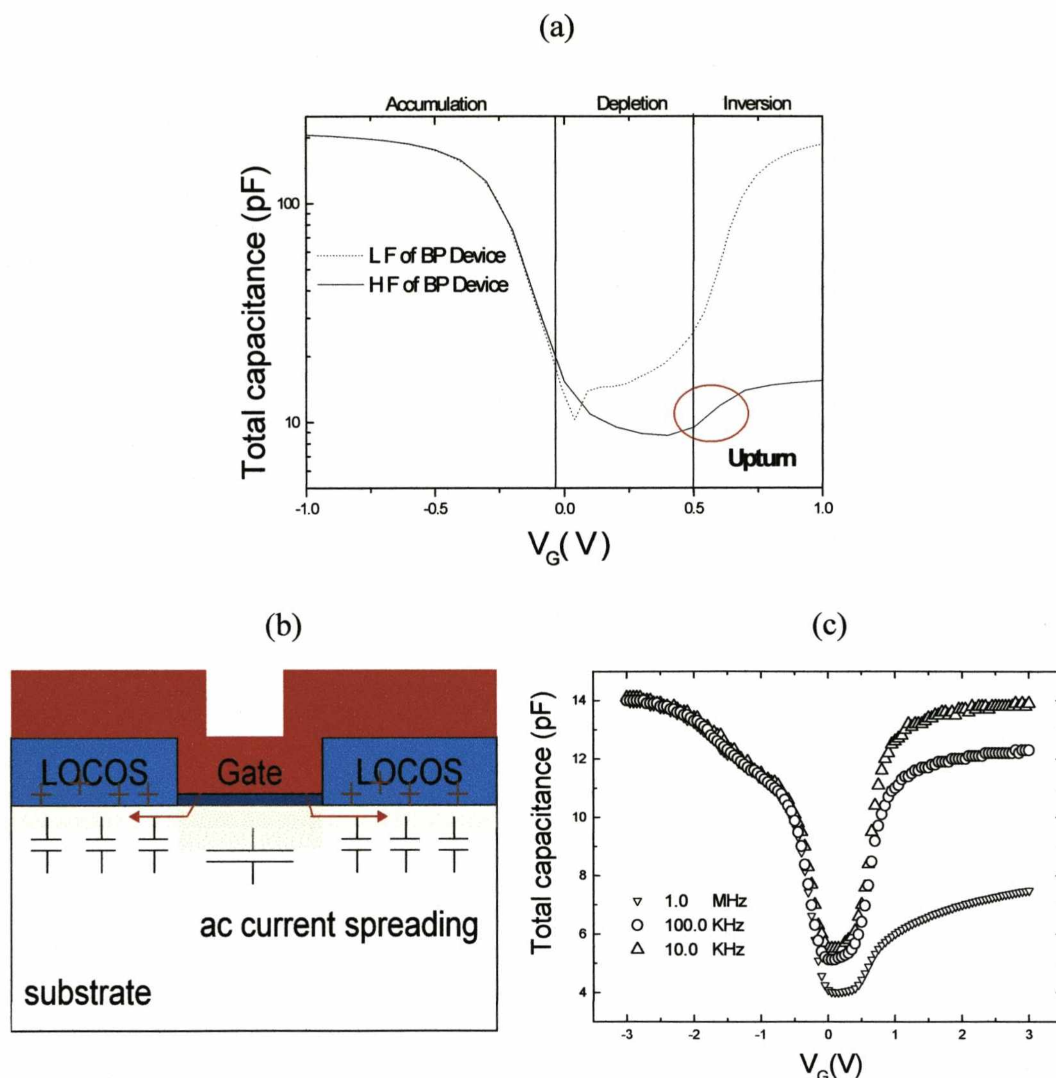



Fig 5.10 (a) Magnified LF & HF curves for the pillar bottom device; (b) Schematic diagram of the influence of oxide charge in the LOCOS; (c) Frequency dependent upturn.

A method based on the Fowler-Nordheim (FN) plot of Fig 5.11 was used to determine the work function of the TiN gate [85]. A pillar top (PT) capacitor with an area of $0.25 \times 10^{-4}$ $cm^{-2}$ was used. The PT capacitor is similar to the PB one but without perpendicular gate regions around the perimeter. The oxide thickness was measured as 8.3nm using ellipsometry [82]. The barrier height at the TiN-oxide interface is first determined from the associated FN plot, using negative gate bias which produces an injection of electrons from the gate. Taking the electron affinity in the oxide as 0.9eV, allows an estimation of the work function. The gate current shown in the inset of Fig 5.10, was measured by sweeping

the gate bias from 0V to -12.5V in steps of 0.2V. The FN current is only evident beyond 8.2V which corresponds to an electric field of about 10MV/cm.

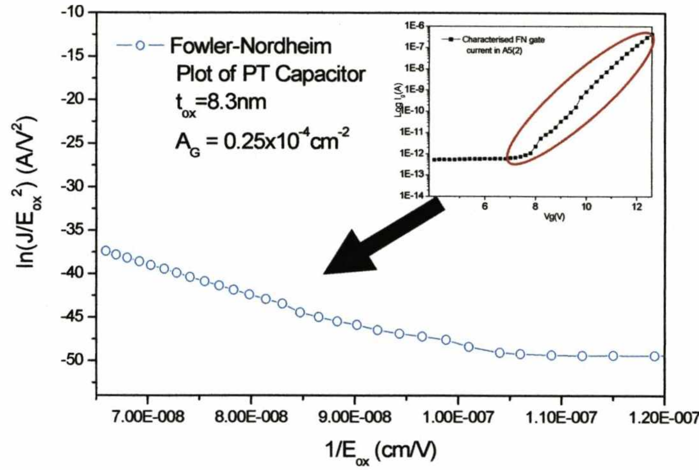



Fig 5.11 Gate current vs. gate bias of the PT capacitor with the Fowler-Nordheim plot included. $E_{ox}$ ($\xi_{ox}$) is the electrical field of gate oxide.

The potential barrier height was extracted as 2.4 eV from the FN plot of Fig 5.11 according to equation 2.30 and 2.31 using the intercept A on $\ln(J/\xi_{ox}{}^2)$ axis at $\frac{1}{E_{ox}} = 0\ \mathrm{cm/V}$ and slope B of the linear part. Values of parameter A and B are $e^{-13.6}$ $A/V^2$ and $-3.6\times10^8$ A/cmV respectively. It is worth noting that in the calculation of the barrier height, a value of electron effective mass is not required in the extraction of the barrier height as the $m_{ox}/m$ terms cancel each other out. The work function of TiN gate as a sum of oxide barrier height and oxide affinity is evaluated to be 2.4eV + 0.9eV = 3.3eV. This low value indicates that the barrier height has been underestimated. If further assuming that the positive fixed oxide charge has an amount of $5.2\times10^{11}cm^{-2}$ that resides in the oxide near the $Si/SiO_2$ interface, the effective voltage across the oxide is reduced by 0.2V according to

$$\Delta V_{ox} = \frac{qN_{ox}}{C_{ox}} \qquad \text{Eq 5.2}$$

Where $\Delta V_{ox}$ is the gate oxide voltage shift, $N_{ox}$ is the fixed oxide charge.

The corresponding oxide electric field becomes

$$\xi_{ox} = \frac{V_{ox}-\Delta V_{ox}}{t_{ox}} \qquad \text{Eq 5.3}$$

With this new gate oxide electric field, the two axes in Fig 5.11 are recalculated resulting in A = $e^{-15.0}$ A/V$^2$ and B=-3.35x10$^8$ A/cmV. Substituting the new A and B into equation 2.30 and 2.31, the oxide barrier height becomes 3.3eV. The total TiN work function is then evaluated to be 3.3 eV +0.9 eV = 4.2 eV.

# 5.2 VMOSFET-FILOX with a Retrograde Body

A retrograde profile is a standard solution to mitigate short channel effects without compromising on-current, as the lower surface doping level avoids carrier mobility degradation. A comparison of a conventional and retrograde 100nm/sub-100nm n channel MOSFET was made using a numerical simulation study [86, 87]. However, only a few experimental evaluations on implanted retrograde profile were successfully carried out in conventional MOSFET [88]. In this section, an attempt to realise retrograde profile in VMOSFET-FILOX devices through implantation is described.

## 5.2.1 Analytical Model

In Chapter 4, the numerical study on the relationship between the threshold $V_T$ voltage and the corresponded minimum depletion region width $W_{dm}$ at the threshold condition has clearly shown that the threshold voltage shift due to SCE increases with a wider $W_{dm}$. Therefore in deep sub-micron devices, the underlying physics to maintain threshold voltage with immunity to severe SCE deterioration is to maintain narrow $W_{dm}$. In practice, this was conventionally achieved by using an adaptive substrate doping $N_a$ of 1x10$^{18}$cm$^{-3}$

for MOSFETs with a channel length around 100nm. In Fig 5.12 the threshold voltage shift due to charge sharing and DIBL evaluated using equation 2.21, for an nMOSFET with 90nm channel length and gate oxide thickness of 3nm is plotted against $W_{dm}$. It is shown that to constrain the total SCE value within 200mV, the $W_{dm}$ needs to be within 49nm.

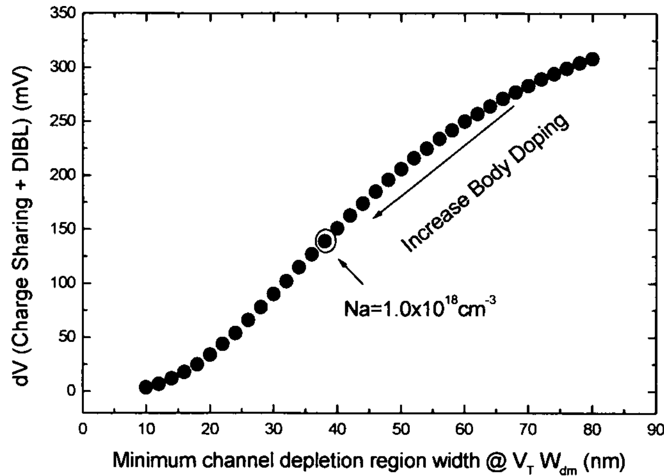



Fig 5.12 Total $V_T$ shift as a sum of CS and DIBL vs. $W_{dm}$

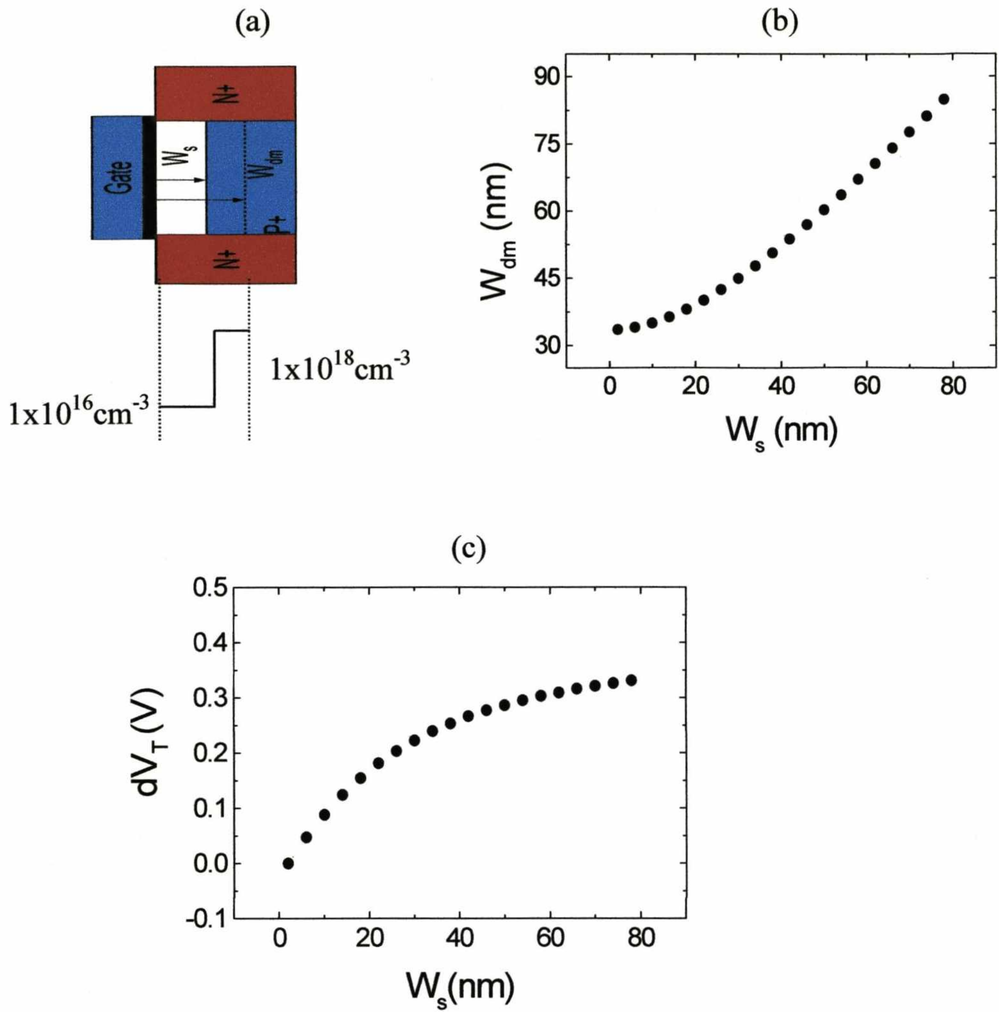



Fig 5.13(a) Schematic diagram of an ideal retrograde body; (b) $W_{dm}$ decreases with $W_s$; (c) $V_T$ shift due to SCE decreases with $W_s$

However in order to further improve the surface mobility and thus enhance on-current, a retrograde body profile is introduced whereby a relatively low doped region is achieved in the surface. A schematic of an idealized retrograde body with a vertical channel is demonstrated in Fig 5.13 (a) where $W_s$ is the width of the surface low doped $N_s$ region with a level of $1x10^{16}cm^{-3}$ while the rest of the body $N_a$ is $1x10^{18}cm^{-3}$. It is very important to note that $W_s$ should also be kept as narrow as possible in order to avoid an excessive impact on $W_{dm}$. From the Poisson equation 5.4 relating total charge in the depletion region to the depletion region width at the threshold condition, the surface potential can be expressed as a function of the $W_{dm}$ and $W_s$ which is shown in equation 5.5. Therefore the

$W_{dm}$ expansion due to $W_s$ can be inversely related to fully inversed surface as concluded by equation 5.6. The relationship of above two terms is quantitative illustration shown in Fig 5.13 (a). The maximum $W_s$ needs to be 36nm to maintain $W_{dm}$ within 49nm. The relationship between $W_s$ and $V_T$ is expressed in equation 5.7 where the last two potential terms together attribute to the total charge in the expanded depletion region at the threshold condition. The difference between the short channel (90nm) $V_T$ and long channel $V_{T0}$ is further plotted as a function of $W_s$ in Fig 5.13 (b). It is shown that for a $W_s$ of 36nm, the total threshold voltage $V_T$ shift is found to be about 245mV which is due to the SCE. This value is about 20% higher than the value of SCE predicted in Fig 5.12, but it gives some confidence that the maximum $W_{dm}$ needs to be 45 to 49 nm in order to achieve a SCE value around 200mV which is the limit of an adequate threshold voltage shift for 100nm MOSFETs. Therefore, ideally for a 100 nm channel length MOSFET, device performance enhancement can be achieved with a SCE of around 200mV by using an abrupt retrograde profile that varies from $1\times10^{16}cm^{-3}$ to $1\times10^{18}cm^{-3}$ within 50nm while retaining the lowly doped region within 36nm.

$$\xi_S = \frac{qN_aW_{dm}}{\varepsilon_{si}} - \frac{qW_sN_a}{\varepsilon_{si}} \qquad \text{Eq. 5.4}$$

Where it is assumed $N_s \ll N_a$,

$$\psi_s = \frac{qN_a}{2\varepsilon_{si}}(W_{dm}^2 - W_s^2) \qquad \text{Eq. 5.5}$$

$$W_{dm} = \sqrt{\frac{4\varepsilon_{si}\psi_B}{qN_a} + W_s^2} \qquad \text{Eq. 5.6}$$

Therefore

$$V_T = V_{fb} + 2\psi_B + \frac{qN_a}{C_{ox}}W_{dm} - \frac{qN_aW_s}{C_{ox}} \qquad \text{Eq. 5.7}$$

Becomes

$$V_T = V_{fb} + 2\psi_B + \frac{qN_a}{C_{ox}}\sqrt{\frac{4\varepsilon_{si}\psi_B}{qN_a} + W_s^2} - \frac{qN_aW_s}{C_{ox}} \qquad \text{Eq. 5.8}$$

### 5.2.2 Numerical Model

It is clear from the literature that an ideal step doping profile as shown in Fig 5.13(a) is difficult to achieve. Using Atomic-Layer Doping and Post Low-Energy Implanting Selective Epitaxy can create delta profiles that have a steepish retrograde doping [89, 90, 91]. In these cases, doping concentration at the $Si/SiO_2$ interface can be more than one order magnitude lower than the peak concentration in the body within a small distance. However, these processes are incompatible with the fabrication process for the VMOSFET devices studied here.

In this work, a retrograde body (RB) profile is implanted into the vertical pillar sidewalls through the exposed silicon surface after removal of the nitride spacer and stress relief oxide from the sidewall. The key steps of the process are outlined in Fig 5.14. The peak concentration underneath the sidewall surface provides the high acceptor (boron) doping level at the edge of the gate depletion width and low doping level in the sidewall surface region. However the retrograde profile after the thermal processes is further degraded. Therefore, in order to achieve the steepest retrograde profile possible, process simulation in Athena has been conducted for selecting the best combination of the initial p-well implantation, RB implantation energy, titled angle and boron dose level. Comparison of final retrograde doping profiles along the cut line one using various implantation conditions after the rapid thermal annealing is shown in Fig 5.15. A large tilt angle of 60 degrees can provide a steep retrograde profile near the surface, the maximum implantation tilt angle that can be used is 45 degrees due to limitation of the implanter. A boron dose level of $4x10^{13}cm^{-3}$ with implantation energy of 45 keV or a boron dose level of $5x10^{13}cm^{-3}$ with implantation energy of 55 keV, gives the steep boron doping roll-off at the surface so could be used for the retrograde body. Since both combinations give the same RB

profile, the first combination is chosen simply for a lower energy is used that it might reduce the implantation damage. The resulting body doping profile is illustrated in Fig 5.16 where the net doping level varies from 5.0 to 7.3 $x10^{17}cm^{-3}$ at the surface from pillar top to bottom to a level of 1.0 $x10^{18}cm^{-3}$ at the edge of the $W_{dm}$. The device simulation confirmed that this $W_{dm}$ is about 45nm when the channel is fully inverted. P-well implantation needs to have a dose level of $1x10^{13}$ $cm^{-2}$ with energy of 75keV as it produces a low doping level of $1x10^{17}cm^{-3}$ for the background boron concentration. This resulted in a p-type substrate that has a low doped background doping on the surface for the channel but is high enough to prevent the body punch through in the bulk. That means that the drain and source arsenic implantation has to use zero degree tilt in order to avoid countering doping the low doped channel region. At the same time, to maintain the channel length at around 100nm, an arsenic dose of $6x10^{15}cm^{-2}$ at 145 keV is used. The rapid thermal annealing condition is set to use the shortest time of 10s and a temperature of 1100°C for dopant activation and damage repair while maintaining the retrograde body gradient. The chosen key step conditions are summarized in table 5.2.

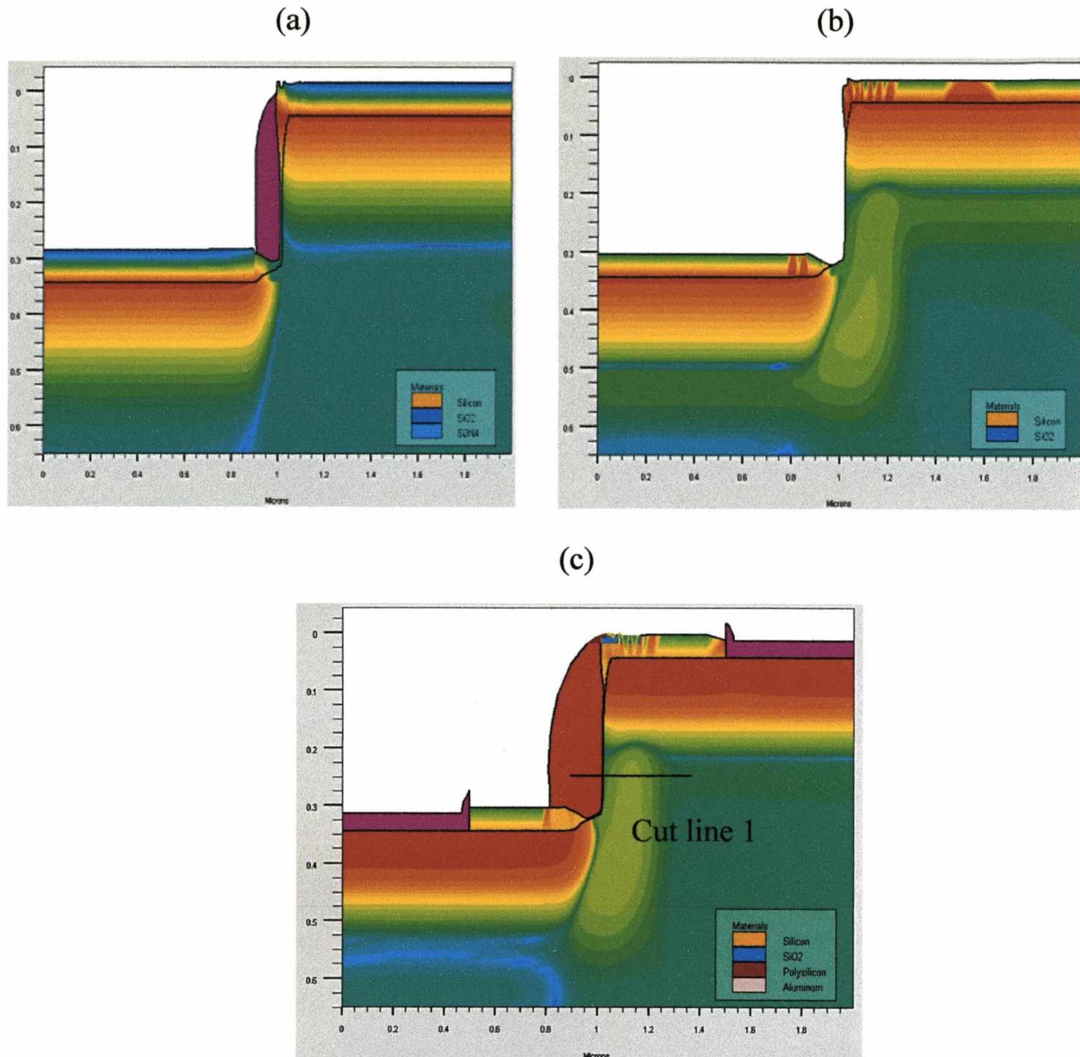



Fig 5.14 Key steps for retrograde body doping process (a) Drain/source implantation after FILOX growth; (b) Retrograde body implantation after nitride fillet and pad oxide growth; (c) Final net doping contour after RTA.

The electrical characteristics of above designed retrograde body device were simulated in Atlas where the models describing the relevant physics are as stated in section 3.3. The transfer characteristics with $V_{DS}$=50mV and $V_{DS}$=1.5V are illustrated in log scale in Fig 5.17 and in linear scale in Fig 5.18 with comparison to uniform body devices which have a net body doping level of $1\text{x}10^{18}\text{cm}^{-3}$ and $5\text{x}10^{17}\text{cm}^{-3}$ respectively. For the RB device the channel length is estimated to be 110nm and the oxide is 2.4 nm. The comparison of the physical and electrical parameters of the three devices is summarized in table 5.3. The net body doping profiles along the position of cutline 1 for the three devices are shown in Fig 5.19. Comparing the RB device to the low doped body device, the SCE is sufficiently suppressed in by the RB design. The threshold voltage is increased by 60% with DIBL improved by 40% whilst sacrificing only 10% on-current. Compared to the device with a

high doped body, the threshold voltage of the RB device is lowered by 28% with only about 15% DIBL deterioration.

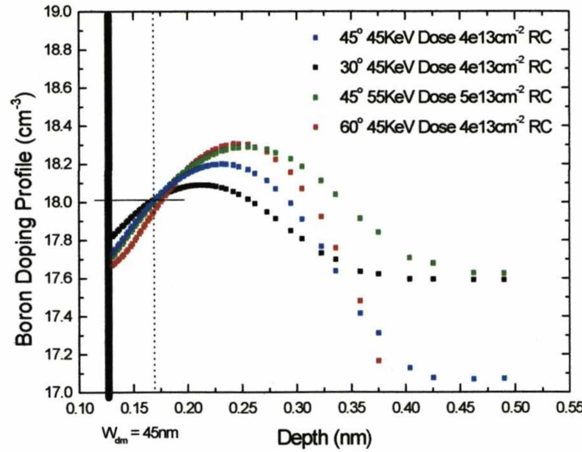



Fig 5.15 Boron doping profile comparison along the body depth (cut line 1) using different implantation conditions.

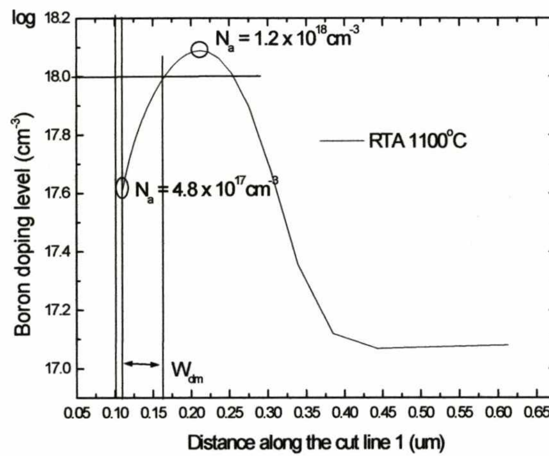



Fig 5.16 Net doping profile along cut line 1 after 45KeV and 45° RB implantation 10s 1100 °C RTA.

Table 5.2 Designed key step conditions summary of RB device fabrication

| | |
|---|---|
| P-well | 1e13 $cm^{-2}$, 75keV |
| Drive-in | 1100 degree |
| Arsenic Implantation | 1 time, 6e15$cm^{-2}$, 145 keV |
| Body Implantation | 4e13$cm^{-2}$, 45keV, 45° |

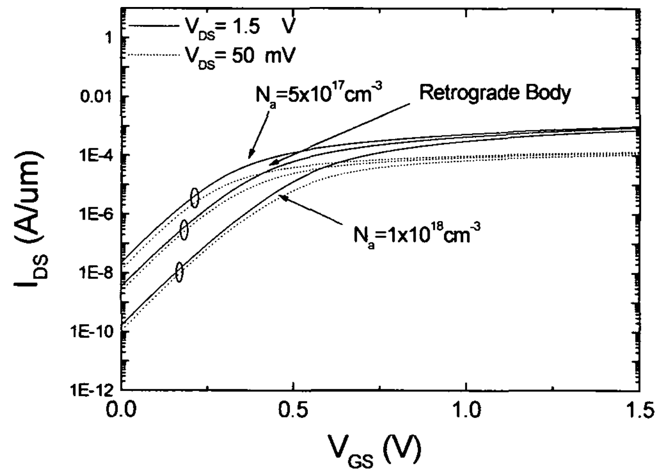



Fig 5.17 Transfer Characteristics under low and high drain biases of the devices with (a) uniform body with a doping level of $5x10^{17}cm^{-3}$; (b) retrograde body with a doping profile varies from of $4.8x10^{17}cm^{-3}$ to $1x10^{18}cm^{-3}$ with $W_{dm}$; (c) uniform body with a doping level of $1x10^{18}cm^{-3}$.

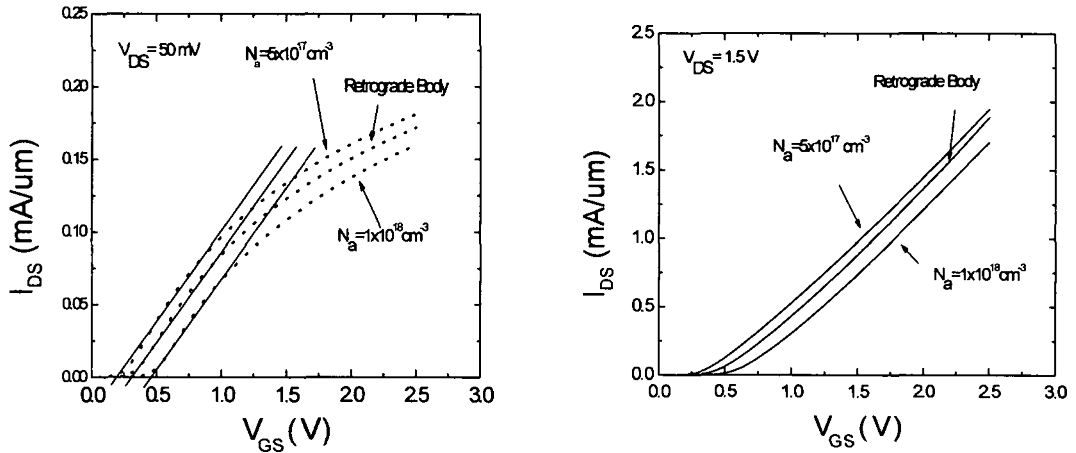



Fig 5.18 Linear plots of transfer characteristics under low and high drain biases of the three devices.

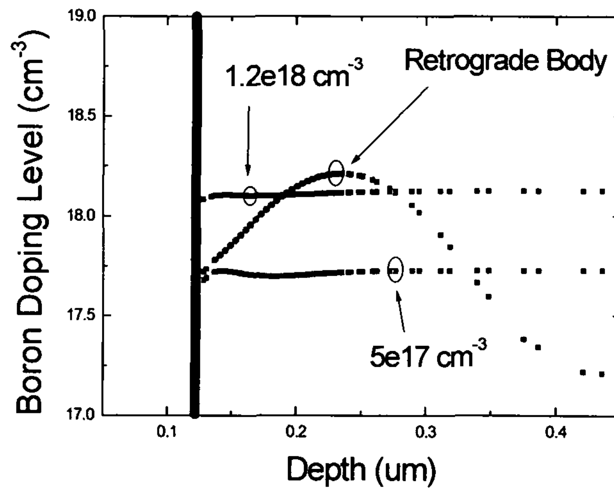



Fig 5.19 Comparison of body doping profiles along the body depth (cut line 1).

Table 5.3 Device parameter comparison of the three cases

| Devices | (a) Uniform | (b) Retrograde Body | (c) Uniform |
|---|---|---|---|
| $t_{ox}$ | 2.4nm | 2.4nm | 2.4nm |
| $N_a$ ($cm^{-3}$) | $4.8 \times 10^{17}$ | $5.0 \times 10^{17}$ ~ $1.2 \times 10^{18}$ | $1.2 \times 10^{18}$ |
| L (nm) | 100 | 110 | 120 |
| $V_T$ (V) | 0.2 | 0.32 | 0.45 |
| DIBL (mV) | 50 | 35 | 30 |
| Ss (mV/dec) ($V_{DS}$=0.05V) | 86 | 83 | 88 |
| $\mu$ s($cm^{-2}$/sV) $V_{DS}=V_{GS}$=1.5V | 26.5 | 19.2 | 14.5 |
| $I_{on}$ (uA/um) $V_{DS}=V_{GS}$=1.5V | 976 | 882 | 738 |
| $I_{off}$ (nA/um) $V_{DS}=V_{GS}$=1.5V | 21.9 | 3.4 | 0.17 |

The on-current, $I_{on}$ of the retrograde device is only 20% higher than that of the highly doped body device. This ratio is not as high as expected. From the 28% reduction in $V_T$, 32% increase in mobility, 8% reduction in channel length by RB profile a total 80% improvement of on-current should be apparent in accordance with an approximate estimation using equation 2.13; the latter assuming that both devices have the same body factor. The 60% unexpected extra degradation of the on-current is most likely due to the combined effect of lower body factor and degraded series resistance due to lower junction net doping level [92].

## 5.2.3 Device Characterisation

The fabrication of VMOSFET-FILOX devices with 100nm channel length and retrograde body doping profile were carried out at KTH, Sweden. These devices also have a structure of gate-all-around poly-Si gate with double gate contacts (DGC) and a P+ ring region that surrounds the device active area. A plan view is shown in Fig 5.20. The DGC

was designed to enhance the small signal circulation in the surrounding poly-Si gate, aiming to reduce the gate resistance compared to a single contact structure. The P+ ring was designed to enhance the boron doping in the area underneath the surface body contact surrounding the active area [93]. This design aims to reduce the substrate resistance. The threshold voltages measured using linear extrapolation methods from the transfer characteristics with $V_{DS}$=50mV are plotted in Fig 5.21. It is shown that all the devices have high threshold voltage averaged around 1.28V. The threshold voltage values of the devices with a P+ ring are generally not significantly lower than those without a P+ ring. This

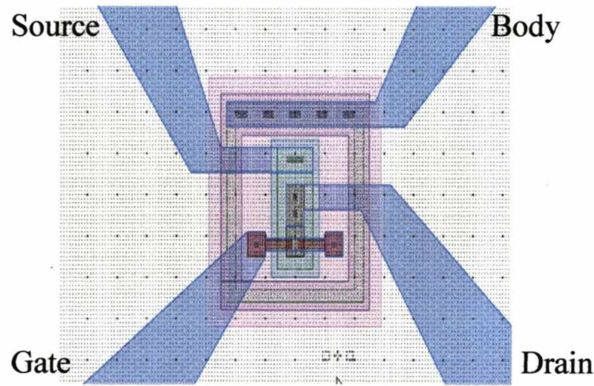



Fig 5.20 Layout structure of a GAA device double gate contacts and P+ ring area surrounding [93].

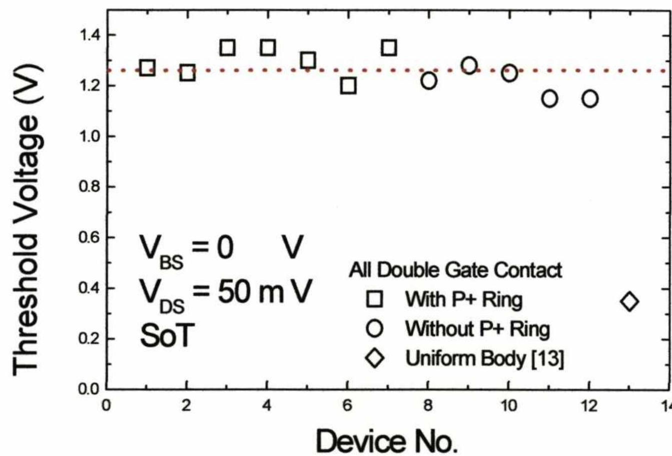



Fig 5.21 Threshold voltages measured from the RB, DGC and P ring devices under SoT mode, with comparison to a uniform body DGC, P ring device [93].

indicates that the body resistance is small enough so that the P+ ring has little effect on the body resistance.

It is also shown in Fig 5.20 that the threshold voltages of the 100 nm retrograde body devices are 3 - 4 times higher than that of a 100nm uniform body device reported in [94]. Since the substrate resistance has little effect on threshold voltage in this case and the gate oxide is unlikely to be thickened [95], the only possible reason for such a high threshold voltage is due to a high body level. The body doping level can be extracted by fitting the body factor calculated at each body bias with the two average body factors characterized in low and high body bias regimes. In Fig 5.22 (a), In the $V_T$ against $V_{gs}$ plot in Fig 5.21 (b), the body factors are then extracted to be 0.778V and 0.444V from the slopes of the linear fit of the $V_T$ vs. body bias curves in low and high body bias regions. The average doping level $N_a$ in the body can thus be evaluated by fitting the average calculated body factors using equation 5.9 to the characterized body factors in low respectively and high body bias regions.

$$\frac{dV_T}{dV_{bs}} = \frac{\sqrt{\varepsilon_{si} q N_a / 2(2\psi_B + V_{BS})}}{C_{ox}} \quad \text{Eq. 5.9}$$

$$\frac{\sqrt{\varepsilon_{si} q N_a 2\psi_B}}{C_{ox}} - \frac{\sqrt{\varepsilon_{si} q N_a / 2(2\psi_B + V_{BS})}}{C_{ox}} = \Delta V_T \quad \text{Eq. 5.10}$$

The $N_a$ value is found to be about $5.0 \times 10^{18} cm^{-3}$ in this sample. A similar result can also be obtained from equation 5.10 by substituting each body bias and corresponding threshold voltage shift and taking the average value of the calculated $N_a$. This body doping range is 5 times higher than the originally designed doping level which is $1.0 \times 10^{18} cm^{-3}$. As a result, it is illustrated in Fig 5.23 that the characterized on-currents are in the order of 10 - 100 times lower than that of the devices with uniform body doping. It can be concluded that the retrograde body design has not been realised and the body is in fact a high doped region. The reason might be related to a mistake in the processing whereby a zero degree

retrograde body implantation was used and this has resulted in a doubling of the boron doping level at the pillar top.

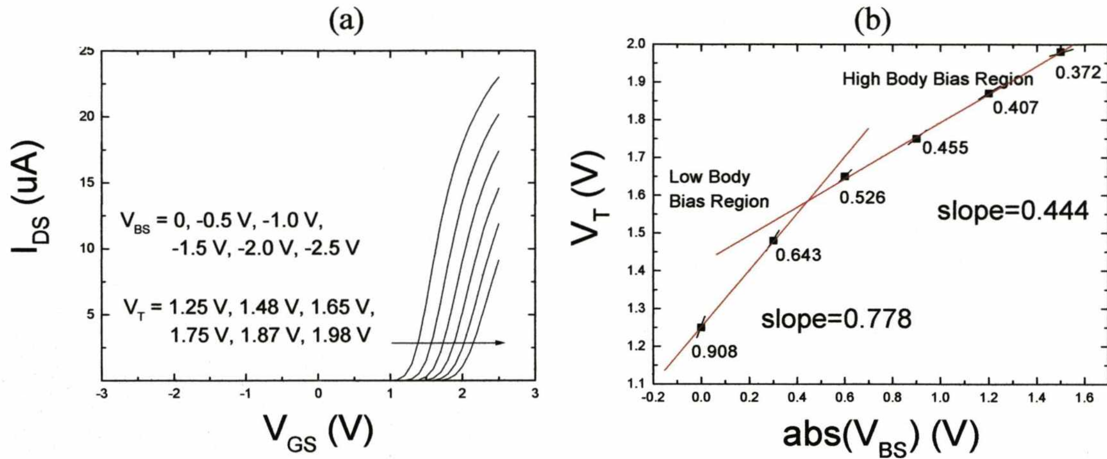



Fig 5.22 (a) $V_T$ extraction from the $I_DV_G$ curves under low drain bias at varied body biases using linear extrapolation method; (b) Calculated average body factors fitted to characterized body factors in low and high body bias region.

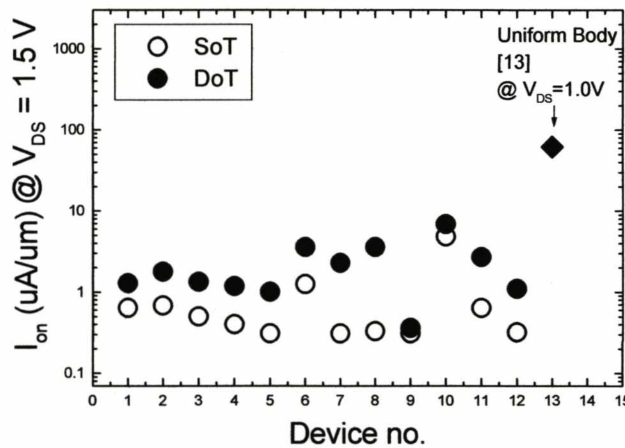



Fig 5.23 On-currents of double gate contact devices for SoT and DoT modes.

The other anomaly in Fig 5.23 is that on-current for DoT mode is always higher than SoT. This is due to a higher DIBL effect in DoT mode that results in a lower threshold voltage, therefore increasing the on-current. In Fig 5.24(a), if comparing the lateral shift between the transfer characteristics with $V_{DS}$=1.5V and $V_{DS}$=50mV for both DoT and SoT modes, the most striking feature is the asymmetry of the DIBL for SoT and DoT where the

DIBL value for DoT is about 190mV whilst no DIBL is observed for SoT. The asymmetrical DIBL values for SoT and DoT are also observed in most of the devices and illustrated in Fig 5.24(b). In the output characteristics shown in Fig 5.25 (a), it can be clearly seen that the breakdown voltage for DoT is 2.25 V while the breakdown voltage for SoT is 5V. At high drain bias the substrate current for DoT is clearly higher than SoT as shown in Fig 5.25(b). It is worthwhile to note that the maximum values for $I_{sub}$ are observed where $V_{GS} \approx V_{DS}/2$ is expected. It can thus be concluded that the saturation current enhancement for DoT is a result of combination effect of degraded DIBL and increased body current. While compared to the SoT even at high drain bias, the on-current curve remains saturated.

All the above drain field related phenomena suggest that the body doping in the channel region is not uniform in the drain to source direction. In fact, it suggests that the boron doping level at the pillar top end is higher than at the pillar bottom end. That is, the DIBL and the on-current are both suppressed in SoT due to a high barrier height at the source end caused by the high boron doping level at the pillar top. At the pillar bottom end, the lower boron doping level induces a small $E_{max}$. Consequently, the impact ionization and therefore the substrate current and the breakdown are suppressed in SoT mode. In contrast, the characteristics for DoT are due to a high $E_{max}$ at the drain end and low barrier height at the source end caused by this non-uniform body doping profile.

The DIBL asymmetry effect is investigated further by conducting a simplified device simulation. The simulation structure with an abrupt body doping profile is shown in Fig 5.26 (a) where the doping level is 60 times higher at the pillar top than that at the bottom with a channel length of 100nm and a gate oxide of 2.6nm. The net doping profile is illustrated in Fig 5.26 (b). The simulated threshold voltage shift due to $V_{DS}$=1.5V shows

that for the DoT mode the DIBL value is further increased by 110mV compared to the SoT mode.

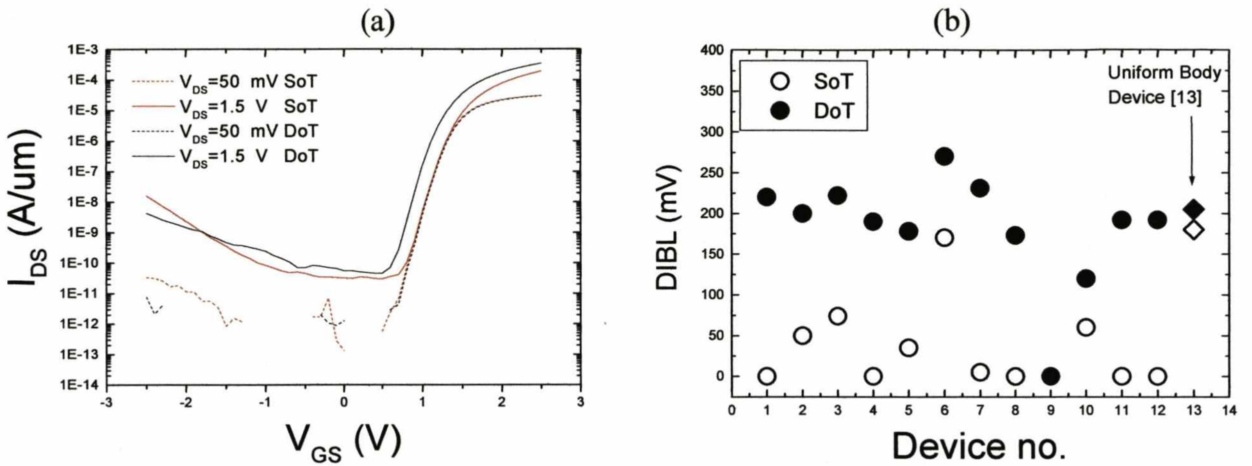



Fig 5.24 (a) Transfer characteristics under low and high drain biases in a sample device; (b) DIBL values for DoT and SoT in the rest of the devices.

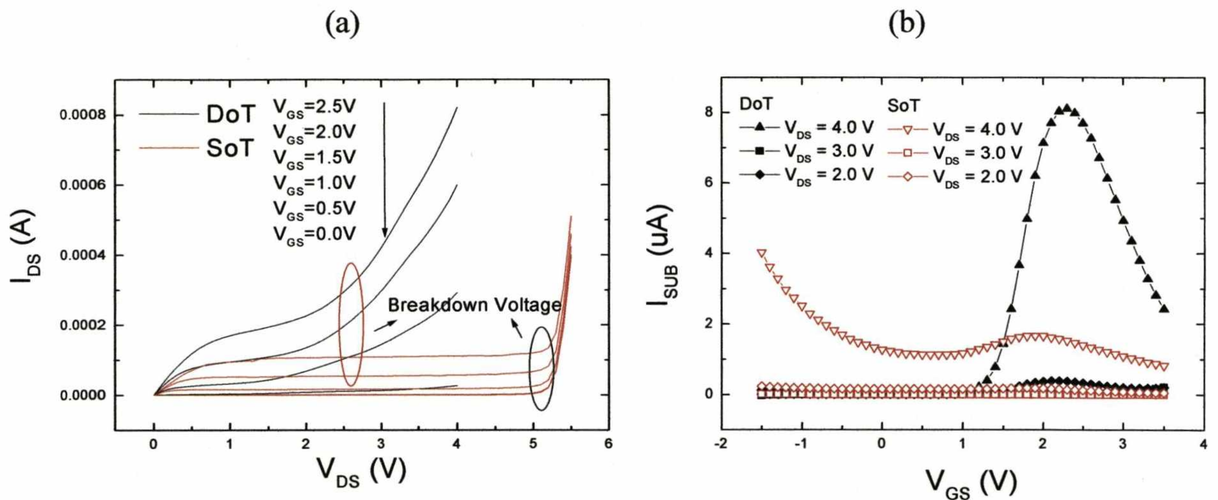



Fig 5.25 Measured (a) output characteristics; (b) Substrate current vs. gate bias under different drain biases for DoT and SoT.

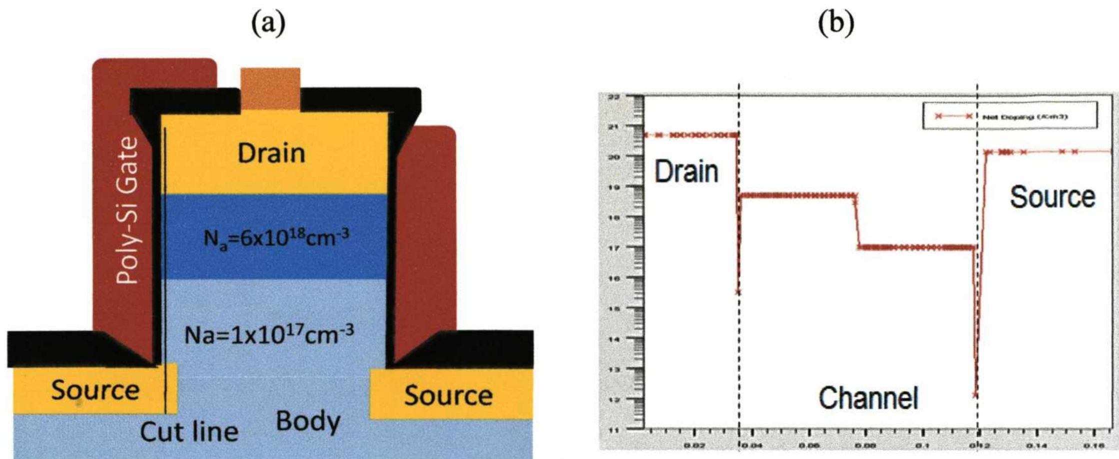



Fig 5.26 (a) Simulation structure of a presumed non-uniform body doping device; (b) the body doping profile along the cut line in the pillar varies from $6x10^{18}cm^{-3}$ to $1x10^{17}cm^{-3}$.

In Fig 5.28 (a) the gate current versus gate bias characteristics of oxides between gate and the body shows that devices exhibit good quality gate and FILOX oxides. The current can be fitted with the direct tunnelling model over the level of $1x10^{-11}$A at the negative gate bias region. At the positive gate bias region above 2.5V, the characterised gate current becomes lower than the predicted value. In the analytical model, the carrier effective mass in the oxide $m_{OX}$ and the free electron mass m ratio and the barrier height are set to be 0.35eV and 3.2eV respectively with a gate oxide thickness of 2.86nm. The reasonable agreement between measured and modelled curves in the negative gate bias region suggests that the leakage is dominated by the direct tunnelling (DT) mechanism in the gate oxide. The gate oxide is also robust against dielectric breakdown with an oxide electric field of 21MV/cm at $V_{GB}$=-5.5V. For the gate-to-source overlap region, the oxide thickness varies from the nominal thickness of 2.6nm to the nominal FILOX thickness of 40nm. The dominance of the DT mechanism is also observed in Fig 5.28 (b). Since the DT mechanism is associated with the thin oxide region, it can be concluded that the leakage in the entire overlap region oxide is dominated by the leakage in the thin oxide. Oxide robustness is also seen, as the gate bias can reach -5.5V without breakdown.

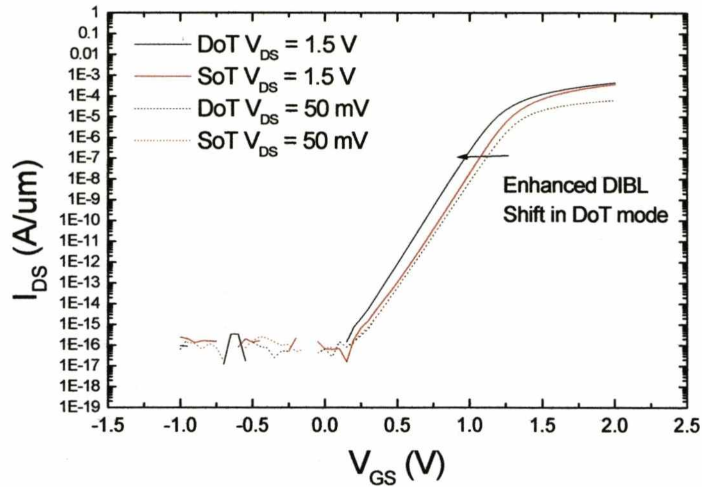



Fig 5.27 Simulated transfer characteristics under high and low drain biases suggest that DIBL is 110 mV higher in DoT than SoT.

(a) (b)

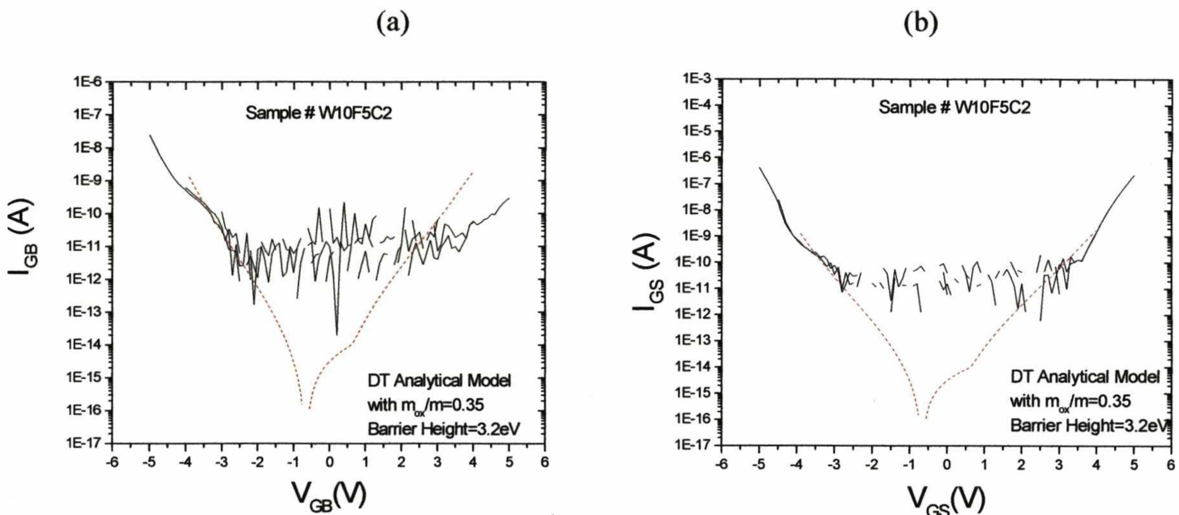



Fig 5.28 (a) Direct tunnelling current is observed in the gate to body oxide with $t_{ox}$=2.6nm (b) Direct tunnelling current is observed in the gate to source overlap region with $t_{FILOX}$ = 36 nm.

## 5. 3 Summary

In this chapter, C-V measurements on 20nm thick Ultra-thin Pillar capacitors with 8nm FILOX indicate the potential for integrating the FILOX process with ultra-thin pillars which could be used to realize fully-depleted vertical MOSFETs. However, capacitors with 16nm, 24nm and 37 nm thick FILOX show less well-behaved C-V plots. The leakage of the oxides

shows that with 37nm FILOX the gate oxide leakage coincides with that of the 8nm FILOX sample. Simulations indicate that the thicker FILOX induces more mechanical stress to the pillar bottom which in turn, may a dislocation-induced leakage path and so enhance oxide leakage. This stress effect is likely to be the cause of the poor yield of 20 nm ultra-thin pillar capacitors which show a decrease from 80% for 20 nm FILOX to 50% for 37 nm FILOX. The ultra-thin pillar capacitors with 37 nm FILOX and various pillar thicknesses show a consistency in C-V characteristics. This consistency provides evidence that the FILOX process has been successfully applied to ultra-thin pillar devices. The work function of the TiN gate is estimated to have a maximum value around 4.3eV if $2x10^{12}cm^{-2}$ positive fixed oxide charge is assumed at oxide Si/oxide interface.

A VMOSFET-FILOX with a retrograde body device was first designed with the aid of an analytical model. The calculations show that the maximum gate induced depletion edge in the body does not exceed 50nm and the low doped surface region does not exceed 36nm for 245mV.However, 2D numerical modelling has suggested that the best retrograde body profile that can be achieved within the constraints of the current fabrication process is from 5.0 to 7.3 $x10^{17}cm^{-3}$ at the surface to 1.2 $x10^{18}cm^{-3}$ at the edge of the $W_{dm}$. The simulated RB profile efficiently suppresses the SCE. However, the on-current is not increased as expected, presumably due to the combined effect of lower body factor and degraded series resistance due to lower net doping at the junction boundary.

All fabricated devices have high threshold voltages. The cause is related to a higher than expected body doping level which was found to be around $5.0x10^{18}cm^{-3}$. The anomalously high body doping has over-doped the intended retrograde body profile. The asymmetrical on-current in DoT and SoT modes has shown to result from asymmetrical DIBL. A simulation study confirms that the explanations for the electrical results is due to asymmetrical body doping level from top to bottom of the pillar. The peak concentration

close to the top junction needs to be 60 times higher than the doping level close to the bottom junction to give the experimental DIBL asymmetry of 110mV. The substrate currents and the breakdown voltage measured from DoT and SoT also show significant differences. The cause is presumably due to the same doping variation as that for the DIBL asymmetry. The leakage current in both gate oxide and gate-to-drain/source overlap region is dominated by direct tunnelling mechanism through the thin oxide layer. Both oxides show good robustness against dielectric breakdown.

# Chapter 6

# Series Resistances in VMOSFETs with FILOX

## 6.1 Introduction

As RF MOSFET scaling enters the deep sub-micron regime, the channel resistance in MOSFET scales with the effective channel length. The series resistance starts to play an important role in determining the current drive capability and thus the RF figures of merit $f_T$ and $f_{max}$ which are defined in section 2.4. Therefore more attention is required on the influence of the drain and source series resistances on the overall device performance. It is already known that $R_s$ and $R_d$ exhibit gate bias dependence in MOSFETs [96]. It is also known that the device electrical performance and reliability, including the key performance indicators saturated drain current $I_{on}$, transconductance, noise figure, cut-off frequency and degradation due to hot carriers, depend more on source resistance $R_s$ than the drain resistance $R_d$ [97]. Therefore, in this work it is of interest to investigate series resistances in each junction of the VMOST-FILOX structure. Due to the asymmetrical characteristics of top and bottom junction regions and the unique FILOX structure, it is important to obtain physical insight into the gate bias dependent series resistance by an analytical model in relation to key metrics for further performance optimisation. The series resistances are then extracted from a device generated from process simulation, using a small signal impedance method based on a practical RF measurement methodology. Results from the RF extraction and the analytical modelling are compared. Series resistances for devices with different FILOX thicknesses are studied based on the device simulations and therefore an optimal value is identified for optimizing $f_T$. Other key process parameters are identified in order to maintain low series resistances.

## 6.2 Analytical Model of the Bottom Junction Resistance

The current conduction paths from the source to drain in a simulated VMOSFET-FILOX under low and high drain bias but with high gate bias are illustrated in Fig 6.1. Along the paths, the series resistance components can be modelled using an equivalent circuit schematically shown within the device structure in Fig 6.2. In the channel region, the resistance component is dominated by the channel resistance in the inversion layer while in the top and bottom junction regions the series resistances are formed of three components: overlap region resistance $R_{ov}$, sheet resistance $R_{sh}$ and contact resistance $R_{co}$. However, due to asymmetry of the junction geometry, the overlap region resistance $R_{ov}$ in the two junctions needs to be analyzed and modelled separately. The circuit models of overlap regions in the top and bottom junctions are illustrated in Fig 6.3 (a) and (b) for the DoT mode where the drain is assigned to the top junction while the source is assigned to the bottom junction.

(a) (b)

Materials: Silicon, SiO2, Polysilicon, Aluminum

Fig 6.1 Current conduction path in VMOSFET-FILOX under a) $V_{DS}$=0.1V $V_{GS}$=1.5V; b) $V_{DS}$=1.5V $V_{GS}$=1.5V; L=100nm; FILOX=40nm.

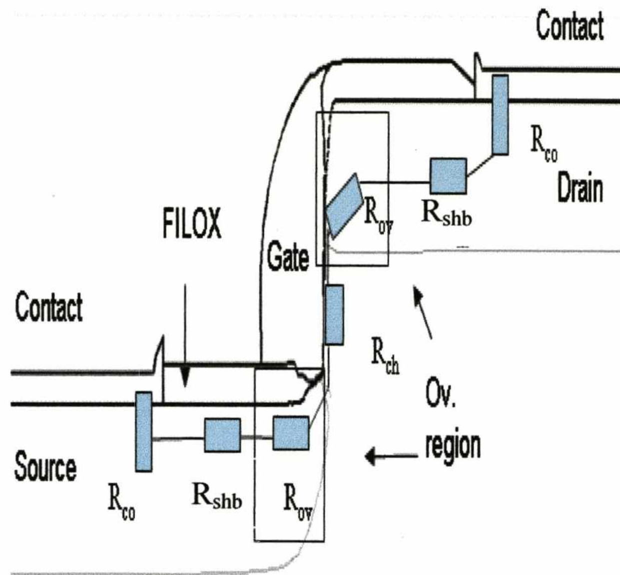



Fig 6.2 A VMOSFET-FILOX structure with an equivalent circuit of the series resistance.

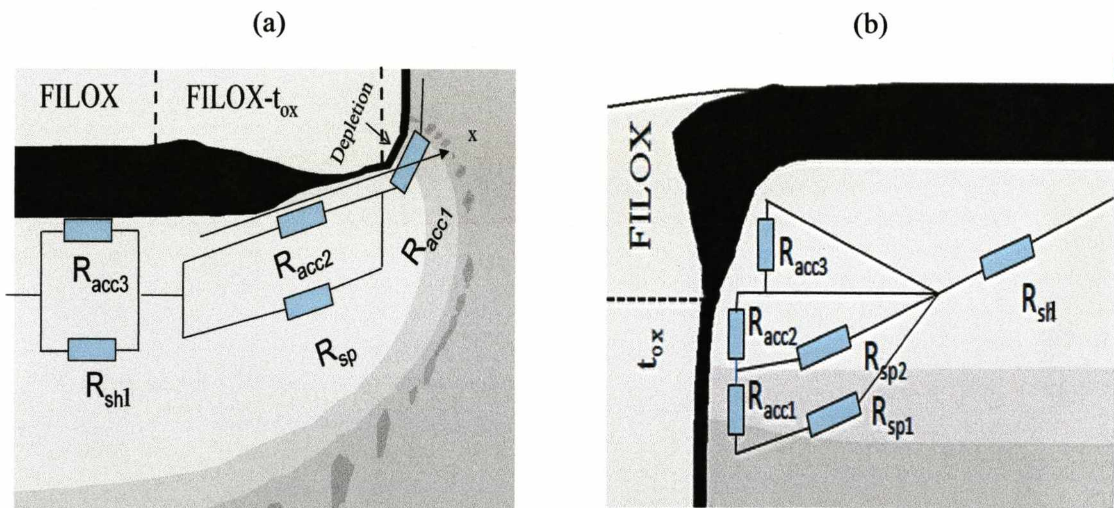



Fig 6.3 Resistance components in the overlap region of the (a) bottom and (b) top junction.

## 6.2.1 Analytical Model for Accumulation Resistance, $R_{acc}$

Once the conduction current has entered the bottom (source) region, it first flows close to the surface in the lateral depletion region of the metallurgical junction where the overlap oxide above remains equivalent to the gate oxide. The electrons which travel through this region are accumulated at the surface underneath the gate oxide. The resistance formed through this path, is referred to as the accumulation layer resistance $R_{acc1}$ as shown in Fig

6.3(a). As the current later flows out of the lateral depletion region at the junction boundary, the current sees two components of resistance. The first is a surface accumulation layer resistance underneath the FILOX-encroached oxide region and the second is the region where the current spreads into the junction bulk. The latter is referred to as the spreading resistance $R_{sp}$ in the deep junction bulk region. It has an increasing cross-sectional area and hence forms a relatively smaller resistance path for current to conduct [98]. These two parallel components known as $R_{acc2}$ and $R_{sp}$ in Fig 6.3 are further in series with the parallel combination of accumulation layer resistance $R_{acc3}$ and the sheet resistance $R_{shl}$ in the junction bulk underneath the thick FILOX. When the current flows out of the overlap region, it conducts through the rest of junction bulk sheet resistance $R_{shb}$ and at last reaches the metal contact window through the contact resistance $R_{co}$.

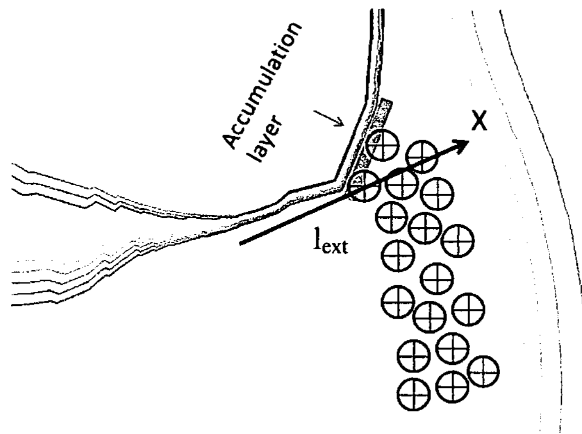



Fig 6.4 Accumulation layer in the junction depletion region. Note that the Gaussian curve is used to approximate the doping variation along x which is also along the accumulation layer length.

The derivation of $R_{accl}$ is started by using the surface potential to evaluate accumulation charge in the depletion region, $Q_{acc}$ as marked out in grey strip in Fig 6.4. The total charge is related to the surface potential through Gauss' law as described in equation 6.1. Note that under positive gate bias, the donor charge in the junction depletion region is not modulated by the surface potential which is set by the gate voltage but rather by the lateral

electrical field. Therefore in the following derivation only the accumulation layer charge in the junction surface is taken into account in $Q_{acc}$ which is set by the gate bias. In the evaluation of this charge, the gradual doping profile of the lateral Arsenic diffusion tail is modelled by a Gaussian diffusion expressed in equation 6.2.

$$Q_{acc}(\psi_s, x) = \sqrt{2 \cdot \varepsilon_{si} \cdot k \cdot T \cdot N_d(x)} \cdot \left[ e^{\frac{-q \cdot \psi_s}{k \cdot T}} + (\frac{q \cdot \psi_s}{k \cdot T}) - 1 \right]^{0.5} \qquad \text{Eq. 6.1}$$

where x is the position along the distance $l_{ext}$ which is between the $N_{dmax}$ point and the junction boundary and equals to 70nm in this case. It is parallel with the junction and uniform oxide thickness above as illustrated in Fig 6.4. $N_{dmax}$ is 1/3 of the maximum doping level in the bottom junction. The varying background doping level $N_d(x)$ is

$$N_d(x) = N_{d\,max} \cdot \exp(\frac{-x^2}{L_{diff}^2}) \qquad \text{Eq. 6.2}$$

where the $L_{diff}$ is the characteristic slope of the Gaussian curvature region and it can be calculated by substituting $N_a$, $N_{dmax}$ and the total distance $l_{ext}$ into equation 6.3 [99]. $L_{diff}$ is calculated to be 31.1nm

$$L_{diff} = \left[ \frac{-l_{ext}^2}{\ln(\frac{N_a}{N_{d\,max}})} \right]^{0.5} \qquad \text{Eq. 6.3}$$

Unlike in [98] where the junction surface potential was neglected in deriving the potential drop across the overlap gate oxide, the use of surface potential in equation 6.4 provides a more accurate model for the dependence of accumulation charge to gate bias where the poly-Si gate depletion effect is also taken into account by the third term [100]. Note that the gate oxide thickness above the depletion region equals to 4nm.

$$V_G(\psi_s) = V_{fb} + \psi_s + \frac{\overline{Q}_{acc}(\psi_s)^2}{2 \cdot q \cdot \varepsilon_{si} \cdot N_{gate}} + \frac{\overline{Q}_{acc}(\psi_s)}{C_{ox}} \qquad \text{Eq. 6.4}$$

Where $\overline{Q}_{acc}(\psi_s)$ is evaluated by equation 6.1 using the average doping level in the depletion region.

Therefore, $R_{accl}$ is calculated after integration of the local resistivity over the lateral depletion region width of the bottom junction. The equation 6.5 suggests that the higher carrier charge in the accumulation layer induces a higher conductivity.

$$R_{acc1}(\psi_s) = \int_{l_{ext}-W_{dep}}^{l_{ext}} \frac{dx}{W \cdot \mu_{eff} \cdot Q_{acc}(\psi_s, x)} \qquad \text{Eq. 6.5}$$

where $\mu_{eff}$ the effective mobility which is extracted from the numerical model within in along the accumulation layer within $W_{dep}$. From the numerical simulation, an average value of effective mobility in the lateral depletion region near the junction boundary is extracted to be 102 $cm^2/Vs$, neglecting the small gate bias dependence. This value is used in the rest of the derivation. $W_{dep}$ is the lateral depletion region width and can be obtained by fitting the maximum electric field at the junction boundary using equation 6.6 where $E_{max}$ is obtained through numerical simulation,

$$E_{max} = \int_{l_{ext}-W_{dep}}^{l_{ext}} \frac{q \cdot N_{d\,max} \cdot \exp(-\frac{x^2}{L_{diff}^2})}{\varepsilon_{si}} \cdot dx \qquad \text{Eq. 6.6}$$

From the above equation, the total $W_{dep}$ can be evaluated to be around 15nm. The final $R_{accl}$ values as a function of gate bias are plotted in Fig 6.5. Its dependency on $V_{GS}$ suggests that a higher $V_{GS}$ yields a lower $R_{accl}$.

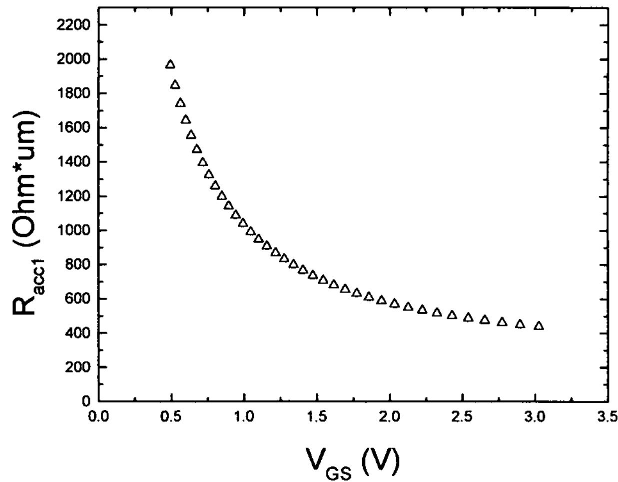



Fig 6.5 $R_{acc1}$ vs. $V_{GS}$.

## 6.2.2 Analytical Model for Spreading Resistance, $R_{sp}$

As the current travels further beyond the depletion region and spreads into the region underneath the FILOX-encroach-gate-oxide, it experiences a larger cross section of the junction bulk and hence tends to spread out with an angle that is determined by the junction geometry, depletion region width in the junction and accumulation layer thickness which approximately equals to the inversion layer. Here the inversion layer thickness is used instead of the accumulation layer thickness as these two values are approximately equivalent in this case and the first one is easier to be evaluated as a function of gate bias. The determination of the angle is described in equation 6.7 with a geometrical illustration in Fig 6.6 where the angle varies with the inversion layer thickness in the channel region, which is a function of the surface potential. The inversion layer thickness, $t_{inv}$, is evaluated as a summary of the classical thickness and the additional thickness due to quantum mechanical mechanism as expressed in equation 6.8 [101]. Note that $Q_{inv}(\psi_s)$ is evaluated using the same approach as for $Q_{acc}(\psi_s)$ with a constant body doping level.

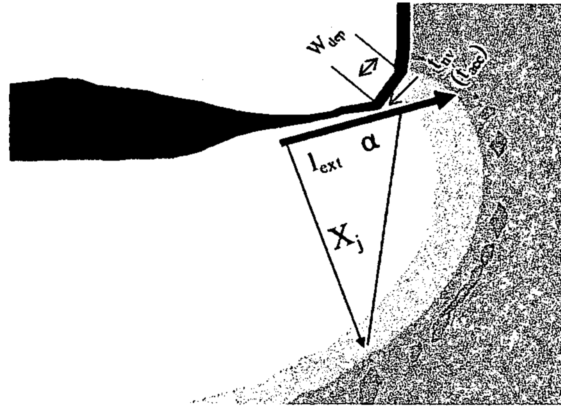



Fig 6.6 Spreading resistance geometry: α is the spreading angle and is determined by the geometry parameters.

$$\tan\alpha(\psi_s) = \frac{X_j - W_{dep} - t_{inv}(\psi_s)}{l_{ext} - W_{dep}} \qquad \text{Eq. 6.7}$$

Where $X_j$ is the junction depth; $t_{inv}$ is the inversion thickness as a function of $\psi_s$, the average surface potential in the channel region;

$$t_{inv}(\psi_s) = t_{classic}(\psi_s) + t_{quantumn}(\psi_s) = \frac{3\cdot k\cdot T}{q\cdot\frac{Q_{inv}(\psi_s)}{\varepsilon_{si}}} + \left[\frac{9\cdot h^2}{4\cdot m_e\cdot q\cdot\frac{Q_{inv}(\psi_s)}{\varepsilon_{si}}}\right]^{\frac{1}{3}} \qquad \text{Eq. 6.8}$$

where h is Planck's constant, $m_e$ is the free electron mass.

The spreading resistance can thus be obtained by integrating the local resistivity over the distance of the current spreading part that runs parallel with the surface, neglecting the doping variation along the vertical direction. The local resistivity is expressed in equation 6.9 as a function of the distance along x where the background doping profile has a Gaussian distribution. The integration of resistivity over the lateral spreading distance is described in equation 6.10 and the results are plotted in Fig 6.7.

$$\rho(x) = \frac{1}{w\cdot q\cdot\mu_b\cdot N_{dmax}\cdot\exp(\frac{-x^2}{L_{diff}^2})} \qquad \text{Eq. 6.9}$$

Where $\mu_b$ is the carrier mobility in the bulk of the junction.

The spreading resistance is evaluated in equation 6.10

$$R_{sp} = \int_0^{l_{ext}-W_{dep}} \frac{t_{inv}(\psi_s)\cdot\rho(x)}{(l_{ov}-W_{dep})\cdot\tan\alpha(\psi_s)+t_{inv}(\psi_s)}\cdot dx \qquad \text{Eq. 6.10}$$

The overall resistance in this region is the spreading resistance, $R_{sp}$, in parallel with the accumulation resistance, $R_{acc2}$. In the derivation of $R_{acc2}$, the average value of thickness of the encroached oxide is taken as the oxide thickness value. The accumulation layer resistance under the rest of the FILOX-encroach-gate-oxide region excluding the lateral depletion region is calculated using equation 6.1 – 6.5 using constant doping level. The gate bias dependence of $R_{acc2}$ is illustrated in Fig 6.8. It can be concluded that $R_{sp}$ is the dominant component in this region.

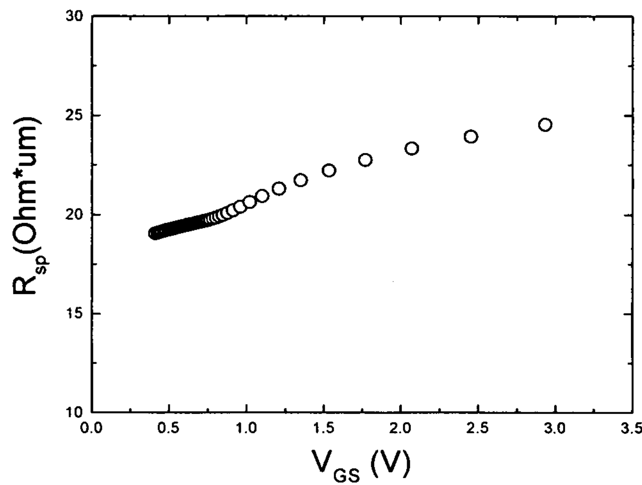



Fig 6.7 $R_{sp}$ vs. $V_{GS}$

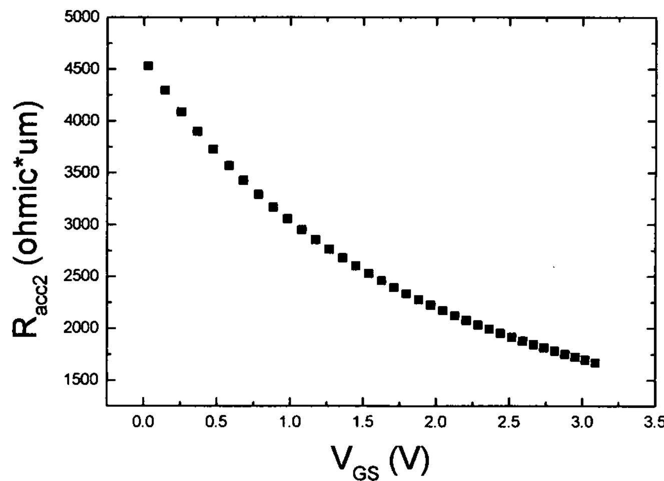



Fig 6.8 $R_{acc2}$ vs. $V_{GS}$

### 6.2.3 Analytical Model for $R_{sh1}$ in Parallel with $R_{acc3}$

The electrons then enter the junction bulk underneath the thick uniform FILOX region and conduct at a direction parallel with the surface. The overall resistance thus consists of two components, accumulation resistance $R_{acc3}$ and the sheet resistance $R_{sh1}$. Using equation 6.11 the sheet resistance of the junction bulk outside the gate overlap region is calculated to be 6.2 ohms·um.

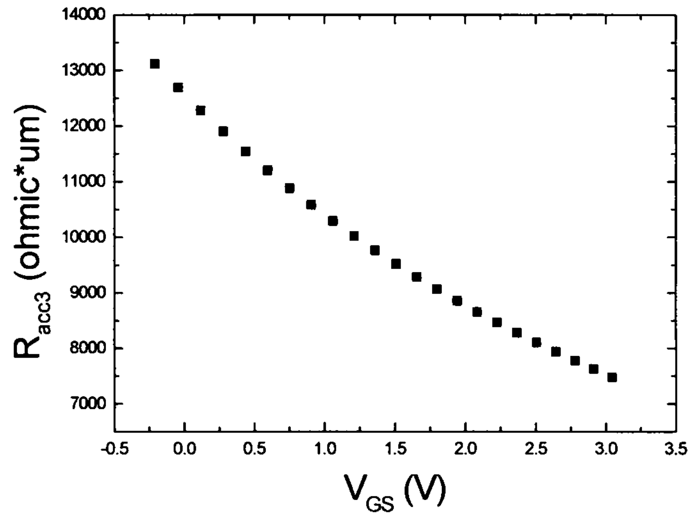



Fig 6.9 $R_{acc3}$ vs. $V_{GS}$

$$R_{sh1} = \int_0^{l_{sh}} \frac{dx}{W \cdot q \cdot \mu \cdot 3N_{dmax} \cdot X_j} \qquad \text{Eq 6.11}$$

Where $3N_{dmax}$ is the peak doping level in the bulk of bottom junction.

Comparing the $R_{acc3}$ value which follows the same method, the results are illustrated in Fig 6.9, where it can be seen that the total resistance in this region is dominated by the much smaller $R_{sh1}$.

The contact resistance model used in this study takes into account the current crowding effect analytically described in [102]. The study shows that the major of the current flows into the metal contact through the edge rather than the entire contact size. The flowing

electrons avoid further conducting through the surface underneath the rest of the metal square. This is due to (1) a remarkably higher sheet resistance in silicon than metal; (2) a transition resistance in the contact region is comparable or even smaller than the silicon sheet resistance. The total $R_{co}$ evaluated using its simplified model is 205Ω·μm.

## 6.2.4 Discussion on Series Resistance in Bottom Junction and Top Junction

The total resistance in the bottom junction is therefore:

$$R_{total} = R_{acc1} + \frac{R_{acc2} \cdot R_{sp}}{R_{acc2} + R_{sp}} + \frac{R_{acc3} \cdot R_{sh1}}{R_{acc3} + R_{sh1}} + R_{shb} + R_{co} \qquad \text{Eq. 6.12}$$

Where $R_{shb}$ is the sheet resistance in the bottom junction bulk calculated using the same equation 6.11.

The comparison of $R_{acc1}$, $R_{sp}$ and $R_{total}$ shown in Fig 6.10 indicates that the total value of series resistance is dominated by $R_{acc1}$ and consequently shows the same gate bias dependence trend with $R_{acc1}$. This means that the bottom junction resistance exhibits a smaller series resistance at high gate bias.

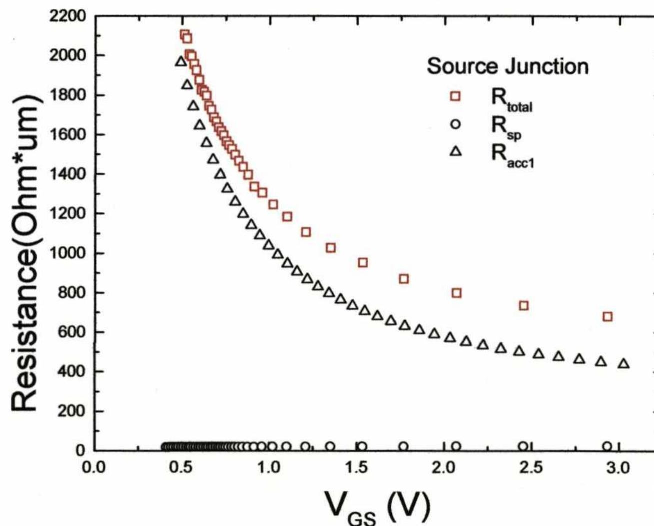



Fig 6.10 $R_{acc1}$, $R_{sp}$, $R_{total}$ vs. $V_{GS}$ of the bottom junction.

For the top junction, it is difficult to conduct a similar analysis in quantifying each series resistance component in the gate overlap region because the current tends to spread into the junction bulk region as soon it enters the junction depletion region. This is associated with the fact that the drain contact is on top and displaced from the junction surface. Because of this geometrical effect, it can be predicted that $R_{acc1}$ varies along the distance into the junction near the top junction boundary. Despite this, it can still be predicted that it is an important parameter similar to the situation in the bottom junction where $R_{acc1}$ is constant. It is also presumed that the distance between the drain contact edge and the vertical pillar surface influences the drain resistance, $R_d$ by affecting the current spreading position that in turn influences the $R_{acc1}$ and $R_{sp}$.

As a conclusion, in order to significantly reduce $R_{acc1}$, as represented by the analytical model, two key processes steps are identified related parameters namely the junction implantation dose that affects the doping level in the Gaussian doping profile region and FILOX thickness encroachment that affects $C_{ox}$. Significantly, these parameters are different at the top and bottom of the vertical pillar as are the respective influences of the gate bias dependence and the asymmetrical resistance values. FILOX tends to encroach more towards the junction boundary position at the pillar bottom for this case. In the next section, device simulations are used for a further investigation of the impact of processing on the series resistances in both junctions.

## 6.3 $R_d$ and $R_s$ Extraction using an RF-Impedance Technique

Many methods of extracting the combined series resistance (drain and source) from DC measurements have been reported and are summarized in [103]. In these methods, an array of devices with a wide range of channel lengths, L are required and significant errors can

be introduced for small values of L. Despite this shortcoming, the L-array methods have been widely used as a key technology indicator. In fact a few DC methods [104, 105] are able to extract $R_d$ and $R_s$ separately and also take account of the gate bias dependence by using a single transistor. These techniques are suitable for the case of vertical MOSTFETs with a small range of channel lengths. However, most of these methods require accurate determination of $L_{eff}$ and complex calculations. In order to avoid the aforementioned disadvantages, in this work the series resistances are extracted from impedances of a MOSFET two port system.

## 6.3.1 Technique Description

The device is biased in the strong inversion region with $V_{DS}$=0V and the transconductance and intrinsic gate track to substrate capacitance are neglected. Since the device is biased above threshold voltage, the channel resistance $R_{ch}$ screens the substrate effects at low frequencies. Therefore the device can be represented by the equivalent simplified circuit depicted in Fig 6.11 [106] which was derived from the original cold FET method in [107]. The series resistances are extracted by applying a small signal to the four terminals at a relatively low frequency range such that the impedances of junction-bulk capacitances can also be neglected.

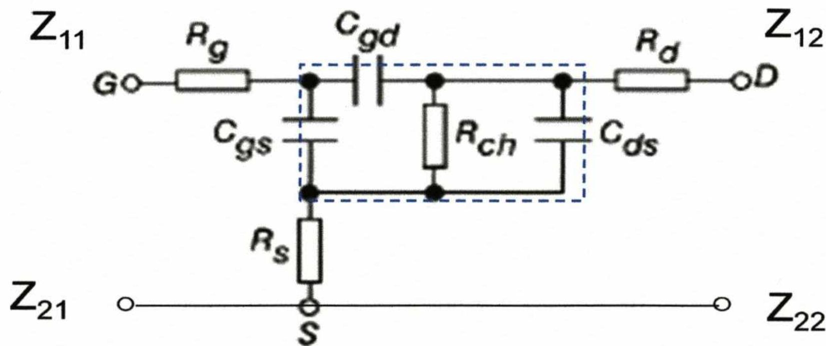



Fig 6.11 The simplified equivalent circuit of a MOSFET [106].

The impedance parameters Z matrix $Z_{11}$, $Z_{12}$, $Z_{21}$, $Z_{22}$ are extracted by applying a 50mV small test signal at the four terminals of the numerical device for various frequencies. Each Z parameter can be expressed in terms of external resistance components $R_g$, $R_s$, and $R_d$ and the Z parameters at the four terminals of the intrinsic part $Z_i$ of the MOSFET. The Z parameter matrix is illustrated by the equation set 6.12.

$$\begin{aligned} Z_{11} &= R_g + R_s + Z_{i11} \\ Z_{12} &= R_s + Z_{i12} \\ Z_{21} &= R_s + Z_{i21} \\ Z_{22} &= R_d + R_s + Z_{i22} \end{aligned} \qquad \text{Eq. set 6.12}$$

where $Z_i$ are derived from the $Y_i$ parameters matrix and its determinant shown through equation set 6.13.

$$\begin{aligned} Z_{i11} &= \frac{\frac{1}{R_{ch}} + j\omega C_{ds} + j\omega C_{gd}}{D} \\ Z_{i12} &= \frac{j\omega C_{gd}}{D} \\ Z_{i21} &= \frac{j\omega C_{gd}}{D} \\ Z_{i22} &= \frac{j\omega (C_{gs} + C_{gd})}{D} \end{aligned} \qquad \text{Eq. set 6.13}$$

where D is the determinant of the $Y_i$ parameters matrix at the four nodes of the intrinsic part. The angular frequency $\omega$ is equal to $2\pi f$ .

$R_s$ and $R_d$ then consist of the real parts of the $Z_{12}$ and $Z_{22}$ parameters; $\omega$ , $R_{ch}$, and $C_x$ are given by the expression shown in equation 6.14 and 6.15. Given that the first three parameters are already known, knowing the values of $C_x$ and $R_{ch}$ allows both $R_s$ and $R_d$ to be calculated. From a linear regression fit between the $-\omega/\text{lm}(Z_{22})$ and $\omega^2$ described in equation 6.16, $C_x$ and $R_{ch}$ can be extracted from the slope and the y axis intercept respectively.

$$R_d = Re(Z_{22}) - R_s - \frac{R_{ch}}{1+(C_x \omega R_{ch})^2}$$

$$R_d = Re(Z_{22}) - R_s - \frac{R_{ch}}{1+(C_x \omega R_{ch})^2} \qquad \text{Eq. set 6.14}$$

$$Im(Z_{22}) = -\frac{\omega C_x R_{ch}^2}{1+\omega^2 C_x^2 R_{ch}^2}$$

Where $C_x = C_{ds} + \frac{C_{gs}C_{gd}}{C_{gs}+C_{gd}}$ and $R_{ch}$ represents the resistance between the drain and the source in the channel.

A sample of the linear regression fit for a device generated from process simulation is shown in Fig 6.12. The device fabrication process included a 40nm FILOX, $0^o$ tilt source/drain arsenic implant and a 40s RTA at $1100^oC$. The small signal frequency was chosen as 100MHz to avoid distortion from the substrate network and junction impedance which are omitted in the equivalent circuit of Fig 6.11. In the extraction, DoT mode was used, that is, the drain is assigned to the top junction. As a result $R_d$ and $R_s$ which represent the series resistance in top and bottom junctions are 479 ohms·um and 541 ohms·um respectively at $V_{GS}$=2V. The extracted results of $R_s$ under four different $V_{GS}$ conditions are illustrated in Fig 6.13 where the values agree with the analytical model of the series resistance in the bottom junction through a functional fitting. The fitting confirms that the series resistance decreases with increasing gate bias. The code for the process simulation used to generate this device is listed in Appendix B. The extracted Z parameters at variant of frequencies under $V_{GS}$=1V, 2V, 3V are attached in Appendix C.

## 6.3.2 The Effect of FILOX Thickness on $R_d$ and $R_s$

To clarify the influence of FILOX thickness on the series resistance, $R_d$ and $R_s$ were extracted from simulation of devices with FILOX thicknesses that vary from 20nm to

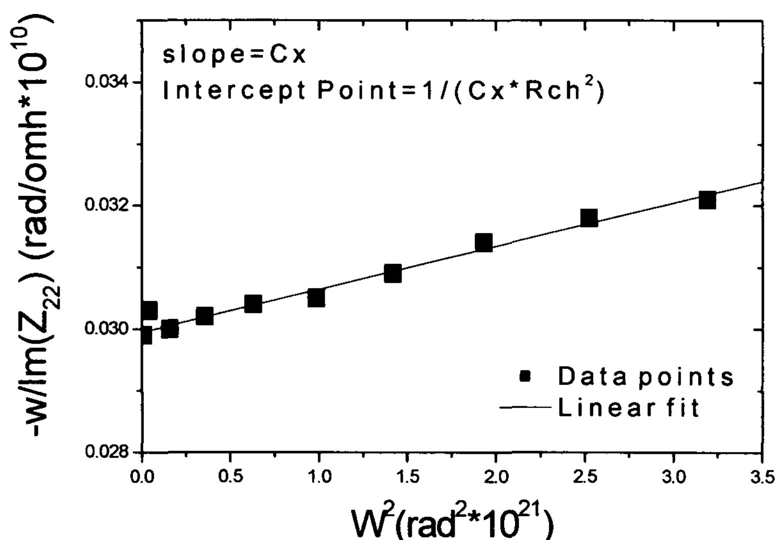



Fig 6.12 $-\omega/\mathrm{Im}(Z_{22})$ vs. $\omega^2$ of the sample at $V_{GS}$=2V with frequency from 100MHz to 9GHz.

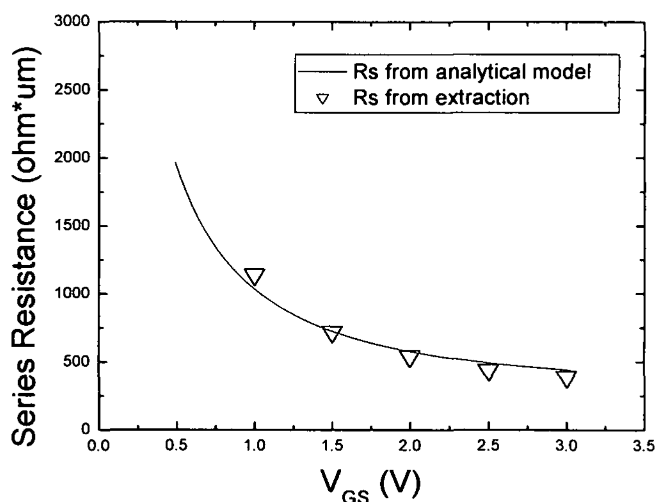



Fig 6.13 Extracted and analytical $R_s$ vs. $V_{GS}$ frequency FILOX=40nm, 0° S/D implant, 40s RTA, $V_{DS}$=0V.

60nm. The results are illustrated and compared in Fig 6.14 which shows that series resistances experience a dramatic increase when the bottom FILOX thickness increases from 50nm to 60nm. At a gate bias of 2V, the drain and source resistance increases from 581 Ω·μm and 479 Ω·μm for 40nm FILOX to 1510 Ω·μm and 4650 Ω·μm for 60nm FILOX respectively. Here the thickness relates to the uniform portion of the FILOX bulk. For 60nm FILOX, the analytical model indicates that the dramatic increase of $R_s$ is mainly

due to enhanced encroachment that has caused thickening of the oxide above $R_{accl}$ and reduction of the arsenic doping level by a screening effect of the FILOX on the implant. The thickness variation of FILOX encroachment ($t_{ox}$-FILOX) generated by the numerical simulation is demonstrated in Fig 6.15(a) where for the bottom junction, the average $t_{ox}$-FILOX above the $R_{accl}$ region is 4nm for 20nm FILOX, $t_{ox}$-FILOX is 7.2 nm for 60nm FILOX. It is difficult to explain the FILOX thickness effect on $R_d$ in detail without the assistance of an analytical model. For the top junction with thicker FILOX, nonetheless it is presumed that $R_d$ increases less than $R_s$ with gate bias because of the much reduced FILOX encroachment into the oxide above $R_{accl}$. The $R_d$ is still significantly higher in the 60nm FILOX device than the 50nm FILOX $R_s$ due to the combined effect of increased FILOX encroachment and the reduced doping level at the Gaussian doping profile region at the junction boundary. In Fig 6.15(b) the doping levels of these two cases at the junction boundary are compared where the device with FILOX 60nm has lower doping level.

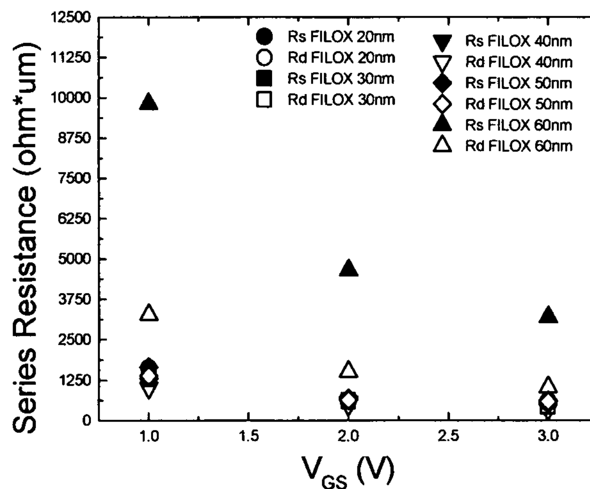



Fig 6.14 $R_d$, $R_s$ vs. $V_{GS}$, $0^o$ S/D implant, 40s RTA, $V_{DS}$=0V.

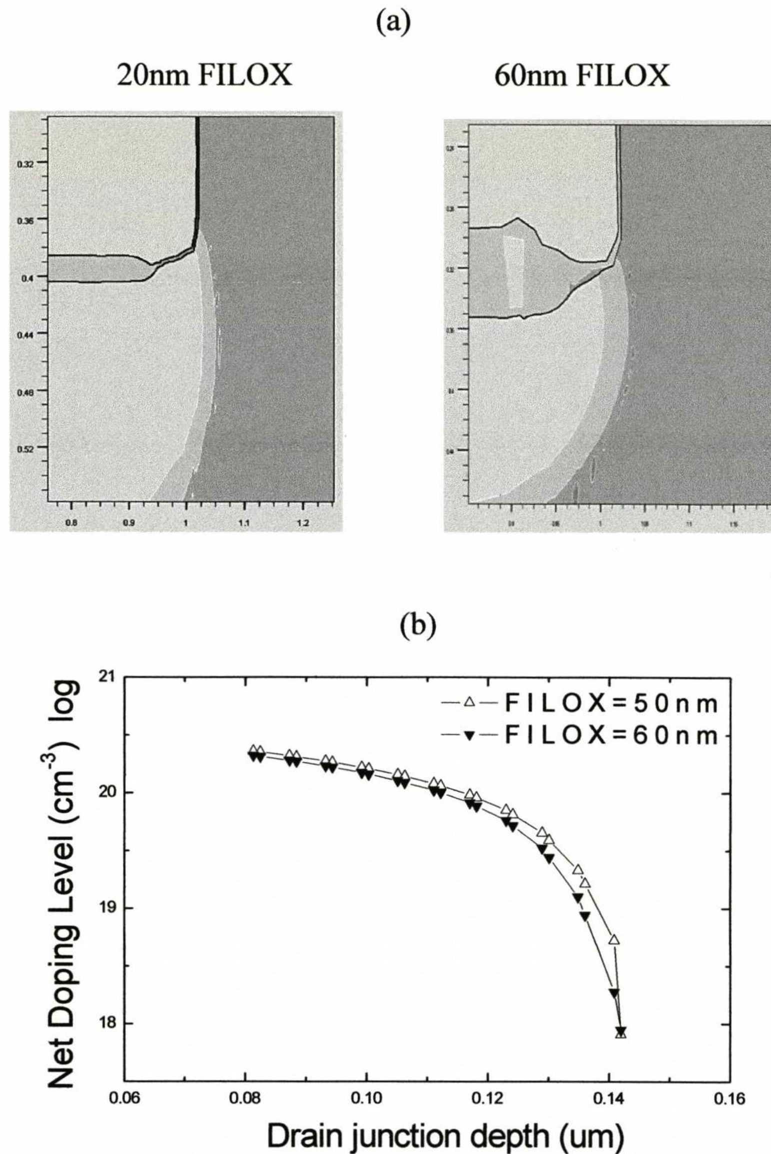



Fig 6.15 (a) FILOX Encroachment above the thinnest (20nm) and the thickest (60nm) bottom junctions (b) Doping profile at junction boundary under FILOX thicknesses of 50nm and 60nm for top junction.

The devices with thinner FILOX show much less variation in series resistances. The small differences also indicate that for these devices, less asymmetry between $R_s$ and $R_d$ is evident, due to significantly less FILOX encroachment into the sidewall near the bottom and top junction boundary, resulting in less variation of $R_{acc1}$. However, apart from FILOX thickness and encroachment difference, the other reason for the fact that the $R_d$ is always smaller than $R_s$ is presumably related to the geometry difference in the junctions. The contact position is at the center of the pillar top, the current is thus 'splited' earlier and

intends to spread into the junction bulk at a lower location compared the location in bottom junction. Therefore spreading resistance in the top junction has more effect in lowering the total series resistance in the top junction rather than the bottom junction. The simulation results have shown that reducing the distance between the top contact edge and the sidewall by 50nm in the top junction causes about a 10% increase in $R_d$.

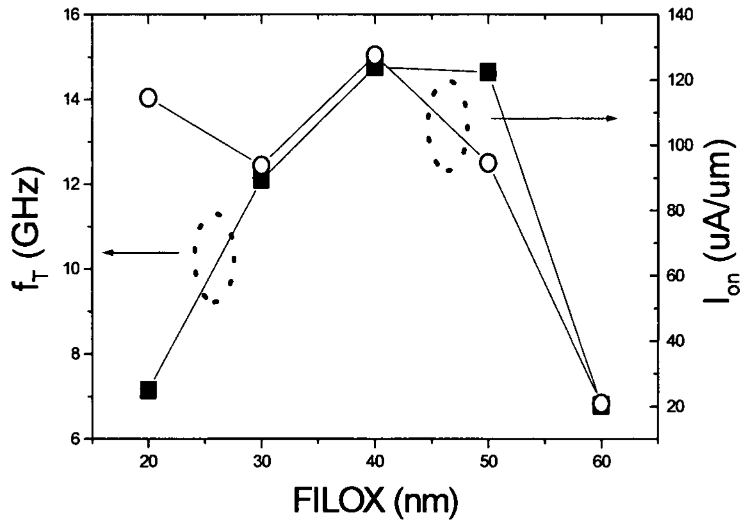



Fig 6.16 $I_{on}$, $f_T$ vs. FILOX thickness; $V_{DS}$=$V_{GS}$=1.0 V.

Table 6.1 $C_{ov}$ at $V_{GS}$=1.0V vs. FILOX thickness

| $t_{FILOX}$ (nm) | 20 | 30 | 40 | 50 | 60 |
|---|---|---|---|---|---|
| $C_{overlap}$ (fF/um$^2$) | 3.96 | 3.76 | 3.15 | 2.94 | 1.88 |

The $f_T$ and $I_{on}$ for the simulated devices at $V_{DS}$=$V_{GS}$=1.0V are shown in Fig 6.16. It can be seen that $f_T$ increases with the increasing FILOX thickness up to 40nm and starts to fall thereafter. The increase in $f_T$ is due to the effect of decreasing overlap capacitance; the extracted total overlap capacitance values are listed in table.1 where a reduction with FILOX thickness can be seen. The decrease of $f_T$ beyond 40nm of FILOX is a result of the dominance of series resistance which limits $I_{on}$ and hence the transconductance, $g_m$. Therefore an optimal FILOX thickness of 40nm is proposed for VMOSFETs for a maximized $f_T$.

## 6.3.3 The Effect of Drain/Source Implantation and RTA on $R_d$ and $R_s$

A comparison of series resistances for varying tilt angle of the source/drain implantation and RTA process conditions is made and shown in Fig 6.17. The RTA temperature is fixed at 1100°C for all the cases. The results for $V_{GS}$=2V are listed in table 2. It is observed that for 40nm FILOX, either 40 second RTA or 15 degree implantation is a necessary process step to maintain the series resistances at low level. This is because compare to 10 second RTA, it extend the junction around the bottom corner and further into the pillar to avoid compromise of series resistance by FILOX encroachment. This is further assisted by using higher implantation energy that additionally increases the overall junction doping level. However, this is not true when the energy becomes so high that the peak of the doping profile moves away from the surface of the bottom junction. Consequently $R_s$ deteriorates due to a reduced surface doping and less junction extension. In this case the short channel effect also becomes more severe due to a shortened channel length.

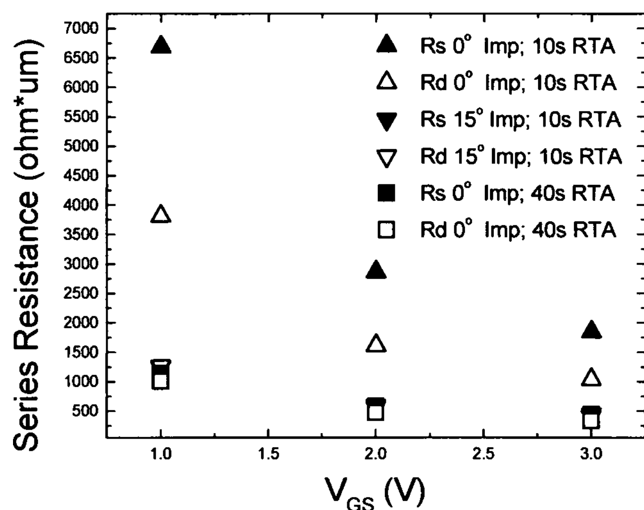



Fig 6.17 $R_d$, $R_s$ vs. $V_{GS}$ for cases of a) 0 degree s/d implant, RTA=10s; b) 15 degree s/d implant, RTA=10s; c) 0 degree s/d implant, RTA=40s; all with FILOX=40nm, $V_{DS}$=0V.

Table 6.2 $R_d$, $R_s$ vs tilt angle, RTA time with $V_{GS}$=2V

| Tilt Angle ($^o$) | RTA time (s) | $R_s$ ($\Omega\cdot\mu m$) | $R_d$($\Omega\cdot\mu m$) |
|---|---|---|---|
| 0 | 10 | 2860 | 1610 |
| 15 | 10 | 589 | 562 |
| 0 | 40 | 581 | 479 |

## 6.4 Summary

An analytical and simulation study of series resistance components in VMOSFET-FILOX was presented. The key parameters that influence the $R_d$ and $R_s$ gate bias dependence and asymmetric device aspects were identified. The analytical model allowed insight into the dominant resistance components whereby apart from lowered junction boundary doping level, the FILOX encroachment additionally increases $R_S$. To examine the dominant process steps that affect the series resistance, a 'virtual experiment' using an impedance-RF method was used to extract $R_d$ and $R_s$ from devices with different FILOX thicknesses using $0^o$ tilt source/drain arsenic implant and a 40s RTA at $1100^oC$. A conclusion can be drawn that once the thickness at the pillar bottom/top increases above 50nm the series resistance increases significantly. The reason for the increase is related to the FILOX encroachment and lowering of the doping at the junction boundary by a screening effect. At a gate bias of 2V, the drain and source resistance increases from 581 $\Omega\cdot\mu m$ and 479 $\Omega\cdot\mu m$ for 40nm FILOX to 1510 $\Omega\cdot\mu m$ and 4650 $\Omega\cdot\mu m$ for 60nm FILOX respectively. An optimal $f_T$ of 15GHz was seen for a FILOX thickness of 40nm at $V_{GS}$=$V_{DS}$=1.0V which represented a trade-off between the dominance of series resistance limited $I_{on}$ and the overlap capacitance. Finally the work also suggested that by using a 10s RTA time, the series resistance is increased significantly higher than the processes using a 40s RTA time or 15 degree angled tilt arsenic implantation for source/drain junctions. This is because the later ones sufficiently extend the junction boundary further away from the FILOX

encroachment around the corner region at the pillar bottom and thus the low series resistance is maintained.

# Chapter 7

# $f_T$ Characterisation

# 7.1 Calibration and De-Embedding

The characteristics of the cut-off frequency, $f_T$ presented in this chapter were initially derived from Y-parameter measurements on VMOSFET-FILOXs with uniformly doped body. An Agilent network analyzer (NWA) was employed, in conjunction with a Cascade RF probe station with a 175um pitch, that connected to the RF layout of the test structure as shown in Fig 7.1, to deliver DC and AC signals. Within each RF layout, there are ten devices with the same structure connected in parallel with each gate, drain and source/substrate pads tied to the rest respectively. Before the Y-parameter measurements took place, a system calibration process on NWA impedance was run with first ensuring the NWA port power was set correctly. A typical RF signal level for modelling transistor was set to be -40dBm which corresponds to a RMS voltage of 2.2mV.

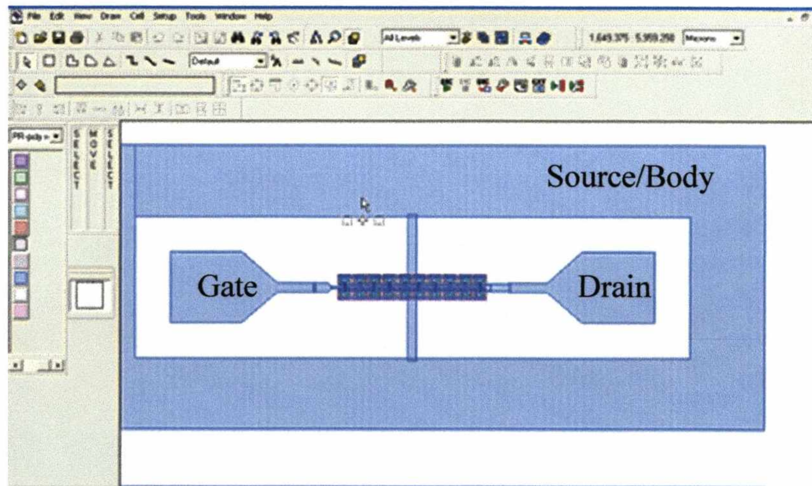



Fig 7.1 RF Layout with ten identical devices connected in parallel where source pad is tied to body using a ring type contact; drain and source pads are deposited separately within the ring.

The Integrated Circuit Characterisation and Analysis Program (IC-CAP) was used to control the NWA and also as a platform for analysing the Y-parameters. In this way, the initial power setting in the NWA was also preset through IC-CAP. These 'soft' settings

along with frequency settings were then sent to NWA to match its hardware settings. The output impedance of NWA was then calibrated by contacting the probes to one of the ISS substrate Calibration Standards; resistance value of 50 ohm in this case. After the calibration, Y-parameters were able to be accurately measured and subsequently transferred to h parameters to allow extraction of $f_T$ values and S parameters for de-embedding. The ICCAP set-up for $f_T$ characterisation and EKV extractions are listed in Appendix D.

In the process of de-embedding the pad parasitic of the RF layout, the frequency response of $S_{11}$ and $S_{22}$ showed that only an open on-wafer dummy structure was needed to extract the parasitic components, as shown in Fig 7.2,. The $S_{11}$ and $S_{22}$ parameters are plotted in the Smith chart of Fig 7.3 where the frequency is swept from 1GHz to 20GHz with the trace running from the right to left.

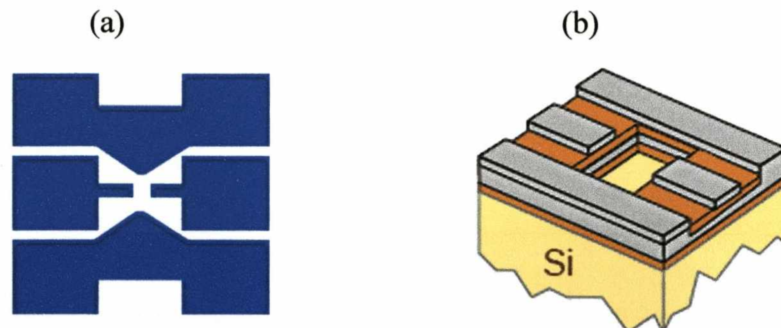



Fig 7.2 (a) 2D schematic diagram and (b) 3D diagram of an open dummy structure for pad parasitic de-embedding.

The traces confined on a close circle in the negative half do not turn into the positive half or other circles. When the frequency increases, the S-parameter follows a circle of equal resistance from the right half into the left and approaches the purely resistive line indicating the decrease of capacitance impedance only. This verifies that there is no effective inductive component in series with resistive components in parallel with the contact pads to the ground or connected between the gate/drain to body/gate contacts. The negligible magnitudes of S12 and S21 also suggest the absence of resistive and inductive

components between the gate, drain to source/substrate pads. Thus the equivalent circuit represents that the pad parasitic and the device under test (DUT) have only capacitive components as illustrated in Fig 7.4. Therefore the 'short' on-wafer dummy structure which has been designed to de-embed any inductive components is not needed.

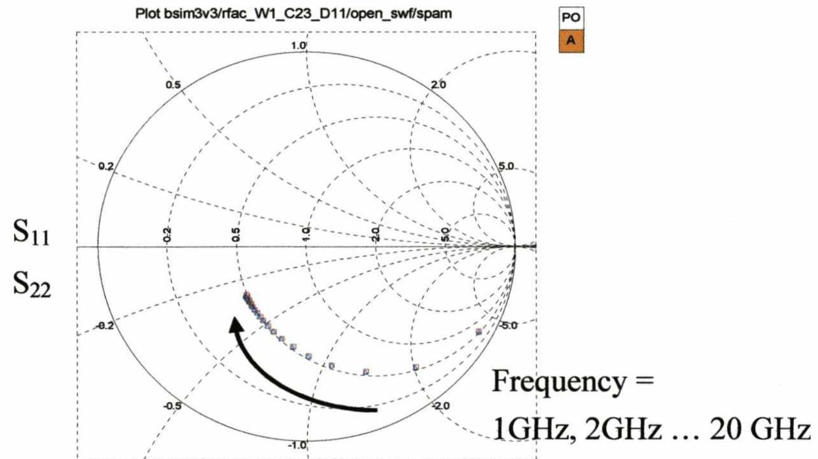



Fig 7.3 Smith chart: the frequency response of $S_{11}$ (blue) and $S_{22}$ (red) as frequency increases from 1GHz to 20 GHz.

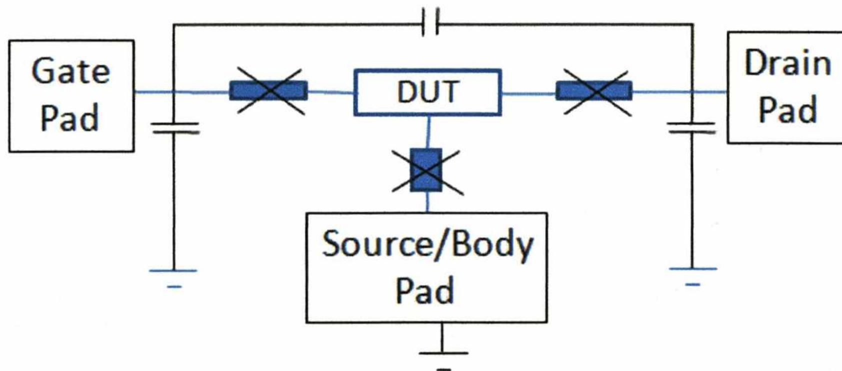



Fig 7.4 Pad parasitic circuitry without inductive components but with capacitive components only.

The real/imaginary graph in Fig 7.5 (a) and the Smith Chart in (b), show that the magnitudes of $Y_{12}$ ($S_{12}$) and $Y_{21}$ ($S_{21}$) parameters extracted from the open dummy structure are negligible compared to those of $Y_{11}$ ($S_{11}$) and $Y_{22}$ ($S_{22}$) parameters. Therefore the first two sets of parameters have very limited impact on the small signal parameters extracted from the device under test (DUT). The last two parameter sets are important as they reflect the impact from the parasitic. The Y-parameters extracted from a DUT are represented by

$Y_{total}$. The Y-parameters after de-embedding, are represented by $Y_{sub}$. Therefore $Y_{sub}$ parameters are equal to $Y_{total}$ parameters subtracted from the Y-parameters of the open dummy structure, $Y_{open}$. The transformation of the $Y_{total}$ to $Y_{sub}$ is thus concluded in equation 7.1. The values of $Y_{total}$ and $Y_{sub}$ represent small signal properties before and after de-embedding and are compared in Fig 7.6 where it is shown that only $Y_{11}$ and $Y_{22}$ are affected by pad parasitic.

$$Y_{sub} = Y_{total} - Y_{open} \qquad \text{Eq 7.1}$$

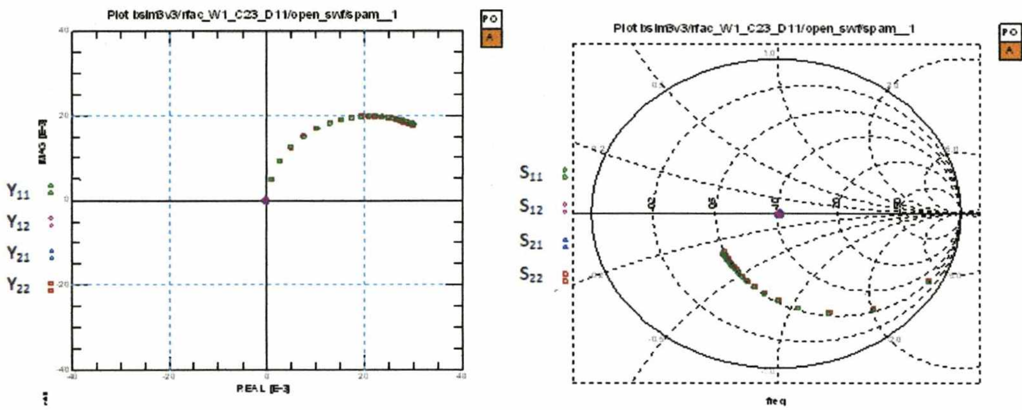



Fig 7.5 Comparison of (a) $Y_{11}$, $Y_{12}$, $Y_{21}$, $Y_{22}$ and (b) $S_{11}$, $S_{12}$, $S_{21}$, $S_{22}$.

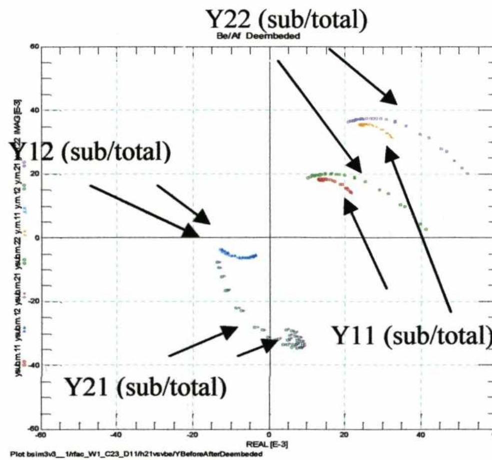



Fig 7.6 Comparison of Y-parameter before de-embedding ($Y_{total}$) and after de-embedding ($Y_{sub}$).

# 7.2 $f_T$ Characterisation of Second Batch VMOSFET-FILOX

## 7.2.1 $f_T$ Extraction Techniques

Two approaches have been tried for $f_T$ characterisation, technique on the same device which has a 100nm channel length, 30um channel width, 40nm FILOX and double gate contact. The first method is to extract $f_T$ from the intercept of the unity current gain, $h_{21}$ axis with the -20dB/dec roll-off line which is extended from the linear part of the log plot of $h_{21}$ vs. frequency curves. Fig 7.7 shows this technique was applied for four gate biases varying from 0.6V to 1.5 V with a 0.3V step and a constant drain bias of 1.5V. The maximum value of $f_T$ is extracted to be 7.8 GHz when $V_{GS}$ = 1.2V and $V_{DS}$ = 1.5V. Note that the source and substrate contacts are always grounded in the rest of this chapter.

The second $f_T$ extraction technique simply follows the cut-off frequency definition by which its value is equal to the product of the magnitude of $h_{21}$ for a particular frequency. In this way, $f_T$ values for various gate and drain biases can be extracted conveniently. The results are plotted in Fig 7.8 where $|h_{21}| \cdot freq$ is plotted against different gate biases with drain bias values of 0.9V, 1.2V and 1.5V. The $f_T$ at $V_{GS}$=1.2V and $V_{DS}$=1.5V is extracted to be approximately 7.8 GHz again in excellent agreement with the result extracted using the aforementioned -20dB/dec method.

In the following $f_T$ extraction results, a range of devices is employed. The second technique was preferred due to its simplicity and speed for taking many values. In the following sections, the influence of bias, gate type, channel length, channel width, and FILOX thickness will be explored.

VMOSFET-FILOX devices with two gate types: double gate contact (DGC) and frame gate contact (FG) structure with different channel length, width, FILOX thicknesses were

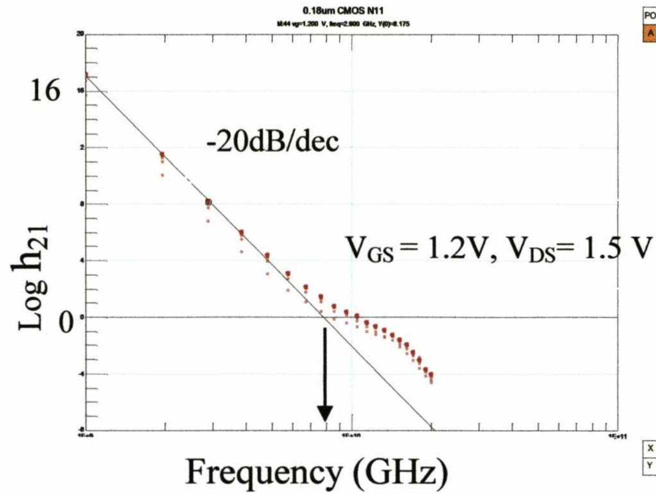



Fig 7.7 Technique A: $f_T$ extracted from the unit current gain axis with the -20dB/dec roll-off line from $h_{21}$ vs. frequency curves. $f_T \approx 7.8$ GHz when $V_{GS} = 1.2$V, $V_{DS} = 1.5$ V.

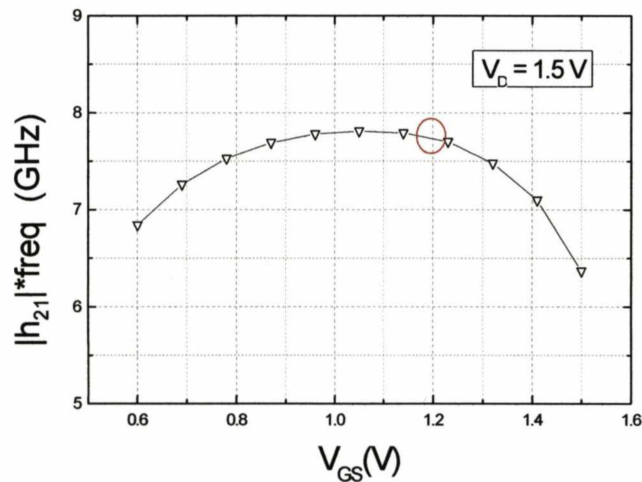



Fig 7.8 Technique B: $f_T = |h_{21}| \cdot freq$ where $f_T$=7.75 GHz when $V_{GS}$= 1.2V, $V_{DS}$ = 1.5 V.

tested. The basic structure of DGC devices has been introduced in section 5.2.3. Fig 7.9 presents the 2D schematic diagram of a VMOSFET-FILOX with a frame gate contact where the poly-Si gate spacer covers the pillar sidewalls. The entire poly-Si gate spacer and the area under the metal gate contact stripe are well protected from dry etched. This thin frame of polysilicon surrounds the pillar and is intended to decrease the gate series resistance and so aid the circulation of RF currents. Apart from the gate type, the device is the same as the DGC device. Note that the body is uniformly doped at a level of $1 \times 10^{18}$ cm$^{-3}$, for all the DUTs and both gate contact types.

### 7.2.2 The Effect of Contact Resistance on $f_T$

From the numerical model generated by a process simulation in accordance with [108], the $f_T$ values are extracted and shown in Fig 7.10 (a). It can be observed that for a VMOSFET with FILOX=40nm, the $f_T$ at $V_{GS}$=$V_{DS}$=1.5 V is 24GHz while for a VMOSFET with FILOX=60nm the $f_T$ is 29GHz. Note that 100 nm thick poly-Si gate

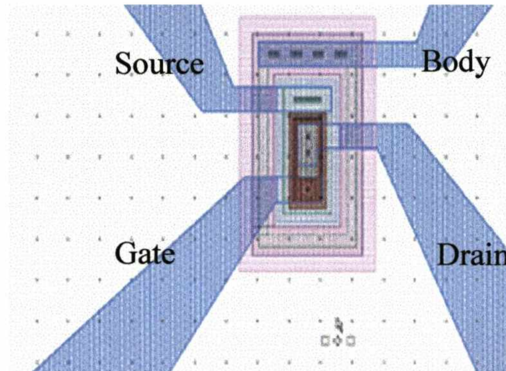



Fig 7.9 Contact layout of a VMOSFET-FILOX with a poly-gate covering the entire pillar sidewall of the pillar and the periphery area on the top marked by red where else is the same with the DGC device presented in Fig 5.19 [93, 109].

overtching has also been taken into account. The $f_T$ values were also measured from a fabricated DGC device with 100nm channel length, 30um channel width and 100nm FILOX thickness as a function of gate bias with $V_{DS}$=1.5V. The simulation and measured are shown and compared in Fig 7.10(a) where it can be observed that the measured maximum $f_T$ is significantly lower. In fact the maximum measured $f_T$ is about 14.2 GHz lower than the simulation result. By connecting two additional resistances with an individual value of 5.5kΩ·µm to the drain and source contacts of the numerical model, the simulated $f_T$ values can be lowered to a similar level to the measured ones as illustrated in the plot. Thus this study suggests that the fabricated device has low $f_T$ values because of the existence of the high additional resistance values which are most likely attributed to the contact interfaces. The contact resistances at the drain and source sides are both higher than the values predicted in the numerical model where ohmic interfaces were assumed.

The rectification of these extra contact resistances on the on-current is shown in Fig 7.10(b) where a good fit is seen on the on-currents of the simulation and measurement after adding the resistances. By using equations 7.2 and 7.3, the resistance in the intrinsic part of device under test can be calculated to be 2240 Ω·μm which is about five times smaller than the total value of the additional contact resistances. The total resistance value existed along the current conduction path between the drain and the source in the fabricated device is 13.24 kΩ·μm

$$I_{onM} \cdot (R_{DUT} + 2R_{add}) = V_{DS} \quad \text{Eq. 7.2}$$

$$I_{onS} \cdot R_{DUT} = V_{DS} \quad \text{Eq. 7.3}$$

Where $I_{onM}$ is the measured on-current and $I_{onS}$ is the simulated on-current at $V_{GS}=V_{DS}=1.5V$; $R_{add}=5.5$ KΩ·μm.

### 7.2.3 The Effect of Biases on $f_T$

The $f_T$ characteristic of a DGC VMOSFET with 100nm channel length, 30um channel width, 40nm FILOX thickness was extracted with $V_{DS}$=0.9V, 1.2V and 1.5V respectively with gate bias varied from 0.6V to 1.5V. The results are illustrated in Fig 7.11 where most of the extraction was carried out with the device operating in the saturation operation region.

For each value of drain bias, $f_T$ first increases with gate bias until it reaches its maximum value at a gate bias where it starts to fall. During the gate sweep, $f_T$ initially increases with the increasing saturation current level driven by higher gate voltage. Then it falls with gate bias due to the combined effect of the increasing overlap gate-to- drain/source capacitance and the decreasing $g_m$. Comparing both effects, the decreasing

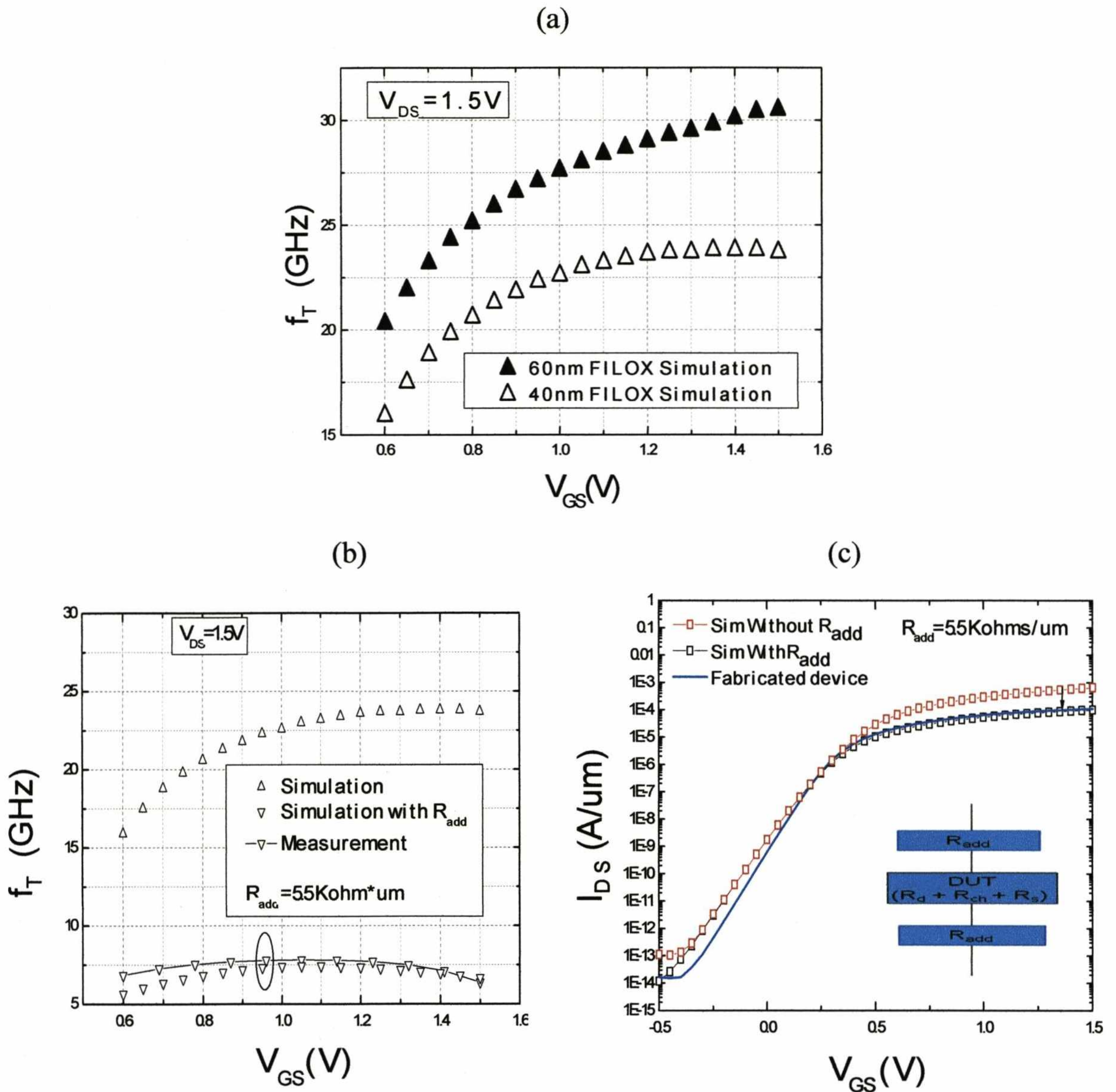



Fig 7.10 (a) $f_T$ vs. $V_{GS}$ extracted from numerically simulated VMOSFET with 40nm and 60nm thick FILOX; (b) $f_T$ comparison of the fabricated device and the numerical model with/without $R_{add}$ (c) $I_DV_G$ comparison of the above two cases.

gate-to-drain/source capacitance takes the dominant role; the decreasing $g_m$ is related to the reduction of mobility for increasing gate bias. The comparison of $g_m$, overlap capacitance and the resulting $f_T$ as a function of gate bias are numerically simulated with the calibrated on-current and results are illustrated in Fig 7.12(a) and (b). It is shown that the peak point of $f_T$ corresponds to the point where the total gate bias dependent overlap capacitance is near its minimum value.

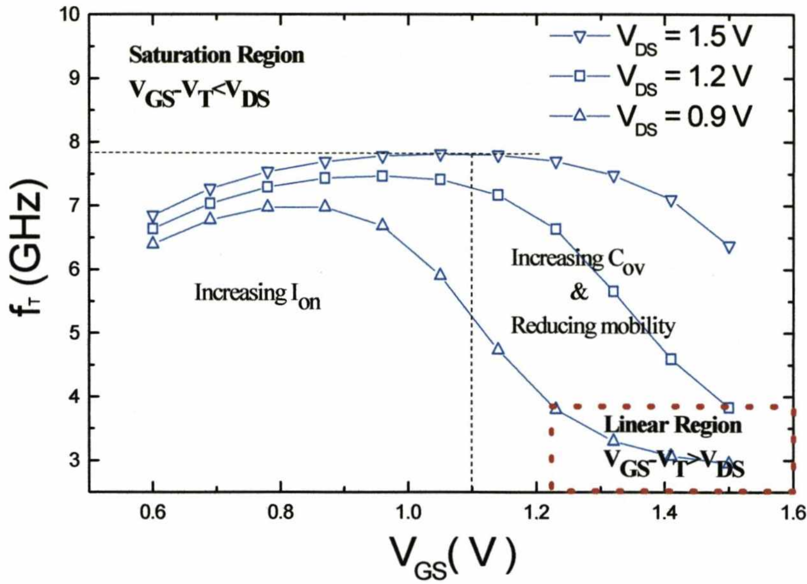



Fig 7.11 $f_T$ vs. $V_G$ of a double gate contact VMOSFET with L=100nm, W=30um, $t_{FILOX}$=40nm.

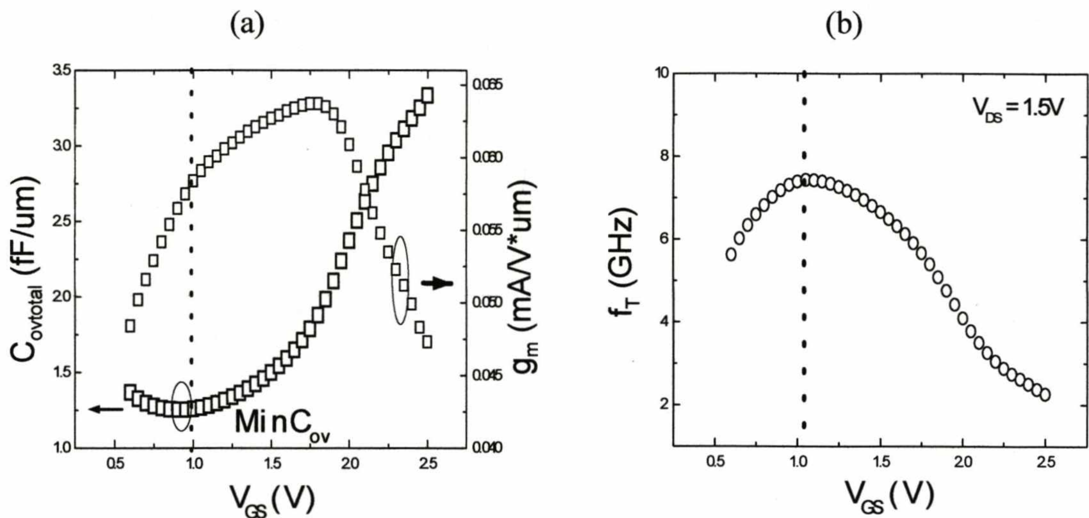



Fig 7.12 (a) Simulated total gate-drain/source overlap capacitance and $g_m$ vs. gate bias; (b) Simulated $f_T$ vs. gate bias; $V_{DS}$=1.5V. The on-current has been calibrated.

In the saturation region, $f_T$ increases with drain bias due to the influence of enhanced saturation current arising from short channel effects (DIBL and CLM). In the linear region, marked by the red square in Fig 7.11 ($V_{GS}-V_T>V_{DS}$), $f_T$ exhibits less roll-off with gate bias. This is because the $g_m$ has much less dependence on the gate bias in the linear region in accordance with equation 2.39. The vertical field dependent surface mobility reduction still causes $g_m$ reduction however.

## 7.2.4 The Effect of Gate Type on $f_T$

The frame gate structure brings the benefit in of protecting the channel from etch damage which can cause creation of interface states [94]. However, $f_T$ of FG devices is lowered than DGC devices. The $f_T$ comparison of the two gate types for 100nm and 150nm channel lengths devices is shown in Fig 7.13. The 100nm channel length device has maximum $f_T$ of the FG device which is 0.47 times that of the DGC device while for 150nm channel length devices, the maximum $f_T$ of FG is also about half that of the DGC device. However, another striking feature is that the $f_T$ values in FG devices show less drain voltage dependence compared to the DGC device due to a better DIBL suppression in FGC [94].

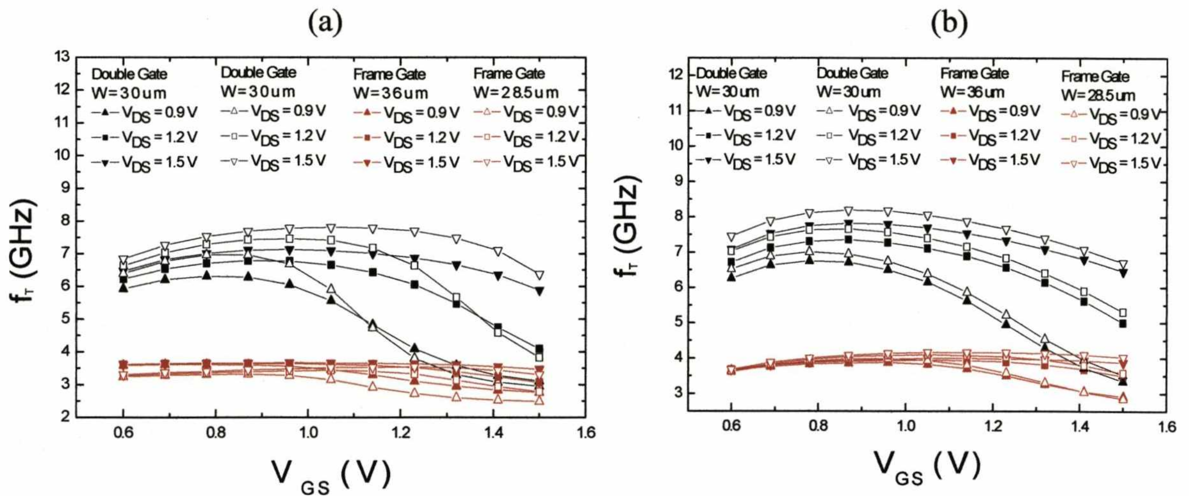



Fig 7.13 $f_T$ comparison of double gate contact and frame gate devices with (a) a channel length of 100nm (b) a channel length of 150nm. 40nm FILOX.

The reason for the lower $f_T$ for FG is related to a larger overlap capacitance area per unit width compared to DGC. This is confirmed by the 3D simulation results of the two different gate types. The two structures, simplified for the ease of numerical convenience, are shown in Fig 7.14. The total area of the poly-Si gate of the DGC device is 1 $um^2$ and

the total area of FG device is 1.16 $um^2$.The top poly-Si gate stripe is neglected due to its 20 times thicker oxide compared to other gate overlap area oxide. This means that the poly-gate area of the DGC device is 86% less than the FG device. The simulated gate-to-drain/source overlap capacitance values are presented in Fig 7.15. The saturated regime, total overlap capacitance in accumulation region for the DGC device is 29.1fF while for the frame gate device it is 33.1fF. The total overlap capacitance of the DGC device is therefore 88% of the FG device. This confirms that the larger poly-Si gate area in the FG device is the reason for its higher gate overlap capacitance and thus lower $f_T$ compared to the DGC device.

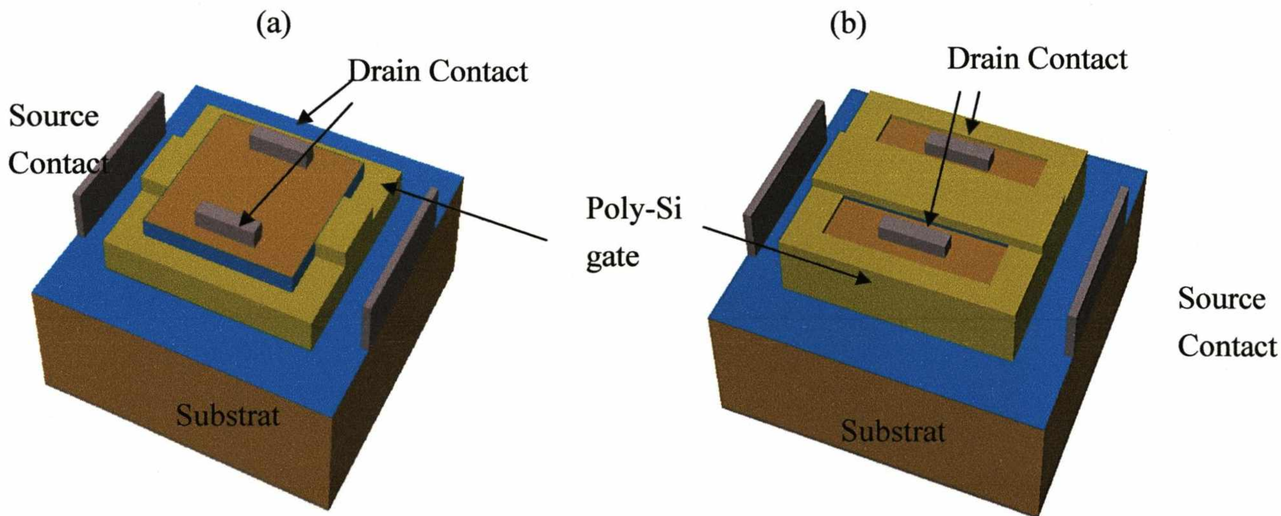



Fig 7.14 Structures of double gate contact and frame gate devices for 3D simulation.

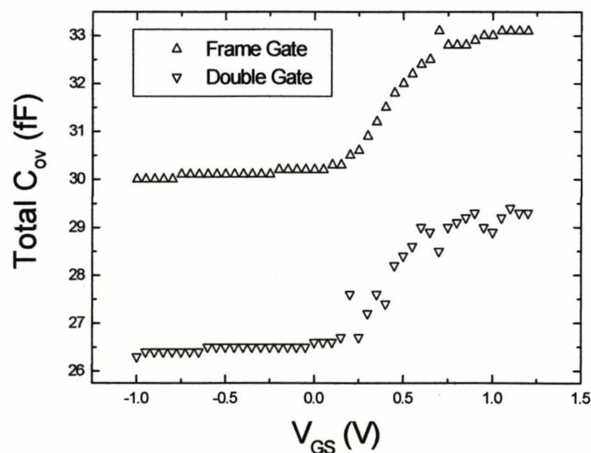



Fig 7.15 Overlap capacitance comparison of double gate and frame gate contact devices with structures shown in Fig 7.14.

## 7.2.5 The Effect of Channel Length and Channel Width on $f_T$

The $f_T$ of devices with channel lengths of 100 nm and 150 nm are compared in Fig 7.16. The longer channel device shows a generally better $f_T$ performance. At the maximum point where $V_{GS}$=0.87V, the 150nm device has a $f_T$ of 8.2GHz which is 5% higher than the maximum value of 7.8GHz of shorter channel length device at $V_{GS}$=1.1V. The reason of this anomaly is the effect of the lower contact resistance which was measured in terms of sheet resistance of the source and drain junction in 150 nm devices: namely, 50 to 150 ohm/sq lower than the 100 nm device. This results in a better drive current and transconductance for the longer device [110]. Ideally, the 150nm channel length device should have 33% lower $g_m$ compared to the 100nm device due to the channel length difference. The comparison of the measured $g_m$ for the devices with these two channel lengths but with a DGC structure is shown in Fig 7.17. It is evident that $g_m$ can be higher in the 150nm channel devices. The double hump variation of $g_m$ as a function of gate bias may result from significant variation of parameters amongst the 10 parallel

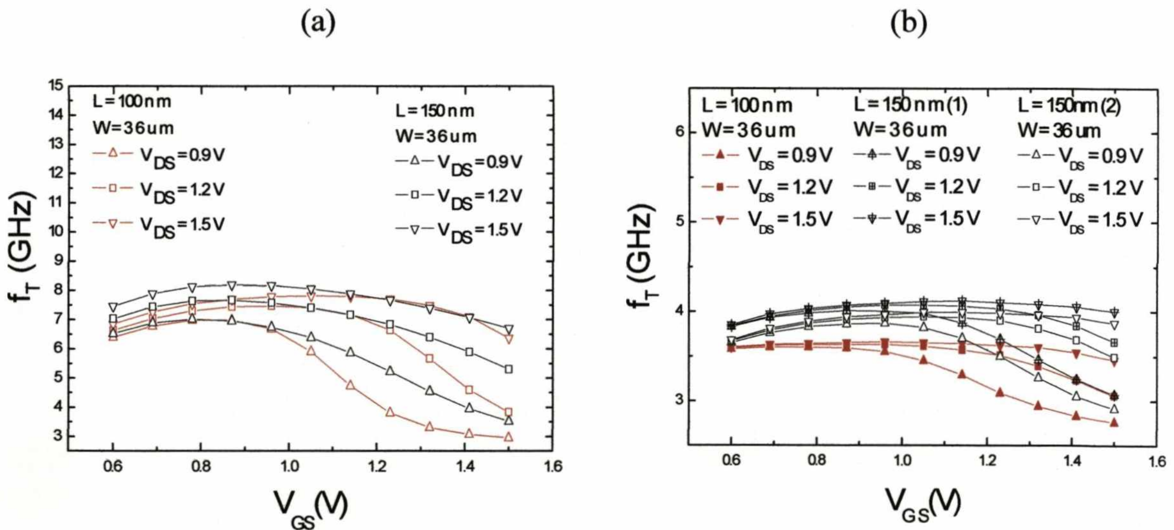



Fig 7.16 $f_T$ comparison of devices with 100nm channel length and 150nm channel length for both (a) double gate contact (b) frame gate contact. 40nm FILOX.

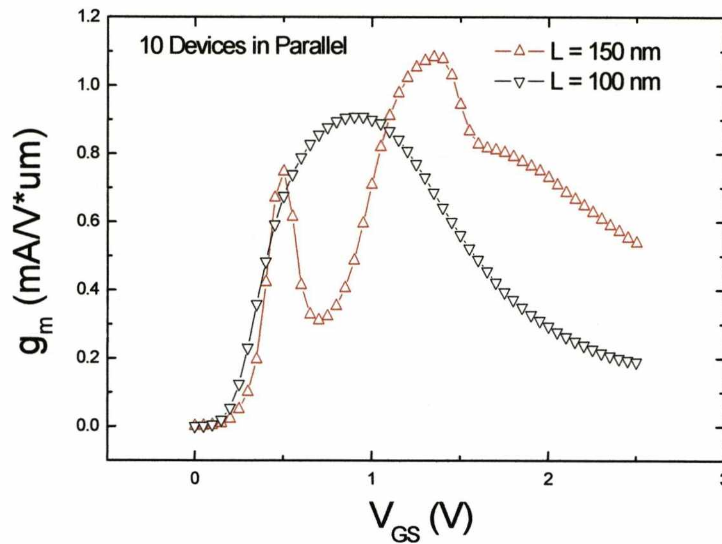



Fig 7.17 $g_m$ comparison of devices with 100nm channel length and 150nm channel length with a double gate contact.

connected testing devices. The cause of the sheet resistance variation among chips and wafers is likely to be related to process problems at the implantation step.

The comparison of $f_T$ from devices with 40nm FILOX and 100nm channel length but with different channel width is shown in Fig 7.18 where in (a) for the FG devices the channel width difference shows only small impact on $f_T$ while in (b) for DGC devices the width effect is bigger. The 24 um width DGC device has a $f_T$ of 8.6GHz at $V_{GS}$=1.05V and it is the highest value throughout all the test devices. However, ideally $f_T$ should not vary with channel width according to equation 2.41. The higher $f_T$ for the 24 um width DGC device might be caused by process variations such as lower junction sheet resistance giving higher transconductance per unit width ($g_{mo}$) or lower capacitance per unit width due to over-etching of the poly-Si gate spacers.

As shown in Fig 7.19, the device with increased active area also does not have improved $f_T$ as no improvement is seen on the on-current [110]. The reason is related to the fact that the series resistance component in these devices is dominated by the large contact

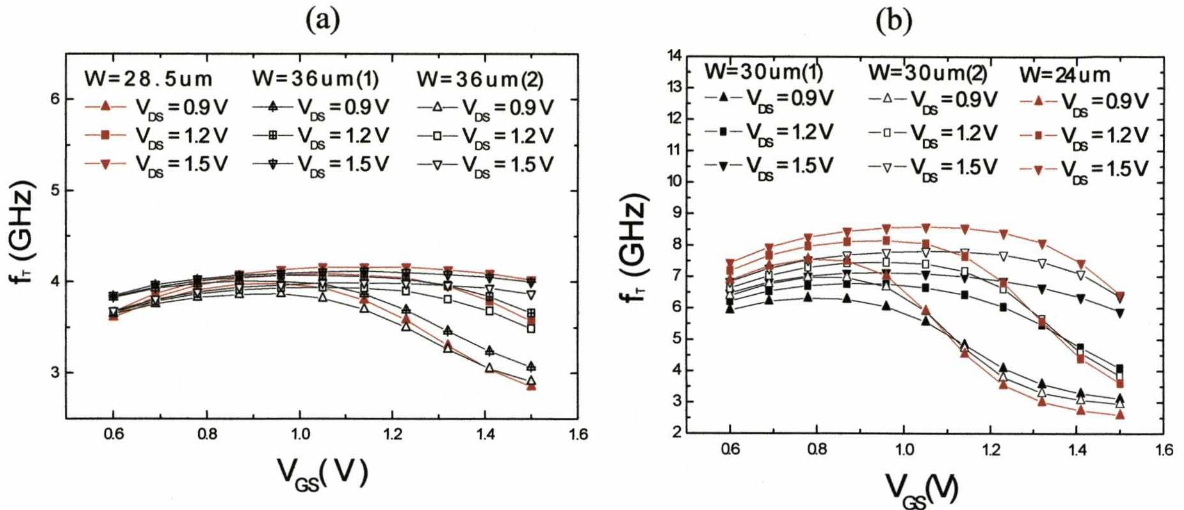



Fig 7.18 $f_T$ comparison of devices with different channel width for (a) double gate contact; (b) frame gate. 40nm FILOX, 100nm channel length.

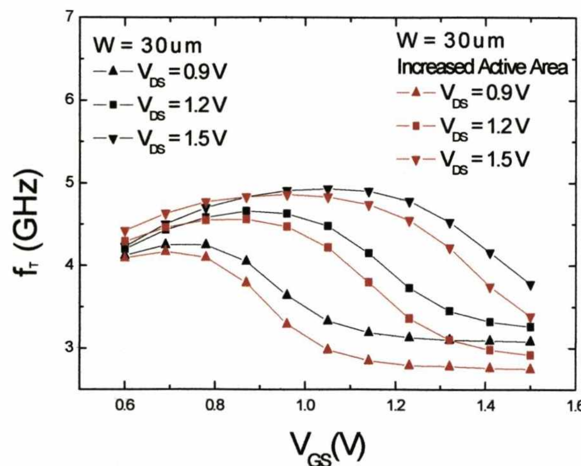



Fig 7.19 $f_T$ comparison of devices with and without increased active area. 40nm FILOX, 100nm channel length.

resistances at the drain and source contact interfaces rather than series resistance in the junctions. Since the contact geometry is also fixed, the resistance therefore the $f_T$ value does not varies with the active area. The small deviation of the $f_T$ curves is presumably caused by the process variation which is not significant as the devices are in the same chip.

## 7.2.6 The Effect of FILOX Thickness on $f_T$

In Chapter 6, the deterioration of series resistance in a 60nm FILOX structure was described. Analytical and numerical modelling of proved that the degradation is due to higher resistance in the accumulation region in the junctions, $R_{acc1}$ which is caused by severe FILOX encroachment. This limitation is also evidently seen in this batch of devices as shown in Fig 7.20 where the device with 60nm FILOX has a maximum $f_T$ only 0.6 times of that of the device with 40nm FILOX. Both devices have 100nm channel length and 30 um channel width. As the measured devices are located in the same chip, the large junction sheet resistance variation is likely to have little effect. A comparison of $I_DV_G$ curves for two samples with 40nm and 60nm thick FILOX are shown in Fig 7.21 (a). $V_{DS}$ is varied from 0.5V to 1.5V. A comparison of on-current in Fig 7.21(b) shows an agreement with the previous simulation study, namely that the on-current of the 60nm FILOX device is lower than that of the 40nm FILOX device. Note that in this case the 60nm FILOX device suffered from severe punch-through. The reason to use this device for comparison is because no good device with 60nm thick FILOX was found in the wafer.

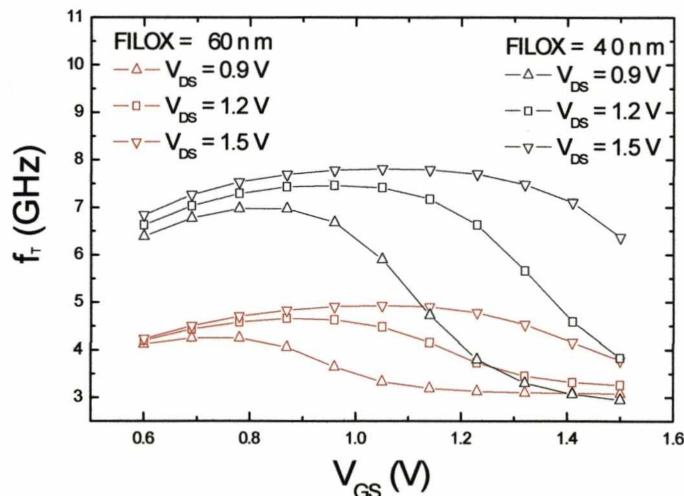



Fig 7.20 $f_T$ comparison of double gate contact devices with different FILOX thicknesses. 30um width, 100nm channel length.

### 7.2.7 Corner Effect

Corner effect at vertical sidewall edges was investigated using 3D simulation and results are shown in Fig.7.22. In Fig 7.22 (a), the results show that conduction current density is enhanced at the sidewall corner region by the poly-Si gate coverage while in (b) without a poly-Si gate wrapping the conduction current density is less. However the on-current is not significantly improved by the corner contribution as indicated by the comparison of the $I_DV_G$ curves with $V_{DS}$=1.5V shown in Fig 7.23. This means that in such wide devices, current enhancement by the corners has very limited impact on the overall current drive

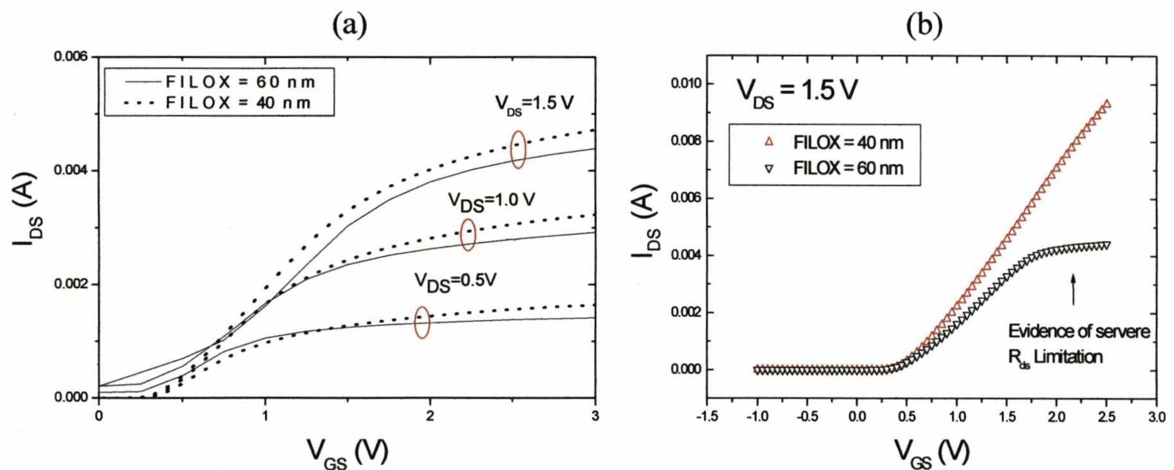



Fig 7.21 Drain current comparison of double gate contact devices with different FILOX thicknesses from (a) measurement (b) simulation. 30um channel width, 100nm channel length.

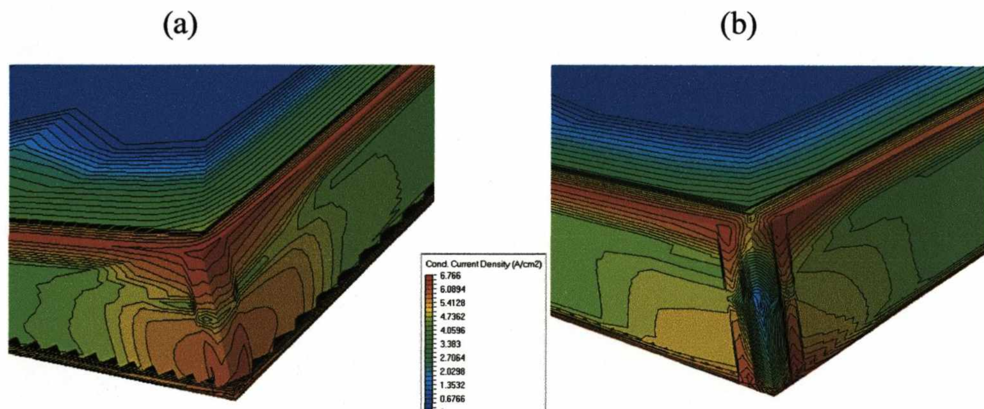



Fig 7.22 Conduction current density contour at the body corner region in (a) the device with poly-Si gate surrounding the corner; (b) the device without poly-Si gate surrounding the corner.

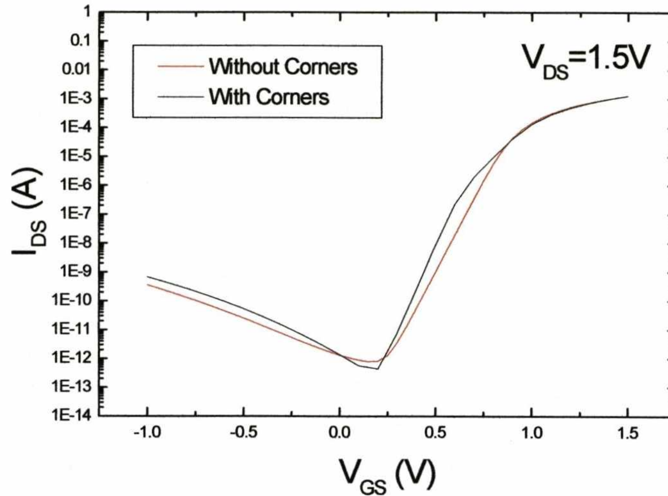



Fig 7.23 Transfer characteristics of devices with/without corner with $V_{DS}$=1.5V where no significant improvement on the on currents by corners is spotted W=4um.

and thus the effect on $f_T$ is negligible.

## 7.2.8 50nm Ideal Device Simulation

From the $f_T$ values presented in Fig 7.10(a), the best $f_T$ predicted by the process simulation generated device with 100nm channel length can achieve 30.5GHz which is a similar value to $f_T$ for the advanced lateral MOSFETs at the 0.35μm technology node according to ITRS road map [3, 111]. Further ideal device simulation with 40nm FILOX and 50nm channel length is conducted with the junction abruptness set to the ITRS requested value of 2.7dec/nm and bodying doping of $2 \times 10^{18} cm^{-3}$ for short channel effect suppression with the doping profile along the channel as shown in Fig.24 (a). Note that in the structure from the previous process simulation, the junction abruptness is 10 nm/dec which is a result of diffusions after 1100°C 10s RTA. This value needs to reduce to 2.7dec/nm for a 50nm technology node in order to meet the ITRS standards for SCE and series resistance values [112]. This requires an advanced laser annealing technique in the rapid thermal annealing step for ultra abrupt junctions [113].

In the simulation structure the oxide thickness is also set to 2nm to gain sufficient gate control against the short channel effect. The simulated $f_T$ values as a function of gate bias is shown in Fig 7.24 (b) with $V_{DS}$=1.0V. The peak $f_T$ within gate bias of 1.5V can reach as high as 99.4GHz. At the other hand, the road maps show that $f_T$ for 0.1um advanced lateral Si-MOSFET varies from 100GHz to 130GHz [3, 111]. Therefore this corresponds to an almost three-generation-hop in RF performance that can be ultimately achieved with VMOSFETs using a 0.35μm lithography stepper with the ultra-low junction abruptness value compared to the advanced lateral Si-MOSFET at the same lithography technology node.

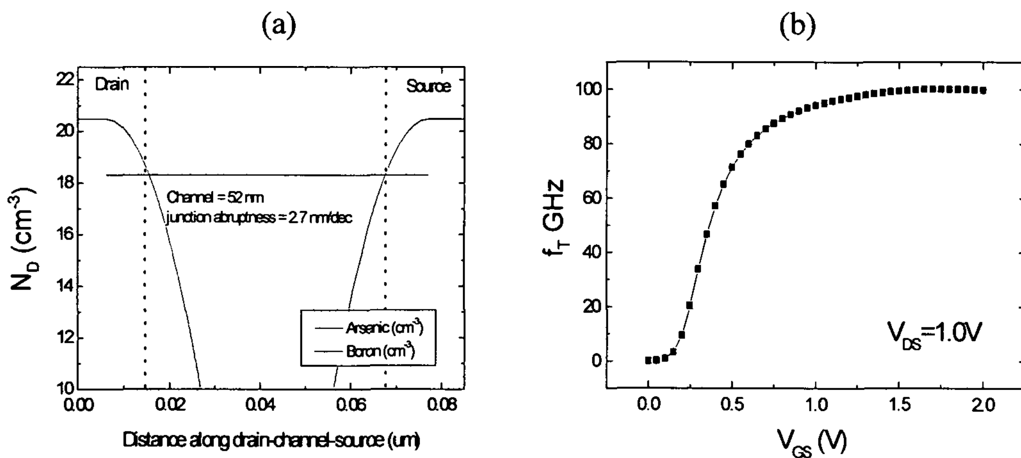



Fig 7.24 (a) Doping profile along the drain, channel and source in a simulated VMOSFET with 50nm channel length and 40nm FILOX; (b) Extracted $f_T$ vs. gate bias.

## 7.3 Summary

In this chapter, the $f_T$ characteristic of VMOSFET-FILOX devices with a number of different structures under different gate and drain bias conditions has been presented. The de-embedding process has indicated that there are only capacitance parasitic components in the RF layout pads. A method that only requires measurement of the current gain at the operation frequency enables easy assessment of $f_T$. The highest $f_T$ obtained was 8.6 GHz, for a double gate device with a channel length of 150nm, a channel width of 24um and

FILOX thickness of 40nm with $V_{DS}$=1.5V and $V_{GS}$=1.1V. The simulation of this device generated by the process simulation shows the peak $f_T$ can go up to 24GHz for 40nm FILOX device and 30.5GHz for 60nm FILOX device which is a similar value to $f_T$ for the advanced lateral MOSFETs at the 0.35μm technology node according to ITRS road map. The comparison of experimental and simulated on-currents of this device suggests that the reason of low $f_T$ can be attributed to large contact resistances. Generally speaking $g_m$ increases with drain bias results in an increase in $f_T$ due to short channel effects. The simulation shows that the combination of gate bias dependent transconductance and gate overlap capacitance determines the maximum $f_T$ and the corresponded $V_{GS}$. The double gate contact structure provides a higher $f_T$ than the frame gate contact structure due to the lower overlap capacitance. This was further confirmed by 3D simulation. The wafers containing 150nm channel length devices exhibit lower junction sheet resistance than those with 100nm channel length devices. This results in higher $f_T$ for the longer channel devices. Width effects are ideally, likely to be negligible although narrower devices can show higher $f_T$ due to the influence of lower junction sheet resistance. Both the measured and simulated on-currents suggested that 40nm FILOX devices have a significant advantage in providing a higher $f_T$ over the 60nm FILOX. The reason is believed to be related to the impact of FILOX thickness on the series resistance. Well-meshed 3D simulations have further provided results indicating that the corners at each sidewall edge bring little impact on wide devices though higher conduction current density is evident at the corner regions. Further ideal device simulation with 40nm FILOX suggests that with the junction abruptness improved from the original 10dec/nm to the ITRS requested 2.7dec/nm for a 50nm channel length, the peak $f_T$ within gate bias of 1.5V can reach as high as 99.4GHz. This corresponds to an almost three-generation-hop in RF performance that can be ultimately achieved with VMOSFETs using a 0.35μm lithography stepper compared to the advanced lateral Si-MOSFET at the same lithography technology node .

# Chapter 8

# EKV Modelling

## 8.1 Introduction

It is described in the Appendix E that the EKV model has the advantages of more physics based and convenience in modelling low power RF/analogue MOSFETs [114-116]. Therefore in this project, the EKV 3.0 model which provides a variety of accurate physical description on higher-order small device phenomena was used for the VMOSFET-FILOX batch devices. Device parameters were obtained using the EKV model extraction tool kit implemented in the IC-CAP platform using the following steps: data acquisition, model simulation, curve fitting, parameters extraction and optimization. These steps are now described.

## 8.2 Data Acquisition

A DGC VMOSFET-FILOX device with 40nm thick FILOX, 30 um channel width and two different channel lengths was selected because of their better $f_T$ performance compared to that of frame gate. The DGC devices near the flat on the wafer where seen to show the lowest level of interface states and gate oxide leakage and so were selected for study. DC characterisation of devices across the four wafers for four different channel lengths, showed wide variations in sheet resistance and interface state density. An example of the variation in current-voltage characteristics for wafers W2, W3 to W1/W4 is shown in Fig 8.1. It was apparent that devices from W1 and W4 had lower interface state density and thus better sub-threshold slopes and were chosen for investigation. The W1 and W4 devices had nominal channel length of 100nm and 250nm respectively. Both devices have a channel width of 30um.

The input data needed for DC modelling includes

(a) $I_DV_G$ curves under a low drain bias (0.05V) and a high drain bias (1.5V) with six body biases varies from 0 V to 2.5 V at a step of 0.5V;

(b) $I_DV_D$ curves with a six gate biases varies from 0V to 2.5V at a step of 0.5V under a low body bias (0.05V) and a high body bias (-2.5V).

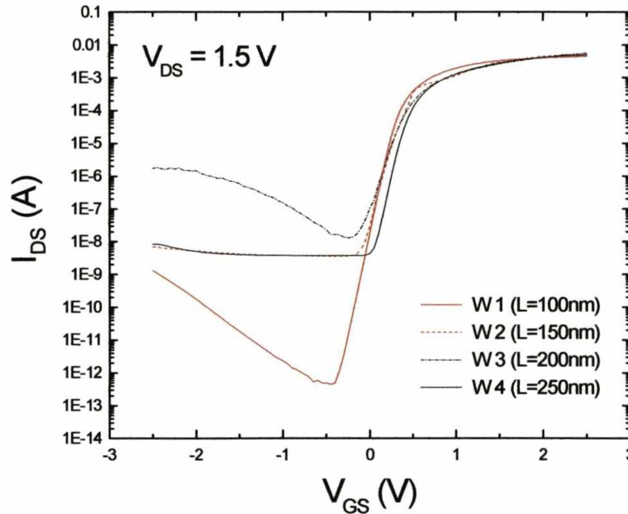



Fig 8.1 Transfer characteristics under $V_{DS}$=1.5V from DGC devices with 40nm FILOX and 30um channel width in the four wafers.

The analysis of these two sets of data is now undertaken and the following assumptions are made. The average junction depth of the transistor was taken as 150nm, to accommodate for the deep top junction. The distance between the poly-Si gate to the field oxide at the pillar bottom is set at 1.5um. A gate oxide of 2.93 nm was obtained from the extraction results from the Ellipsometry measurements [95].

## 8.3 Extraction Strategy

The extraction process is summarised in [117] and re-illustrated in Fig 8.2. The longest channel length (250nm) device was taken as the 'long and wide device' (long device). During the extraction of the parameters for the long device, the body doping level of $1x10^{18}cm^{-3}$ should ensure reasonably good immunity to short channel effects. The $C_{ox}$

parameter was obtained by fitting against the large planar capacitor C-V plot; the threshold voltage, body effect, and surface mobility parameters were extracted from the long device characteristics by fitting. From the 'short and wide' device (short device) with a channel length of 100nm, the series resistance parameter, charge sharing, DIBL, short channel effect related threshold voltage factors, velocity saturation and channel length modulation were extracted. Through the fitting of junction and gate overlap capacitances C-V measurement, the capacitive parameters regarding to the junction boundary doping profile, junction area and overlap region area can be obtained. Finally, given a reliable DC model, the S parameters fitting allows AC parameters of gate sheet resistance, substrate network components and optimized junction/overlap capacitance parameters.

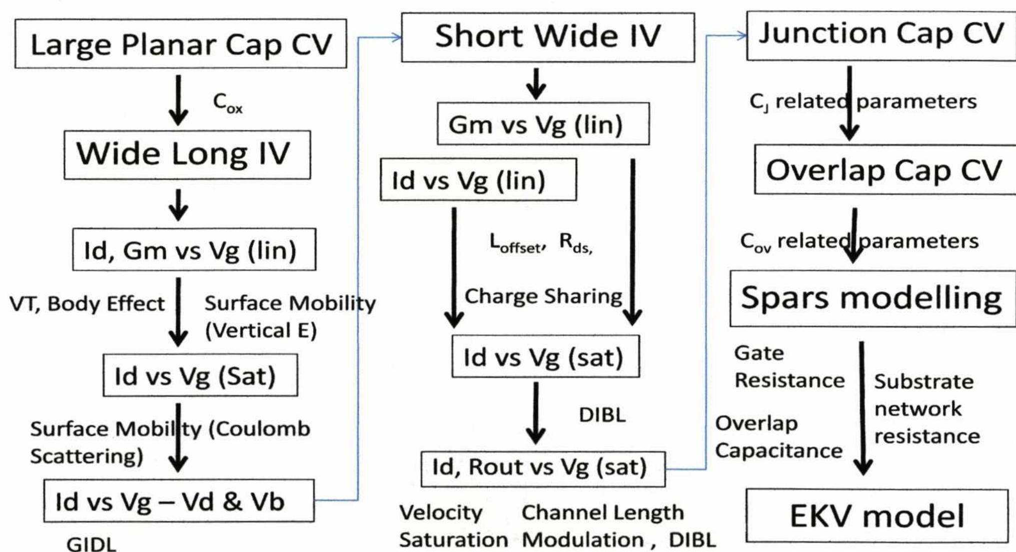



Fig 8.2 EKV model parameters extraction strategy. [117]

## 8. 4 Parameter Extraction

With the device information and input data imported into the EKV tool kit, the first step is to load the simulator from the Advanced Design System into IC-CAP and then run a simulation with default parameters. The $C_{ox}$ parameter was then extracted by fitting the

simulated large planar gate oxide capacitor C-V with the measured data in the accumulation region as shown in Fig 8.3 where the solid line represents the simulation data and the symbols represent the measured data. The $C_{OX}$ value was also confirmed by hand calculation.

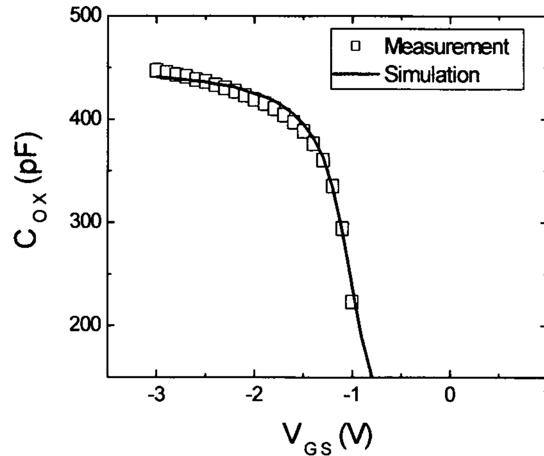



Fig 8.3 COX extraction by fitting the accumulation region in high frequency C-V plot for a large planar gate oxide capacitor (Line – Simulation data; Symbol – Experiment data as the same for the following graphs).

The threshold voltage at zero body bias (VTO), the body factor (GAMMA), field dependent mobility parameters were extracted from the transfer characteristics of the 250nm channel length device under low and high drain biases. The VTO and GAMMA were extracted from the fitting of threshold voltage and sub-threshold slope for the $I_DV_G$ curve with $V_{DS}$=50mV with $V_{BS}$ varied from 0V to -2.5V with a -0.5V step. Fitting of the current and transconductance measurements above the threshold voltage, gave the transconductance factor KP and the mobility model parameters E0, E1, ETA which describes the mobility reduction due to the vertical field effect. The $I_DV_G$ curve with $V_{DS}$=50mV after the fitting is shown in Fig 8.4. It is apparent that the moderate inversion operation region at high body bias proved difficult to fit. The reason might be related to the presence of $SiO_2$/Si interface states that influence the moderate inversion current at high body bias.

The parameters ZC and THC describe the Coulomb scattering dependence within the mobility model. However, it is demonstrated in Fig 8.5, that even after using the optimizer tool kit it was still difficult to obtain good fits for $I_DV_G$ and $g_m$ with $V_{DS}$=1.5V above $V_{GS}$=1.0V by just tuning these two parameters.

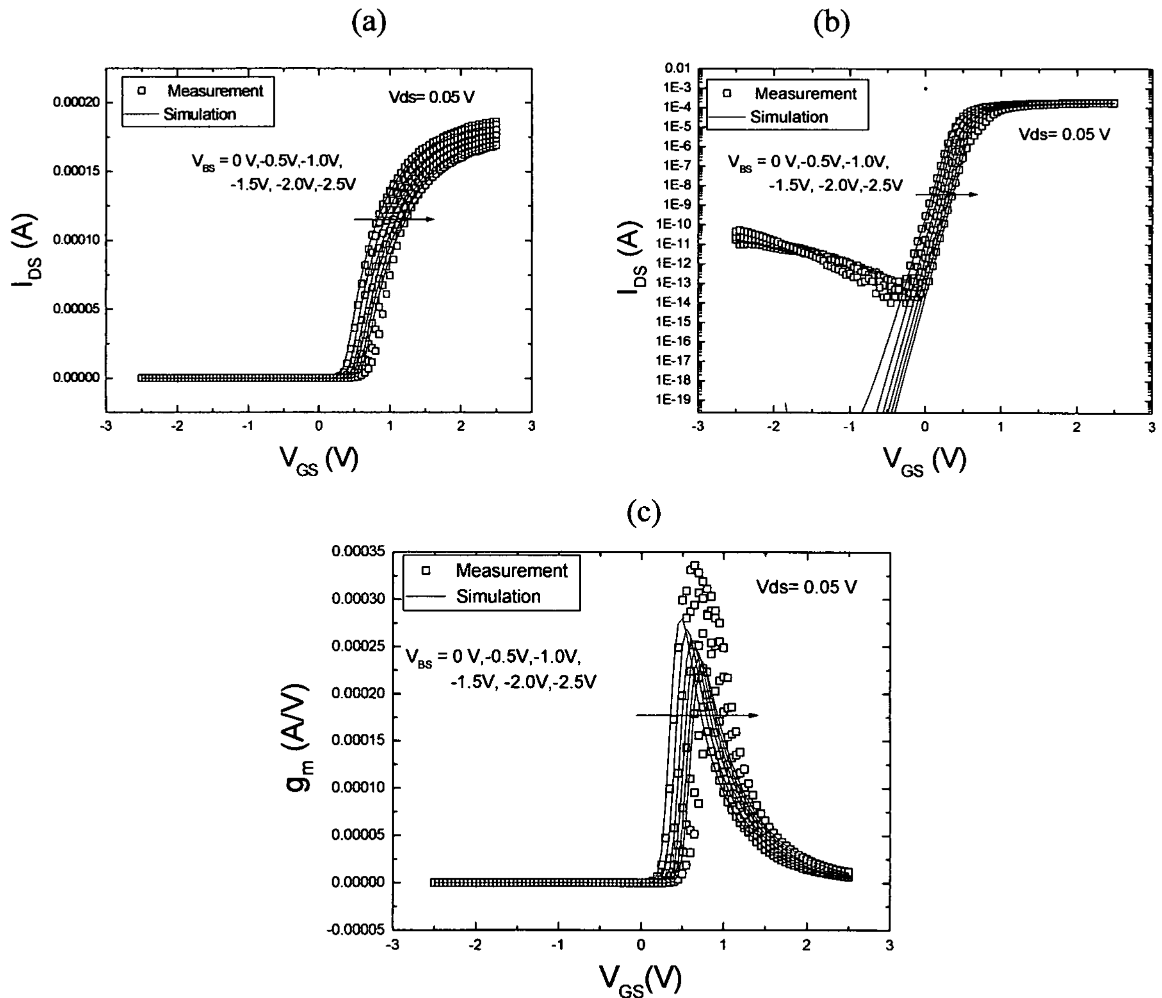



Fig 8.4 VTO, GAMMA, KP, E0, E1, EKA extraction by fitting the simulation and measurement in (a) linear graph of $I_DV_G$; (b) log graph of (a); (c) $g_m$; all with $V_{DS}$=50mV.

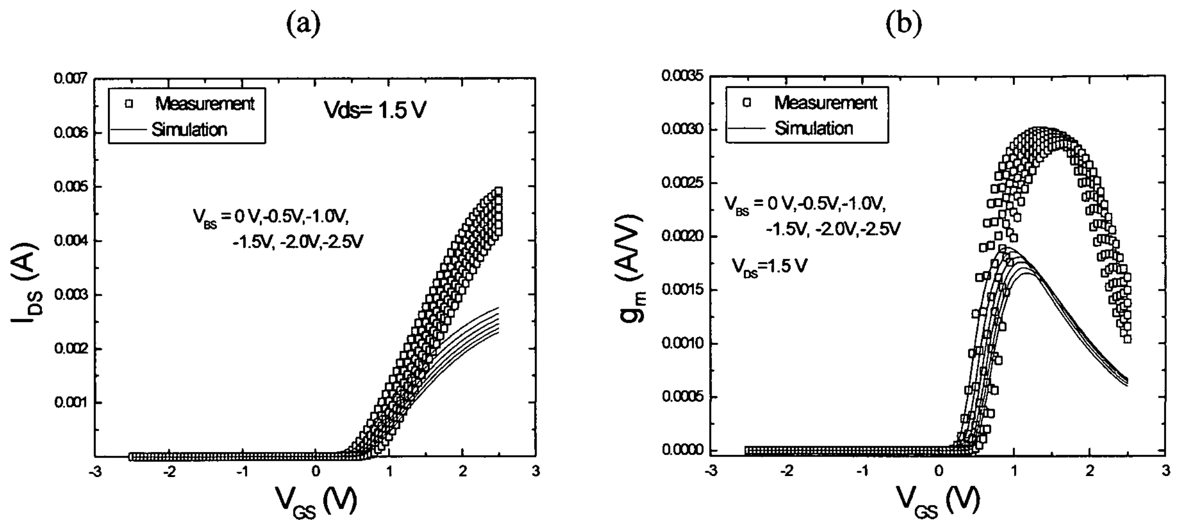



Fig 8.5 ZC and THC extraction from measured and fitting (a) $I_DV_G$ and (b) $g_m$ through a auto-optimiser tool kit; $V_{DS}$=1.5V.

Using the 100nm channel length device, the series resistance related parameter RLX was first extracted by fitting both the on-current of the $I_DV_G$ curves with $V_{DS}$=50mV and $V_{DS}$=1.5V consistently. The CE effect coefficient on threshold voltage LETAD and the slope factor dependence on CS effect parameter NCS were extracted by simultaneously fitting the $I_DV_G$ curves under $V_{DS}$=50mV with different body biases. The DIBL effect coefficient SIGMAD and the corresponded factor ETAD that affects the slope were extracted from the difference of the threshold voltage between the $V_{DS}$=50mV and $V_{DS}$=1.5V and fitting of the slopes at low gate biases. The drain to source leakage current characteristic at negative gate bias was left unfitted at this stage due to anomalies likely to arise from non-uniform oxides (gate and FILOX transition in FILOX encroachment region) and the asymmetrical junctionsstructure inherent in VMOSFETs. The final $I_DV_G$ and $g_m$ curves after above fitting are shown in Fig 8.6. The velocity saturation parameters UCRIT and early voltage effect factor LAMBDA were then optimized from the fitting of the short channel device $I_DV_D$ and output resistance characteristics with both $V_{BS}$=0V and $V_{BS}$=-2.5V. The final fitted curves are shown in Fig 8.7 (a)-(d). Previous research suggested that the body doping at the pillar top can be two times that at the pillar bottom

[66]. So the reverse short channel effect related parameters NLR was used to take into account the non-uniform body doping effect on the body effect coefficient and thus the sub-threshold slopes of both the long and short devices. Moreover, the value for the long channel threshold voltage correction AVT was also used to maintain the threshold voltages of the long device with different body biases after the previous short device fittings.

After RLX extraction from the short channel device, the simulated $I_DV_G$ curve of the long channel device under $V_{DS}$=50mV above the threshold voltage now gives a lower current as shown in Fig 8.8. The underestimated current level above the threshold voltage suggested the influence of series resistance even exists in the long channel device because the value of the contact resistance is evidently high as described in section 7.2.2. This also

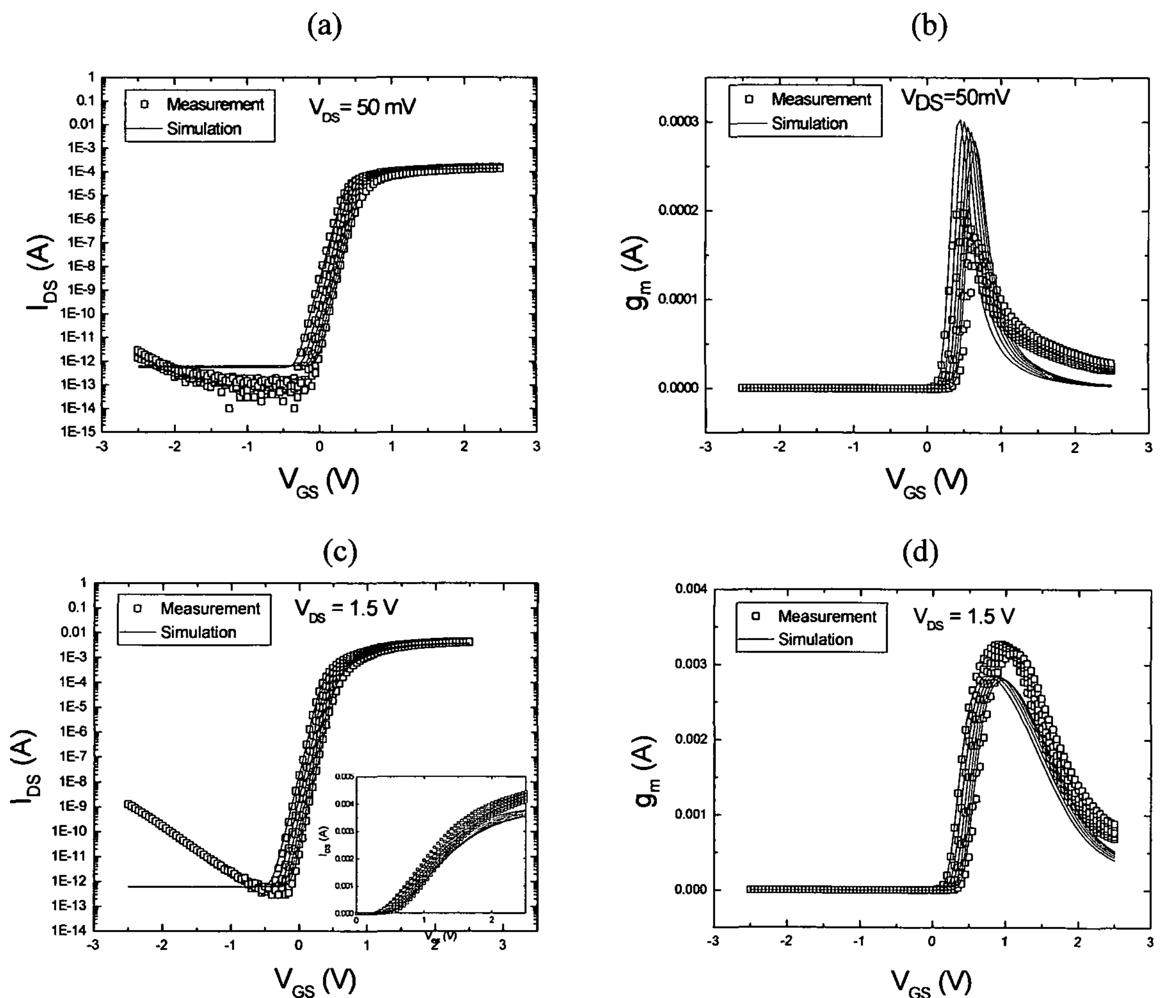



Fig 8.6 DL, RLX, ETAD, LETAD and NCS extraction through fitting of measured and simulated $I_DV_G$ and $g_m$ curves of the short channel device with $V_{DS}$=0.05V (a) - (b) and $V_{DS}$=1.5V (c) - (d) .

indicates that the channel length in the long device is not sufficiently long enough to neglect the series resistance effect. Nominally in the long channel case the series resistance should be considered negligibly small compared to the channel resistance in the long channel device.

Since the series resistance effect was omitted in the initial simulation of $I_DV_G$ curves of the long channel device before RLX extraction, the extracted KP and the mobility reduction factors due to vertical gate field were then underestimated as result of ignoring RLX. However, by scarifying accuracy of the long channel device model, the fitting of the simulated current above the threshold voltage of the short channel device could still be maintained.

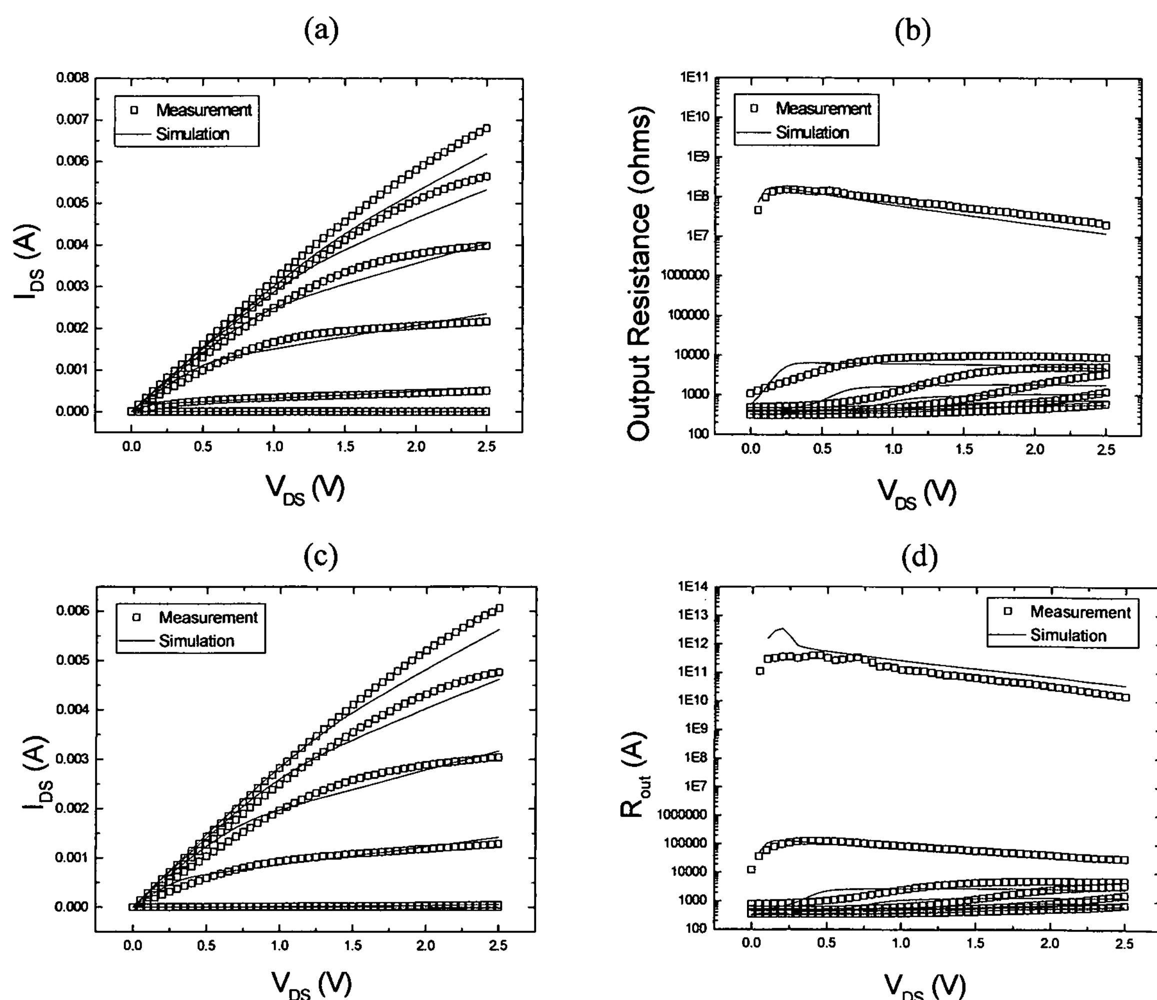



Fig 8.7 Measured and simulated $I_DV_D$ and output resistance curves of the short channel device after extraction of UCRIT, LAMBDA: (a) $I_DV_D$ with $V_{BS}$=0V; (b) resistance curves with $V_{BS}$=0V; (c) $I_DV_D$ curves with $V_{BS}$=-2.5V (d) resistance curves with $V_{BS}$=-2.5V.

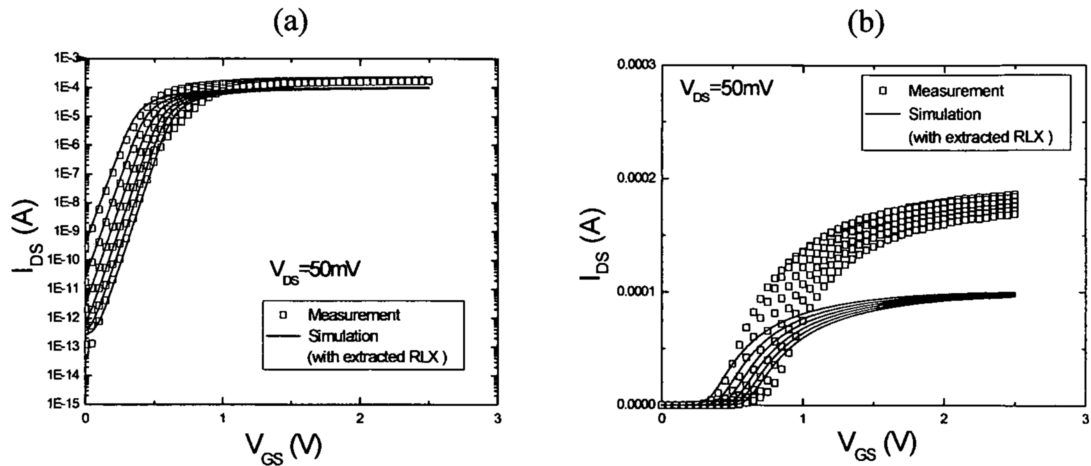



Fig 8.8 Comparison of measured and simulated $I_DV_G$ curves of long device using the RLX extracted from the short device in (a) log scale (b) linear scale.

By adjusting RLX to fit the simulated currents above the threshold voltage for $V_{DS}$=1.5V and $V_{DS}$=50mV of the long device, the fitting of the short channel device would then become poor as a result. It can be concluded therefore that the self-consistent fitting of the transfer characteristics for both devices using a single series resistance parameter can not be achieved. Different series resistance values in the short and long channel devices are apparent in Fig 8.8 by comparing on-currents for $V_{DS}$=1.5V. Since the channel length difference is 2.5 times, it is expected theoretically that for the same series resistance, the on-current of the short device should also be about 2.5 times that of the long device. This point is substantiated by the simulation data represented by the solid line in Fig 8.9. However, the measured on-current of the short device (circle plus line) is only about 1.4 times that of the long device (square plus line). This indicates that short channel device has a larger series resistance than the long channel one. In the rest of the modelling, the series resistance in the short device is used.

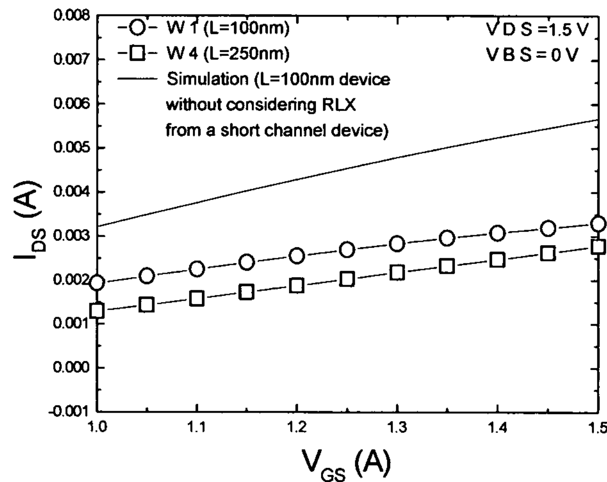



Fig 8.9 On-currents comparison of the long and the short devices to the simulated short device. Use the same RLX that is extracted from the long device fitting.

The channel length modulation (CLM) is also evident in the measured long channel $I_dV_d$ curve where the induced saturation current enhancement is marked out by red arrows in Fig 8.10. Using the extracted Early voltage and 'critical velocity for electrons' factor UCRIT from the short device, the simulated saturation current for the long device shows good fitting to the measured curves at least for gate bias below 1.5V. The remaining saturation current difference is because the previously extracted critical velocity for electrons from the short device is not sufficiently high enough for the long device. Note that the long channel length is likely to be shortened by 20nm as a result of the pillar over-etching. A conclusion can be drawn that apart from the series resistance, the critical velocity for electrons also show inconsistency between the short and long device. The higher critical velocity for electrons induces higher velocity saturation in the long device than originally expected from theory.

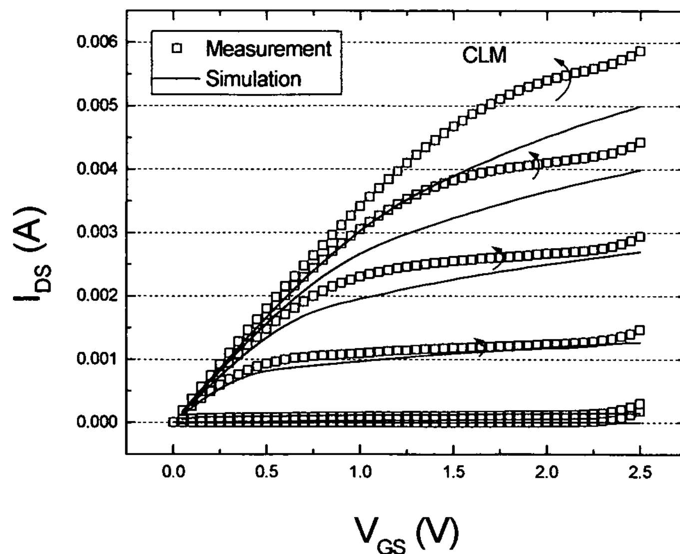



Fig 8.10 Fitting of the measured and simulated output characteristics of the long channel device using the channel length modulation related parameters and critical velocity for electrons factor extracted from the short device. (RLX is extracted from the long device).

Having obtained the SCE and saturation current related parameters using the short device, the $I_DV_G$ curve and $g_m$ curve with $V_{DS}$=1.5V of the long channel device are re-simulated without RLX extracted from the short channel device. The results are shown in Fig 8.11 where better fitting is demonstrated compared to the initial fitting shown in Fig 8.8. This provides some confidence of the validity of the previous extraction approach for the transconductance factor, mobility model, saturation velocity and short channel effect related parameters. The difference in the high gate bias regime is likely to be caused by the

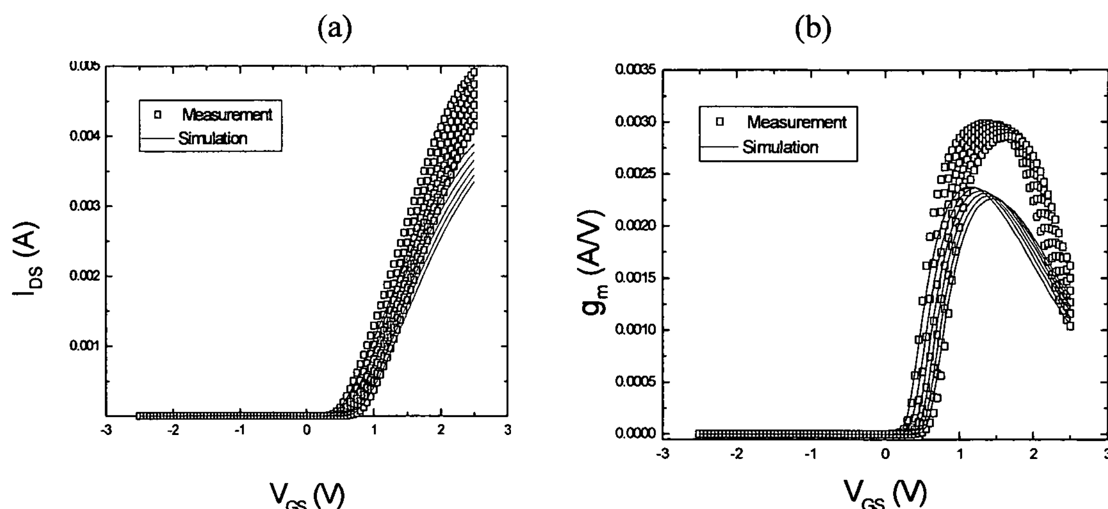



Fig 8.11 (a) Reasonably good fitting of $I_DV_G$ with $V_{DS}$=1.5V in the long channel device after using the velocity saturation and SCE related parameters from the short device. (Use the RLX value that is extracted from the long device); (b) fitting of $g_mV_G$ with $V_{DS}$=1.5V.

aforementioned underestimate of velocity saturation and SCE related parameters in the long device.

Since the series resistance should be also be considered in the initial fitting of the $I_DV_G$ curve with $V_{DS}$=50mV for the long device, the extracted transcoductance factor, mobility model related parameters have therefore somewhat been over-estimated in order to maintain the fit. It has also been proved to be difficult to maintain fitting consistency for both the long and short channel devices because of inconsistency in the series resistance and critical velocity for electrons parameter. Moreover, due to process variation across the wafers and lack of good devices with different channel length, creating a scalable model is impossible as a result of lack of consistent devices with a number of different channel lengths on this batch of VMOSFET-FILOXs. However, it is observed that the short device data shows better fitting than the long device. It can be concluded that the short device modelling can be considered valid and the results can be used for the RF modelling.

The measurements of the drain/source junction capacitance in the device are used for the estimation of junction capacitance area parameters which are the area component of diode capacitance CJS/CJD, area exponent of diode capacitance MJS/MJD.

The measurements of the overlap capacitance of the gate-to-drain/source area test structures are used for the estimation of overlap capacitance area parameters which are the length of the gate overlap area LOV, bias-independent overlap capacitance CGSO/CGDO and fringing capacitance factor KJF/CJF.

The frequency responses of the measured S parameters of the short channel device fitted by the simulation are demonstrated in Fig 8.12 where gate bias sweeps from 0 to 2.5V while $V_{DS}$ sweeps from 50mV to 1.5V. However, in order to obtain the above ultimate S parameter fitting, apart from the S11, S12, S21, S22 parameters themselves, their corresponded phase and magnitude curves are also used. The fitting starts with the extraction of junction and overlap capacitance parameters as large derivation of the

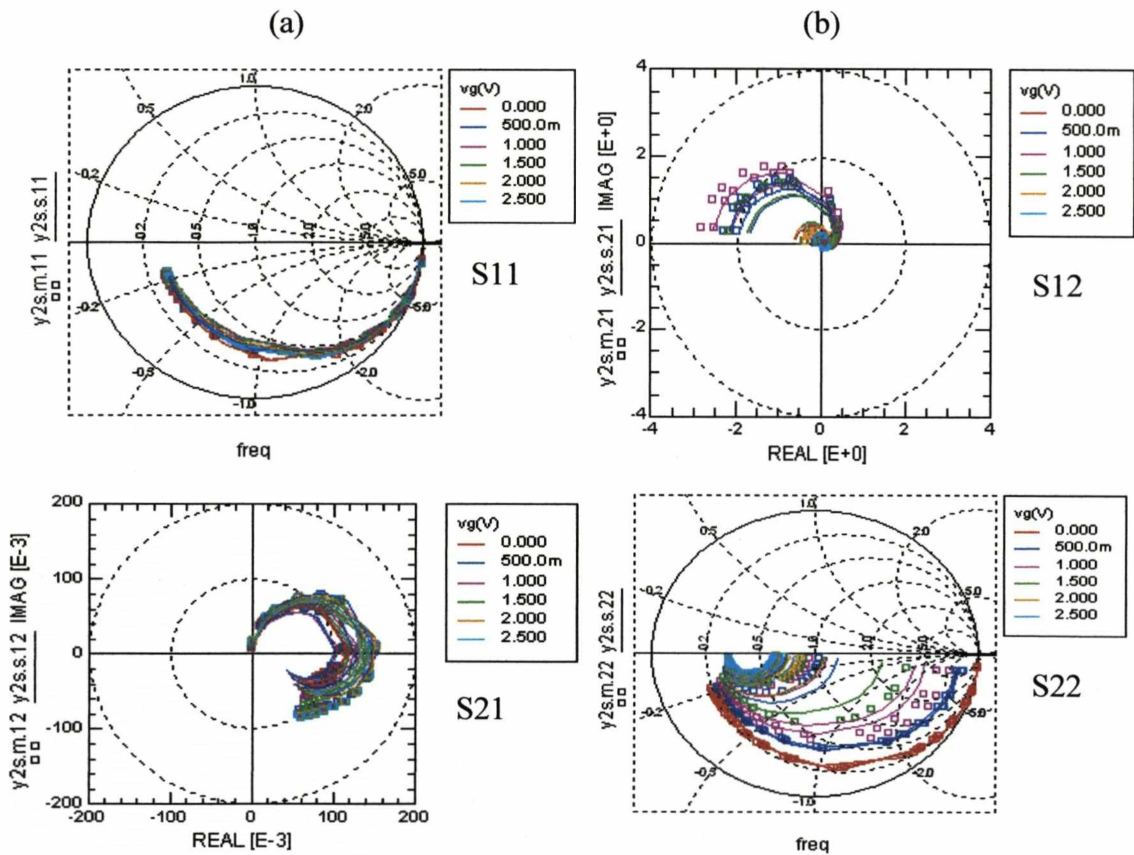



Fig 8.12 Fitting of (a) S11, (b) S12, (c) S21, (d) S22 parameter curves of the short channel device with $V_{GS}$=0, 0.5V,1.0V, 1.5V 2.0V, 2.5V and $V_{DS}$=50mV, 0.5V,1.0V, 1.5V. ($V_{DS}$ sweeping orders not)

simulated data and measurement is seen on S parameters at the first time. Based on the values from the CV plots, the CJD, CJS, MJD and MJS are extracted from the fitting of

S22 and its phase curve. LOV, CGDO and CGSO are extracted from the fittings of magnitudes of S12 and S21. The gate sheet resistance parameter RGSH and gate-to-body overlap capacitance CGBO are extracted from the fitting of magnitude and phase part of S11. The S22 curve is not very sensitive to the variation of the substrate network resistance parameters even at 10 GHz which proves it not sufficiently high enough for these effects to be seen. However, these parameters are used to fine tune the S22 curve.

Through the above fitting steps, it was found that the junction and gate overlap capacitances parameters at drain side have much more significant impact on the above three S parameters than the source. It is also concluded that higher drain junction value in VMOSFET induces higher output impedance under high gate bias in the RF range. The coarse fitting in S parameters curves under medium drain and gate biases is likely because of the device variation between the one used for AC measurement and the one for DC measurement. The ignorance of the non-quasi-static effect in the model might also be the reason for the worse fitting seen at high frequency simulation.

## 8.5 Summary

The DC part of the compact model of the double gate contact VMOSFET-FILOX with 40nm thick FILOX has been constructed using the EKV3 modelling tool kit in the IC-CAP platform. The transconductance factor and mobility related parameters are overestimated in a representative 'long' channel device (250nm). This is the longest device available but it suffers from series resistance and short channel effects which compromises the methodology. Good fittings of the $I_DV_G$, $g_m$ and $I_DV_D$ characteristics of the short (100nm) device over a range of bias conditions have confirmed a good accuracy of the compact model if only for the short device. Nonetheless, several anomalies will need to be

considered carefully if scalable modelling is constructed in the future. Apart from the series resistance and short channel effect that exist in the 'long device', the inconsistency of series resistance among the long and short devices adds more uncertainty when extracting some scalable parameters such as channel length dependent drain and source charge sharing, DIBL, channel length modulation factors. Inconsistent values for critical velocity of electrons also introduced difficulties in obtaining universal fitting among devices with a range of channel lengths. The variation of channel length due to the pillar height over-etch also contributes to model inaccuracy. All these inconsistency issues are believed to arise from the relatively immature fabrication process but will be used to inform modifications to the next run. From CV measurements, the overlap and junction capacitance parameters are extracted. Through the fitting steps on S parameters and its corresponded phase and magnitude curves, the junction, improved overlap capacitance parameters extraction are achieved as well as the further extraction of the gate sheet resistance, gate-to-body overlap capacitance and substrate network parameters. It was found that the junction and gate overlap capacitances parameters at drain side have much more significant impact on the above three S parameters than the source. It can be also concluded that a higher drain junction value in VMOSFET induces higher output impedance in the RF range under high gate bias. Some unavoidable coarse fitting of S parameters curves under medium drain and gate biases is likely because of the characteristics variation between the devices used for AC measurement and the one for DC measurement.

Table 8.1 below illustrates the extracted DC and AC parameters. The physical meaning and analytical expression of each parameter involved in the EKV3 model can found in the user manual [118]. Table 8.2 summarises the physical effects included in the model and also indicates those phenomena not included in this modelling process.

Table 8.1 Extracted EKV model Parameters

| COX | gate oxide capacitance per unit area | 0.011825 $F/m^2$ | * | XJ | junction depth | 1.50E-07 m |
|---|---|---|---|---|---|---|
| PHIF | bulk fermi potential | 0.480286 V | * | VTO | long-channel threshold voltage | 0.332479 V |
| GAMMA | body factor parameter | 0.32786 $V^{0.5}$ | * | KP | transconductance parameter | 106E-05 $A/V^2$ |
| E0 | mobility reduction coefficient I | 1.59E+08 V/m | * | E1 | mobility reduction coefficient II | 7.98E+0 8 V/m |
| ETA | mobility Reduction due to vertical field factor | 2.87978 | * | ZC | lateral field induced mobility reduction factor I | 5.00E-06 |
| DL | effective length difference | 1.06E-08 m | * | THC | lateral field induced mobility reduction factor II | 0.002835 |
| UCRIT | longitudinal critical field | 1.16E+07 V/m | * | LAMBDA | channel length modulation factor | 0.887 |
| DELTA | order of velocity saturation model | 2 | * | QLR | threshold voltage factor of RSCE | 0.000236 |
| NLR | reversed short channel effect 2 | 0.000939 | * | LETA | charge sharing effect coefficient | 0.22733 |
| NCS | slope factor dependence from charge sharing | 1 | * | ETAD | primary DIBL coefficient | 0.760468 |
| SIGMAD | secondary DIBL coefficient | 2.03E-06 | * | RLX | series resistance factor | 3.0m |
| CJS | perimeter component of source junction capacitance | 4.2E-9 F/m | * | CJD | perimeter component of drain junction capacitance | 3.9E-9 F/m |
| MJS | area exponent of source junction capacitance | 2.67 | * | MJD | area exponent of drain junction capacitance | 0.07 |
| PBS | perimeter parameter of source junction capacitance | 0.445 | * | PBD | perimeter parameter of drain junction capacitance | 0.19 |
| CGSO | gate-source overlap capacitance | 1.13n | * | CGDO | gate-drain overlap capacitance | 0.7n |
| CGBO | gate-body overlap capacitance | 370n | * | RGSH | gate sheet resistance | 1.46 |

8.2 Physics modelled vs. un-modelled

| Modelled | Not modelled |
|---|---|
| Basic bias effect on the channel charge | Quantum mechanical effects |
| Mobility that covers all scattering | Gate oxide current |
| Series Resistance | Gate Induced Drain Leakage |
| Charge Sharing Effect | Impact Ionization |
| Drain Induced Barrier Lowering | Non-quasi-static Effect |
| Channel Length Modulation | Length and Width Scaling |
| Velocity Saturation | Temperature Dependence |
| Body Doping Non-uniformity | Noise |
| External and Intrinsic Resistance and Capacitance | |

# Chapter 9

# Conclusions & Suggestions for Future Work

## 9.1 Conclusions

In this thesis, technology designed to investigate the feasibility of CMOS process compatible vertical MOSFET for RF applications was explored both theoretically and experimentally. The simulation results exhibit a much better device performance than the fabricated device for both DC and AC aspects. Some important device performance inhibitors and anomalies in device characteristics were indentified. The underlying physics of these anomalies were studied with the assistance of analytical, numerical and compact models, in relation to the fabrication process in order to identify and propose further improvement to the technology.

The devices in the first batch were vertical MOSFETS with a junction stop (JS) structure, which was incorporated to suppress impact ionization, bulk punch through and form shallow top junctions. The device simulation indicates that the 70nm VMOSFET-JS device with a body doping of $3.0\text{x}10^{18}\text{cm}^{-3}$ and drain/source junctions of 50nm and 30nm have a $f_T$ of 33GHz with an on-current of 380μA/μm at $V_{GS}$=1.5V and an off-current of 7.6pA/μm. However, the characterisation shows that the best characterized on-current is 18 times lower than this value and 26 times lower than the value of the 70nm technology node in the ITRS road map. The additional limiting effect of the on-current is proposed to be due to the presence of additional series resistance connected to the top junction caused by a native oxide layer between the poly drain and the Si drain junction. Compared to devices with a thin JS layer, and no JS, it is observed experimentally that devices with 20nm thick JS structure provide significant suppression of the substrate current and the breakdown voltage in drain on top (DoT) mode compared to source on top (SoT) mode. This asymmetry provides strong evidence that the presence of the JS structure results in reduced junction electric field with in turn, successfully suppresses impact ionization. This batch of

devices was found to suffer from shifts (compared to theory) and variations in threshold voltage across the wafer as a result of possible channel length variation, the presence of fixed oxide charge and the fact that some devices have high interface trap densities at the top of the sidewall, due to over-etching during the poly-Si gate spacer definition. A numerical modelling study of short-channel effects (SCE) showed that the junction stop structure provides significantly better bulk punch-through immunity and SCE control compared to the conventional vertical device. The simulation results also showed that it is possible to provide a trade-off between the junction stop and body doping to reduce DIBL and increase channel mobility which in turn, leads to an improved $I_{on}/I_{off}$ ratio. For body doping of $5.0x10^{17}cm^{-3}$ and $6.0x10^{17}cm^{-3}$, the JS gives improvements in $I_{off}$ of 58.7% and 37.8% respectively for a given $I_{on}$. It is important to control accurately the drain spacer width which is the key parameter for controlling the depth of the top junction. The maximum $W_{dm}$ in a device was shown to be a critical point in the design of optimal the junction depth. It was defined as the point at which the SCEs saturate with increasing drain junction depth. In a 70nm device with a body doping of $1x10^{18}cm^{-3}$, this critical point is about 50nm which corresponds to a drain spacer width of 30nm. To maintain a DIBL and charge sharing effect induced $V_T$ shift within 220mV, a 5nm drain spacer width is needed.

The second batch comprised ultra-thin pillar capacitors with a variety of FILOX thicknesses and pillar thicknesses. Well-behaved C-V characteristics on 20nm thick Ultra-thin Pillar capacitors with 8nm FILOX indicated the potential for integrating the FILOX process with ultra-thin pillars which could be used to realize fully-depleted vertical MOSFETs. However, capacitors with 16nm, 24nm and 37 nm thick FILOX show less well-behaved C-V plots. At negative gate bias the oxide leakage of 37nm and 8nm FILOX were about the same where 16nm and 24nm have lower leakage level. The enhancement of oxide leakage in 37nm FILOX device might be related to a degraded mechanical stress

problem. Simulations indicate that the thicker FILOX induces more mechanical stress at the pillar bottom which in turn, may create a dislocation-induced leakage path and so enhance oxide leakage. The yield of 20nm ultra-thin pillar capacitors was found to drop from 80% for 20 nm thick FILOX to 50% for 37nm thick FILOX. The ultra-thin pillar capacitors with 37 nm FILOX and various pillar thicknesses showed a consistency in C-V characteristics. This consistency provides evidence that the FILOX process has been successfully applied to ultra-thin pillar devices.

A retrograde body structure was for the first time, designed to be integrated into a VMOSFET aiming for on-current enhancement while retain SCE control. For a 100nm VMOSFET-FILOX, to maintain a maximum threshold voltage shift of 245mV due to SCEs, the analytical model indicates that the maximum gate induced depletion edge in the body should be within 50nm. To maintain the mobility, the low doped surface region should be within 36nm. More accurate 2D numerical modelling indicated that the best retrograde body profile that can be achieved within the constraints of the current fabrication process is from 5.0 to 7.3 $x10^{17}cm^{-3}$ at the surface to 1.2 $x10^{18}cm^{-3}$ at the edge of $W_{dm}$. However, it was found that the fabricated retrograde body devices had an average body doping level of around $5.0x10^{18}cm^{-3}$ which has resulted in an over-doping of the intended retrograde body profile. The asymmetrical on-current, DIBL and breakdown voltage measured in DoT and SoT modes were found to be consistent with asymmetrical body doping level from top to bottom of the pillar. The leakage current in both gate oxide and gate-to-drain/source overlap region which has FILOX encroachment segments was found to be dominated by the direct tunnelling mechanism through the thin gate oxide region. Both gate and FILOX oxides showed good robustness against dielectric breakdown.

VMOSFET-FILOX devices which suffered from severe FILOX encroachment, exhibited a deterioration of on-current drivability which was found to be due to the increased series

resistance arising in the accumulation layer in the lateral junction depletion region, designated $R_{acc}$. It was found that avoiding FILOX encroachment above the region that defines $R_{acc}$ results in significant improvement of the $f_T$. An analytical and simulation study of series resistance components in VMOSFET-FILOX was presented indentifying two important parameters, namely the oxide thickness above, and the doping level in the accumulation layer. These two parameters determine the dominant components $R_{acc1}$ and in turn $R_d$ and $R_s$ and their gate bias dependent characteristics. The series resistance in each junction was quantified by using an impedance-RF method applied to 'virtual' devices generated from process simulations. By using a 40s RTA time or 15 degree angled tilt arsenic implantation for source/drain in a 40nm FILOX device, the junction can be extended further away from the FILOX encroachment around the corner region at the pillar bottom and therefore the series resistance is reduced compared to a 10s RTA. Despite thicker FILOX brings advantages in reducing the drain/source-gate overlap capacitances, the drain and source resistance increases from 581 Ω·μm and 479 Ω·μm for 40nm FILOX to 1510 Ω·μm and 4650 Ω·μm for 60nm FILOX. With a bias condition of $V_{GS}=V_{DS}=1.0$ V, an optimal $f_T$ of 14.8 GHz was seen for a FILOX thickness of 40nm which represented a trade-off between the dominance of series resistance limited $I_{on}$ and the overlap capacitance.

The devices in the third batch are VMOSFET-FILOX structures which include a frame gate contact intended to decrease the gate series resistance and also protect the sidewalls from poly-Si gate etching induced damage. The simulations calibrated against the fabrication process, show that for a VMOSFET with FILOX=40nm, the $f_T$ at $V_{GS}=V_{DS}=1.5$ V is 24GHz while for a VMOSFET with FILOX=60nm, the $f_T$ at $V_{GS}=V_{DS}=1.5$V is 30.5GHz which is a similar value to $f_T$ for the advanced lateral MOSFETs at the 0.35μm technology node according to ITRS road map. Further ideal device simulation with 40nm

FILOX suggests that with the junction abruptness improved from the original 10dec/nm to the ITRS requested 2.7dec/nm [9] for a 50nm channel length, the peak $f_T$ within gate bias of 1.5V can reach as high as 99.4GHz. This corresponds to an almost three-generation-hop in RF performance that can be ultimately achieved with VMOSFETs using a 0.35μm lithography stepper compared to an advanced Si-MOSFET at the same lithography technology node if the junction abruptness can be reduced to 2.7dec/um. However, the highest $f_T$ obtained from the measurement for the 100nm fabricated DGC device was 8.6 GHz, for a double gate device with a channel length of 150nm, a channel width of 24um and FILOX thickness of 40nm with $V_{DS}$=1.5V and $V_{GS}$=1.1V with an drive current of 58.65 μA/μm. By comparing the characterised on-current to the previous simulation result, the difference suggests that there exists an additional series resistance of 10 kΩ·um which is most-likely attributed to the drain/source contact interface resistances. Compared to the junction resistances presented in Chapter 6, the contact resistance is about 10 times higher. This is to say that the low $f_T$ in this batch of devices is largely due to limitation from the poor contact resistance. The calibrated simulation provides values for the combination of gate bias dependent transconductance and gate overlap capacitance, which determines the maximum $f_T$ and its corresponding $V_{GS}$. The 3D device simulations have confirmed that double gate devices could provide a higher $f_T$ than the frame gate contact structure due to lower overlap capacitance caused by a smaller gate overlap area. The $f_T$ might also be lowered by the higher junction sheet resistance in 100nm channel length devices than in 150nm channel length devices due to process variation at the implantation stage. Both the measured and simulated on-currents suggested that 40nm FILOX devices have a significant advantage in providing a higher $f_T$ over the 60nm FILOX. The reason is believed to be related to the impact of FILOX thickness on the series resistance as discussed in Chapter 6. Well-meshed 3D simulations have further provided results

indicating that the corners at each sidewall edge bring little impact on wide devices though higher conduction current density is evident in the corner regions.

In this work a compact model covering both DC and AC characteristics of the device is constructed based on EKV modelling approach. The DC part of the compact model of the double gate contact VMOSFET-FILOX with 40nm thick FILOX has been successfully constructed using the EKV3 modelling tool kit in the IC-CAP platform. However, the accuracy of the 'long' device model is limited by the high series resistance and short channel effects. A device with channel length of 250nm was used as the best available one but there was evidence of increased current saturation due to short channel and on-current degradation arising from series resistance. Despite of this, good fittings of the $I_DV_G$, $g_m$ and $I_DV_D$ characteristics of the short (100nm) device over a range of bias conditions have confirmed an acceptable accuracy of the compact model of the short channel device. Apart from the series resistance and short channel effect that exist in the 'long device', the inconsistency of series resistance and critical velocity of electrons among the long and short devices potentially adds more uncertainty when attempting to extract a scalable model. The parameters describing the AC characteristics of the model are extracted from the measured CV and S parameter plots. Through the fitting of the measured and simulated S parameters and its corresponded phase and magnitude curves, the junction, overlap capacitance parameters extraction are achieved as well as the further extraction of the gate sheet resistance, gate-to-body overlap capacitance and substrate network parameters. A full model covers both DC and AC performances targeting on the device with a 100nm channel length was constructed. Through the study using the compact model, it was found that the junction and gate overlap capacitances related parameters at drain side have much more significant impact on the above three S parameters than at the

source side. It can be also concluded that a higher drain junction value in VMOSFET induces higher output impedance in the RF range under high gate bias.

## 9.2 Suggestions for Future Work

Through the work carried out in this project, some significant results have been achieved in investigating the strengths and weaknesses of some novel device architectures which were designed to enhance vertical MOSFET technology. The fabricated devices have provided evidence that some of the design targets have been successfully realized. However, there were some design and modelling goals not yet realized in the current batches. In the next batches, there are some further improvements that can be done over the existing designs for a better suitability as RF components. Some suggestions for future device fabrication and compact modelling are:

(A) A further batch of retrograde body devices, both short and long channel length. This would assure a comparison between the experimental data and the analytical and numerical designs to see if on-current enhancement can be achieved without sacrificing excessively the suppression on the off-current.

(B) To optimise the on-current by reducing the series resistance in the devices with FILOX=60nm with a RTA time of 40s or 15$^{o}$ tilt angle implantation. The role of $R_{acc1}$ in series resistance can be experimentally identified by comparing devices with and without these optimisation steps.

(C) To optimise the cut-off frequency $f_T$ value which theoretically can reach a maximum value of 29GHz for a 100nm device with 60nm thick FILOX. Double gate contact

should be used instead of frame gate contact devices for overlap capacitance reduction. Also very importantly, a silicidation process should also be applied to the drain/source contact interface in order to achieve the ohmic contact resistance optimisation. Moreover 50nm channel length should be fabricated to boost $f_T$ further to a value of 25 GHz for an unsilicided device. With a silicidation process, a 50nm device with 60nm FILOX and without FILOX encroachment problem may exhibits a maximum $f_T$ up to about 60GHz presumably. Meanwhile, the poly-Si gate etch process step needs to be optimised to avoid damage which results in the creation of interface states in the channel. A maximum oscillation frequency, $f_{max}$ extraction would allow an experimental evaluation of the impact of gate types on the device power gain performance at RF range.

(D) To further verify the values of series resistance in a VMOSFET, experimental work should be carried out on fabricated devices using the RF-impedance method in the lab

(E) To achieve an accurate and scalable EKV model. 'Long' devices should have a channel length up to 280nm to 300nm with a body boron doping pushed up to suppress SCEs. Devices with a 50nm channel length are then needed as the 'short' devices for extraction of the short channel related phenomena related parameters.

(F) Improvements in the process are required to maintain uniformity of sheet resistance in junctions across the wafers and precise control of pillar height to avoid channel length variation. To allow realisation of a scalable EKV model, devices with at least 4 different channel lengths with much tighter process variation are required.

(G) The feasibility of using EKV3.0 on modelling devices with asymmetrical junctions and non-uniform body doping needs to be reassessed. This is because the derivation of the EKV model assumes symmetrical junctions which have equal electrical influence on the channel charge control, which is not the case in these vertical structures.

As an extension to the retrograde body design, an ultra thin body vertical MOSFET is proposed which is compatible with the FILOX process. A simple process flow is shown in Fig 8.1. In (a), the oxide bulk grown on the P type substrate is etched to form the insulator body. In (b), the ultra thin undoped amorphous Si body is deposited by LPCVD on an oxide region. It is followed by a low temperature annealing carried out for crystallization in the thin body layer while a high dose Si implantation is used to break up the native oxide at the interfaces. In (c), a thick amorphous silicon layer (150nm) was deposited to form the region reserved for the top junction. In (e) - (f), the process follows standard nitride fillet formation and FILOX growth routine. The drain and source are be formed by arsenic implantation in (g) followed by gate oxide growth, poly-Si gate deposition and etching and metal contact deposition. The net doping contour of the final device simulation after the rapid thermal annealing is shown in (h).

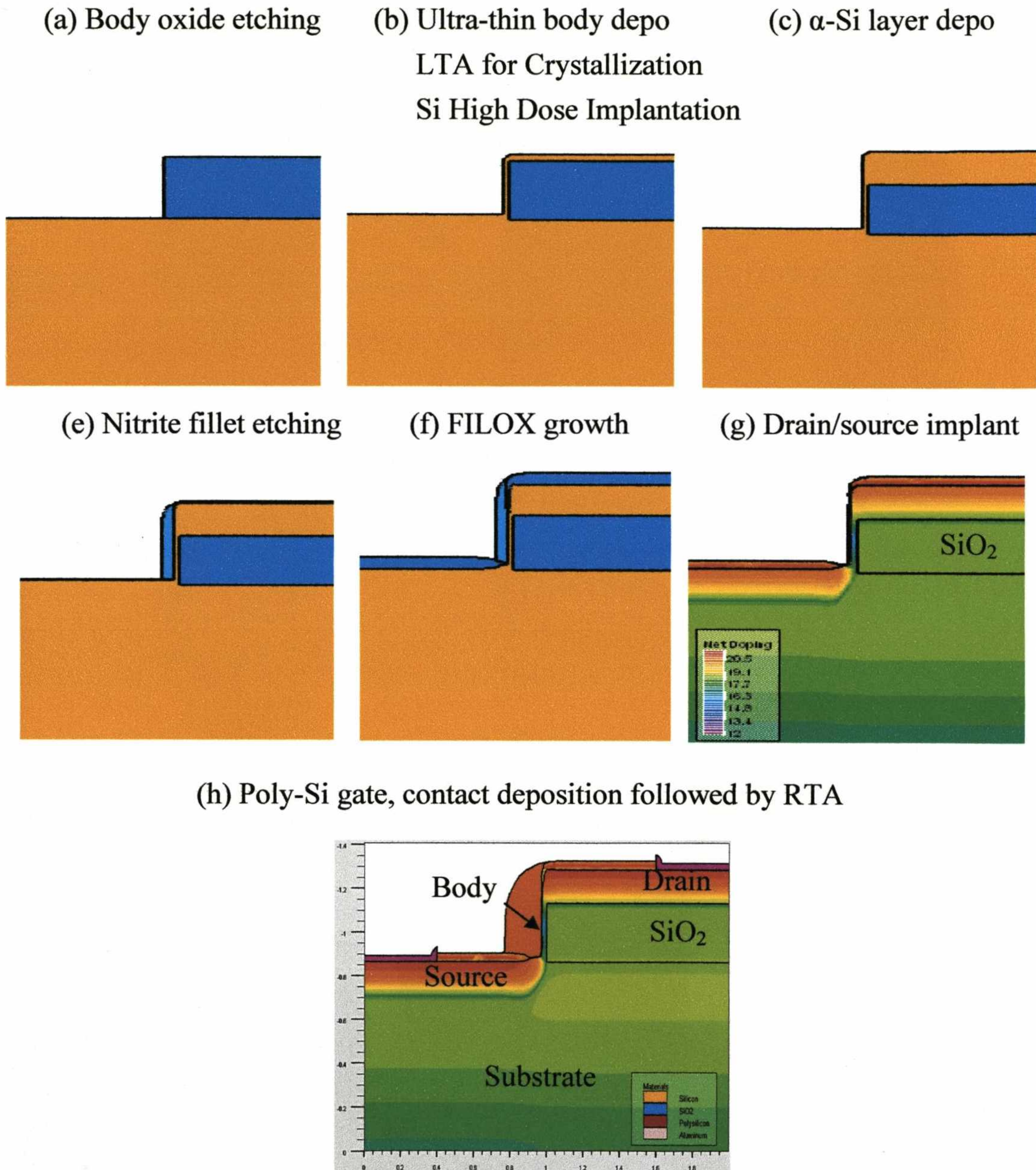



Fig 9.1 A brief process flow for fabrication of a ultra-thin body VMOSFET structure.

Table 9.1 Performance comparison among the simulated UTVMOSFET and fabricated VMOSFETs with single gate and double gate contacts.

| | $V_T$ (V) | $I_{on}$ (uA/um) | $I_{off}$ (nA/um) | DIBL ( mV) | Ss (mV/dev @$V_{DS}$=1V) |
|---|---|---|---|---|---|
| UTVMOSFET | 0.42 | 175 | 1.39 | 0 | 90 |
| VMOSFET (SG) | 0.3 | 71.9 | 56.8 | 200 | 180 |
| VMOSFET (FG) | 0.35 | 159 | 0.137 | 35 | 80 |

*Note that Gate oxide thickness is 3.2 nm with a channel length of 230nm.

From the performance comparison in table 9.1, the UTVMOSFET has excellent immunity to SCEs similar to that of VMOSFETs with FG and significantly better than VMOSFETs with single gate contact. It also has significantly the best on-current among the three devices, due to the low-doped channel region with a reasonable level of off current. Furthermore, by reducing the channel layer thickness/depletion region width further, the SCE immunity and off-current in the UTVMOSFET can be further improved.

# Reference List


[1] D. Wang, 'Enabling Technologies and Circuit Design for RF/AMS IC and ASIC', Tutorial,
International Conference on Solid-State and Integrated-Circuit Technology, Oct, 2006.

[2] B. J. Baliga, 'Silicon RF Power MOSFETs', World Scientific Publishing Co. Pte. Ltd, 2005

[3] F. Schwierz, J.J. Liou, 'RF transistors: Recent developments and roadmap toward terahertz applications', Solid-State Electronics, Vol. 51, Issue 8, pp.1079-1091, Aug 2007.

[4] T. S. Low, T. S. Shirley, C. P. Hutchinson, G. K. Essilfie, W. C.Whiteley, R. E. Yeats, and D.C. D'Avanzo, 'InGaP HBT Technology for RF and Microwave Instrumentation,' Solid State Electron., Vol. 43, Issue 8, pp. 1437–1444, Aug. 1999.

[5] K.J. Kuhn, S. Ahmed, P. Vandervoorn, A. Murthy, B. Obradovic, K. Raol, W. Shih, I. Chao, I. Post, S.Chambers, 'Integration of Mixed-Signal Elements into a High-Performance Digital CMOS Process', Intel Technology Journal, Vol. 06, Issue 2, pp.31-41, May, 2002.

[6] G. Niu, 'SiGe Technology for Revolution of Personal Communications', online resources: http://www.eng.auburn.edu/users/niuguof/sige_intro.htm.

[7] R.B. Staszewski, R. Staszewski, J.L. Wallberg, T. Jung, C.-M. Hung, J. Koh, D. Leipold, K. Maggio, P.T. Balsara, 'SoC with an integrated DSP and a 2.4-GHz RFtransmitter', IEEE Trans. on VLSI Systems, Vol. 13, Issue. 11, pp. 1253-1265, November, 2005.

[8] H.J. Sigg, G.D. Vendelin, T.P. Cauge, J. Kocsis, 'D-MOS transistor for microwave applications', IEEE Trans. on Electron Devices, Vol. 19, Issue. 1, pp. 45-53, 1972.

[9] A.O. Adan, T. Yoshimatsu, S. Shitara, N. Tanba, and M. Fukumi, 'Linearity and low-noise performance of SOI MOSFETs for RF applications', IEEE Trans. Electron Devices, Vol. 49, Issue 5, pp.881–888, May 2002.

[10] International Technology Roadmap for Semiconductors (ITRS) - Process Integration, Devices and Structures. http://public.itrs.net, 2005.

[11] Mark, 'Intel Tukwila 2 billion transistor chip is world's first: 2GHz Itanium process', Product Reviews, www.product-reviews.net, Feb, 2008.

[12] P.M. Solomon, K.W. Guarini, and Y. Zhang et al. 'Two gates are better than one', IEEE Circuits and Devices Magazine, Vol. 19, Issue 1, pp.48-62, Jan. 2003.

[13] V.W. C. Chan and P.C. H. Chan. 'Fabrication of gate-all-around transistors using metal induced lateral crystallization', IEEE Electron Device Lett., Vol. 22, Issue 2, pp.80-82, 2001.

[14] M. Lemme, T. Mollenhauer, W. Henschel, T. Wahlbrink, and H. Kurz. Nanoscale, 'SOI-MOSFETs with non-planar multiple gates', International Conference on Ultimate Integration of Silicon, pp.15-18, 2003.

[15] T. Schulz, W. Rösner, L. Risch, T. Aeugle, U. Langmann, and A. Korbel, '130 nm vertical PMOS transistors with p poly-gate', in Proc. ESSDERC'98, pp. 168–171, 1998.

[16] J. Moers, A. Tönnesmann, D. Klaes, L. Vescan, A. van der Hart, A. Fox, M. Marso, P. Kordo˘s, H. Lüth, 'Vertical Silicon MOSFETs based on Selective Epitaxial Growth', Proc. of the ASDAM 2000, pp. 67–70, 2000.

[17] C. Fink, J. Schulze, I. Eisele, W. Hansch, W. Werner and W. Kanert, 'Reducing of Ron in Vertical Power-MOSFETs due to Local Channel Doping', Jpn.J.App.Phys, Vol. 40, Issue 4, pp.2637-2641, 2001.

[18] H. Gossner, I. Eisele and L. Risch, 'Vertical Si-Metal-Oxide-Semiconductor Field Effect Transistors with Channel Length of 50nm by Molecular Beam Epitaxy', Jpn. J. Appl. Phys. Vol. 33, Issue 4B, pp.2423-2428, 1994.

[19] D. Klaes, J. Moers, A. Tonnesmann, M. Grimm, S. Wickenhauser, L. Vescan, M. Marso, P. Kordos, H. Luth, T. Grabolla, 'Selectively Grown Vertical Si p-MOS Transistor with Reduced Overlap Capacitances', Thin Solid Films, Vol. 336, Issue 1 – 2, pp.306 – 308, 1998.

[20] C. K. Date and J. D. Plummer, 'Suppression of the floating-body effect using SiGe layers in vertical surrounding-gate MOSFETs', IEEE Trans. Electron Devices, Vol. 48, Issue 12, pp. 2684–2689, 2001.

[21] M. Yang, C.-L. Chang, M. Carroll, and J. C. Sturm, '25-nm p-channel vertical MOSFETs with SiGeC source-drains', IEEE Electron Device Lett., Vol. 20, Issue 6, pp.301–303, June 1999.

[22] J. M. Hergenrother, S.-H. Oh, T. Nigam, D. Monroe, F. P. Klemens, and A. Kornblit, 'The vertical replacement-gate (VRG) MOSFET', Solid State Electron., Vol. 46, Issue 7, pp. 939–950, Jul. 2002.

[23] K. Mori, A. Duong, W.F. Richardson, 'Sub-100-nm Vertical MOSFET with Threshold Voltage Adjustment', IEEE Trans. Electron Devices, V.49, Issue 1, pp.61-66, Jan. 2002.

[24] H. Takato, K. Sunouchi, N. Okabe, A. Nitayama, K. Hieda, F. Horiguchi, and F. Masuoka. 'Impact of surrounding gate transistor (sgt) for ultra-high-density lsi's', IEEE Trans. Electron Devices, Vol.38, Issue 3, page. 573-578, March 1991.

[25] T. Schulz, W. Rosner, L. Risch, A. Korbel, and U. Langmann, 'Short-channel vertical sidewall MOSFETs', IEEE Trans. Electron Devices, Vol. 48, Issue 8, pp. 1783–1788, Aug. 2001.

[26] J. Moers, S. Trellenkamp, M. Goryll, S. Hogg, P. Kluth, and Q.-T. Zhao. 'Vertical P Channel with Double-gate MOSFETs', International Conference on Ultimate Integration of Silicon, pages 135-138, 2003.

[27] M. Masahara, Y. Liu, S. Hosokawa, T. Matsukawa, K. Ishii, H. Tanoue, K. Sakamoto, T. Sekigawa, H. Yamauchi, S. Kanemaru, and E. Suzuki. 'Ultra-thin channel vertical dg mosfet fabricated by using ion-bombardment-retarded etching', IEEE Trans. Electron Devices, Vol. 51, Issue 12, Dec, 2004.

[28] K. C. Liu, S. K. Ray, S. K. Oswal, and S. K Banerjee, 'A deep submicron Si Ge /Si vertical PMOSFET fabrcated by Ge ion implantation', IEEE Electron Device Lett., Vol. 19, No. 1, pp. 13–15, Jan. 1998.

[29] Z. Y. Wu, S. Hall and W. Eccleston, 'Suppression of the parasitic bipolar transistor in deep sub-micron MOSFETs by the use of a narrow band-gap source', Proc. of ESSDERC '95, pp.509-512, Frontieres, 1995.

[30] C. K. Date, J. D. Plummer, 'Suppression of the Floating-Body Effect Using SiGe Layers in Vertical Surrounding-Gate MOSFETs', IEEE Transactions on Electron Devices, Vol. 48, Issue 12, pp. 2684-2689, Dec. 2001.

[31] B. Goebel, D. Schumann, and E. Bertagnolli, 'Vertical n-channel MOSFETs for extremely high density memories: the impact of interface orientation on device performance', IEEE Trans. Electron Devices, Vol. 48, Issue 5, pp.897-906, May 2001.

[32] M. Jurczak, E. Josse, R. Gwoziecki, M. Paoli, T. Skotnicki, 'Investigation on the Suitability of Vertical MOSFET's for High Speed (RF) CMOS Applications', Proc. ESSDERC'98, pp. 172–175. 1998.

[33] X. Chen, Q.C. Ouyang, G. wang, S.K. Banerjee, 'Improved Hot-Carrier and Short-Channel Performance with Vertical nMOSFETs with Graded Channel Doping', IEEE Trans. Electron Devices, V.49, Issue 11, pp.1962-1967 , Nov. 2002.

[34] V.D. Kunz, T.Uchino, C.H. Groot, P. Ashburn, D.C. Donaghy, E. Gili, S. Hall, Y. Wang, P. L. F. Hemment, 'Reduction of parasitic capacitance in vertical MOSFET's by fillet local oxidation (FILOX)', IEEE Trans. Electron Devices, Vol. 50, Issue 6, pp. 1480-1487, Jun. 2003.

[35] H. Liu, Z. Xiong, J. K.O. Sin, 'An Ultrathin Vertical Channel MOSFET for Sub-100-nm Applications', IEEE Trans Electron Devices, Vol 50, Issue 5, pp.106-112, May 2003.

[36] V.D. Kunz. 'CMOS compatible vertical surround gate MOSFETs with reduced parasitic', PhD thesis, University of Southampton, June 2003.

[37] V.D. Kunz, C.H. de Groot, E. Gili, T. Uchino, S. Hall, and P. Ashburn. 'CMOS-compatible vertical MOSFETs and logic gates with reduced parasitic capacitance', Proc. of ESSDERC'2004, pages 221-224, September 2004.

[38] S. Hall, D. Donaghy, O. Buiu, E. Gili, T. Uchino, V.D. Kunz, C.H. de Groot, and P. Ashburn. 'Recent developments in deca-nanometer vertical MOSFETs.' Microelectronic Engineering, Vol.72, page.230-235, 2004.

[39] D.C. Donaghy, S. Hall, C.H. Groot, V.D. Kunz, P. Ashburn, 'Design of a 50nm vertical MOSFET incorporating a dielectric pocket', IEEE Trans. Electron Devices, Vol. 51, Issue 1, pp. 158-161, Jan. 2004.

[40] E. Gili, T. Uchino, M. M. A. Hakim, C. H. de Groot, O. Buiu, S. Hall, and P.Ashburn. 'Shallow junctions on pillar sidewalls for sub-100-nm vertical MOSFETs'. IEEE Electron Device Lett., Vol. 27, Issue 8, page.692-695, August 2006.

[41] E. Gili, T. Uchino, M. M. A. Hakim, C. H. De Groot, P. Ashburn, and S. Hall. 'A new approach to the fabrication of CMOS compatible vertical mosfets incorporating a dielectric pocket', International Conference on Ultimate Integration of Silicon, pages 127-130, April, 2005.

[42] L.Tan, First Project Group Meeting, May, 2007.

[43] M. Jurczak, T. Skotnicki, R. Gwoziecki, M. Paoli, B. Tormen, P. Ribot, D. Dutartre, S. Monfray, and J. Galvier. 'Dielectric pockets - a new concept of the junctions for deca-nanometric cmos devices', IEEE Trans. Electron Devices, Vol. 48, Issue 8, pp.1770-1775, Aug, 2001.

[44] T.Uchino, E. Gili, M. M. A. Hakim, V. D. Kunz, C. H. de Groot, P. Ashburn, L. Tan, S. Hall, 'Improved Vertical pMOSFET Performance Using a Dielectric Pocket and an Epitaxial Channel', submitted to ESSDERC 2007, April, 2007.

[45] Y. Taur, T.H. Ning. 'Fundamentals of Modern VLSI Devices', Cambridge University Press, Cambridge, 1998.

[46] T.N. Nguyen, 'Small-geometry MOS transistors: Physics and modelling of surface- and buried-channel MOSFETs', Ph.D. dissertation, Standford University, CA, 1984.

[47] Y. Tsividis. 'Operation and Modelling of the MOS Transistor', McGraw-Hill, Inc., 2nd edition, 1999.

[48] R.F. Pierret, 'Semiconductor Device Fundamentals', Addison-Wesley, Reading, MA, 1996.

[49] J. Chen, T. Y. Chan, I. C. Chen, P. K. Ko, and C. Hu. 'Sub-breakdown Drain Leakage Current in MOSFET', IEEE Electron Device Lett., Vol. 8, Issue 11, pp.515-517, November 1987.

[50] J.R. Brews, Chap 3, 'High Speed Semiconductor Devices', ed. S.M. Sze, John Wiley & Sons, New York, 1990.

[51] L. Risch, R. Maly, W. Berger, and R. Kirchen, 'Charge losses of n-doped trench cells,' in Proc. Of Solid State Devices Mater., pp. 585–588, 1988.

[52] Dieter K. Schroder, 'Semiconductor Material and Device Characterisation', second edition, John Wiley & Sons, Inc, New York, 1998.

[53] Z.A. Weinberg, 'Tunnelling of electrons from Si into thermally grown SiO2', Solid-state Electronics, Vol.20, Issue 1, pp.11-18, 1977.

[54] A. Gehring, 'Simulation of tunnelling in semiconductor devices', PhD dissertation, Technische Universität Wien, Austria, Nov, 2003.

[55] G. Liu, 'Thesis of Fully Integrated CMOS Power Amplifier', Electrical Engineering and Computer Sciences, University of California at Berkeley, 2006.

[56] Burghartz JN, Hargrove M, Webster C, Groves R, Keene M, Jenkins K, 'RF potential of a 0.18-lm CMOS logic technology'. IEEE Trans. Electron Devices, Vol 47, Issue 4, pp.864-70, 2000.

[57] S. P. Voinigescu, S. W. Tarasewicz, T. MacElwee, and J. Ilowski, 'An assessment of the state-of-the-art 0.5 _m bulk CMOS technology for RF applications', IEDM Tech. Dig., pp.721–724, 1995.

[58] S. Eminente, M. Alessandrini, C. Fiegna, 'Comparative analysis of the RF and noise performance of bulk and single-gate ultra-thin SOIMOSFETs by numerical simulation. ' Solid-State Electron, Vol. 48, Issue 4, pp.543-549, 2004.

[59] H. Beneking, 'High Speed Semiconductor Devices – Circuit aspects and fundamental Behaviour', Chapman and Hall, 1994

[60] F. Schwierz, 'Wide Bandgap and Other Non-III-V RF Transistors: Trends and Prospects', ASU Tempe, March 2004.

[61] M. Chan, K. Hui, R. Neff, C. Hu, P. Ko, 'A Relaxation Time Approach to Model the Non-Quasi-Static Transient Effects in MOSFETs', Tech. Dig. Of IEDM. pp. 169-172, 1994.

[62] Y. Cheng, M.J. Deen, C.H Chen, 'MOSFET Modelling for RF IC Design', IEEE Transactions on Electron Devices, Vol. 52, issue 7, pp. 1286-1303, 2005.

[63] T. Skotnicki, MASTAR, Available: http://www.itrs.net/models.html.

[64] L. F. Register, E. Rosenbaum, and K. Yang, 'Analytic model for direct tunnelling current in polycrystalline silicon-gate metal-oxidesemiconductor devices,' Appl. Phys. Lett., vol. 74, p. 457, Jan. 1999.

[65] Enrico Gili, Private communication, March, 2006.

[66] E. Gili, V. D. Kunz, T. Uchino, M. M. Al Hakim, C. H. de Groot, P. Ashburn, and S. Hall. 'Asymmetric gate induced drain leakage and body leakage in vertical mosfets with reduced parasitic capacitance', IEEE Trans. Electron Devices, Vol. 53, Issue 5, pp.1080-1087, May 2006.

[67] K.-F. You and C.-Y. Wu. 'A new quasi-2-d model for hot-carrier band-to-band tunnelling current', IEEE Trans. Electron Devices, Vol. 46, Issue 6, pp.1174-1179, June 1999.

[68] S.K. Jayanarayanan, S. Dey, J.P. Donnelly and S.K. Banerjee, 'A novel vertical MOSFET with a dielectric pocket', Solid-State Electronics, Vol. 50, Issue 5, pp.897-900, May. 2006.

[69] T. Schulz, W. Rosner, R. Lothar, 'Short-channel vertical sidewall MOSFETs', IEEE Trans. Electron Devices, Vol. 48, Issue 8, pp.1783-1788, Aug. 2001.

[70] C.M. Osburn, I. De, K. F. Yee, A. Srivastava, 'Design and integration considerations for end-of-the roadmap ultrashallow junctions', Journal of Vacuum Science and Technology, Vol. B18, Issue 1, pp. 338-345, Jan/Feb. 2000.

[71] J. M. Hergenrother, S.H. Oh, T. Nigam, D. Monroe, F. P. Klemens, and A. Kornblit. 'The vertical replacement-gate (VRG) MOSFET', Solid-State Electronics, Vol. 46, Issue 12, 939–950, Sep. 2002.

[72] K. Mori, A. Duong, and W. F. Richardson, 'Sub-100-nm Vertical MOSFET with Threshold Voltage Adjustment', IEEE Trans. Electron Devices, Vol. 49, Issue 1, pp. 61-66, Jan. 2002.

[73] A.C. Lamb, L.S. Riley, S. Hall, V.D. Kunz, C.H. de Groot, Peter Ashburn, 'A 50nm channel vertical MOSFET concept incorporating a retrograde channel and a dielectric pocket', Proc. of ESSDERC'2001, pp.347-350, Sep. 2001.

[74] L. D. Yau, 'A simple theory to predict the threshold voltage of short-channel IGFET's ', Solid-State Electronics, Vol. SSE-17, Issue 10, pp. 1059, Oct. 1974.

[75] G. W. Taylor, 'Sub-threshold Conduction in MOSFET's', IEEE Trans. Electron Devices, Vol. 25, Issue 3, pp. 337-350, March 1978.

[76] A. A. Mutlu, R. Mahmud, 'Two-Dimensional Analytical Model for Drain Induced Barrier Lowering (DIBL) in Short Channel MOSFETs', Proc. of IEEE Southeast Conference' 2000. pp.340-344, 2000.

[77] T Skotnicki, MASTAR, Available: http://www.itrs.net/models.html.

[78] S. Sleva, Y. Tuar, 'The Influence of Source and Drain Junction Depth on the Short-Channel Effect in MOSFETs', IEEE Trans. Electron Devices, Vol. 52, Issue 12, pp.2814-2816, Dec. 2005.

[79] R. Gwoziecki, T. Skotnicki, 'Physics of the sub-threshold slope – initial improvement and final degradation in short CMOS devices', Proc. of ESSDERC'2002, pp.639-642, 2002.

[80] Zhi-Hong Liu, Chenming Hu, 'Threshold Voltage Model for Deep-Submicrometer MOSFET's', IEEE Trans. Electron Devices, Vol. 4, no.1, pp.86-96, Jan. 1993.

[81] H.Kurata and T.Sugii, 'Impact of shallow source/drain on the short channel characteristics of pMOSFETs', IEEE Electron Device Lett., Vol. 20, Issue 2, pp.95-96, 1999.

[82] Private communication, P. Ashburn, T. Uchino, University of Southampton, Feb 2007.

[83] H. Lee, J Hwang, Y.J. Park, H.S. Min, 'A leakage current mechanism caused by the interaction of residual oxidation stress and high-energy ion implantation impact in advanced CMOS technology', IEEE Electron Device Letters, Vol. 20, Issue 5, May 1999.

[84] G.B. Choi, S.H. Hong, S.W. Jung, H.S. Kang, Y.H. Jeong, 'RF Capacitance Extraction Utilizing a Series Resistance Deembedding Scheme for Ultra leaky MOS Devices ', IEEE Electron Device Lett., Vol. 29, Issue 3, pp.238-241, 2008.

[85] S Zafa, C Cabral, Jr. R.Amos and A.Callegari, 'A method of measuring barrier heights, metal work functions and fixed charge densities in metal/SiO2/Si capacitor', Applied Physics Letters, Vol.80, Issue 25, June 2002.

[86] S.T. Ma, J.R. Brews, 'Comparison of Deep-Submicrometer Conventional and Retrograde n-MOSFET's', IEEE Trans. Electron Dev., Vol. 47, Issue 8, pp. 1573-1579, August 2000,.

[87] I. De and C. M. Osburn, 'Impact of Super-Steep-Retrograde body Doping Profiles on the Performance of Scaled Devices', IEEE Trans. Electron Dev., Issue 8, pp. 1711-1717 August 1999.

[88] G. Guegan, D. Souil, S. Deleonibus, S. Tedesco, C. Laviron, P. Previtali, M.E. Nier, 'Channel Engineering for 50 nm P-Channel MOSFET', Proceeding of the 32nd Solid-State Device Research Conference (ESSDERC'2002), Vol. 46, Issue 8, pp. 119-122, 2002.

[89] H.C. Wann, C. Hu, K. Noda, D. Sinitsky, F.Assaderaghi and J. Bokor, 'Channel Doping Engineering of MOSFET with Adaptable Threshold Voltage Using Body Effect for Low Voltage and Low Power Applications', Proceedings of Technical Papers, International Symposium on VLSI Technology, System, and Applications, pp.159-163, May-Jun, 1995.

[90] K.T. Nishinohara, Y.Akasaka, T.Saito, A. Yagishita, A. Murakoshi, K. Suguro, T. Arikado, 'Surface Channel Metal Gate Complementary MOS with Light Counter Doping and Single Work Function Gate Electrode', Jpn J. Appl.Phys. Vol.40, Issue 4, pp. 2603-2606, 2001.

[91] K. Noda, T. Uchida, T. Tatsnmi, T. Aoyama, K. Nakajima, H. Miyamoto, T. Hashimoto, and I. Sasaki, ''0.1μm Delta- Doped MOSFET Using Post Low-Energy Implanting Selective Epitaxy,' 1994 Symposium on VLSI Technology Digest of Technical Papers, pp.19, 1994.

[92] S.Venkatesan, J.W. Lutze, C. Lage, W.J. Taylor, 'Device drive current degradation observed with retrograde body profiles', Proc. IEDM 1995, pp. 419-422. 1995

[93] M.M.A. Hakim, P. Ashburn, Internal Report, 'Mask design for 1st batch of VMOSFET-FILOX.' , University of Southampton, Aug., 2007

[94] M.M.A. Hakim, L. Tan, T. Uchino, O. Buiu, W. Redman-White, S. Hall and P. Ashburn, 'Improved sub-threshold slope in RF vertical MOSFETs using a frame gate architecture.' Proceedings of ESSDERC 2008, Aug. 2008

[95] W. Davey, L. Tan, Ellipsometry measurements of FILOX and Gate oxide test wafers, Internal report, 3rd EPSRC project meeting, Aug., 2008

[96] G.J. Hu, C. Chang, Y Chia, 'Gate-Voltage-Dependent Effective Channel Length and Series Resistance of LDD MOSFET's', IEEE Trans. on Electron Devices, Vol. 34, Issue 12, p.2469-2475, 1987.

[97] J.F. Chen, J. Tao, P. Fang, C. Hu, 'Performance and reliability comparison between asymmetric and symmetric LDD devices and logic gates', IEEE J Solid-State Circuits; Vol. 34, Issue 3, pp.367-71 1999.

[98] E.Gondro, F.Schuler, P.Klein, 'A Physics Based Resistance Model of the Overlap Regions in LDD-MOSFETs', International Conference on Simulation of Semiconductor Devices and Processes (SISPAD'1998), pp.267-270, 1998.

[99] S.D. Kim, C.M. Park, Jason C.S. Woo, 'Advanced Model and Analysis of Series Resistance for CMOS Scaling Into Nanometer Regime – Part I: Theoretical Derivation', IEEE Trans. on Electron Devices, Vol. 49, Issue 3 pp.457-466, March 2002.

[100] L. Tan, 'Derivation the Analytical Expression of Gate Depletion Region by Poisson Equation and Guass Law', PhD status report, April, 2005.

[101] S.A. Schwarz, S.E. Russek, 'Semi-Empirical Equations for Electron Velocity in Silicon: Part II-MOS Inversion Layer', IEEE Transc on Electron Devices, Vol. 30, Issue 12 Dec. 1983.

[102] H. Murrmann and Dietrich Widmann, 'Current Crowding on Metal Contacts to Planar Devices', IEEE Trans. on Electron Devices, Vol.ED-16, Issue12, Dec. 1969.

[103] S. Biesemans, M. Hendriks, S. Kubicek, and K.D. Meyer, 'Practical Accuracy Analysis of Some Existing Effective Channel Length and Series Resistance Extraction Methods for MOSFET's', IEEE Trans. on Electron Devices, Vol. 45, Issue 6, pp.1310-1316, June 1998.

[104] C. Lou, W. Chim, D. Chan, Y. Pan, 'A Novel Single-Device DC Method for Extraction of the Effective Mobility and Source-Drain Resistances of Fresh and Hot-Carrier Degraded Drain-Engineered MOSFET's', IEEE Trans. on Electron Devices, pp 1317-1323, Vol. 45, Issue 6, June 1998.

[105] D.M. Kim, H.C. Kim, H.T. Kim, 'Modelling and extraction of gate bias-dependent parasitic source and drain resistances in MOSFETs', Solid State Electronics, Vol. 47, Issue 6, pp 1707-1712, 2003.

[106] E. Torres-Rios, R. Torres-Torres, G. Valdovinos-Fierro, E.A. Gutiérrez-D, 'A Method to Determine the Gate Bias-Dependent and Gate Bias-Independent Components of MOSFET Series Resistance From S-Parameters', IEEE Trans. on Electron Devices, Vol. 53, Issue 3, pp.571-573, March 2006.

[107] A. Bracale, D. Pasquet, J.L. Gautier, V. Feriet, N. Fel, J.L. Pelloie, 'Small Signal Parameters Extraction for Silicon MOS Transistors', 30th European Microwave Conference, pp 1-4, Oct. 2000.

[108] M.M. Hakim, P Ashburn, 2cd Batch Process List # 8, Private Communication, 2007.

[109] M.M.A Hakim, Private Communication at 2rd EPSRC project meeting, Feb, 2008.
[110] M.M.A Hakim, Private Communication at 3rd EPSRC project meeting, August, 2008.
[111] J.J. Liou, F. Schwierz, "RF MOSFET: recent advances and future trends", Electron devices and solid-state circuits, pp.185-192, Dec, 2003.
[112] M.Y. Kwong, K. Reza, P. Griffin, J.D. Plummer, R.W. Dutton, "Impact of lateral source/drain abruptness on device performance", IEEE Trans. on Electron Devices, Vol. 49, Issue 11, pp. 1882-1890, Nov. 2002.
[113] S. B. Felch, D. F. Downey, E. A. Arevalo, S. Talwar, C. Gelatos, and Y. Wang, "Sub-melt laser annealing followed by low-temperature RTP for minimized diffusion," in Conf. Ion Implantation Technology, Sept.2000, pp. 167–170.
[114] C.C. Enz, E.A. Vittoz, 'Charge-based MOS Transistor Modelling – The EKV model for low-power and RF IC Design', John Wiley & Sons LtD, Published in 2006.
[115] S.C. Terry, J.M. Rochello, D.M. Binkley, B.J. Blalock, D.P. Foty, M.Bucher, 'Comparison of a BSIM3V3 and EKV MOST Model for a 0.5 um CMOS Process and Implications for Analog Circuit Design', Nuclear Science Symposium Conference Record, Vol.1, page 317-321, Nov, 2002.
[116] M. Bucher, A. Bazigos, F. Krummenacher, J.M. Sallese, C. Enz, 'EKV 3.0: An Advanced Charge Based MOS Transistor Model', Chapter 3, A Design-oriented MOS Transistor Compact Model for Next Generation CMOS, Springer Netherlands, pp.67-69, 2006.
[117] S. Yoshitomi, A. Bazigos, M. Bucher, 'EKV3 Parameter Extraction and Characterization of 90nm RF-CMOS Technology' 14th Int.Conf. on Mixed Design, (MIXDES 2007), Ciechocinek, June 2007.
[118] Team of EKV Compact MOSFET Model, 'The EPFL-EKV MOSFET Model Equations for Simulation', Downloadable at http://legwww.epfl.ch/ekv/.

# Appendix A

## Atlas device simulation of VMOSFET-JS with 50nm Xj.

```
go devEdit
work.area x1=0 y1=-0.17 x2=0.976 y2=0.4
region reg=1 name=substrate mat=Silicon color=0xffcb00 pattern=0x4 \
    polygon="0.593,-0.081 0.607,-0.08 0.613,-0.078 0.613,-0.078 0.613,-0.01 0.613,-0.01 0.609,-0.008 0.593,-0.007 0.593,-0.005 0.593,0.005 "\
    "0.593,0.075 0.976,0.075 0.976,0.4 0,0.4 0,0.075 0.383,0.075 0.383,0.005 0.372,0.002 0.371,0 0.371,-0.001 "\
    "0.365,-0.01 0.363,-0.01 0.363,-0.078 0.363,-0.078 0.363,-0.079 0.369,-0.084 0.37,-0.088 0.37,-0.093 0.593,-0.093 0.593,-0.084"
impurity id=1 region.id=1 imp=Boron \
    peak.value=3.0e+18 ref.value=1000000000000 comb.func=Multiply
constr.mesh region=1 default
region reg=2 mat=SiO~2 \
    polygon="0.359,-0.156 0.41,-0.156 0.45,-0.156 0.45,-0.153 0.363,-0.153 0.363,-0.093 0.363,-0.078 0.363,-0.01 0.363,0.003 0.12,0.003 "\
    "0.12,0 0.15,0 0.36,0 0.36,-0.093 0.359,-0.093"
constr.mesh region=2 default
region reg=3 mat=SiO~2 \
    polygon="0.856,0 0.856,0.003 0.613,0.003 0.613,-0.01 0.613,-0.078 0.613,-0.093 0.613,-0.153 0.526,-0.153 0.526,-0.156 0.617,-0.156 "\
    "0.617,-0.093 0.616,-0.093 0.616,0 0.85,0"
constr.mesh region=3 default
region reg=4 name=gate mat=Polysilicon elec.id=1 color=0xffff00 pattern=0x5 \
    polygon="0.36,0 0.15,0 0.15,-0.015 0.26,-0.015 0.26,-0.17 0.41,-0.17 0.41,-0.156 0.359,-0.156 0.359,-0.093 0.36,-0.093"
impurity id=2 region.id=4 imp=Phosphorus \
    peak.value=5e+21 ref.value=1000000000000 comb.func=Multiply
constr.mesh region=4 default
region reg=5 name=gate mat=Polysilicon elec.id=1 color=0xffff00 pattern=0x5 \
    polygon="0.616,0 0.616,-0.093 0.617,-0.093 0.617,-0.156 0.621,-0.156 0.625,-0.155 0.715,-0.155 0.715,-0.025 0.85,-0.025 0.85,0"
impurity id=2 region.id=5 imp=Phosphorus \
    peak.value=5e+21 ref.value=1000000000000 comb.func=Multiply
constr.mesh region=5 default
region reg=6 name=source mat=Aluminum elec.id=2 \
    polygon="0.976,0 0.976,0.003 0.856,0.003 0.856,0"
constr.mesh region=6 default
region reg=7 name=source mat=Aluminum elec.id=2 \
    polygon="0.12,0 0.12,0.003 0,0.003 0,0"
constr.mesh region=7 default
region reg=8 name=SiSource mat=Silicon color=0xffcb00 pattern=0x4 \
    polygon="0.391,-0.001 0.391,0 0.392,0.002 0.393,0.005 0.393,0.075 0,0.075 0,0.003 0.12,0.003 0.363,0.003 0.363,-0.01 "\
    "0.383,-0.01 0.385,-0.01"
impurity id=3 region.id=8 imp=Arsenic \
    peak.value=1.4e+20 ref.value=1000000000000 comb.func=Multiply
constr.mesh region=8 default
region reg=9 name=SiSource mat=Silicon color=0xffcb00 pattern=0x4 \
    polygon="0.595,-0.01 0.593,-0.01 0.613,-0.01 0.613,0.003 0.856,0.003 0.976,0.003 0.976,0.075 0.588,0.075 0.588,0.005 0.585,-0.005 "\
    "0.588,-0.007 0.589,-0.008"
impurity id=3 region.id=9 imp=Arsenic \
    peak.value=1.4e+20 ref.value=1000000000000 comb.func=Multiply
constr.mesh region=9 default
region reg=10 name=drain elec.id=3 mat=Polysilicon color=0xffff00 pattern=0x5 \
    polygon="0.593,-0.113 0.383,-0.113 0.383,-0.093 0.363,-0.093 0.363,-0.153 0.45,-0.153 0.526,-0.153 0.613,-0.153 0.613,-0.093 0.593,-0.093"
impurity id=2 region.id=10 imp=Phosphorus \
    peak.value=5e+21 ref.value=1000000000000 comb.func=Multiply
```

```
constr.mesh region=10 default
region reg=11 mat=SiO~2 color=0xff pattern=0x2 \
     polygon="0.383,-0.113 0.593,-0.113 0.593,-0.093 0.588,-0.093 0.39,-0.093 0.383,-0.093"
constr.mesh region=11 default
region reg=12 name=SiDrain mat=Silicon color=0xffcb00 pattern=0x4 \
     polygon="0.392,-0.079 0.382,-0.078 0.363,-0.078 0.363,-0.078 0.363,-0.093 0.411,-0.093 0.413,-0.093 0.413,-0.081 0.398,-0.08
0.395,-0.079"
impurity id=3 region.id=12 imp=Arsenic \
     peak.value=1.4e+20 ref.value=1000000000000 comb.func=Multiply
constr.mesh region=12 default
region reg=13 name=SiDrain mat=Silicon color=0xffcb00 pattern=0x4 \
     polygon="0.597,-0.078 0.565,-0.081 0.565,-0.081 0.563,-0.083 0.563,-0.093 0.613,-0.093 0.613,-0.078 0.599,-0.078"
impurity id=3 region.id=13 imp=Arsenic \
     peak.value=1.4e+20 ref.value=1000000000000 comb.func=Multiply
constr.mesh region=13 default
region reg=14 name=drain mat=Aluminum elec.id=3 \
     polygon="0.45,-0.165 0.526,-0.165 0.526,-0.156 0.526,-0.153 0.45,-0.153 0.45,-0.156"
constr.mesh region=14 default
#region reg=15 name=RetrogradeL mat=Silicon color=0xffcb00 pattern=0x4 \
     #polygon="0.383,-0.01 0.363,-0.01 0.363,-0.078 0.383,-0.078"
#impurity id=1 region.id=15 imp=Boron \
     #peak.value=5e+16 ref.value=1000000000000 comb.func=Multiply
#constr.mesh region=15 default
#region reg=16 name=RetrpgradeL mat=Silicon color=0xffcb00 pattern=0x4 \
    # polygon="0.593,-0.078 0.613,-0.078 0.613,-0.01 0.593,-0.01"
#impurity id=1 region.id=16 imp=Boron \
    #  peak.value=5e+16 ref.value=1000000000000 comb.func=Multiply
#constr.mesh region=16 default
region reg=17 name=base mat=Aluminum elec.id=4 \
          polygon="0.0,0.4 0.0,0.41 0.976,0.41 0.976,0.40 0.0,0.4"
constr.mesh region=17 default
base.mesh height=10 width=10
bound.cond !apply max.slope=28 max.ratio=300 rnd.unit=0.001 line.straightening=1 align.points when=automatic
imp.refine min.spacing=0.02
constr.mesh max.angle=90 max.ratio=300 max.height=10000 \
     max.width=10000 min.height=0.0001 min.width=0.0001
constr.mesh type=Semiconductor default
constr.mesh type=Insulator default
constr.mesh type=Metal default
constr.mesh type=Other default
constr.mesh region=1 default
constr.mesh region=2 default
constr.mesh region=3 default
constr.mesh region=4 default
constr.mesh region=5 default
constr.mesh region=6 default
constr.mesh region=7 default
constr.mesh region=8 default
constr.mesh region=9 default
constr.mesh region=10 default
constr.mesh region=11 default
constr.mesh region=12 default
constr.mesh region=13 default
constr.mesh region=14 default
constr.mesh region=15 default
constr.mesh region=16 default
constr.mesh region=17 default
Mesh Mode=MeshBuild
refine mode=both x1=0.003 y1=-0.1707 x2=0.968 y2=0.3604
```

```
refine mode=both x1=0.3628 y1=-0.0936 x2=0.3857 y2=-0.0096
refine mode=both x1=0.363 y1=-0.093 x2=0.3841 y2=-0.0096
refine mode=both x1=0.36 y1=-0.093 x2=0.38 y2=-0.0096
refine mode=both x1=0.5891 y1=-0.0927 x2=0.6132 y2=-0.0104
refine mode=both x1=0.5886 y1=-0.093 x2=0.6131 y2=-0.0096
refine mode=both x1=0.6 y1=-0.093 x2=0.6131 y2=-0.0096
base.mesh height=10 width=10
bound.cond !apply max.slope=28 max.ratio=300 rnd.unit=0.001 line.straightening=1 align.Points when=automatic
struct outfile=perfect.str
#tonyplot vmos1.str -set vmos1.set
tonyplot perfect.str
############ go to atlas package ############
go atlas
###### set the device contact ######
contact    name=source neutral
contact    name=gate n.polysilicon
contact    name=drain neutral
contact    name=base neutral
###### set material models ######
material taun0=7.3e-7 taup0=7.3e-7 vsaturation=1e7
###### set material models #####
models cvt consrh auger bgn fermi print ksp=0 ksn=0 numcarr=2 hhi nearflg ioniz bb.a=1.000e11 bb.b=1.9e07 bb.gamma=2.5 bbt.std
kla
Impact crowell
Interface QF=-2.9e12
inttrap e.level=0.3 acceptor density=1e12 sign=1e-16 sigp=1e-17 degen=12
###### set the method ######
method gummel newton
###### solve the condition bias ######
solve init
###### Bias the gate ######
###### Bias the drain ######
#solve Vdrain=0.1
solve Vdrain=0.05
solve Vdrain=0.1
solve Vdrain=0.25
solve Vdrain=1.0
###### Ramp the drain ######
###### prope field potential & generation ######
###### Ramp the gate ######
solve vgate=-0.05
solve vgate=-0.1
solve vgate=-0.25
log outf=3E1850nmXj(Vd1).log master
solve vgate=-2.5 vstep=0.05 vfinal=2.5 name=gate AC freq=1.0e+6 vss=0.01
#REGRID log doping ratio=6 outf=grid2 dopf=dopxx max.level=2
###### set the output characteristics ######
output  e.field j.electron j.hole j.conduc j.total e.velocity h.velocity \
     ex.field jx.electron jx.hole jx.conduc jx.total ex.velocity \
     hx.velocity ey.field jy.electron jy.hole jy.conduc jy.total \
     ey.velocity hy.velocity flowlines e.mobility h.mobility qss e.temp \
     h.temp charge recomb val.band con.band qfn qfp j.disp photogen impact \
     tot.doping
###### save the output characteristics to the structure ######
save outf=3E1850nmXj(Vd1).str
###### plot the final results ######
tonyplot 3E1850nmXj(Vd1).log -set 3E1850nmXj(Vd1).set
#tonyplot 3E1850nmXj(Vd1).str -set 3E1850nmXj(Vd1).set
###### extract the threshold voltage ######
```

```
#extract name="nvt" xintercept(maxslope(curve(abs(v."gate"),abs(i."drain"))))
#extract name="nvt_ave" (xintercept(maxslope(curve(abs(v."gate"),abs(i."drain"))))
        - abs(ave(v."drain"))/2.0)
#extract name="vt_final" x.val from curve(v."gate",(dydx(v."gate",(dydx(v."gate", i."drain"))))) \
        where y.val = max(dydx(v."gate",(dydx(v."gate", i."drain"))))
###### extract the transconductance ######
extract name="max_cur" max(i."drain")
extract name="gm" max(dydx(abs(v."gate"),abs(i."drain")))
extract name="gm" max(dydx(v."gate",i."drain"))
extract name="gm_curve" curve(v."gate",(dydx(v."gate",i."drain"))) outfile="gmcurve1.dat"
tonyplot gmcurve1.dat
extract name="gmdydx" deriv(v."gate", i."drain") outfile="dydx1003.dat"
tonyplot dydx1003.dat
#extract name="gmdydx2" deriv(v."gate", i."drain", 2) outfile="dydx1003.dat"
#tonyplot dydx1003.dat
###### extract the capacitances (gate.source/drain) ######
extract name="c_min" min(c."gate""source" + c."gate""drain")
extract name="c_curve" curve(v."gate",(c."gate""source" + c."gate""drain")) outfile="c1003.dat"
tonyplot c1003.dat
###### extract the cut off frequency ######
extract name="ft_curve" curve(v."gate",((dydx(abs(v."gate"), abs(i."drain")))/(6.28*(c."gate""source" + c."gate""drain"))))
outfile="ft.dat"
###### extract on current ######
#extract name="Ion" y.val from curve(v."gate",i."drain") where x.val=2.0
###### extract leakage current ######
#extract name="Ioff" min(i."drain")
#probe name=substrate_field.dat x=0.5 y=0.01 FIELD
#tonyplot substarte_field.dat
Quit
```

# Appendix B

ABrief process simulation for VMOSFET-FILOX With 40nm FILOX for series resistance extraction.

This process uses zero degree drain/source implantation 40s 1100°C RTA

```
go athena
set nitrideThick = 0.066
set gateOx = 12
################################### define mesh...
line x loc=0.0 spac=0.100
line x loc=0.9 spac=0.002
line x loc=1.1 spac=0.002
line x loc=2.0 spac=0.100
line y loc=0 spac=0.002
line y loc=0.15 spac=0.002
line y loc=0.4 spac=0.002
line y loc=1.0 spac=0.100
############################## start off material...
######################### p-type wafer...
######################## start of with a boron doped wafer (1Ohm*cm).
initialize silicon orientation=100 boron resistivity=1 space.mul=2
# p-well implant... using pearson model ... for high implant dose preferable turn-on
##################################cluster damage model
########################method high.conc full.cpl cluster.dam
implant boron dose=1.0e14 energy=75 pearson
##################################etch the pillar
etch silicon start x=0.0 y=0.0
etch continue x=1.0 y=0.0
etch continue x=1.0 y=0.370
etch done x=0.0 y=0.370
################################### 10mins O2 gas of drive in anealing
diffus time=10 temp=1100 dryo2 press=1.00
############################### 30mins nitride gas of drive in anealing
diffus time=30 temp=1100 nitro press=1.00
tonyplot
strip oxide
################################### stress relief pad oxide growth...
diffuse time=10 temp=900 dryo2 press=1.00 hcl.pc=3
tonyplot
extract name="pad_sio2" thickness material="sio~2" mat.occno=1 x.val=0.1 junc.occno=1 datafile="data.dat"
##################################deposit nitride layer
depo nitride thick=0.066 divisions=8
################################dry etch to leave the nitride fillet on the top of pad oside
etch nitride dry thick=0.066
etch oxide dry thick=$"pad_sio2"/10000
#############################dry etch to leave the nitride fillet on the top of pad oxide
#define the material viscous for laters thermal step
material oxide visc.0=5.1 visc.E=3.48 weto2
material nitride visc.0=2e3 visc.E=2.5625
oxide stress.dep=t
method viscous
#now grow the FILOX
```

```
diffuse time=1.33 temp=1100 weto2
############################drain source zero degree implant
implant arsenic dose=6.0e15 energy=100 tilt= 0 pearson
tonyplot
##########################to expose the vertical pillar sidewall
strip nitride
######################define etch machine in simulator
rate.etch machine=wetEtcher wet.etch oxide n.m isotropic=1.0
etch machine=wetEtcher time=20 min
######################meshing technique: method gridinit.ox=0.002 grid.oxide=0.002
######################now gate oxide
diffuse time=12 temp=800 dryo2 press=1.00
#####################poly-gate spacer depostition
deposit material=polysilicon thickness=0.200 division=8 c.phos=1e21
#######################etch to leave gate spacer
etch polysilicon left x=0.6 thick=0.200
etch polysilicon right x=1.04 thick=0.200
method fermi compress
#######################40s 1100degree rapid thermal annealing ##############
diffuse time=40/60 temp=1100 nitro press=1.0
#######################etch oxide for contact windows ##################
etch oxide left x=0.4
etch oxide right x=1.6
###########################now deposit the Al contacts #############
deposit alumin thick=0.03 division=2
###########etch the track to form the contacts #####################
etch alumin start x=0.4 y=-0.4
etch continue x=0.6 y=-0.4
etch continue x=0.6 y=0.5
etch done x=0.4 y=0.5
etch alumin start x=0.7 y=-0.4
etch continue x=1.6 y=-0.4
etch continue x=1.6 y=0.5
etch done x=0.7 y=0.5
electrode name=gate x=0.65 y=0.08
electrode name=source x=0.1 y=0.36
electrode name=drain x=1.8 y=0.05
electrode name=substrate backside
structure outfile=L100nmFILOX40nm.str
tonyplot L100nmFILOX40nm.str -set L100nmFILOX40nm.set
quit
```

# Appendix C

Z-parameters results for 100nm VMOSFET-FILOX with 40nm FILOX using zero degree drain/source implantation, 40s 1100°C RTA.

Under biases conditions:

$V_{GS}$=1V $V_{DS}$=0V

| Re(Z22) | Re(Z12) | Re(Z11) | Im(Z22) |
|---|---|---|---|
| 2.15E+03 | 1.14E+03 | 6.75E+02 | -9.55E-02 |
| 2.15E+03 | 1.14E+03 | 6.54E+02 | -9.55E-01 |
| 2.15E+03 | 1.14E+03 | 6.54E+02 | -4.78E+00 |
| 2.15E+03 | 1.14E+03 | 6.54E+02 | -9.55E+00 |
| 2.15E+03 | 1.14E+03 | 6.53E+02 | -4.77E+01 |
| 2.14E+03 | 1.14E+03 | 6.52E+02 | -9.53E+01 |
| 2.13E+03 | 1.13E+03 | 6.48E+02 | -1.89E+02 |
| 2.10E+03 | 1.12E+03 | 6.41E+02 | -2.79E+02 |
| 2.07E+03 | 1.10E+03 | 6.31E+02 | -3.65E+02 |
| 2.03E+03 | 1.08E+03 | 6.20E+02 | -4.45E+02 |
| 1.98E+03 | 1.05E+03 | 6.06E+02 | -5.19E+02 |
| 1.93E+03 | 1.02E+03 | 5.91E+02 | -5.85E+02 |
| 1.87E+03 | 9.95E+02 | 5.75E+02 | -6.45E+02 |
| 1.81E+03 | 9.63E+02 | 5.58E+02 | -6.96E+02 |

$V_{GS}$=2V $V_{DS}$=0V

| Re(Z22) | Re(Z12) | Re(Z11) | Im(Z22) |
|---|---|---|---|
| 1.02E+03 | 5.41E+02 | 3.22E+02 | -2.10E-02 |
| 1.02E+03 | 5.41E+02 | 3.23E+02 | -2.10E-01 |
| 1.02E+03 | 5.42E+02 | 3.24E+02 | -1.05E+00 |
| 1.02E+03 | 5.41E+02 | 3.24E+02 | -2.10E+00 |
| 1.02E+03 | 5.41E+02 | 3.24E+02 | -1.05E+01 |
| 1.01E+03 | 5.38E+02 | 3.22E+02 | -2.07E+01 |
| 1.02E+03 | 5.40E+02 | 3.23E+02 | -4.18E+01 |
| 1.01E+03 | 5.38E+02 | 3.22E+02 | -6.24E+01 |
| 1.01E+03 | 5.36E+02 | 3.21E+02 | -8.27E+01 |
| 1.00E+03 | 5.33E+02 | 3.19E+02 | -1.03E+02 |
| 9.96E+02 | 5.29E+02 | 3.17E+02 | -1.22E+02 |
| 9.88E+02 | 5.25E+02 | 3.15E+02 | -1.40E+02 |
| 9.80E+02 | 5.21E+02 | 3.13E+02 | -1.58E+02 |
| 9.71E+02 | 5.16E+02 | 3.10E+02 | -1.76E+02 |

$V_{GS}$=3V $V_{DS}$=0V

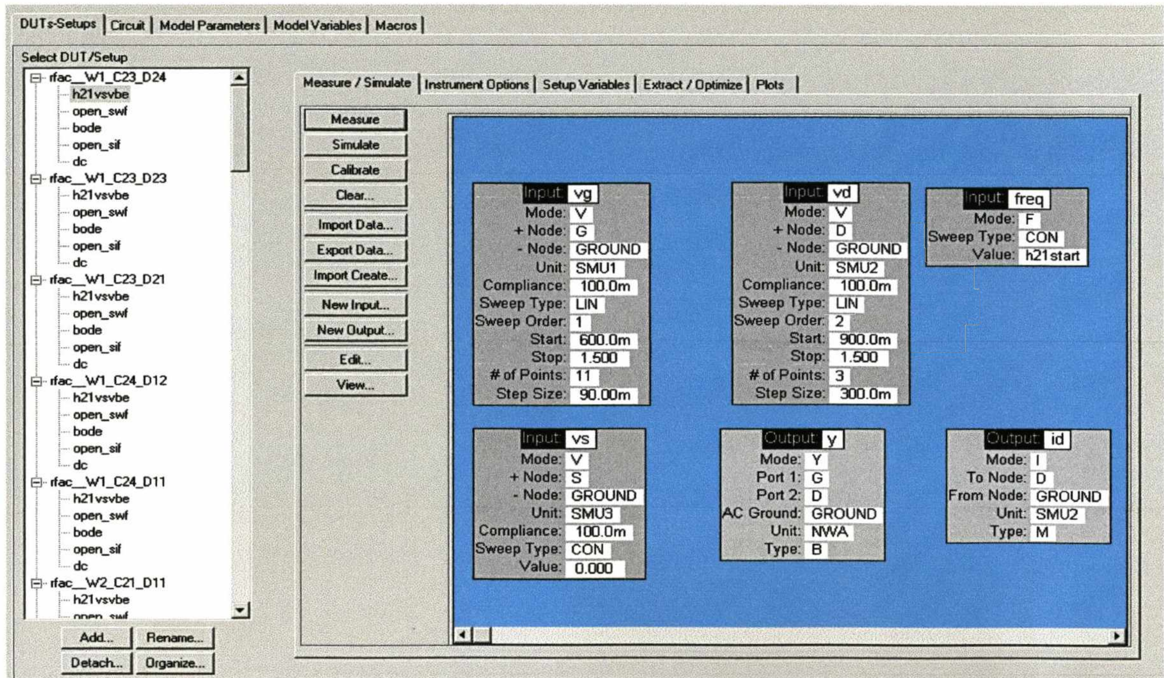
| Re(Z22) | Re(Z12) | Re(Z11) | Im(Z22) |
|---|---|---|---|
| 7.25E+02 | 3.87E+02 | 2.32E+02 | -1.04E-02 |
| 7.28E+02 | 3.89E+02 | 2.40E+02 | -1.06E-01 |
| 7.30E+02 | 3.90E+02 | 2.41E+02 | -5.35E-01 |
| 7.27E+02 | 3.88E+02 | 2.40E+02 | -1.05E+00 |
| 7.30E+02 | 3.90E+02 | 2.41E+02 | -5.34E+00 |
| 7.30E+02 | 3.90E+02 | 2.41E+02 | -1.07E+01 |

| | | | |
|---|---|---|---|
| 7.29E+02 | 3.89E+02 | 2.40E+02 | -2.13E+01 |
| 7.28E+02 | 3.89E+02 | 2.40E+02 | -3.19E+01 |
| 7.26E+02 | 3.88E+02 | 2.39E+02 | -4.23E+01 |
| 7.24E+02 | 3.87E+02 | 2.39E+02 | -5.26E+01 |
| 7.21E+02 | 3.85E+02 | 2.38E+02 | -6.27E+01 |
| 7.18E+02 | 3.83E+02 | 2.37E+02 | -7.26E+01 |
| 7.14E+02 | 3.81E+02 | 2.36E+02 | -8.23E+01 |
| 7.10E+02 | 3.79E+02 | 2.35E+02 | -9.16E+01 |

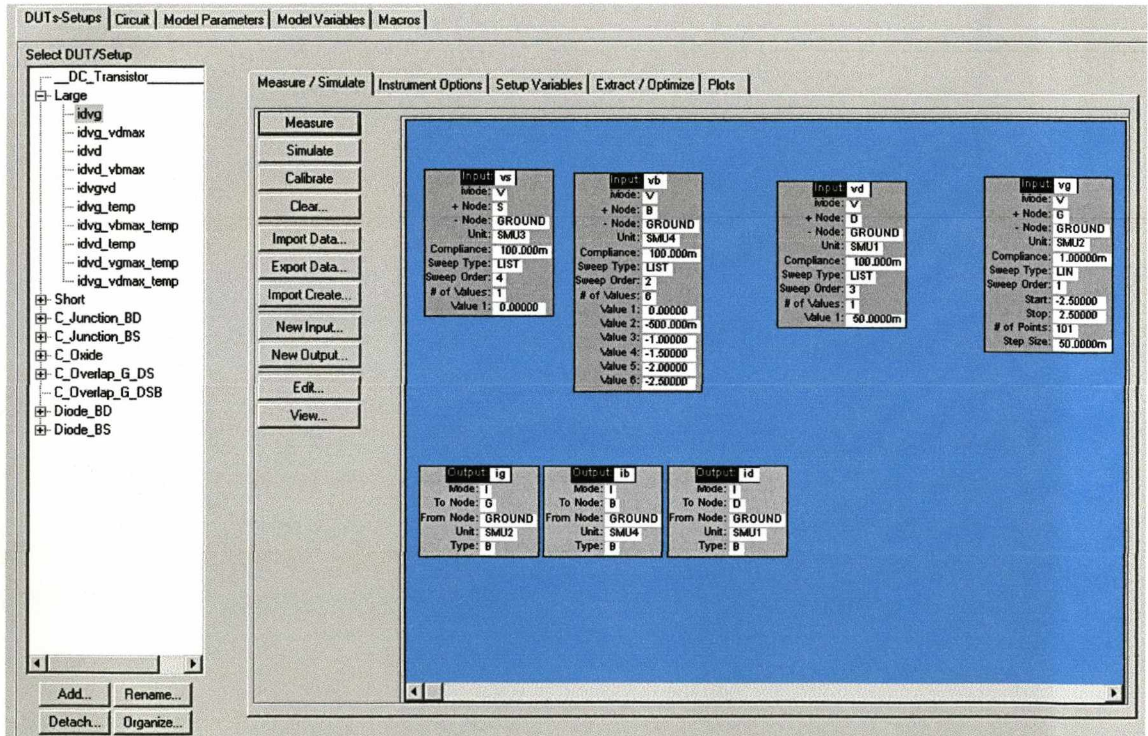
# Appendix D

## IC-CAP Setup for $f_T$ characterisation and EKV model – DC part extraction

### I. $f_T$ Characterisation:




### II. EKV Modelling – DC and CV Part



Appendix E

# Brief Introduction to Enz-Krummenacher-Vittoz (EKV) Model Bases

The EKV model explicitly describes the basic relationships between currents, charges and biases using a charge-surface potential approach where the variation of inversion charge with respect to surface potential and gate, drain, source bias conditions are linearized. In this process, these relations are simplified by using concepts of slope factor $n_q$ and channel pinch-off voltage $V_p$. The substrate bias is taken as a reference rather than the source which is used in most of the industry standard models such as BSIM. In an n-type long channel device, the inversion layer charge is related to surface potential $\psi_s$ or $V_p$ and channel potential V as expressed as below

$$Q_{inv} = n_q C_{ox}(\psi_s - 2\psi_B) \quad \text{Eq. F1}$$

or

$$Q_{inv} = n_q C_{ox}(V_p - V) \quad \text{Eq. F2}$$

where $n_q$ is the slope factor with a mathematical definition of $n_q = \frac{1}{C_{ox}} \frac{dQ_{inv}}{d\psi_s}$, V is the channel potential defined as the electron quasi-Fermi potential as before. The term V is controlled by the drain and source voltage $V_D$ and $V_S$. $V_P$ is further related to gate voltage, $V_G$ using the expression below

$$V_P = \frac{V_G - V_{FB} - 2\psi_B - \gamma\sqrt{2\psi_B}}{n_q} \quad \text{Eq. F3}$$

where $\gamma_b$ is the substrate modulation factor (also known as the body-effect coefficient) given as

$$\gamma_b = \frac{\sqrt{2qN_a\varepsilon_{si}}}{n_q} \quad \text{Eq. F4}$$

To further simplify the derivation, the potential and charge parameters can be normalized using equations F5 and F6,

$$\frac{V}{v} = \frac{\psi}{\psi} = U_T = \frac{kT}{q} \qquad \text{Eq. F5}$$

$$q_{inv} = \frac{Q_{inv}}{Q_{spec}} \qquad \text{Eq. F6}$$

Where the specific charge factor $Q_{spec} = -2nU_TC_{ox}$ ,

Substituting equation F2 into the $Q_{inv}$ expression in equation F7 derived from Poisson's equation and replacing $\psi_S$ with the pinch-off voltage and channel voltage, the inversion layer charge can then be related to $V_P$ and V with normalisation as shown in equation F8.

$$Q_{inv} = -\gamma_b C_{ox}\sqrt{U_T}\left(\sqrt{\frac{\psi_S}{U_T} + \exp\frac{\psi_S - 2\Phi_F - V}{U_T}} - \sqrt{\frac{\psi_S}{U_T}}\right) \qquad \text{Eq. F7}$$

$$2q_{inv} + \ell n q_{inv} = v_p - v \qquad \text{Eq. F8}$$

Since in this model, gate, drain and source are referred to substrate, the drain current is equal to the difference between forward reverse current components. These current components and the total drain current can be normalised by a term $I_{spec} = 2n\mu C_{ox}\frac{W}{L}U_T^2$ and are presented in equation F9. The drain current can then be expressed as equation F10.

$$\frac{I_D}{i_d} = \frac{I_F}{i_f} = \frac{I_R}{i_r} = I_{spec} \qquad \text{Eq. F9}$$

$$i_d = i_f - i_r \qquad \text{Eq. F10}$$

The normalized forward and reverse current are further related to $q_s$ and $q_d$ which are normalized charge densities at the source and drain side of the channel:

$$i_f = \int_{v_S}^{\infty} q_i \cdot dv = q_s^2 + q_s \qquad \text{Eq. F11}$$

$$i_r = \int_{v_d}^{\infty} q_i \cdot dv = q_d^2 + q_d \qquad \text{Eq. F12}$$

Where $q_s$ and $q_d$ are controlled by the potential differences: $v_p$-$v_d$ and $v_p$-$v_s$ respectively [114].

By combining equation F8, F10, F11 and F12, a general equation can be obtained relating drain, source and pinch-off voltage to the forward and reverse current through the

charge terms. Therefore the current-voltage relations can be summarised in equation F13 of which the detailed derivation is presented in [114].

$$v_p - v_{s,d} = \sqrt{1 + 4i_{f,r}} + \ell n\left(\sqrt{1 + 4i_{f,r}} - 1\right) - (1 + \ell n2) \qquad \text{Eq. F13}$$

Equation F14 can allow an accurate interpolation of the current between the weak and strong inversion regimes as follows:

$$i_{f,r} = \ell n^2[1 + \exp\frac{v_p - v_{s,d}}{2}] \qquad \text{Eq. F14}$$

The pinch-off voltage $V_P$ is a function of gate bias $V_G$ as shown in equation F3. As a result, the EKV model describes the current-to-voltage relation accurately in all modes of inversion and therefore provides good continuity in describing the transition from weak to moderate to strong inversion. This is particularly important for analogue and RF devices. The BSIM models especially BSIM3v3 are known to be inaccurate in the moderate inversion region [115].

As discussed previously, the charge linearization, parameter normalization and symmetry of forward and reverse operation are used to derive analytical expressions for the MOSFET current. Besides the current, most of the physics related parameters in the model can be derived or related to the inversion charges $q_s$ and $q_d$. This leads to a significant reduction in complexity of the model structure as well as making parameter extraction a much simpler task with fewer parameters required. Meanwhile, the model maintains close linkage to the fundamental device physics. These parameters include transconductance, intrinsic capacitances, mobility, thermal and gate noise, short channel effects and non-quasi-static effect etc. The most important small-signal parameters are the transconductances. The transconductances of the drain, source and gate nodes are treated separately as indicated in equation F15.

$$\Delta I_D = \frac{\partial I_f}{\partial V_S}\Delta V_S + \frac{\partial I_r}{\partial V_D}\Delta V_D + \frac{\partial I_D}{\partial V_G}\Delta V_G = G_{ms}\Delta V_s - G_{md}\Delta V_D + G_m\Delta V_G \qquad \text{Eq. F15}$$

Where $G_{ms}$ is the source transconductance, $G_{md}$ is the drain transconductance, $G_m$ is the gate transconductance which can be related to $q_s$ and $q_d$ as

$$G_{ms} = G_{spec} q_s \quad \text{Eq. F16}$$

$$G_{md} = G_{spec} q_d \quad \text{Eq. F17}$$

Where $G_{spec} = 2n\mu C_{ox} \frac{W}{L} U_T$

$$G_m = \frac{G_{ms} - G_{md}}{n_q} \quad \text{Eq. F18}$$

Thus the transconductance parameter in different operation regions can be related to the inversion charges at the source and drain ends of the channel and further to the gate, drain, and source biases according to equation F8 and F3.

When the device is operating at high frequency, the intrinsic part of the MOSFET also needs to include the intrinsic capacitances to allow modelling of the transient currents at each terminal of the device. These capacitances can be defined as the variation of gate charge $Q_G$ with respect to variations of the terminal biases $\Delta V_S$, $\Delta V_D$, $\Delta V_B$. The most important three intrinsic capacitances are defined below, after normalisation

$$c_{gsi} = -\frac{\partial Q_G}{\partial V_S C_{ox}} = \frac{q_s}{3} \cdot \frac{(2q_s + 4q_d + 3)}{(q_d + q_s + 1)^2} \quad \text{Eq. F19}$$

$$c_{gdi} = -\frac{\partial Q_G}{\partial V_D C_{ox}} = \frac{q_d}{3} \cdot \frac{(2q_d + 4q_s + 3)}{(q_d + q_s + 1)^2} \quad \text{Eq. F20}$$

$$c_{gbi} = -\frac{\partial Q_G}{\partial V_B C_{ox}} = \frac{n-1}{n}(1 - c_{gsi} - c_{gdi}) \quad \text{Eq. F21}$$

The intrinsic capacitances can also be continuously described between the weak and strong inversion regions with the help of an interpolation function.

The advanced aspects of the operation of deep-submicron devices such as short channel effect, vertical and lateral field dependent mobility, velocity saturation, poly-depletion and quantum effects can also be coupled with the surface potential based model allowing continuous validation of these phenomena in all operation regions. Full details are presented in [114,116].

It can be concluded that the EKV model provides analytical, continuous and physically correct descriptions of inversion charge variation in weak, moderate and strong regions with respects to bias variations and is more closely linked to the processing parameters.

This compact model use sufficiently simple expressions with a minimum need for process dependent parameters and less fitting parameters than other industry standard models. It is particularly well suited to the design of analogue circuits.

# Appendix F

**Published Papers:**

L. Tan, M. M. A. Hakim, S. Connor, A. Bousquet, W. Redman-White, P. Ashburn, S. Hall, 'Characterisation of CMOS Compatible Vertical MOSFETs with New Architectures through EKV Parameter Extraction and RF Measurement Characterisation of CMOS Compatible Vertical MOSFETs with New Architectures through EKV Parameter Extraction and RF Measurement', The 10th International Conference on Ultimate Integration of Silicon, March, 2009.

M.M.A. Hakim, L. Tan, T. Uchino, O. Buiu, W. Redman-White, S. Hall and P. Ashburn, 'Improved sub-threshold slope in short channel vertical MOSFETs using FILOX oxidation.' Special Issue, Journal of Solid-State Electronics, 2009.

L. Tan, M. M. A. Hakim, T. Uchino, W. Redman-White, P Ashburn and S. Hall, 'DC Effect of Asymmetrical Characteristics of Junction Regions in Implantation Defined Surrounded Gate Vertical MOSFETs,' Accepted by The 9th International Conference on Solid-state and Integrated Circuit Technology, Oct. 2008. (Did not go for the presentation due to the work load)

M.M.A. Hakim, L. Tan, T. Uchino, O. Buiu, W. Redman-White, S. Hall and P. Ashburn, 'Improved sub-threshold slope in RF vertical MOSFETs using a frame gate architecture.' The 38th European Solid-state Device Research Conference, Aug., 2008.

L. Tan, S. Hall, O. Buiu, M.M.A. Hakim, T. Uchino, P. Ashburn, W. Redman-White, 'Series Resistance in Vertical MOSFETs with Reduced Drain/Source Overlap Capacitance', The 9th International Conference on Ultimate Integration of Silicon, March, 2008.

L. Tan, O. Buiu, S. Hall, E. Gili, T. Uchino, P. Ashburn, 'The influence of Junction Depth on Short Channel Effects in Vertical MOSFETs', Journal of Solid-State Electronics, Vol. 52, Issue 7, pp.1002-1007, July, 2008.

L. Tan, O. Buiu, S. Hall, E. Gili, P. Ashburn, 'A technology for building shallow junction MOSFETs on vertical pillar walls', The 8th International Conference on Solid-State and Integrated Circuit Technology - ICSICT. pp.472-474, Oct., 2006.

L. Tan, J. Chen, S. Hall, P. Ashburn, 'Improvement in $f_T$ for Vertical MOSFETs with reduced parasitic capacitance by the FILOX', PREP05, 2005.

**Other submitted papers and joined engineering contest:**

L. Tan, T.Uchino, M. M. A. Hakim, S. Hall, O.Buiu, P. Ashburn, M.Lemme, J.Moers 'Technology for Ultra-thin Pillar Vertical MOSFETs with Reduced Overlap Capacitance', submitted to The 37th European Solid-state Device Research Conference, April, 2007.

T.Uchino, E. Gili, M. M. A. Hakim, V. D. Kunz, C. H. de Groot, P. Ashburn, L. Tan, S. Hall, 'Improved Vertical pMOSFET Performance Using a Dielectric Pocket and an Epitaxial Channel', submitted to The 38th European Solid-state Device Research Conference, April, 2007.

L.Tan, S.Hall, 'Feasibility of Deco-nanometer Vertical MOSFETs for RF application', final six, Speak-Out-Engineering, IET Contest, May, 2007.