January 2020

PCIe GEN4 AND PCIe GEN3/SATA DEVICES SWITCHING SCHEME

HP INC

PCIe Gen4 and PCIe Gen3/SATA Devices switching scheme

Disclosed is a way to support PCIe NVMe Gen4 SSD Devices in addition to maintaining support for PCIe NVMe Gen3 SSD's and SATA and Hybrid drives like H10. Chipsets are being architected to support PCIe Gen4 interface in the CPU for higher bandwidth devices such as graphics and high speed SSDs. However, the I/O controller in the chipset maintains support for PCIe Gen3/SATA and stops short of supporting PCIe Gen4 devices.

Most thin and light platforms can only provide one M.2 slot dedicated to the storage device due to the physical limitations of the platform which is why this disclosure addresses the ability to support all SSD types in one M.2 slot. Please see the block diagram below for the implementation:
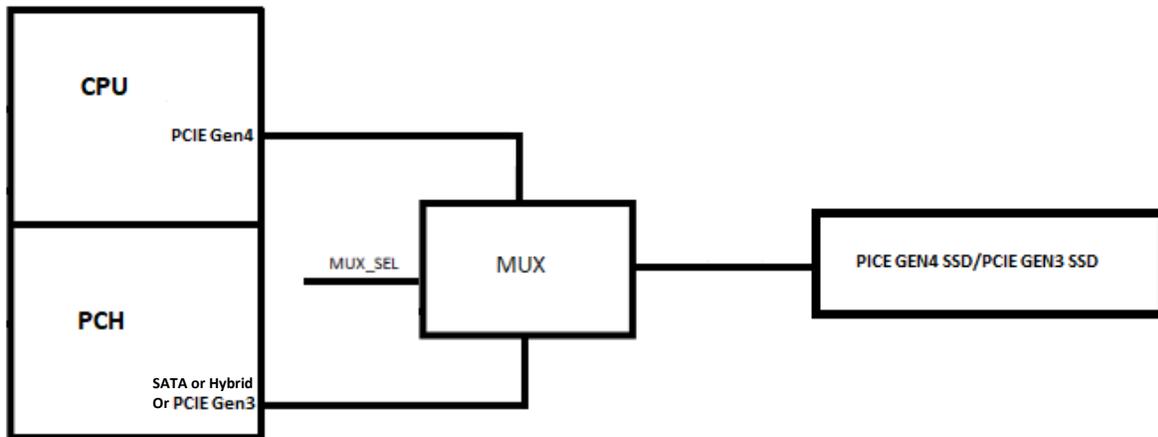
Figure 1: Block Diagram Showing the Ability to Switch Between CPU and PCH based PCIe/SATA Interface

When the system boots, system BIOS will default to PCH and interrogate the SSD and find out its capabilities and if it notices that SSD is capable of Gen4 NVMe, it will issue a RESET and force retraining to the Gen4x4 interface from the CPU side instead of the current Gen3x4 or SATA on the I/O side of the chipset.

PCIe Gen4 is the fourth generation of the Peripheral Component Interconnect Express motherboard interface and it is twice as fast as PCIe Gen3. PCIe Gen4 NVMe SSD's are starting to appear in the market but are still not mainstream, the proposed switching scheme method is to support the PCIe Gen4 NVMe SSD when it is widely available in the market while continuing to support the lower end options available today.

The advantage of this switching scheme is to support the highest speed PCIe Gen4 NVMe SSD devices when they become available which gives higher value to the existing hardware by extending its life longer. At the same time all the older interfaces like SATA and PCIe Gen3 are still supported including special interfaces like Hybrid drives which require special setup capabilities only present in the I/O controller.

Disclosed by Monji Jabori, Jonathan Vu and Darrell Brokmeyer, HP Inc.