UNIVERSITAS GUNADARMA

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SURAT PERJANJIAN PENUGASAN
DALAM RANGKA PELAKSANAAN PROGRAM PENELITIAN
TAHUN ANGGARAN 2016
Nomor : 017.1/LP/UG/VI/2016

Pada hari ini **Selasa** tanggal **Dua Puluh Satu** bulan **Juni** tahun **Dua Ribu Enam Belas**, kami yang bertandatangan di bawah ini :

1. Dr. Ir. Hotniar Siringoringo, M.Sc. : **Ketua LP Universitas Gunadarma,** bertindak atas nama Rektor **Universitas Gunadarma** yang selanjutnya dalam Surat Perjanjian ini disebut sebagai **PIHAK PERTAMA;**

2. Dr. Eri Prasetyo Wibowo : Dosen Universitas Gunadarma, dalam hal ini bertindak sebagai pengusul dan Ketua Pelaksana Penelitian Tahun Anggaran 2016 untuk selanjutnya disebut **PIHAK KEDUA.**

Perjanjian penugasan ini berdasarkan pada Surat Perjanjian Pelaksanaan Hibah Penelitian bagi dosen perguruan tinggi Swasta Kopertis Wilayah III Tahun Anggaran 2016, **Nomor : 790/K3/KM/SPK.LT/2016, tanggal 14 Juni 2016**

PIHAK PERTAMA dan **PIHAK KEDUA**, secara bersama-sama bersepakat mengikatkan diri dalam suatu Perjanjian Pelaksanaan Penugasan Penelitian **Kerjasama Luar Negeri dan Publikasi Internasional** Tahun 2016 dengan ketentuan dan syarat-syarat sebagaimana diatur dalam pasal-pasal sebagai berikut:

Pasal 1

(1.) **PIHAK PERTAMA** memberi tugas kepada **PIHAK KEDUA**, dan **PIHAK KEDUA** menerima tugas tersebut untuk melaksanakan Penugasan Penelitian **Kerjasama Luar Negeri dan Publikasi Internasional** tahun 2016 dengan judul '**Design and Implementation of Asynchronous Analog to Digital Converter (A-ADC) Based on CMOS Technology into A CHIP**'.

(2.) **PIHAK KEDUA** bertanggung jawab penuh atas pelaksanaan Administrasi dan keuangan atas pekerjaan sebagai mana dimaksud pada ayat 1 dan berkewajiban

menyerahkan semua bukti-bukti pengeluaran serta dokumen pelaksanaan lainnya dalam bendel laporan yang tersusun secara sistematis kepada **PIHAK PERTAMA**.

Pelaksanaan Penugasan Penelitian **Kerjasama Luar Negeri dan Publikasi Internasional** tahun 2016 sebagaimana dimaksud judul penelitian di atas didanai dari DIPA Direktorat Riset dan Pengabdian Masyarakat Dirjen Direktorat Riset dan Pengabdian Masyarakat dirjen Riset dan Pengembangan Kemenristekdikti Nomor SP DIPA-042.06.1.401516/2016 tanggal 7 Desember 2015.

Pasal 2

(1) **PIHAK PERTAMA** menyerahkan dana penelitian sebagaimana dimaksud dalam pasal 1 sebesar **Rp. 160.000.000,-** ***(Seratus Enam Puluh Juta Rupiah)*** yang berasal dari DIPA Direktorat Riset dan Pengabdian Masyarakat Dirjen Direktorat Riset dan Pengabdian Masyarakat dirjen Riset dan Pengembangan Kemenristekdikti Nomor SP DIPA-042.06.1.401516/2016 tanggal 7 Desember 2015.

(2) Dana Penugasan Pelaksanaan sebagaimana dimaksud pada ayat (1) dibayarkan oleh **PIHAK PERTAMA** kepada **PIHAK KEDUA** secara bertahap dengan ketentuan sebagai berikut:

a. Pembayaran Tahap Pertama sebesar 70% dari total bantuan dana kegiatan yaitu 70% X ***Rp. 160.000.000,- = Rp. 112.000.000,- (Seratus Duabelas Juta Rupiah)***.
b. Pembayaran Tahap Kedua sebesar 30% dari total dana yaitu 30% X ***Rp. 160.000.000,- = Rp. 48.000.000,- (Empat Puluh Delapan Juta Rupiah),*** dibayarkan setelah **PIHAK KEDUA** menyerahkan *hardcopy* Laporan Kemajuan Pelaksanaan Penugasan Penelitian Kerjasama Luar Negeri dan Publikasi Internasional Tahun Anggaran 2016 paling lambat tanggal 30 September 2016 dan Laporan Penggunaan Anggaran 70% yang telah dilaksanakan kepada **PIHAK PERTAMA** dan mengunggah *soft copy*nya ke SIMLITABMAS paling lambat tanggal 30 Oktober 2016.
c. **PIHAK KEDUA** bertanggungjawab mutlak dalam pembelanjaan dana tersebut pada ayat (1) sesuai dengan proposal kegiatan yang telah disetujui dan berkewajiban untuk menyerahkan kepada **PIHAK PERTAMA** semua bukti-bukti pengeluaran sesuai dengan jumlah dana yang diberikan oleh **PIHAK PERTAMA**.
d. **PIHAK KEDUA** berkewajiban mengembalikan sisa dana yang tidak dibelanjakan kepada **PIHAK PERTAMA** untuk disetor ke Kas Negara.

Pasal 3

Dana Penugasan sebagaimana dimaksud dalam Pasal 2 ayat 1 dibayarkan kepada **PIHAK KEDUA** melalui rekening yang diajukan dan atas nama **PIHAK KEDUA**

Pasal 4

(1) **PIHAK KEDUA** berkewajiban menindaklanjuti dan mengupayakan hasil Program Hibah Penelitian berupa hak kekayaan intelektual dan atau publikasi ilmiah sesuai dengan luaran yang dijanjikan pada Proposal.

(2) Perolehan hasil sebagaimana dimaksud pada ayat (1) harus dilaporkan secara lengkap kepada **PIHAK PERTAMA**

Pasal 5

PIHAK KEDUA berkewajiban:

(1) **Mengisi** catatan harian pada situs simlitabmas.ristekdikti.go.id mulai 15 Juli 2016.
(2) **Mengunggah** laporan kemajuan pelaksanaan kegiatan pada situs simlitabmas.ristekdikti.go.id paling lambat tanggal 20 Agustus 2016.
(3) **Mengikuti** Monitoring dan Evaluasi (Monev) internal yang direncanakan akan dilaksanakan sekitar tanggal 15-20 Agustus, dan Monev Eksternal sekitar tanggal 1-30 September 2016.
(4) **Mengunggah laporan akhir dan proposal lanjutan (bagi yang lanjut)** pada situs simlitabmas.ristekdikti.go.id paling lambat Tanggal 30 Oktober 2016.
(5) **Mengunggah laporan keuangan** pada situs simlitabmas.ristekdikti.go.id paling lambat Tanggal 30 Oktober 2016.
(6) **Menyerahkan *hardcopy* laporan akhir penelitian 3 eksemplar dan laporan keuangan 1 eksemplar kepada PIHAK PERTAMA paling lambat 10 November 2016.**
(7) **Mengikuti diseminasi hasil penelitian yang direncanakan akan dilaksanakan sekitar bulan Desember 2016.**

Pasal 6

Perubahan terhadap susunan tim pelaksana dan substansi pelaksanaan Program Hibah Penelitian dapat dibenarkan apabila telah mendapat persetujuan tertulis dari Direktur Penelitian dan Pengabdian Kepada Masyarakat Direktorat Jenderal Pendidikan Tinggi.

Pasal 7

(1) Apabila **PIHAK KEDUA** selaku ketua pelaksana sebagaimana dimaksud pada Pasal 1 tidak dapat melaksanakan Program Hibah Penelitian Tahun 2016, maka **PIHAK KEDUA** wajib mengusulkan pengganti ketua pelaksana yang merupakan salah satu anggota tim yang memenuhi syarat kepada **PIHAK PERTAMA**.
(2) Apabila **PIHAK KEDUA** tidak dapat melaksanakan tugas dan tidak ada pengganti ketua sebagaimana dimaksud dalam Pasal 1 maka **PIHAK KEDUA** harus mengembalikan dana kepada **PIHAK PERTAMA** yang selanjutnya disetor ke Kas Negara.
(3) Bukti setor sebagaimana dimaksud pada ayat (2) disimpan oleh **PIHAK PERTAMA.**

Pasal 8

(1) Apabila sampai dengan batas waktu yang telah ditetapkan untuk melaksanakan Hibah Penelitian telah berakhir, **PIHAK KEDUA** belum menyelesaikan tugasnya dan atau **terlambat mengirim laporan Kemajuan** dan atau **terlambat mengirim laporan akhir**, maka **PIHAK KEDUA** dikenakan **sanksi denda sebesar 1 ‰ (satu permil) setiap hari keterlambatan sampai dengan setinggi-tingginya 5% (lima persen)**, terhitung dari tanggal jatuh tempo sebagaimana tersebut pada

laporan akhir, maka **PIHAK KEDUA** dikenakan **sanksi denda sebesar 1 ‰ (satu permil) setiap hari keterlambatan sampai dengan setinggi-tingginya 5% (lima persen)**, terhitung dari tanggal jatuh tempo sebagaimana tersebut pada pasal 1 ayat (1), 2 dan ayat (3), yang terdapat dalam Surat Perjanjian Pelaksanaan Program Hibah Penelitian Universitas Gunadarma Tahun Anggaran 2016 ;

(2) Denda sebagaimana dimaksud pada ayat (3) disetorkan ke Kas Negara dan foto copy bukti setor denda yang telah divalidasi oleh KPPN setempat diserahkan kepada **PIHAK PERTAMA.**

Pasal 9

(1) Apabila dikemudian hari judul Penelitian Kerjasama Luar Negeri dan Publikasi Internasional sebagaimana dimaksud pada Pasal 1 ditemukan adanya duplikasi dengan Hibah Penelitian lain dan/atau ditemukan adanya ketidak-jujuran/itikad kurang baik yang tidak sesuai dengan kaidah ilmiah, maka kegiatan Program Hibah Penelitian tersebut dinyatakan batal dan **PIHAK KEDUA** wajib mengembalikan dana Penelitian Kerjasama Luar Negeri dan Publikasi Internasional Tahun 2016 yang telah diterima kepada **PIHAK PERTAMA** yang selanjutnya disetor ke Kas Negara.

(2) Bukti setor sebagaimana dimaksud pada ayat (1) disimpan oleh kepada **PIHAK PERTAMA.**

Pasal 10

Hal-hal dan atau segala sesuatu yang berkenaan dengan kewajiban pajak berupa PPN dan/atau PPh menjadi tanggungjawab **PIHAK KEDUA** dan harus dibayarkan ke kantor pelayanan pajak setempat sebagai berikut:

(1.) Pembelian barang dan jasa dikenai PPN sebesar 10% dan PPh 22 sebesar 1,5%;

(2.) Belanja honorarium dikenai PPh Pasal 21 dengan ketentuan:

a. 5% bagi yang memiliki NPWP untuk golongan III, serta 6% bagi yang tidak memiliki NPWP.
b. Untuk golongan IV sebesar 15%; dan

(3.) Pajak-pajak lain sesuai ketentuan yang berlaku.

Pasal 11

(1) Hak atas kekayaan intelektual yang dihasilkan dari pelaksanaan Program Hibah Penelitian diatur dan dikelola sesuai dengan peraturan dan perundang-undangan yang berlaku.

(2) Hasil Program Hibah Penelitian berupa peralatan dan/atau alat yang dibeli dari kegiatan ini adalah milik Negara yang dapat dihibahkan kepada institusi/lembaga/masyarakat melalui Surat Keterangan Hibah.

Pasal 12

(1) Apabila terjadi perselisihan antara **PIHAK PERTAMA** dan **PIHAK KEDUA** dalam pelaksanaan perjanjian ini akan dilakukan penyelesaian secara musyawarah dan mufakat, dan apabila tidak tercapai penyelesaian secara musyawarah dan mufakat maka penyelesaian dilakukan melalui proses hukum.

Pasal 13

Surat Perjanjian Penugasan Pelaksanaan Program Hibah Penelitian ini dibuat rangkap 2 (dua) dan bermaterai cukup sesuai dengan ketentuan yang berlaku.

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PIHAK KEDUA

Dr. Eri Prasetyo Wibowo
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Code/Field of science: 465/ Teknik Elektro dan Informatika yang belum tercantum

RESEARCH P R O P O S A L
INTERNATIONAL RESEARCH COLLABORATION AND SCIENTIFIC PUBLICATION

DESIGN AND IMPLEMENTATION OF ASYNCHRONOUS ANALOG TO DIGITAL CONVERTER (A-ADC) BASED ON CMOS TECHNOLOGY INTO A CHIP

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GUNADARMA UNIVERSITY, INDONESIA

JANUARY 2016

LEMBAR PENGESAHAN
PENELITIAN KERJASAMA LUAR NEGERI DAN PUBLIKASI INTERNASIONAL

Title of Research	:	Design and Implementation of Asynchronous Analog to Digital Converter (A-ADC) Based on CMOS Technology into A CHIP
Code/Name of Field of science	:	465 / Bidang Teknik Elektro dan Informatika Lain Yang Belum Tercantum
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Length of research period	:	2 years
Year of research	:	2
Total research funds	:	Rp 400.000.000,00 (US $ 0)
Research funds of current year	:	- to Dikti Rp 200.000.000,00 (US $ 0)
		- Internal univ. Rp 5.000.000,00 (US $ 0)
		- Others Rp 0,00 (US $ 0)
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ABSTRACT

The research will design and transform the Asynchronous ADC (A-ADC) into CHIP, using the N comparators method. The A-ADC is used for embedding system of low in power consumption, high speed, at 100 MSPS, high resolution, and small layout size. The research work takes two years time for completion.

The first year work aims at completing the design, verification, and simulation, which is followed by designing the MOS composition and parameter of the A-ADC, refers to the parameters generated in the schematic design. Layout of the design is stimulated in order to get design information, as resulted, before it is fabricated. The results obtained are verified in accordance with the schematic design. Indicator of this stage achievement is layout of A-ADC Chip, to be sent for fabrication.

And in the second year, is to finalizing the work and sending the floor plan layout for fabrication, aims at producing the A-ADC Chip. The layout will be fabricated, using CMP-TIMA services, in France, which indicate the existing MOU in action, between Gunadarma University and Universite de Bourgogne, Dijon, France. Mentor Graphics with AMS 0.35 um CMOS technology were used for designing and stimulation the circuit.

The overall research output as targeted, will be the CIP ADC, go along with international publications, and obtaining Intellectual Property Right (HAKI). And included exchange of professors and students.

Keyword : analog; digital; asynchronous; schematic; layout; Mentor Graphics

CHAPTER 1 INTRODUCTION

1.1. BACKGROUND

Analog to Digital Converter (ADC) is one of the main components in digital signal processing system. It serves to convert analog into digital signals. The process of digitalization is done through sampling and quantization. Sampling speed will determine the number of samples per unit time (seconds). Medium resolution quantization determines the number of bits used to encode the value of each sample. With the continued development of high speed digital electronic devices that use analog data input, the role of the ADC is increasing.

Types of ADC are manifold as shown in Figure 1.1. There are several options to determine the type of ADC is designed.

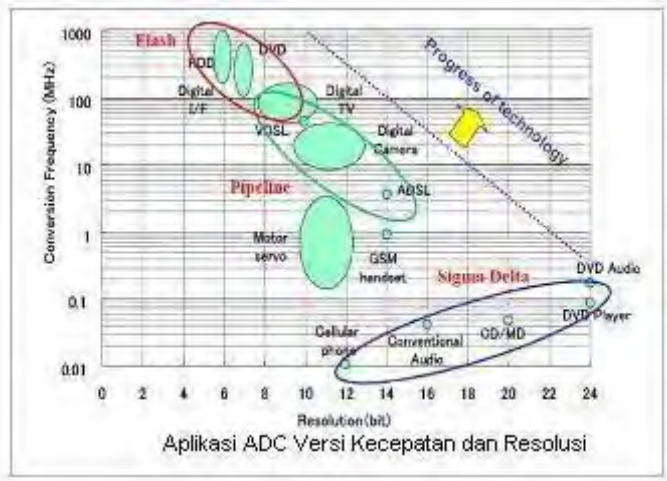


Figure 1.1. Comparison of ADC performance

Currently, the need for an ADC is quite high, with special attention to the following specifications: low power consumption, low voltage, high conversion speed small delay, large bits output and minimum area layout. With these specifications, Asynchronous ADC (A-ADC) is one of the devices to be conducted in the research collaboration.

The track record of the research team can be seen in Figure 1.2. Since 2005 a team of researchers have developed a laboratory of System on chip and worked in the CMOS design.

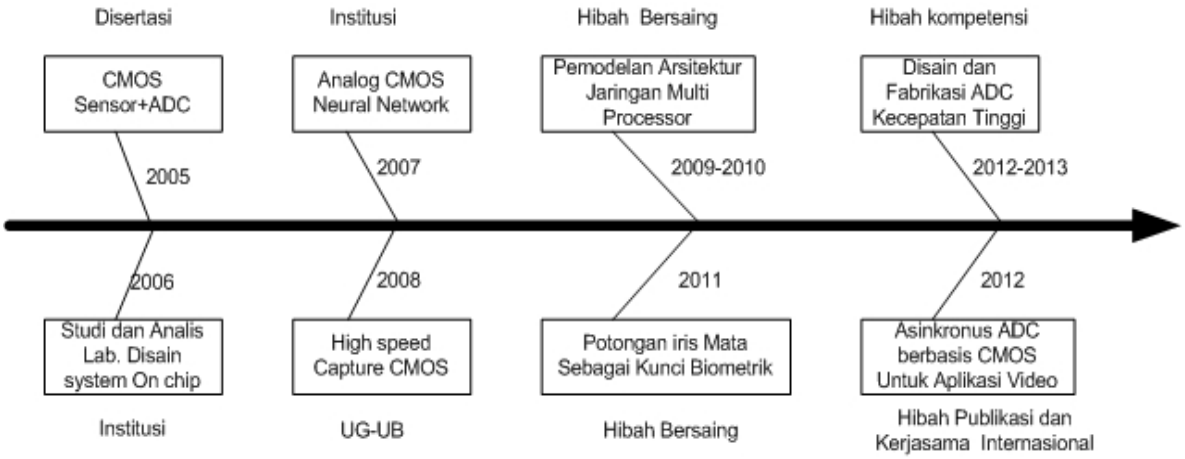


Figure 1.2. Road map of researchers

Research Collaboration between Universite de Bourgogne France and Gunadarma University, base on institutional sharing principle, since 2005 to date has produced scientific articles published in international journals and proceeding, research grants, including "Hibah Bersaing, Hibah Kompetensi". In line with exchange of professors and students, Dr Eri Prasetyo Wibowo, a member of collaborative research of Gunadarma University, was invited and to become "Jury"of dissertation for Gunadarma doctorate student, defended his dissertation at Universite de Bourgogne France, late November 2013.

In first year 2012, the Gunadarma research Team, consisting of Busono Sorjiwirjo, Prof., Dr (Head), Eri Prasetyo Wibowo (Member) and Hamzah Afandi(Member), had received and implemented the first year of the three successive years research grant, as proposed, under the International Research Collaboration and Scientific Publication. From Directorate General of Higher Education.

The second year grant, however, was not granted, due to late notification. And the research Team were unable to expose its proposal as required, which ultimately decided the second research grant to be discontinued, if not considered disqualified.

Therefore, in first year 2014/2015, the Team submitted the second year proposal as initially planed for realization of the ADC design into a CHIP . We do expect that the on-going research work will be implemented as planed, and to enable the

collaborative research Team end up the last part of the three successive years plan in First year 2015/2016.

1.2. SPECIAL PURPOSE

The objective of this research is Designing and implementing 8 bits Asynchronous ADC, have speed 100 MSPS with the topology of N comparators such as comparators, digital logic, DAC (switch capacitor), sample and hold using mentor graphics software with AMS (Austria Micro Systems) 0.35 micron CMOS technology. Furthermore fabricated to be a Chip.

1.3. PRIORITY OBJECTIVE AND RESEARCH URGENCEY

Primacy in the research is to open a new discourse in chip design that is able to change paradigm of the backwardness of indonesia in the chip industry to move ahead into state of chip designer on international scale. This is done by creating an A-ADC design on a single chip, also its development for SOC (System On Chip). Its fabrication plans are coordinated with leading research center institution in other countries, especially LEAD or LE2i Universite de Bourgogne France.

CHAPTER 2 STATE OF THE ART

2.1. ADC Architecture

Architecture of ADC, ADC (Analog to Digital Converter) is one of the main components in digital signal processing system. As he name implies ADC serves to convert analog signals (continuous) into digital signal (discrete). The process of digitalization is done through sampling and quantization. Sampling speed will determine the number of samples per unit time (seconds). While quantization determines resolution number of bits used to encode the value of each sample. With the continued development of high speed digital electronic devices that use analog data as its source, the role of ADC continues to increase [Song, et al, 2007][Cheongyuen, 2008]. Suppose on camera and radio frequency requires specification type of ADC having high speed and resolution. Shown in figure 2.1, grouping of several type of ADC technologies, namely Sigma Delta, SAR, Pipeline and Flash

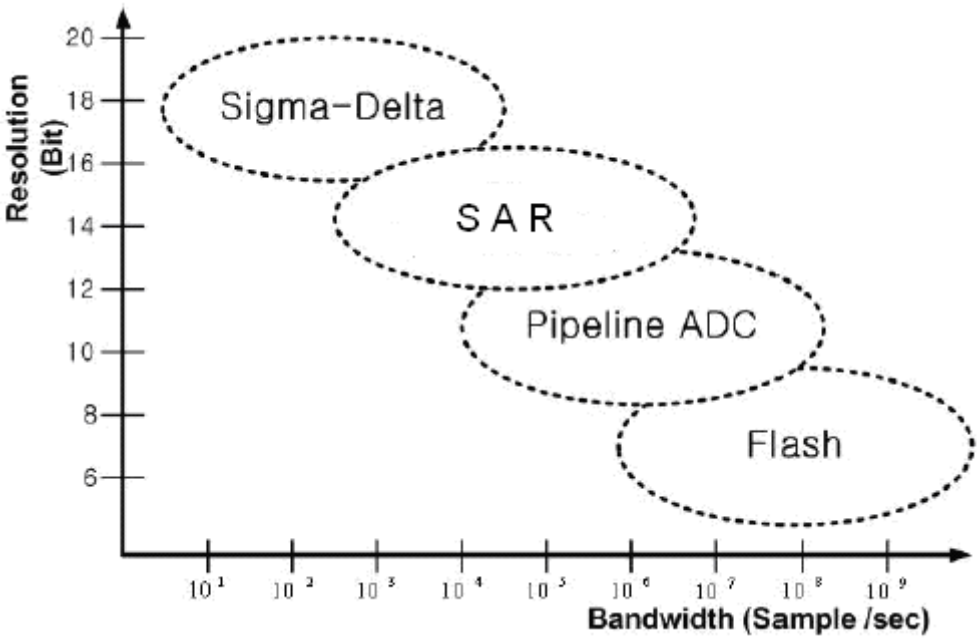


Figure 2.1. ADC Architecture Based on Resolution and Speed[Song, et al, 2007][Cheongyuen, 2008]

There are two types of an ADC architecture classification based on the sampling, namely over-sampling (sigma-delta) and Nyquist sampling (SAR, Pipeline and Flash)

shown in figure 2.2.

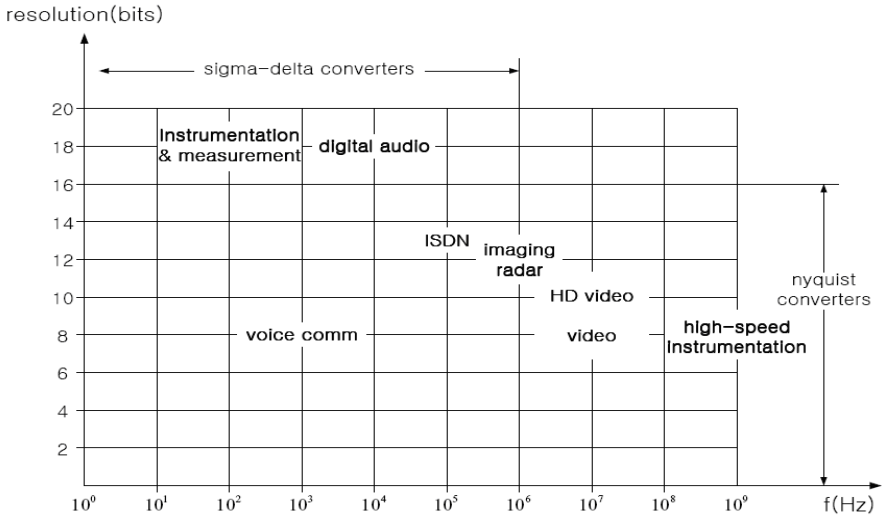


Figure 2.2. ADC Based on Resolution and Speed [Cheongyuen, 2008]

The working principle of SAR ADC type is shown in figure 2.3. When the input signal V(in) is being sample and hold, the comparator compares Vin with reference voltage (Vref), the comparator output (logic value 1) is used to open clock pulse gate to the SAR that contains the counter. The binary logic result of the of the counter is change into an analog voltage, when Vref = Vin the comparator is 0 and the clock pulse gate is closed, the result of this enumeration is proportional to the input signal (Vin). ADC of this type has a low speed and the application more on measuring equipment or istrumentation.

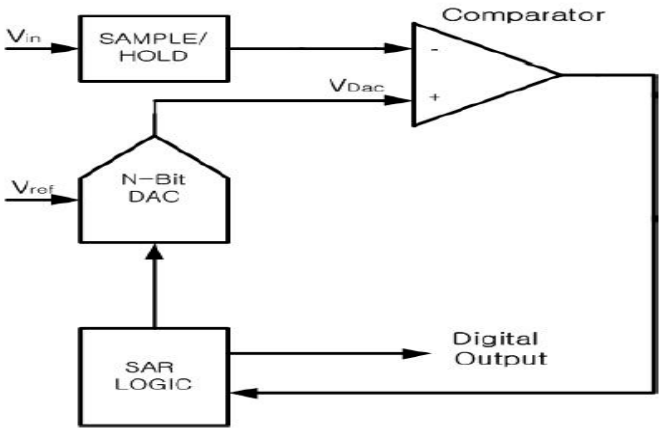


Figure 2.3. Type of SAR ADC [Song, et al, 2007]

The working principle of sigma delta ADC type is shown in figure 4. When the input signal summed with feedback of 1-bit DAC, the output is converted by the integrator into a triangular shape, by 1-bit ADC the signal is converted into serial digital bit stream, with digital decimator that contain filter and lowering sampling resulting digital serial output that is proportional to the input signal (Vin). This type of ADC is widely applied in audio equipment because it has a high resolution, but the drawback is low speed. The development of mixed technology designs, many kind of research in ADC is done in attempt to increase the speed so the ADC can be used for RF application.

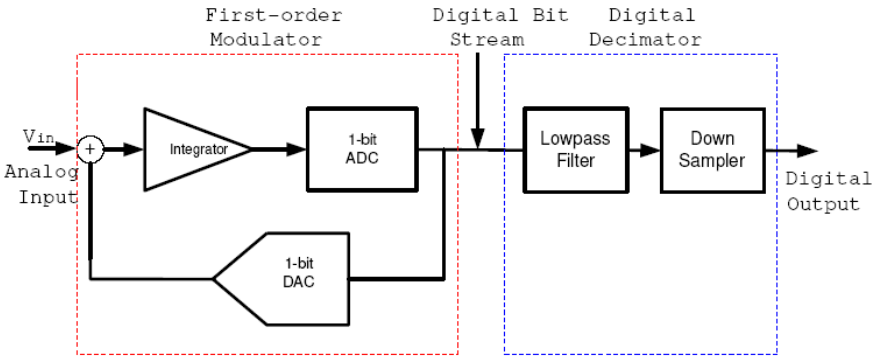


Figure 2.4. Type of Sigma Delta ADC[Song, et al, 2007]

The working principle of ADC on figure 2.5 requires many comparators as input voltage (Vin) comparator. The number of comparators used is 2^N-1(N is number of bits),for ADC with 8-bit output will require 255 comparators. Because the conversion process of paralle to the input more quickly, then the comparator output is adjusted with the decoder so that resulting digital binary output. This type of ADC applications are widely in digital video conversion process because it has high speed. The weakness of this AC is a large power dissipation and low resolution. Research on this ADC is continuing, one of which is folding method that reduces the number of comparators, while helping to reduce power dissipation and improve the resolution.

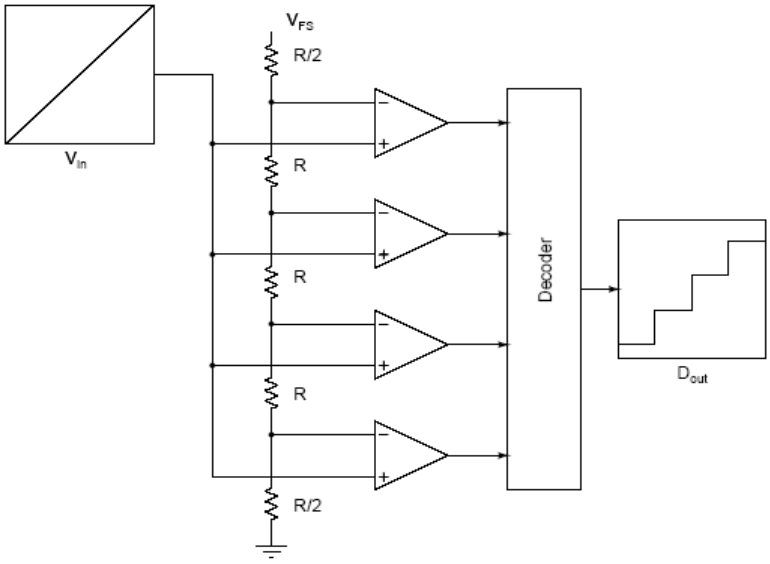


Figure 2.5. Flash Type of ADC [Song, et al, 2007]

The working principle of pipeline ADC in figure 2.6 applies pipeline process (cascade) with two phases (sample and multiplying). The process begin at the first stage, the input signal is compared to Vref by the comparator (ADC) and generate digital output MSB. The output is also used to control the function of Vref which is given in multiplying process (DAC), so it produce voltage residues (Vres) for the next stage. For example, the 8-bit digital output require 8 clock cascade proscess, with 7 full stage and 1 stage containing the ADC and the last stage is the LSB. This ADC applications are widely used in cameras and RF because it has high resolution and speed.

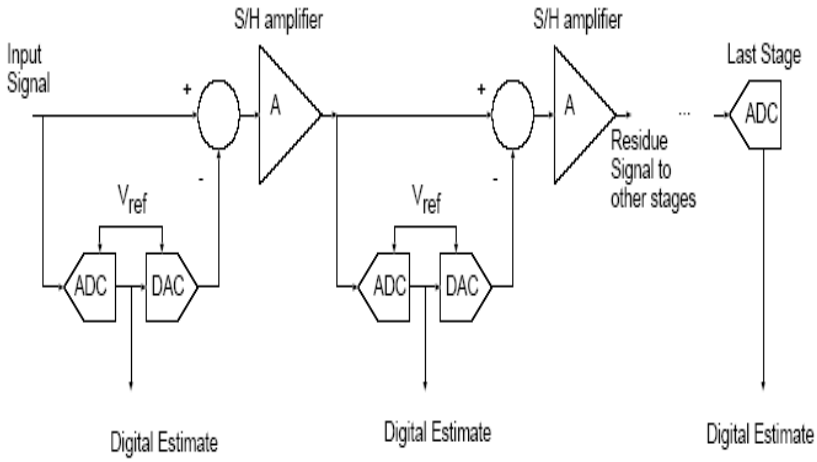


Figure 2.6. Pipeline ADC[Song, et al, 2007][Seung Chui, Jeon, & Kwon, June 2007]

Asynchronous ADC is a species with a Nyquist data sampling. This ADC is a new variant of ADC type. Its working principle is actually a modification of the SAR type ADC. Block diagram of A-ADC can be seen on figure 2.7.

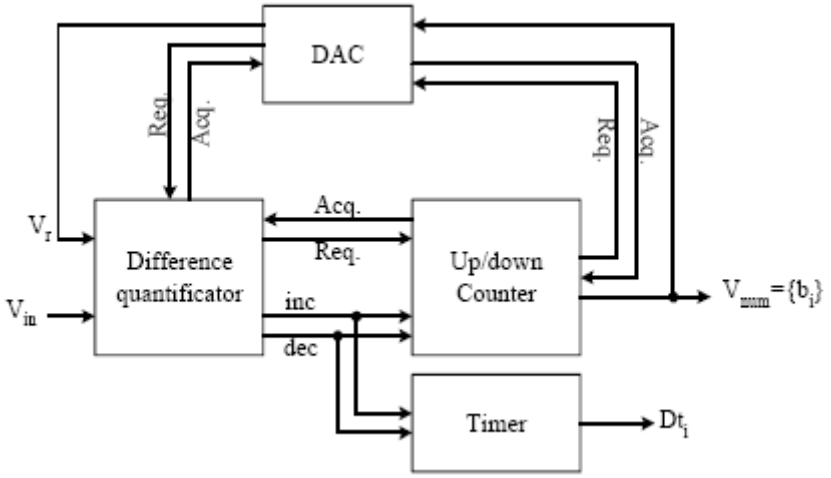


Figure 2.7. Asynchronous ADC[Allier, Goulier, Sicard, & Renaudin, 2005]

2.2 Reference of Asynchronous ADC Architecture

ADC architecture that is designed in this research is the development of asynchronous ADC architecture (A-ADC) designed by M. Trakimas where the main design is in the switch capacitor(SC)[Trakimas, Sonkusale, & Tufts, 2008]. Analog signal input will be captured by the SC is then compared to the signal or reference voltage. In addition, input signal SC also will get a signal from the decoder which is also a comparation of digital data signal from the previous signal. Figure 2.8 shows that all input control of analog signals will be process by capacitors and resistors that designed as switching. The function of the Op-Amp is to strengthen the signal in order to become the standard for digital data processing input.

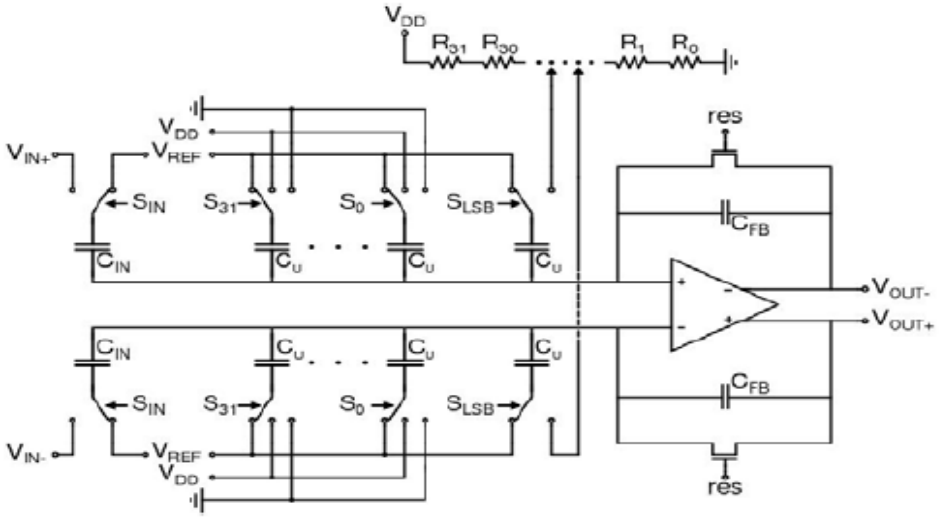


Figure 2.8. Switch Capasitor Architecture [Trakimas, et al, 2008]

Normaly, in amplification, occured ripple will be tempered by the capacitors and resistors that intalled as feedback on the amplifier[Tulabandhula & Mitikiri, 2009]. In digital data processing this research reducetheja Tulabandhula's research that use comparator as its main component.

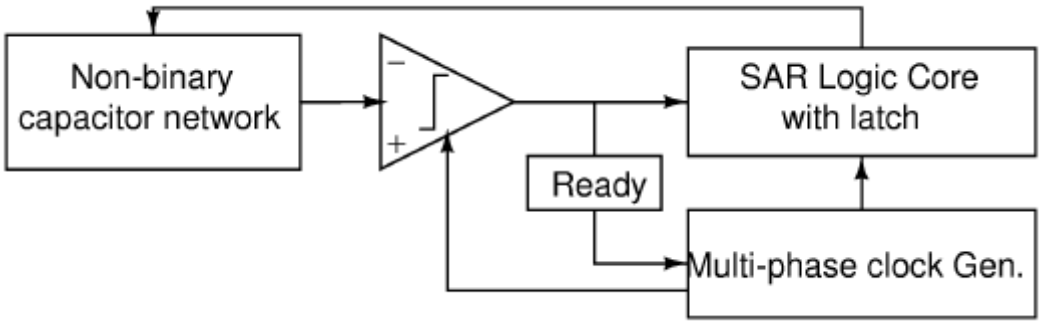


Figure 2.9. Single Comparator Digital Processing[Tulabandhula, et al, 2009].

Comparator-based digital data processing still use clock pulse that associated with main logic. This cause each part will wait each other when the signal is going to fed back. Because the per-bit-data is based on single comparator, it require a lot of power if need to be designed in 8 bits.

Overall design is refer to the research of Shuo-Wei who did the design of the ADC which require several clock generators for multi ADC reduce to 1 clock for type

ADC[Chen, member, IEEE, & Fellow, December 2006]. The block design is simple but the outside clock will cause actual ADC to be waiting each other to produce parallel signal.

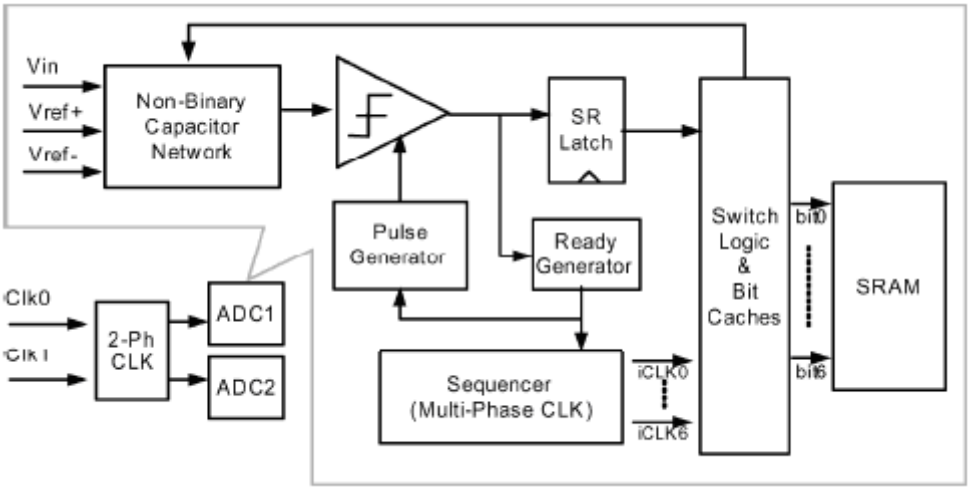


Figure 2.10. Block Diagram of Simple A-ADC[Chen, et al, 2006]

By looking at the advantages and the disadvantages of the previous research design, this research will produce an ADC Chip that has low power consumption, low voltage, high convertion speed, small delay, and large bits output.

CHAPTER III RESEARCH METHODS

Research activities of A-ADC Chip design will be held in 2 stages of research layout design and fabrication. Each phase is expected to take 1 year. The research stages are shown in figure 3.1.

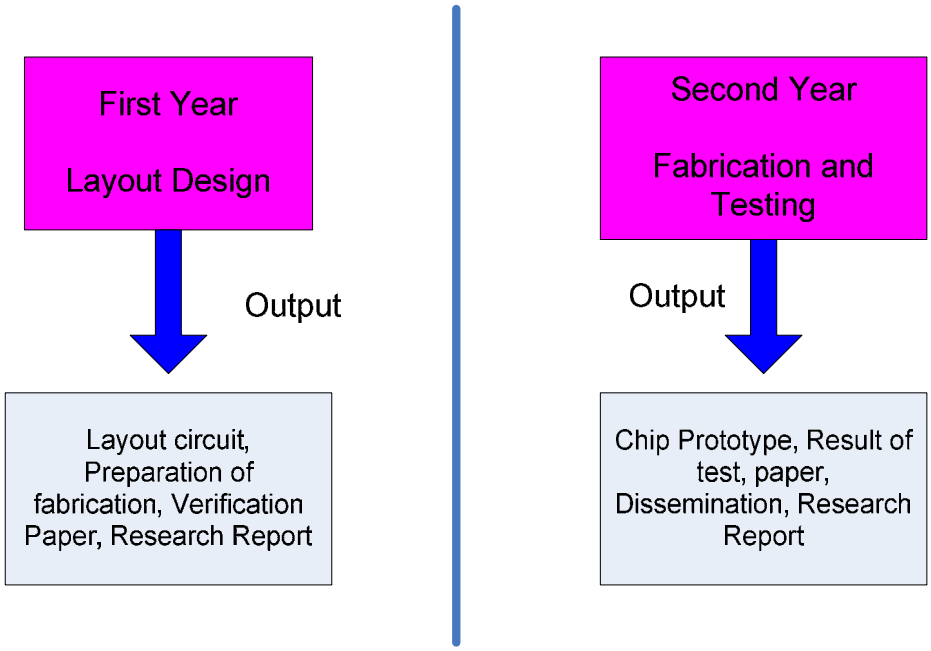


Figure 3.1. A-ADC Chip Research Method

The A-ADC layout which is resulted in the first stage will be fabricated in the second year research. A-ADC CHIP prototype is Final result of this research (second year).

3.1 Layout Design

After completing the design, verification, and simulation, the next step is to design the MOS composition and parameter of the A-ADC Chip that refer to the parameters generated in the schematic design. Our design is based on 0.35 µm technology from Austrian Micro System (AMS). Layout designed is also simulated in order to get the information of our design result before it fabricated. The results are also verified so that it is in accordance with the schematic design. Indicator of achievement of this stage is layout of A-ADC Chip that will be sent for fabrication. The process describe in figure 3.2.

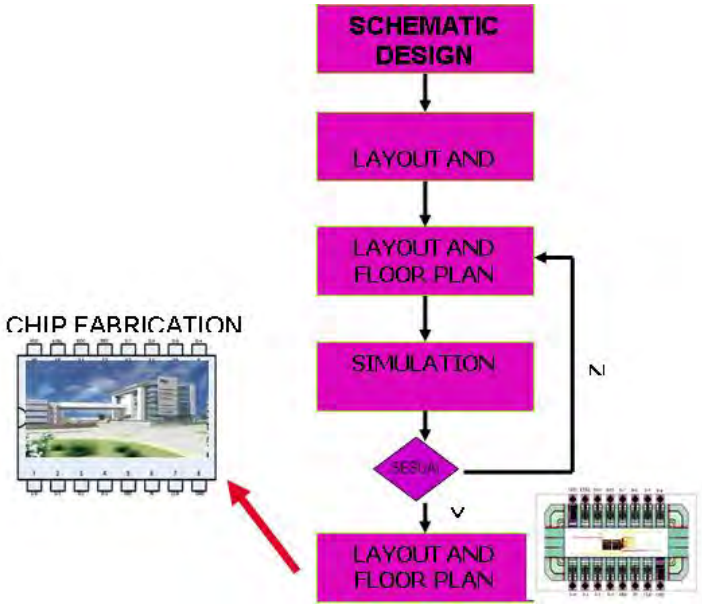


Figure 3.2. Layout Design Methodology

3.2 Fabrication

The layout result will be sent for fabrication that will produce the A-ADC Chip. Indicator of achievement of this stage is the A-ADC. Layout will be fabricated using the services of CMP-TIMA France, because we already existing MOU with them. Chip manufacturer profile can be seen in Figure 3.3

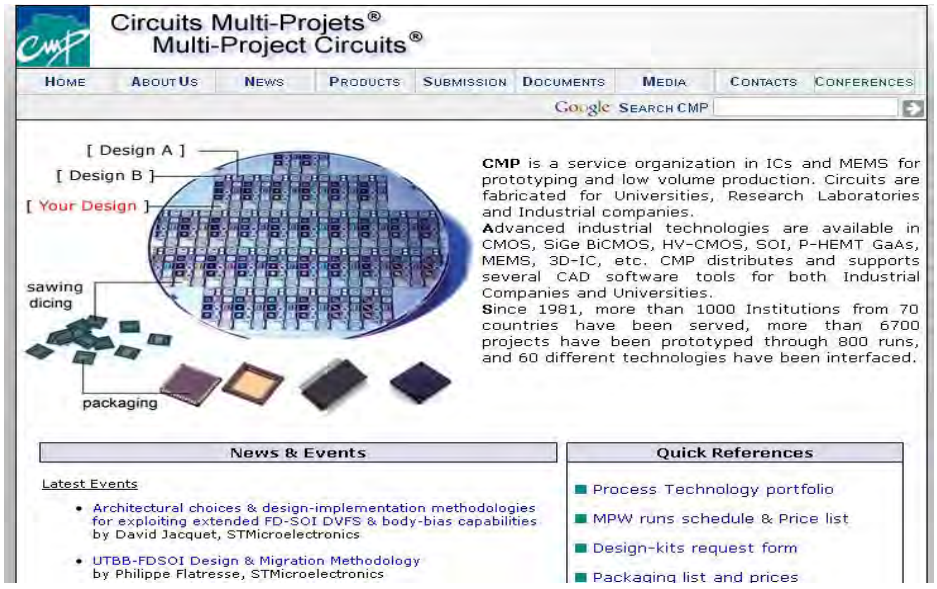
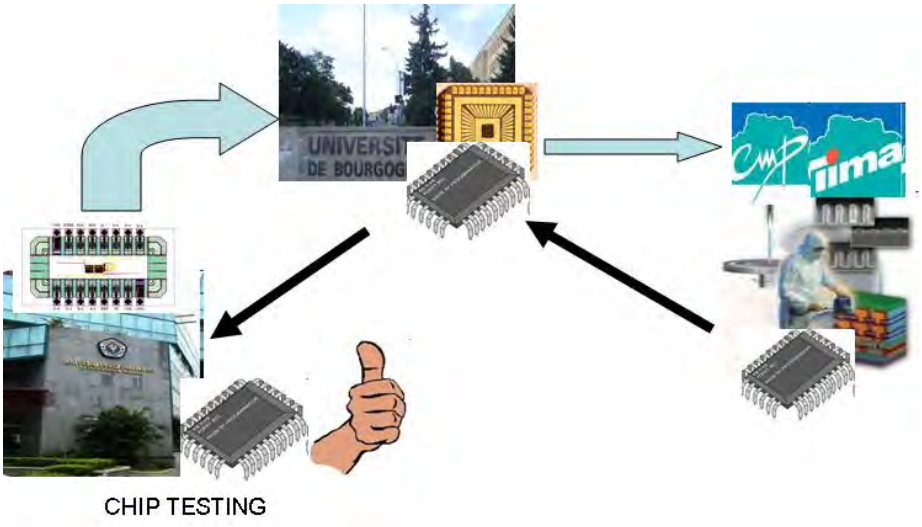


Figure 3.3. Chip Manufacturer Profile

To send a layout to the chip manufacturer is sending layout file in gds format using the File Transfer Protocol (FTP), so the file is guaranteed safe.

Delivery process in the form of the GDS layout via File transfert Protocol (FTP) that has been provided by the CMP-TIMA. Layout received and verified by the CMP-TIMA, if there are still errors then returned a file to Gunadarma , to be corrected, after corrected the file is sent back to the CMP-TIMA until the error disappeared. Chip-making process takes place from 2 to 3 months. After completion of the A-ADC chip prototype sent to Gunadarma for hardware verification and testing. Delivery process for the fabrication of the chip can be seen in figure 3.4.



Gambar 3.4. Proses pengiriman dan pembuatan purwarupa Chip A-ADC

CHAPTER IV BUDGETING AND RESEARCH SCHEDULE

4.1. Budgeting

No	Expenditure	The proposed Cost (Rp.)	
		First Year	Second Year
1.	Honorarium	60.000.000,-	60.000.000,-
2.	Materials	65.000.000,-	75.000.000,-
3.	Travelling	50.000.000,-	33.000.000,-
4.	ETC: data processing, report, publication, seminar	25.000.000,-	32.000.000,-
	Total	200.000.000,-	200.000.000,-

4.2. Schedule

No	**Activity**	**First Year**				**Second Year**			
1	Layout design and simulation								
2	Final layout check								
3	Sending layout to fabrication								
4	Waiting result fabrication								
5	Chip Testing								
6	Report								

REFERENCES

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Trakimas, M., Sonkusale, S., & T. U. (January 2008). A 0.8 V Asynchronous ADC Energy Constrained Sensing Aplications. (pp. 173-176). IEEE, CCIC.

Tulabandhula, T., & Mitikiri, Y. (2009). A 20MS/s 5.6 mW 6b Asynchronous ADC in 0.6 um CMOS. *IEEE VLSI Design , 2*, 111-116.

Wu, T. L. (2009). *Power Integrity and EMC Design for High Speed Circuit Packages.* IEEE.

APPENDIX

Appendix 1. Budgeting Justification

First Year

Expenditure	Detail of Expenditure	Unit	Total of unit	Unit price	Total Price	Sub Total
Honorarium						
	Head	Month	10	1,500,000	15,000,000	
	Member 1	Month	10	1,250,000	12,500,000	
	Member 2	Month	10	1,250,000	12,500,000	
	Asisten Disegner	Person	1	7,500,000	7,500,000	
	Administrasi	Person	1	7,500,000	7,500,000	
	Techniciant	Person	1	5,000,000	5,000,000	
					Sub Total	60,000,000
Materials						
	Mentor Graphics Software (lisensi 1 tahun)	paket	1	20,000,000	20,000,000	
	AMS Teknology 0,35 mikron Software	paket	1	10,000,000	10,000,000	
	Memory acceleration	Paket	1	10,000,000	10,000,000	
	Processor Acceleration	Paket	1	15,000,000	15,000,000	
	Board FPGA	Paket	1	10,000,000	10,000,000	
					Sub Total	65,000,000
Traveling						
	Transport	Overseas SeminarTrip	2	15,000,000	30,000,000	
	Akomodasi	Trip	2	10,000,000	20,000,000	
					Sub Total	50,000,000
ETC	Data Processing	Paket	1	10,000,000	10,000,000	
	Reoprt	Paket	1	5000000	5,000,000	
	Publication	Paket	1	5000000	5,000,000	
	Seminar	paket	1	5,000,000	5,000,000	
					Sub total	25,000,000
					T O T A L	**200,000,000.00**

Second Year

Expenditure	Detail of Expenditure	Unit	Total of unit	Unit price	Total Price	Sub Total
Honorarium						
	Head	Month	10	1,500,000	15,000,000	
	Member 1	Month	10	1,250,000	12,500,000	
	Member 2	Month	10	1,250,000	12,500,000	
	Asisten Disegner	Person	1	7,500,000	7,500,000	
	Administrasi	Person	1	7,500,000	7,500,000	
	Techniciant	Person	1	5,000,000	5,000,000	
					Sub Total	60,000,000
Materials						
	Mentor Graphics Software (lisensi 1 tahun)	paket	1	20,000,000	20,000,000	
	AMS Teknology 0,35 mikron Software	paket	1	10,000,000	10,000,000	
	Chip Fabrication	paket	1	45,000,000	45,000,000	
					Sub Total	75,000,000
Traveling						
	Transport Intl. Conf	Paket	1	15,000,000	15,000,000	
	Acomodation (hotel +meal)	Days	3	3,000,000	9,000,000	
	Intl. Conf. Registration	Paket	1	9,000,000	9,000,000	
					Sub Total	33,000,000
ETC						
	Data Processing	Paket	1	10,000,000	10,000,000	
	Reoprt	Paket	1	5000000	5,000,000	
	Journal Publication	Paket	1	10,000,000	10,000,000	
	Dessimination	paket	1	7,000,000	7,000,000	
					Sub total	32,000,000
					T O T A L	**200,000,000.00**

Appendix 2. Institution Supporting

UNIVERSITAS GUNADARMA

SK.No. 92/DIKTI/Kep/1996.
Fakultas Ilmu Komputer, Teknologi Industri, Ekonomi, Teknik Sipil & Perencanaan, Psikologi, Sastra.
Program Diploma (D3) Manajemen Informatika, Teknik Komputer, Akuntansi Komputer, Manajemen Keuangan dan Pemasaran ***Terakreditasi.***
Program Sarjana (S1) Sistem Informasi, Sistem Komputer, Teknik Informatika, Teknik Elektro, Teknik Mesin, Teknik Industri, Akuntansi, Manajemen, Teknik Arsitektur, Teknik Sipil, Psikologi, Sastra Inggris ***Terakreditasi.***
Program Magister (S2) Sistem Informasi, Manajemen, Teknik Elektro, Sastra Inggris, Psikologi, Teknik Sipil.
Program Doktor (S3) Ilmu Ekonomi, Teknologi Informasi / Ilmu Komputer.

SURAT PERNYATAAN PEMAKAIAN FASILITAS

Saya yang bertanda tangan dibawah ini :

Nama	:	Prof. Dr. E.S Margianti, SE, MM
NIDN	:	0303055403
Pankat	:	Rektor
Jabatan Fungsional	:	Guru Besar

Dengan ini menyatakan bahwa semua fasilitas lab, Internet dan ruang yang ada di Universitas Gunadarma yang terkait dengan penelitian saudara Prof. Dr. Busono Soerjowirjo dan Tim anggota yang berjudul " DESIGN AND IMPLEMENTATION OF ASYNCHRONOUS ANALOG TO DIGITAL CONVERTER (A-ADC) BASED ON CMOS TECHNOLOGY INTO A CHIP"

Bisa dipakai kapan saja dan tidak dipungut biaya apapun

.

Demikian pernyataan ini dibuat dengan sesungguhnya dan dengan sebenar-benarnya.

Depok, 4 February 2014

Menyetujui,
Rektor Universitas Gunadarma

(Prof. Dr. E.S. Margianti, SE, MM)
NIDN: 0303055403

Appendix 3. Working Organization

No	Nama/NIDN	Institution	Domain	Time Allocation (Jam/Minggu)	Task Force
1	Dr. Eri Prasetyo Wibowo /0331036604	Gunadarma University	Microelectronics	10	Coordination of activities, contact person with the chip manufacturer, approval and verification of the final result.
2	Prof. Dr. Boesono Soerjowirjo	Gunadarma University	System on Chip design	10	Circuit and layout design,simulation, Testing and trials Chips, international collaboration contact person
3	Dr. Joko Purnomo, ST, MT/ 0314097104	Gunadarma University	Electronics Engineering	10	Circuit and layout design,simulation, Testing and trials Chips

Appendix 4. Letter of Statement / MOU

RESEARCH COLLABORATION

AGREEMENT
Between
LEAD Universite de Bourgogne France
And
Center for Microelectronics & Image Processing Studies
Gunadarma Universite Indonesia

WHEREAS both parties, LEAD Universite de Bourgogne and Center for Microelectronics & Image Processing Studies Gunadarma University agree to collaborate in System on CHIP design research topics. The two Parties assigned researchers as listed below to execute the research mention. The research agreement will take forms as follow:

No	Organization	Researchers	Assignment
1.	LEAD Universite de Bourgogne	Prof. Dr. Michel Paindavoine	Supervisor and facilitator to chip fabrication
2.	Doctoral program of Information Technology Gunadarma University	Prof. Dr. Busono Soerjowirjo	Advisor and supervisor local university
3.	Center for Microelectronics & Image processing UG	Dr. Eri Prasetyo Wibowo	Coordinator and Supervisor SOCs design
4.	Electrical Engineering	Dr. Joko Purnomo	Designer SOCs

If necessary, this agreement will be subject to amendment as outlined in any addenda. LEAD Universite de Bourgogne and Center for Microelectronics & Image Processing Studies Gunadarma University will determine specific co-operative initiative jointly on an ongoing basis.

The parties confirm that the agreement took effect on the October 2013.

Prof. Michel Paindavoine
LEAD, Université de Bourgogne

Dr. Eri Prasetyo Wibowo
Center for Microelectronics & Images Processing Studies UG

COOPERATION AGREEMENT

Between

Université de Bourgogne, France

and

Gunadarma University, Indonesia

This agreement aims at promoting science and technology, strengthening human resource capability, and empowering its contribution to industries with special emphasis on Electronics, Computer Science and Image Technology applications.

1. Scope of Cooperation

i) Joint Research.

a. Université de Bourgogne : assists Research and Post-Graduate Program of Gunadarma University in the preparation of project proposals and in the initial implementation of joint research projects.

b. Université de Bourgogne and Gunadarma University apply jointly for research projects with relevant funding agencies, and suitable consultancy services as requested by industries in France and/or Indonesia.

ii) Staff and student exchange
Staff and student exchange include :

(1) Exchange of staff, to participate in and to assist the implementation of joint research projects.

(2) Exchange of students, to meet the requirement for completion of their study program.

iii) Post-Graduate Program
The Post-Graduate Program concerns the sector of Science and Technoloy in Information and Communication (STIC).

iv) Seminars
Université de Bourgogne and Gunadarma University conduct seminars jointly aiming at promoting science and technology and its applications for participants from universities, research institutions, and industries.

v) Other relevant matters
Other relevant matters as agreed by Université de Bourgogne and Gunadarma University will be carried out, such as professional short term training, publications, production of software, and design systems.

2. Work Plan and Funding

The mode of cooperative activities and the implementation of the work plan are based on annual actions, as agreed by both parties. The duration of this agreement is unlimited unless one of the parts decides to cancel the agreement. In this case the running program has to be accomplished to its end.
Université de Bourgogne and Gunadarma University contribute in so far as possible. Funding resources from external agencies needed to support cooperative activities, are considered important, they should be explored permanently and as a priority, throughout the implementation.

Each participating university tries to obtain grants for its students, during the study periods performed in the partner laboratory. These grants, however, should not be considered as mandatory.

It is agreed that the two contracting universities will accomplish the useful actions to obtain, as far as possible, the necessary funding to accomplish the present agreement, in particular :
- travel, salaries, accomodation of the specific staff working for this research project cooperation agreement,
- providing of research books, hardware and software equipment.

3. Duration of Cooperation

The duration of this agreement is unlimited unless one of the parts decides to cancel the agreement. In this case the running program has to be accomplished to its end.

4. Communications

Any notice, request, document, or other communication submitted by either Université de Bourgogne or Gunadarma University under this agreement will be in writing or by any available source of communication, at the following addresses :

Gunadarma University
Jalan Margonda Raya 100, Pondok Cina
Depok, 16424
Indonesia

Université de Bourgogne
Maison de l'Université
BP 27877
21078 Dijon Cedex
France

Dijon, September 17th 2002

Professor Dr. E.S. Margianti, SE,MM
Rector of Gunadarma University

Professor Dr. Bernard Laurin
President of Université de Bourgogne

Appendix 5. Researchers Curriculum Vitae

Head Researcher

I. IDENTITY

Nama Lengkap	Dr. Eri Prasetyo Wibowo, S.Si, MMSi
Jenis kelamin	Laki-laki
Jabatan Fungsional	Lektor Kepala
NIP/NIDN	920286 / 0331036604
Tempat dan Tanggal Lahir	Kendal, 31 maret 1966
Alamat Rumah	Perum Taman Puspa Kav. 120 Cimanggis Depok
Nomor Telp./Fax	021) 87715301 / (021) 7872829
Nomor HP	081380724028
Alamat kantor	Jl. Margonda Raya No.100, Depok 16424
Nomor telepon/fax	021) 78881112 / (021) 7872829
Alamat e-mail	eri@staff.gunadarma.ac.id
Lulusan yang telah dihasilkan	S1= 28 Orang, S2= 14 Orang, S3= 7 Orang
Matakuliah yang diampu	1. Analisa Sistem Komputer 2. Elektronika Lanjut (CMOS Desain) 3. Sistem Tertanam (Embedded System) 4. Perancangan Elektronika Berbantuan Komputer 5. Pemrograman Multimedia 6. Perancangan perangkat keras 7. Pengolahan Citra

II. Education Background

Program:	S1	S2	S3
Nama PT	Univ. Gadjah Mada, yogyakarta	Univ. Gunadarma Jakarta	Univ. Burgundy, France
Bidang Ilmu	Elektronika & Instrumentasi	Sistem Informasi	Elektronique Informatique
Tahun Masuk	1985	1993	2001
Tahun Lulus	1991	1995	2005
Judul Skripsi/Thesis/ Disertasi	Steam drum level control ammonia units in Asean Aceh Fertilizer Company	Design and developing information system software to control microcomputer assembly quality	Reconnaissance de visages : Vers une implantation sur silicium
Nama Pempimbing/ Promotor	Drs. Widodo Priyodiprodjo M.Sc, EE	Prof. Dr. Kudang Boro Seminar	Prof. Dr. Michel Paindavoine

III. Research Experience

No	Tahun	Judul Peneltian	Pen Danaan	
			Sumber	Jml (juta Rp)
1.	2009 (Ketua)	Pemodelan Arsitektur Jaringan Multi Processor Tertanam pada Chip Untuk Sistem Kamera Kecepatan Tinggi	HB Dikti	30
2.	2010 (Ketua)	Pemodelan Arsitektur Jaringan Multi Processor Tertanam pada Chip Untuk Sistem Kamera Kecepatan Tinggi	HB Dikti	30
3.	2010 (Anggota)	Sistem Pengenalan Individu Berbasis Potongan Iris Mata Sebagai Kunci Biometrik Pintu Otomatis Secara Real Time	HB Dikti	30
4.	2009	Sensor Kamera CMOS	UG- Univ. de Bourgogne, Prancis	300
5.	2008	Embedded analog CMOS Neural network Inside High Speed Camera	UG	20
6.	2007	Avoider Robot Design to DIM The Fire With DT-Basic Mini System	UG	10
7.	2007	Studi dan Analisa CMOS desain, pokok studi, ADC, Sensor CMOS	UG	7,5
8.	2006	Studi dan Analisa Lab. Elektronika desain	UG	4
9.	2011-2013 (Ketua)	DISAIN DAN IMPLEMENTASI (Fabrikasi) KONVERTER ANALOG KE DIGITAL PIPELINE KECEPATAN TINGGI BERBASIS TEKNOLOGI CMOS 0.35 µm	Penelitian Kompetensi Dikti	193
10.	2011- (Anggota)	TO DESIGN THE ANALOG TO DIGITAL CONVERTER (ADC) BY USING ASYNCHRONOUS METHOD AIMS AT PRODUCING ADC CHIP FOR VIDEO SIGNAL CONVERSION APPLICATION	Kerjasama dan Publikasi Internasional DIKTI	174

IV. Community Services

No	Tahun	Judul Pengabdian kepada masyarakat	Pen Danaan	
			Sumber	Jml (juta Rp)
1.	2007	Workshop " Disain Skematik, Layout dan Simulasi Dengan Mentor Graphics	UG	15
2.	2006	Student Programming Camp	UG, SUN	100
3.	2009-2011	ECAVOIRE Erasmus Mundus	Erasmus Mundus, UG	150
4.	2009	UG ICT Award 09	UG, SUN	200

			Megaswara	
5.	2008	Sosialisasi dan Pengetahuan TI bagi Masyarakat	Megaswara TV	10

V.a. Scientific Journals

No.	Tahun	Judul Artikel Ilmiah	Volume/ Nomor	Nama Jurnal
1.	Dec. 2010	Ocular Biometric System Focused on Iris Localization and Embedded Matching Algorithm	2/6	International Journal of Computer and Electrical Engineering **(IJCEE) Singapura**
2.	Jan. 2011	REAL TIME WARNING SYSTEM DESIGN FOR WEB DEFACE BASED ON SHORT MESSAGE SERVICE	23/1	Journal of Theoretical and Applied Information Technology (**JATIT**) **Pakistan**
3.	Feb. 2010	Modeling Harmonics Effects Elimination Using Active Filter On Unbalance Load Power System	62/1	International Journal of Word Academy Of Science, Engineering and technology, **Malaysia**
4.	Jan. 2009	Identifikasi Kebutuhan Model Sistem Informatika Kedokteran Universitas Gunadarma	36/1	Journal CDK
5.	April 2008	Teknik Cube Mapping Dengan OpenGL	4/1	Jurnal Teknologi Komputer Dan Informatika
6.	April 2006	Desain Sistem Pengenalan Wajah Dengan Variasi Ekspresi dan posisi Menggunakan Metode Eigenface	1/11	Informatika & Komputer
7.	2007	Mikrokontroler AT89S51TM sebagai Pengendali Pengiriman Informasi Kebakaran Melalui Telepon Seluler	1/3	UG Journal
8.	2007	Desain sistem Keamanan gedung Menggunakan Pendeteksi Gerakan dengan Sensor Infra Red	1/2	UG Journal
9.	April 2003	Konsep kamera CMOS : Pixel	1/8	Informatika dan Komputer
10.	Dec. 2003	DESAIN PENCACAH BINER 4-BIT MENGGUNAKAN PRESET RESET SEREMPAK DENGAN INPUT DATA VARIABLE	3/8	Journal Informatika dan Komputer
11	Maret 2011	Simulasi Prosedur Keselamatan Ketika Terjadi Kebocoran Gas LPG di Dalam Gedung Berbasis Serious Game	07/02/11	Jurnal Ilmiah Ilmu Komputer
12	Sep 2011	Designing and Implementing System of real Time Face detection and recognition based	Vol 01 issue 04	Asian transaction on Computers

		on RBF		
13	March 2012	Designing and Implementing Individual Identification System Based on Iris colors	Vol. 37 No. 1	JATIT Journal
14	Dec 2012	Design and Implemention of ADC Implanted in 10 000 frame/s High-Speed CMOS Sensor	Vol. 4, No. 6	IJCEE Singapura

V.a. Conference / proceedings

No.	Tahun	Judul Artikel Ilmiah	ISBN/ISSN	Nama Prosiding
1.	Dec. 2008	Design Space Exploration for a Custom VLIWarchitecture: Direct Photo Printer Hardware Setting using VEX Compiler Prosiding	978-7695-3493-0	SITIS08, Bali, Indonesia IEEE Computer Society
2.	June 2010	High Speed Asynchronous ADC In CAD Mentor Graphics AMS 0,35 µm CMOS	978-1-4244-7577-3	(ICSEM), Manila, Philipines
3.	May 2009	Real-Time Iris Recognition System Using A Proposed Method	978-0-7695-3654-5	IEEE Computer Society, Singapore
4.	July, 2009	Embedded analog CMOS Neural network Inside High Speed Camera	978-1-4244-4952-1	Prosiding ASQED, Malaysia
5.	Feb. 2010	Design Low Power 135mW Pipeline ADC With Speed 80 MSPS 8-bit		Prosiding ICESIT, Thailand
6.	April 2010	Concept and development of modular VLIW processor based on FPGA		ICSEM, Thailand
7.	Nov. 2010	Network Architecture Design Exploration and Simulation on High Speed Camera System using SynDEx		kicss2010, Thailand
8.	Dec. 2008	Development of Uclinux Platform for Computer Vision Algorithm in FPGA Devices	978-979-1223-66-9	Prosiding Wosoc 08, Bali, Indonesia
9.	Oct. 2009	Disain penguat OP-AMP dua stage untuk aplikasi ADC sigma delta dengan kecepatan tinggi menggunakan cmos teknologi 0,35 mikron	978-979-8689-12-3	Prosiding EIS 2009, Surabaya
10.	Nov. 2010	Perancangan Asinkron ADC Kecepatan Tinggi Menggunakan CMOS Teknologi AMS 0,35 µm	1411-6286	Prosiding KOMMIT 2010, Bali Indonesia
11	5-7 Nov	Design and implementation of non-	Proc. of SPIE Vol. 8558	Photonics Asia,

	2012	linear image processing functions for CMOS image sensor	85580O-1	Beijing 5-7 Nov 2012
12	19-20 Dec. 2012	A 8-bits ADC Design in AMS 0.35 µm CMOS Process for High Speed Communication System		ICNMED, Hongkong 19-20 dec. 2012
13	19-20 Dec. 2012	A Comparison Study of Three of Input Buffer Designed Using 0.35µm CMOS Technology		ICNMED, Hongkong 19-20 dec. 2012

VI. Book Writing

No.	Tahun	Judul Buku	Jumlah Halaman	Penerbit
1	2013	Konsep dan Disain ADC berbasis CMOS	450	Graha Ilmu
2	2011	Desain CMOS VLSI	157	Gunadarma Press
3	2007	Desain Skematik, Layout dan Simulasi dengan Menggunakan Perangkat Lunak Mentor graphics	110	Gunadarma Press
4	2006	Instalasi Mentor Graphics (IC Flow) pada sistem Operasi Linux	60	Gunadarma Press
5	1999	Dasar Fisika Energi	140	Gunadarma Press

VII. Intellectual Property

No.	Tahun	Judul /Tema HKI	Jenis	Nomor Pendaftaran/Sertifikat
1.	2012	Peubah analog ke digital kecepatan tinggi	Paten	Proses Pengajuan

Semua data yang saya isikan dan tercantum dalam biodata ini adalah benar dan dapat dipertanggungjawabkan secara hukum. Apabila di kemudian hari ternyata dijumpai ketidak-sesuaian dengan kenyataan, saya sanggup menerima risikonya.

Demikian biodata ini saya buat dengan sebenarnya untuk memenuhi salah satu persyaratan dalam pengajuan hibah Penelitian Kompetensi.

Depok, March 2014
Pengusul,

(Dr. Eri Prasetyo Wibowo, Ssi, MMSI)

Member of Researcher 1

I. Identity

Name : Busono Soerowirdjo, Prof., Ph.D

NIDN : 0301064401

Place/Date of Birth : Purworejo / June 1, 1944

Addess : Jl. Pintu Air I No. 12 RT/RW 07/08
Gandul, Limo, Depok, Jawa Barat 16512

Phone : +62217503400 / +628128240428

Email : busono@staff.gunadarma.ac.id

II. Education Background

Year	Degree	Field	University
1983	Ph.D	Microelectronics	Southampton University, England
1975	M.Sc	Elektronika	Southampton University, England
1972	B.Sc	Electrical Engineering	Institut Teknologi Bandung, Indonesia

III. Scientific Experience

No	Tahun	Judul Peneltian	Pen Danaan	
			Sumber	Jml (juta Rp)
1.	2009	Sensor Kamera CMOS	UG- Univ. de Bourgogne, Prancis	300
2.	2008	Embedded analog CMOS Neural network Inside High Speed Camera	UG	20
3.	2007	Avoider Robot Design to DIM The Fire With DT-Basic Mini System	UG	10
4.	2007	Studi dan Analisa CMOS desain, pokok studi, ADC, Sensor CMOS	UG	7,5
5.	2006	Studi dan Analisa Lab. Elektronika desain	UG	4
6.				
7.	2011- (Ketua)	TO DESIGN THE ANALOG TO DIGITAL CONVERTER (ADC) BY USING ASYNCHRONOUS METHOD AIMS AT PRODUCING ADC CHIP FOR VIDEO SIGNAL CONVERSION APPLICATION	Kerjasama dan Publikasi Internasional DIKTI	174

IV. Work Experience

Period	Position	Institution
2009 -	Director of Doctorate Programmes	Gunadarma University
2007 -	Member of National Accreditation on Board for Higher Education (BAN-PT)	
1999 -	Senior Lecturer	Gunadarma University
1996 – 1998	CEO	PT Citra Hagen Utama
1986 – 1996	Supervisor of Telecommunication Group	Mobil Oil Indonesia. Inc
1984 - 1986	Head of Research Center for Electronics Devices	LEN-LIPI (National Electronics and Electrical Research Institute
1972 – 1979	Head of Electronics and Electrical Devices Laboratory	LEN-LIPI
1967 – 1972	Technician in Telecommunication and Electronics Laboratory	LEN-LIPI

V. Research and Publications

Title	Year	Article/Proceeding
Implementasi Sandi Hill dalam pembuatan Program aplikasi penyandian citra	2007	Majalah Ilmiah Matematika dan Komputer, Jilid 23,No.1, p.1-8, April 2007, Gunadarma University, Jakarta.
Perancangan aplikasi Sistem Informasi Geografis untuk perangkat bergerak	2007	Jurnal Ilmiah Informatika dan Komputer, Jilid11, No.3 pp.164-169, Desember 2007, Gunadarma University, Jakarta.
Analisis Sistem Keamanan Bluetooth	2007	Jurnal Ilmiah Informatika dan Komputer, Jilid 11 No.2, p122-131, Agustus 2006, Gunadarma University, Jakarta.
Kinerja 2 tipe transistor bipolar dengan emitter dari bahan polysilicon	2004	Proc. KOMMIT, pp. 824-829, 2004.
Sistem Informasi Geografis penyebaran terumbu karang Kepulauan Seribu	2004	Proc. KOMMIT, pp. 378-384, 2004.
Metoda dua temperatur untuk mengukur resistansi basis dari transistor	2004	Proc. KOMMIT, pp. 819-823, 2004
Pembersih ruangan dari asap rokok	2004	Proc. KOMMIT, pp. 815 -818, 2004

melalui ruang ionisator		
Perancangan permintaan melalui SMS terhadap layanan perpustakaan Universitas Gunadarma	2004	Proc. KOMMIT, pp. 121- 128, 2004.
Pemonitoran traffic pada jaringan komputer Universitas Gunadarma	2004	Proc. KOMMIT, pp. 596 - 599, 2004
Comparison of experimental and theory results on polysilicon emitter bipolar transistors	1984	IEEE Trans. Electron Devices, vol. ED-31, pp.853 – 860, 1984
Experimental results of polysilicon emitter bipolar transistors	1983	Proc. 13th ESSDERC, Kent, UK, 1983
TEM and RBS studies of the regrowth of arsenic implanted polysilicon due to oxidation drive-in	1982	International Colloquium on Polycrystalline Semiconductors, University of Perpignan, France, Sept 1982.
The influence of surface treatments on the electrical characteristics of bipolar transistors with polysilicon emitters	1982	IEDM Tech.Digest., paper 28.1, San Fransisco, USA 1982.
Computed and experimental results on polysilicon contact emitter in bipolar transistors	1982	Proc. 12th ESSDERC, Munich, Germany 1982
Effects of surface treatments on the electrical characteristics of bipolar transistors with polysilicon emitters	1982	Solid State Electron., vol.26, pp.495 – 901, 1982.
Polysilicon emitters for bipolar transistors	1981	IOP Conference on New Forms of Silicon for use in Semiconductor Devices, London, 1981
Arsenic profiles in bipolar transistors with polysilicon emitters	1981	Solid State Electron., vol.24, pp.475-480, 1981
Electrical properties and doping profiles of transistors with polysilicon emitters	1980	Proc. 10th ESSDERC, York, UK, 1980

Jakarta, January 30, 2014

(Busono Soerowirdjo, Prof., Ph.D)

Member of Researcher 2

I. IDENTITY

Nama Lengkap	Dr. Joko Purnomo, ST, MT
Jenis kelamin	Laki-laki
Jabatan Fungsional	Lektor
NIP/NIDN	950585/0314097104
Tempat dan Tanggal Lahir	Klaten, 14 September 1971
Alamat Rumah	Perum Bukit Waringin B3/24, Kedung Waringin, Bojong Gede, Bogor
Nomor Telp./Fax	
Nomor HP	08159975989
Alamat kantor	Jl. Margonda Raya No.100, Depok 16424
Nomor telepon/fax	021) 78881112 / (021) 7872829
Alamat e-mail	jokopurn@staff.gunadarma.ac.id
Lulusan yang telah dihasilkan	S1= 11 Orang
Matakuliah yang diampu	1. Sistem Operasi 2. Organisasi sistem Komputer 3. Arsitektur Komputer 4. Mikroprosesor 5. Jaringa Komputer 6. Teknologi Semikonduktor

II. Education Background

Program:	D3	S1	S2	S3
Nama PT	Univ. Gadjah Mada, yogyakarta	Univ. Gunadarma Jakarta	Univ. Gunadarma Jakarta	Univ. Gunadarma Jakarta
Bidang Ilmu	Teknik Elektro	Teknik Elektro	Device Elektronika	Teknologi Informasi
Tahun Masuk	1990	1996	1999	2007
Tahun Lulus	1995	1998	2001	2011
Judul Skripsi/Thesis/ Disertasi	Pencatat Data Elektronik Dengan Mikrokontroller 68HC11	Perekam Suara Elektronik	Perekam Suara Elektronik dengan ADC Sigma Delta	Disain Pengubah Analog ke Digital (ADC) Jenis Asynchronous Berbasis Teknologi 0,35 um CMOS Proses
Nama Pempimbing/ Promotor	Ir. Teguh Santosa	Drs. Soebiyantoro. M. Eng	Prof. Boesono Soerowiryo Ph. D	Prof. Boesono Soerowiryo Ph. D

IV. Scientific Article

No.	Tahun	Judul Artikel Ilmiah	Nama Kegiatan	Tempat
1.	2008	PERANCANGAN ASINKRON ADC	KOMIT	Denpasar

		KECEPATAN TINGGI MENGGUNAKAN TEKNOLOGI AMS 0,35 µm		
2.	11-12 Juni 2010	HIGH SPEED ASYNCHRONOUS ADC IN CAD MENTOR GRAPHICS AMS *0,35 µm CMOS*	International Conference on Networking and Information Technology	Manila Pilipina
3.	21 Oktober 2009	DISAIN PENGUAT OPERASIONAL (OP-AMP) DUA STAGE UNTUK APLIKASI ADC SIGMA-DELTA) **(ΣΔ)** DENGAN KECEPATAN TINGGI MENGGUNAKAN CMOS TEKNOLOGI AMS 0,35 µm	Industrial Electronics Seminar' (IES) 2009	EEPIS-ITS, Surabaya
4.	5 Agustus 2009	DISAIN PENGUAT OPERASIONAL (OP-AMP) DUA STAGE UNTUK APLIKASI ADC PIPELINE DENGAN KECEPATAN TINGGI MENGGUNAKAN CMOS TEKNOLOGI AMS 0,35 µm	Seminar Nasional Teknik Industri (SNTI)	Universitas Sultan Agung, Semarang
5.	19-20 Dec. 2012	A 8-bits ADC Design in AMS 0.35 µm CMOS Process for High Speed Communication System		ICNMED, Hongkong 19-20 dec. 2012

Semua data yang saya isikan dan tercantum dalam biodata ini adalah benar dan dapat dipertanggungjawabkan secara hukum. Apabila di kemudian hari ternyata dijumpai ketidak-sesuaian dengan kenyataan, saya sanggup menerima risikonya.

Demikian biodata ini saya buat dengan sebenarnya untuk memenuhi salah satu persyaratan dalam pengajuan hibah Penelitian Kompetensi.

Depok, Desember 2013
Anggota Pengusul,

(Dr. Joko Purnomo)

Appendix 6. Research Origininality Statement

UNIVERSITAS GUNADARMA

SK. No. 92/DIKTI/Kep/1996
Fakultas Ilmu Komputer, Teknologi Industri, Ekonomi, Teknik Sipil & Perencanaan, Psikologi, Sastra
Program Diploma (D3) Manajemen Informatika, Teknik Komputer, Akuntansi Komputer, Manajemen Keuangan dan Pemasaran ***Terakreditasi***
Program Sarjana (S1) Sistem Informasi, Sistem Komputer, Teknik Informatika, Teknik Elektro, Teknik Mesin, Teknik Industri, Akuntansi, Manajemen, Arsitektur, Teknik Sipil, Psikologi, Sastra Inggris ***Terakreditasi***
Program Magister (S2) Sistem Informasi, Manajemen, Teknik Elektro, Sastra Inggris, Psikologi, Teknik Sipil
Program Doktor (S3) Ilmu Ekonomi, Teknologi Informasi / Ilmu Komputer.

SURAT PERNYATAAN KETUA PENELITI

Saya yang bertanda tangan dibawah ini :

Nama	: Dr. Eri Prasetyo Wibowo
NIDN	: 0331036604
Pangkat/Gol.	: -
Jabatan Fungsional	: Lektor Kepala

Dengan ini menyatakan bahwa proposal penelitian saya dengan judul:
DESIGN AND IMPLEMENTATION OF ASYNCHRONOUS ANALOG TO DIGITAL CONVERTER (A-ADC) BASED ON CMOS TECHNOLOGY INTO A CHIP

yang diusulkan dalam skema Kerjasama Luar Negri dan Publikasi Internasional untuk tahun anggaran 2015. bersifat original dan belum pernah dibiayai oleh lembaga / sumber dana lain.

Bilamana di kemudian hari ditemukan ketidaksesuaian dengan pernyataan ini, maka saya bersedia dituntut dan diproses sesuai dengan ketentuan yang berlaku dan mengembalikan seluruh biaya penelitian yang sudah diterima ke kas negara.

Demikian pernyataan ini dibuat dengan sesungguhnya dan dengan sebenar-benarnya.

Depok, 4 Maret 2014,

Mengetahui,

Ketua lembaga Penelitian

(Dr. Ir. Hotniar Siringoringo M.Sc)
0309116501

Yang Menyatakan

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(Dr. Eri Prasetyo Wibowo)
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Jl. Margonda Raya 100 Depok 16424 Telp. (021) 78881112, 7863788, Jl. Akses Kelapa Dua Cimanggis Telp. (021) 8719525, 8727541, Email : sektor@gunadarma.ac.id