A 64-channel, 1.1-pA-accurate On-chip Potentiostat for Parallel Electrochemical Monitoring

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***Abstract*—Electrochemical monitoring is crucial for both industrial applications, such as microbial electrolysis and corrosion monitoring as well as consumer applications such as personal health monitoring. Yet, state-of-the-art integrated potentiostat monitoring devices have few parallel channels with limited flexibility due to their channel architecture. This work presents a novel, widely scalable channel architecture using a switch capacitor based Howland current pump and a digital potential controller. An integrated, 64-channel CMOS potentiostat array has been fabricated. Each individual channel has a dynamic current range of 120dB with 1.1pA precision with up to 100kHz bandwidth. The on-chip working electrodes are post-processed with gold to ensure (bio)electrochemical compatibility.**

I. Introduction

Parallel, accurate electrochemical monitoring is crucial for high-throughput and/or widely variable applications in the industrial and consumer fields. To study individual electrochemical half reactions, a potentiostat architecture with a 3-electrode setup is used [1]. For the development of novel microbial electrochemical reactors, multichannel potentiostats allow to tune the electrical settings optimally with flexible stimulation patterns, irrespective of the natural statistical variation of the microorganisms or the environment dynamics [2]. Similarly, for the study of novel anti-corrosion coatings, a very slow aging process, parallelization notably speeds up those experiments [3]. For personal healthcare monitoring, various biomolecules act as electrochemical transducers. As such, a multichannel on-chip potentiostat can assess the impact of different chemicals simultaneously [4] at low cost.

Current SotA parallel on-chip potentiostats focus mostly on parallelizing the readout circuitry, by measuring the current of each individual channel while keeping the potential equal for all channels. As such only a single, analog potential controller is required. In [5], an active microelectrode array (MEA) for DNA analysis is presented with 16 parallel readout channels. Using a more advanced circuit architecture, [6] expanded the number of parallel readout channels to 1024 with 93dB dynamic range. Yet, both have only a single stimulation unit. While this is sufficient for studying the spatial effects of electrochemical reactions, a truly parallel stimulation and sensing potentiostat with large dynamic range is required for monitoring those high-throughput and/or widely variable processes.

In [7], a multi-functional MEA is presented with 59760 electrodes and 2048 parallel readout channels. The number of independent stimulation units is expanded to 16. In [8] the multiplexed cyclic voltammetry with 16 parallel independent stimulation and sensing potentiostats is further investigated.

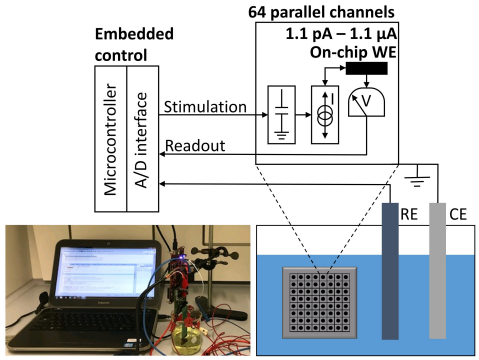

Fig. 1. System overview

Further expanding the amount of independent potentiostats operating simultaneously is however challenging for the SotA architectures due to the limited chip input/output pin numbers. Moreover, the largest dynamic range of the current sensing unit in SotA designs is below 100dB. Therefore, in this paper a current stimulation structure is used with a boosted dynamic range. The potentiostat control is maintained by the digital feedback loop running on an external microcontroller. The lift-off process used to pattern electrodes on chip can be modified in order to improve the process yield. Compared to the SotA designs, this paper therefore introduces the following novelties: 1) a scalable multiplexing architecture resulting in 64 independent stimulation channels with only a single input pin and a single output pin, and fully software-programmable control with an arbitrary waveform; 2) a switch capacitor based current pump with bipolar output, 120dB wide dynamic range, and 1.1pA resolution; 3) a post-processing technique with thick metal and an extra protection layer to pattern on-chip working electrodes (WEs).

This paper is structured as follows: First, section II introduces the channel architecture. The circuit implementation is discussed in section III. Next, section IV details the post-processing steps to pattern the electrodes. Finally, section V presents the electrical measurement and chemical cyclic voltammetry results.

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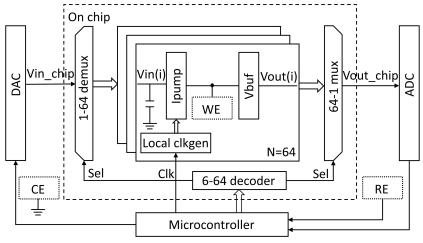


Fig. 2. Channel multiplexing architecture

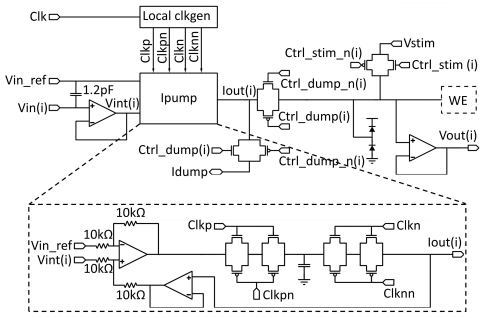


Fig. 3. Schematic of a single channel

II. System architecture

The 64-channel potentiostat consists of three parts: the multiplexing architecture, the bipolar current-stimulation/voltage-sensing potentiostat channel and the on-chip working electrode, shown in Fig. 1. They are discussed below.

A. Multiplexing architecture

A flexible, scalable multiplexing architecture is shown in Fig. 2. A digital controller is used to close the feedback loop. Only one input/output pair together with a single external ADC/DAC is required to control all channels using time-division multiplexing.

Through the selection signal *Sel*, driving the 1-64 multiplexer and 64-1 demultiplexer, each channel can be selected individually. As such, the ADC can sense the output voltage of each channel, and send it to an off-chip, low-cost microcontroller (TI TMS320F28379D). The microcontroller runs a digital proportional-integral (PI) controller to maintain the output potential of each channel equal to a set-point by stimulating the channel's current. The set-point potential can be time-varying, represented by a fully-programmable waveform.

A capacitor at the input of every channel stores the channel-specific current-stimulation input signal when the channel is not selected. In this way, all 64 channels are stimulated simultaneously with only one input pin. The interface between the digital controller and the analog chip is composed of a single 12-bit, 250-kS/s ADC and DAC. This scheme is easily scalable to a large number of channels by increasing either the storage capacitor size or the mixed-signal sample rate.

B. Potentiostat channel

This work applies a current stimulation, voltage measurement architecture. The channel schematic is shown in Fig. 3. A Howland current pump is implemented with a switch capacitor topology. Such scheme has the benefit of a large dynamic current range, because the value of the equivalent resistor of a switch capacitor is inversely proportional to the tunable switch clock frequency. All channels share the same switch capacitor clock to set the coarse output range. The input voltage of the current pump is channel-specific and used for output fine-tuning.

C. On-chip working electrode

The working electrodes are integrated on chip to allow a wide parallelization. The top metal layer of the non-processed chip is aluminum (Al). As Al is not electrochemically stable, each electrode receives a biocompatible gold (Au) coating during post-processing.

III. Circuit level design

The chip is designed in 180nm technology with 3.3V supply. Each channel consists of a memory capacitor, an output voltage buffer (Vbuf) and a bipolar current pump (Ipump).

The memory capacitance value of 1.2pF limits the voltage drop to be less than 1mV when cycling through all 64 channels while have no impact on the required bandwidth.

In order to run a complete cyclic voltammetry with sufficient accuracy, the targeted voltage sensing swing is set to 2V and the targeted resolution is 1mV. The output voltage measurement unit is implemented with an opamp in unity feedback. A rail-to-rail configuration [9] is adopted to maximize the swing without adding much extra area.

A modified Howland current pump is used to provide the wide-dynamic bipolar currents [10]. The current pump uses two opamps, four 10kΩ resistors and one tunable resistor (R_tune), generating a bipolar current $Iout = (Vin - Vin\_ref)/R\_tune$. The first opamp together with all the resistors generates a differential bipolar current while the second opamp isolates the output load from the internal resistors.

The tunable resistor (R_tune) is implemented with a switch capacitor ($R = 1/fC$), which results in a large dynamic range by adjusting the switch clock frequency. For the switch capacitor, a 100fF small capacitor C is chosen to achieve an extremely large equivalent resistor and as such a very low minimal current resolution. The switches are implemented as transmission gates to maximize the output swing. The switch size is minimized to reduce the clock feedthrough which decreases the output accuracy. Additional switches are added in series to decrease the static leakage. Non-overlapping clocks are locally generated to prevent leakage during switching.

During simulation, the output resistance of the current pump is about 20 times larger than R_tune, leading to a wide load range. 10% accuracy can be achieved at 500fA output current

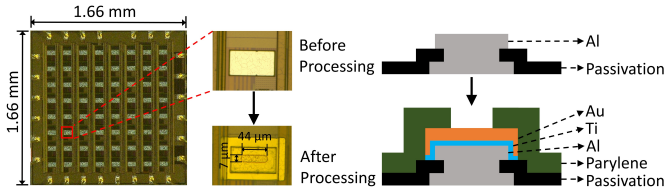
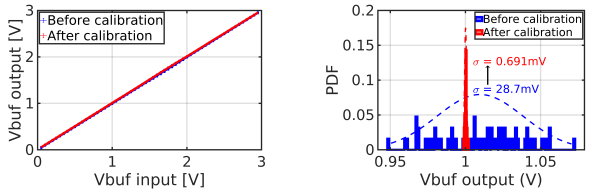
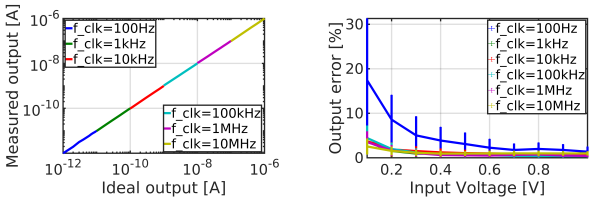


Fig. 4. Chip die photograph and post-processing



(a) (b)

Fig. 5. Vbuf DC output (a) and distribution at 1V input (b) before and after calibration



(a) (b)

Fig. 6. Ipump DC output (a) and error after calibration (b)

(50mV input, 100Hz clock frequency). The thermal noise is not an issue since the current pump bandwidth is coupled to the switch clock frequency and shrinks in proportion with the current range.

To decouple the current pump from the memory capacitor, an input voltage buffer stage is added. For testing purposes, additional transmission gates are inserted between the current pump and the voltage buffer.

IV. Post-processing

The biocompatible interface between the chip and a (bio)chemical solution is achieved by patterning Au on top of each Al electrode. It was found that the surface of the Al bond pad is not sufficiently flat, especially at the edges. A process is designed to overcome this issue, which consists of a) gluing the diced chip on a supporting wafer, together with surrounding dummy chips; b) applying and patterning a two-layer liftoff resist stack; c) sputtering 100nm Ti as thick diffusion barrier and then a thick Au layer (400nm); d) dissolving the liftoff resist; e) depositing 5μm of Parylene C; f) patterning the Parylene by lithography and oxygen plasma. Photoresist exposure was done using direct laser writing.

An electrode after post-processing is shown in Fig. 4. The extra Parylene step provides a protection on the Al electrode edges. To further prevent possible Al corrosion at the edge after Au deposition, an edge-shifted pattern is used: The Ti/Au layer is patterned with 15μm extra margin at each side on top of the Al electrode, while the Parylene opening shrinks with 35μm at each side on top of the Ti/Au pattern. The final WE area is $7\times44\mu m^2$.

With the improved process, not all Al electrodes are completely covered with Au due to the bond pad surface topography. New processes are being investigated to completely solve this issue.

V. Measurement results

The chip is first measured electrically before post-processing, and then electrochemically after post-processing.

A. Electrical measurements

1) Voltage sensing: The DC output error of the voltage buffer is measured and calibrated through a two-point calibration: From two consecutive measurement points, a 2-coefficient fitting (gain and offset compensation) is done to calculate the voltage buffer input corresponding to the expected output. Then the output is measured again with compensated input and compared with the expected value. Fig. 5 shows the voltage buffer output before and after calibration.

2) Current stimulation: The current pump DC output is measured through the voltage across an external resistor (from 100kΩ to 1GΩ). The wide range from 1pA to 1μA for one channel is shown in Fig. 6a, with maximum 0.35% nonlinearity. The output current is configurable by both the clock frequency and the input voltage.

A similar calibration procedure is used to calibrate all 64 channels. The post-calibration error is below 10% except in the pA range output (100Hz clock frequency), where the maximum post-calibration error equals 31%, as shown in Fig. 6b. This error is much larger than simulation (<1%), probably caused by the insufficient measurement setup isolation. Note that only the positive current output is shown, as similar measurements were obtained for the negative current.

The output resolution with the current measurement set-up is evaluated from the measured noise over the system time constant (∼1s for 100Hz clock), resulting in 1.14pA. The 1.1μA measured maximum current is limited by the maximum allowed switch-capacitor clock frequency, set by the opamp bandwidth.

3) Closed loop system: The system bandwidth needs to be sufficiently large in order to run dynamic measurements. The transfer function of the system is measured with a dummy load resistor. The current pump input and the voltage buffer output are connected to the network analyzer. The external microcontroller is not taken into account because it operates at a fast clock (200MHz). The results with different clock frequencies are shown in Fig. 7. 117kHz bandwidth is achieved with 10MHz clock frequency and 1Hz bandwidth can be extrapolated for the 100Hz clock or 1∼10pA operation. However, the measured bandwidth is actually limited by the load resistor and it is not possible to use smaller load resistors

TABLE I
STATE-OF-THE-ART COMPARISON

Reference	JSSC-08 [5]	JSSC-17 [7]	TCAS-18 [8]	ISSCC-19 [6]	**This work**
CMOS fabrication technology[μm]	0.25	0.18	0.35	0.25	**0.18**
Chip area[mm^2]	5×3	10.1×7.6	3.79×3.79	7×9	**1.66×1.66**
WE size[μm^2]	70×70∼100×100	3×7.5	20×20	∼30×30	**7×44**
Number of WE	16	59760	256	1024	**64**
Number of independent channels	1	16	16	1	**64**
Imax[μA]/Sensitivity[pA]	0.11/240	∼1/1000	13/1390	0.0125/0.28	**1.1/1.1**[1]
Current dynamic range[dB]	53.2	∼60	82.6	93	**120**
Measured voltage swing[V]	1.25	1.0	5.2	1.5	**2.5**
Bandwidth[Hz]	10k	10k	150k	50	**117k @ 0.1∼1μA ∼1 @ 1∼10pA**
Max. Power consumption[mW]	∼10	86	125	∼256	**125**

[1] 0.5 in simulation

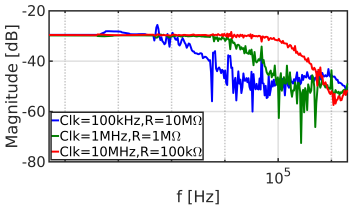


Fig. 7. System transfer function magnitude

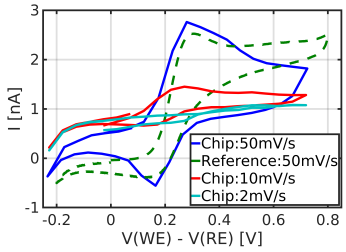


Fig. 8. Cyclic voltammetry results benchmarked with commercial potentiostat

due to the network analyzer dynamic range limitation.

B. Electrochemical measurements

Cyclic voltammetry (CV) in chemical solutions is used to verify the close loop performance and quality of the post-processing. The bonded chip was emerged into 0.3mmol/L potassium ferrocyanide solution with a commercial Ag/AgCl RE (ALS, Japan) and a Pt wire as the CE. A closed loop CV was run at different scan rates, shown in Fig. 8. The result at 50 mV/s is compared with a commercial potentiostat (Gamry Reference 600+) using a 100×100μm^2 dummy electrode array, normalized to the chip electrode area. The most likely cause of the observed differences are the boundary effects because of the smaller on-chip electrode.

VI. CONCLUSION

This work presents a 180nm CMOS 64-channel potentiostat. Compared to SotA (Table I), 4× more independent electrochemical characterization channels and 30dB larger current dynamic range are achieved. These innovations make the chip feasible to monitor high-throughput, widely-variable electrochemical processes, such as microbial electrolysis, anti-corrosion studies and biomolecule detection, with fast and flexible characterization. Further research on the post-processing is needed to improve the reliability.

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