FOSS EKV2.6 at GitHub

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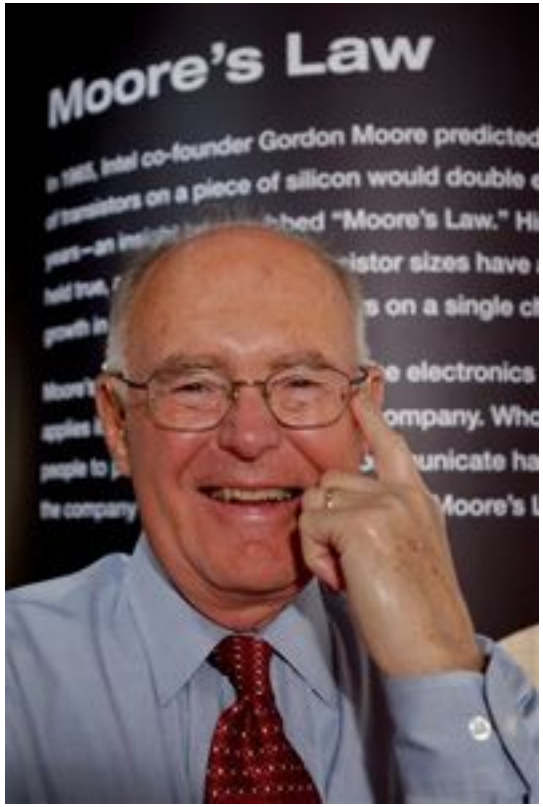
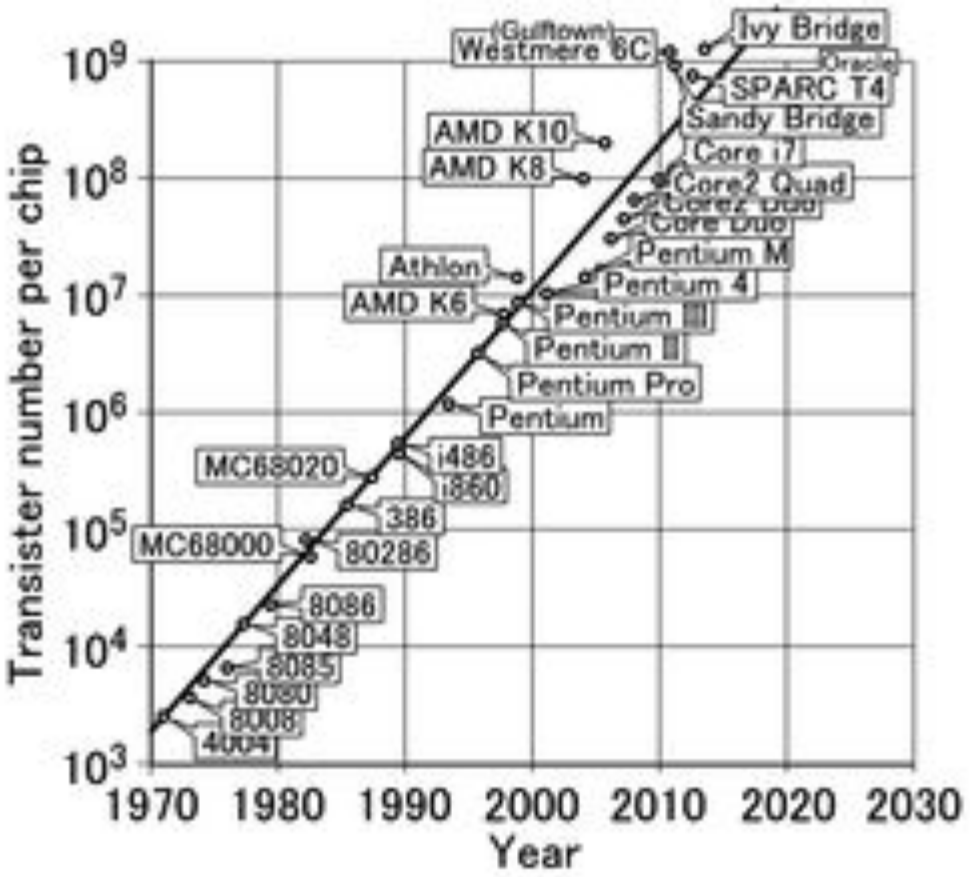
FOSS EKV2.6 Verilog-A

OUTLINE

- Moore's Law
- FOSS Modeling/Simulation Flow
- Development of the Compact Models
- EKV v2.6 Model Structure
- Testchip Layout
- Parameter Extraction Methodology
- Electrical Characterization
  - Pinch-off Voltage Characteristic
  - IV and CV Characteristic
  - 1/f Noise Characteristic
- Model Implementation
  - ADMS
  - Qucs Benchmarks
  - FOSS EKV2.6 Verilog-A at https://github.com/ekv26/model
- Summary

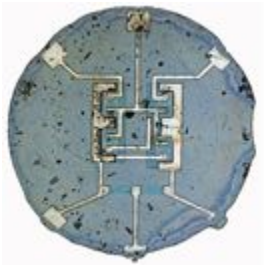
Moore’s Law





Moore’s Law is the fundamental driver of the semiconductor industry, what’s even more important is what it delivers to the end user.

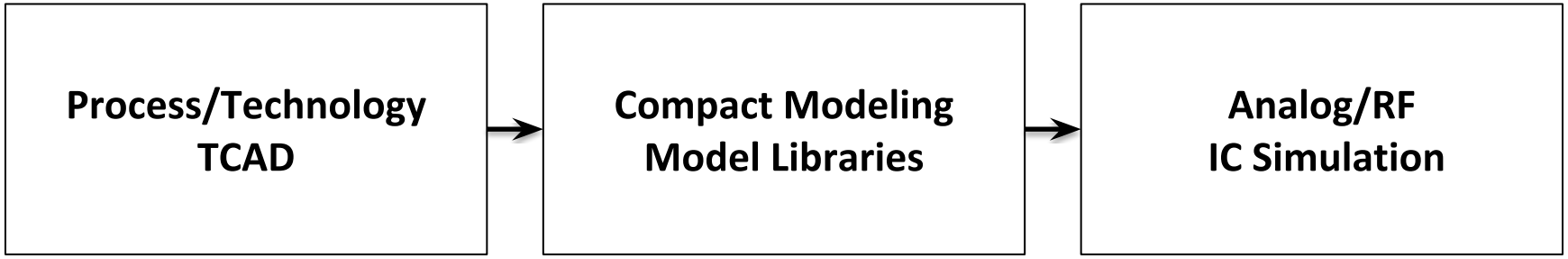
Moore’s Law (cont.)



The first working monolithic devices (IC) presented by Fairchild Semiconductor on May 26, 1960

The Raspberry Pi Zero is half the size of a ModelA+, with twice the utility. A tiny Raspberry Pi that’s affordable enough for any project!
($5 or even free as early 2016)
<www.raspberrypi.org/products/pi-zero>

FOSS Modeling/Simulation Flow

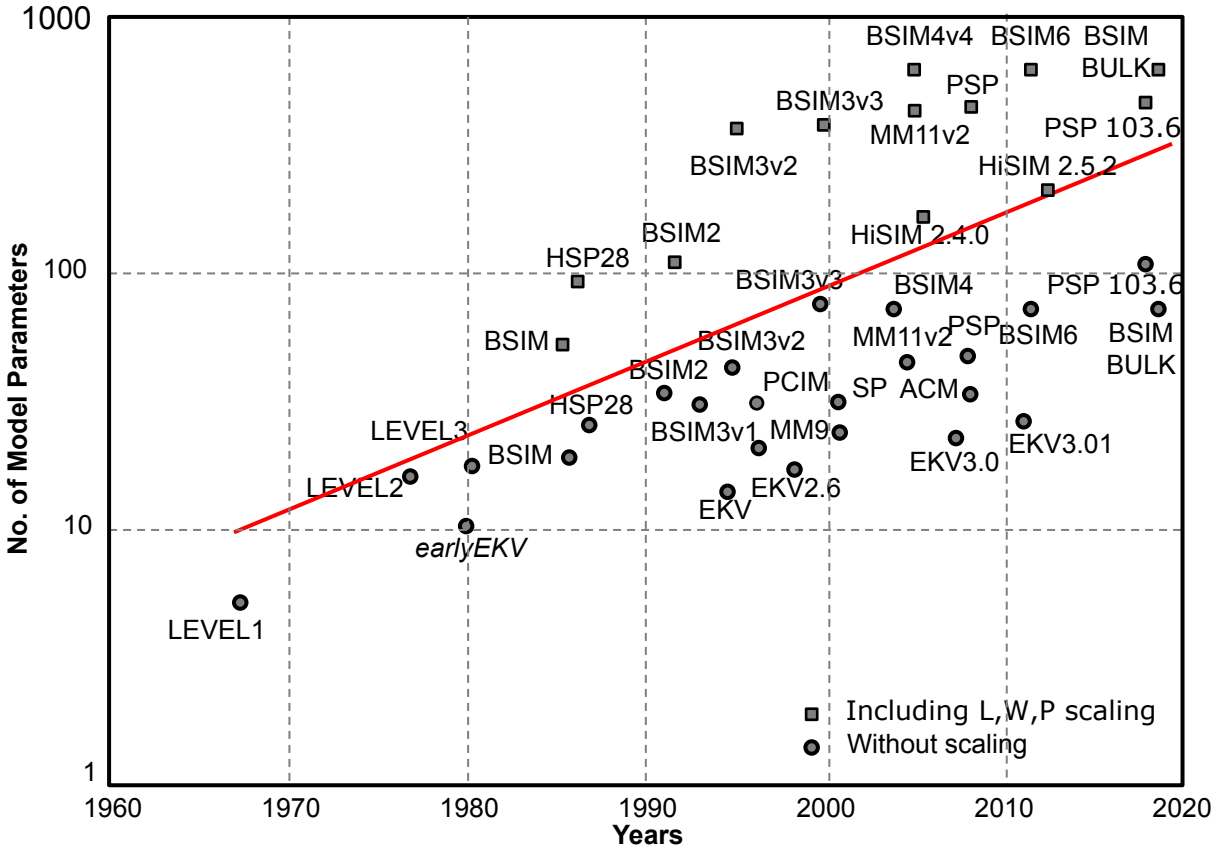


- Cogenda TCAD
- DevSim TCAD
- *other*
  EM Simulators

- Spice/Verilog-A Simulators
- Verilog-A Standardization
  - ADMS
  - MAPP
- *measurements*
- *parameterization*
- *other*

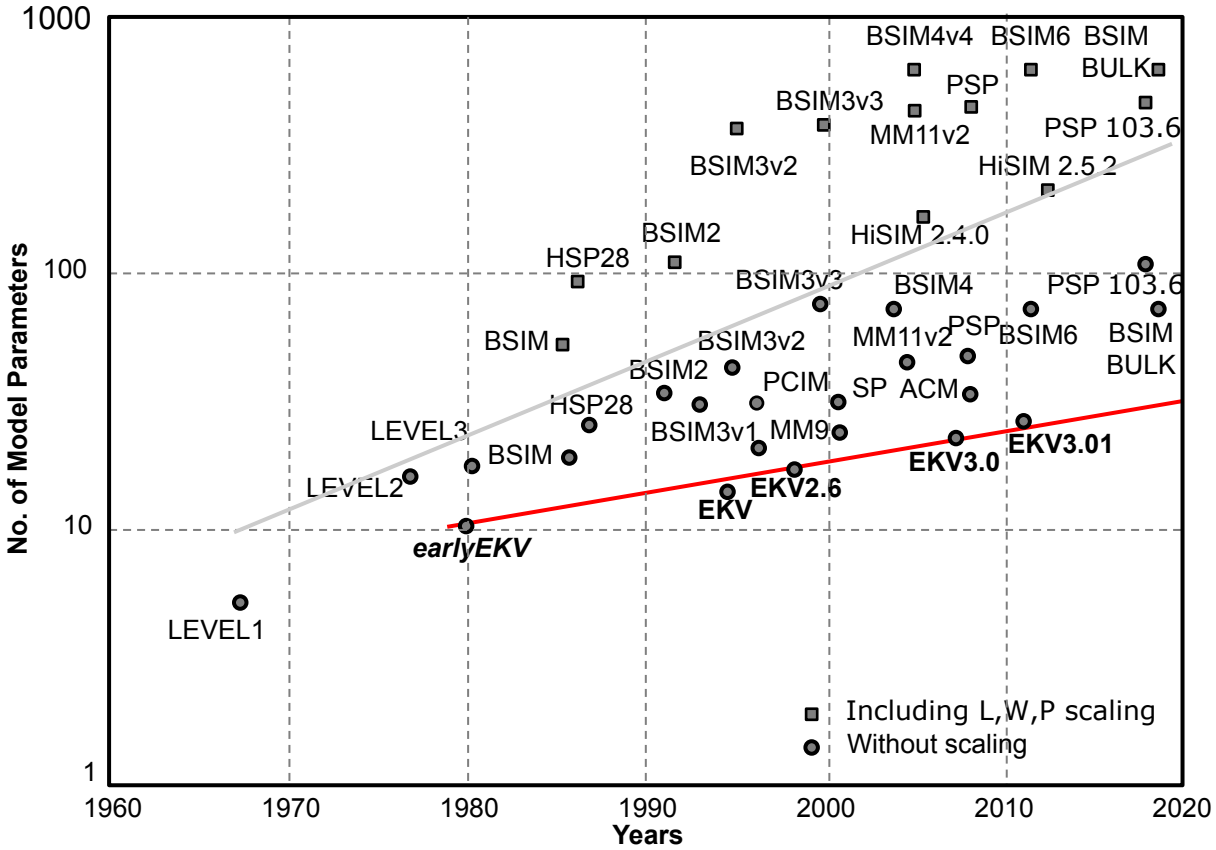
- Ngspice
- Qucs
- Xyce
- GnuCap
- *other*

Development of the Compact Models



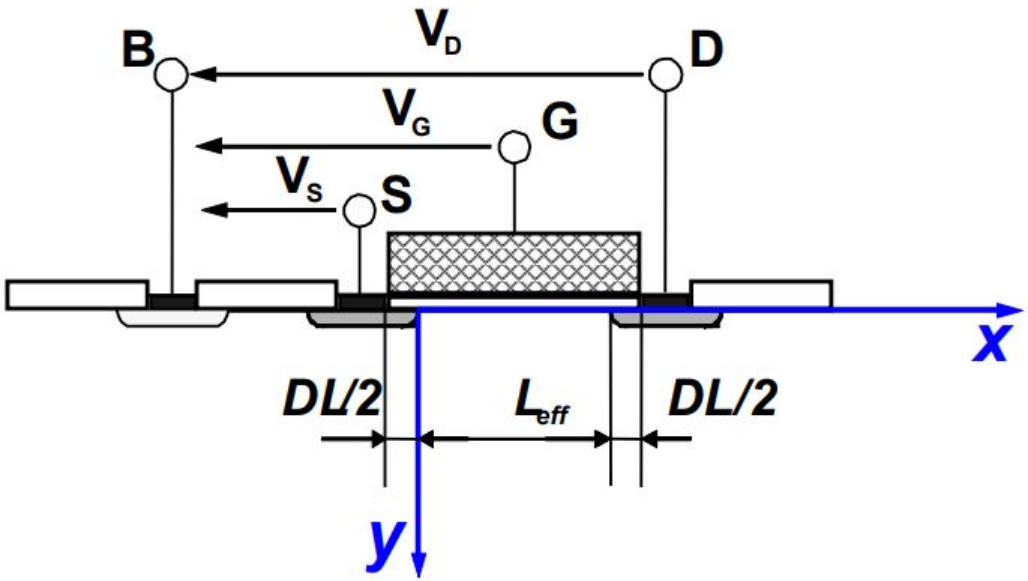
- Number of DC model parameters vs. the year of the introduction of the model
  Most recent versions of the BSIM, EKV, HiSIM and PSP models are included
- Significant growth of the parameter number that includes geometry (W/L) scaling

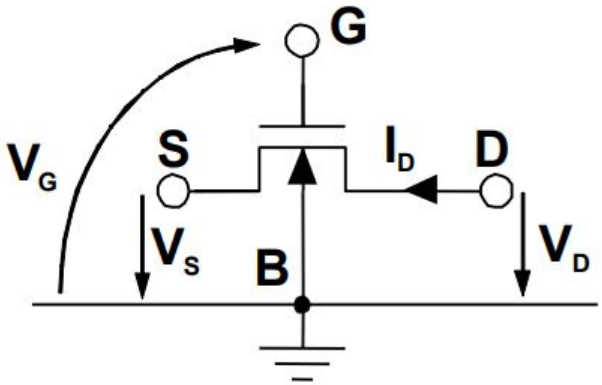
Development of the Compact Models



- Number of DC model parameters vs. the year of the introduction of the model
  Most recent versions of the BSIM, EKV, HiSIM and PSP models are included
- Significant growth of the parameter number that includes geometry (W/L) scaling
- Independent MOSFET model development based on the roots of the semiconductor physics and the design driven EKV modeling methodology
- EKV preserves coherent charge-based framework for static/dynamic modeling

EKV v2.6 Model Structure





Bulk-reference, symmetric model structure.
Drain current expression including drift and diffusion:

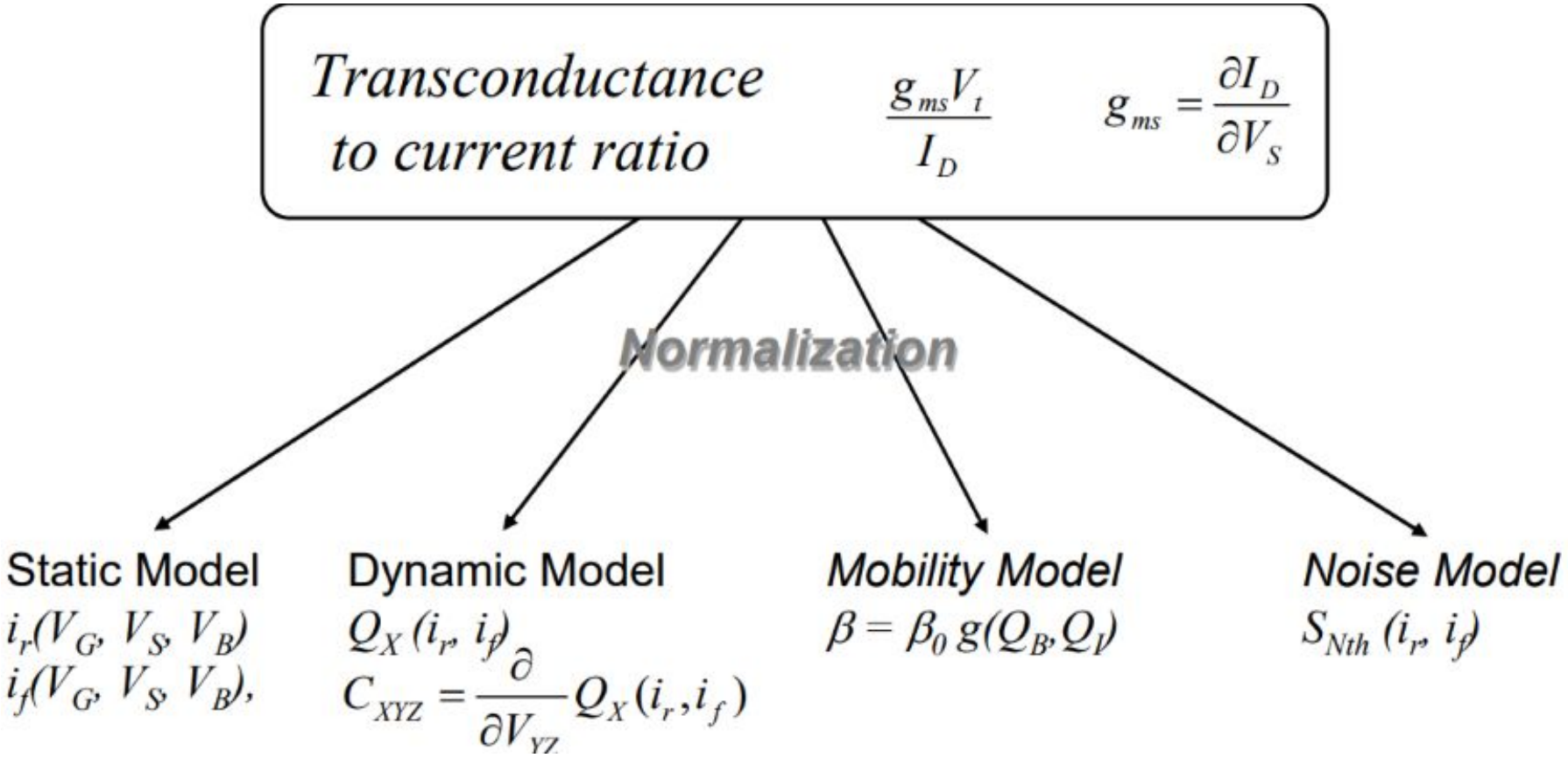
$$I_D = \beta \int_{V_S}^{V_D} \left(\frac{-Q_I'}{C_{OX}'}\right) \cdot dV_{CH} = \beta \int_{V_S}^{\infty} \left(\frac{-Q_I'}{C_{OX}'}\right) \cdot dV_{CH} - \beta \int_{V_D}^{\infty} \left(\frac{-Q_I'}{C_{OX}'}\right) \cdot dV_{CH} = I_F - I_R$$

where:

$$\beta = \mu \cdot C_{OX} \frac{W_{eff}}{L_{eff}}$$

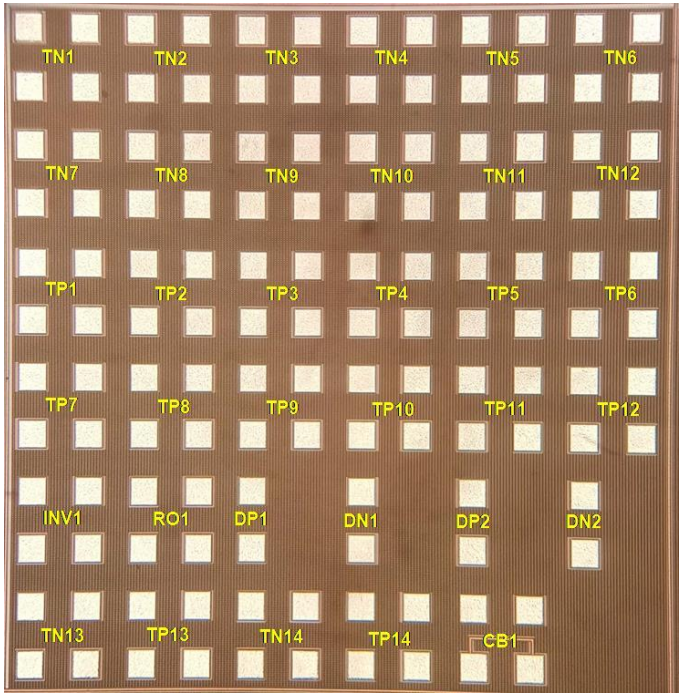
EKV v2.6 Model Structure (cont.)

Physical model basis leads to accurate description of transconductance-to-current ratio at all current levels allows coherent derivation of all model quantities including static, dynamic and noise modeling aspects.



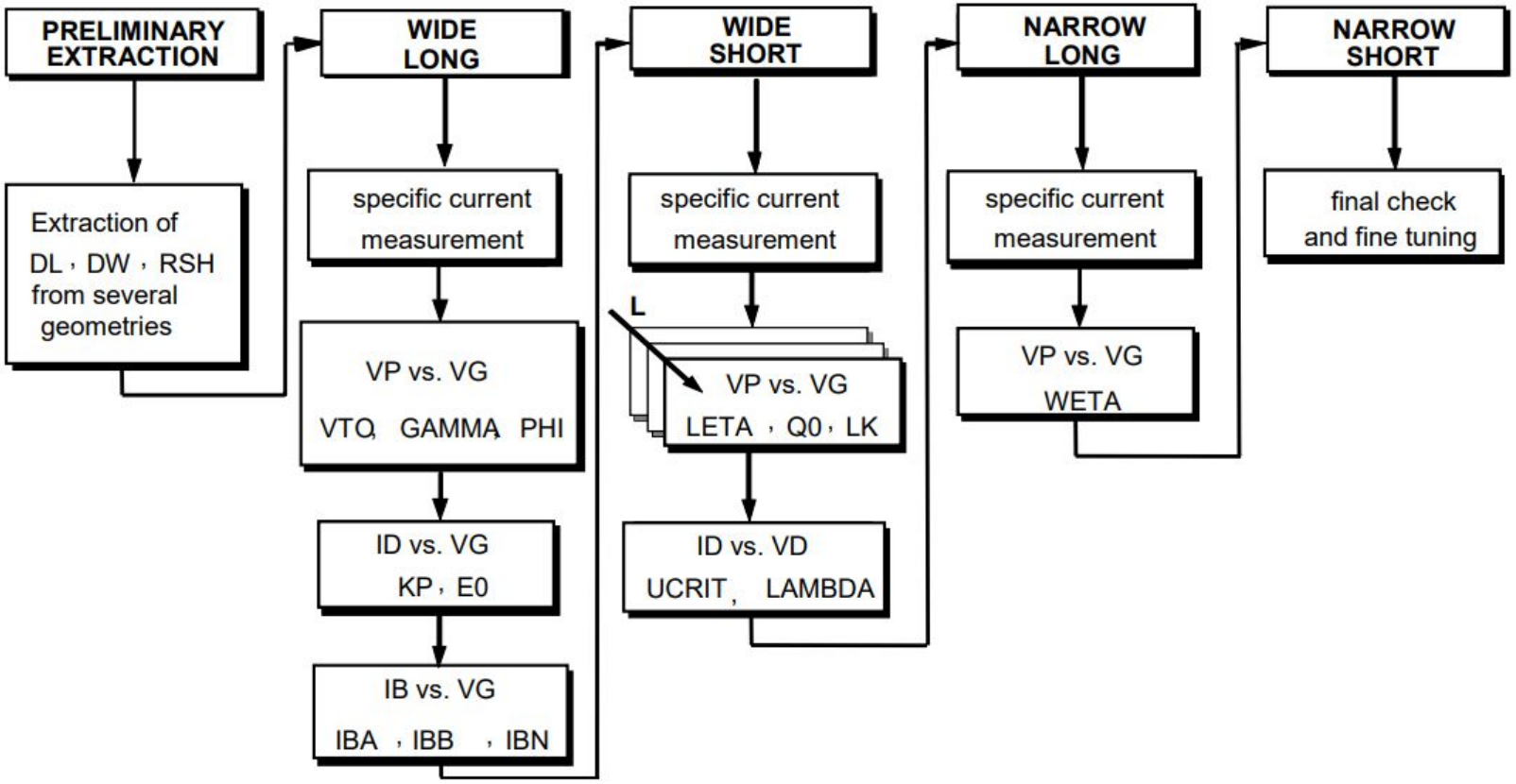
Testchip Layout in 180nm CMOS

Type of devices	Parameters
n-channel MOSFETs p-channel MOSFETs T(N/P)1-14	W=0.24 µm; L=0.18 µm (min.size devices) W=3 µm; L=0.18, 0.24, 0.3, 0.4, 0.6, 1.0 µm W=0.24, 0.3, 0.5, 1.0 µm; L=1.0 µm W=10 µm; L=10 µm (max.size devices) 10 parallel fingers of W=5 µm, L=10 µm W=50 µm, L=10 µm (wide devices)
CMOS inv. INV1	W_N=0.24 µm, W_P=0.24 µm, L_N= L_P =0.18 µm
CMOS ring osc. OSC1	W_N=0.24 µm, W_P=0.24 µm, L_N= L_P =0.18 µm 31 stages
n^+-pwell, p^+-nwell diodes D(N/P)1-2	W=L=100 µ W=10 µm, L=100 µm (10 fingers)



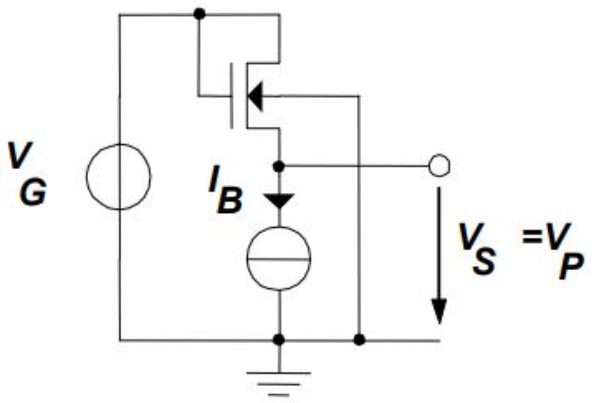
Europractice is acknowledged for providing free access to UMC 180 nm CMOS silicon and all corresponding libraries and PDKs for the EKV2.6 test chip design and manufacturing.

Parameter Extraction Methodology

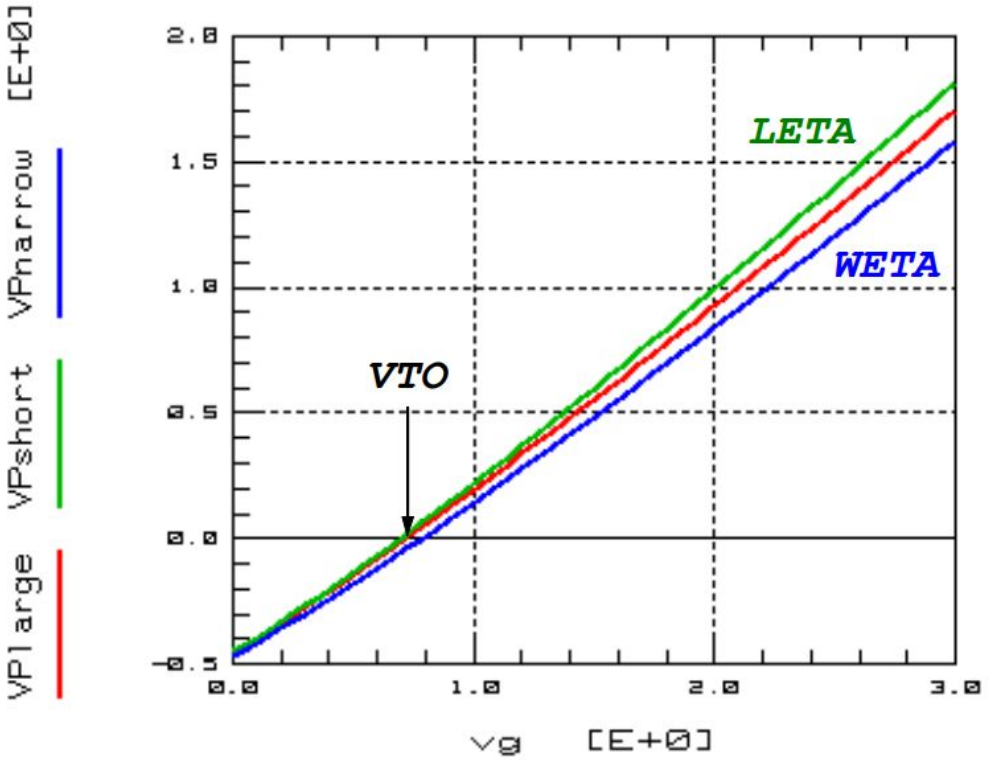


- Parameter extraction methodology established for EKV v2.6
- Sequential task performed from an array of transistors in the W/L plane.

Pinch-off Voltage Characteristic

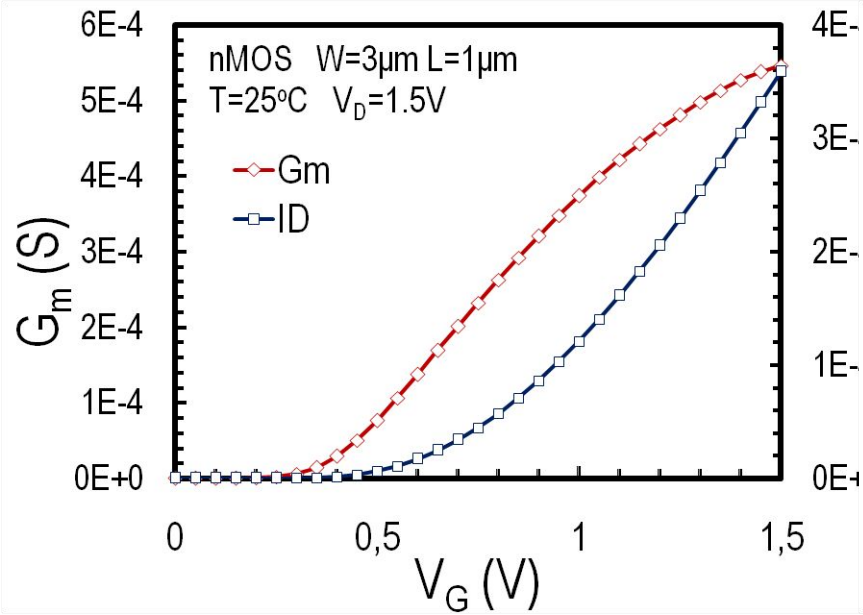


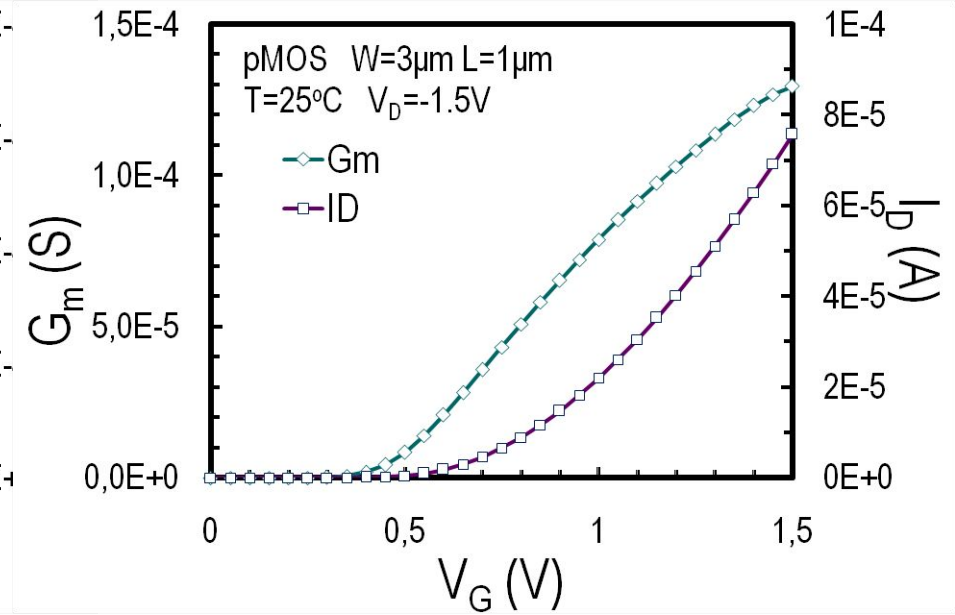
$$I_B = \frac{I_S}{2} = n \cdot \beta \cdot U_T^2$$



- Pinch-off voltage measurement at constant current ($I_S/2$)
- Gate voltage V_G is swept and $V_P=V_S$ is measured at the source for a transistor biased in moderate inversion and saturation
- Effects of short- and narrow-channels are analyzed using the charge-sharing approach.
- Corresponding parameters: LETA and WETA

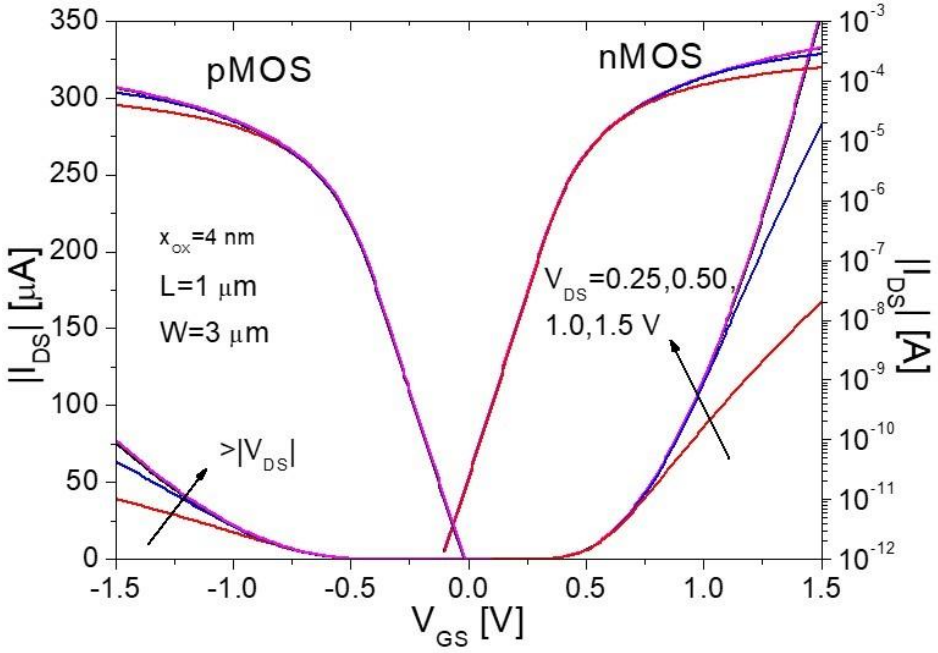
Transfer Characteristics in Saturation

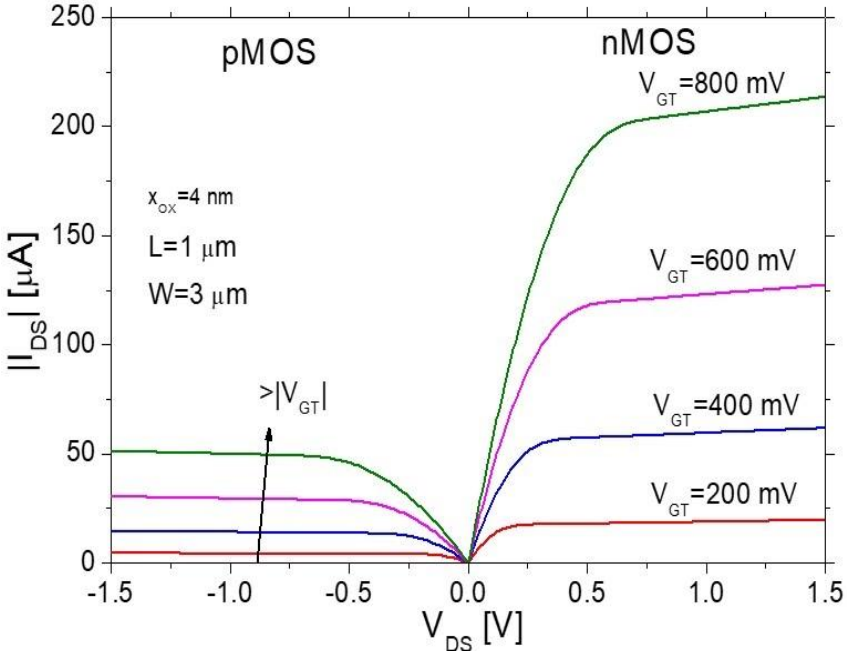




- ID-VG measurement in saturation
  - Determine gate transconductance gm
  - Extract technology current I0, slope factor n a

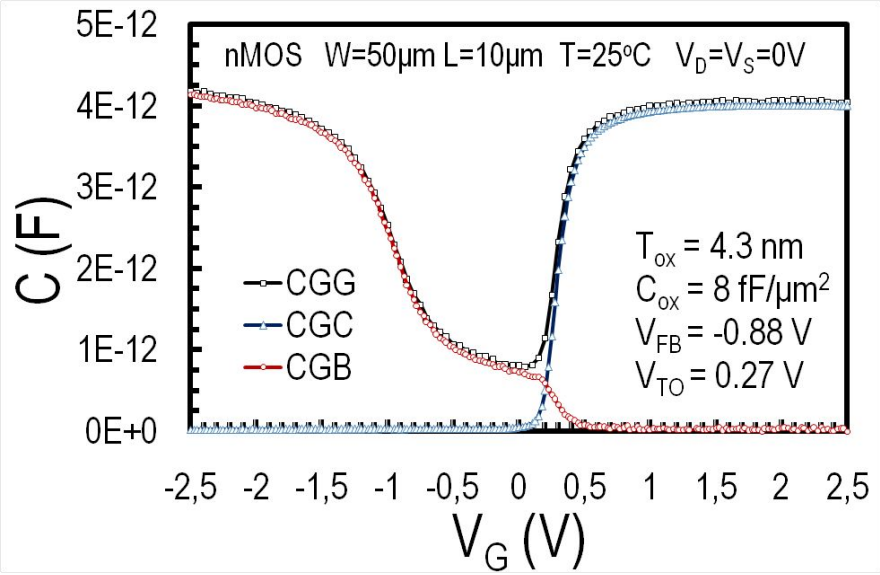
p- and n-MOS IV Characteristics

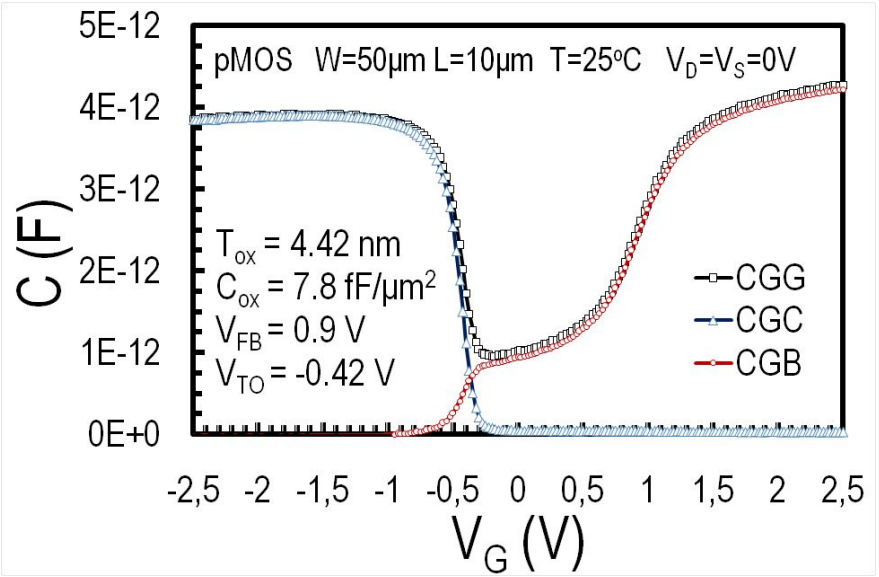




- ID-VG and ID-VD measurements

CV Characteristics – Extraction of C_{ox}

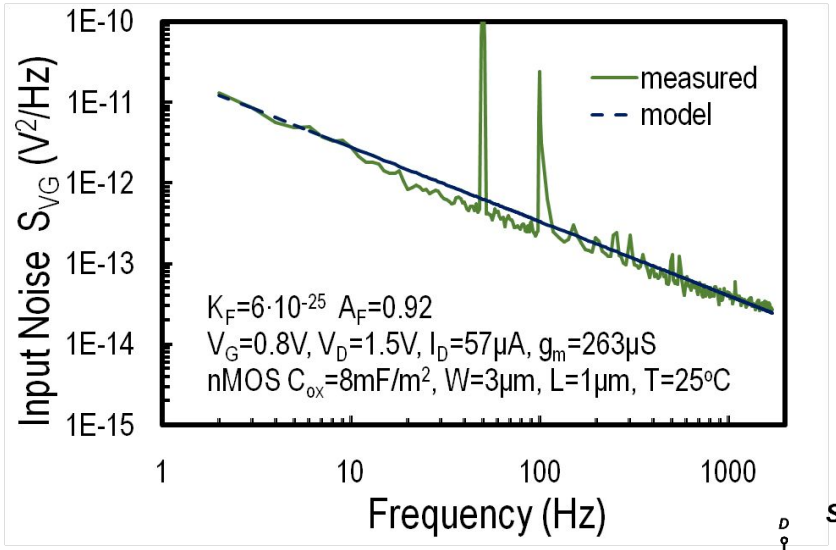


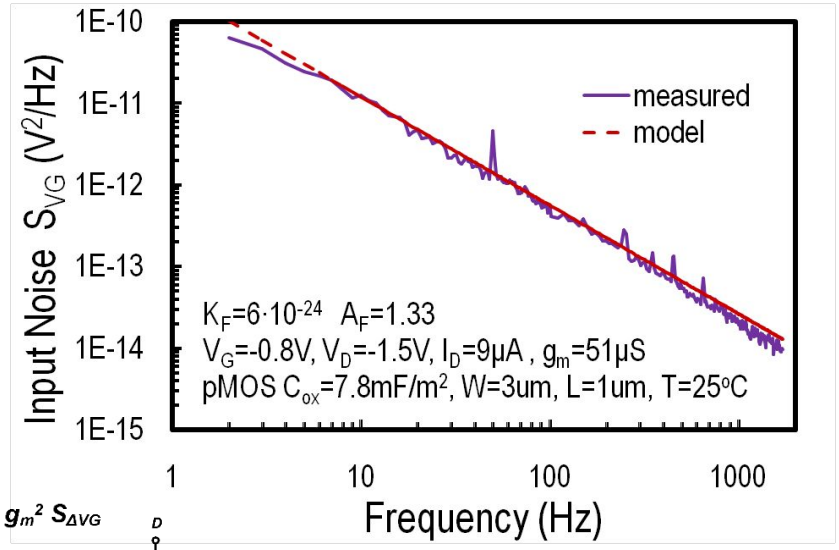


- Split CV measurements
  - CGG total gate capacitance
  - CGC channel capacitance
  - CGB gate-bulk capacitance
- Extraction of gate capacitance Cox
  - Cox obtained in inversion: Cox=CGG, inv(max)/(W·L)

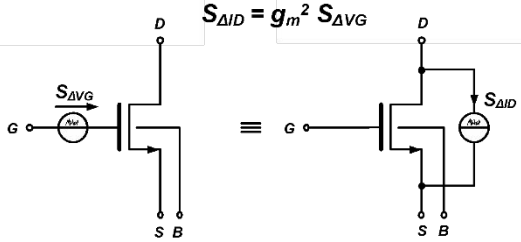
Parameter	Units	NMOS	PMOS
COX	F/m2	8.00E-3	7.80E-3
TOX	m	4.31E-9	4.42E-9

Input Noise Power Spectral Density Svg(f)





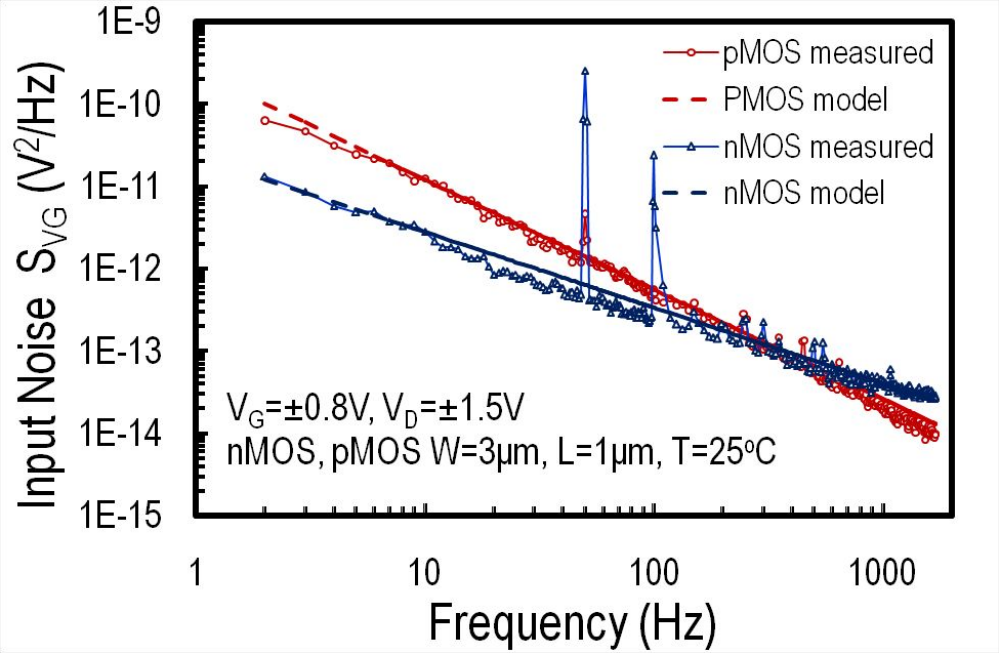
$S_{\Delta ID} = g_m^2 \, S_{\Delta VG}$



- Referring output noise to the input:
  - $S_{VG}(f) = S_{ID}(f)/g_m^2$
- Extract KF, AF parameters

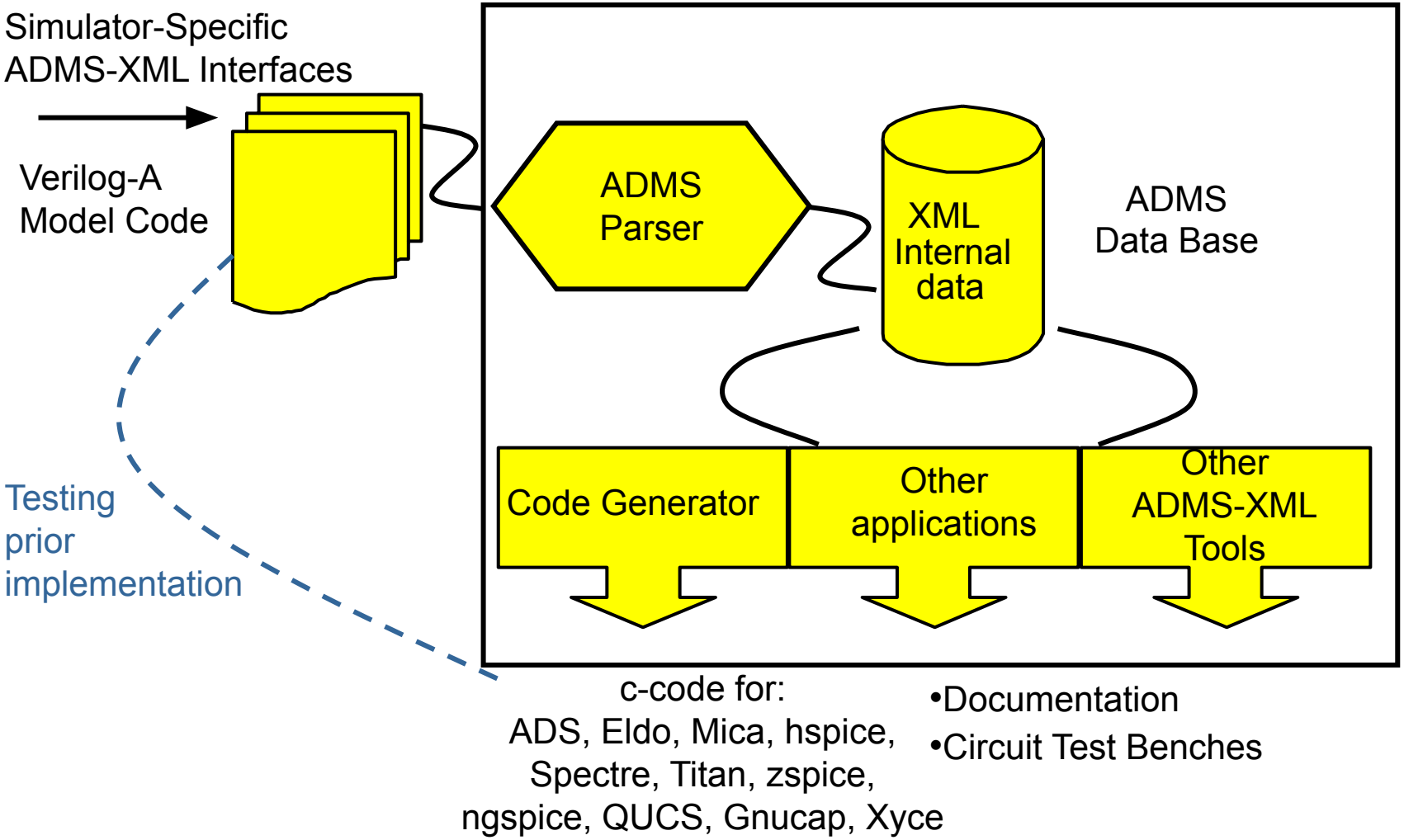
Parameter	Units	NMOS	PMOS
KF	V2F	6E-25	6E-24
AF	-	0.92	1.33

Comparison nMOS-pMOS 180nm CMOS



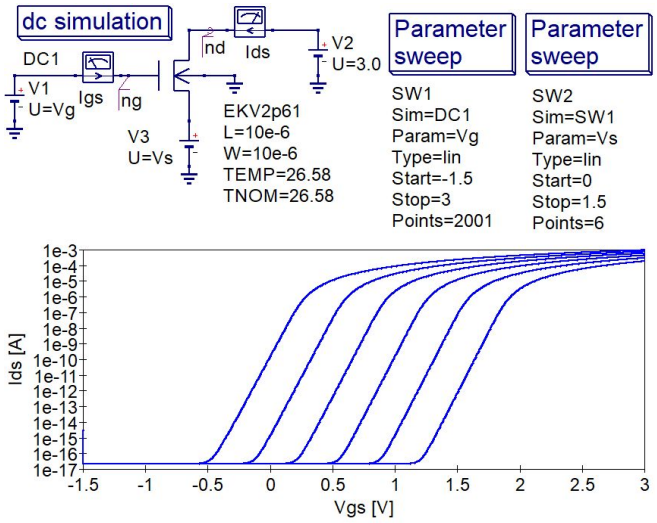
- Use input referred noise to compare among different devices
  - nMOS input referred noise is lower than pMOS @f ≤ 250 Hz
  - But: … nMOS has higher corner frequency f_c.
  - "1/f" is not always 1/f !

ADMS - Overview

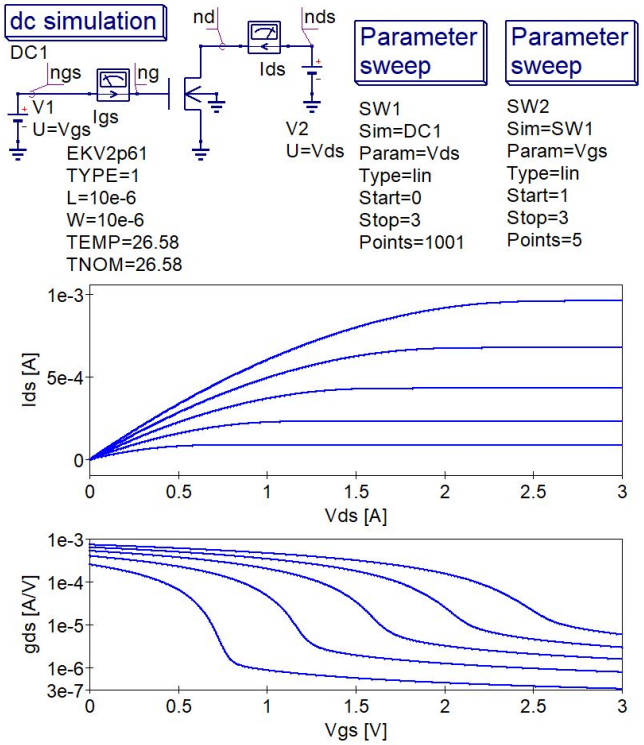


[REF] http:// mot-adms.sourceforge.net

Qucs EKV2.6 n-MOSFET Long Channel IVs



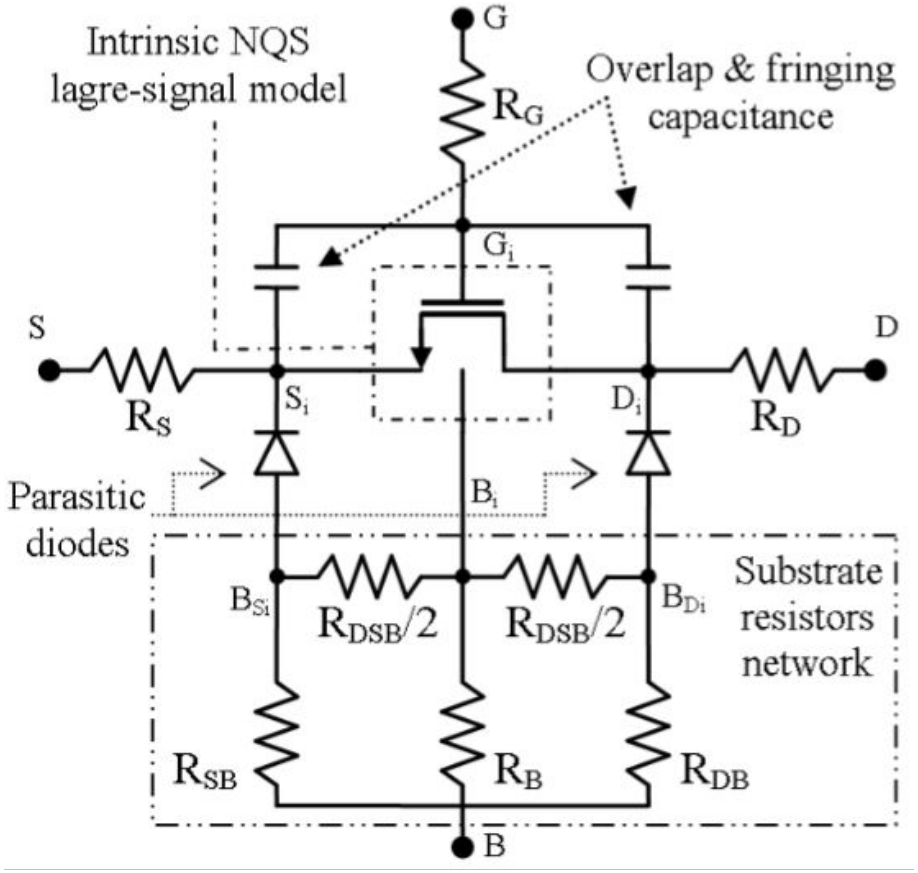
Transfer Ids-Vgs characteristics



Output Ids-Vds characteristics

[REF] http://qucs.sourceforge.net

FOSS EKV2.6 Verilog-A Outlook



- EKV RF modeling
- SOI and TFT Technologies
- EKV HV
- Cryogenic electronics
- Ageing, radiation effects, reliability modeling

FOSS EKV2.6 Verilog-A

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