AN INVESTIGATION OF CdS THIN FILMS AND GERMANIUM-CdS-COPPER SWITCHING DEVICES

A Thesis

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CONTENTS

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SUMMARY

ıe object of this work was investigation of the distinctive non-
›latile memory characteristic exhibited by Germanium - Cadmium
ılphide - Copper devices. To this end a device was fabricated by
ıe evaporation of CdS on to single crystal Germanium, and part of
ıe work involved an investigation of CdS condensation from vapour
ıd the electrical properties of the films thus produced. From
E M measurements on films condensed on to single crystal Sodium
ılloride, the CdS film was deduced to be epitaxial. The surface
ıd cross-section of films condensed on to Germanium and glass
ɜre inspected by means of a S E M.

ıarticular attention was directed to the performance of the high
ıcuum system and electron beam gun evaporation of CdS, and
›mparisons were made between single source and other evaporation
ɜchniques. The vapours present before and during CdS evaporation
ɜre analysed with the aid of mass spectrograph equipment.

ıe electrical properties of CdS films were studied and a survey
ıs made of devices showing similar electrical characteristics.
ıeories are offered to explain the observed phenomena and these
ɜe discussed.

ɛtensive electrical measurements were made on a large number of
ɜvices fabricated under a variety of conditions. From these
ɜasurements it was clear that the switching exhibited by the
ɜvice was attributable to the formation and destruction of
ghly conductive filaments within the CdS film, and that switching
ɜpends not only on the electronics but also on the thermodynamics
ɜ the device.

'ore this work began it was suspected that the switching
ıibited by Ge-CdS-Cu and similar semi-conductor devices, was
'ely electronic and therefore different in origin from that
ıcovered in glass devices.

'ough this work it has become clear that, in spite of the
ısiderable structural and electrical differences between
.taxial semi-conductor and glass devices, switching
dependent in both cases on similar thermal effects even
ıugh these may have been initiated by different electronic
ıcesses.

INTRODUCTION

: main purpose of this thesis is an investigation of the electrical
:racteristics of Ge-CdS-Cu devices. The thin evaporated CdS film
.ys an important role in the creation of such characteristics.
:ever, unlike high quality semiconductors formed, for example,
)m the melt, the structure and electrical characteristics of
:porated thin films cannot be assumed, and this is particularly
:e of compound semiconductors such as CdS. For this reason the
:st three chapters concentrate on the CdS film formation, its
:ucture, the influence of the condensation conditions, and the
)ortance of controlling these conditions to produce consistent films.

Chapter 4 the electrical characteristics of thin CdS films are
.ated to film structure and condensation conditions, but no
:surements are offered on CdS films in isolation. Such measurements
ld be useful as an aid to understanding the Ge-CdS-Cu device,
)viding they related to the CdS film alone. Unfortunately it is not
sible to make such measurements on the film in complete isolation
n it has been evaporated on to a Germanium substrate, as the
manium substrate cannot be prevented from interfering with such
:surements. An alternative approach would be to use another type
substrate, but this could produce misleading results, as the
ucture, and hence electrical characteristics of the CdS film, depend
atly on the substrate. For this reason Chapter 4 provides only
indication of the trends displayed by CdS on other types of
strate. Later, in Chapters 7 and 8, device measurements are made
m which relevant electrical characteristics of the CdS film may be
uced.

ices with similar switching characteristics to Ge-CdS-Cu are
cussed in Chapter 5 to facilitate direct comparisons of physical
ucture and electrical characteristics. The theories proposed to
lain the switching phenomena are discussed in this chapter as
paration for the analysis section of Chapter 7.

hapter 7 both non-switching and switching characteristics of
.cal devices are presented. Although the switching of these
.ces is the primary interest, the non-switching characteristics
ride considerable information on the electronics of the device.
results are analysed for each group of experiments with respect
iodels representing the device in its various states and this
)ws the accuracy and validity of the models to be assessed
.vidually.

hapter 8 the electrical characteristics of a group of devices
:icated under a variety of condensation conditions and with various
:trate orientations and metal electrode types, are investigated in
:r to determine the individual effects of these fabrication
ameters.

CHAPTER 1

EVAPORATION, CONDENSATION AND GROWTH OF CADMIUM SULPHIDE FILMS

INTRODUCTION

Large steps forward have been made in the last fifteen years in the improvement of evaporation techniques and vacuum technology, as well as in the understanding of the formation, structure and composition of thin evaporated films. As a result the reproducibility and reliability of devices made from such films have improved considerably. Some results vary from worker to worker: this reflects differences in the quality of the equipment used and the manner of its use.

This chapter describes in qualitative terms the effects of the many factors which determine the growth and structural quality of evaporated CdS thin films.

EVAPORATION OF CADMIUM SULPHIDE

The composition of a vapour evaporated from a heated source material, i.e. the evaporant, depends on the temperature of the evaporant, its purity, and the unavoidable background pressure. These are the factors that determine the total pressure, the overall stoichiometry, i.e. the relative density of constituent atoms, the relative quantities of constituent molecules, and the impurities content of the vapour. The composition of the vapour may be critical in the subsequent condensation of the film.

Dissociation

Cadmium Sulphide dissociates upon heating into cadmium atoms and sulphur molecules.[1,2,3]

$$CdS = Cd + \sum_{8}^{1} a_n S_n$$

The sulphur molecules in the CdS vapour range in size from 1 to 8 atoms. The average size decreases with increasing vapour temperature and decreasing vapour pressure.[1,4,5] CdS evaporated at temperatures greater than 600°C has vapour with S_2 as the predominant sulphur molecule.[1,4]

2 Rate of evaporation

The major factors determining the rate of evaporation are evaporant temperature and purity. Experiments on single crystal CdS (0001) face, have shown that the temperature dependence of the rate is proportional to $\exp \frac{-1}{T(^{\circ}K)}$.[6] Excess cadmium, sulphur, or impurities such as copper, in the evaporant, will give a lower evaporation rate than stoichiometric, impurity free, CdS. The excess constituent of the compound - cadmium or sulphur as the case may be - will diffuse to the surface and evaporate at a greater rate than the other constituent. When the excess constituent becomes depleted and the evaporant becomes stoichiometric, then the rate increases. Thus the rate at which cadmium atoms, N_{Cd}, and sulphur atoms, N_S, are evaporated and the ratio of these rates, $\frac{N_{Cd}}{N_S}$, may vary considerably with time, even though the evaporation temperature is constant. Furthermore, evaporant impurities not only affect the evaporation rate, they may also be found in the vapour.

The rate of evaporation is also dependent on the crystal face allowed to evaporate.[6] Powdered and polycrystalline evaporants have an uncontrollable surface area which changes with time due to preferential evaporation, and this leads to less stable evaporation rates than those found in the evaporation

of single crystals.

Residue gases

Residue or background gases, even in small amounts, can affect the evaporation rate. Pressures of less than 10^{-5} torr (mm Hg) are necessary to ensure that molecules and atoms can evaporate unimpeded.[8,9] These residue gases are mixed with the vapour and may chemically react with the molecules and atoms. Ensuring a sufficiently high evaporation rate diminishes the impurity content of the vapour,[9,10] e.g. evaporation at 2400Å/min in an oxygen pressure of 10^{-7} torr will result in a maximum impurity content of 0.25%.

HETEROGENEOUS NUCLEATION AND FILM GROWTH

This sub-section is a general description of the nucleation and growth of one material on a substrate of another material, and is based mainly on the work done on metal[12,13] and single component semi-conductor condensation. The model is also valid for compound semi-conductor condensation when the condensation of the components individually is not possible.

Nucleation from a single component vapour

Atoms from the vapour impinge on the substrate surface. If the kinetic energy* of the atom is not excessive, then the atom will become physically adsorbed, i.e. an adatom, but able to move in the plane of the surface of the substrate. These adatoms may re-evaporate or they may become chemically adsorbed.

* The kinetic energy of the atom is a function of the temperature of the vapour.

By collision with other diffusing adatoms they may form or add to 3 - dimensional clusters. These clusters of adatoms which may also diffuse, are unstable in that they may either increase or decrease in size. If a cluster exceeds a critical size however, it becomes a stable nuclei and continues to grow.

Nucleation will continue until the average distance between the nuclei corresponds to the mean diffusion distance of adatoms and clusters. Nucleation has reached saturation when all the clusters that form are captured by the existing nuclei.

Preferential nucleation may take place on substrate surface irregularities, e.g. scratches, but in general nucleation depends on the statistics of the processes involved.

Film growth

The nuclei continue to grow after saturation by addition directly from the vapour or from the capture of unstable clusters. The region between the nuclei decreases and large islands are formed by the coalescence of nuclei. Large scale coalescence of the islands under further growth results first in a connected network and subsequently in a continuous film as the gaps in the network are filled.

Formation of grain boundaries

The individual nuclei are mostly defect free and can have both different lattice orientations and different crystal structures from each other. When two nuclei coalesce, the smaller nuclei tends to reorientate or recrystallise to accommodate misorientations or differences in the crystal structure between the two nuclei. A grain boundary

is formed if the misorientation is severe and if large scale coalescence limits the reorientations.

Fibre texture and epitaxial growth

Crystallites or grains of polycrystalline films condensed on a single crystal, polycrystalline or amorphous substrates, tend to have some form of preferred lattice orientation. This may develop during any stage from nucleation through to continuous film growth.

Normally a preferred crystal plane is parallel to the substrate surface. Single or double fibre texture describe a film with crystallites of one or two degrees of preferred lattice orientation.

These textures can occur regardless of the crystal structure, if any, of the substrate and tend to form at a post-nucleation stage. In films of cubic crystal structure many possible preferred orientations can be observed. The most frequently observed orientation at any particular stage of growth may change with continued growth. The preferred orientation of hexagonal and cubic crystal structured films can be strongly dependent on the angle of incidence of the impinging vapour to the substrate. The c-axis of the crystallites of hexagonal crystal structure tends to orientate towards the direction of the impinging vapour. At normal incidence the c-axis is perpendicular to the substrate surface with the a-axes randomly orientated.

Epitaxial films only occur on single crystal substrates where the preferred orientation develops from the nucleation stage.

The surface energy of the substrate/nuclei interface varies with different relative orientations of the lattices of the nuclei and substrate.

In single crystal films of hexagonal structure only one preferred orientation develops, the c-axis being perpendicular to the substrate and the a-axes having one preferred orientation relative to the substrate lattice.

MODEL FOR CONDENSATION OF A BINARY COMPONENT VAPOUR (AFTER GÜNTHER[14])

The condensation of a vapour having two components to form a stoichiometric film is only possible if certain conditions are fulfilled, viz. the substrate temperature and impinging fluxes of both components must be within certain critical limits, the limits being determined by the characteristics of the substrate surface and of the vapours.

Development of the model

Above the surface of the substrate the vapour has two components - A and B. It is assumed that the components interact only on the substrate surface. N_A and N_B are the fluxes and p_A and p_B are the partial pressures associated with A and B.

The particles of the vapour incident on the substrate are physically adsorbed and are free to move within the plane of the substrate surface. The adsorbed particles can interact with other particles and become chemically adsorbed - or they can re-evaporate.

The density of the physically adsorbed particles at any time is described by

$$n_i = \frac{N_i}{w} \exp \frac{\Delta G}{kT_s} \quad , \quad i = A,B \quad \ldots\ldots\ldots(1)$$

ΔG = the interfacial energy

w = the transmission frequency

k = Boltzmann's constant

T_s = the absolute temperature of the surface

N_i = the incident flux A or B

The probability of interaction between particles A and B on the surface gives n_{AB} which is an estimate of the flux of chemically adsorbed molecules A_nB_m

$$n_{AB} = \text{constant} \times n_A n_B$$

Since n_i is proportional to N_i then n_{AB} is proportional to the product of the incident fluxes

$$n_{AB} \quad \alpha \quad N_A N_B$$

n_{AB}, the flux of adsorbed molecules, is strongly temperature dependent. Consider now component A incident on the substrate without the presence of B. N_{KA} is the rate at which particles of A become chemically adsorbed. Condensation of A may be expressed by

$$N_{KA} = 0 \text{ if } T_s > T_{Acrit}(p_A)$$

$$N_{KA} > 0 \text{ if } T_s < T_{Acrit}(p_A)$$

$$\text{where } T_{Acrit}(p_A) < T_{eA}(p_A)$$

Thus condensation occurs when the temperature of the substrate is lower than a critical temperature which is dependent on p_A. T_{eA} is the equilibrium temperature of the vapour.

Alternatively

$$N_{KA} = 0 \text{ if } p_A < p_{Acrit}(T_s)$$

$$N_{KA} > 0 \text{ if } p_A > p_{Acrit}(T_s)$$

$$\text{where } p_{Acrit}(T_s) > p_{eA}(T_s)$$

Condensation occurs when the vapour pressure is greater than a critical value, p_{Acrit}, which is dependent on T_s. p_{eA} is the equilibrium pressure of the vapour at the temperature of the substrate. Supersaturation, q_A, and critical supersaturation, q_{Acrit}, are defined as

$$q_A = \frac{p_A}{p_{eA}} \quad , \quad q_{Acrit} = \frac{p_{Acrit}}{p_{eA}}$$

The differences between T_{Acrit} and T_{eA} and p_{Acrit} and p_{eA} are determined by the energies of the vapour/substrate interface.

For condensation on to a substrate of the same material the differences are very small, but for a dissimilar substrate material supersaturations of many orders of magnitude may have to be overcome.

$q_{Acrit} \simeq 1$ for homogeneous condensation

$q_{Acrit} \gg 1$ for heterogeneous condensation

During continuous condensation when the substrate is covered by the vapour material, the condensation changes from heterogeneous to homogeneous with the accompanying reduction of the critical supersaturation.

Thus the rate of growth of all the film except the first covering layer is determined by homogeneous condensation.

Returning to our two component condensation, we can now define for each of the components a critical value of incident flux,

N_{Acrit} and N_{Bcrit}, associated with the critical supersaturations and critical substrate temperatures T_{Acrit} and T_{Bcrit}.

Components A and B will condense separately as determined by their different critical values of substrate temperature and flux. An important additional consideration is the interaction of A and B on the substrate surface. The rate at which the molecule A_nB_m is formed is n_{AB} which is proportional to N_AN_B. Significant densities of the molecule are formed when

$$N_AN_B > \text{constant}$$

The molecule on the substrate surface has an equilibrium pressure p_{eAB} which usually corresponds to its dissociation pressure. For most molecules

$$p_{eAB} < p_{eA}, p_{eB} \qquad \ldots\ldots\ldots(2)$$

i.e. the molecule is less volatile than its constituents.

This is a necessary condition for the validity of the model for stoichiometric condensation. The molecule may condense on the substrate at a temperature too high for condensation of its constituents. Equation (2) thus implies

$$T_{ABcrit} > T_{Acrit}, T_{Bcrit}$$

where T_{ABcrit} is the critical substrate temperature above which the compound will re-evaporate.

The critical flux of one component for condensation of the molecule is dependent on the availability of the other component. N_{KAB} is the flux of the condensing molecules

$$N_{KAB} = 0 \quad \text{if} \quad N_A < N_{Acrit}\ (N_B) \text{ or } N_B < N_{Bcrit}\ (N_A)$$

$$N_{KAB} > 0 \quad \text{if} \quad N_A > N_{Acrit}\ (N_B) \text{ or } N_B > N_{Bcrit}\ (N_A)$$

Directly from equation (2) we can deduce that

$$N_{Acrit}\ (N_B)\ \left[\text{for } A_nB_m \text{ condensation}\right] < N_{Acrit}\ \left[\begin{matrix}\text{for pure A}\\ \text{condensation}\end{matrix}\right]$$

and

$$N_{Bcrit}\ (N_A)\ \left[\text{for } A_nB_m \text{ condensation}\right] < N_{Bcrit}\ \left[\begin{matrix}\text{for pure B}\\ \text{condensation}\end{matrix}\right]$$

We can now describe the limits for stoichiometric condensation, i.e. the condensation of only the molecule A_nB_m

$$N_AN_B > \text{constant} \qquad \text{.....(3)}$$

$$N_{Acrit}\ (N_B) < N_A < N_{Acrit}\ \left[\text{for pure A}\right] \qquad \text{...(4)}$$

and $$N_{Bcrit}\ (N_A) < N_B < N_{Bcrit}\ \left[\text{for pure B}\right] \qquad \text{...(5)}$$

Equation (3) states that adequate fluxes of A and B are necessary for formation of molecules. In addition (4) and (5) state that the fluxes of the components should be less than the critical levels above which condensation of the individual components would occur. The equations (3), (4) and (5) are all highly dependent on the temperature of the substrate.

Figures 1a, b and c show the different possible compositions of the condensate by varying fluxes N_A and N_B at three temperatures. Figure 2 shows the dependence of the condensate composition on the substrate temperature for equal fluxes of A and B.

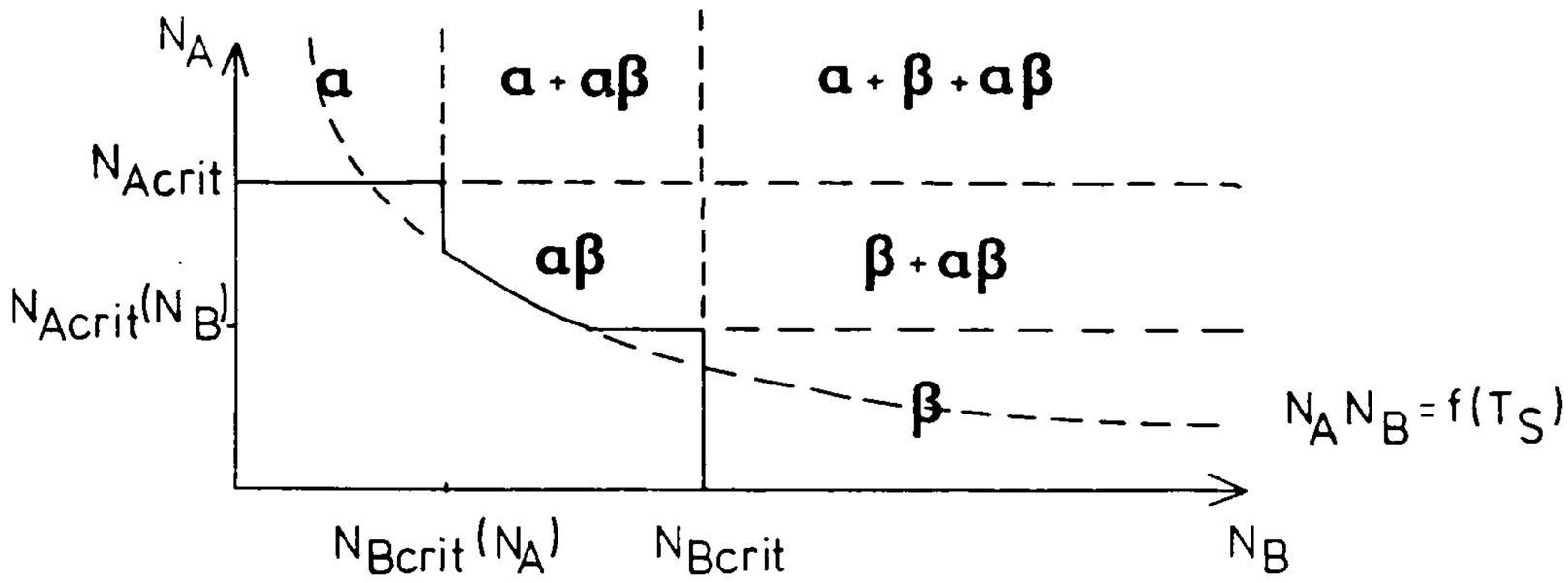
(T_{Acrit} has been assumed arbitrarily greater than T_{Bcrit} for both Figures 1 and 2)

From these figures it can be seen that the condensation is always stoichiometric for substrate temperatures greater than T_{Acrit}. At temperatures below this, pure A or B may condense if N_A or N_B are outside the upper limits described by equations (4) and (5).

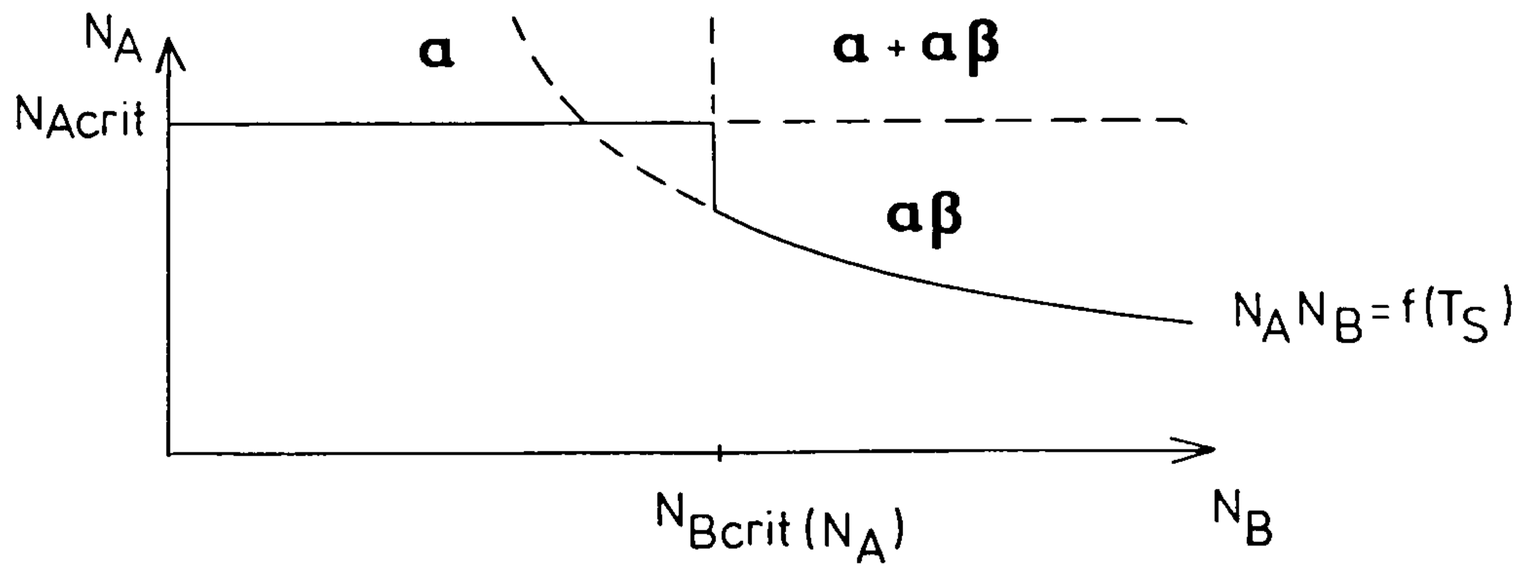
FIGURE 1 a, b & c

The composition of the condensation flux, N_K, as a function of the incident fluxes, N_A and N_B, and substrate temperature, T_S.

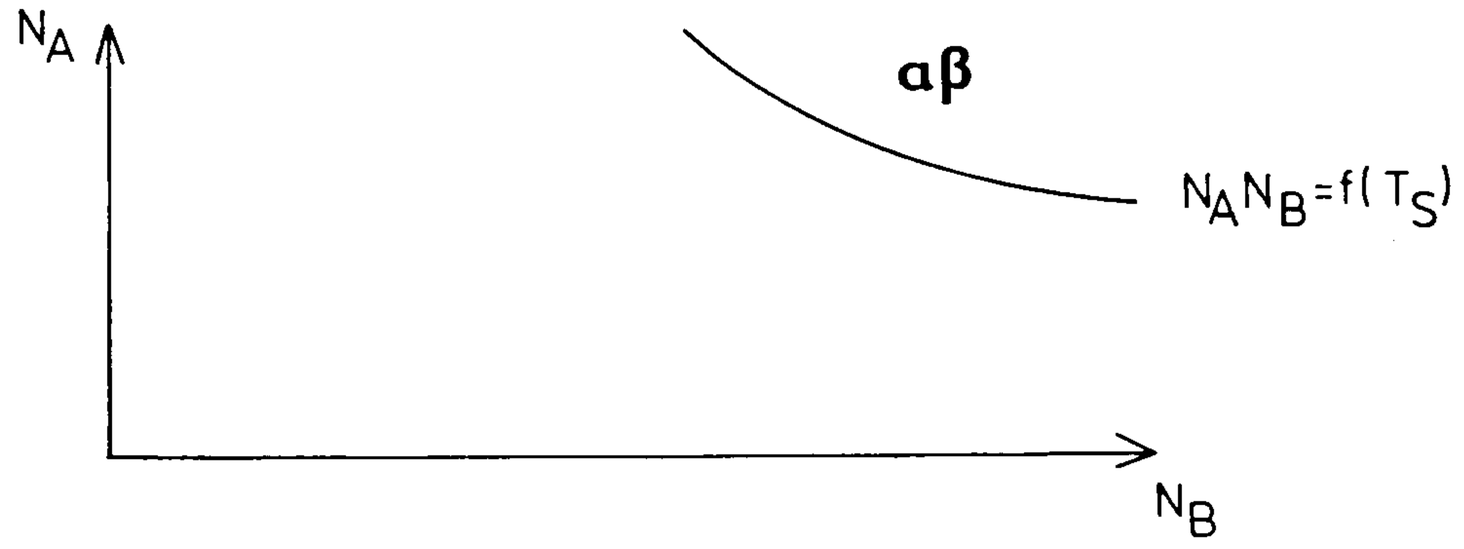
a) $T_S < T_{Bcrit}$



b) $T_{Bcrit} < T_S < T_{Acrit}$



c) $T_{Acrit} < T_S$



Notes

1) **α** represents condensation of A.
   β represents condensation of B
   αβ represents condensation of $A_n B_m$
2) A is Cadmium and B is Sulphur in CdS condensation.

FIGURE 2

The condensation flux, N_K, as a function of the substrate temperature, T_S.

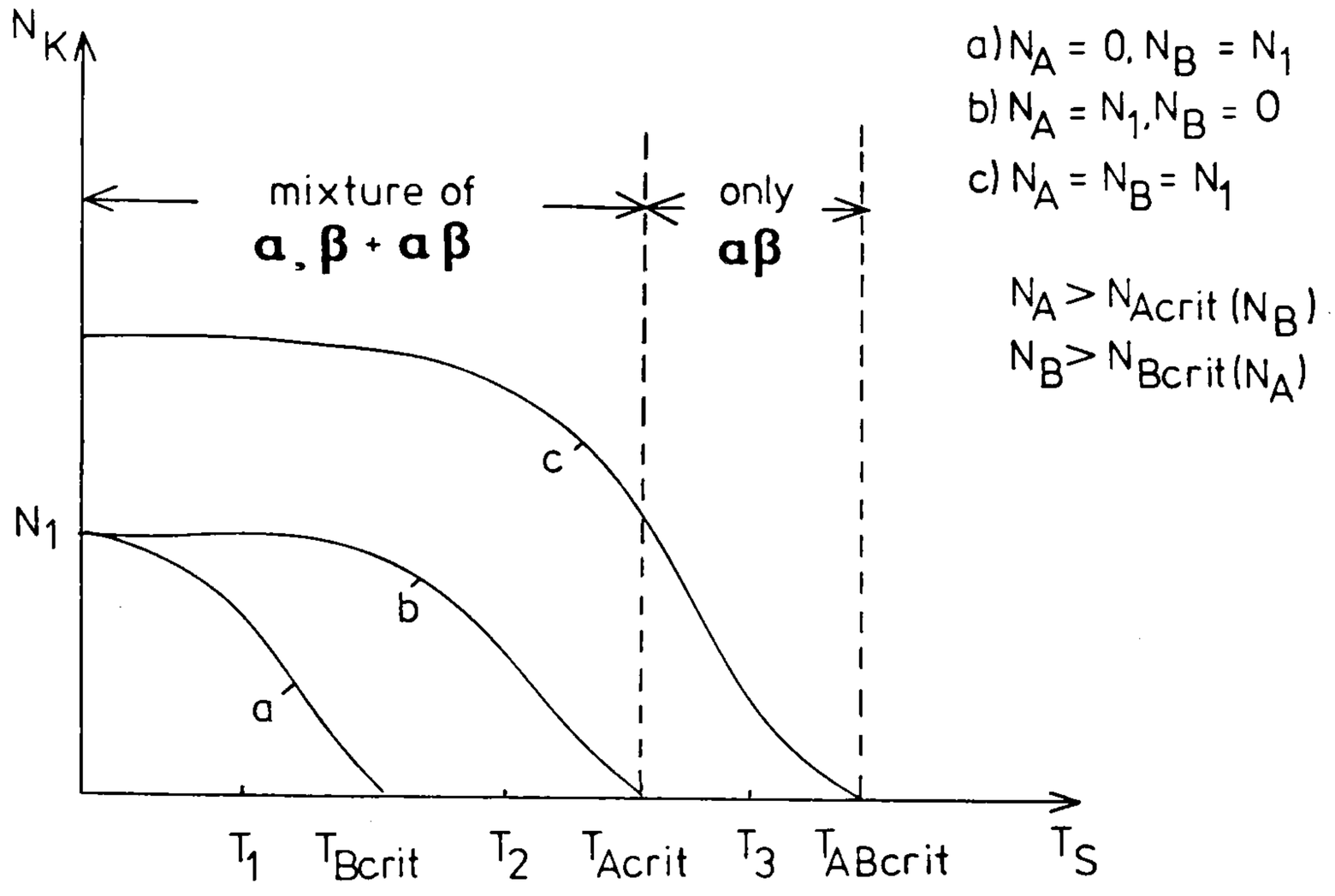
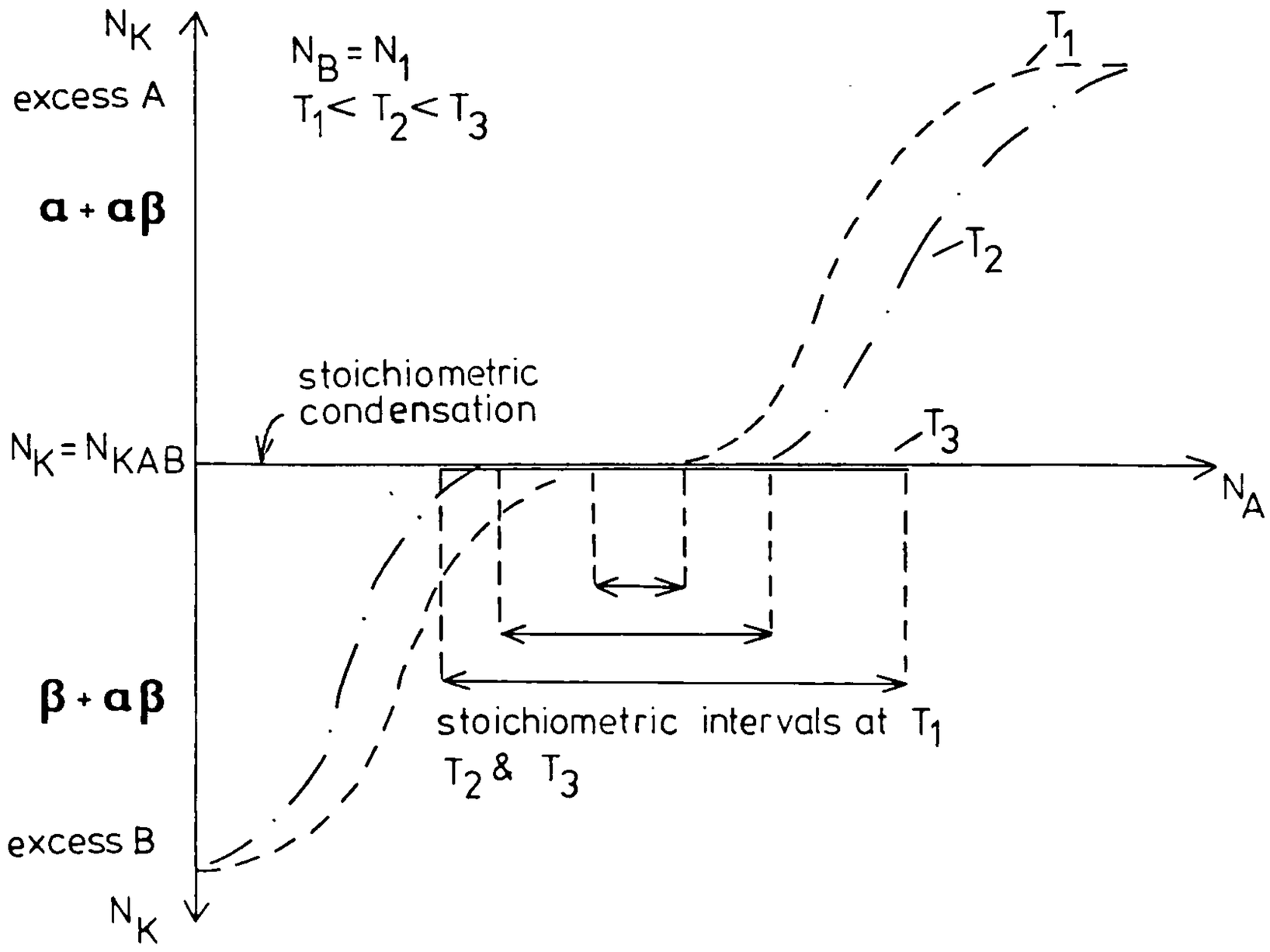


FIGURE 3

"Stoichiometric interval"

The dependence of the composition of the condensation flux, N_K, on the incident flux, N_A, and the substrate temperature, T_S.



The overall condensation flux, N_K^*, decreases with increasing substrate temperature due to the temperature dependence of equation (1) (density of adsorbed particles).

Figure 3 shows the increase of the "stoichiometric interval" (i.e. the range N_A or N_B can vary allowing only the molecule to condense) with increasing substrate temperature.

Condensation of Cadmium Sulphide

CdS is less volatile than its constituents, and therefore fulfills the necessary condition for stoichiometric condensation.

$$p_{eCdS} < p_{eCd} , p_{eS_n}$$

Sulphur is more volatile than cadmium, therefore the critical substrate temperature for sulphur condensation is lower than for cadmium condensation. The critical substrate temperature for sulphur is dependent on the equilibrium pressure, p_{eS_n}, which varies with the relative quantities of sulphur molecule in the vapour. Both T_{Cdcrit} and $T_{S_n crit}$ are dependent on the impinging rates of cadmium and sulphur. Experimentally, critical substrate temperatures have been found or deduced for a variety of substrates and widely differing constituent impinging rates.

$$T_{S_n crit}{}^{3,15} = 20 - 40^{\circ}C$$

$$T_{Cdcrit}{}^{3,15} = 150 - 200^{\circ}C$$

$$T_{CdScrit}{}^{5,16,17} = 380 - 500^{\circ}C$$

Films condensed on to low temperature substrates, i.e. less than $50^{\circ}C$, are cadmium rich and are black in colour (Even small

* where $N_K = N_{KA} + N_{KB} + N_{KAB}$

grains of cadmium have been detected[19]). At higher substrate temperatures the films are more stoichiometric and appear reddish-brown on Germanium substrates, or orange-yellow on glass substrates. (The films have a colour that more closely resembles that of bulk crystal CdS at the higher substrate temperatures.)

The rate of condensation decreases with increasing substrate temperature even though the impinging rates may be constant[20]. The sticking coefficient of a vapour is the ratio between the rate of condensing material and the rate of the impinging material.

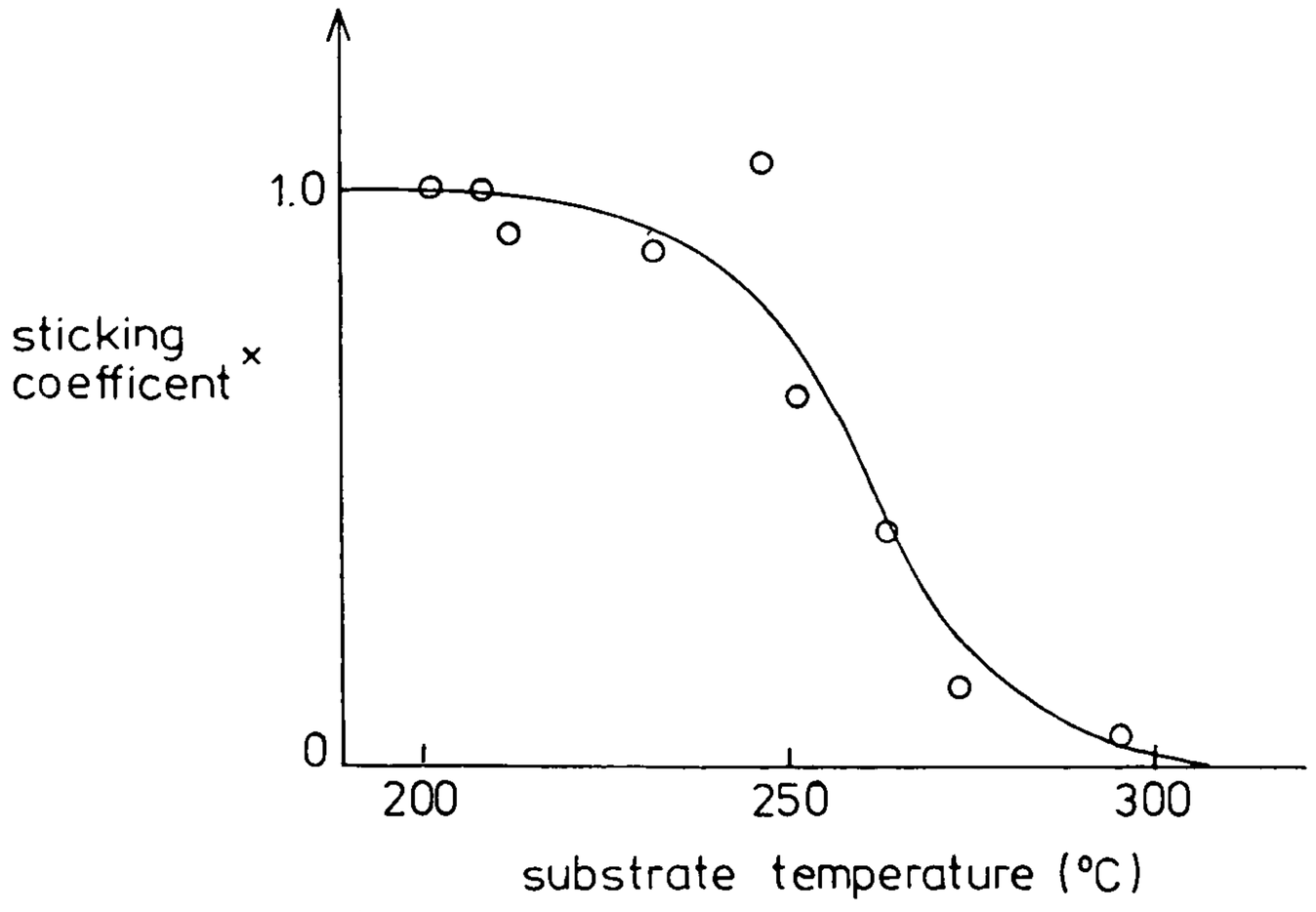
Figure 4 shows the sticking coefficient as a function of substrate temperature. (The sticking coefficient was deduced from the comparison of the thicknesses of CdS condensed on hot and cold substrates after exposure to the same amount of vapour.) No difference in the sticking coefficient between glass or Germanium substrates was observed for the range of impinging rates* 1000 to 6000 Å/min.

The sticking coefficient is independent of the impinging rate except at very low rates when a time delay occurs before the start of condensation. The time delay, t_D, decreases with increasing impinging rate and decreasing substrate temperature. t_D is also dependent on the energy of the vapour/substrate interface. (t_D is much larger for heterogeneous than for homogeneous condensation and is associated with the time necessary for nucleation.)

* Impinging rates were deduced from the condensation of the vapour on a quartz crystal - See Section 2.52.

FIGURE 4

The "sticking coefficent" of CdS vapour, on glass and Germanium, as a function of substrate temperature



× see section 2.52 for measurement technique

Condensation of CdS on to single crystal sodium chloride at 200°C gave the following results

Impinging rate* (Å/min)	Exposure time (seconds)	CdS thickness on substrate (Å)	t_D† (seconds)
80	450	0	>450
200	150	<100	>120
2000	15	≈600	≈0

* Impinging rates were deduced from the condensation of the vapour on a quartz crystal - See Section 2.52.

† t_D = Exposure time - $\frac{\text{CdS thickness}}{\text{impinging rate}}$

Thus for impinging rates less than a critical rate, $N_{CdScrit}$, the time delay tends to infinity and no condensation takes place. At high impinging rates the delay is negligible.

1.43 Application of the model for different CdS evaporation methods

Four methods have been used to grow CdS films by vacuum deposition. The methods used one or two sources with compound and/or elemental source materials.

With knowledge of the condensation model for a binary component vapour it is possible to appraise the relative merits of these methods of growing stoichiometric CdS films.

(i) Separate cadmium and sulphur sources[15] (the "three temperature" method)

The temperatures of both the sources and of the substrate are controlled independently. The rate of each impinging component is controlled by adjusting the temperature of its source. It should be possible using this method to condense stoichiometric films even at substrate temperatures less than $T_{S_n crit}$. At these low temperatures the "stoichiometric interval"

is smaller than at higher temperatures - see Figures 1a and 3 - but with the fine control of component impinging rates, condensation within the interval should be possible. Condensing films at low substrate temperatures takes advantage of higher sticking coefficients.[19]

(ii) Single CdS source[5,19]

Evaporating from a single compound source is the simplest method, but it is not as flexible as the "three temperature" method. The temperature of the source determines both the composition and the pressure of the vapour incident on the substrate.

In Section 1.20 it was seen that, even at constant source temperatures, the evaporation from the compound may be far from stoichiometric and that the rate of evaporation may vary. The variability of the vapour imposes further restrictions on the condensation conditions required for stoichiometry. Only for substrate temperatures greater than T_{Cdcrit} can there be certainty of achieving stoichiometric composition of the film. At temperatures lower than T_{Cdcrit} the rate of impinging sulphur and cadmium cannot be controlled sufficiently to ensure condensation within the "stoichiometric interval". The rate of impinging sulphur tends to be too low, resulting in cadmium rich condensation[5].

(iii) Separate CdS and sulphur sources[21]

This method partly overcomes the difficulty encountered in the single compound source method

of condensing stoichiometric films at temperatures lower than T_{Cdcrit}. Sufficient sulphur is evaporated by this method to ensure that $N_{Cd} < N_{S_n}$. The evaporation of the compound provides the impinging cadmium, and at substrate temperatures between T_{Cdcrit} and $T_{S_n crit}$ the rate of impinging cadmium controls the rate of condensation of the compound. N_{Cd} must however not exceed N_{Cdcrit} or free cadmium will still condense. But if $N_{Cd} < N_{S_n}$ and condensation takes place under the conditions represented by the region $\alpha+\alpha\beta$ (i.e. Cd + CdS) of figure 1b, then the free cadmium content of the condensed film will be very small.

(iv) Single CdS and sulphur source[22,23]

This method is unsuited for uniform CdS film condensation as the sulphur will be evaporated at a much faster rate than cadmium from the compound.

The first condensed layers of the film will be stoichiometric if the substrate temperature is greater than $T_{S_n crit}$, but the pure sulphur in the source will quickly be consumed and further evaporation will be solely of the compound (as in method (ii)). This method is more suited for evaporation of a GaAs and Ga mixture[24], where at the same temperature, the vapour pressure of the compound and element are sufficiently close for the method to be effective.

In Chapter 3 the improvement of the structural quality of the condensed film with increasing substrate temperature will be

discussed. Bearing this improvement in mind, the advantage of condensing stoichiometric films at low substrate temperatures does not appear to be too relevant, unless condensation at higher temperatures is prohibited by low sticking coefficients. (This restriction does not apply to CdS condensing on Germanium or glass substrates.) Thus the main advantage of the "three temperature" method at substrate temperatures greater than T_{Cdcrit} is that it gives direct control over the incident fluxes N_{Cd} and N_{S_n}, and hence control over the condension rate of CdS.

1.44 Implications of the model

Günther's model describes all the necessary conditions for stoichiometric growth of a binary component vapour. Stoichiometry in the model is assessed at a macroscopic level. At a microscopic level within the "stoichiometric interval", films may have a significant lack of stoichiometry and this can exercise a profound effect on the electrical characteristics of the film. stoichiometry at the macroscopic level is sufficient however to allow the nucleation and growth theory described in Section 1.30 to be valid.

CHAPTER 2

2.00 EQUIPMENT AND TECHNIQUES USED FOR FILM GROWTH

2.10 INTRODUCTION

This chapter describes the equipment and techniques used to evaporate CdS films from a single compound source. The lay-out, operation and performance of the equipment as well as the accuracy of the measuring apparatus are also discussed.

2.20 VACUUM EQUIPMENT

The equipment used, shown in Figure 5, consisted of a working chamber of a stainless steel well with a twelve inch bell jar pumped by a two-stage rotary pump, a 50 litre/s ion pump and a titanium sublimation pump.

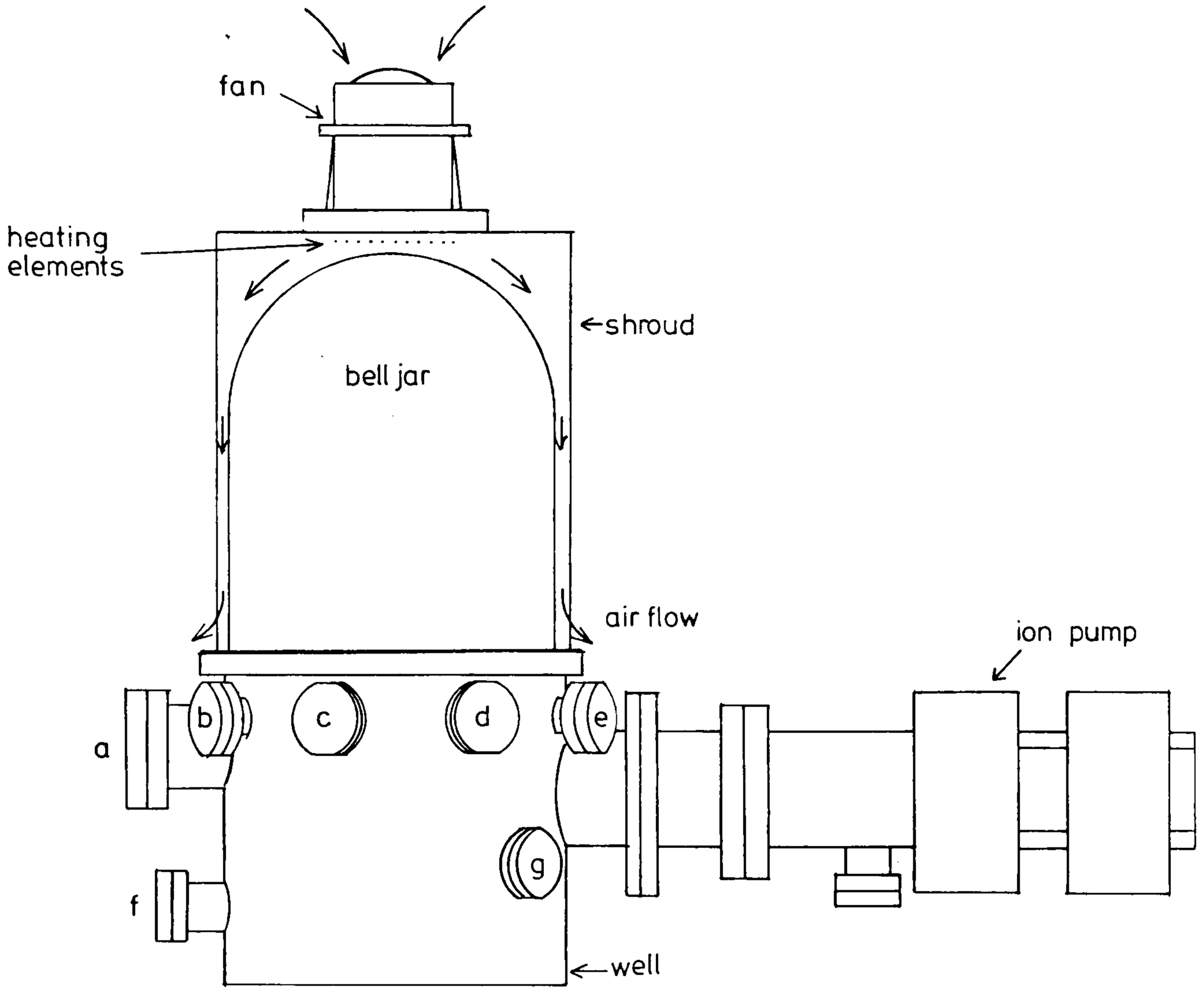
The system is initially evacuated to below 5×10^{-3} torr (mm Hg) by the rotary pump. (Hydrocarbon contamination by the rotary pump fluids is reduced by a bakeable Zeolite trap between the rotary pump and the chamber). The ion pump may be started at this pressure and the rotary pump isolated from the system. The ion pump, in conjunction with the sublimation pump (operated regularly for short periods), pumps the system to its final pressure. The pressure of the system is measured with an ionisation gauge located within the well of the chamber, and is between 2 and 5 times higher than the pressure in the ion pump.

2.21 System bake-out

The system is mildly baked-out at temperatures in the range 80 to 110^{o}C. The ion pump and the chamber well are wrapped

FIGURE 5

The High Vacuum Equipment - General Layout



Port Assignments

Port a : Water cooling for thickness monitor
Port b : Ionisation Guage
Port c : Electrical connections for thermocouple and PRT
Port d : Not used
Port e : Water cooling for electron gun
Port f : Sublimation pump
Port g : Connection to rotary pump via valve and Zeolite trap

Ports not shown

Diagonally opposite d : Electrical connections for substrate heating block
Diagonally opposite c : Linear motion drive for shutter

with heating tape and enclosed by a layer of reflective aluminium foil. The bell jar, which is also enclosed in a reflective shroud, is baked-out by a fan mounted above it and blowing hot air. The apparatus in the chamber and the chamber itself are radiantly heated by the substrate heating block. The bake-out increases the rate of out-gassing of the adsorbed gases from all surfaces in the system and reduces the water vapour in the system.

The heating of the ion pump and chamber well remains on during loading and unloading, i.e. while the system is open to the atmosphere, enabling a shorter pump down cycle time by reducing the water vapour and other contaminant gas adsorption. The fan above the bell jar is also used to cool the bell jar after bake-out and while the substrate heating block is on.

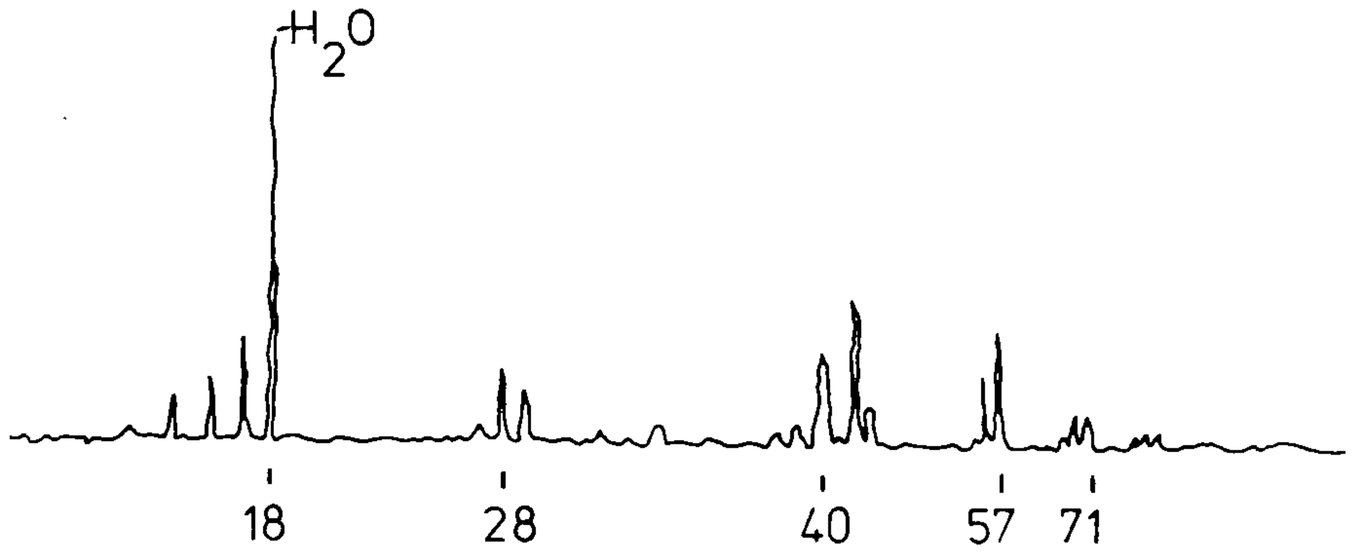
2.22 Performance

The ultimate pressure of the system without bake-out is 3×10^{-7} torr in 5 hours, and with the 2 hour bake-out 10^{-8} torr in a total of 6 hours. Figure 6a shows the mass spectrograph of the residue gases at 2×10^{-8} torr. (With the mass spectrometer apparatus on the system the bake-out is not as thorough as it would normally be). The predominant peak shown on Figure 6a is water vapour and a large mass spectra was also observed for hydrogen. At higher pressures water vapour is even more predominant over the other gases shown in Figure 6b, the mass spectrograph for the residue gases at 6×10^{-8} torr. The peaks also show the presence of organic and hydrocarbon as well as atmospheric gases.

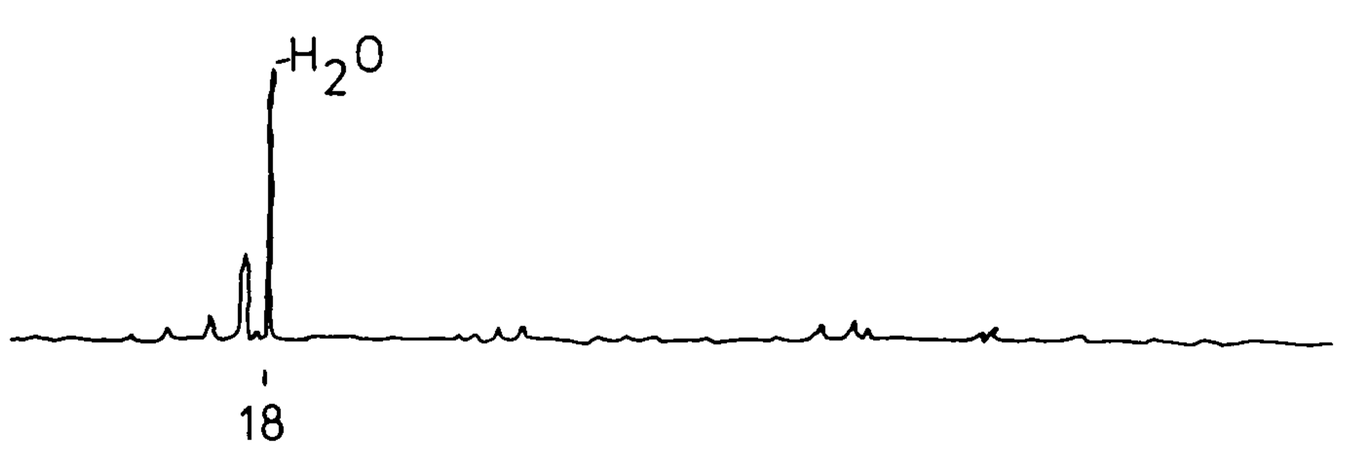
FIGURE 6a, b & c

Mass Spectragraphs

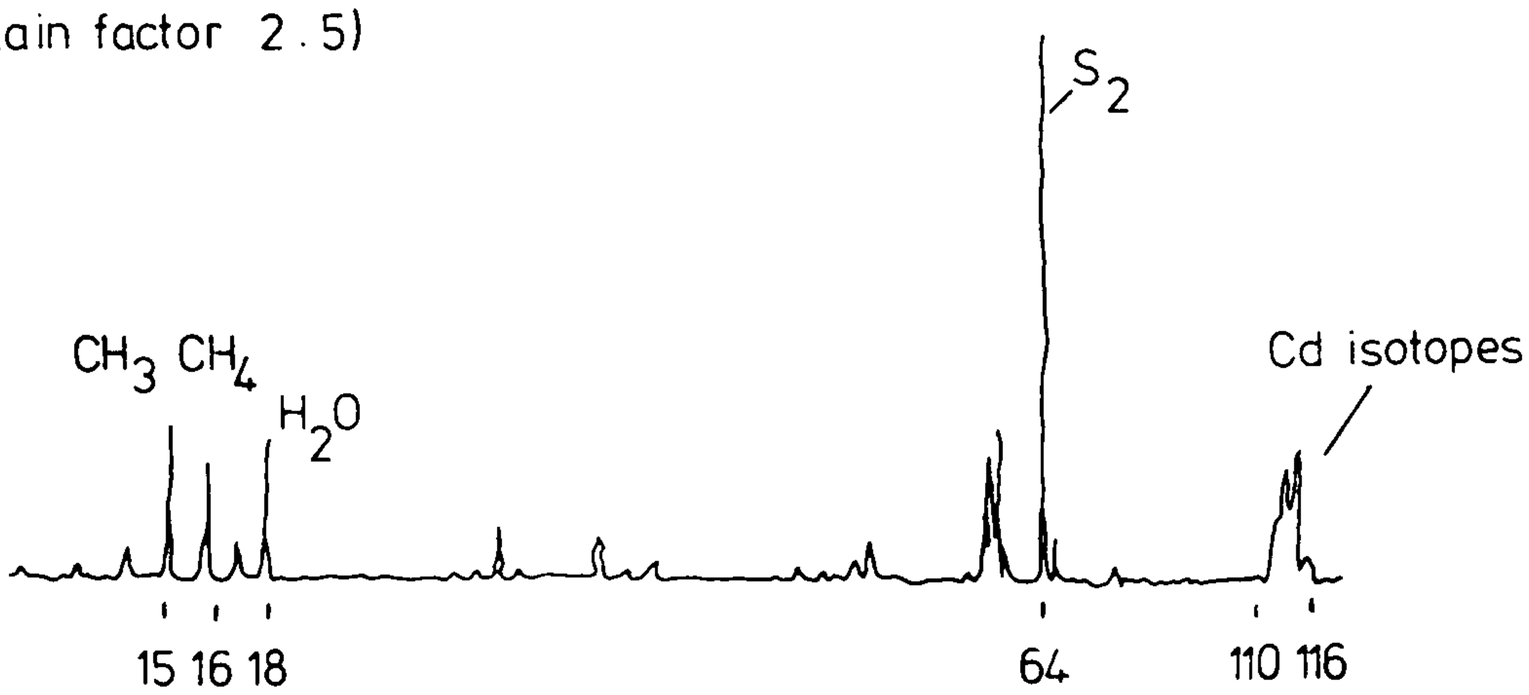
a) Residue gases, 2×10^{-8} torr after bake-out (gain factor 10)



b) Residue gases, 6×10^{-8} torr (gain factor 2.5)



c) Vapours present during CdS evaporation, 2×10^{-7} torr (gain factor 2.5)



This type of system is relatively free of hydrocarbon contamination without having the elaborate baffles and cold traps associated with oil diffusion pump systems capable of similar low pressures. The main disadvantage of the ion pump system is the relatively slow pumping speeds and thus long pump down cycle times.

2.30 CHAMBER EQUIPMENT LAY-OUT

Figure 7 shows the general lay-out of the equipment inside the working chamber. The focussed electron beam evaporator is mounted centrally in the chamber and emits a stream of vapour vertically upwards. The substrate holder and heating block are mounted 3.5cm directly above the evaporator.

The shutter, which is moved by a linear motion drive operated externally, can shield the substrate from the evaporator.

The thickness monitor crystal is positioned to intercept part of the vapour stream which is not intercepted by the shutter positioning.

2.40 FOCUSSED ELECTRON BEAM GUN EVAPORATOR

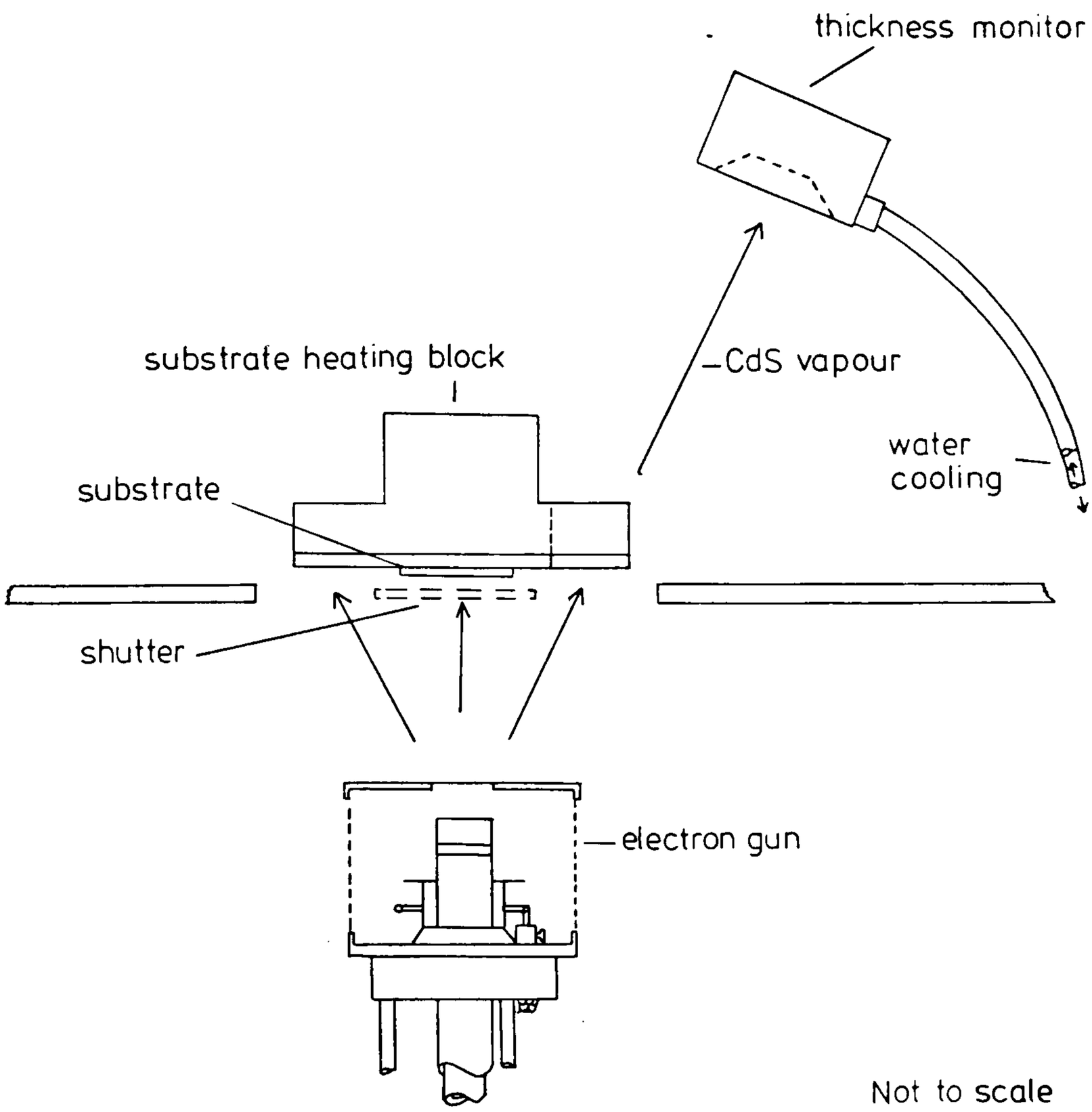
2.41 Operation

The electron beam gun, shown in Figure 8, heats the evaporant by electrostatically focussing the electrons emitted from the filament on to a region of the evaporant surface. The evaporant is contained in a water-cooled hearth which conducts away the heat.

The heat loss through conduction allows only the evaporant in the near vicinity of the bombarding electron beam to melt and

FIGURE 7

Working Chamber Equipment Lay-out



Not to scale

FIGURE 8

Focussed Electron Beam Evaporator

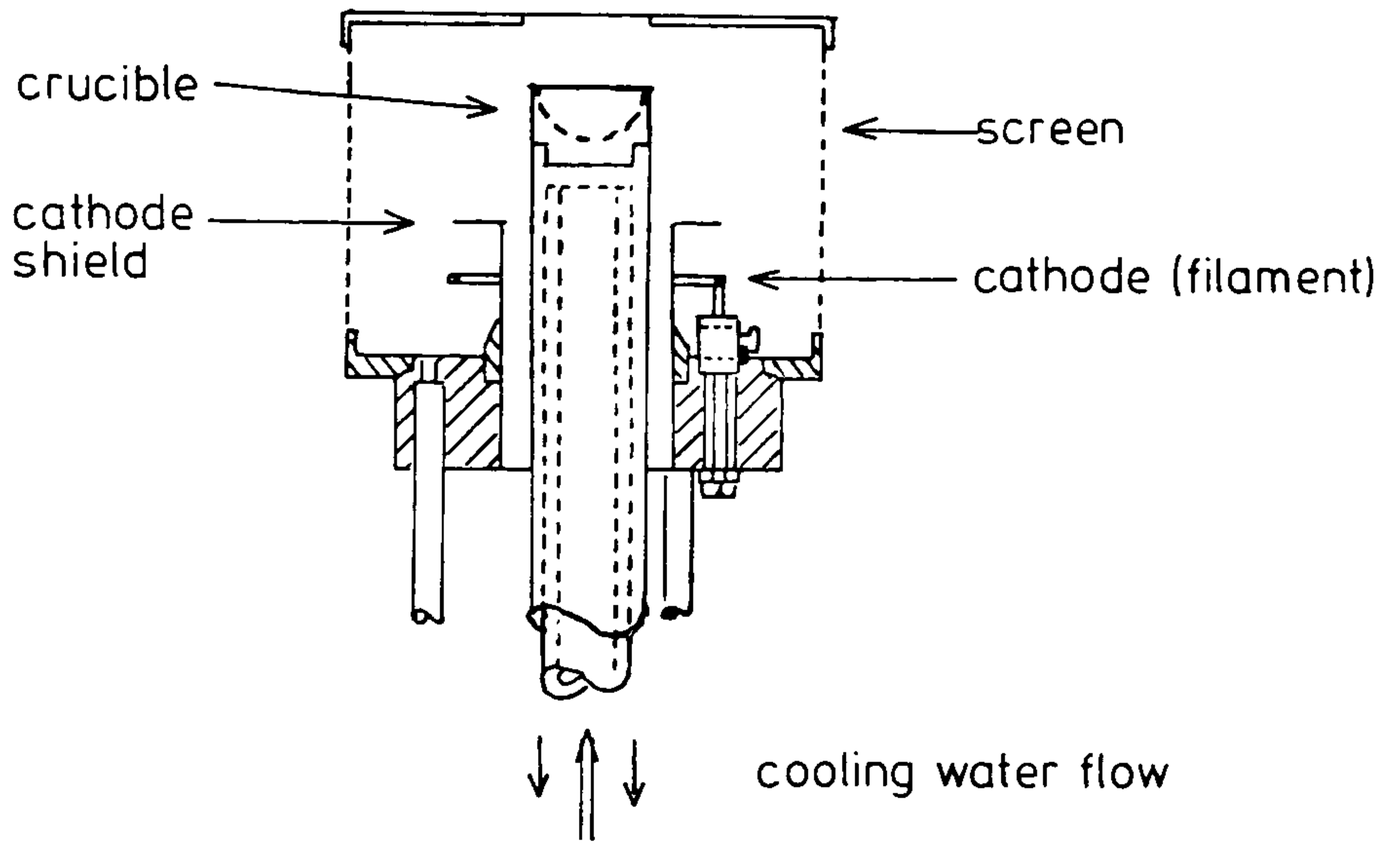


FIGURE 9

Variation of the spot size during the evaporation

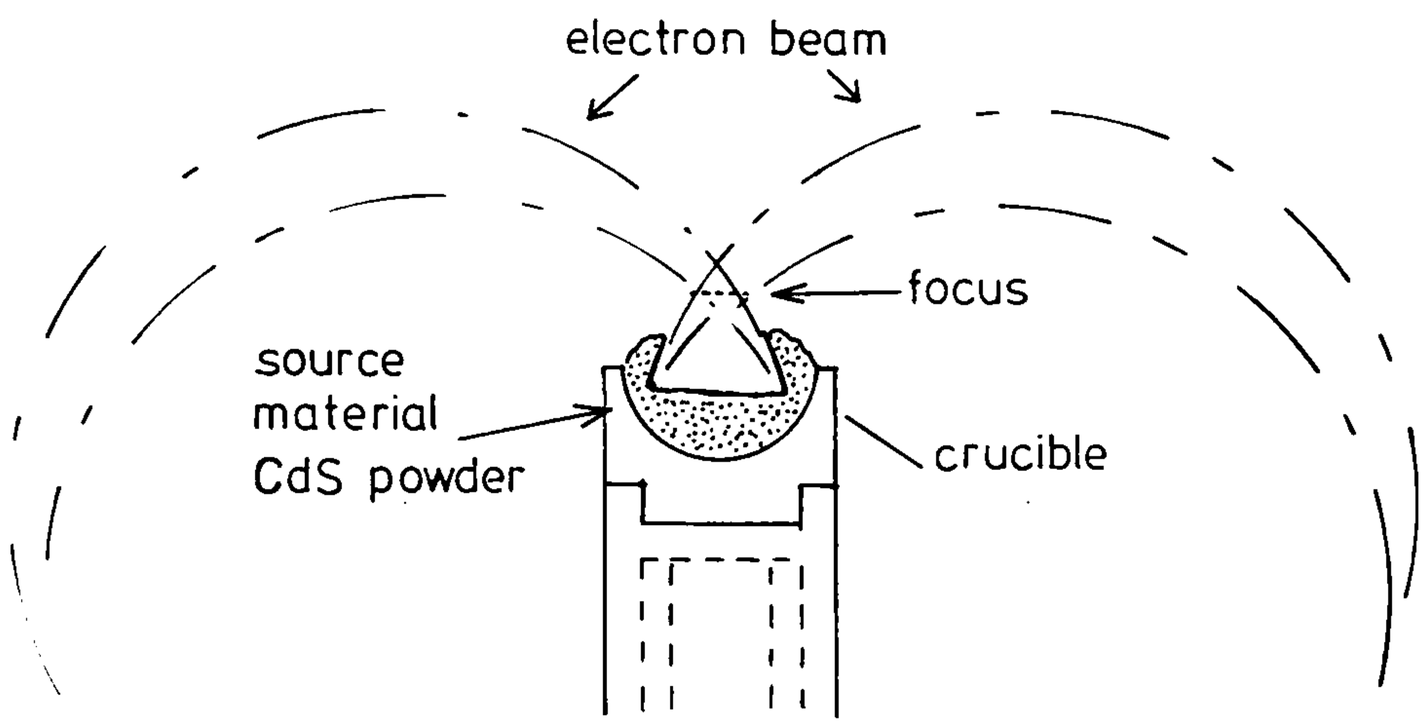
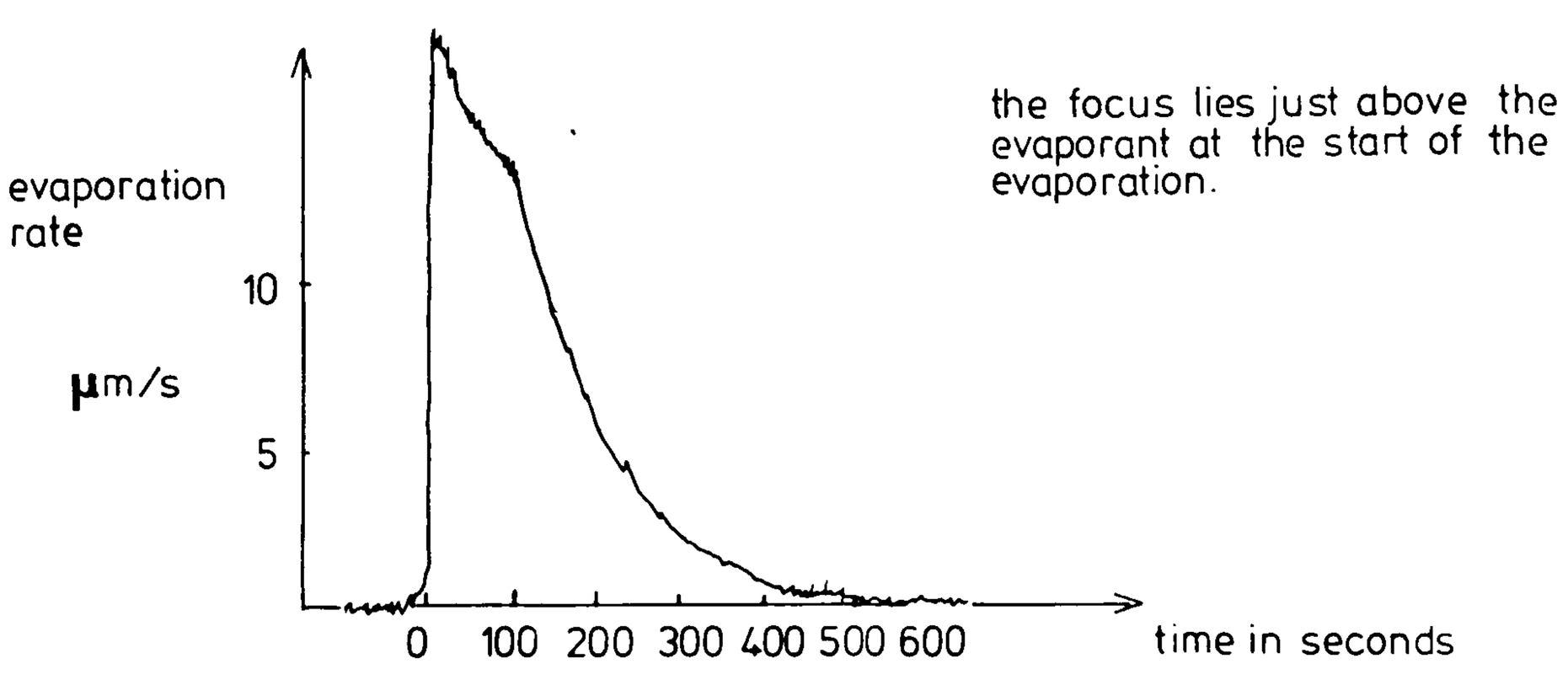


FIGURE 10

Change of Evaporation Rate with Time at constant electron beam power



evaporate. (CdS tends to sublimate at temperatures lower than its melting point).

Using the "cold crucible" type of evaporator reduces the contamination likely from a hot hearth/evaporant interface by ensuring that the hearth is always relatively cool. Contamination of the evaporant by emission of particles from the filament is prevented by the shielding of the electron gun, i.e. the evaporant is out of line of sight with the filament.

2.42 Degas

Out-gassing of the filament and parts of the gun assembly which are subjected to radiant heating by the filament and heated evaporant, can also produce significant contamination during evaporation.

The background pressure increases considerably during this out-gassing, e.g. pressure has been observed to increase from 5×10^{-8}torr to 8×10^{-7}torr. The electron gun, and to a certain extent the evaporant are degassed by operating the gun for a short time at higher powers than are normally used for evaporation. (The substrate is protected by a shutter during the degas).

After the background pressure has returned to its pre-degas value, the gun may again be operated, but the out-gassing only results in a pressure increase to 2×10^{-7}torr.

2.43 Characteristics and performance

The localised hot spot on the surface of the evaporant provides a stream of vapour which escapes from the evaporator by means of the hole in the screen. The size of the spot on

the evaporant surface is determined by the position of focus of the electron beam. The position of focus is determined by the electrostatic field strength and the geometry of the evaporant, hearth and screen positions.

Figure 9 shows the change in spot size for the normal case where the focus is just above the evaporant surface at the beginning of the evaporation. During the evaporation, the evaporant is consumed and as its surface retreats from the focus position the spot size increases, i.e. the electron beam at the surface of the evaporant becomes unfocussed. If the electron beam power* remains constant as the area increases, the temperature of the spot decreases because of the reduction of the incident power density. The rate of evaporation from the spot decreases due to the reduction of the overall temperature which is not compensated by the increase of the effective area of the spot. Figure 10 shows the change of the rate of evaporation with time, at a constant electron beam power. The rate of evaporation, as recorded by a quartz crystal thickness monitor, may be kept constant by increasing the beam power during the evaporation. At low rates of evaporation, e.g. 0.13mm/min of evaporant, the rate of adjustment of the beam power necessary for a constant rate of evaporation may be accomplished manually.

At most of the evaporation rates used, a certain amount of spitting of unevaporated CdS from the hearth was observed, particularly at high evaporation rates. (This was due to the CdS in the hearth being in powdered form.)

* Electron beam power = emission current x electrostatic field voltage

Varying the source temperature not only controls the rate of evaporation per unit area, but also determines the kinetic energy[11] of the evaporated cadmium and sulphur and the average size of the sulphur molecule[22].

The limited capacity of the hearth to hold evaporant was increased by the insertion of a molybdenum crucible - see Figure 8. This addition changed the overall characteristics of the evaporation by reducing the rate of heat conduction from the evaporant. With the crucible, evaporation rates greater than 6000Å/min are not possible due to thermal run-away effects.

Figure 6c shows the mass spectragraph during an evaporation of CdS. The mass spectrometer was positioned 35cm from the evaporator and intercepted part of the CdS vapour stream. The normal substrate to evaporator distance was 3.5cm, so the cadmium* and sulphur peaks will indicate approximately one hundredth of the cadmium and sulphur that would normally be intercepted by the substrate.

The background gases that are represented by the other peaks are likely to be typical, in both variety and size, of the contaminants in the vicinity of the substrate, because the residual gases are much less affected by distance from the evaporator. Comparing Figures 6b and 6c (the spectro-graphs for before and during the evaporation), it can be seen that the major increase of contamination by operation of the gun appears to be by desorption of organic compounds, emphasising that even higher standards of cleanliness are

* Cadmium has a range of peaks, 110 to 116, relating to its variety of isotopes

required than were then considered necessary. The only sulphur molecule that was detected in the range of evaporation rates normally used was S_2 represented by the peak at 64. The ratio of the sizes of the sulphur and cadmium peaks have been observed to change during the evaporation, indicating changes in the relative composition of the vapour. The ratio has also been shown to be dependent on the purity of the source material. (Eagle Pitcher Grade A CdS produces a vapour with a higher sulphur content than Optran, obtained from BDH Ltd, which is less pure)

2.50 THICKNESS AND RATE OF CONDENSATION MEASUREMENT

2.51 Thickness uniformity and measurement

The thickness distribution of a film evaporated from the electron beam gun is similar to that of a point source, i.e. the thickness is inversely proportional to the square of the source to substrate distance. The thickness of the evaporated film was estimated from the interference fringes of sodium light at the edge of the film, i.e. where the film on the substrate makes a step change in thickness.

At the source to substrate distances normally used, the thickness at the centre of the film is only 5% greater than the edge of a 20mm diameter substrate. At this distance sufficiently thick films could be grown and still be beyond the range of the spitting from the evaporation referred to in Section 2.43.

2.52 Quartz crystal thickness monitor

The thickness and condensation rate of the film on the substrate is monitored indirectly during the evaporation by a quartz crystal thickness monitor.

Part of the vapour stream from the source condenses on an area of the quartz crystal and is proportional in quantity to the majority of the vapour stream which is incident on the substrate - see Figure 7. The crystal frequency of oscillation changes in proportion to the mass condensing on it. The thickness of the film, and by differentiation the rate of condensation, may thus be measured.

The thickness of the film condensed on the substrate, in comparison with that on the crystal, depends on the relative positions of the source, substrate and crystal, as well as on their temperatures and vapour supersaturations.

The frequency of oscillation of the crystal is also sensitive to temperature variation and during an evaporation the crystal, by the necessity of its positioning, must be subject to radiant heat from the evaporator. The crystal is mounted in a water-cooled holder which allows only a small area to be subjected to radiant heat, and thus only small variations of crystal temperature are allowed.

If the temperature of the crystal varies significantly a change in the frequency of oscillation will occur without associated condensation. Almost all the CdS vapour incident on a cold substrate will condense. At higher substrate temperatures the sticking coefficient reduces, until at temperatures greater than $T_{CdScrit}$ no condensation is possible. Thus the relative thickness of CdS on the quartz crystal and the hot substrate will depend on the substrate temperature - the crystal temperature remaining constant. It is thus necessary to calibrate the observed frequency change of the crystal to the thickness

of the film condensed on the substrate* over the range of possible substrate temperatures.

This calibration also allows for the relative positioning of the crystal and substrate. Figure 4 shows the calibration, indicating the sticking coefficient as a function of substrate temperature. The impinging rate of the vapour at low substrate temperatures is therefore approximately the condensation rate. (Sticking coefficient $\simeq 1$). At higher substrate temperatures the condensation on the crystal still indicates the impinging rate of the vapour on the substrate but not the condensation rate.

The surface of the crystal is covered with a previously evaporated film of CdS. Thus the time delay before significant condensation is likely to be lower on the crystal than on the substrate, because the crystal condensation is homogeneous and on a cold surface. From mass spectrometer work it was observed that for the same condensation rate on the quartz crystal the relative quantities of sulphur and cadmium in the vapour could be considerably different. This observation shows that the condensation on the crystal, particularly at high substrate temperatures, is likely to indicate inaccurately the condensation on the substrate. Almost all the vapour incident on the crystal condenses, i.e. the condensation rate of the film on the crystal is proportional to $N_{Cd} + N_S$, but the substrate at higher substrate temperatures is more selective.

The thickness of the film condensed on the substrate at temperatures greater than T_{Cdcrit} is proportional to the flux of the

* The substrate, at each substrate temperature, is exposed to the same rate of impinging fluxes for the same time.

less available component, e.g. $N_K \simeq N_S$ if $N_{Cd} > N_S$. Thus the condensation on the crystal is likely only to be truly representative of the condensation on the substrate when $N_{Cd} = N_S$. The misrepresentative crystal condensation could explain a scatter of $\pm$ 10% observed in the calibration at substrate temperatures in the region of 200 to 250°C. The scatter decreases with decreasing substrate temperature and this could be an indication of the average variation in stoichiometry of the incident vapour during an evaporation.

2.60 SUBSTRATE PREPARATIONS

The single crystal Germanium substrates were 2cm diameter discs approximately 0.5mm thick. Intrinsic and a range of p-type Gallium doped Germanium substrates were used. The orientations of the substrate's surface were (110) and (111). The glass substrates were laboratory standard microscope slides cut into 2.5cm squares.

2.61 Substrate polishing and cleaning

The Germanium discs were polished flat by 3μm diamond paste. The discs were degreased and cleaned by ultrasonic agitation in trichlorethylene and then acetone before being washed thoroughly in running de-ionised water. The discs were first blown dry by a strong jet of oxygen and then thoroughly dried on a hot plate in a clean atmosphere. The glass substrates were degreased and cleaned by the same method as the Germanium discs except that the glass substrates were washed in soapy water before degreasing.

2.62 Substrate mounting and heating

The clean substrate was mounted on a stainless steel holder

and held in position by two stainless steel clips. The holder was then bolted, substrate downwards, to the underside of the stainless steel heating block, which was then mounted directly over the evaporator.

The heating block was heated by four helical tungsten filaments contained within quartz sleeves inserted into holes at the top of the block - see Figure 11. The heating block was held by only two ceramic supports so the loss of heat from the block was mainly by thermal radiation. The block was designed to ensure an even temperature distribution over its lower surface.

Due to the high heat capacity and low heat loss of the block when the substrate temperatures were greater than 200°C, about an hour and a half cooling time was necessary to return the block to room temperature.

2.70 SUBSTRATE TEMPERATURE MEASUREMENT

The temperature on the substrate was estimated by use of a Chromel-Alumel thermocouple located close to the substrate on the substrate holder. Figure 12 shows the thermocouple attached to the substrate holder. The hot junction of the thermocouple is heated by conduction along the attaching wire and by radiation from the heating block surface.

The variation in the proximity of the thermocouple to the heating block surface results in a maximum error at 200°C of 5°C, which decreases with decreasing block temperature.

During the evaporation the temperatures of the substrate and thermocouple increase due to radiant heat from the evaporator. The rise in temperature of the substrate is dependent on the

FIGURE 11

Substrate Heating Block

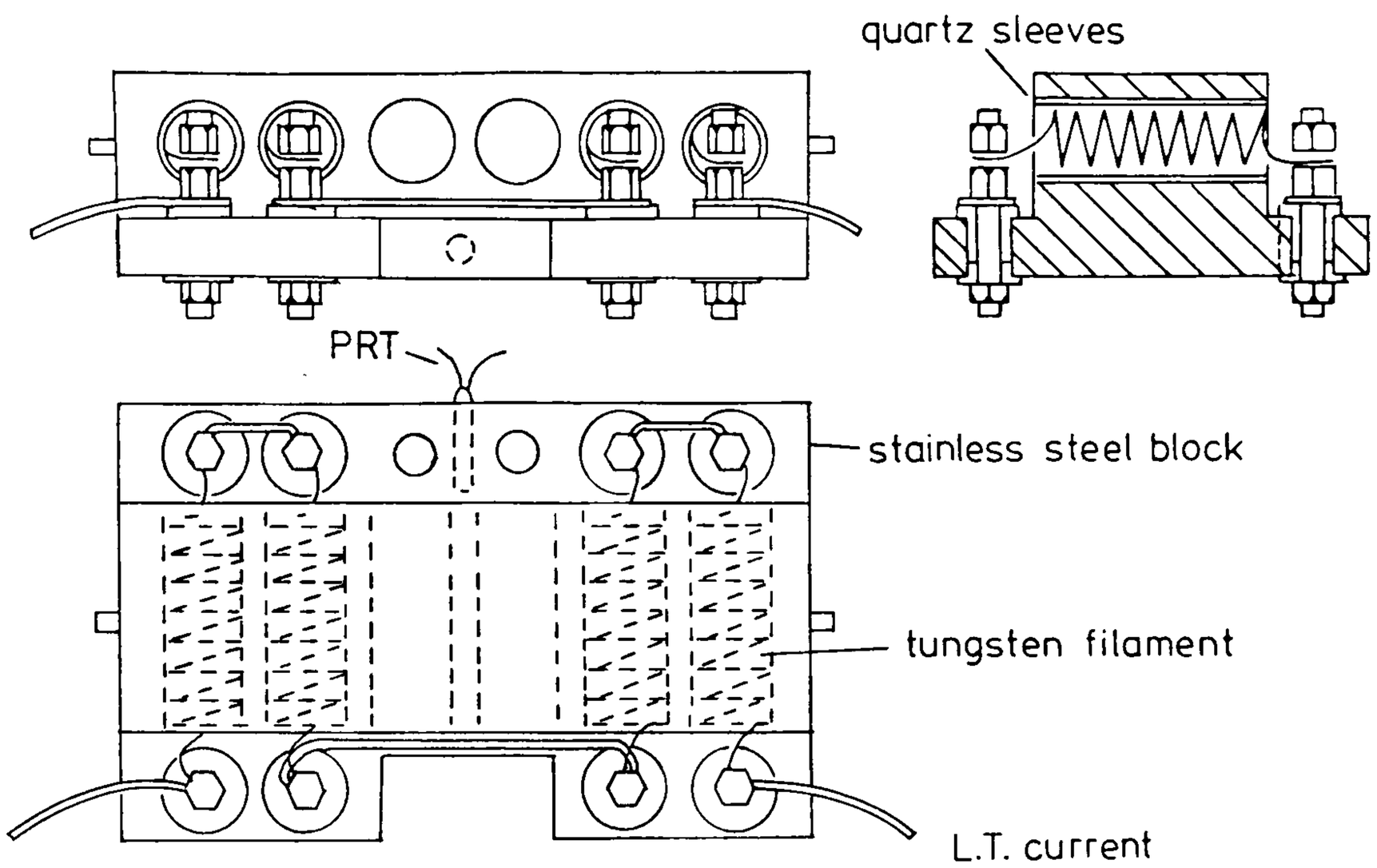
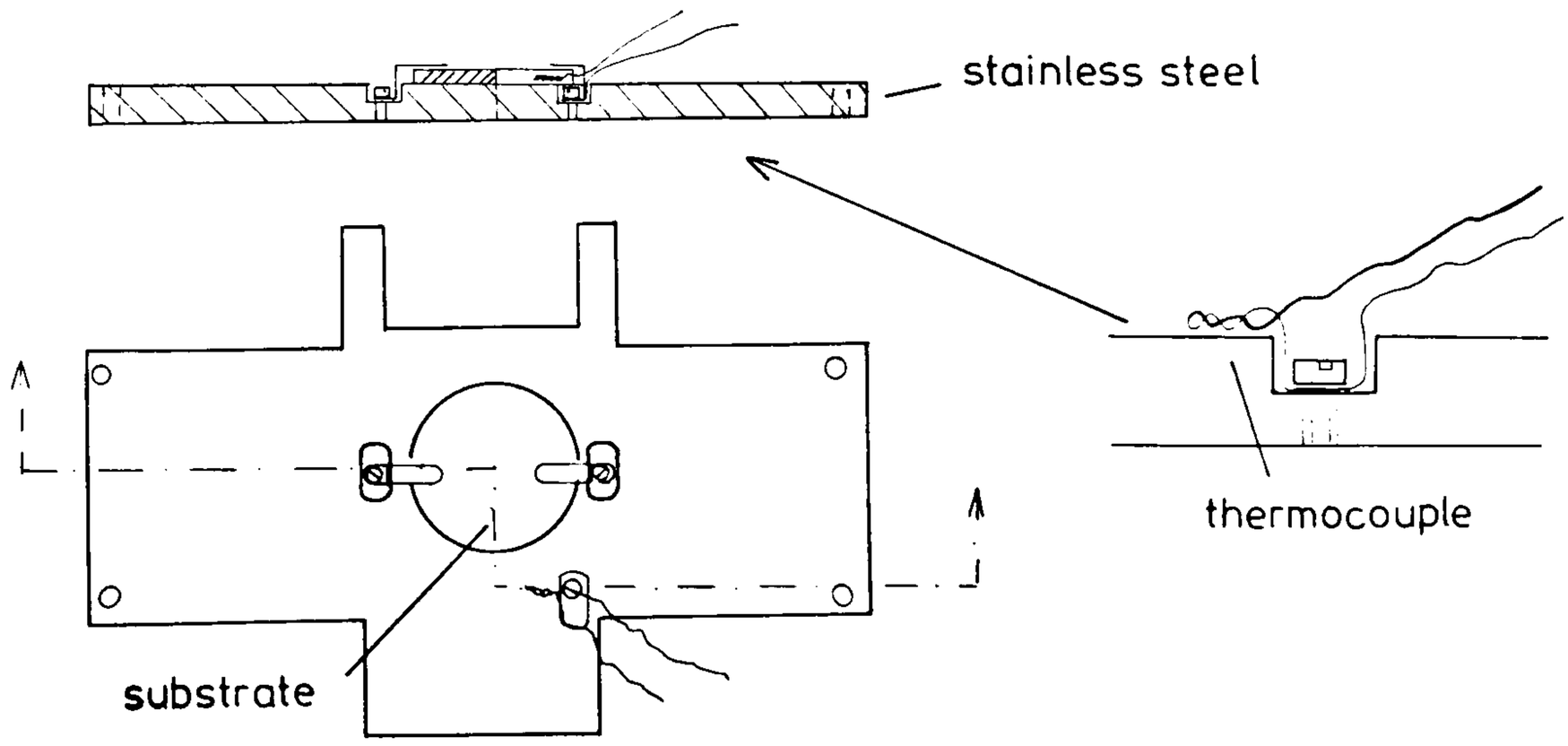


FIGURE 12

Substrate Holder and Thermocouple

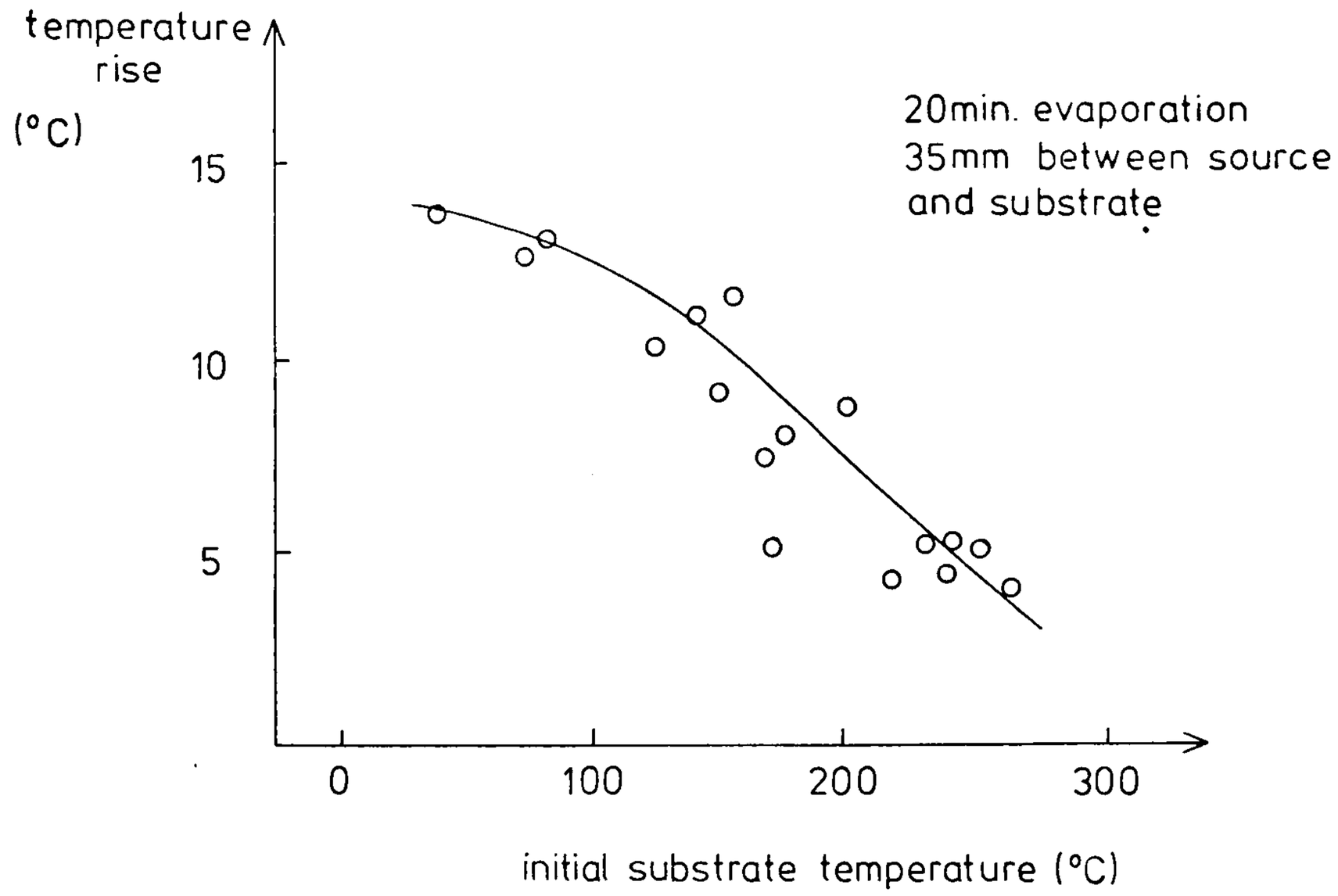


temperature of the source and the initial temperature of the substrate, the separation of the source and substrate and the duration of the evaporation. Figure 13 shows the temperature rise as measured by the thermocouple, as a function of the substrate temperature with all other factors remaining constant. The thermocouple voltage tended to decrease progressively because of the short-circuiting effect of condensing CdS on the thermocouple. This effect became significant only after several evaporations and it was then necessary to remove and clean the thermocouple.

A platinum resistance thermometer (PRT) is located in a close-fitting hole in the heating block and is unaffected by the condensation of CdS. The PRT is calibrated to the temperature of the clean thermocouple and gives a more consistent temperature measurement of the surface. Calibration of the PRT temperature to the thermocouple temperature is only valid once the block temperature is stabilised, i.e. the temperature of the PRT and surface are constant. Thus the PRT cannot be used to measure the increase in temperature of the substrate during the evaporation.

FIGURE 13

Rise in Substrate Temperature
during the evaporation as a function of
the initial Substrate Temperature



CHAPTER 3

3.00 STRUCTURE OF CdS FILMS

3.10 INTRODUCTION

This chapter describes the observed structure of CdS films grown under a variety of conditions. The trends observed follow directly from the theories of nucleation and film growth described in Section 1.30 and are generally true for evaporated films of most materials. The structure and quality of the films, i.e. the size, orientation and crystallographic phase of the crystallites and the density and types of defects, are strongly dependent on the condensation conditions.

3.20 THE EFFECTS OF THE DIFFERENT CONDENSATION PARAMETERS

The structure of a film grown on a particular substrate is strongly dependent on the adatom mobility on the surface of the substrate at nucleation stage. The structure, and particularly the crystallite size of the film in the later stages of growth, are closely related to the density of the nuclei at saturation,[25] which is determined by the adatom mobility.

The mobility of the adatoms is dependent on the kinetic energy of the impinging atoms or molecules, the substrate temperature, and the condensation rate. These factors, as well as determining adatom mobility can individually have a strong effect on the film structure.

3.21 Kinetic energy of the impinging particles

The kinetic energy of the impinging particles, which increases

with increasing source temperature, is reduced by collision with background gas particles.[11] The smaller the kinetic energy of the impinging particles of vapour, the smaller the "in plane" velocity of these particles after they have been adsorbed on to the substrate surface. Thus the adatom mobility and crystallite size are smaller.

If the vapour impinges on to the substrate at an oblique angle, a component of the kinetic energy of the impinging particles is parallel to the substrate surface. This results in larger "in plane" velocity of the adatoms and to larger crystallites than those observed with perpendicularly incident vapours.

3.22 Substrate temperature

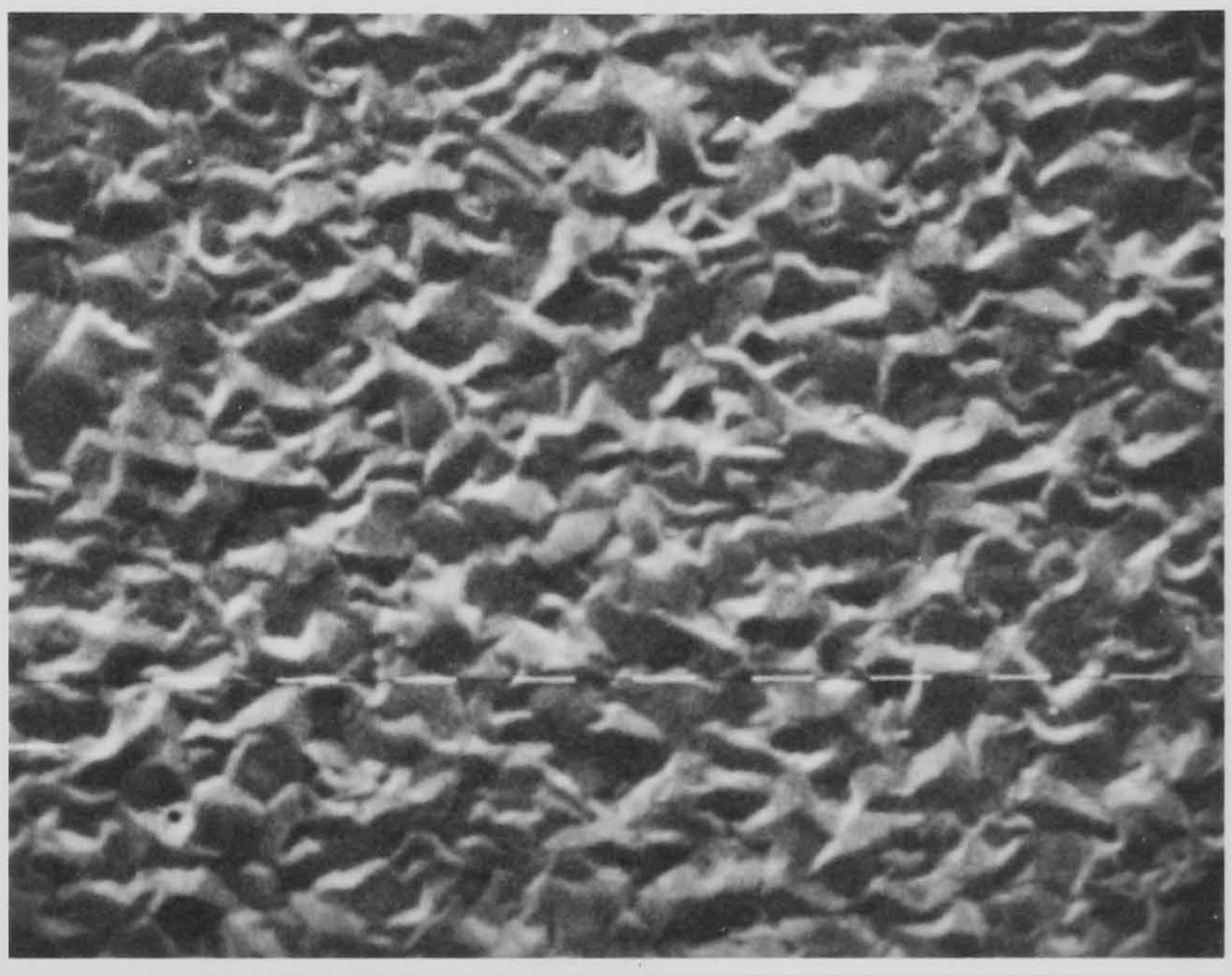
In general, crystallite size and quality increases with increasing substrate temperature.[10,11] Figures 14a and 14b show a much larger crystallite size for a film grown at 200°C compared with a film grown at 70°C . The increase in crystallite size is partly due to increase in adatom mobility, but also to enhanced re-crystallation during the coalescence of the islands at higher substrate temperatures. Improvement in adatom mobility with increasing substrate temperature is also caused by the increased desorption of surface contaminants.

From the model in Section 1.40 it was found that the stoichiometry of the condensed film increases with increasing substrate temperature. Lattice defects have also been found to decrease with increasing substrate temperature.[10]

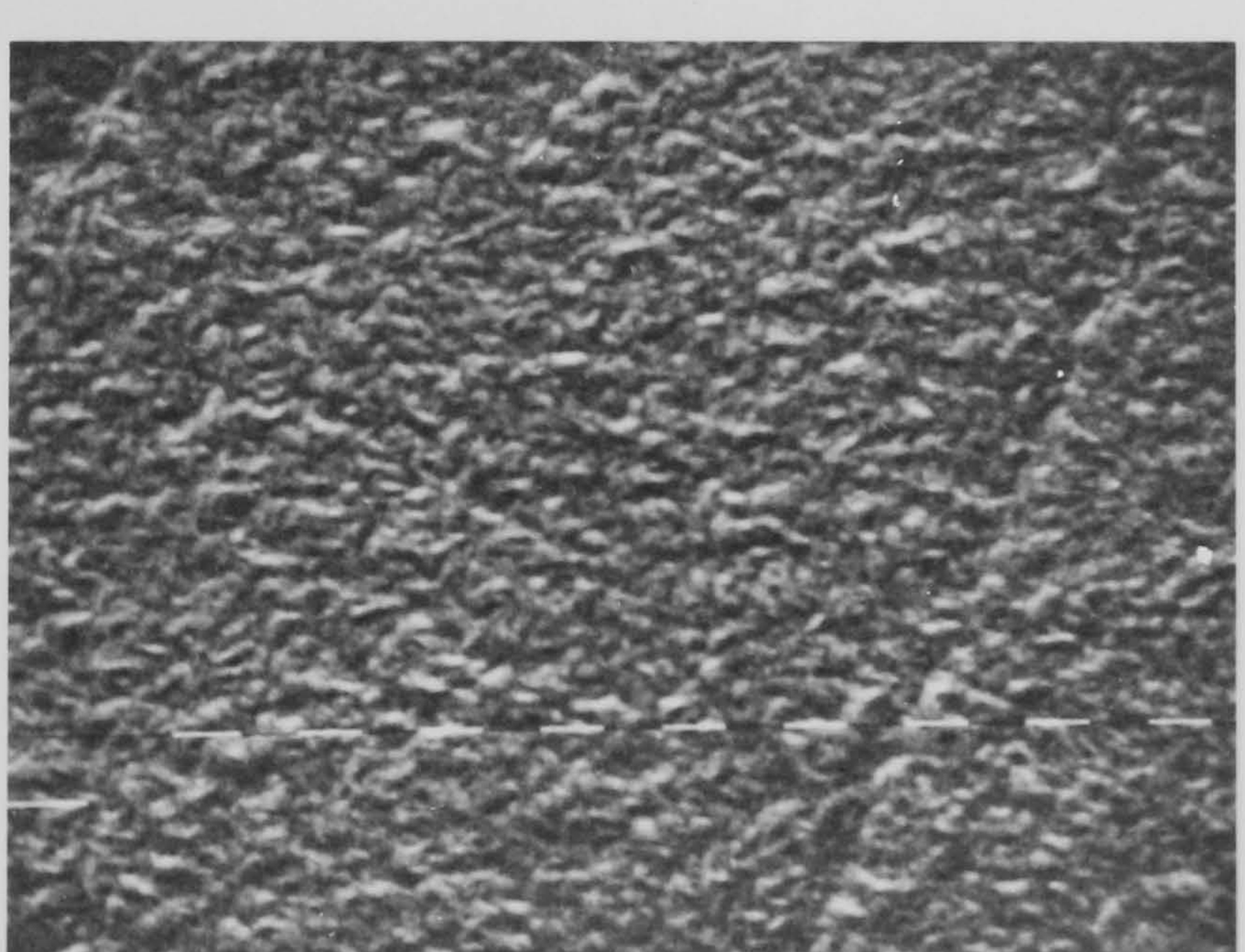
On single crystal substrates epitaxy was observed to improve with increasing temperature.[12] At substrate temperatures

FIGURES 14 a & b

Scanning Electron Microscope photographs
of CdS films, 6 μm thick, at 2400 Å/min.
on Germanium (100)



a) Substrate Temperature 200°C



b) Substrate Temperature 70°C

greater than the epitaxial temperature, the films became perfectly epitaxial, i.e. the film crystal structure is completely orientated with respect to the crystal structure of the substrate although several preferred orientations[13,17] and both the crystallographic phases[17] of CdS may exist.

Increasing the substrate temperature decreases the number of preferred orientations, until normally only one orientation is preferred. Similarly only one crystallographic phase is possible at higher substrate temperatures.

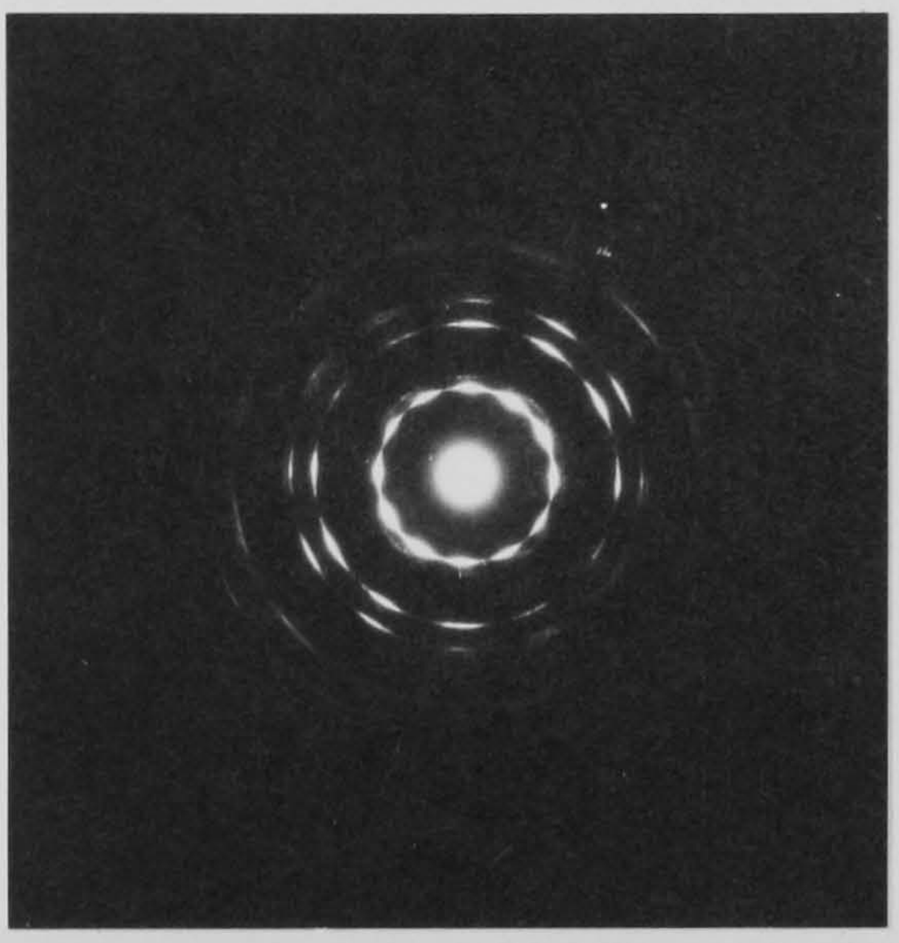
Figure 15a shows the diffraction pattern for CdS grown on NaCl at 170°C. From this pattern it can be seen that the film consists of wurzite (hexagonal type) phase crystallites with the c-axis perpendicular to the substrate surface, and that there is a scatter of crystallite orientation about the c-axis around two preferred orientations at 30° to each other.

Figure 15b, at the higher substrate temperature of 200°C, shows improved epitaxy. The sphalerite (cubic type) phase is dominant and has one preferred orientation. Small amounts of perfectly orientated, doubly positioned, wurzite crystallites are also present.

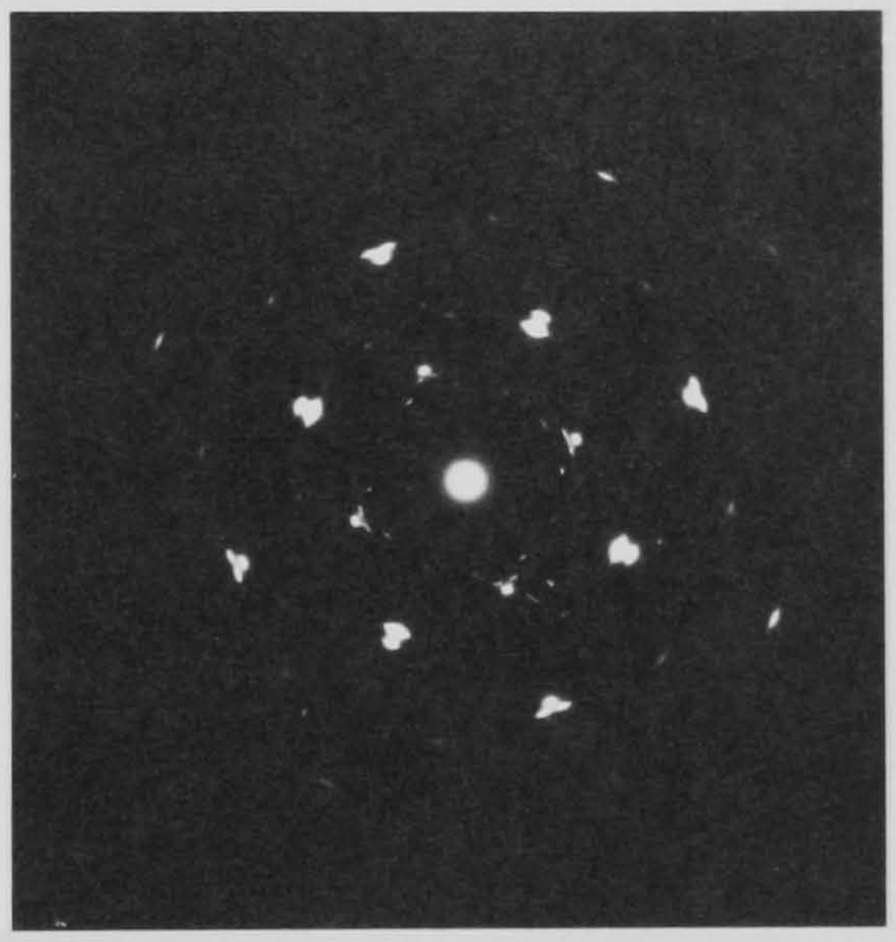
These diffraction patterns indicate the change in structure between partially orientated and epitaxial films with increasing substrate temperature and a change of the dominant crystallographic phase. Similar work by Abdalla, Holt and Wilcox,[17] also on CdS films on NaCl, has indicated that a further increase in substrate temperature will result in a single crystal film, i.e. a film with only one crystallographic phase and one preferred orientation. The precise value of the epitaxial

FIGURES 15 a,b,c & d

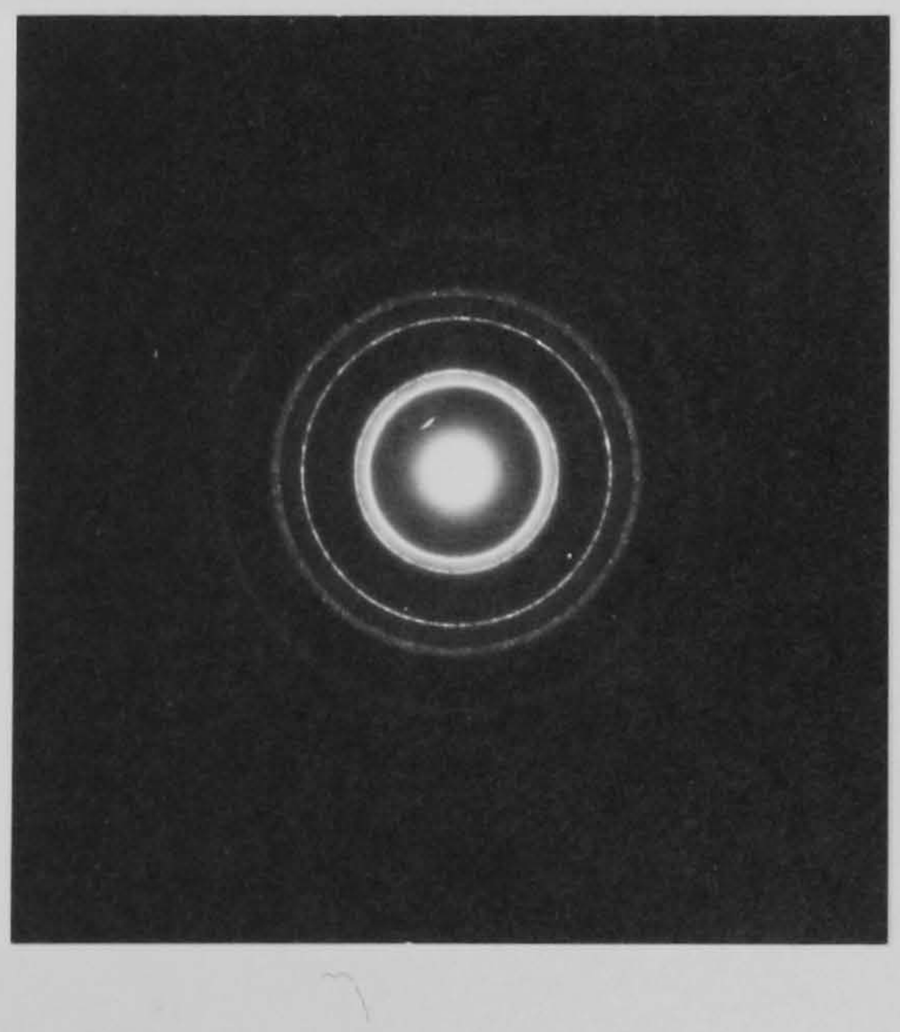
Transmission Electron Microscope diffraction patterns of CdS films grown on NaCl (100)



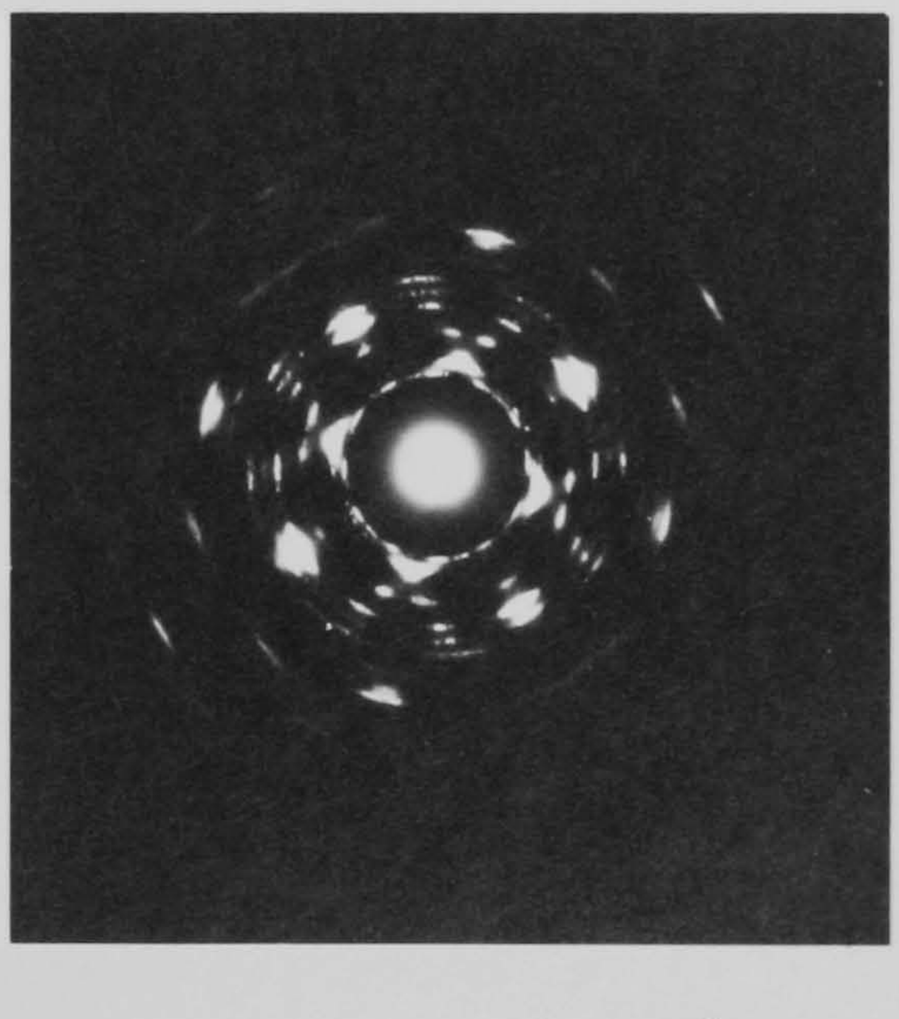
a) CdS on NaCl at 170°C, 700Å thick, at 1000Å/min.



b) CdS on NaCl at 200°C, 600Å thick, at 2000Å/min.



c) CdS on polycrystalline Al at 200°C, 700Å thick, 1000 Å/min.



d) CdS on NaCl at 200°C, <100Å thick, at <300Å/min.

temperature depends on the evaporation system as well as on such parameters as supersaturations, sticking coefficients, and the nature and cleanliness of the substrate.

3.23 Condensation rate

The condensation rate depends on both the vapour supersaturation and the substrate temperature. At high condensation rates, which may be brought about by high supersaturations and/or low substrate temperatures, the adatoms become chemically adsorbed with little surface diffusion. The adatom mobility and thus crystallite size are small. The high condensation rate also results in the "burying" of adatoms in random sites, i.e. chemical adsorption in non-equilibrium positions, by the following arrival of more adatoms and an increase in the density of lattice defects in the crystallites is observed.[10] At very low condensation rates, contamination from the background gases may be sufficiently high to result in a decrease in the structural quality of the film. Commonly, condensation at 600Å/min with a background pressure of 10^{-6}torr produces high quality epitaxial, and even single crystal, films.[16] So condensation at similar and faster rates at background pressures of less than 2×10^{-7}torr should not significantly contaminate the film.

The epitaxial temperature decreases with decreasing condensation rate if the background pressure is sufficiently low, and the quality of the film increases.[16]

3.30 INFLUENCE OF THE SUBSTRATE

3.31 Substrate crystal structure

Amorphous or polycrystalline substrates tend to have randomly orientated nuclei. C-axis orientation towards the impinging

vapour forms during the later stages of growth. Figure 15c shows the diffraction pattern of CdS film grown on to an evaporated film of Aluminium on a NaCl substrate. From the diffraction pattern it can be seen that the Aluminium is polycrystalline and that the CdS film is wurzite with randomly orientated crystallites. The CdS film is 700Å thick and may be too thin to show the progressive c-axis orientation.

CdS grown on single crystal substrates tends to show strong orientation at the nucleation stage. By comparing Figures 15a and 15c, which are diffraction patterns for the same film condensed on the NaCl and the polycrystalline substrates respectively, it can be seen that the film on the single crystal substrate has a high degree of c-axis orientation and is partially orientated with respect to the substrate.

Abdalla, Holt and Wilcox[17] have shown that CdS grown epitaxially on (100) and (110) faces of NaCl has parallel sphalerite structure whilst wurzite forms on the (111) face [the (0001) plane parallel to the surface]. Figure 15b, in agreement with this work, shows a dominant sphalerite structure on the (100) face on NaCl. The film is orientated with the CdS (100) face parallel to the substrate surface. Similar trends have also been found on the three crystal faces of Germanium, though in general the epitaxial temperatures for Germanium are higher.

3.32 Substrate surface preparation

For the growth of epitaxial films it is necessary that the substrate be clean. If the surface of the substrate is disordered, even though the substrate is single crystal, epitaxial

growth may be inhibited. The surface may have contamination in the form of an oxide layer, adsorbed gases from the atmosphere, or chemicals from "cleaning" and polishing. For CdS grown on NaCl it has been found that improving the cleanliness of the substrate surface reduces the epitaxial temperature.[17] Non-epitaxial film on amorphous or polycrystalline substrates also require thorough cleaning to minimise preferential nucleation and the incorporation of the contaminants into the initial layers of the film, as this may result in a lack of adhesion.

In general, it appears that the poorer the order of the substrate surface, either through contamination of a single crystal substrate or simply by the use of disordered substrate, the greater is the likelihood of the formation of wurzite. Sphalerite tends to form on highly ordered substrates, normally on (100) and (110) faces of single crystals under epitaxial conditions. The argument used to explain the preferred orientation of nuclei, discussed in Section 1.34, may be extended to allow for crystallographic phases of the nuclei, i.e. the surface energy of the substrate/nuclei interface varies for different relative orientations of the nuclei and for different crystallographic phases. A greater preference is shown for the orientation and phase of the nuclei that have a low energy interface with the substrate.

3.33 Reactive substrate

The condensation of CdS on to relatively inert substrates has already been discussed, but a further complication occurs if the substrate is particularly reactive with a component of the vapour. Some metals, e.g. silver, and particularly copper, have a strong affinity for sulphur and there will exist

competition on the surface of these reactive substrates between the cadmium and the reactive metal to form their sulphides.

The metal substrate may react with the sulphur adatoms to the exclusion of the cadmium and form a layer of the sulphide on the substrate, e.g. a copper substrate has been observed to react with the CdS vapour to form distinctive black copper sulphide several microns thick.

The reaction between the sulphur vapour and a copper substrate has been investigated[26] and the formation of copper sulphide from a CdS vapour has been offered as an explanation for some anomalous electrical characteristics.[27,28] Gold and Aluminium* substrates appear little affected by sulphidation reaction with the vapour.

3.40 EFFECT OF FILM THICKNESS

Non-epitaxial films of CdS have randomly orientated nuclei on the substrate surface. As growth continues there is preferential growth of the crystallites orientated with the fastest growing crystal face towards the direction of the impinging vapour.[29,30] In crystallites of hexagonal or wurzite structure the fastest rate of growth is along the c-axis - thus those crystallites whose c-axes are aligned toward the incident vapour grow fastest.[24] Similarly, CdS crystallites of sphalerite structure may grow along the (100) or (111) axes.[24] An evolutionary procedure continues with increasing thickness of the film, the preferred orientated crystals growing faster than those with lesser preferred orientations. The preferred

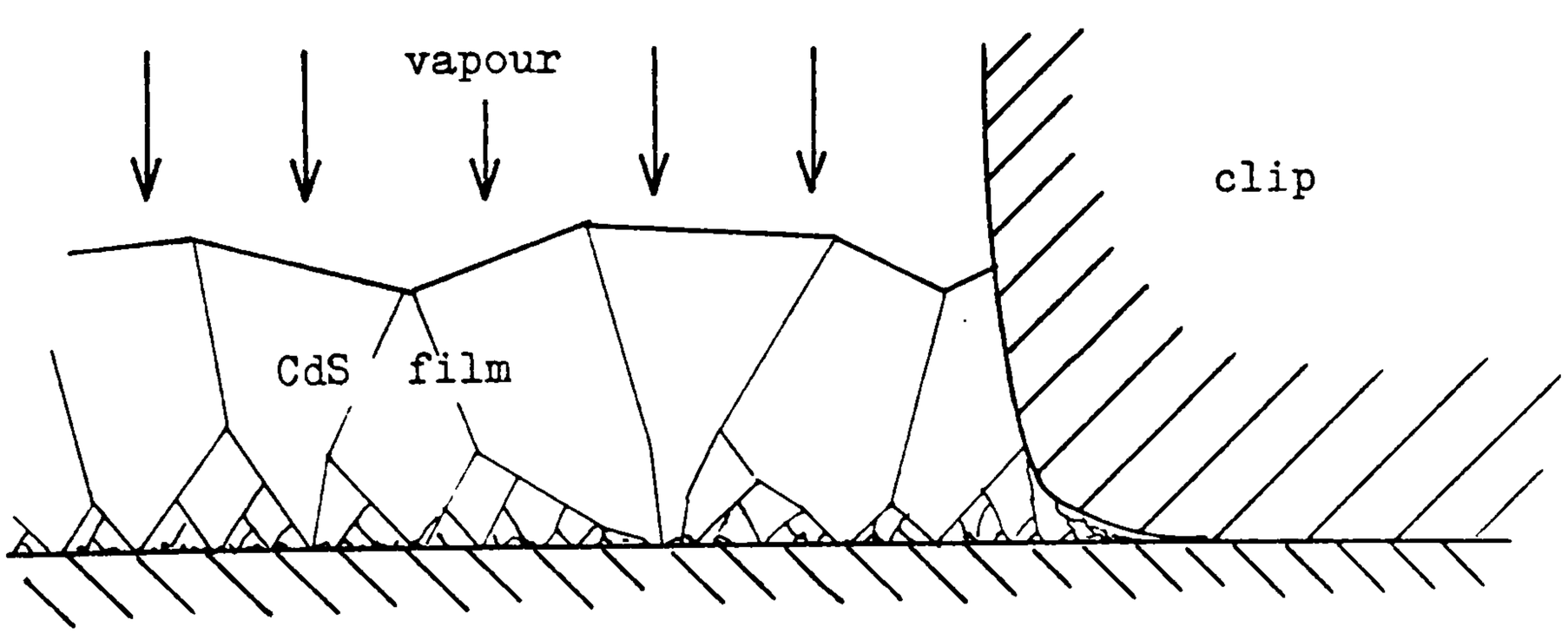
* Aluminium after exposure to the air has a protective oxide layer.

crystallites become elongated in the direction of the incident vapour, i.e. growth is columnar.

The size of the preferred orientation crystals on the surface of the film increases with increasing thickness, as these crystallites expand to the exclusion of the slower-growing crystallites. The alignment of the preferred fast-growing crystallites thus improves considerably from being completely random at nucleation to having close alignment of all crystallites appearing on the surface of thicker films.

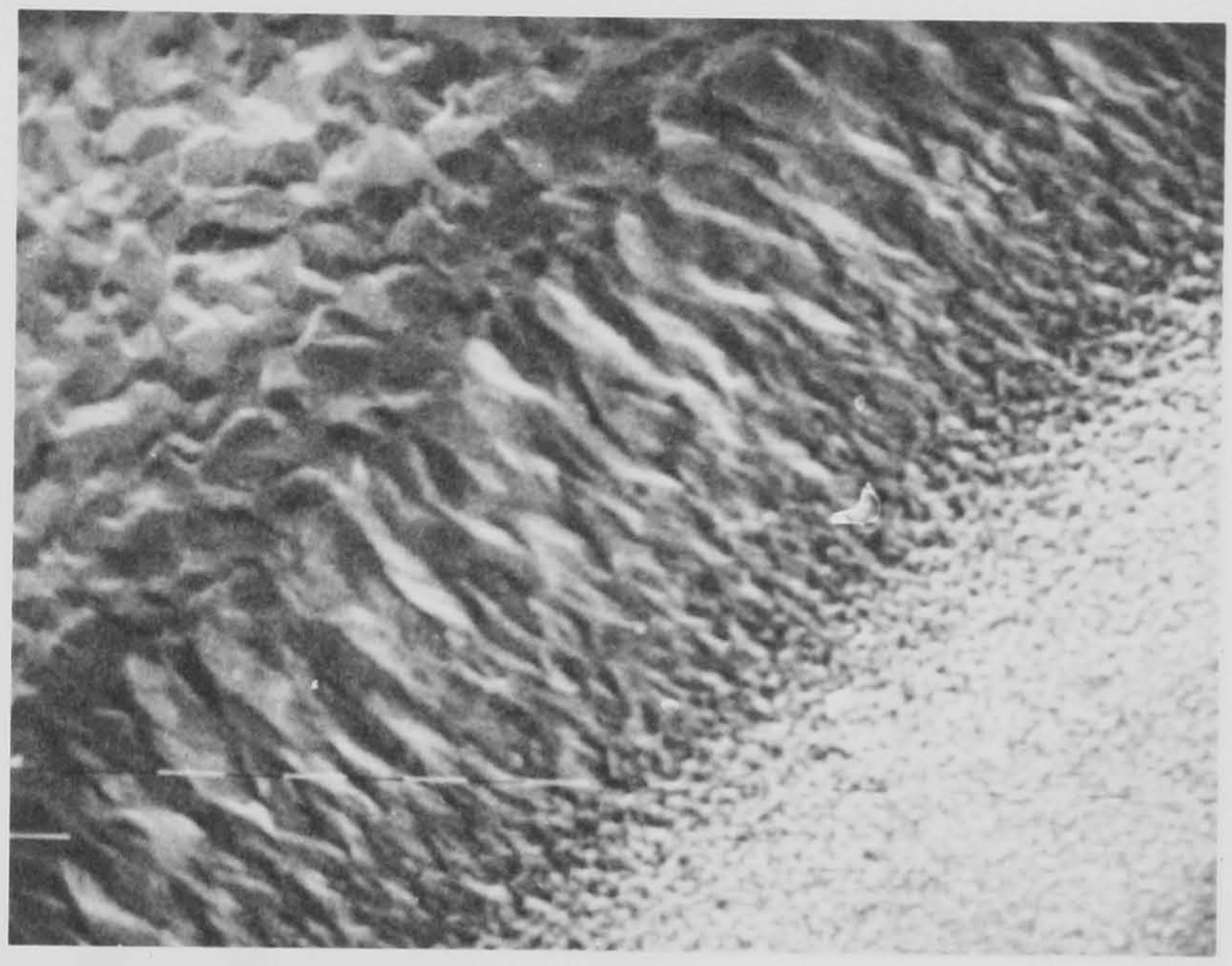
The final crystallite size at the surface is determined by nuclei size at saturation[25] and condensation rate. The degree of preferential orientation of the film occurs earlier in films grown slowly than on those grown quickly.[5]

Figure 16a shows the structure at the edge of a 6μm CdS film grown on Germanium at 200°C. The edge is formed by the shadowing effect of a clip securing the substrate to the substrate holder. The clip is in close contact with the substrate and only a small amount of vapour encroaches under it at the beginning of the condensation. At the later stages film growth prevents further condensation under the clip and the film continues to grow up the edge of the clip - see diagram below.



FIGURES 16 a & b

Scanning Electron Microscope photographs of a CdS film, 6 μm thick, grown at 2400 Å/min. on Germanium (100) at 200 °C



a) Edge shadow of film

b) Fractured edge of film

After removal of the clip, the structure of the film grown from the perpendicularly impinging vapour can be seen. The crystallites are seen to be columnar and to increase in size from small nuclei on the substrate to $\approx 1\mu m$ at the surface by evolutionary selection.

Figure 16b also shows the cross-sectional structure of the same CdS film as is shown in Figure 16a, except that the edge has been formed by breaking the substrate and the film. In this case the structure is not so easily recognisable because of the damage caused by the fracture.

Few, if any, studies have been made of the variation of the crystal structure of epitaxial CdS films with increasing thickness. Some work has been done however on the condensation of gold films on air contaminated NaCl.[13] This work has shown that very thin (60Å) films have several orientations and phases while thicker (600Å) films are perfectly epitaxial with only one phase and orientation.

Figures 15b and 15d show the diffraction pattern for CdS films 600Å and less than 100Å thick grown on NaCl, which has also been air contaminated, at a substrate temperature of 200°C. The thinner film, Figure 15d, shows partially epitaxial film of CdS which has sphalerite and doubly positioned wurzite phases. As described before, Figure 15b is epitaxial and almost single crystal. The improvement of film epitaxy and the dominance of one particular phase is in agreement with the work of Matthews,[13] but qualification is necessary for both Matthews and this present work. In both cases the thin and thick films were grown at different condensation rates - slow and fast.

The effect of growing the film slowly has been shown to increase the epitaxy of the film.[16] As it is observed that the epitaxy of the slowly grown film is less than of the quickly grown film, it must be concluded that the increase in epitaxy is caused by the increased film thickness.

3.50 DEFECTS

In general, the majority of defects are formed during and after the coalescence of the nuclei.[11] The density of the defects increases with increasing condensation rate but decreases with increasing substrate temperature and increasing thickness after coalescence. Three dimensional defects such as grain boundaries and crystallites of a second phase, are also present except in single crystal films, and even single crystal films may have several orientations or phases present in the first few layers of growth before the single preferred orientation completely dominates.[13]

Stacking faults and dislocations which appear in epitaxial[16] and non-epitaxial films can have a variety of causes, which include stresses formed during coalescence[11] and also stress due to the difference in thermal expansion between film and substrate.[31] Point or chemical defects may arise from the incorporation of impurities or by the selective loss of sulphur from non-stoichiometric CdS films.[8]

CHAPTER 4

4.00 THE ELECTRICAL PROPERTIES OF CdS THIN FILMS

4.10 INTRODUCTION

Thin evaporated semiconductor films exhibit electrical properties vastly different from the bulk material. In thin films, grain boundaries, large densities of defects and surface effects, give rise to a considerable anisotropy in the carrier mobility and free carrier density.

4.20 MEASUREMENT OF FILM ELECTRICAL PROPERTIES

The electrical properties of thin films are anisotropic as a result of the anisotropic growth and structure of the film. As the film increases in thickness crystallites increase in size and become more orientated, which may result in predominance of a particular phase of the material.

The electrical properties of the film "in plane", are considerably different from the properties normal to the plane of the film, i.e. "cross plane". As an illustration of this important characteristic, consider a film which has grain boundary barriers limiting[32] the current flow. "In plane" conduction will result in current flowing predominantly normal to the grain boundaries. Conductivity will be lower for thin films as a greater number of grain boundary barriers are in evidence. "Cross plane" conduction will result in current flowing predominantly parallel to the grain boundaries. "Cross plane" conductivity is thus little affected by the grain boundaries and much greater than the "in plane" conductivity.

The resistivity of the substrate determines the type of electrical measurement which can be made on a film. Generally, high resistivity, glass substrates are used for "in plane" film measurements, and evaporated metal film substrates for "cross plane" measurements. As discussed in Section 3.30, the structure of the film is dependent on the surface structure of the substrate. The structure, and hence the electrical properties of the films for "in plane" and "cross plane" measurements, are likely to be different because of the differences in the substrates.

One group of researchers,[31,33] has used the electron density deduced from "in plane" Hall experiments to calculate "cross plane" mobility from "cross plane" resistivity. To carry out the experiments it was necessary to evaporate the film on to glass for the "in plane", and on to aluminium for the "cross plane" measurements. The validity of their conclusion is questionable: even though the trends may be similar for both types of substrate, it is unlikely that the structure and properties will be quantitively the same for both films. The electrical properties of thin semi-conductor films are very sensitive to both micro and macroscopic differences in the structure of the film, and different substrates of similar type can produce films with large differences in electrical properties.[34]

4.30 CROSS PLANE ELECTRICAL PROPERTIES

Electron density and mobility are the major properties measured in CdS films. The electron density is a scalar quantity and the trends observed by "in plane" measurements

can be related to the "cross plane" direction, but mobility is a vector quantity and must be measured in the "cross plane" direction.

4.31 Effect of film thickness

(i) Electron density

From Hall experiments on CdS[5,33,35,36] it has been shown that the electron density increases with increasing film thickness except when the source temperature is high.[35] (In this case the electron density is relatively constant with respect to film thickness.) This trend appears to depend on the source material and is probably the function of a change in the stoichiometry of the source CdS as a result of sulphur segregation.[35]

(ii) Mobility

Mobility is determined by the scattering mechanisms present. In polycrystalline films, grain boundaries and surface scattering can dominate over the bulk, lattice and impurity scattering mechanisms. In addition stacking fault scattering within crystallites can dominate the cross plane mobility and give rise to cubic phase CdS[31] within a predominantly hexagonal phase film.

In general, the "cross plane" mobility could be expected to be much greater than the "in plane", and be closer to the bulk mobility.[31,37] "Cross plane" mobility has been shown to be limited by the stacking fault mechanism[31] which produces a barrier lower than that of grain boundaries. In Section 3.40 it was observed that the cubic phase of CdS is in evidence only

for very thin films. If this dependence can be assumed to be typical of epitaxial CdS films, then it can be deduced that the stacking faults have greatest density close to the substrate. This would result in lower mobility for thin films and also be consistent with the suggestion that stacking faults are caused by the stresses[31] produced by the difference in thermal expansion between substrate and film. These stresses result in plastic deformation of the first few layers of film as the substrate and film cool to room temperature after condensation.

4.32 Effect of substrate temperature

(i) Electron density

Again from the Hall experiments, it has been shown that as the substrate temperature increases the electron density decreases.[33,36] This is consistent with the decrease of defects as the substrate temperature increases - as described in Section 3.50.

(ii) Mobility

Cross plane measurements[31] have shown the resistivity to reach a maximum at a substrate temperature during condensation at 220°C. The electron density has a slow dependence on substrate temperature,[33] and the deduced mobility thus shows a distinct minimum at approximately 220°C. It has been suggested that this substrate temperature is critical to the production of a maximum stacking fault density during the condensation.[31]

4.33 Effect of condensation rate

(i) Electron density

There is not enough evidence to identify a simple interdependence between electron density and condensation rate. One group of researchers[33,36] reports a strong increase in electron density with increasing condensation rate for films grown at a substrate temperature of 220°C. A second group[5] reports a strong but reverse dependence for films grown at 180°C. It can only be concluded that electron density is very sensitive to the condensation conditions and possibly to the evaporation characteristics of the researcher's equipment.

(ii) Mobility

There does not appear to have been any experimental work on the dependence of the "cross plane" mobility on condensation rate. But from Section 2.23 and the "in plane" dependence on mobility, it would be reasonable to expect a decrease in mobility[33] with increasing condensation rate as the number of defects increases. Only if the background pressure during evaporation is high, i.e. greater than 10^{-6} torr, and the condensation rate is lower than 600Å/min, will the density of defects and mobility increase with increasing condensation rate.[16]

4.40 SUMMARY

In Chapter 3.00 the structure and quality of evaporated CdS films were shown to depend in a complex manner on the evaporation and condensation parameters. In this chapter the electrical properties have been shown to depend on the same parameters in no less complex a manner. It would have been surprising if it had not been so.

CHAPTER 5

5.00 THRESHOLD AND MEMORY DEVICES

5.10 INTRODUCTION

Threshold and memory devices have distinctive and similar switching characteristics, which result in two stable conduction states. The conduction state the device is in at any time is dependent on its thermal and electronic history.

A large selection of devices made from different materials and fabricated by a variety of techniques show these switching characteristics. The characteristics exhibited by any device depend not only on the geometry and the physical and electronic parameters of the device but also on the external circuit.

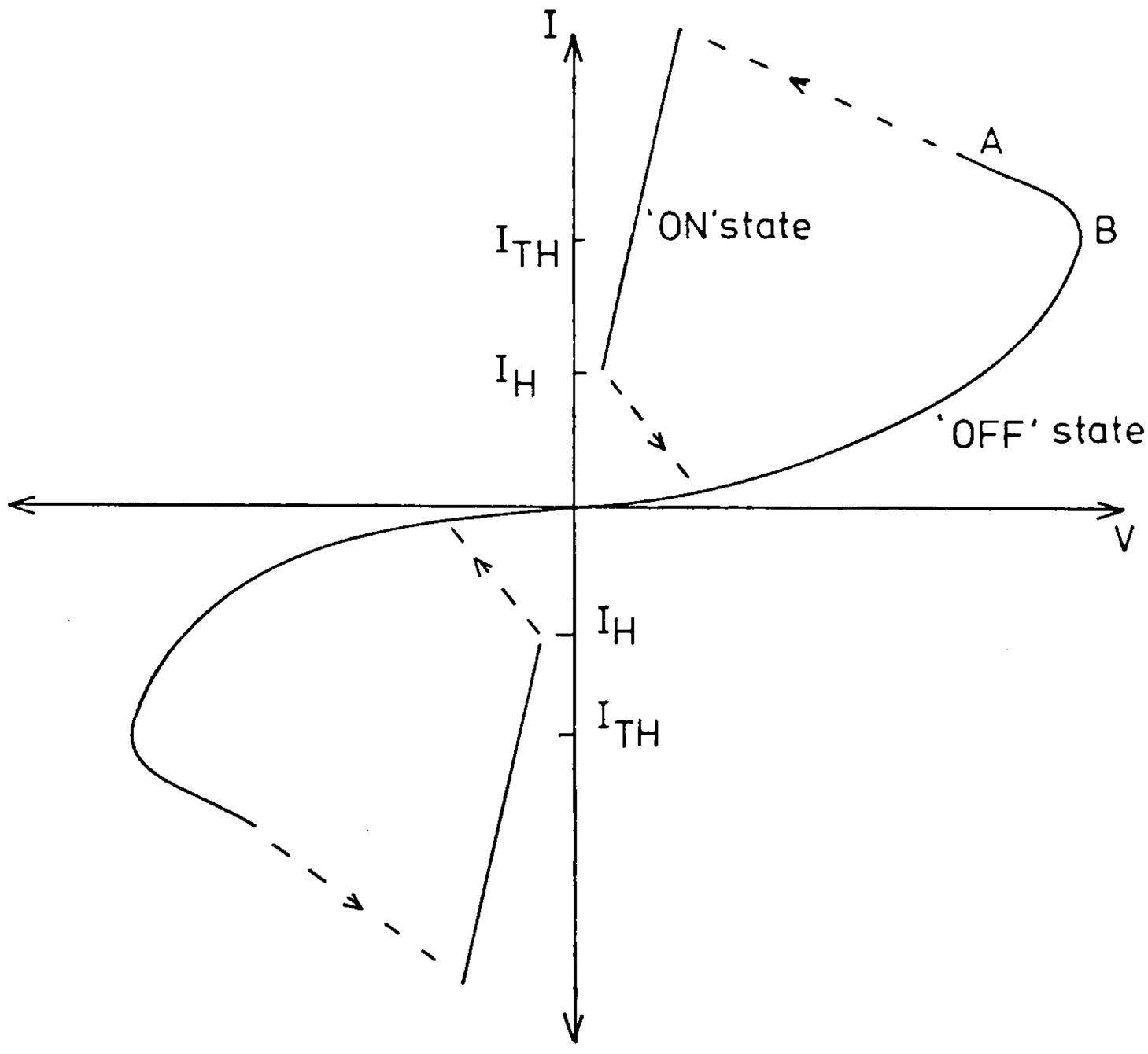
5.20 ELECTRICAL CHARACTERISTICS

Both devices exhibit two conduction states, viz. the "OFF" state and the more conducting "ON" state. Typical threshold and memory characteristics are shown in Figure 17 a) and b) respectively.

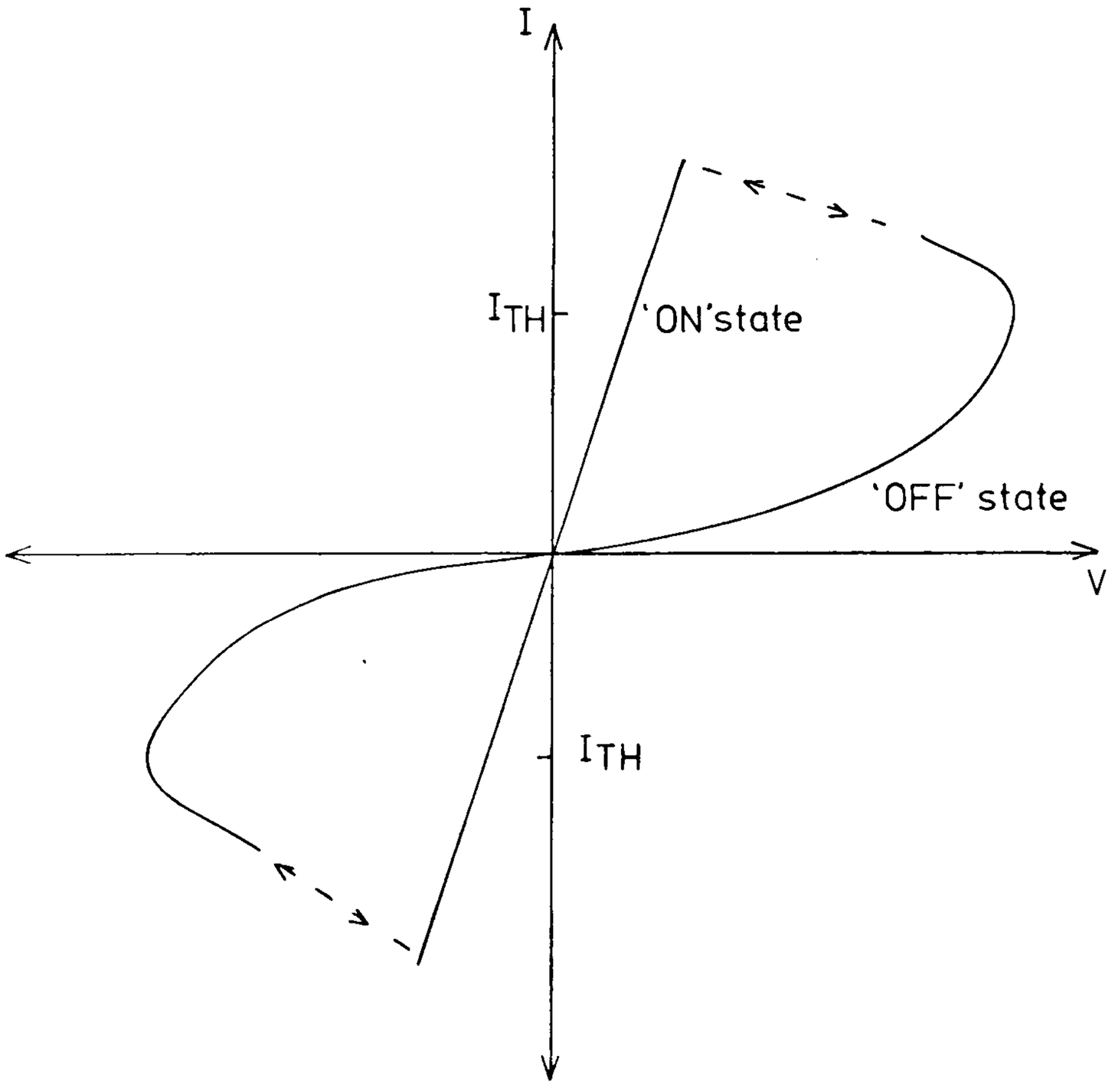
Prior to any switching the device is found to be in the OFF state. Both types of device will switch to the ON state if a current threshold, I_{TH}, is exceeded. The characteristic of the device during switching will follow a "load line" determined by the external circuit. This will be discussed later in Section 6.70 but at this juncture it is to be noted that the series resistance in the external circuit controls the current during switching.

FIGURE 17a & b

a) Threshold device characteristics



b) Memory device characteristics



During switching between states a stable negative differential resistance region can be observed if the series resistance is sufficient.[38,39,80] Negative differential resistance is a differential increase in the current when the voltage is decreased. This region is shown in Figure 17 a) as part of the characteristic between A and B. The negative resistance region is observed in all threshold devices[38,39,40] and can also be observed in some memory devices.[41,42,43]

Threshold devices will not remain in the ON state if the current is reduced below a holding current, I_H. These devices switch back to the OFF state again along a load line determined by the external circuit. The ON state can only be achieved if again the threshold current I_{TH} is exceeded.

Memory devices, on the other hand, succeed in remaining in the ON state even if the applied voltage to the device is reversed or completely removed. Memory devices can be returned to the OFF state by the application of a large, fast current pulse.[40,43]

Anistropic switching can be observed in some threshold[40,44] and memory devices,[42,45] i.e. characteristics which are not identical under both polarities of applied voltage. Some memory devices can only be switched to the ON state by one voltage polarity and returned to the OFF state only by application of the opposite polarity.[42,45] This type of behaviour is normally accounted for by the lack of device symmetry, which is likely to be both physical and electronic.

5.30 SWITCHING DEVICES

Threshold and memory phenomena have been observed in a great variety of devices but originally and predominantly in glass devices.[39,40,44,46,47]

Generally glass devices consist of a thin layer of glass sandwiched between two metal contacts. This type of device can exhibit both memory and threshold characteristics and has been the most thoroughly investigated of all these devices. The glass, which is typically evaporated in a thin layer is amorphous and thus has high resistivity,[48,49] large trap densities and consequently low carrier mobilities.[40,50]

The same characteristics are also exhibited by many different types of device.[41,51] Thin layers of polycrystalline semiconductor films,[51] epitaxial films,[42,51] compound films,[42,45,52,53] elemental films,[54] amorphous oxide films,[55] and many others have been sandwiched between contacts to form switching devices. Non-metal contacts have been used, such as elemental[44] or compound semi-conductors[51,53] which have been evaporated or are single crystals.[51] Fabrication techniques such as the halide close-spaced[42] have been used as well as evaporation.

Typical features of threshold and memory devices are:-

a) Thin layer of the medium, 1 to 100 μm thick, sandwiched between contacts.

b) Low electrical and thermal conductivity medium.

c) High density of imperfections within medium - resulting in low mobilities and low carrier lifetimes.

d) High electrical and thermal conductivity contacts.

These characteristics, identified from a survey of the literature, appear at the present stage of our knowledge to be necessary conditions for switching, but in themselves they may not be sufficient.

5.40 STABLE STATES AND SWITCHING MODELS

As a result of the large variety of these switching devices, a large number of models exist to explain device behaviour. Switching mechanisms are of particular interest because, though the switching characteristics are similar for all devices, the ON and OFF states show considerable diversity.

5.41 Stable states

It is generally agreed that the OFF state is due to uniform conduction over the whole area of the device, and that the ON state results from the formation of the high conduction filament[51,56] of small cross sectional area within the medium between the contacts.

The characteristics exhibited by the devices in the OFF state are clearly dependent on the electrical conduction of the medium and any contact effects. Space-charge limited currents[51,41] have been observed in some device OFF states.

The characteristics exhibited by devices in the ON state are very different from those in the OFF state. For example memory diodes have characteristics in the ON state similar to those of semi-metals or degenerate semi-conductors,[42,48,51] and appear quite ohmic at low currents. Threshold devices in the OFF state tend to have super linear characteristics, i.e. current increasing with voltage at a power greater than one.

The filament formed in the threshold case disappears if the current falls below I_H and conduction over the whole contact area returns.

5.42 Threshold device switching

Most models basically fall into two categories, viz. electro-

thermal and purely electronic. The difficulty with most models is that the physics are inherently complex and quite sweeping assumptions are made before tractable solutions become possible. Arguments rage over which simplifying assumptions are valid and which are not.[46] Most models are not generally valid for all types of switching device but nevertheless the switching characteristics are similar. The following models show the two different approaches.

(i) Electro-thermal models[39]

These models are based on the assumption that the only contribution electronic conduction makes to the switching mechanism is indirectly through Joule self-heating. The temperature in any region of the device depends on the current densities within the device. If the conductivity of the device medium is temperature-dependent, then current densities are dependent on temperature. The interdependence of current density, conductivity and temperature are described by the "heat equation".

$$C \frac{\delta T}{\delta t} = \frac{J^2(T)}{\sigma(T)} - \nabla(K \nabla T)$$

where T is the absolute temperature
J is the current density
σ is the electrical conductivity
t is the time
C is the specific heat per volume
K is the thermal conductivity

This equation is non-linear as well as having three physical dimensions and time dependence. Temperature is a function of position and time.

Many assumptions can be made to "simplify" the equation, e.g. neglecting the time derivative by assuming slow changes in temperature.

The boundary conditions can also be simplified. An assumption often made is that the contacts are infinite heat sinks. Some assumptions are more questionable than others, but what appears certain is that most cannot be valid for all cases of switching that have been observed.

Even after assumptions have been made the equation can only be resolved by numerical computation.[39,46] It is always difficult to discern from such calculations which trends genuinely reflect the physics of the devices and which are a direct consequence of the assumptions themselves.

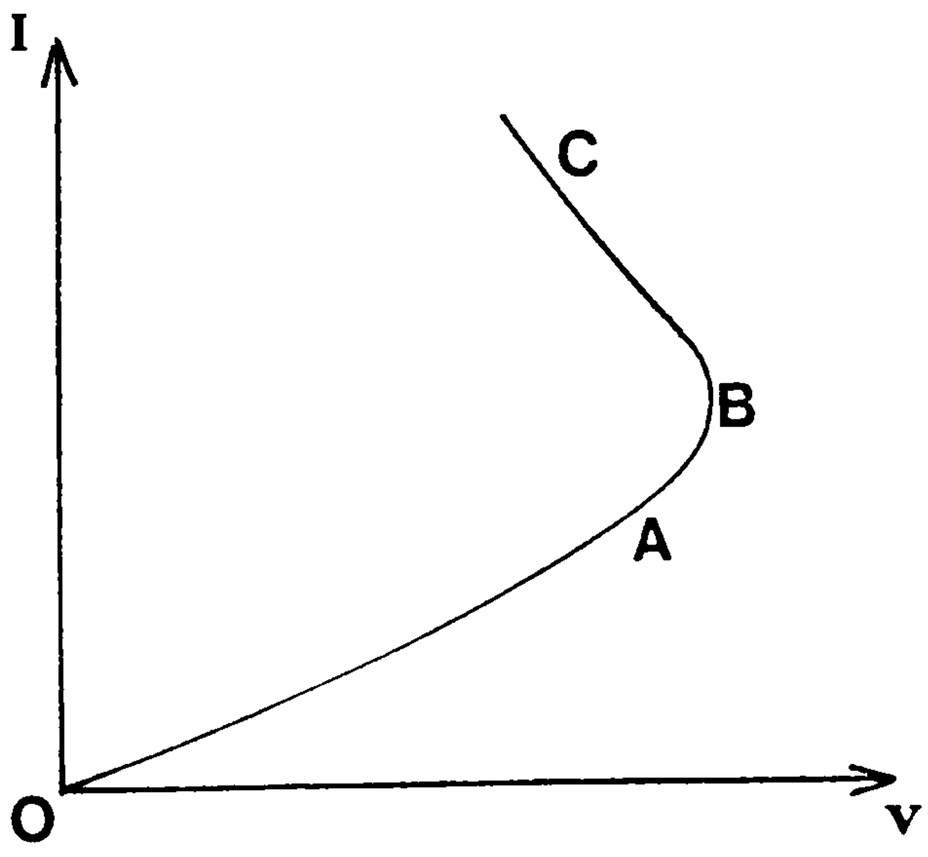
Calculations based on a particular set of assumptions[46] have shown the formation of a temporary high current density filament within the medium if a threshold is exceeded. The current flowing through the device is concentrated in the filament, which has a high conductivity as a result of high temperature. Up to the threshold the current density over the whole device was evenly distributed. Thus a threshold type of characteristic has been derived from numerical computation of a simplified heat equation. But a greater understanding of the switching mechanism may be possible through physical description.

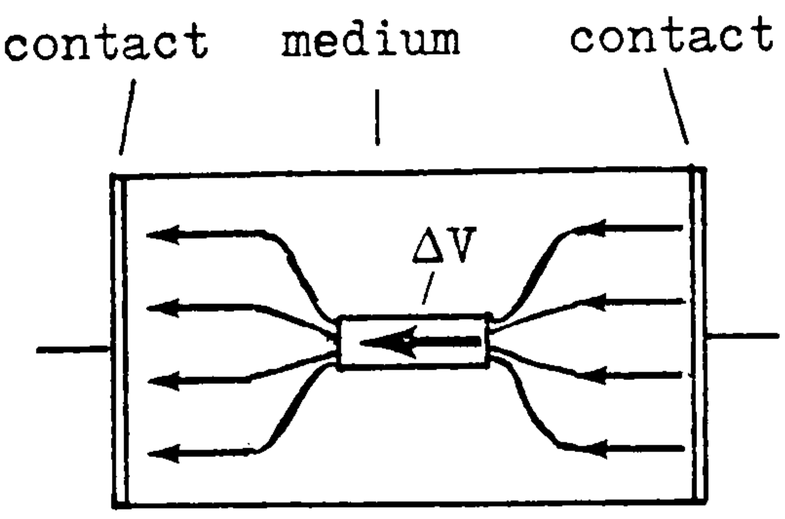
Assume that a small volume, Δv, of the medium has a higher electrical conductivity than the surrounding regions and that conductivity increases rapidly with temperature. A higher current density is attracted to Δv due to its high conductivity. This results in a higher temperature for Δv because of Joule self-heating.

At low levels of current density there is no significant

temperature differential between Δv and the surrounding regions of the medium which remain close to the ambient temperature. The temperature differential does become significant at higher current densities however. The higher temperature of Δv further increases the conductivity of Δv, and this results in higher current densities and an increase in the temperature differential between Δv and its surroundings. This positive feedback results in a concentration of current flow in Δv. Thus the medium is partially short-circuited by Δv.

As Δv is hotter than the rest of the medium a temperature gradient is present. Thus regions just outside Δv are at a higher temperature than the remote medium. This results in an increase in the size of the higher conductivity region to ΔV. Large current densities will exist before and after ΔV along the current path as a result of Joule self-heating by the converging and diverging current as it enters and leaves the high conductivity region. These larger current densities plus the temperature gradient elongate the ΔV towards the contacts.





current flow in device between A and B.

Thus region O to A is the electrical characteristic of the medium at low current levels. Region A to B shows a rapid increase in conductivity of the device due to the formation of the short-circuiting region ΔV. At B the high conductivity filament extends through the device from contact to contact. An increase in current will rapidly increase the conductivity of the filament through increasing the diameter and temperature. The decreasing device voltage resulting from increasing current produces the negative resistance characteristic B to C.

The necessary conditions for such models to apply are :-

a) electrical conductivity that rises rapidly with temperature, and
b) low thermal conductivity.

This electro-thermal switching mechanism is inherently slow - the speed being determined by the rate at which the temperature of the medium can rise. Typically, switching is possible in milliseconds. Some devices however have shorter switching times - of the order of nanoseconds.[49] Faster electronic switching mechanisms have been suggested for such devices.

(ii) a) Electronic models

Several electronic models appear to be based on electronic transport in the relaxation regime.[47,50,57]

The less widely known type of semiconductor is the "relaxation" type. These have dielectric relaxation times longer than the carrier lifetime. This results in significant space charge effects as recombination is the faster process. If, for example, a number of holes are injected into such a semi-conductor, the immediate effect is fast recombination.

Carrier densities adjust quickly through recombination until $np = n_i^2$ and the recombination rate then tends to zero. At a later time dielectric relaxation returns the carrier densities to their equilibrium levels.

In comparison, "lifetime" semi-conductors have a carrier lifetime longer than the dielectric relaxation time. A result of this is that local space charge neutrality is quickly attained in the absence of contact effects. If, for example, a number of holes are injected into such semi-conductors the immediate effect is a flow of electrons to compensate and neutralise the excess charge of the holes. At a later time, recombination returns the carrier densities to their equilibrium levels.

The most general model[50] that shows a threshold type of switching characteristic requires minority carrier injection into a "relaxation" semi-conductor. At low injection no significant space charge effects are observed but higher injection can result in all majority carriers recombining.

Near the minority carrier injecting contact, a space charge region forms and recombination within this region is near to zero. The current is carried by minority carriers in this region, which has high conductivity, and it increases in size with increasing current. At the end of the space charge region there exists a "recombination front" of high recombination rate. At the other side of this "front" majority carrier current is predominant. In the space charge region the fermi level is pinned by recombination rather than by space charge effects as in the "lifetime" case.

The device when in the ON state, consists of only a large minority carrier space charge region extending almost the full length of the device, and a short recombination front. Majority carriers injected immediately recombine so that the low conductivity majority carrier current region disappears in the ON state. The major drop in voltage appears over the recombination front and results in high electric fields.

Even though this model is based on highly compensated crystalline semi-conductor band structures, it is still considered valid for glass devices. Both types of material are highly resistive which leads to long dielectric relaxation times, and both have high densities of imperfections which lead to short lifetimes.

Other models require injection of minority carriers to produce a region of high conductivity in an otherwise low conductivity material, i.e. "double injection".[58,59] Double injection models do not necessarily require a medium of the "relaxation" type.

The "double injection" model for a n-type semi-conductor requires a high density of acceptor type recombination centres located just below the fermi level. These recombination centres have a greater capture cross section for holes than for electrons, and holes injected from the anode are quickly captured. Consequently the centres become empty of electrons, and the lifetime of injected holes increases as the capture rate diminishes. The electron density and recombination rate are not reduced to zero as in the "relaxation" case. As injection of holes increases, the region of long hole lifetime extends. Negative

resistance will be observed when holes can transit the whole medium and the greater amount of the current is carried by holes. The medium, in a sense, shows a p-type semi-conductor behaviour.

Similar behaviour is predicted for a fully compensated semi-conductor,[47] i.e. a semi-conductor with a large equal density of donor and acceptor centres, which leads to an equal density of holes and electrons in equilibrium. Injections of both holes and electrons give similar results to the injection of minority carriers of the model above - both holes and electrons acting like minority carriers. Negative resistance results when there is overlapping of the two high conductivity regions that extend from both contacts.

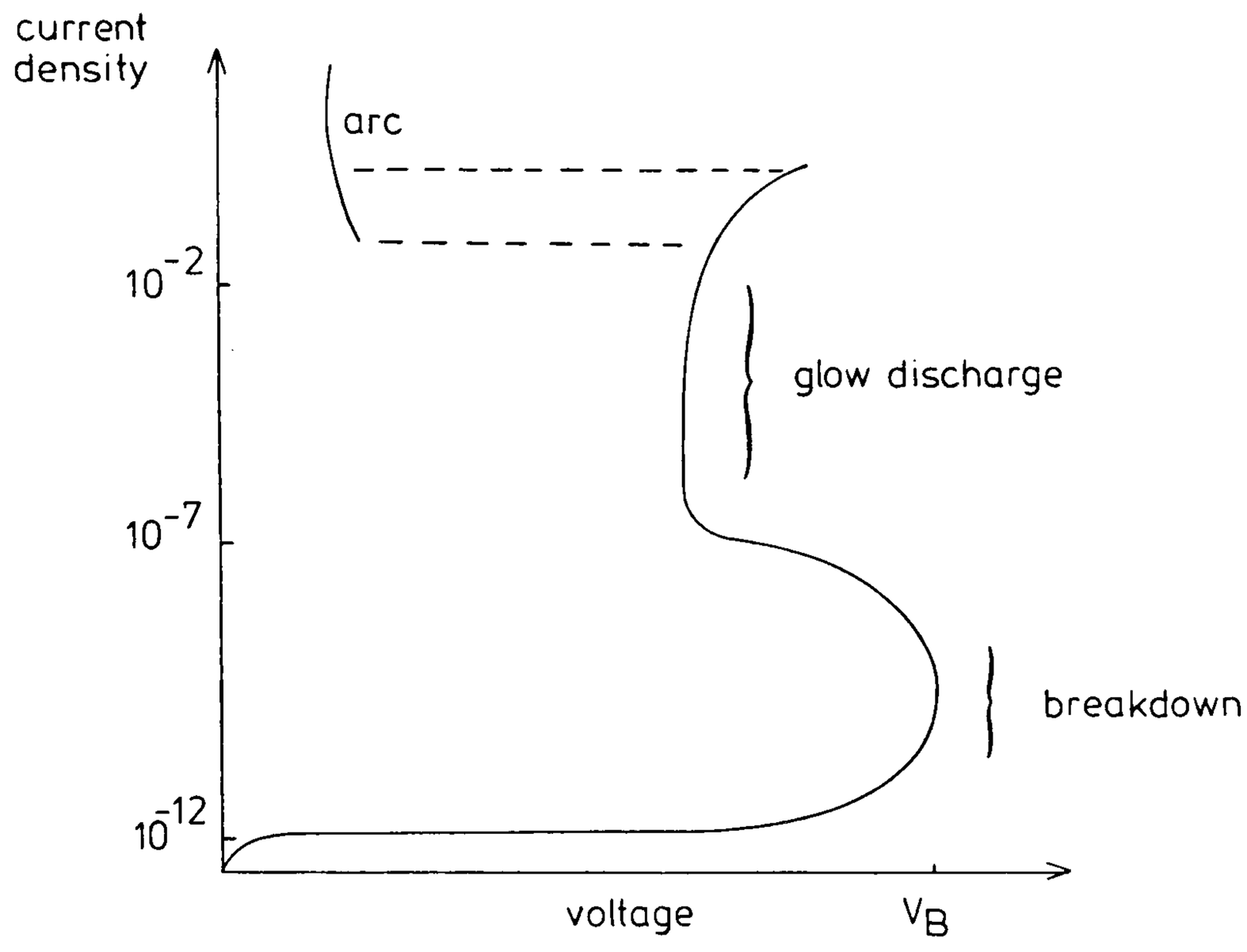
These electronic models do not exclude the possibility of filament formation and the observation of temperature effects. They show rather that a threshold characteristic can result from purely electronic processes. Filament growth may enhance the threshold characteristic, but it is a result of the electronic and not the electro-thermal switching mechanism.

(ii) b) Gas discharge analogy

Striking similarities exist between threshold switching and gas discharge characteristics. Figure 18 shows a typical gas discharge characteristic which has all the essential ingredients of threshold characteristics. Gas discharge characteristics[60] are due to the transport of electrons and positively charged gas ions in an electric field between two metal electrodes. At low voltages conduction of the naturally occurring gas ions and electrons results in very low currents. Higher currents

FIGURE 18

Gas Discharge Characteristic



are produced by higher electric fields which increase the kinetic energy of the electrons to such a level that they ionise gas atoms upon collision and thus increase the number of charge carriers. The rapid increase of current with voltage is a result of an avalanche effect, i.e. multiple collisions which produce a rapid increase in the number of charge carriers.

At higher currents self-sustaining discharge or "breakdown" occurs as a result of the positive ions gaining sufficient energy from the electric field to produce secondary electrons from the cathode on impact. During breakdown the current can increase by several orders of magnitude with no increase of applied voltage.

At still higher currents a "glow" discharge zone can be achieved at a lower voltage than is required for "breakdown". In this zone of the characteristic the current density on the surface of the cathode remains constant and variation of the current results in the utilisation of a greater or smaller area of the cathode.

Although the gas discharge effect gives rise to an ON and OFF state and a filament type of current constriction in the ON state, some of the gas discharge processes do not provide a direct analogy for semi-conductor and glass devices.

Avalanche is a common breakdown effect[61] in semi-conductors as well as in gas discharge experiments, but secondary emission is only relevant to gas discharge. Recombination of positive and negative charge carriers is negligible in gas discharge but can be an important process in the semi-conductor.

The electric field and space charge distribution in the ON state in the two types of medium also have considerable similarities.

5.43 Memory device switching

It seems to be generally agreed that the switching characteristics of the memory devices are directly related to those of threshold devices, and that at a critical current the temporary filament becomes permanent through a change of physical structure.[51,56] The threshold switching mechanism, which may be described by one or more of the models discussed in 5.42, initiates the change. The point at which the transition from a temporary to a permanent filament occurs depends on many factors, including the geometry of the device and the nature of the medium. In fact some devices show only the threshold characteristic and fail to form a permanent filament. Others form a permanent filament almost as soon as the device starts switching.

(i) Thermal model[48]

It has been found that considerable changes in conductivity can be caused in a chalcogenide glass by thermal cycling. This effect was shown to be a result of recrystallisation induced by changing the glass temperature. The experiment succeeded in isolating the temperature effects from other, often misleading, device effects such as contamination from contacts and ambient atmosphere.

Highly resistive glass was heated to just below its melting point and then gradually cooled. This process converted the glass to high conductivity. Mobilities of the magnitude of

$85cm^2/Vs$ at room temperature were observed and the glass exhibited characteristics similar to semi-metals or extrinsic semi-conductors.

To return the glass to its highly resistive state it was heated beyond its melting point and then quickly quenched. This cycle can be repeated many times without signs of degradation.

The change in conductivity is due to spinodal decomposition of the glass, which at certain temperatures causes phase separation. The phase separation results in the formation of regions of semi-metal compounds from the glass.[56] The regions of semi-metal compound disappear when the glass is melted and rapidly cooled.

This model can apply to switching devices when changes of temperature are caused by Joule self-heating. The conductivity is determined by the rate of temperature increase and decrease. If the current flowing through the device increases slowly the temperature of the whole device and its surroundings increases. When the current is removed, even if this is done quickly, the device will nevertheless cool slowly as a large heat capacity exists in the low thermal conductivity glass. If the current is in the form of a fast pulse then only in the immediate region of high current flow - probably within a filament - will the temperature rise. Cooling will be rapid after the current disappears as the surroundings are still close to ambient temperature.

In general, for glass devices phase separation at specific temperatures will result in conductivity changes. But for two component compounds such as ZnSe, CdS, etc. recrystallisation

rather than phase separation may be the cause of the changes.

For some applications this model has the major limitation that the switching occurs at a much slower rate than has been observed in some devices. The switching and formation of a permanent filament is inherently slow regardless of whether the threshold switching mechanism is electro-thermal or electronic - typically time delays of several microseconds are required.[40,51] A permanent filament can be formed in a nanosecond with some devices,[40,56] so a model for faster filament formation is necessary.

(ii) Thermo model with electromigration[40]

This model is essentially the same as discussed in (i) above except that the phase separation or recrystallisation is the result of electrical breakdown, which for most materials occurs if the electric field within the device exceeds 10^6V/m. The electrical breakdown leads to a sudden rise in temperature and ionisation of atoms in the region of the breakdown. The migration of these charged particles under the influence of the electric field results in an increased rate of decomposition and filament formation along the path of the breakdown. The charged particles need only drift a short distance, e.g. 20Å, under the effect of the device's electric field to result in considerable changes in structure within the filament.

The filament when formed can be ruptured by application of a fast current pulse. As in the purely thermal model the highly conductive filament heats up quickly to above melting point and is cooled rapidly by its surroundings after the pulse has passed. (The fast increase in temperature is the same "thermal runaway"

observed in most devices when the heating caused by the current flow is greater than the cooling effect of the surroundings)

(iii) Electrical initiation of Mott transition model[62]

It has been observed that a small change in the density of excess metal atoms in semi-conductors can lead to a considerable change in the resistivity and type of conduction. A good example of this Mott transition is the crystalline semi-conductor antimony triselenide (Sb_2Se_3) with excess antimony (Sb). At concentrations of excess Sb lower than the critical (0.5% excess weight) the resistivity is close to the stoichiometric, and the conduction is typical of high resistivity semi-conductors. If Sb_2Se_3 has a concentration of excess Sb greater than the critical level, then a metal-like conduction appears and the resistivity is six orders of magnitude lower than stoichiometric. The sudden transition from semi-conductor to metal-like conduction is due to the overlapping of the donor atom, Sb, wave functions when their density is above the critical level. The conduction observed, whether semi-conductor or metal-like is inherent in the as-grown Sb_2Se_3 and is not directly dependent on the applied voltage.

Crystalline stibnite, Sb_2S_3, exhibits a Mott transition that is only observed after application of a critical electric field. The as-grown stibnite, regardless of the concentration of excess Sb, does not show a Mott transition, but if sufficient excess Sb is present and sufficient electric field is applied, switching to a lower resistivity metal-like conduction state is observed. The switch to the metal-like state is accomplished in a few tens of nanoseconds and the new region of low resistivity follows the line of the electric field breakdown, forming

a filament. The breakdown electric field can be as low as 10^5V/m for stibnite with a large density of excess Sb and this is compared with 2.5 x 10^8V/m for stoichiometric stibnite. The stibnite can be returned to its high resistance, semi-conductor-like state, by heating externally or internally through Joule self-heating by the application of a fast current pulse.

Two potential sites for the Sb donor have been postulated to explain this phenomenon. When the donor is in the lower potential site the semi-conductor type of conduction and high resistivity are observed. Under the influence of the applied electric field the donor can move into a higher potential site which is physically close to the lower. In the environment of the new site the wave function of the donor has physically expanded allowing metal-like conduction through overlapping. A potential barrier prevents the donor from slipping back to the lower potential site.

5.44 Filament formation characteristics[56]

The formation of a highly conducting filament in a highly resistive medium will result in the characteristic ON state of threshold and memory devices. The mechanisms by which filaments, temporary and permanent, may be formed have been discussed in Sections 5.42 and 5.43. This section describes the observations of filament formation which appear to apply particularly to glass devices. Little work has been done in this part of the field for other types of device.

In threshold devices the temporary filament is formed when the threshold current I_{TH} is exceeded. The highly conductive filament disappears if the current is reduced below the holding

current I_H, as no permanent filament has formed, and the device returns to its OFF state.

The application of a current pulse to a potential memory device can result in one of several different states. If a current pulse of magnitude greater than I_{TH} is applied with a very short duration - less than 10 μs for some glass devices - then a temporary filament is formed. If the time period allowed is too short or the magnitude of the pulse is insufficient no permanent filament growth begins. Increasing the duration of a pulse of sufficient magnitude to above a critical time allows permanent filament growth to begin, normally from the anode. If the duration of the pulse is sufficient the permanent filament will continue to grow until it reaches the cathode. The device will then be in the ON state with a permanent filament.

If the pulse is of sufficient magnitude and duration to start growth but of insufficient duration to complete growth, a partially completed filament is formed. When the current is removed before the permanent filament growth is completed, the temporary filament between the tip of the permanent filament and the cathode disappears. The device returns to an OFF state with a decreased resistance due to the short-circuiting effect of the partially completed permanent filament.

To return the device to the ON state the current threshold I_{TH} must be exceeded. The temporary filament then returns in the gap between the partially completed filament and the cathode. In this case, the voltage associated with I_{TH} is lower as a result of the short-circuiting effect of the partially completed filament, which has the same effect as reducing the thickness

of the medium. The permanent filament continues to grow after a short delay, and when the filament reaches the cathode a small increase in conductivity is observed. This indicates that the permanent filament has lower resistance than the temporary.

The diameter[51] and the rate of growth[40,56] of the permanent filament both increase as current exceeds that necessary to start permanent filament growth.

It has been assumed for convenience that the filament grows from the anode, and this has been found to be the general case - though all the experiments showing growth from the anode have been on p-type glasses. One can only speculate on the direction of growth in n-type materials.

An interesting observation of the polarity dependence of filament growth has been made when the polarity has been reversed when the filament is partially grown. This results in retraction of the partially grown filament towards the new cathode and then growth of a new filament from the new anode.

5.50 CdS THRESHOLD AND MEMORY DEVICES

Both threshold and memory devices have been fabricated from thin evaporated films of CdS. These devices appear to conform to the necessary conditions for switching devices discussed in Section 5.30.

5.51 CdS switching medium

The thermal conduction coefficient of CdS[63] is low and comparable with that of some glasses. Switching devices have evaporated CdS films of high resistivity,[28] i.e. low electrical

conductivity, and have a high density of imperfections[37,41,64] in the form of traps and grain boundaries. The high density of imperfections leads to low carrier mobility[64] and short carrier lifetimes. Thus a thin layer of evaporated CdS sandwiched between contacts possessing high thermal and electrical conductivity fulfils the necessary criteria for switching devices. Further, the evaporated CdS, due to its high density of imperfections and high resistivity, could easily form a relaxation semi-conductor.

CdS has a large energy band gap (2.4eV) and evaporated CdS is n-type. Typically the electron density in these films is $10^{14}cm^{-3}$ in equilibrium. This implies that the hole density is very low, i.e. of the order of $10^{-16}cm^{-3}$ in equilibrium. Consequently hole conduction is normally ignored in CdS.[64,65] The evaporated film is non-uniform physically and this results in a non-uniform distribution of carriers in equilibrium. Furthermore, in evaporated films the trap density tends to exceed the free electron density by several orders of magnitude.[37,36] Consistent with the models, CdS has been observed to support temporary, high current density filaments.[67]

5.52 CdS switching devices

The simplest of these devices consists of the evaporated CdS sandwiched between two evaporated metal contacts.[41,64] It appears that either ohmic contacts such as Indium and Aluminium[41] or rectifying contacts such as Gold[64] can be used. (This is consistent with the switching observed in several oxide films,[64] which is also independent of the electrode material.) The switching is deduced to be a purely bulk effect of the CdS even though the conduction in the OFF state may be determined to a

degree by the contact effects. The effectiveness of a contact barrier will be small due to the large density of trap states situated in the energy band gap reducing the barrier thickness. As a result, tunnelling currents will predominate.[43,66,68]

Avalanche and double injection[64] as well as recrystallisation[27] have been suggested as the mechanisms responsible for switching.

The OFF state is super linear[41,64] and the ON state has been observed either as super linear[41] or ohmic[64] - the unusual super linear "ON state" could be due to an uncompleted filament and could in fact be an intermediate state between OFF and ON.

Filament formation has been observed to damage thin metal electrodes.[52] Thicker metal electrodes were not damaged and such devices had longer switching lifetimes before degradation than devices with thin electrodes. This could be simply explained by the thicker electrode being a more effective heat sink and thus ensuring a lower temperature in the vicinity of the filament-contact interface. High temperatures in the vicinity of this interface would result in contamination of the medium by diffusion of the electrode material.

The asymmetric nature of these devices is reflected in the polarised characteristics observed. Even in superficially symmetric devices, e.g. Au-CdS-Au,[64] an almost rectifying characteristic can be observed in the OFF state. This is not only due to the preferential growth of the CdS film but also chemical reactions between the CdS vapour and the metal contact substrate during the evaporation. (This was discussed more fully in Section 3.33) "Foreign" compounds such as Cu_xS_y [52] can form and may dominate the switching performance of the device.

The literature[64] states that memory switching occurs within a microsecond but it is not clear whether this time relates to temporary or permanent switching. Permanent switching usually takes longer than temporary, and this is normally attributed to permanent switching being a thermal process whereas temporary is electronic.[40]

5.53 Summary

CdS as a threshold switching medium, appears to accommodate thermal switching mechanisms rather than the established electronic mechanisms such as relaxation and double injection models which require minority carrier injections. But switching at a rate too fast for thermal switching has been observed in CdS, indicating that electronic switching processes must also occur. In Chapter 7 an electronic model which allows for the creation of hole-electron pairs through avalanche will be proposed.

CHAPTER 6

6.00 DEVICE FABRICATION AND MEASUREMENT

6.10 INTRODUCTION

In this chapter the details of the device design, fabrication, mounting and measurement are described.

6.20 DEVICE DESIGN

The majority of experimental work was carried out on p-type Germanium - n-type Cadmium Sulphide - Copper devices, as these devices were known to exhibit the switching characteristics under investigation.[69,70]

The design of the device was modified by changing the substrate doping, film condensation parameters, and the type and area of the metal contact to the CdS film. Each parameter was modified in turn to allow the effect on the electrical characteristics to be observed and information obtained on the electronic structure and operation of the device.

6.21 Ohmic contact to the Germanium

An ohmic contact was made to the p-type Germanium substrate by evaporating a layer of Copper on to a large area of its surface. Copper is an acceptor impurity in Germanium[71] and, with heating, the Copper will diffuse into the Germanium and form a p^+ region, giving an ohmic contact. Tests on a Copper-Germanium-Copper device confirmed an ohmic contact even when the device was only subjected to radiant heating during the Copper evaporation.

6.22 Metal contacts to CdS

The surface of Cadmium Sulphide, unlike most common II - VI compounds, is not dominated by surface or interface states,[72,73,74] and this means that the electrical barrier between the CdS and a metal contact is dependent on the type of metal. The height of the barrier[75] from a metal contact to the CdS film, which is normally n-type,[5] can be large with Platinum or very small with Indium. The barrier height is less if the surface of the CdS film is contaminated[75,76] prior to the condensation of the metal film. Exposing the CdS to oxygen,[76] for example, can modify extensively the rectifying barriers of Gold and Copper[76] and can produce an insulating Aluminium Oxide layer between the CdS and an Aluminium contact,[77] which is normally ohmic.[37,73,75]

The metals used in this study for contacts to CdS were Copper, Aluminium and Chromium. Copper produces a rectifying barrier of between 0.4 and 0.7eV.[73,76] Chromium was chosen as an ohmic contact in preference to Indium[76,78] and Gallium[78] as these materials have low melting points which could adversely affect the device's performance during temperature experiments.

6.23 Heterojunction between the Germanium and CdS

Unlike the contacts to Germanium and CdS discussed in Section 6.21 and 6.22, the junction between Germanium and CdS cannot be so easily defined.

Prior to the evaporation of the CdS film the Germanium substrate was exposed to the atmosphere as well as to the chemicals used for polishing and cleaning. A layer of impurities existed therefore on the substrate's surface during CdS condensation, and as a result the interface or transition region between the

substrate and film was a complex mixture of compounds.[76,79] The impurities of the interface region produce localised energy states,[80] additional to the surface energy states[74,81] which are due to the termination of the Germanium and CdS lattices. These interface energy states,[81,82,83,84] depending on their density, energy level and type - acceptor or donor - can determine the energy band positions within the Germanium and CdS, and thus the electrical characteristics of the junction. If, for example, the interface energy states are so numerous in the vicinity of the fermi level then the interface region will have "metal-like" characteristics.[81,85]

6.30 EVAPORATION OF METALS

All the metals used for electrical contact were evaporated in an Edwards coating unit incorporating an oil diffusion pump. Copper and Chromium were evaporated from cermite crucibles by a focussed electron beam, and Aluminium from a tungsten spiral filament heated by a current passing through it. Aluminium could not be evaporated from cermite crucibles because in its molten state it quickly reacts[7] and destroys the crucible - and contaminated Aluminium is then evaporated.

Background pressure increases during the evaporation of Copper, but the rate of evaporation was limited in this case so that the pressure did not rise above 5×10^{-5}torr. Aluminium and Chromium have the opposite effect on background pressure and both of these metals can be evaporated with pressures of less than 2×10^{-5}torr.

99.999% pure Aluminium and Copper wire and Chromium chips were used as the source materials.

The chamber apparatus is shown in Figure 19. Above the electron beam gun is a movable shutter shielding the samples mounted above from the initial outgassing of the gun and crucible. Only when the underside of the shutter begins to be coated with the evaporating metal is the shutter swung aside to expose the sample to the stream of metal vapour. The rate of evaporation is controlled by the flow of current through the filament and is measured by a Quartz crystal thickness monitor. The crystal is situated above the sample and directly in the stream of vapour. Between 0.5 and 1 μm of metal was condensed on to the samples at a rate of approximately 10,000 Å/min.

Aluminium was evaporated from the tungsten filament mounted on the upper side of the shutter. The shutter allows the Aluminium and the filament to be outgassed "out of sight" of the sample. The shutter was only swung into position directly below the sample when a steady stream of vapour was observed to be coating inside the bell jar. The Quartz thickness monitor was calibrated for both the electron gun and tungsten filament source positions, and also for all three metal densities.

The sample temperature rose to approximately 80^{o}C as measured by a Chromel-Alumel thermocouple during the evaporation of Copper and Chromium as the result of the high crucible temperatures required. The Aluminium evaporation did not affect the sample temperature significantly as a much lower temperature was required to evaporate this metal.

During the evaporation of the metal contacts the samples were held by glass slides in a slide holder as shown in Figure 20. For the evaporation of the ohmic Copper contact a large portion

FIGURE 19

Coating Unit Chamber Layout

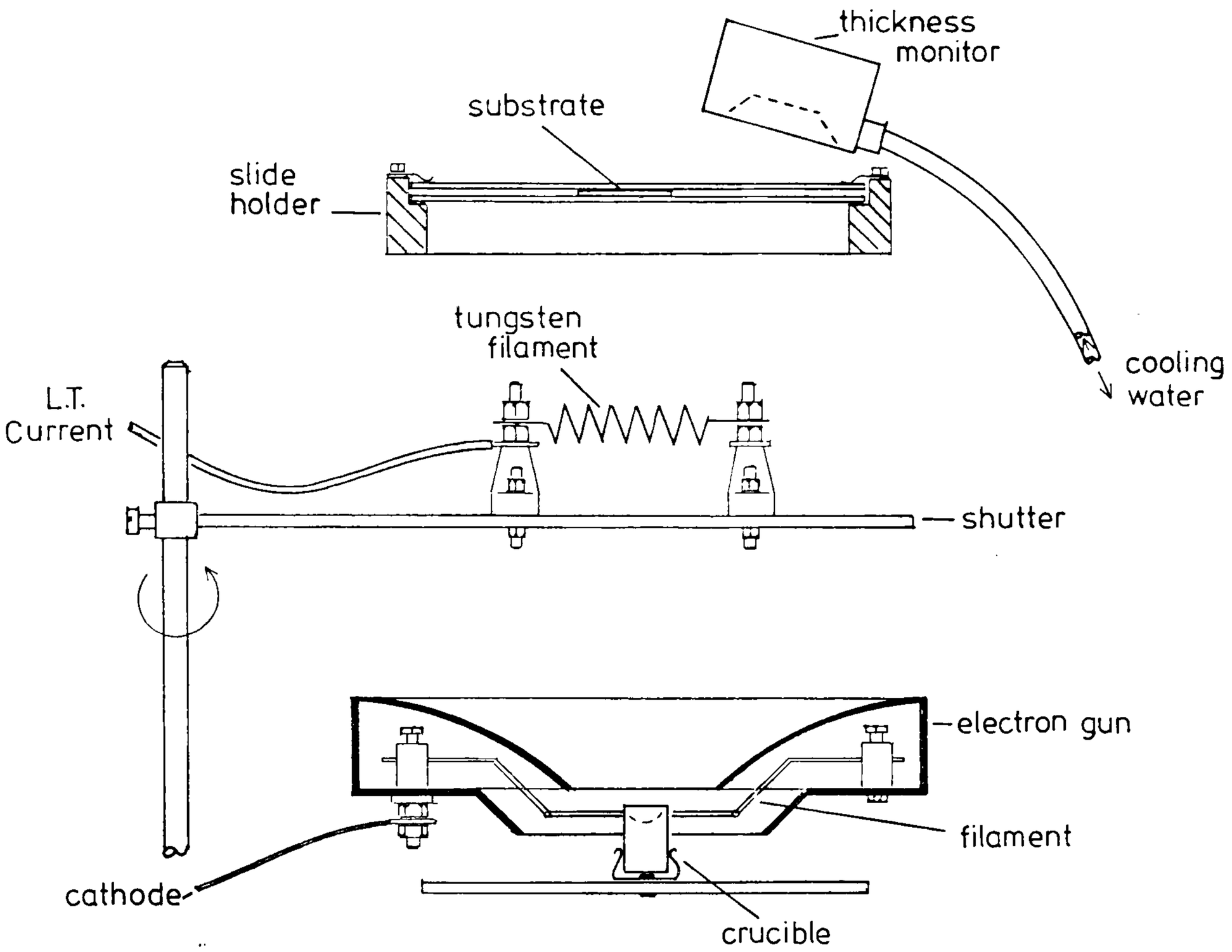


FIGURE 20

Substrate in Slide Holder

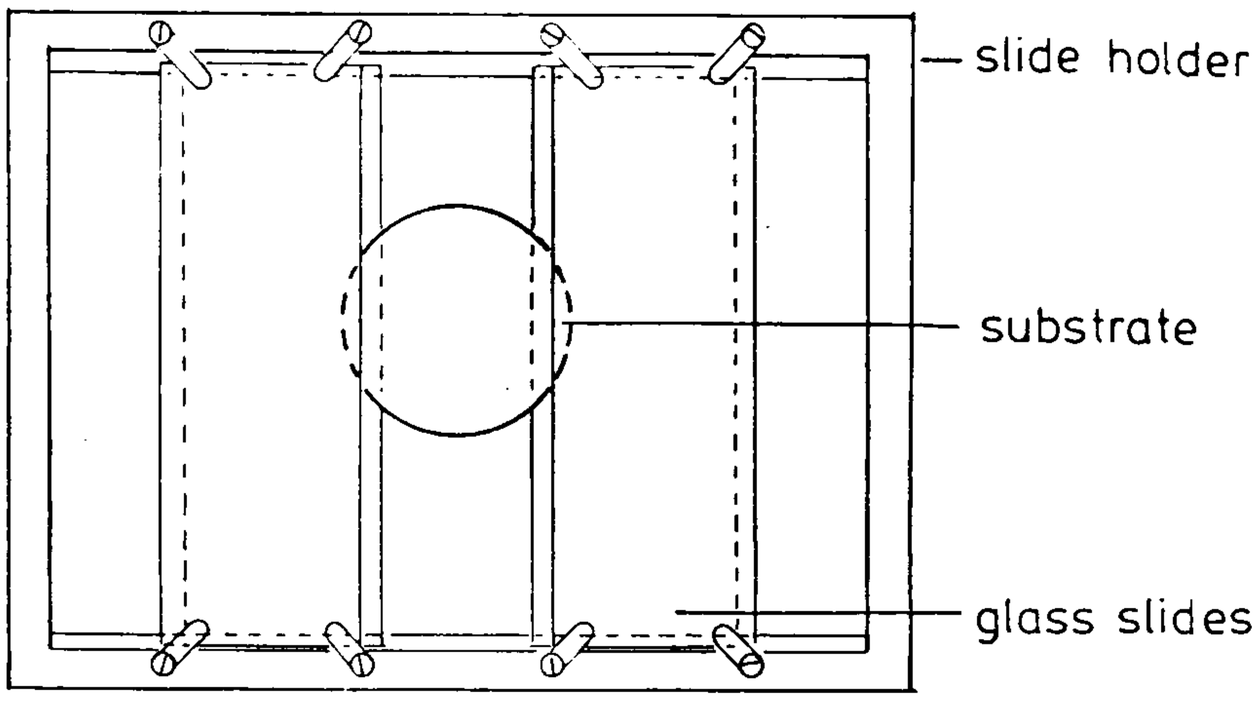


FIGURE 21

Substrate Mask

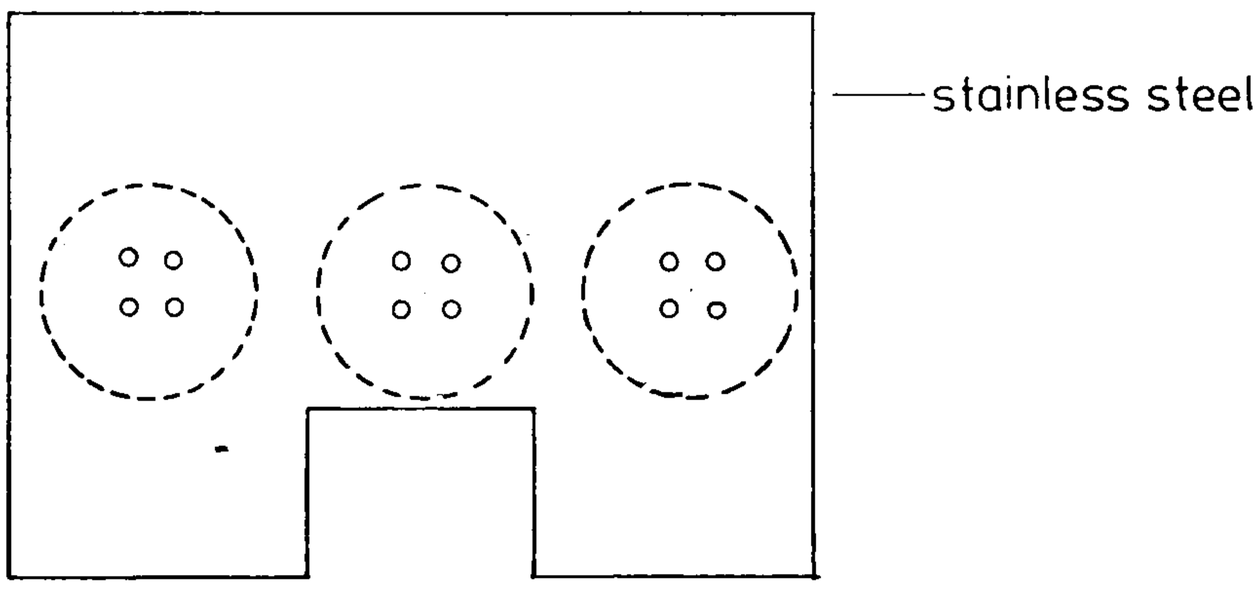
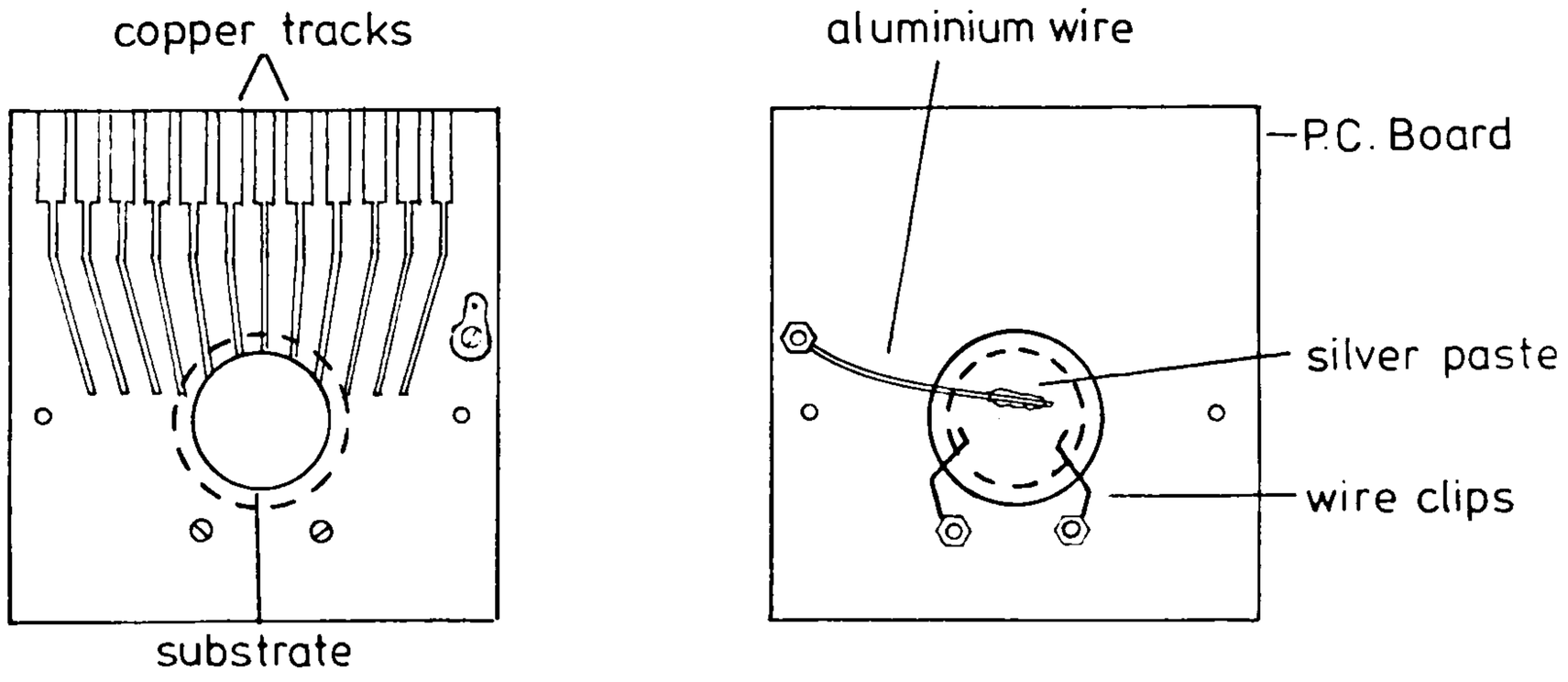


FIGURE 22

Sample Holder



of the Germanium substrate's surface was left exposed. A stainless steel mask, Figure 21, was used to limit the area of condensation on to the sample. Several samples could have contacts evaporated on to their surfaces simultaneously.

Appreciating the desirability of evaporating metal contacts on to the CdS film within the high vacuum equipment, i.e. without exposing the film to the air, this was attempted. But the results were inconsistent: devices produced under superficially identical conditions showed very different electrical characteristics. Some had very low resistances - especially the Copper contact devices - and it is believed that the inconsistencies were probably attributable to contamination, which at the time of the experiments was virtually unavoidable.

6.40 DEVICE FABRICATION

The Germanium substrate, which was typically 2cm in diameter and 0.5mm thick, was polished and cleaned as described in Section 2.61. The substrate was then mounted in the slide holder which was then placed in the Coating Unit. The Copper contact was evaporated on to the substrate. The sample was then removed from the Coating Unit and the cleaning process was repeated. It was then loaded into the high vacuum system and the CdS film evaporated under the desired conditions. Upon removal from the high vacuum system the sample was loaded into the Coating Unit for the evaporation of the metal contacts on to the CdS film.

When several samples were required to have metal contacts evaporated simultaneously for comparison purposes, the samples were exposed to the atmosphere for periods of between an hour

and two days. Ideally all samples should have been exposed for the same period of time but the high vacuum system could only perform one evaporation at a time: if more than one type of metal was required to be evaporated on to a sample it was necessary to expose samples to the air between evaporations.

The sample, complete with metal contacts, was then mounted and clipped to a sample holder as shown in Figure 22. The sample holder consisted of a printed circuit board etched to leave suitable Copper tracks for making electrical contact to the devices. The sample, with the CdS film uppermost, was mounted below a hole in the printed circuit board and held securely in place by wire clips which allowed it a small degree of thermal expansion and contraction during the temperature experiments.

The electrical connection to the Copper film on the Germanium was made by an Aluminium wire coated with silver paste. A connection was made between the wire and the printed circuit board by means of a small nut and bolt. To make an electrical connection to the CdS contacts it was necessary to prepare a short length of gold wire with a gold ball formed at one end. The ball was formed by heating one end of the wire with a flame, and, when coated with silver paste it could then be stuck on to the CdS contact. The other end of the gold wire could then be stuck with silver paste, on to one of the copper tracks on the printed circuit board.

The sample holder allowed the fragile samples to be handled easily and convenient electrical connection to the devices of the sample to be made by soldered connections to the copper tracks on the printed circuit board.

Thermal compression bonding was investigated as an alternative method of making electrical connections to the devices. This required that the ball formed at the end of a gold wire be pressed on to a heated area of the device's metal contact. The gold ball would fuse with the metal of the contact to form a strong bond. However, this bonding method requires that

a) the metal contact is over 0.5 μm thick,

b) the mechanical contact between the CdS and the metal contact is strong,

c) the contact is not adversely affected by heating.

Copper and Chromium contacts with thicknesses over 0.5 μm were difficult to achieve without heating examples excessively during the evaporation. All three types of contact to CdS appeared to have poor adhesion and the copper contacts oxidised as they were heated. Because of this thermal compression bonding was discarded.

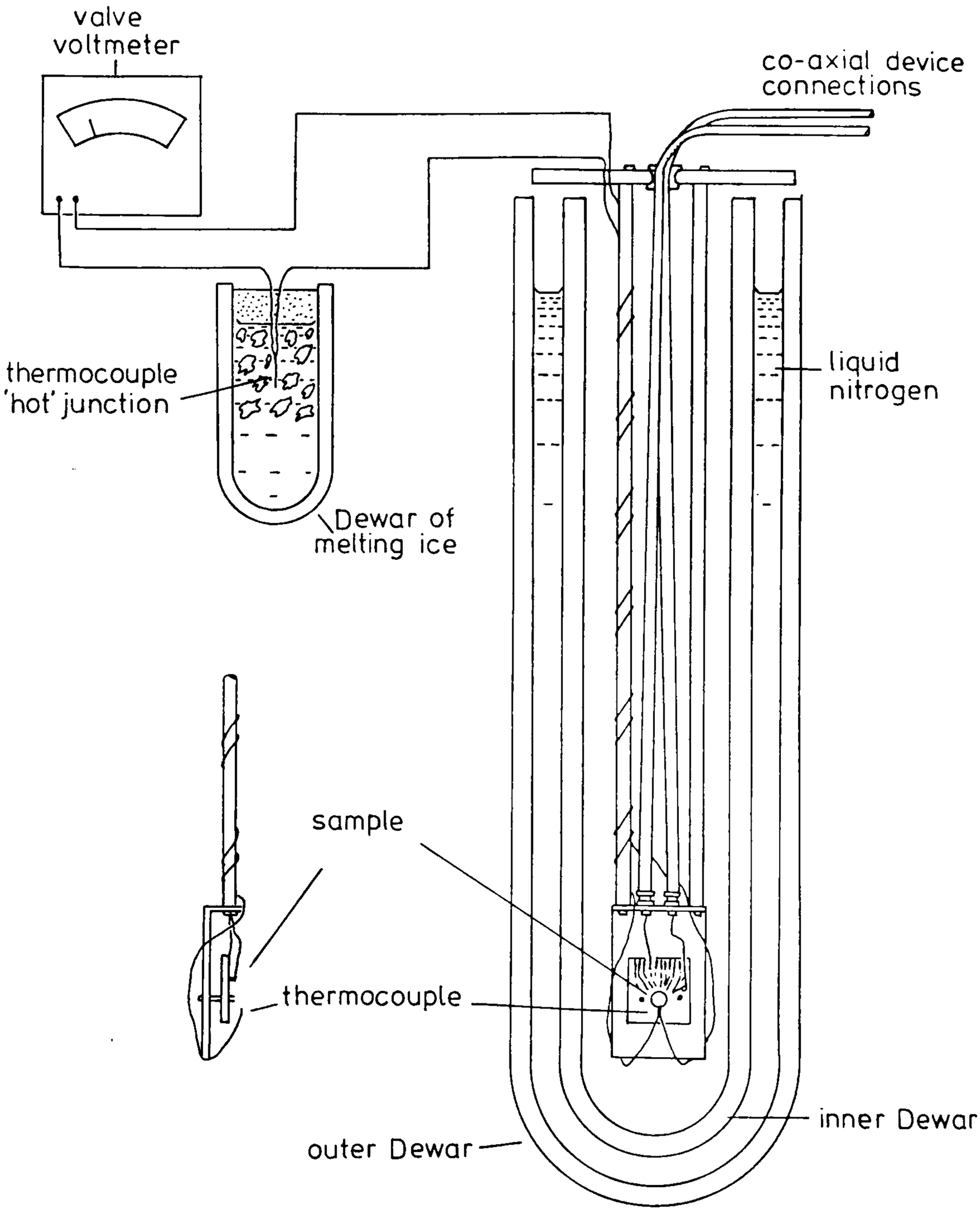
6.50 SAMPLE BOARD MOUNTING

6.51 Room and low temperature experiments

The sample mounted on its board was attached to the plate at the end of the supporting assembly so that the device could be lowered into the inner Dewar of a double Dewar arrangement as shown in Figure 23. In this position the device was in semi-darkness. A Chromel-Alumel thermocouple was located close to the device for temperature measurement. The "hot junction" of the thermocouple was kept at 0^{o}C by immersion in a small Dewar of melting ice. The thermocouple e.m.f. was measured with a valve voltmeter. Electrical connections were made to the sample board via two co-axial cables with their screens connected to the supporting assembly.

FIGURE 23

Low Temperature Experiment Apparatus



The temperature of the sample depended on the quantity of liquid nitrogen in the outer Dewar and when the outer Dewar was filled to the top the temperature recorded by the thermocouple was 85°K. The temperature measurement was checked by using the liquid nitrogen temperature of 77°K as a reference.

The outer Dewar was not topped up during the experiment so the temperature rose as the liquid nitrogen boiled off. The temperature at the bottom of the inner Dewar rose slowly to begin with and reached a maximum rate of 1°C/min after two hours, before slowing down to reach room temperature 3½ hours later. The electrical characteristics before and after were compared to ensure that no permanent change in the device had taken place during the experiment.

When the devices were taken to a lower temperature by the use of liquid Helium, the room temperature characteristics were observed to have been considerably changed, indicating that permanent changes had occurred. In some cases the CdS film began peeling off the substrate as the device returned to room temperature even though Germanium and CdS have similar temperature coefficients of expansion.[63]

6.52 High temperature experiments

The sample holder mounted on the lower plate, now removed from the supporting assembly, was suspended in an oven as shown in Figure 24. The oven had an in-built fan ensuring that the hot air was well distributed. The temperature of the air inside the oven was measured by the Chromel-Alumel thermocouple and a thermometer. The oven was equipped with a thermostat allowing the temperature to be controlled to within ±1°C. The samples

FIGURE 24

High Temperature Experiment Apparatus

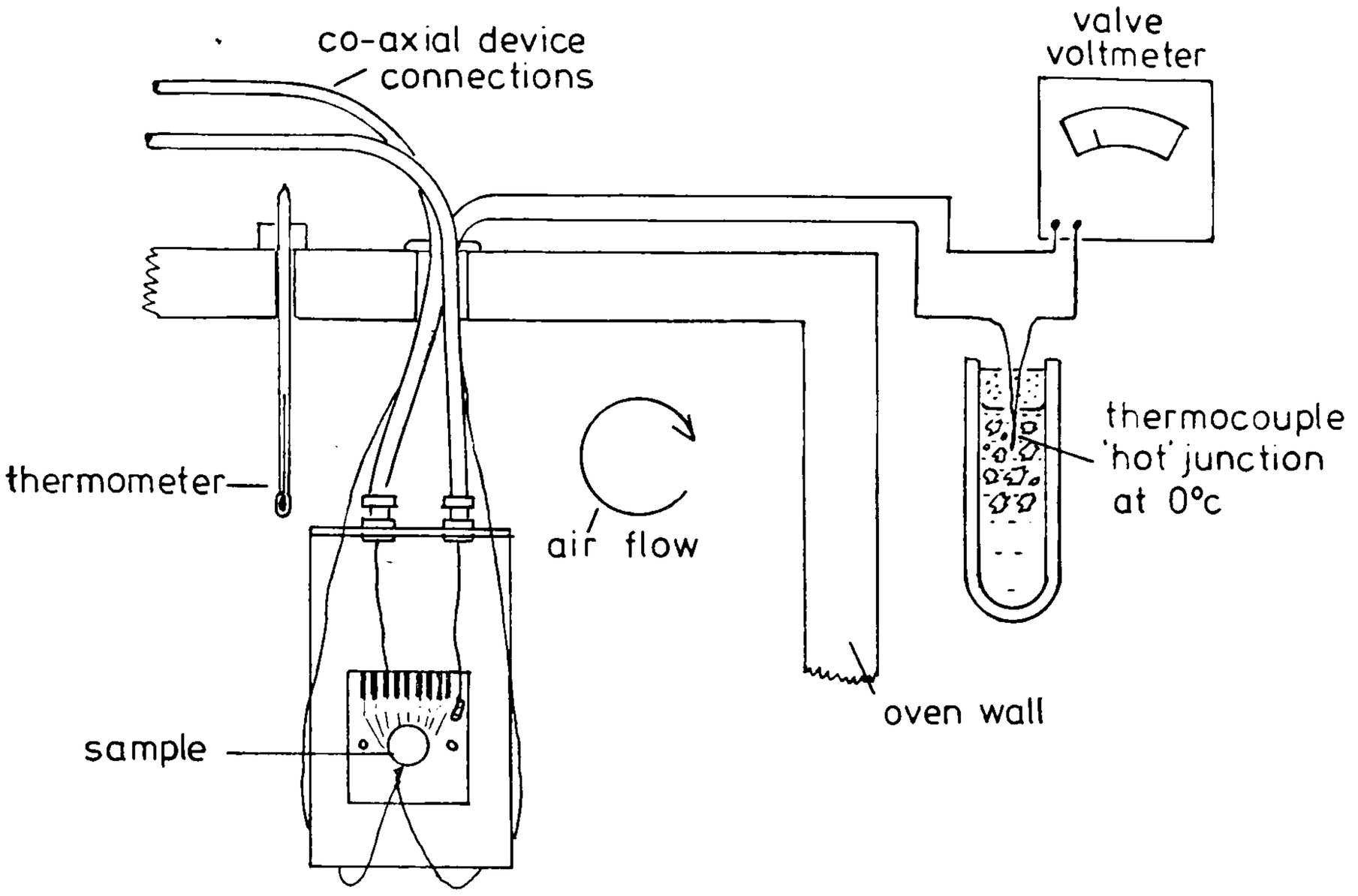
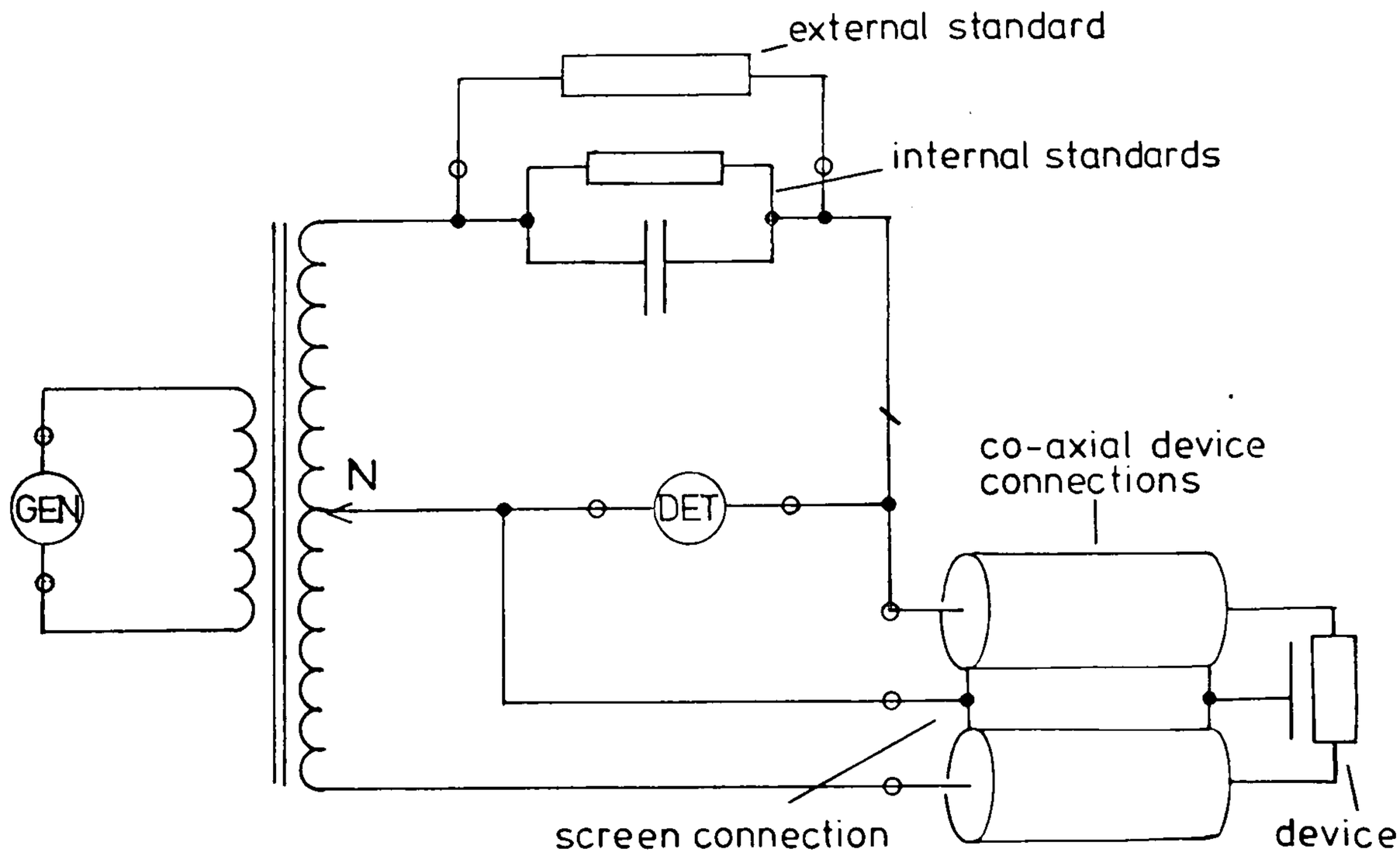


FIGURE 25

Simplified circuit of the GR bridge (zero bias measurements)



were allowed to stabilise at each new temperature before measurements were taken.

6.60 CAPACITANCE AND CONDUCTANCE MEASUREMENTS

The capacitance and conductance of devices can give considerable information about their electronic structure and the dependence of these two properties on frequency, d.c. bias and temperature was investigated.

The accuracy of the capacitance measurements depends on the conductance of the device as well as the sensitivity of the bridge.[86,87] Devices with loss factors* below 0.15 allow capacitance to be measured to an accuracy of a small fraction of a picofarad, but typically the devices described in this work have loss factors in the range 1 to 10. High loss factors decrease the accuracy of bridge measurements, as the balance is more difficult to detect.

6.61 Zero bias

Two capacitance bridges were used, the General Radio 1615A, which is a Transformer Ratio-Arm bridge for the frequency range 300Hz to 100kHz, and a Radio Frequency Wayne Kerr B601 bridge for the frequency range 100kHz to 1MHz.

The maximum conductance which can be measured with the internal standards of the GR bridge is 111 $\mu\mho$, but this was not high enough for the majority of the devices. The conductance of the device depended on its state, e.g. in its virgin state the conductances could be as low as 2 $\mu\mho$, but in its switched state it could be as high as 10m$\mho$. The bridge conductance range was

* Loss factor = $\frac{\text{conductance}}{\text{susceptance}}$

extended to 1056 μ℧ by inserting an external standard of 0.945μ℧ in parallel with the bridge standards, as shown in Figure 25. The external standard consisted of a resistor totally enclosed in a small brass box connected to the bridge by two GR chassis connectors. The external standard could be added to the bridge standards in increments of 94.5μ℧ up to a maximum of 945μ℧ by means of a decade switch.

The external standard added a small amount of capacitance as well as conductance to the bridge standards. The effective capacitance was 8pF for every increment of 94.5 μ℧ . The presence of this capacitance was shown when measuring a device with a capacitance of 80pF and a conductance of 100 μ℧ . When the device was measured without the addition of the external standard the true values were indicated, but when the decade switch applied 94.5μ℧ in parallel with the bridge standards the bridge showed the device as having a capacitance of 72pF and a conductance of 5.5 μ℧ .

The "3 terminal" method[85,86] was used to reduce the effect of stray capacitances and leakage currents. This was accomplished by connecting the screens of the co-axial cables (connecting the device to the bridge) to the neutral line, as represented by N in Figure 25. This effectively allowed the bridge to balance the conductance and capacitance of the device alone. Open circuit tests showed the complete experimental set up as having an effective capacitance of 2.4pF and leakage conductance of 0.16 μ℧ .

The input voltage to the bridge was limited to ensure that the voltage across the device was 35mV±10mV peak to peak. It was necessary to limit the voltage across the device as voltages in

excess of 70mV affected both the capacitance and conductance. This was due to the rapid increase of device conductance with voltage resulting in the bridge presenting non-sinusoidal voltage signals to the detector. Voltages below 20mV, on the other hand, made balancing difficult as the voltage to be detected was low even when the maximum gain of the Rohde and Scharz UMB detector used was 60dB.

The absolute accuracy of the GR bridge is stated[85] as less than 0.3% for the frequency range 50Hz to 100kHz and capacitances between 1pF and 0.01 μF but this level of accuracy cannot be achieved for high loss factor devices when the voltage applied to the device is limited. It was possible to measure the low frequency conductance and capacitance with an accuracy of better than 1.5% when the corrections for stray capacitances and conductances had been made. At higher frequencies the accuracy decreased to ±10pF and ±2 μU in the worst cases.

The absolute accuracy of the Wayne Kerr bridge[86] is stated as 1% in the range 15kHz to 5MHz but this bridge was also affected by the high loss factor of the device and the limited applied voltage. At 100kHz there was at most an 8% difference in the capacitance and a 6% difference in the conductance between measurements on the two types of bridge.

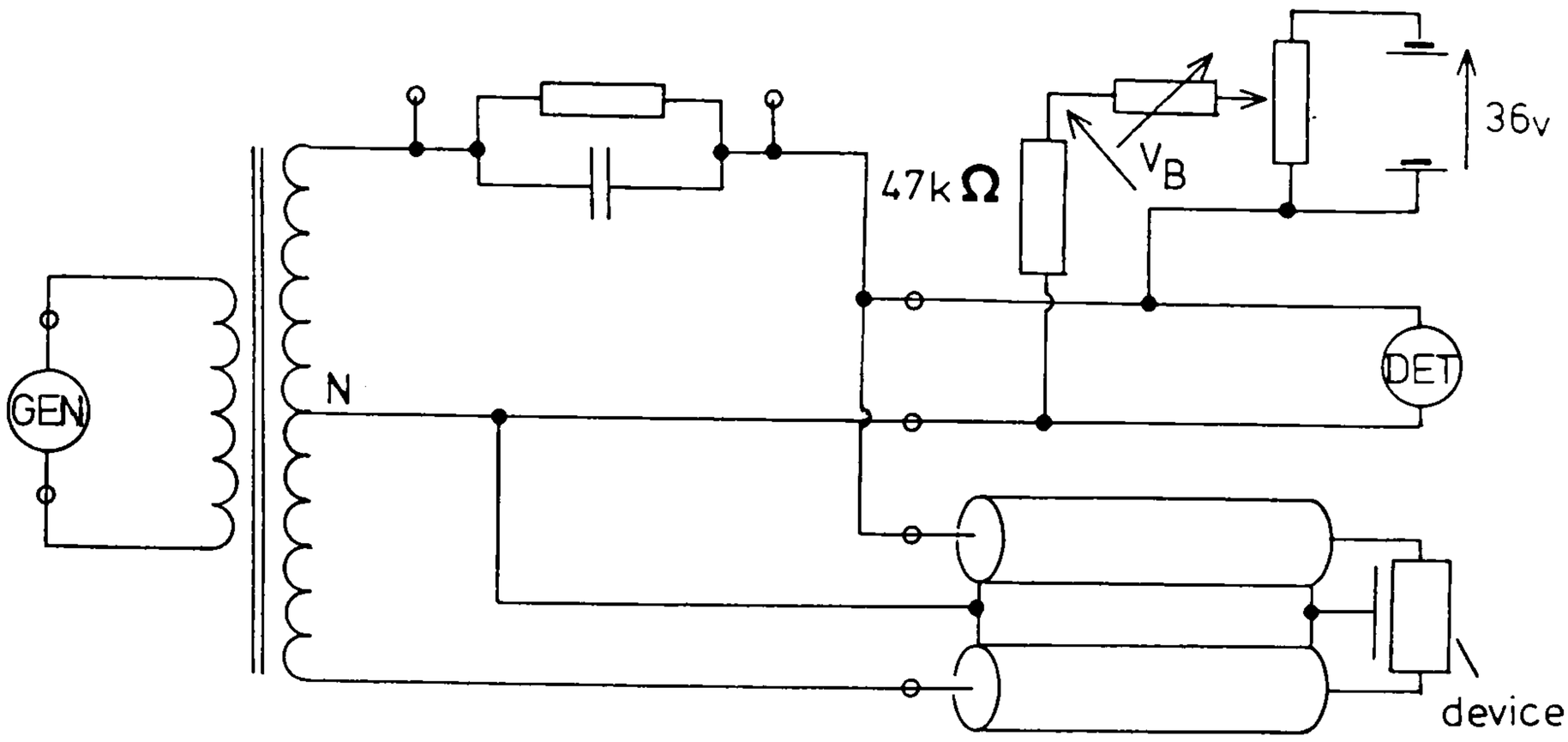
6.62 Variable bias

Figure 26(a) shows the simplified circuit of the GR bridge and the external circuit which allowed a d.c. voltage to be applied to the device during the capacitance and conductance measurements. The d.c. voltage was supplied by a group of 4.5v dry cell batteries in series and the voltage was set by means of

FIGURE 26

Simplified circuit of the GR bridge
(Variable bias measurements)

a) a.c. circuit



b) equivalent d.c.circuit

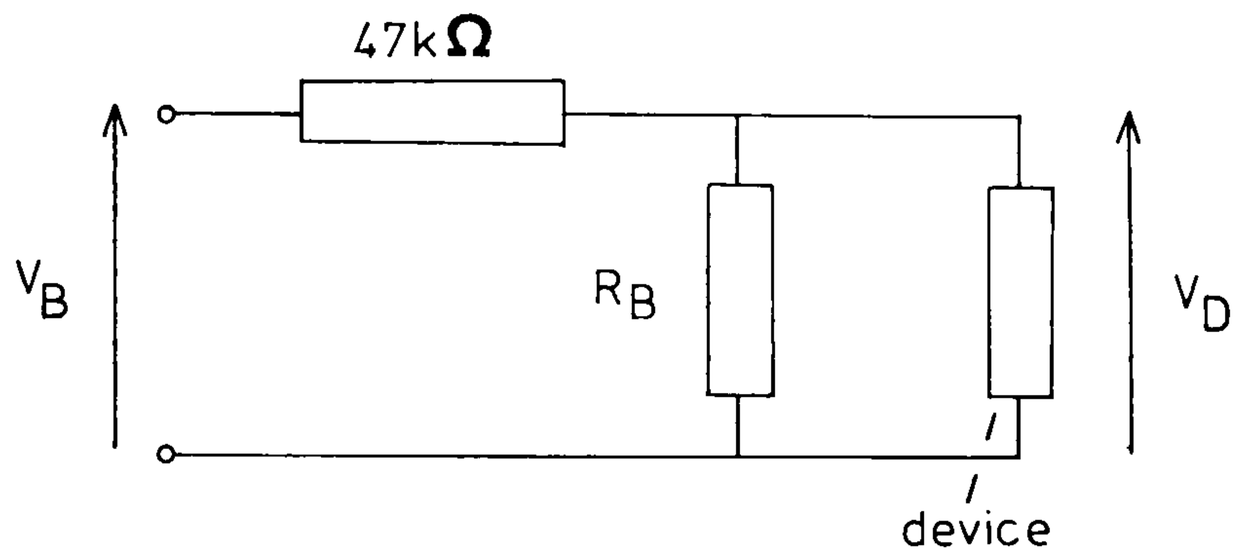
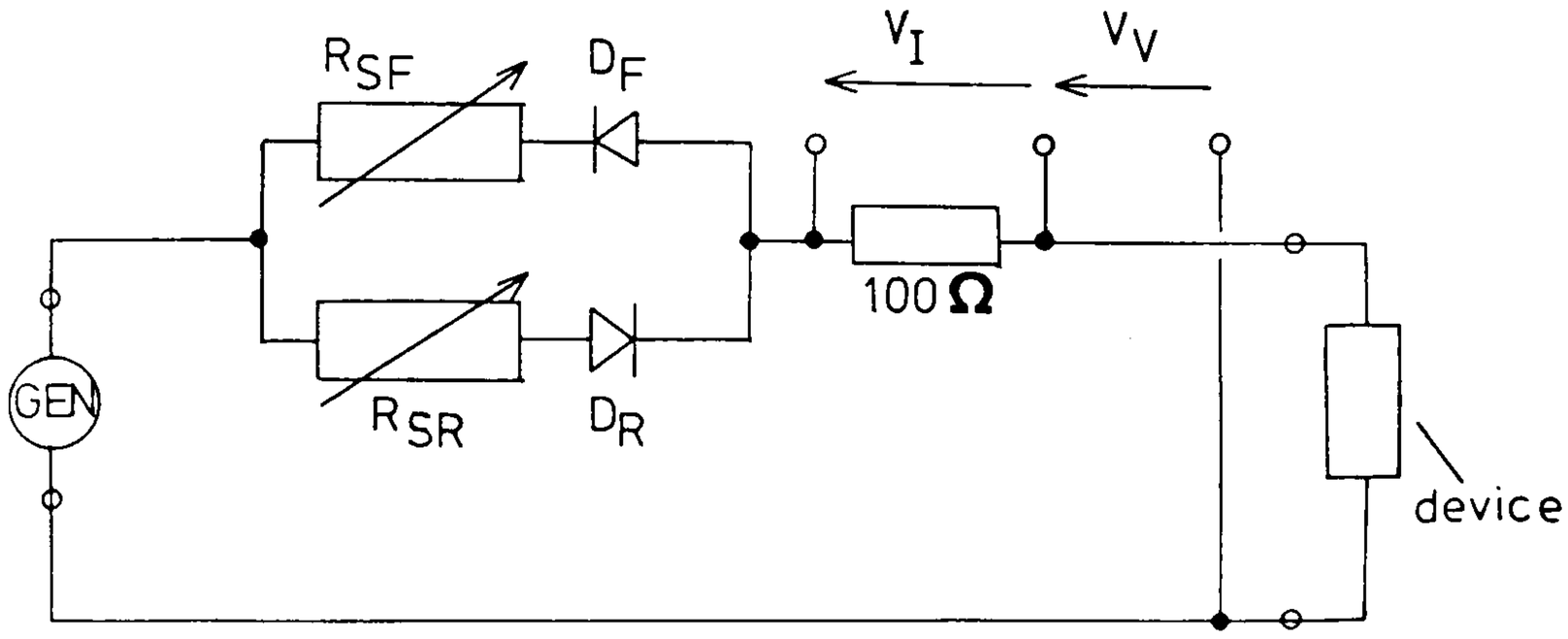


FIGURE 27

Circuit for I-V characteristic CRO display



two potentiometers, one for crude and one for fine adjustment. The 47kΩ resistor, mounted in the GR 874 enclosure was used to isolate the d.c. voltage circuitry from the bridge. Figure 26(b) shows the equivalent d.c. circuit of the bridge, device and d.c. supply. The resistance R_B is the effective resistance of the bridge and it depends on the bridge range selected and the conductance standards switched in.

The maximum d.c. current which the bridge can be subjected to without magnetisation of the transformer is 8mA.[85] The external circuit ensured that the batteries could not supply more than 1mA to the bridge.

The effect on the bridge of the external circuit was to add considerable inductance to the device side. The measurement of a resistor appeared to indicate an inductance the equivalent of 810pF for every increment of the external standard decade switch. For example, if a device was measured to have an apparent inductance of -1030pF and the external standard switch was applying two increments, i.e. 2 x 94.5μΩ and 2 x 810pF, then the true capacitance of the device would be 1620pF - 1030pF = 590pF. This correction factor appears to be independent of the frequency of the signal and the d.c. voltage applied to the device.

It was not possible to measure the d.c. voltage applied to the device and the capacitance and conductance simultaneously, as the valve voltmeter used to measure the voltage interfered with the normal operation of the bridge. The d.c. device voltage, V_D, was found indirectly by measuring V_B, the d.c. voltage applied to the 47kΩ resistor.

$$V_D = V_B \frac{R_B}{47k\Omega + R_B}$$

This formula can only be used when the device resistance greatly exceeds the effective bridge resistance R_B, which is $100k\Omega \pm 2k\Omega$ for the ranges required. When the device's resistance was low it was necessary to measure directly the d.c. device voltage after the bridge had been balanced.

Before measurement with the bridge it was necessary to discover the range of applied d.c. voltage within which the device was stable and did not drift. It was also necessary to measure the device's d.c. electrical characteristic after the bridge measurements to ensure that its state had not changed during the experiment.

6.70 CURRENT - VOLTAGE CHARACTERISTIC MEASUREMENT

The current-voltage characteristics of the device were displayed on a CRO screen with the aid of the circuit shown in Figure 27. The CRO, a Tektronics 531A, had to have a "floating earth" to allow the device voltage signal V_V and the voltage signal V_I, representing the device current, to be applied to the X and Y plates of the CRO respectively. A sine wave was applied to the input terminals from a signal generator. The diodes D_F and D_R determine which series resistance R_{SF} or R_{SR} applies under forward and reverse biases respectively. R_{SF} and R_{SR} are independent switch selected resistance values from 300Ω to $100k\Omega$ and both switches have an "open circuit" position.

The resistances only become important when the device switches from one state to another. The series resistance determines the path of switching. If, for example, the series resistance is very much greater than the device resistance during switching then the device will switch with constant current. On the

other hand, if the series resistance is zero the device current can rise indefinitely during switching.

The frequency of the applied signal was limited to 50Hz. At lower frequencies some device characteristics were not reproducible through the current drifting with time. This current drift was very pronounced when the device characteristic was displayed on an X-Y recorder with the applied d.c. voltage manually controlled. At higher frequencies, e.g. above 100Hz, the capacitance of the device resulted in a "looping" effect being displayed on the screen caused by the voltage being out of phase with the current.

With the circuit used it was possible to apply single polarity signals and control their magnitude by adjusting the signal generator output level. Continuous switching was also possible and the series resistance under forward and reverse bias could be adjusted independently.

This dynamic method of measuring the device characteristics was chosen because of the drift often observed at currents in excess of a few microamps. For more accurate measurement of the device current-voltage characteristic at current levels below 1 μA, the oscilloscope was replaced by two valve voltmeters, to measure V_V and V_I, and the signal generator was replaced by a d.c. power supply.

The CRO was calibrated with its reference voltage, and the valve voltmeters with the CRO and an AVOmeter. The resistance R_I, which was used to measure the device current, was checked to be $100\,\Omega \pm 0.5\,\Omega$. The overall accuracy of current and voltage measurement was better than ± 2% over the voltage range 10mV to 10V and the current range 10 μA to 10mA.

CHAPTER 7

7.00 CHARACTERISTICS OF Ge - CdS - Cu MEMORY DEVICES

7.10 INTRODUCTION

This chapter describes in detail the characteristics of Ge - CdS - Cu memory diodes and proposes a switching model which attempts to explain the observed phenomena.

The characteristics described are the result of measurements on scores of devices. The performance of every device depends strongly on the fabrication parameters and in absolute terms no two devices produced identical characteristics. This chapter will describe the general trends observed and the following chapter the dependence of the device characteristics on the fabrication parameters.

It was always necessary to test every device repeatedly to ensure the validity of the measurements. The mere act of testing these sensitive devices could cause a profound change in their characteristics. This was particularly true for capacitance experiments where the current-voltage characteristics before and after were compared to ensure that the experiment itself had not changed the state of the device.

The results of this chapter are based on devices with the fabrication parameters:

Germanium substrates:	Gallium doped 10^{17} to $10^{19} cm^{-3}$ Orientation (100) Thickness 0.5 to 1.0mm
Cadmium sulphide film:	Substrate temperature 180 to 230°C Condensation rate 1000 to 3000Å/min Thickness 2 to 2.5 μm

Copper contact : CdS exposed to air
CdS at 50 to 80°C during Copper condensation
Thickness 0.5 to 1 μm
Area 1 or 3.5mm^2

These devices had very distinctive characteristics similar to those of devices fabricated from different types of materials by very different processes. Interest has always centred on the switching of such devices.

The virgin, OFF and ON states have not been so thoroughly investigated although these states can offer much information on the electronics of the devices.

The device electronics are far removed from the precise and well-understood physics of p - n homojunctions of Germanium and Silicon. Heterojunction and non-ohmic metal semi-conductor junction devices have more complex characteristics, especially when fabricated by the evaporation of thin films.

7.20 GENERAL CHARACTERISTICS OF THE DEVICE

The devices, though grown under a variety of conditions, exhibit the same distinctive trends. Devices which are fabricated under superficially identical conditions can show considerable variation of characteristic even though the trends are similar.

The most striking and unusual feature of the device is of course the memory effect. The device has potential applications as a solid state memory which can take advantage of well-established photo-lithographic techniques to produce high density, non-volatile, memory arrays.

The typical current-voltage characteristic of these memory devices is shown in Figure 28. This memory characteristic is exhibited only after the initial "forming" of the device. Switching is not initially exhibited by the device after fabrication. A very high resistance "virgin" state is formed into the switching characteristic by the application of sufficient "breakdown" voltage. The memory switching cycle of these devices from OFF to ON is generally only possible under reverse bias and switching from ON to OFF under a forward bias. (Forward or positive bias is defined as the Germanium being positively biased with respect to the Copper contact on the CdS film)

When the device is in either state, applying small a.c. or d.c. voltages will not affect the zero bias resistance. Applying a reverse bias which allows the current to exceed I_{THR} results in the device switching from OFF to ON, and applying forward bias greater than V_{THF} results in a return to the OFF state.

7.30 THE VIRGIN STATE

The extensive capacitance and conductance measurements are assessed with respect to a model which attempts to represent the device in the virgin state. Some characteristics considered in isolation do not support any model conclusively but it is possible to make valid deductions about the electronics of the device by relating the results of a number of experiments.

7.31 Outline of the device characteristics

Figure 29 shows the current-voltage characteristic of the device when subjected to a 25Hz sine wave. The "looping"

FIGURE 28

Current-Voltage Characteristic of the
Ge-CdS-Copper Memory Device

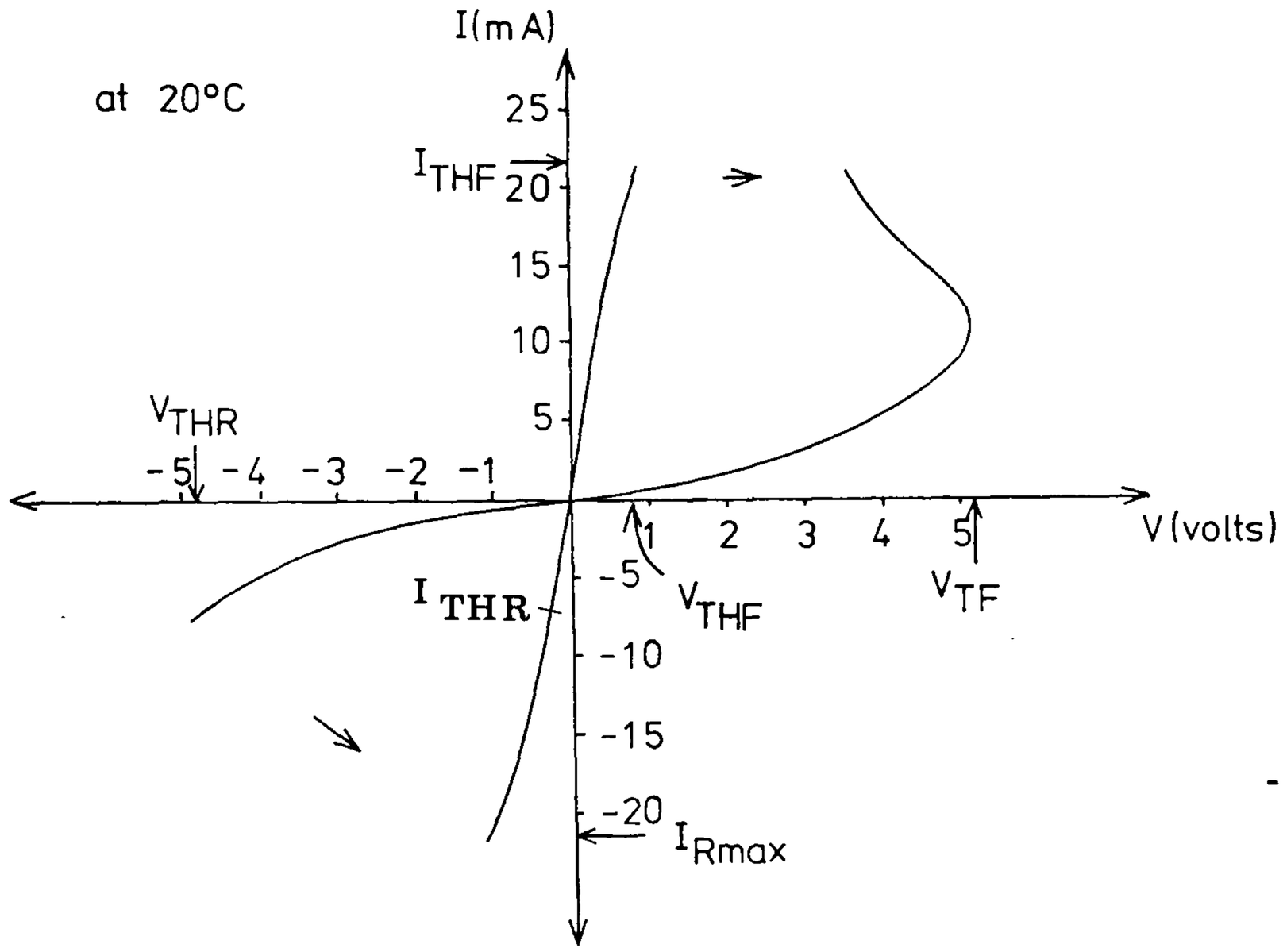
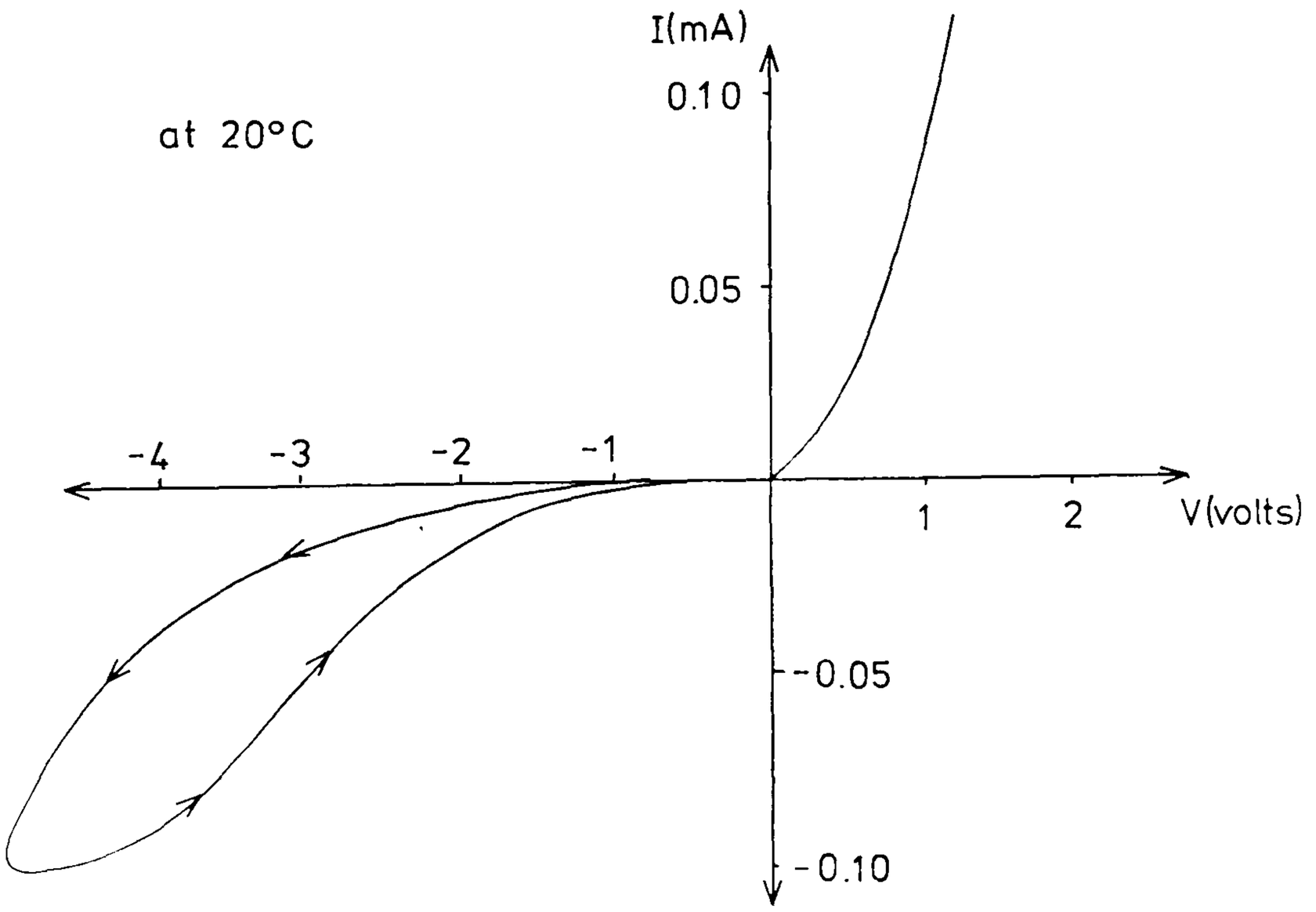


FIGURE 29

Current-Voltage Characteristic of the device
virgin state under a 25Hz sine wave voltage



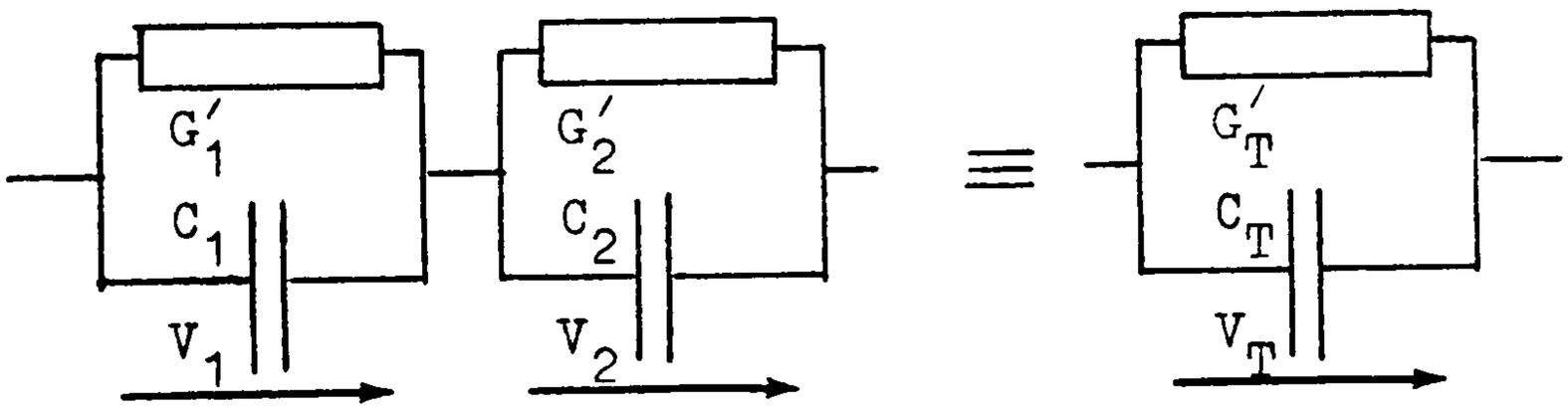
effect clearly seen under reverse biases is dependent on the frequency and magnitude of the applied signal. The effect is inductive and typical of the "current creep" effects[88] which can be associated with power dissipation significantly changing the device temperature and conductance. The characteristic is clearly rectifying with the "easy" direction under forward bias, and shows considerable similarity to point contact device characteristics.[88]

The device shows considerable frequency dispersion at low frequencies, and capacitance and conductance are proportional to the device area. The devices are also very sensitive to light and temperature.

7.32 Capacitance, conductance dependence on frequency

i) Measurement and model

Consider for the moment that two regions exist within the device and that the equivalent circuit of each region is a capacitance and conductance in parallel. Two such regions in series will result in an overall equivalent circuit.



where $C_1 = f_1(V_1,w)$ is the capacitance of Region 1

$C_2 = f_2(V_2,w)$ is the capacitance of Region 2

$G_1 = g_1(V_1,w)$ is the conductance of Region 1

$G_2 = g_2(V_2,w)$ is the conductance of Region 2

V_1 and V_2 are the d.c. voltages distributed over the two Regions 1 and 2

$V_T = V_1 + V_2$ is the total d.c. voltage over the device

w is the frequency of a small signal a.c. voltage

The overall admittance of the circuit can be expressed as a parallel capacitance, C_T, and conductance G_T, where

$$G_T = \frac{(w/w_1)^2 + 1}{(w/w_2)^2 + 1} \cdot G_0(G_1,G_2) \quad \ldots\ldots\ldots\ldots (6)$$

$$C_T = \frac{(w/w_3)^2 + 1}{(w/w_2)^2 + 1} \cdot C_0(G_1,G_2,C_1,C_2) \quad \ldots\ldots\ldots (7)$$

where $w_{1,2,3}$ are characteristic frequencies which will depend on the parameters G_1, G_2, C_1 and C_2. (The full equations appear in Appendix I)

Even if the parameters are assumed frequency independent, G_T and C_T are likely to have a frequency dependence. (The only exception results from $C_1G_2 = C_2G_1$ and in this case G_T and C_T will have the same frequency dependence, if any, as G_1 and C_1) Within the frequency range of this experiment we assume that the parameters are frequency independent.

The experimental capacitance characteristic shown in Figure 30 is typical of these devices. A theoretical characteristic consistent with C_o = 1300pF, $w_2 = 3.1 \times 10^4$rad/s and $w_3 = 9.8 \times 10^4$rad/s can be chosen to fit the experimental curve at its greatest change of log (capacitance) with log (frequency). Although the two characteristics show divergence at both high and low frequencies the same distinctive trend can be observed. The divergencies at high and low frequencies indicate a frequency dependence of the parameters of the order of $C \propto w^{-0.13}$ which is superimposed on the frequency dependence described by Equation 7.

The theoretical characteristic shown is only valid between 6 and 30kHz. Other theoretical characteristics could be chosen

FIGURE 30

Virgin State Capacitance versus Frequency

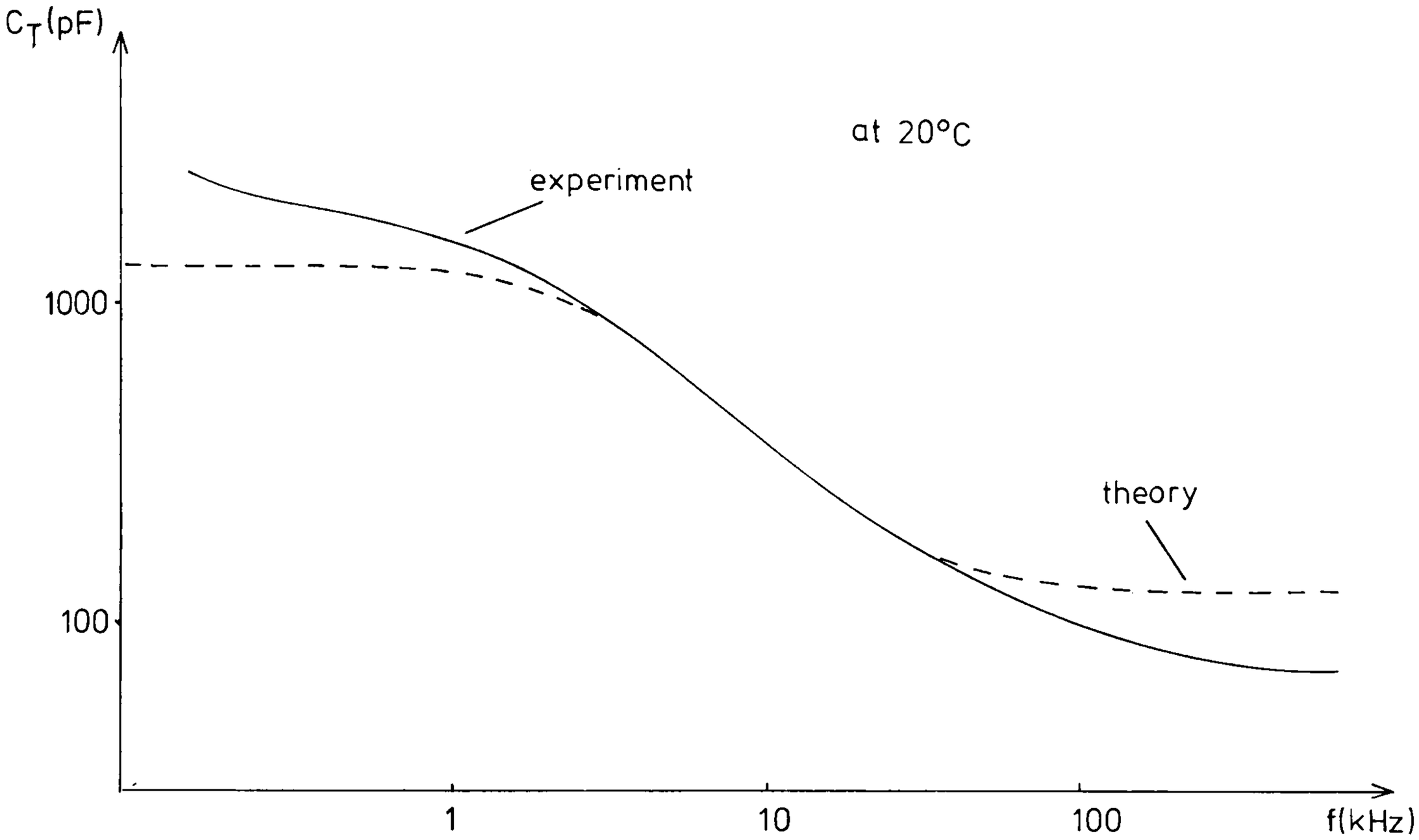
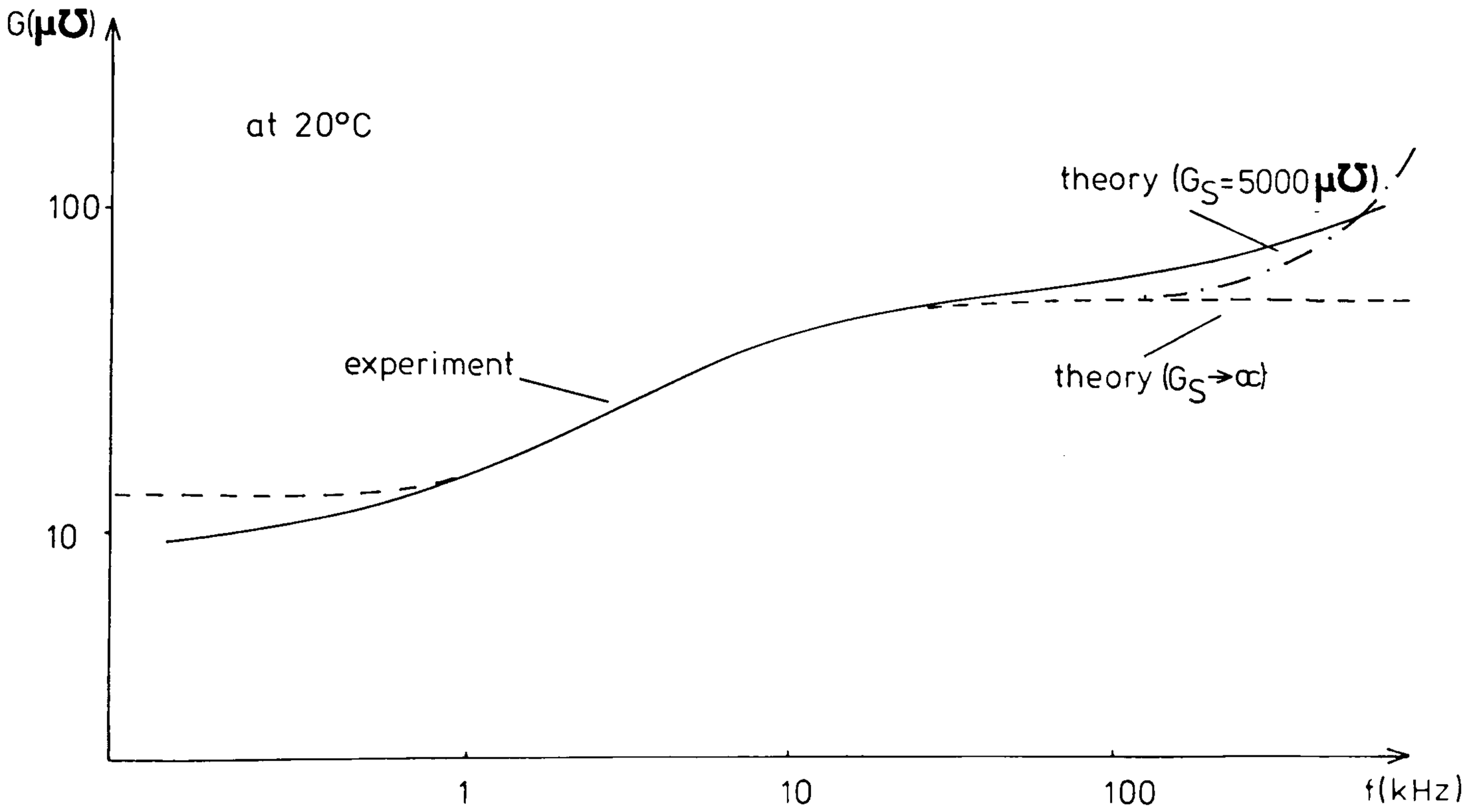


FIGURE 31

Virgin State Conductance versus Frequency



to fit the experimental curves at higher and lower frequencies, but these characteristics will have less validity due to the interference of parameter frequency dependences. C_o, w_2 and w_3 alone do not determine the parameters, but rather the interdependence of the parameters.

The parameters can however be determined by considering both the conductance and capacitance dependence on frequency.

Figure 31 shows the experimental conductance associated with Figure 30. The theoretical characteristic consistent with $G_o = 13\,\mu\mho$, $w_1 = 1.6 \times 10^4$ rad/s, and $w_2 = 3.1 \times 10^4$ rad/s, fits the experimental characteristic closely over the frequency range 1 to 25kHz. Using Equations 6 and 7 and the values G_o, C_o, w_1, w_2, w_3 derived from the experimental characteristics, the parameters can be calculated to be

$$C_1 = 2240\text{pF}, \quad C_2 = 138\text{pF}, \quad G_1 = 17.5\,\mu\mho, \quad G_2 = 56\,\mu\mho$$

which are valid over the frequency range 6 to 25kHz.

At frequencies greater than 25kHz the experimental conductance characteristic shows a continued increase with frequency. This trend could of course be a result of the frequency dependence of the parameters, particularly G_2, or of a conductance G_S in series with regions 1 and 2. The overall admittance of the circuit including G_S can be expressed as a parallel capacitance, C_D, and conductance, G_D, where

$$G_D = \frac{(w/w_4)^2 + 1}{(w/w_5)^2 + 1} \cdot G_X(G_T, G_S) \quad \ldots\ldots\ldots\ldots (8)$$

$$C_D = \frac{1}{(w/w_5)^2 + 1} \cdot C_X(G_T, G_S, C_T) \quad \ldots\ldots\ldots (9)$$

and $w_{4,5}$ are characteristic frequencies which are dependent on

the parameters G_T, G_S and C_T. (The full equations appear in Appendix II) G_T and C_T themselves are frequency dependent as shown by Equations 6 and 7.

Only if G_S is sufficiently large will the low frequency characteristic be unaffected by the inclusion of G_S, i.e. if G_S is much greater than G_2 and G_1, then G_D and C_D simplify to G_T and C_T. If G_S is not sufficiently large, a complex characteristic results.

At very high frequencies, w much greater than w_4, the device conductance is G_S and capacitance decreases at a rate proportional to w^{-2}. The theoretical plot shown in Figure 31 is with $G_S = 5000\ \mu\mho$ and assumes the previously deduced parameters. The low frequency characteristic is not significantly affected by the addition of G_S. Only at frequencies in excess of 100kHz is the conductance beginning to rise towards G_S. The resultant reduction of capacitance will not be observed at these frequencies. It may be deduced however that G_S can be greater than $5000\ \mu\mho$; if not, the observed increase in conductance will occur more rapidly at lower frequencies. If instead of adding G_S to our model, a third region is added with parallel conductance G_Y and capacitance C_Y in series, then it is possible for C_Y to be large without affecting the low frequency characteristics. The necessary condition for this is

$$\frac{G_Y}{C_Y} \gg w_3 \gg \frac{G_1 + G_2}{C_1 + C_2}$$

i.e. G_Y must be very large if C_Y is of the same order of magnitude as $C_1 + C_2$. Thus a large capacitance in the device may remain undetected as long as its parallel conductance is large.

ii) Discussion

The basic assumption which was made in the previous section was that no other frequency dependent mechanism or mechanisms would produce the observed dispersion. The equivalent circuit model has been shown to give results corresponding to the experimental measurements, but several other frequency dependent mechanisms need to be considered.

It has been shown that the dielectric constant, ϵ_r, of a CdS film grown under similar conditions has a frequency dependence with a relaxation time of 20mS.[89] Over the frequency range up to 200kHz, ϵ_r decreases by a factor of 2, but the device capacitance can decrease by a factor of 29. Clearly the frequency dependence of CdS is not the major cause of the dispersion characteristics of the device. The high conductance of the Germanium ensures that its relaxation time is so short that significant dispersion only occurs at frequencies far in excess of 200kHz.

The capacitance of an ideal CdS Schottky junction will also have a frequency dependence through ϵ_r at these frequencies, but again the effect is weak. At higher frequencies the Schottky diode has a stronger dependence on frequency, i.e. $C \alpha w^{-\frac{1}{2}}$ and $G \alpha w^{\frac{1}{2}}$,[61] which does not correspond to the experimental measurements.

Junctions made with wide energy band gap semi-conductors with high trap densities[90] show strongly dispersive characteristics as do Metal-Insulator-Semi-conductor junctions[92] but neither shows the distinctive symmetrical characteristics observed.

Thus the equivalent circuit model seems to be the only viable explanation for the observed measurements.

The high value of capacitance in Region 1, 2.2nF, is far in excess of the geometric capacitance expected from the Germanium, 0.3pF, or the CdS film, 50pF. This indicates the existence of a junction or a dipole layer[83] within the device.

The capacitance of Region 2, 138pF, is more consistent with the CdS film. The conductance of this region, 56$\mu\mho$, allows the resistivity to be calculated as $10^6\ \Omega$cm from its geometry. This resistivity is close to that found from the relaxation time calculations,[89] and is typical of CdS evaporated films.[5,90]

Typical mobilities for evaporated CdS films range between 1 and $50 cm^2/Vs$.[5,66] Using these mobilities in conjunction with the resistivity deduced above, the free electron density is calculated to be between 1.2×10^{11} and $7 \times 10^{12} cm^{-3}$, which implies that the fermi level lies between 0.37 and 0.47eV below the Conduction Band at room temperature.

7.33 Capacitance, conductance dependence on temperature

i) Measurement and model

Figures 32 and 33 show the temperature dependence of capacitance and conductance respectively. The low frequency graph of log (C_T) versus $(\text{Temperature})^{-1}$ shows considerable similarity to the log (C_T) versus log (w) characteristics of the previous section. This can be explained by considering Equation 7 at low frequencies

FIGURE 32

Virgin State Capacitance versus Temperature

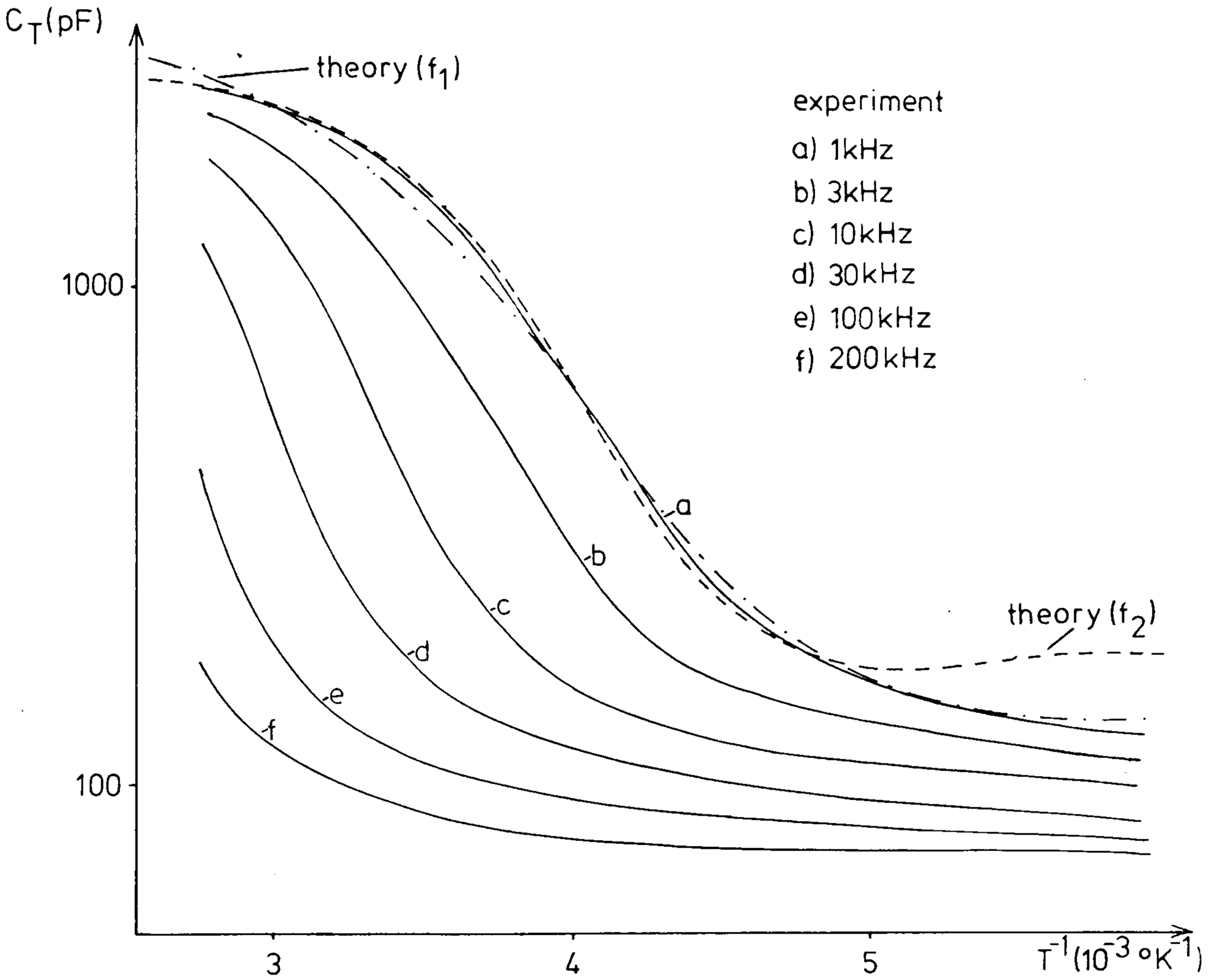
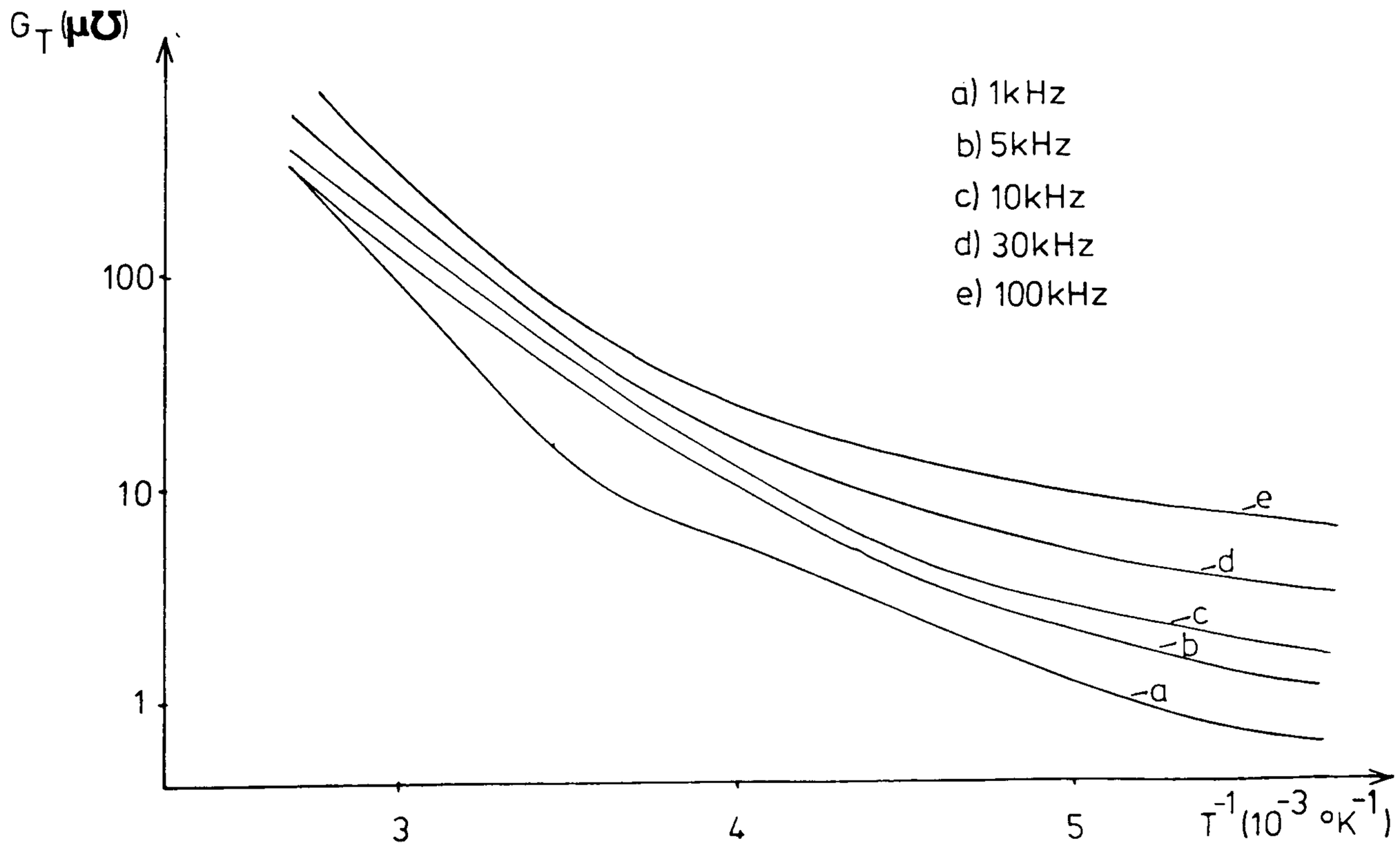


FIGURE 33

Virgin State Conductance versus Temperature



$$C_T(w_{low}) = \frac{C_1 + f(T)^2 C_2}{(1 + f(T))^2} \quad \ldots\ldots\ldots\ldots (10)$$

$$\text{where } f(T) = f_o \exp \frac{eE_o}{kT} = \frac{G_1(T)}{G_2(T)} \quad \ldots\ldots\ldots (11)$$

E_o and f_o are constants independent of temperature

e charge of an electron

k Boltzman's constant

T Absolute temperature

Equations 10 and 11 will give the familiar symmetrical characteristic. The ratio of conductances G_1 and G_2 thus has an exponential dependence on temperature.

It was found that although the trends described by the above equations follow those of the experimental results, there was not a detailed correspondence over the whole temperature range.

From Figure 33 two distinct temperature zones are observed. The device conductance has two distinct activation energies, one above and one below $T^{-1} = 3.5 \times 10^{-3}\ {}^{o}K^{-1}$. The low frequency conductance of the device is deduced from Equation 6.

$$G_T(w_{low}) = \frac{G_1 G_2}{G_1 + G_2} = \frac{f(T)}{1 + f(T)} G_2 \quad \ldots\ldots\ldots\ldots (12)$$

The trends observed in Figure 33 can be explained by G_1 and G_2 having different activation levels. This gives the same form for f(T) as Equation 11 where E_o is the difference between the two activation levels. An additional possibility is that if G_1 and G_2 have more than one activity level each, then f_o and E_o will have different values in the different temperature zones. Figure 33 suggests two temperature zones with a boundary at $3.5 \times 10^{-3}\ {}^{o}K^{-1}$.

Exploring this possibility it was found that

$$f_1(T^{-1} > 3.5 \times 10^{-3}\ {}^{o}K^{-1}) = 1.7 \times 10^{-3} \exp \frac{0.147}{kT}$$

$$f_2(T^{-1} < 3.5 \times 10^{-3}\ {}^{o}K^{-1}) = 5 \times 10^{-5} \exp \frac{0.217}{kT}$$

results in a very good correspondence over a large temperature range as shown in Figure 32.

Using these functions and $G_T(w_{low})$ with Equation 12, G_1 and G_2 may be found for the different temperature zones

For $T^{-1} > 3.5 \times 10^{-3}\ {}^{o}K^{-1}$

$$G_1 = 2 \times 10^{2} \exp \frac{-0.061}{kT}, \quad G_2 = 1.3 \times 10^{5} \exp \frac{-0.208}{kT}$$

For $T^{-1} < 3.5 \times 10^{-3}\ {}^{o}K^{-1}$

$$G_1 = 2 \times 10^{9} \exp \frac{-0.47}{kT}, \quad G_2 = 4 \times 10^{13} \exp \frac{-0.687}{kT}$$

This theory assumes that the temperature dependence of the capacitance parameters is negligible, but Figure 32 appears to indicate that in practice there exists a slow dependence.

At high frequencies $w_1(T)$, $w_2(T)$ and $w_3(T)$ result in complex temperature dependences for C_T and G_T.

ii) Discussion

The assumption that the temperature dependence of the device capacitance is purely the result of the temperature dependence of the conductances G_1 and G_2, gives a simple but accurate model which allows a close correspondence to the observed characteristics. The possible variation of the capacitances C_1 and C_2 with temperature has been assumed to be negligible, but the validity of this assumption now requires investigation.

The experimental capacitance characteristics show a strong

dependence on temperature, i.e. $C \alpha T^{6.1}$ at 230°K or $C \alpha \exp^{\frac{-0.188}{kT}}$ at 250°K.

Ideal junctions show a weak temperature dependence at such temperatures primarily through the dependence of the diffusion voltage. MIS devices[92] and junctions with deep impurities[90] can show an exponential dependence of capacitance on temperature, but neither shows the distinctive symmetrical characteristic observed, i.e. the capacitance of these devices shows a continued exponential decrease in capacitance as temperature decreases, whereas the observed characteristics show a rapid decrease in this dependence at low temperatures.

The capacitance of semi-conductor materials, which is proportional to the dielectric constant, is essentially independent of temperature except through the dependence of the relaxation time on conductance. The temperature dependence of the relaxation time will only result in a 50% reduction of capacitance, as the high frequency dielectric constant region is shifted to lower frequencies. The relaxation time is the product of the dielectric constant and the low frequency resistivity which will have an exponential dependence on temperature.

The device conductance shows a temperature dependence typical of semi-conductors and amorphous materials, i.e. several activation energy levels which are related to barriers[5] and impurity energy levels[5,91] within the device. From Figure 33 two energy levels are strongly indicated at 0.47 and 0.208 eV.

The model suggests that the total device conductance is the result of the two conductances G_1 and G_2 in series. Each conductance has at least two activation levels. From its high capacitance, Region 1 was deduced to be a junction, and from this analysis a barrier of 0.47eV is indicated.

The lower energy level, 0.06eV, may indicate the Gallium acceptor level in Germanium, which lies 0.011eV[93] above the Valence Band but the accuracy of the model approach must be in question for such subtle variations with temperature. CdS has a donor level as low as 0.03eV[19,91] or 0.04eV.[37] So there is no indication here whether the junction region is Germanium or CdS.

Region 2 is strongly suspected of being bulk CdS - discussed in the previous section. Activation levels at 0.208 and 0.687eV are deduced from the temperature analysis. However, mobility in CdS evaporated films is limited by grain boundary scattering which results in an activation level of 0.1 ± 0.01eV,[37,94] or stacking faults which result in an activation level of 0.038 ± 0.006eV.[31]

The conductance G_2 is a product of the mobility and the free carrier density, i.e. $G_2 = e\mu_n n$ for n-type CdS. This suggests that donor levels exist in the CdS at 0.11 and 0.59eV below the conduction band for the grain boundary scattering. The sulphur vacancy in CdS produces a donor level at 0.12eV which approximately corresponds to the shallow donor level.

From their relative contributions to the free electron density as described by

$$G_2 = 4 \times 10^{13} \exp -\frac{0.687}{kT} + 1.3 \times 10^{5} \exp -\frac{0.208}{kT} \quad \ldots\ldots (13)$$

the 0.59eV donor level can be deduced to have an effective density of the order of 10^8 greater than the 0.11eV donor level. The true density of the donor levels will be considerably affected by the existence of ionised acceptor levels within the CdS.

If we assume that N_A is the density of acceptor states and that they lie far below the fermi level, then a fixed negative space charge of N_A^- will result. The total fixed positive space charge will be the sum of the ionised donor levels at 0.11 and 0.59eV. The shallow donor level, N_{DS}, will be fully ionised as it lies far above the fermi level. The deep donor has N_{DD}^+ ionised donor levels[95] which are determined by the position of the fermi level.

$$N_{DD}^+ = N_{DD}\left(1 - \left(1 + 0.5\exp\frac{E_{DD} - E_F}{kT}\right)^{-1}\right) \quad \ldots\ldots\ldots\ldots (14)$$

where N_{DD} is the total density of deep donor energy states

E_{DD} and E_F are the deep donor and fermi energy levels

Space charge neutrality requires that the free electron density, n, equals the difference between the positive and negative space charges

$$n = N_{DD}^+ + N_{DS}^+ - N_A^-$$

When the fermi level is close to the deep donor level at high temperatures $n \simeq N_{DD}^+$, i.e. the free electron density is approximately equal to the density of ionised deep donor levels, as suggested by Equation 13.

If the fermi level rises due to a reduction of temperature then the deep donor level becomes totally neutralised and

$n \simeq N_{DS}^{+} - N_{A}^{-}$, i.e. the free electron density is determined by the difference between the shallow ionised donor and ionised acceptor densities.

Even though the effective density at the shallow donor levels may be of the order of 10^{8} less than at the deep donor levels, the shallow level may be strongly compensated by the acceptor levels and have a high density.

At room temperature free electron densities of between 1.2×10^{11} and $7 \times 10^{12} cm^{-3}$ were indicated from the conductivity of the CdS. From Equation 13 we find that $n \simeq N_{DD}^{+}$ at room temperature and, by the insertion of the fermi levels and free electron densities into Equation 14, the total density of deep donor states may be found to be between 2×10^{13} and $6 \times 10^{16} cm^{-3}$. The effective shallow donor density from Equation 13 is 10^{8} less than the deep donor states, i.e. between 2×10^{5} and $6 \times 10^{8} cm^{-3}$.

(When the stacking fault activation level is used rather than the assumed grain boundary barrier these densities are increased by a factor of 10)

The deep level need not be a donor level - an acceptor level at 0.59eV will also give a temperature dependence as described by Equation 13. At room temperature the acceptors at this level will be partially ionised and their density can be calculated in a similar manner to the deep donor level case to have a density of between 2×10^{13} and $6 \times 10^{16} cm^{-3}$. The negative space charge of the deep acceptor will be more than fully compensated by the positive effective shallow donor space charge. The shallow donor density in this case will be far in excess of the density required for the deep donor case. In

fact the density will be of a similar order of magnitude to the density of deep acceptor states.

7.34 Capacitance, conductance dependence on bias voltage

i) Measurements and model

In the previous sections the device was tested at zero bias, but in this section the capacitance and conductance variation with bias is studied.

From the previous sections it appears likely that the two dominating regions of the device are a junction and bulk CdS. If we continue the analysis based on this model we should find that the junction region is strongly dependent on bias and that in comparison the bulk CdS is independent of bias.

Figures 34 and 35 show the capacitance and conductance response of a device over a range of biases and frequencies. From the capacitance and conductance dependence at zero bias, using the analysis technique of Section 7.32, the parameters are estimated to be

$$C_J(V_T = 0) = 700pF \qquad G_J(V_T = 0) = 4.6\,\mu\mho$$

$$C_B(V_T = 0) = 50pF \qquad G_B(V_T = 0) = 34\ \mu\mho$$

The suffixes J and B are used to represent the junction and bulk CdS regions (previously referred to as Regions 1 and 2) respectively. V_T is the total bias over the device, and V_B and V_J are the biases associated with regions B and J ($V_T = V_B + V_J$).

FIGURE 34

Virgin State Capacitance versus Device Bias

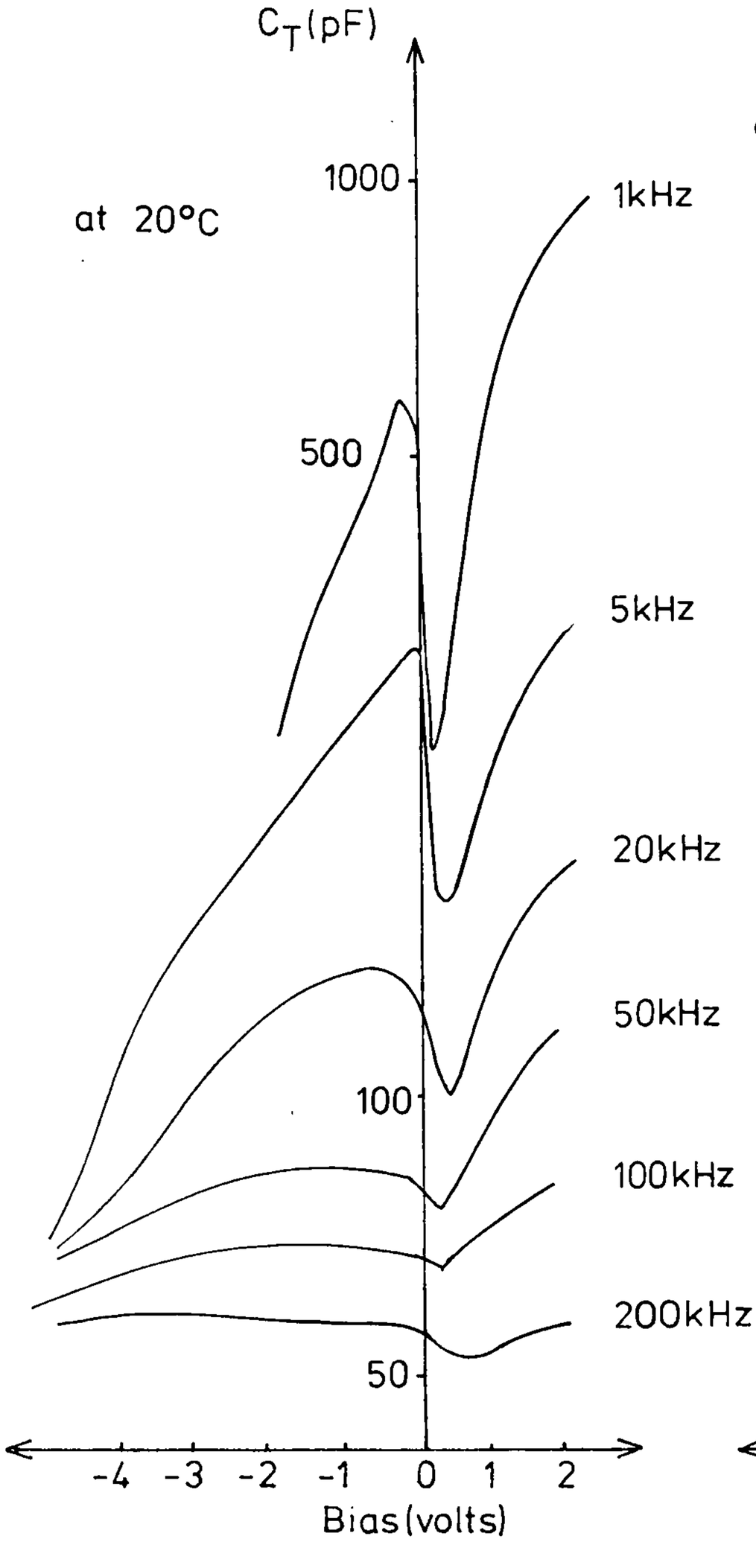
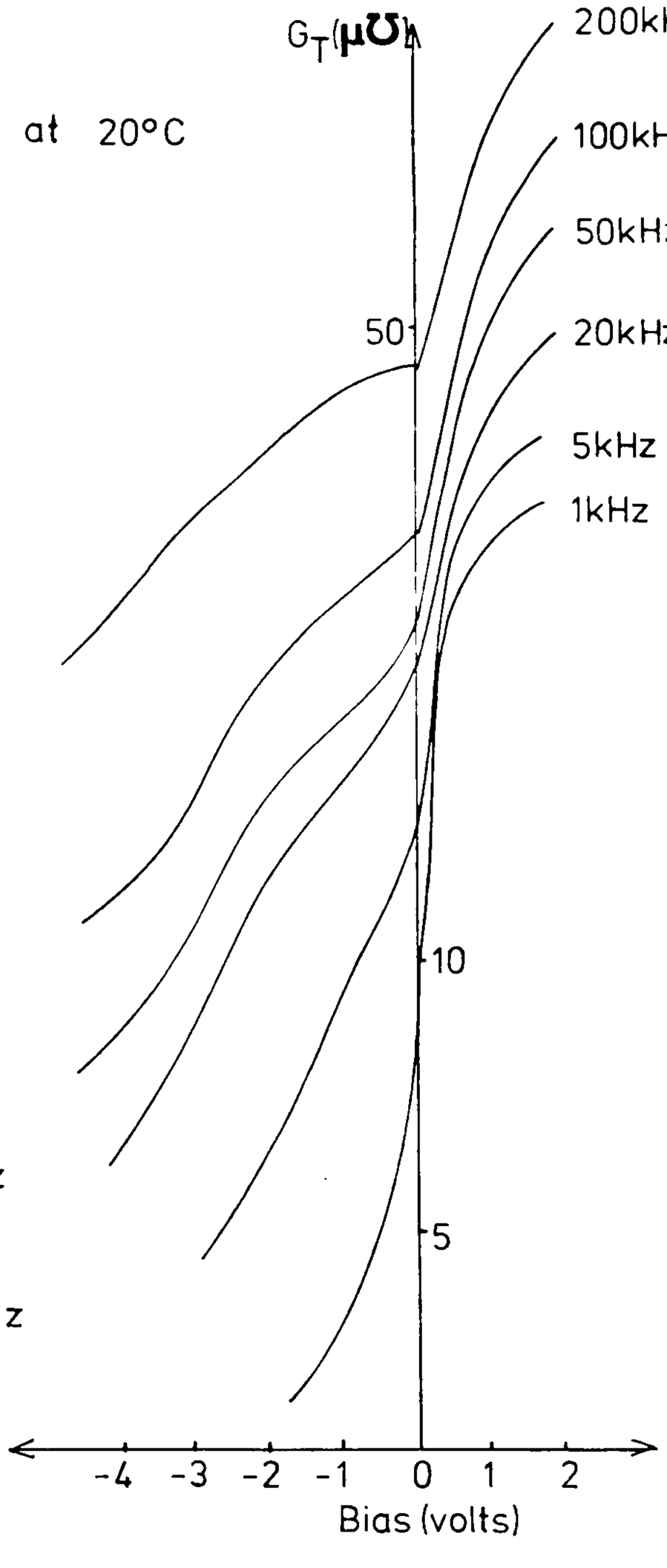


FIGURE 35

Virgin State Conductance versus Device Bias



The full equations which govern the responses are

$$C_T(V_T) = \frac{(w/w_3(V_T))^2 + 1}{(w/w_2(V_T))^2 + 1} \cdot \frac{C_J(V_T) + f^2(V_T)C_B(V_T)}{(1 + f(V_T))^2} \quad \ldots (15)$$

$$G_T(V_T) = \frac{(w/w_1(V_T))^2 + 1}{(w/w_2(V_T))^2 + 1} \cdot \frac{G_J(V_T)G_B(V_T)}{G_J(V_T)+G_B(V_T)} \quad \ldots\ldots\ldots (16)$$

$$\text{where } f(V_T) = \frac{G_J(V_T)}{G_B(V_T)}$$

Region B is assumed to be bulk CdS so $G_B(V_T) = 34\,\mu\mho$ and $C_B(V_T) = 50pF$ are independent of bias. All parameters will continue to be assumed independent of frequency.

Equations 15 and 16 can be greatly simplified if the frequency is assumed low, i.e. w_{low} is much less than $w_1(V_T)$. This allows simplification to

$$C_T(V_T, w_{low}) = \frac{C_J(V_T) + f^2(V_T)C_B}{(1 + f(V_T))^2} \quad \ldots\ldots\ldots\ldots (17)$$

$$G_T(V_T, w_{low}) = \frac{G_J(V_T)G_B}{G_J(V_T)+G_B} \quad \ldots\ldots\ldots\ldots\ldots\ldots (18)$$

The 1kHz responses, which are the lowest available*, will be taken to represent $G_T(w_{low})$ and $C_T(w_{low})$ and thus the d.c. or 0 Hz conductance and capacitance of the device.

(N.B. Conductance refers to the small signal conductance $G = \frac{dI}{dV}$, where I is the device current. Thus at any bias a small change of bias, dV, will result in a small change in current dI.)

$G_T(w_{low})$ is a known function of V_T from the experiment. Applying Equation 18, $G_J(V_T)$ can be calculated, as G_B is also

* At lower frequencies current creep effects are in evidence.

known. With $G_J(V_T)$, $f(V_T)$ can be calculated, and when $f(V_T)$ is inserted into Equation 17 the capacitance of the junction is found as a function of the total device bias, i.e. $C_J(V_T)$.

Both the conductance and the capacitance of the junction need now to be expressed as functions of the junction bias V_J.

Numerically integrating $G_T(w_{low})$ with respect to V_T gives the device current $I_T(V_T)$. The junction bias is the total device bias less the bulk CdS bias

$$V_J = V_T - V_B \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (19)$$

$$\text{where } V_B = \frac{I_T(V_T)}{G_B}$$

Thus V_J and V_B can be calculated as functions of V_T. Using $V_J(V_T)$ allows $C_J(V_J)$, $G_J(V_J)$ and $I_J(V_J)$ to be calculated.

Figure 36 shows the deduced $I(V_J)$ versus V_J characteristic and indicates the expected rectifying trend with the "easy" direction forward bias. Figure 37 shows the forward bias of the junction, log $I(V_J)$ versus V_J, and indicates the relationship

$$I = I_S(\exp \frac{eV_J}{\eta kT} - 1) \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (20)$$

$$\text{where } I_S = 0.27\mu A$$
$$\eta = 2.72$$

At voltages in excess of $V_J = 0.3V$ the characteristic becomes very sensitive to the value selected and used for G_B in Equation 19, e.g. a 3% change in G_B at 0.33V will result in a 35% change in G_J. As G_B can only be estimated, little can be deduced in this voltage range.

FIGURE 36

Deduced "Junction" Current-Voltage Characteristic

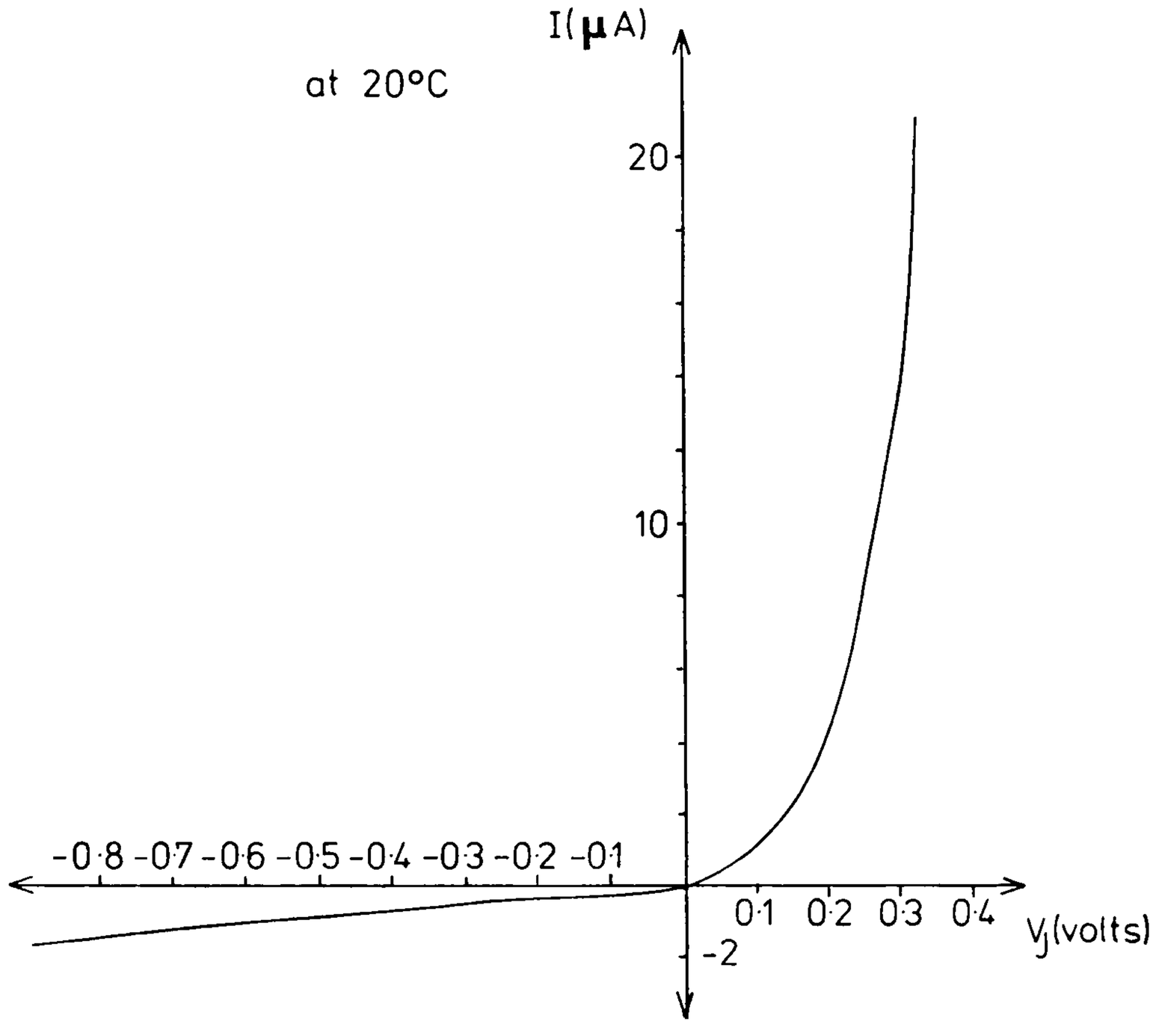
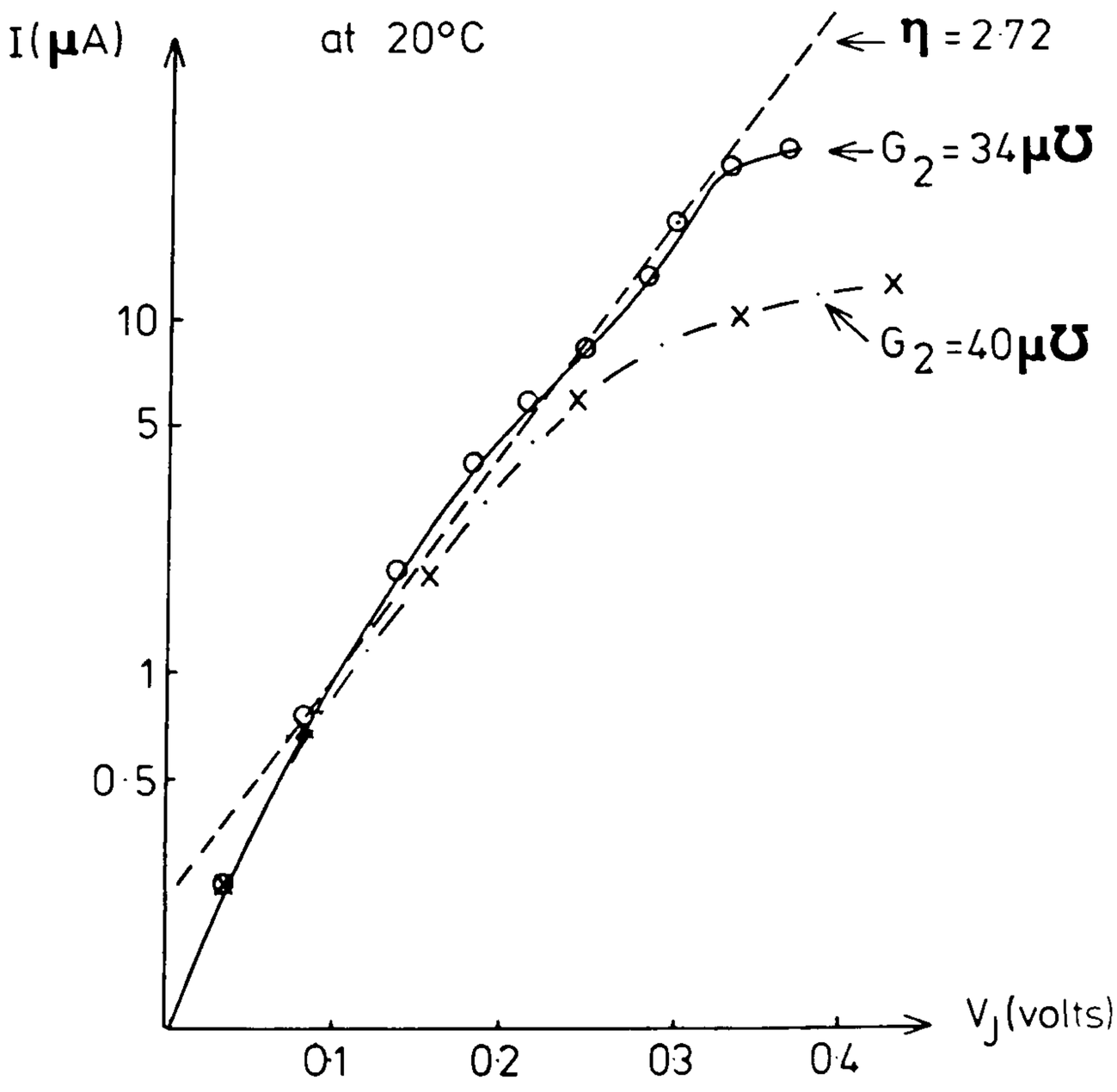


FIGURE 37

Log (Current) versus Deduced "Junction" Voltage Characteristic



The factor η, which is between 2 and 4 for Germanium point contact and Gallium Arsenide p - n junctions,[96,97] tends to unity for Germanium diffused p - n junctions. The deviations from the ideal, $\eta = 1$, are possibly the result of recombination in the junction transition region[96] or recombination by interface states.[76]

Figure 38 shows the deduced plot of $(C_J(V_J))^{-2}$ versus V_J. The strong reverse bias trend indicates an abrupt junction which obeys

$$C_J = \left(\frac{e \epsilon N_o}{2(V_D - \frac{kT}{e} - V_J)} \right)^{\frac{1}{2}}$$

where V_D = 0.6V, the junction diffusion potential

N_o = $4.5 \times 10^{17} cm^{-3}$, the junction doping density

and ϵ is the permittivity of the medium

The forward bias capacitance shows a curious anomaly, viz., the "spike" at low bias. This "spike" appears to be a result of some inaccuracy in the series of assumptions that have been made, particularly the selection of the value for G_B. It will be shown that this spike is not an essential feature in producing the observed experimental characteristics.

The general trend of the forward bias characteristic is rapid increase in capacitance up to 0.2V and then a continual slower increase to capacitances of the order of nF. If the slope of the characteristic is assumed to be due solely to a spatial variation in the doping, i.e. $N_o(x)$, then

$$\frac{dC^{-2}}{dV_J} = \frac{2}{e \epsilon N_o(x)}$$

FIGURE 38

Deduced "Junction" Capacitance versus Bias

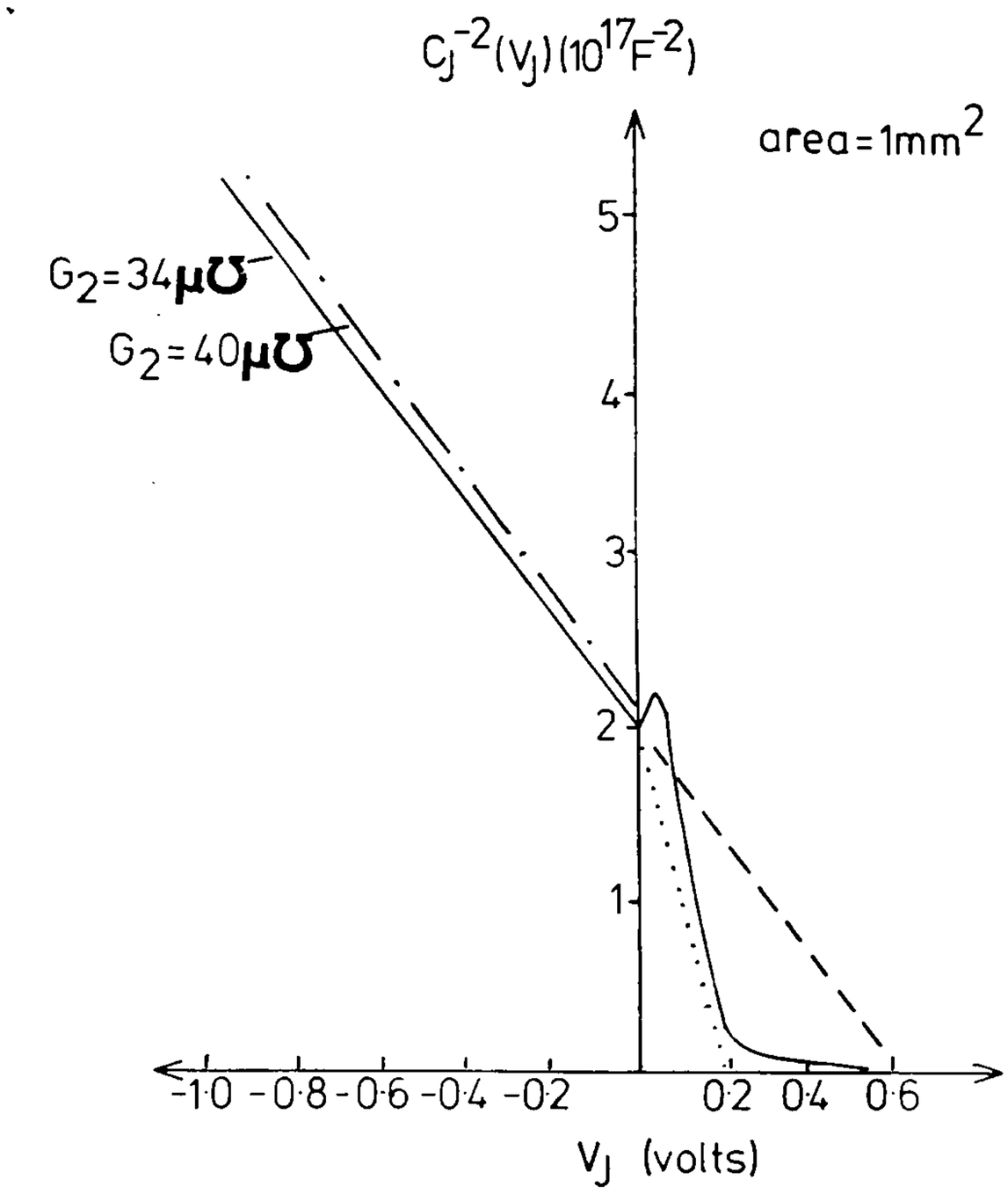
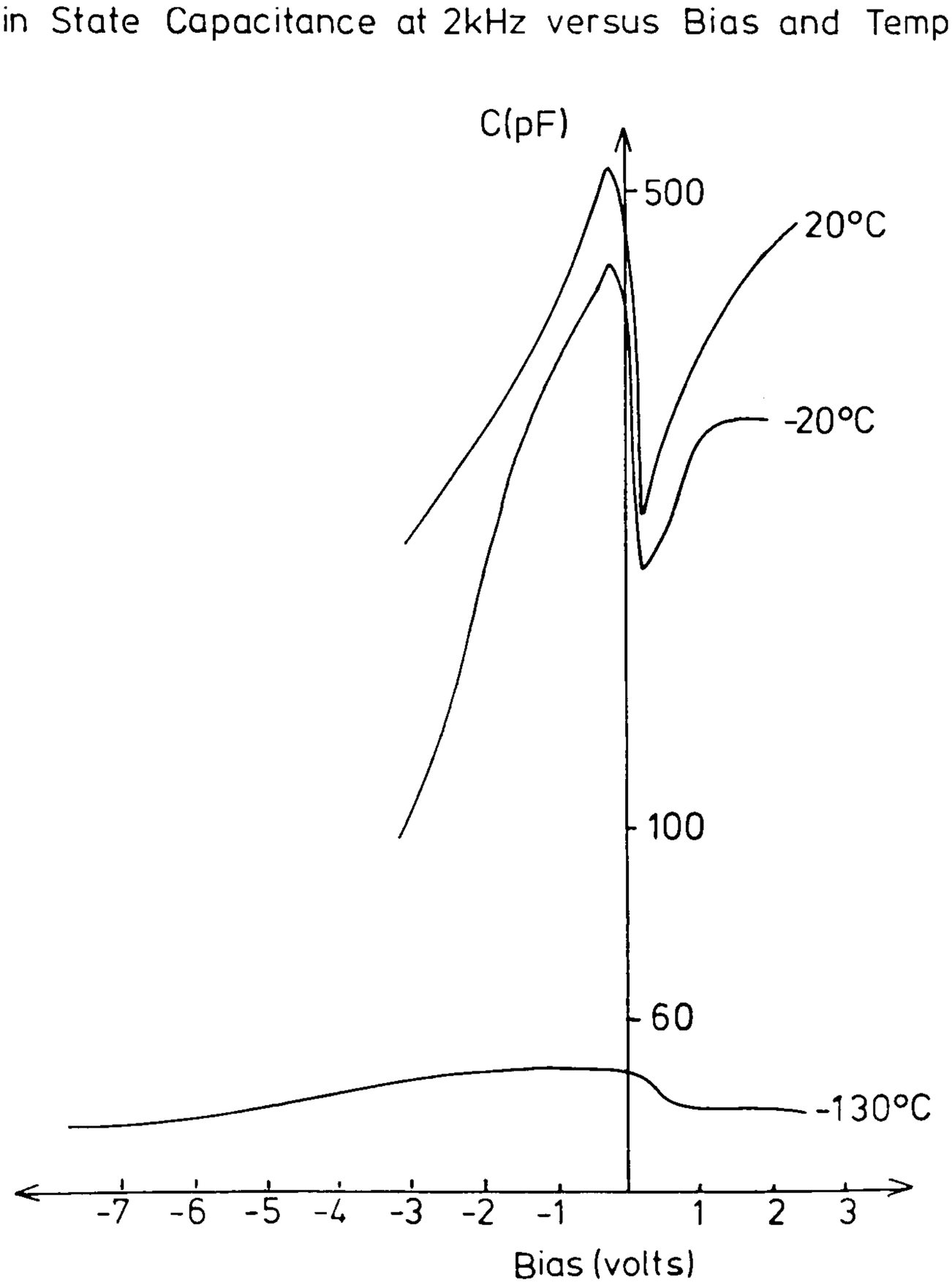


FIGURE 39

Virgin State Capacitance at 2kHz versus Bias and Temperature



The doping in the vicinity of the junction is not constant and is less than the bulk semi-conductor doping.

In Appendix III the capacitance of a junction with two doping regions is deduced to be

$$C = \left(\frac{e \epsilon N_b}{2}\right)^{\frac{1}{2}} \left(V_D - V + \frac{e x_a^2}{2\epsilon} (N_b - N_a)\right)^{-\frac{1}{2}} \quad \ldots\ldots\ldots (22)$$

where N_a is the doping density near the interface
N_b is the doping density further from the interface
and x_a is the depth of the N_a region

The intercept $C^{-2} = 0$ on the C^{-2} versus V characteristic occurs at V_I. Thus the diffusion voltage

$$V_D = V_I + \frac{e x_a^2}{2\epsilon} (N_a - N_b)$$

The slope of the deduced Figure 38 indicates that N_b is greater than N_a and this implies that the diffusion voltage will be less than the intercept voltage V_I, which equals 0.6V.

Figure 39 shows the temperature and bias dependence of $C(w_{low})$. At low temperature the voltage dependence of the device capacitance is considerably reduced - which is to be expected from consideration of Equation 17. As temperature decreases, $f(V_T)$ increases exponentially and Equation 17 simplifies to

$$C_T(w_{low}, T_{low}) = C_B(T_{low})$$

$$\text{when } \frac{C_J}{C_B} \ll f^2(V_T)$$

The capacitance characteristic at $-130^{\circ}C$ is likely to be purely a result of a voltage dependence of C_B. Figure 32 shows that

below $-90^{\circ}C$ the contribution of C_J to C_T is negligible. The variation of C_B with bias is small, only a 10% reduction in forward and reverse bias being observed.

ii) Discussion

The parameters C_B and G_B were deduced from the frequency dependence of the device at zero bias and were used throughout the analysis. The frequency and bias independence of these parameters was assumed, but the sensitivity of the results to small variations in these parameters indicates a need for investigation. The parameter C_B has little affect on the analysis except at large reverse biases where $C_J \ll C_B$, which is outside the experimental range of bias. But the parameter G_B, which was deduced to be $34\,\mu\mho$, could have a profound effect on the results.

If G_B is assumed to be as large as $40\,\mu\mho$, the deduced dependence of junction capacitance on bias is little affected. As shown in Figure 38, the slope of the reverse bias characteristic is virtually unaffected by attributing a value of $40\,\mu\mho$. The junction conductance is however considerably affected by the selection of this value for G_B - as shown in Figure 37.

The conductance at biases in excess of +0.2V deviates below the straight line approximation of Equation 20, but at lower biases the same trend is observed. It can be shown therefore that the deduced characteristics of the junction are modified by G_B to a small degree at values at least between $34\,\mu\mho$ and $40\,\mu\mho$, but the fundamental trends described by Figures 38 and 37 and Equations 20 and 21 remain valid.

Figure 40 shows a comparison between the experimental

characteristic at 1kHz and two theoretical curves based on models approximating to the results of the previous chapter.

The first and simplest model assumes that the junction is ideal and that Equations 20 and 21 which determine the capacitance and conductance of the junction with respect to bias, are strictly followed. The broken lines in Figures 37 and 38 show the assumed dependences. Under reverse bias a good correspondence is observed for the w_{low} curve, but under forward bias the "slot" or "valley" at 0.3V is not in evidence and the capacitance shows a decrease towards 50pF, which is contrary to the experiment. From Equation 17 with $f(V_T)$ increasing rapidly under forward bias, $C_J(V_T)$ must also be increasing rapidly with forward bias to result in the observed increase in device capacitance.

The second model is identical to the first except that it assumes a more rapid increase in capacitance for the forward bias junction than in the ideal case. The dotted line of Figure 38 shows the assumed dependence. The reverse bias correspondence of this model is identical to the first model and the forward bias characteristic shows the "slot" at the correct value of bias. The w_{low} theoretical curve continues to increase with increasing forward bias, which follows the experimental trend.

It should be noted that the junction is at extreme forward bias at such device biases and both the conductance and capacitance will be increasing rapidly as V_J approaches V_D - which is less than 0.6V. The greater part of V_T will be dropped over the bulk CdS, and increasing the device voltage will only result in a very small increase in V_J as $R_B \gg R_J$, i.e. the resistance of

the bulk CdS is very much greater than the resistance of the junction.

It should be noted that the anomalous "spike" in the deduced capacitance dependence, Figure 38, has been shown to be not an essential ingredient; ignoring the "spike" results in the same trend as the experiment.

Figure 40 also shows the high frequency experimental curve $C_T(200kHz)$ and the theoretical curve $C_T(w_{high})$. The theoretical high frequency curve is only dependent on C_J and C_B as $C_T(w_{high}) = \frac{C_J C_B}{C_J+C_B}$ and shows only a small variation with bias, C_J being much larger than C_B, which is independent of voltage.

Figure 40 provides a comparison between the 5kHz theoretical and experimental characteristics and considerable divergence is apparent even though the low and high frequency characteristics show good correspondence.

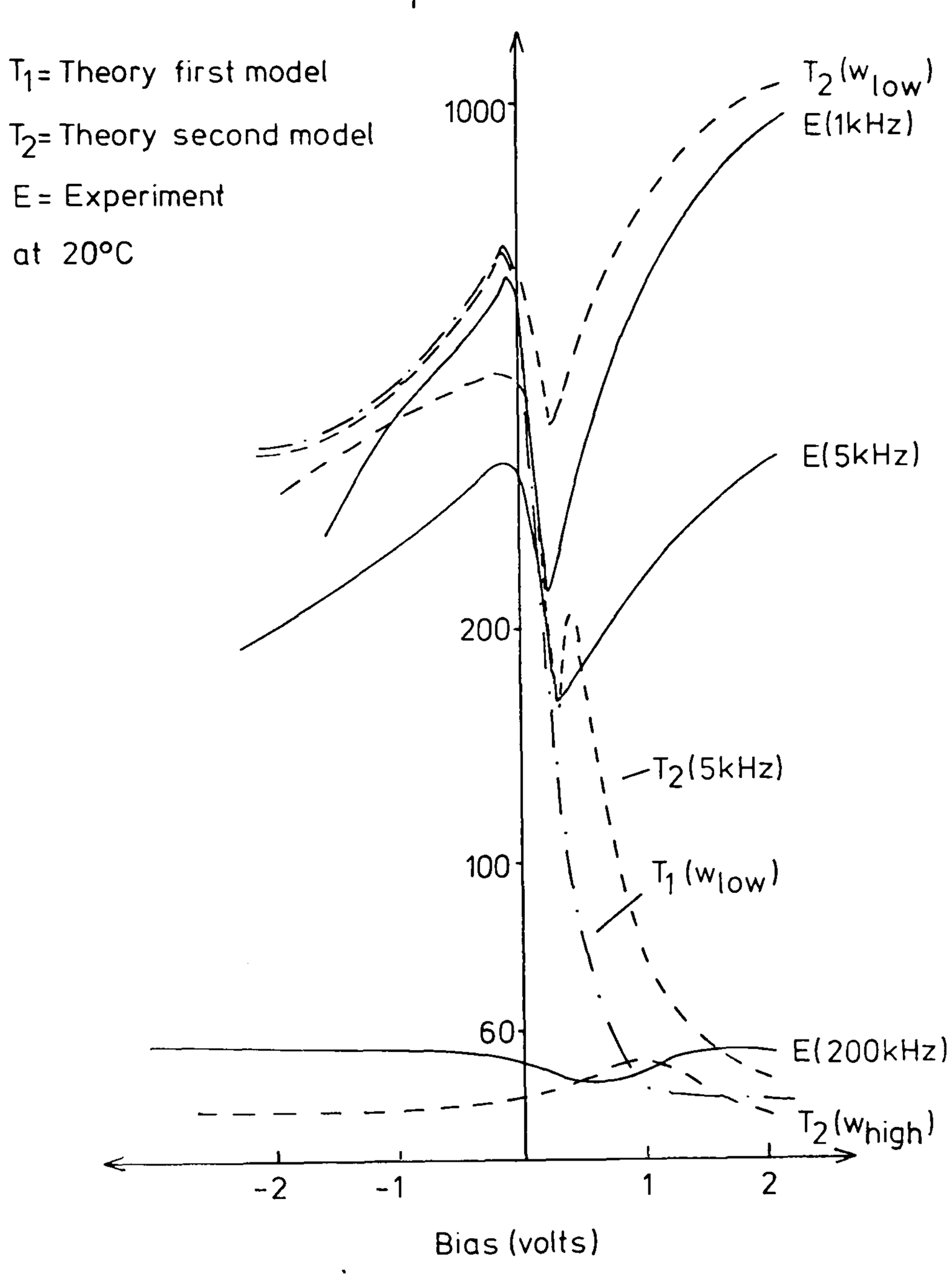
The characteristic frequencies w_1, w_2 and w_3 which determine the frequency response of the device at frequencies between w_{low} and w_{high}, are dependent on the bias of the device through the dependence of parameters - the equations appear in Appendix I. A fundamental assumption of the analysis was that the $C_T(1kHz)$ and $G_T(1kHz)$ experimental characteristics can be used to represent $C_T(w_{low})$ and $G_T(w_{low})$, but this will only be true if 6.28×10^3 rad/s (1kHz) is less than w_1.

Using the calculated and assumed parameters it is possible to calculate w_1, w_2 and w_3 as functions of bias. For low biases 6.28×10^3 rad/s is less than w_1 but at larger biases, and

FIGURE 40

Comparison of Experimental and Theoretical

Virgin State Capacitance versus Bias characteristics



particularly forward biases greater than 0.7V, this is not the case. The implication is that C_T(1kHz) and G_T(1kHz) should not be used to represent $C_T(w_{low})$ and $G_T(w_{low})$ for these biases. Lower frequency experimental curves should be used, but these are prohibited by current creep effects. It follows from this discovery that the forward bias characteristics of the junction above 0.3V must be discounted.

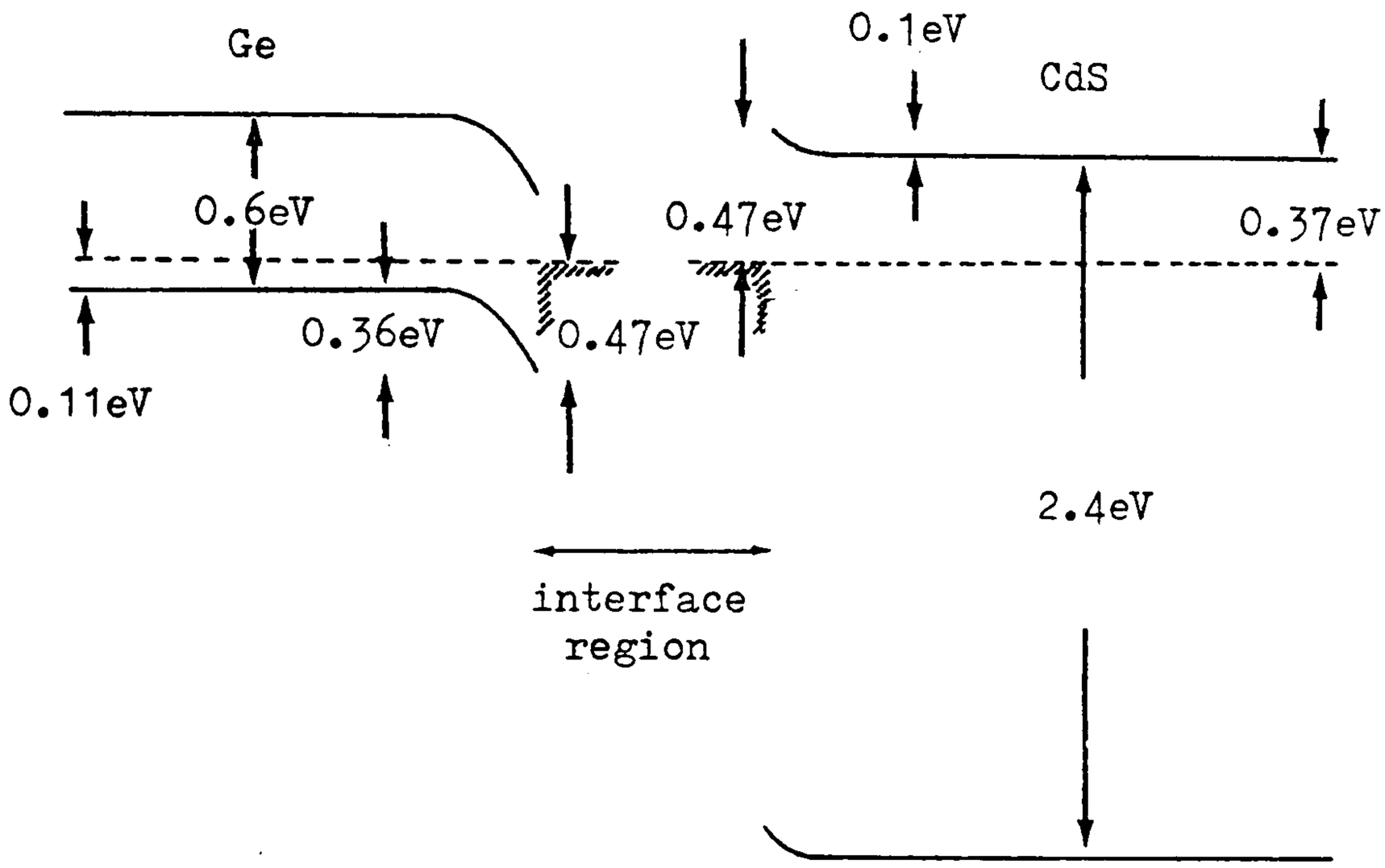
Although the previous sections identify Region 2 as bulk CdS, Region 1 has only been discovered to be a junction - but at this stage it is unidentified. From the preceding analysis the location of this junction can now be identified.

Two possible locations exist giving a result having the correct rectifying polarity. One is between the Germanium and the heterojunction interface, and the other between the heterojunction interface and the CdS. Both would result in the "easy" direction of current flow under forward bias. Interface states, which exist between the two semi-conductor materials of a heterojunction, can dominate the energy band structure of the junction.[80,81,83,84] For example a high density of acceptor type interface states within the energy band gap of an n - type semi-conductor will result in a rectifying junction irrespective of the work function of the other semi-conductor in the heterojunction.[81,85] Depending on the type, energy, and density of the interface states, the energy bands of the Germanium and CdS can provide either ohmic or rectifying junctions.

From the previous sections the fermi level of the CdS was discovered to be between 0.37 and 0.47eV below the Conduction

Band. The fermi level in Germanium with nominally $10^{17}cm^{-3}$ doping is 0.11eV above the Valence Band.

The barrier from the interface region,[94] assumed to be a quasi-metal in this exercise,[81,85] to the semi-conductor is 0.47eV from the temperature dependence of device conductance at zero bias, and the diffusion voltage barrier from the semi-conductor to the interface region is less than 0.6eV from the capacitance dependence on bias. The diagrams below show two types of junction possible.



It can clearly be seen from these two diagrams that $V_D(Ge) = 0.36eV$, or $V_D(CdS) = 0.1eV$ or less. If the barrier within the CdS is as low as 0.1eV then under a small forward bias the junction will become ohmic. From the continuous exponential increase shown in Figure 36, this clearly is not the case. Furthermore, from the capacitance dependence on bias - Figure 38 - the doping density was deduced to be $\simeq 4 \times 10^{16}cm^{-3}$. This doping density far exceeds the average effective density calculated for CdS - the deep donor level not being exposed by the 0.47eV barrier.

The rectifying junction is thus deduced to be between the Germanium and the interface region - the 4 x $10^{16}cm^{-3}$ doping density deduced from Figure 38 being consistent with a nominal $10^{17}cm^{-3}$ acceptor doping of the Germanium.

7.40 THE OFF STATE

Using the extensive knowledge of the device gained in the previous section, the OFF state can now be investigated. The OFF state is either a result of forming the virgin device or of switching the device from the ON state.

7.41 Outline of the device characteristics in the OFF state

Figure 41 shows a typical log(Current) versus log(Voltage) characteristic for the device in its three distinct states - virgin, OFF and ON.

In its OFF state the device has a much more stable low frequency characteristic and does not suffer from the "current creep" effects which were so prevalent in the virgin state. The conductance of the device is much greater than in the virgin state at all frequencies - typically by a factor of ten. The frequency dispersion of capacitance is still strong and results in lower capacitances over the frequency range.

7.42 Capacitance and conductance dependence on frequency

Figure 42 shows both the capacitance and conductance dependence on frequency of the device in the virgin and OFF states. Using the analysis of Section 7.32 the virgin state parameters are calculated to be

$$G_J = 60\ \mu\mho\ ,\quad C_J = 5nF\ ,\quad G_B = 100\ \mu\mho\ ,\quad C_B = 50pF$$

FIGURE 41

Log (Current) versus Log (Voltage) for Virgin, OFF and ON states

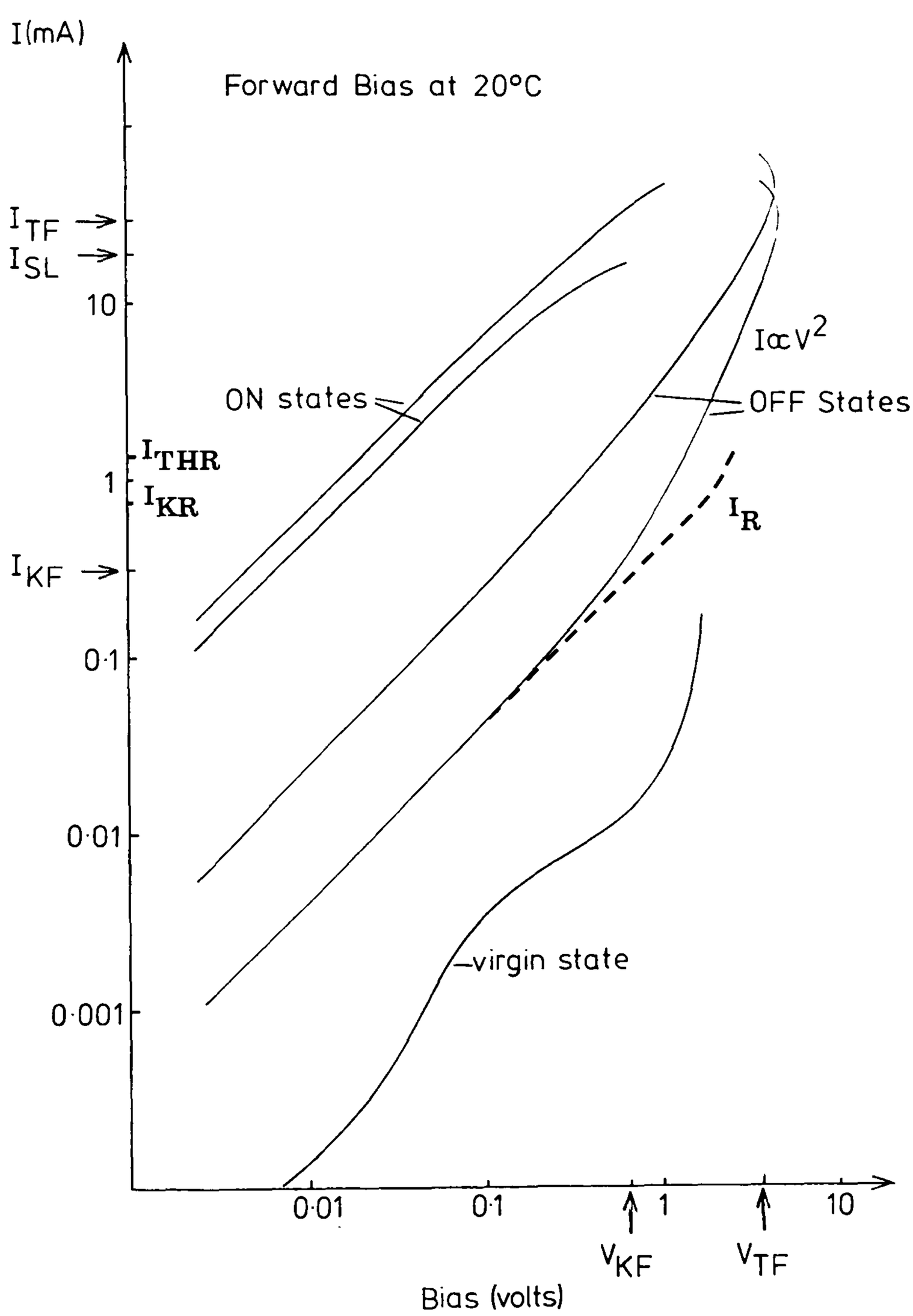
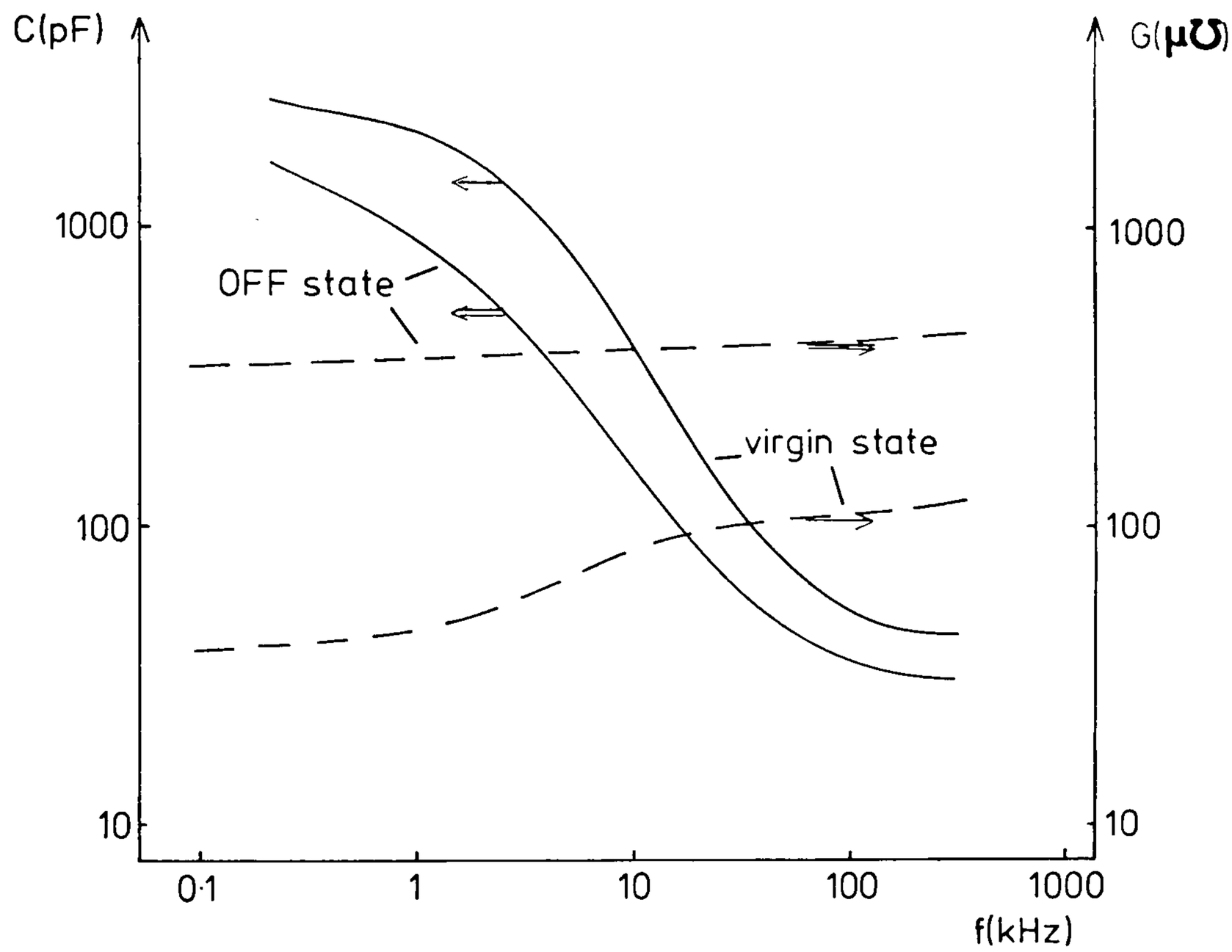


FIGURE 42

Comparison of virgin and OFF state Capacitance
and Conductance versus Frequency Characteristics



The OFF state, which shows a similar trend, has parameters

$$G_1 = 2800\ \mu\text{℧}\ ,\quad C_1 = 100\text{nF}\ ,\quad G_2 = 400\ \mu\text{℧}\ ,\quad C_2 = 40\text{pF}\pm 10\text{pF}^{*}$$

From this experiment alone it can be seen that both the "junction" and "bulk CdS" regions of the device have been affected by forming. The conductance of the device increases considerably with forming and the capacitance decreases at low frequencies.

Region 1 is suspected of being the remains of the "junction" region as the bulk CdS cannot support capicitances as high as 100nF. Region 2 appears to be the bulk CdS as before - the capacitance has remained essentially the same but the conductance has increased by a factor of 4. The increase in conductance of the bulk CdS may be due to recrystallisation of low conductivity sections of the film. The CdS up to 0.2 μm from the substrate interface is likely to have low conductivity due to the high level of disorder in this region. Conductivities in the rest of the film can be of the order of 10^4 higher than in this disordered region.[5,35] Even though the conductance of the bulk CdS region is affected by forming, the capacitance remains the same as the permittivity and geometry are essentially unaffected.

Cycle switching of the device can result in OFF states with similar trends but different in quantitative terms. Thus if G_{TA} is less than G_{TB} at low frequencies then the low frequency device capacitances relating to these states are found to be

*Measurement of low capacitance when the device conductance is greater than 111 μ℧ results in this uncertainty.

$$C_{TA}(w_{low}) < C_{TB}(w_{low})$$

but the high frequency device capacitances are

$$C_{TA}(w_{high}) \simeq C_{TB}(w_{high})$$

These trends may be understood by considering the relative magnitudes of the parameters and simplifications of the major equations. The total device capacitances can be expressed as

$$C_T(w_{high}) = C_2 \text{ as } C_1 >> C_2$$

$$\text{and } C_T(w_{low}) = \left(\frac{G_2}{G_1+G_2}\right)^2 C_1 \text{ as } G_1^2 C_2 << G_2^2 C_1$$

Even if C_1 and G_1 are unaffected by the change of OFF state, the observed trends can be explained by

$G_{2A} < G_{2B}$ where G_{2A} is the G_2 parameter of OFF state A
and G_{2B} is the G_2 parameter of OFF state B

and this is consistent with the total conductances G_{TA} being less than G_{TB}, as $G_T(w_{low})$ approximates to G_2. Modifications of G_2 could be a result of partial recrystallisation of the CdS film. Suitable changes in C_1 can also result in the observed trend but a variation of G_1 cannot result in an increase of device capacitance and conductance as observed.

In the OFF state the application of white light has the same effect as increasing the device temperature, i.e. $C_T(w_{low})$ increases but $C_T(w_{high})$ remains essentially the same. These trends can again be explained by the increase in G_2, the conductance of the CdS film, because of its sensitivity to light[98] and heat.[66,91] Indeed the indications are that the device continues to be sensitive to light even when the current flow is over less than the whole area of the device because of recrystallation.

7.43 Current - voltage characteristics

i) Measurement

Figure 41 shows typical OFF state characteristics when a 50Hz sine wave is applied to the device. The basic device characteristics show clear trends.

a) Ohmic conduction region - for both low forward and reverse biases

$$I \alpha V^1, \quad \begin{matrix} I(V + ve) < I_{KF} \\ I(V - ve) > I_{KR} \end{matrix}$$

b) Square law conduction region - normally only observed in forward biases

$$I \alpha V^2, \quad I_{KF} < I(V + ve) < I_{SL}$$

c) Superlinear conduction region - observed in high forward and reverse biases

$$I \alpha V^n, \quad \begin{matrix} I_{SL} < I(V + ve) < I_{TF} \text{ , } n > 2 \\ I_{KR} > I(V - ve) > I_{THR}, \; n > 1 \end{matrix}$$

(Under both forward and reverse biases n increases with the applied bias, $|V|$, but not rapid enough for an exponential dependence)

Approximately 1 in 5 evaporations resulted in devices that show a region $I \alpha V^n$ where n is a constant with respect to voltage and lies between 3 and 4.5.

d) Differential negative resistance region - normally only observed in the forward bias

$$I \alpha V^{-n}, \quad I(V + ve) > I_{TF} \text{ , } n > 0$$

(Under reverse bias the device tends to switch to the ON state, but for sufficiently high frequency applied voltage a negative resistance region in the reverse bias can be observed)

e) Forward bias conductance is greater or equal to the reverse bias conductance at any specific value of bias

$$\frac{dI(V + ve)}{dV} \geq \frac{dI(V - ve)}{dV}$$

Although the virgin state conductance is directly proportional to the device area, the formed state conductance is not related to the device area and devices with identical areas can form to different conductance states.

The table below shows the dependence of the characteristic parameters on temperature, light intensity and G_a, where G_a is the zero bias conductance of the device at ambient temperature and incident light. G_o is the zero bias device conductance when the temperature is non-ambient or the light level is greater than incident.

Parameter	Increasing white light intensity	Increasing temperature	Increasing G_a
G_o	Increases	Increases	x
V_{KF}	Increases slightly	Decreases	Increases
V_{TF}	Decreases slightly	Decreases	Decreases slightly

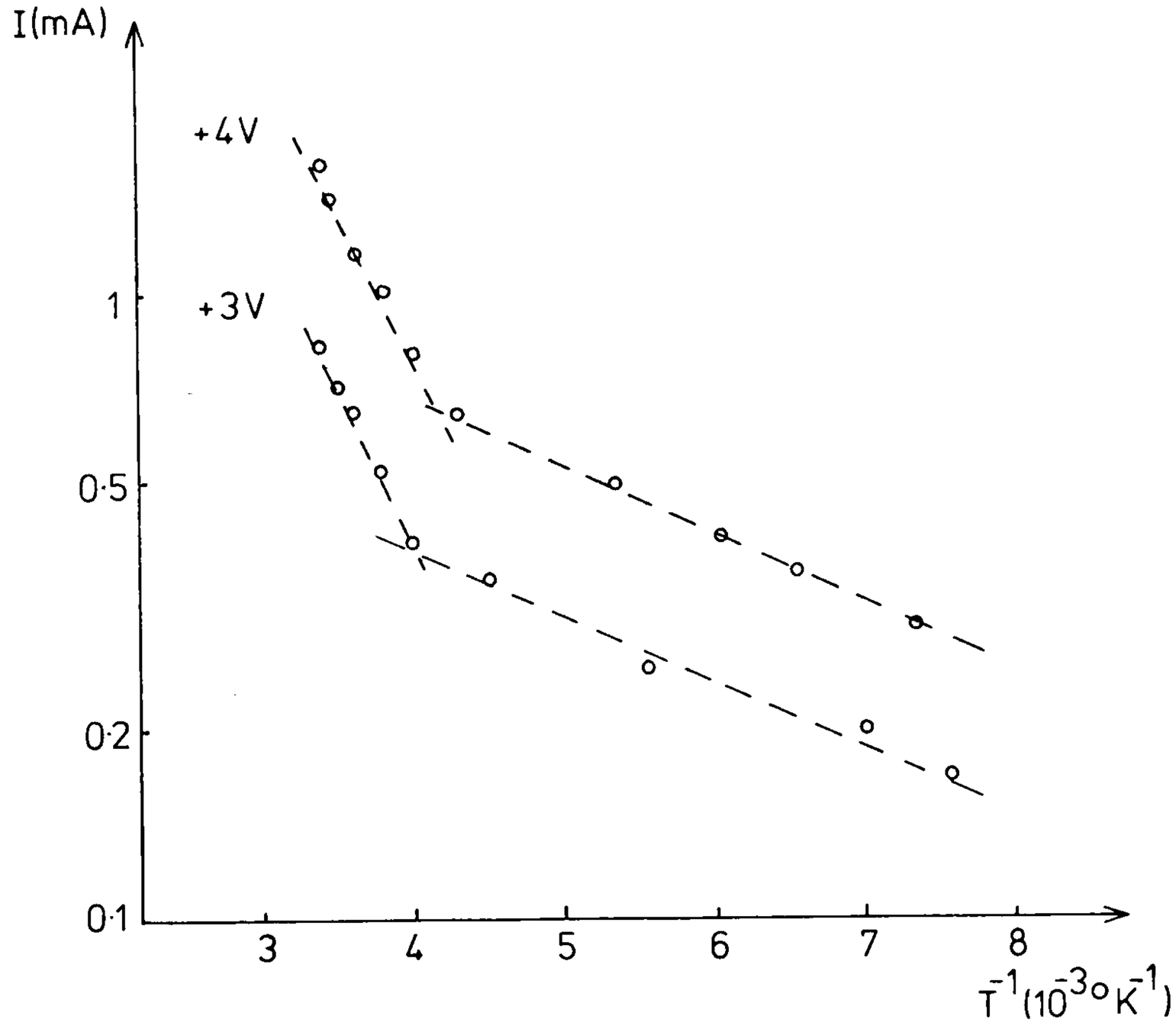
Figure 43 shows the temperature dependence of device conductance under 3 and 4V forward bias. Two activation levels are observed - 0.126 and 0.015eV. These represent conduction in the ohmic region as V_{KF} increases so rapidly with decreasing temperature that it significantly exceeds 4 volts, and the experiment bias then falls outside the square law region. Increasing temperature seems to result in some recrystallisation as step changes in conductance occur.

ii) Discussion

The forward bias characteristics are typical of thin high

FIGURE 43

OFF State Current versus Temperature



resistivity films.[38,59,65,91] If the film is homogeneous and has two identical electrical contacts, the forward and reverse bias characteristics would be expected to be identical. The experimental results show the reverse bias conductance to be less than the forward bias at any current greater than I_{KF}. This may be due to a series resistance of 100 to 200 Ω, which may be the remnant of the reversed biased junction observed in the virgin state. The forward biased resistance of the junction is likely to be very small.

Ohmic conduction at low biases will be solely due to drift electron current and the current density will be

$$J_{\Omega} = \frac{e\mu_n n_o V}{L} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots (23)$$

where e is the electronic charge
μ_n is the drift mobility of electrons
n_o is the free electron density in equilibrium
V is the applied voltage
L is the thickness of the CdS film

At higher biases the square law region of conduction indicates a space-charge-limited (SCL) current regime.

In semi-conductors SCL currents are the result of the injection of minority carriers which alter the carrier lifetimes and allow the minority carrier current to dominate. This mechanism of "double injection"[38,99,100] of majority and minority carriers cannot easily be applied to CdS as the barrier to the injection of holes is between 1.4 and 2.4eV and always greater than the barrier to electron injection. The transition of ohmic to SCL current occurs when the injected minority carrier hole density exceeds the equilibrium electron density - and this is not possible in CdS.

In insulators - and some authors[65,99] consider CdS to be an insulator - "single injection", i.e. the injection of majority carriers only, can also result in SCL currents. For a trap free insulator[65] the charge per unit area forced in upon application of a voltage, V, is

$$Q = CV = \frac{\epsilon V}{L} \quad \ldots\ldots\ldots\ldots\ldots\ldots (24)$$

C is the capacitance of the insulator layer

ϵ is the permittivity of the insulator layer

L is the thickness of the insulator layer

The transit time for the injected charge through the insulator is

$$T = \frac{L}{\mu_n E^*} = \frac{L^2}{\mu_n V} \quad \ldots\ldots\ldots\ldots\ldots\ldots (25)$$

μ_n is the mobility of electrons in the insulator

E is the average electric field in the insulator

The current density can now be calculated from Equations 24 and 25 as

$$J_{SC} = \frac{Q}{T} \simeq \frac{\epsilon \mu_n V^2}{L^3} \quad \ldots\ldots\ldots\ldots\ldots\ldots (26)$$

When traps are in evidence Equation 26 is modified by a factor θ . This factor is required because injecting electrons into the insulator results in an increase in the trapped as well as free electron density.

The free electron density is $n = N_C \exp \frac{E_F - E_C}{kT}$ and the trapped

*The assumption that the electric field is constant over the whole insulator thickness is not strictly true[99] but this does not affect the calculation significantly.

electron density is $n_{DS} = N_{DS} \exp \frac{E_F - E_{DS}}{kT}$, if a single donor trap level of density N_{DS} is assumed at E_{DS} which lies above the fermi level, E_F, in equilibrium.

The total space charge is

$$Q = e(n - n_o + n_{DS} - n_{DSO}) \quad \ldots\ldots\ldots\ldots (27)$$

n_o and n_{DSO} are the equilibrium densities of free and trapped electrons respectively

For the case of high injection, i.e. n is much greater than n_o and n_{DS} is much greater than n_{DSO}, then the fraction of the total space charge available for free conduction is

$$\theta = \frac{eN}{Q} \simeq \frac{n}{n_{DS}} = \frac{N_C}{N_{DS}} \exp \frac{E_{DS} - E_C}{kT} \quad \ldots\ldots\ldots (28)$$

$$\text{if} \quad n_{DS} >> n$$

The modified expression for SCL current is thus

$$J_{SC} = \frac{\epsilon \theta \mu_n V^2}{L^3} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (29)$$

(Superlinear conduction of the form $I \alpha V^{n+1}$ where n is greater than 1 is indicative of SCL currents in semi-conductors with more than one significant trap level above the fermi level in equilibrium)

The transition between ohmic and SCL current dominance occurs at V_K where $J_{SC} = J_\Omega$ and from Equations 23 and 29

$$V_K = \frac{eL^2 n_o}{\epsilon \theta} \quad \ldots\ldots\ldots\ldots\ldots (30)$$

From Figure 41 a typical value of V_K is found and with $L = 2 \mu m$ and $\epsilon_r \simeq 12$ Equation 30 becomes

$$\frac{\theta}{n_o} = \frac{eL^2}{V_K \epsilon} = 1.2 \times 10^{-20} cm^3 \quad \ldots\ldots\ldots\ldots\ldots (31)$$

From Equation 23 and using G_o from Figure 41, and assuming electron mobility between 1 and $50cm^2/Vs$ and device area of $1mm^2$, the electron density is found

$$5 \times 10^{11} < n_o < 2.5 \times 10^{13} cm^{-3} \quad \ldots\ldots\ldots (32)$$

From this range of electron density a range of possible θ is found by using Equation 31

$$6 \times 10^{-9} < \theta < 3 \times 10^{-7} \quad \ldots\ldots\ldots\ldots (33)$$

This is a very low value for θ , which is the ratio between the free electron and trapped electron density in equilibrium. The donor level must lie above the fermi level - otherwise the injection of electrons will not significantly increase the trapped electron charge and the simplification that n_{DSO} is much smaller than n_{DS} will not be valid. The fermi level from Equation 32 must be between 0.44 and 0.34eV below the Conduction Band. Even for a donor situated at 0.4eV below the Conduction Band, Equation 28 gives the donor density N_{DS} as between 4×10^{20} and $7 \times 10^{18} cm^{-3}$. The donor density will be greater for donors situated closer to the Conduction Band.

Section 7.33 ii) suggests a donor level at 0.1 and at 0.57eV if mobility is assumed to be barrier limited, or at 0.17 and 0.65eV if mobility is assumed to be stacking fault limited. The deep donor level will not play a significant role as it lies well below the fermi level. For donors at 0.1 or 0.17eV donor densities will be

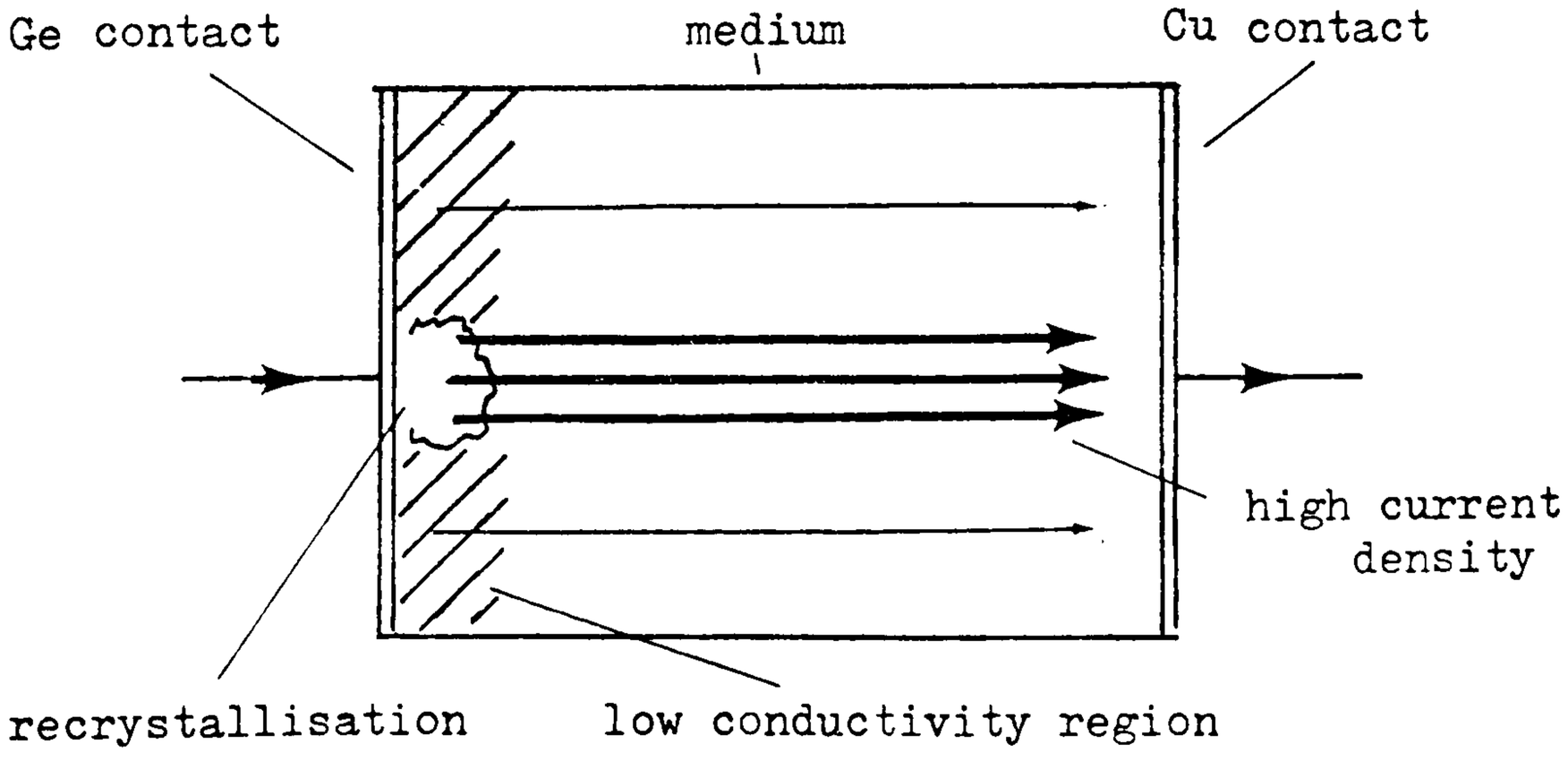
$$4 \times 10^{25} > N_{DS} > 7 \times 10^{23} cm^{-3} \text{ for donors at 0.1eV}$$

$$\text{or} \quad 2 \times 10^{24} > N_{DS} > 5 \times 10^{22} cm^{-3} \text{ for donors at 0.17eV}$$

from Equation 33 $\ldots\ldots\ldots\ldots\ldots\ldots (34)$

These densities are far in excess of measured trap densities in CdS.[37,101] A large density of donor states can exist above the fermi level without resulting in a high density of free electrons if a large density of compensating states also exists. For example if the number of donor states is N_{DS} almost all are ionised as the energy level E_{DS} is far above the fermi level. The ionised donor states are partially compensated by ionised acceptor states, N_A^-, lying below the fermi level. The free electron density in equilibrium is the difference between N_A^- and N_{DS}^+ which may be very small in comparison with N_{DS}^+.

The analysis of Section 7.32 applies to the film before forming and the deduced free electron density, n_o, will be an average for the whole film. After forming, the overall conductance increases, and this is understood to be "penetration" of the very low conductivity region[5,35] near the Ge - CdS interface through to the remaining higher conductivity portion of the film. The "penetration" may be the result of the recrystallisation of sections of the low conductivity region near the interface. Current will be concentrated in the region of the "penetration". Current flow in the remainder of the film will also be concentrated as the effective area of high conduction has been limited to the area of "penetration".



This is supported by the fact that the OFF state conductance is not directly related to the device area.

The overall effect on the analysis is that n_o may be several orders of magnitude greater than indicated by Equation 32, as the effective area of high conduction may be much smaller than the $1mm^2$ copper contact area.

The analysis deriving Equation 29 for J_{SC} assumes a homogeneous insulator, and in particular a uniform density of donors. This is unlikely to be the case, especially in evaporated films.[5,35,36] A gradation of the donor density will still allow square law ($I \alpha V^2$) conduction[56] but at different voltages from those expected in the ideal case. For example if the donor density in the vicinity of the cathode is greater than the average for the film, then SCL currents will be lower than in the ideal case and V_K will be larger.

Combination of the effects of current constriction by forming, and gradation of donor densities within the film, can effectively reduce the over-large donor desities deduced in Equation 34 to reasonable levels. (It should be noted that if donor densities are in the region of $10^{18} cm^{-3}$ or greater, the donors will form an energy band[95] rather than the assumed discrete energy level, and conduction within the band may be possible.[43,102])

The application of white light or increasing the temperature, increases the conductivity in the ohmic and SCL current regimes as may be expected. The application of white light marginally increases V_K, which is consistent with other measurements on CdS.[65] Increasing the temperature shows a strong decrease in V_K. This can be investigated by considering the temperature

dependence of Equation 30.

$$V_K(T) \quad \alpha \quad \frac{n_o}{\theta} \quad \alpha \quad \exp \frac{E_{FO}(T) - E_{DS}}{kT} \qquad \ldots\ldots\ldots\ldots\ldots\ldots (35)$$

where $E_{FO}(T)$ is the fermi level in equilibrium

The temperature dependence of the fermi level needs to be calculated to determine $V_K(T)$. The density of free electrons, n_o, is determined by the requirement for space charge neutrality. From Equation 13 the free electron density at room temperature equals the deep ionised donor density, N_{DD}^{+}. The temperature dependence of the fermi level can be determined for the range of temperatures $n_o \approx N_{DD}^{+}$.

$$n_o = N_C \exp \frac{E_{FO} - E_C}{kT} = N_{DD} \exp \frac{E_{DD} - E_{FO}}{kT}$$

which implies

$$E_{FO} = \frac{E_{DD} + E_C}{2} - kT \log_e \frac{N_C}{N_{DD}}$$

and substituting E_{FO} into Equation 35 gives

$$V_K(T) \quad \alpha \quad \exp \frac{E_{DD} + E_C - 2E_{DS}}{2kT} \qquad \ldots\ldots\ldots (36)$$

If $2E_{DS}$ is less than $E_{DD} + E_C$ then V_K will decrease with increasing temperature. But assuming E_C is the reference level, 0.0eV, gives $E_{DS} = -0.11$eV and $E_{DD} = -0.59$eV, which makes the exponent of Equation 36 negative, and this is not in agreement with the observed trend.

However, if the free electron density is much greater due to the "penetration" of the low conductivity region then the fermi level will lie closer to the Conduction Band and $n_o \simeq N_{DS}^{+} - N_A^{-}$.

When the fermi level is still sufficiently below E_{DS} then modifying the temperature will not change n_o significantly and

$$E_{FO} \simeq E_C - kT \log_e \frac{N_c}{n_o}$$

which gives

$$V_K(T) \quad \alpha \quad \exp \frac{E_C - E_{DS}}{kT}$$

This relationship is in agreement with the observed trend of decreasing V_K with increasing temperature.

The conductivity of the film in equilibrium as a function of temperature will be dominated by the temperature dependence of the mobility - the free electron density being relatively independent of temperature. Figure 43 shows an activation level of 0.126eV in the vicinity of room temperature and suggests grain boundary barrier dominated mobility. But as Figure 43 represents the characteristic of only one sample, it is felt that a larger number of devices requires to be tested before this trend can be confirmed.

The significant increase in the forward bias threshold, V_{TF}, with decreasing temperature can be understood by considering the process of avalanche ionisation caused by the high electric field.[48,64] The electric field is unevenly distributed within the film - the maximum, E_{max}, existing at the anode.[38,65] The breakdown electric field for materials can be considerably decreased from 10^6V/cm, which is typical of insulators,[66] if the material has a large density of impurities.[62] The maximum electric field in the SCL current regime is only $\sqrt{2}$ times[99] the geometric electric field which is the applied voltage divided by the thickness of the material. Typically V_{TF}

occurs when the maximum electric field is in the region 1 to $6 \times 10^4 V/cm$.

Avalanche ionisation[61] occurs when the electric field imparts enough energy to free electrons so that upon collision with lattice or trap hole-electron pairs are produced which increase the number of charge carriers and conductivity. These additional carriers can then cause further ionisation by collision, and so on ....., resulting in a rapid increase in conductivity over a small voltage range. The kinetic energy of a charge carrier increases with increasing mobility and increasing applied electric field.[38,60] If the mobility is grain boundary or stacking fault limited, then mobility will decrease as temperature decreases. The electric field to cause ionisation must therefore increase with decreasing temperature to ensure that sufficient energy is available for the ionisation.

7.50 SWITCHING AND THE ON STATE

In this section switching and the effect of switching on the ON state are investigated. A model is proposed and this is directly related to the formation and destruction of temporary and permanent filaments in amorphous glasses.

7.51 Outline of device characteristics

From a study of the switching characteristics it soon becomes obvious that any single device can have a variety of similar characteristics. This variety is a result of the method of switching, and to a smaller degree, the history of the device, as well as being dependent on the physical and electrical parameters of the device itself.

Figure 44 shows two switching cycles of a device at different times in its life. Even though the applied voltage is almost identical and the external circuit is identical, there are considerable differences between the characteristics. The transition was brought about by temporarily reducing the series resistance and allowing a higher switching current to flow in reverse bias. The transition between characteristics is thus a result of a historical change in the method of switching. The OFF state is modified by the transition in such a way that it remains in its modified state even after removal of the applied voltage.

There exists a complex interaction of factors which determine the state into which the device will switch. The current flowing through the device during switching is an important factor in determining the switch to both the OFF and ON states. The current is determined by the applied voltage to the device and this is a function of the series resistance in the circuit during switching. The switching current is also dependent on the device resistance which is very dependent on the current at all stages in the switching sequence.

Figure 44 shows switching cycles typical of the characteristics produced when the delay between the forward and reverse biases is of the order of seconds. If this delay is reduced by the application of a sine wave the switching cycle is significantly modified.

7.52 Switching model

Space-charge-limited currents produce high electric fields near the anode contact.[65,99] It will be within this region that

FIGURE 44

Switch Cycles at Two Periods
in a Device's Life

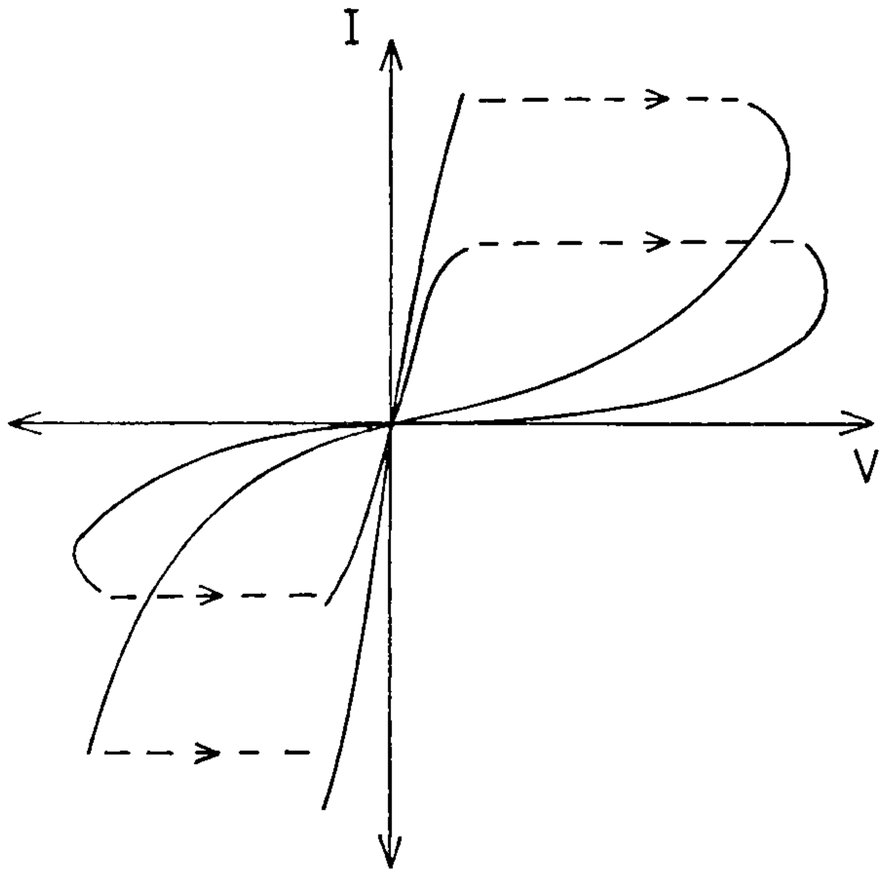


FIGURE 45 -

Forward Bias Switching
from ON to OFF state

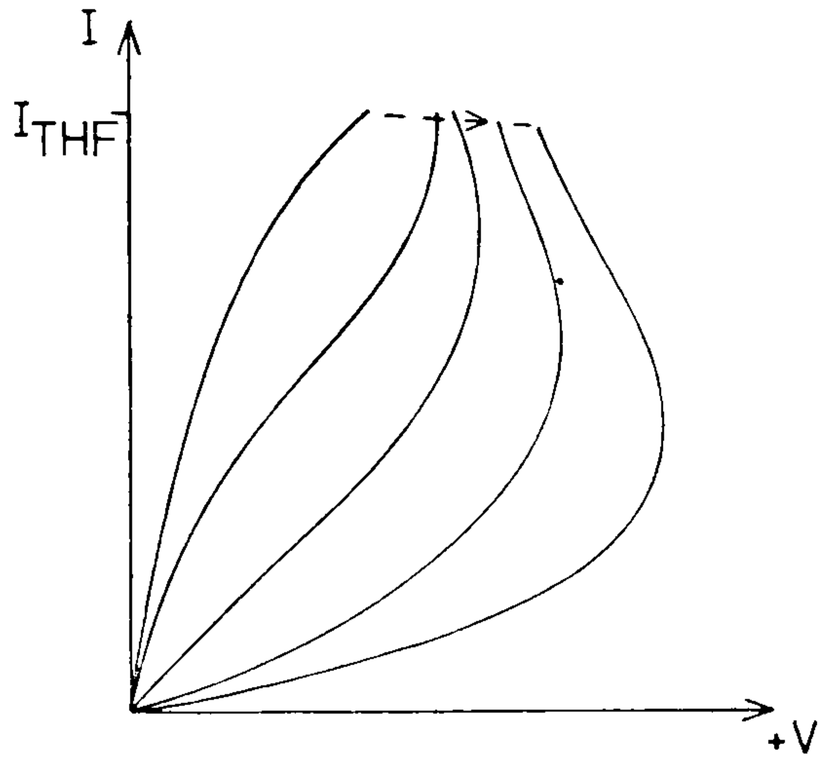


FIGURE 46

Reverse Bias Switching
from OFF to ON state

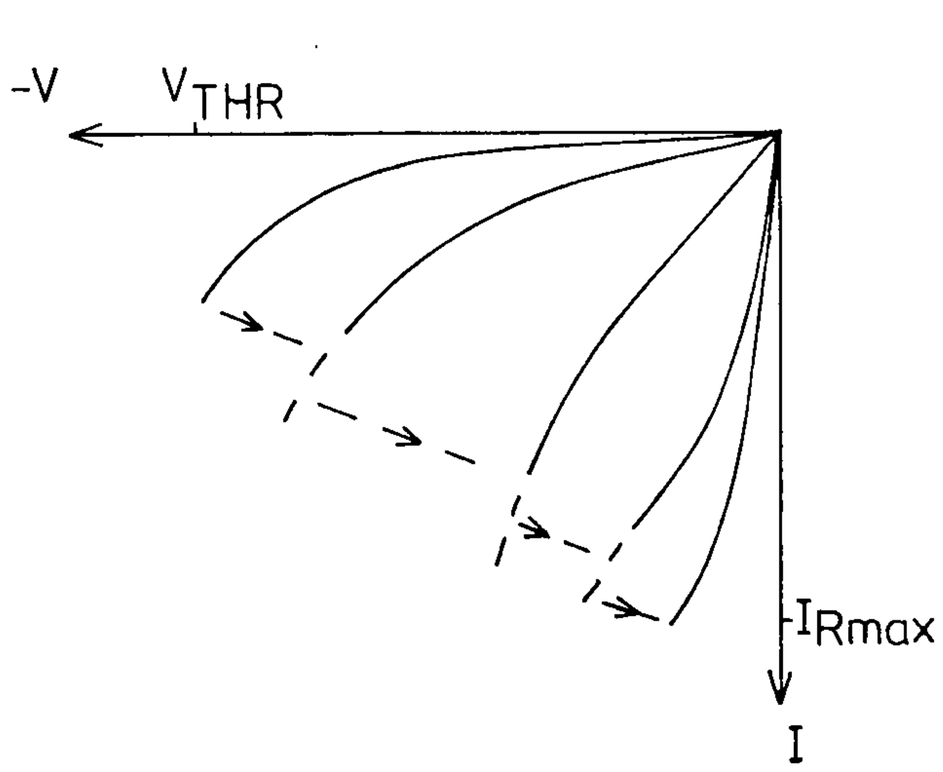
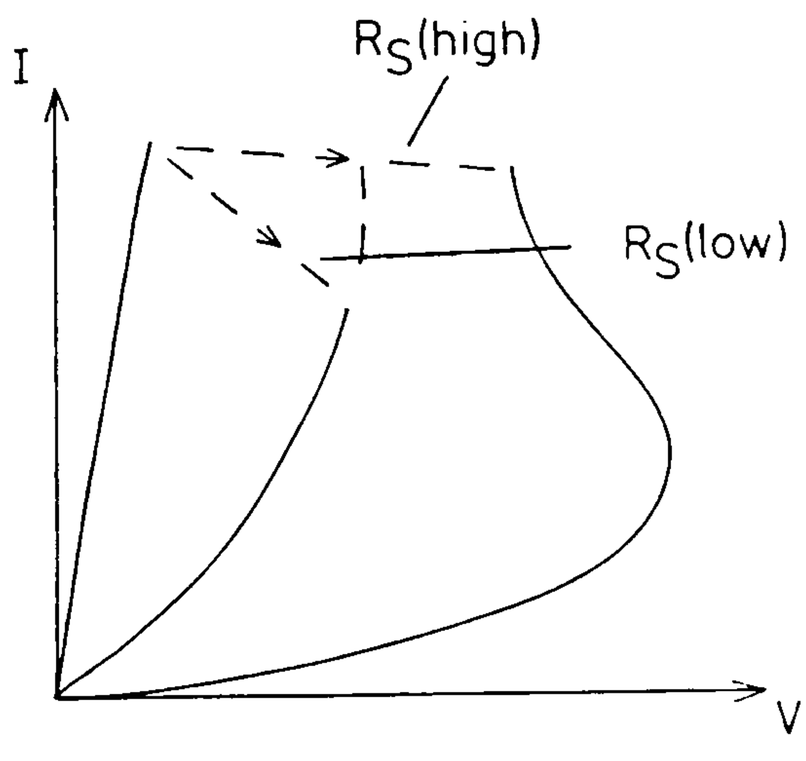


FIGURE 47

Effect of Series Resistance on
Switching to the OFF State



avalanche ionisation will begin and hole-electron pairs will be produced. The electrons will be swept quickly out of the region but the holes, due to their lower mobility,[64] will remain longer and form a positive space charge region.

This positive space charge region close to the anode decreases the SCL current produced electric field. (In the gas discharge experiments the positive gas ions produce a space charge and thus high electric fields near the cathode,[60,64] but the gas prior to ionisation does not have localised high electric fields as do the semi-conductor and glass.)

At higher currents current constriction[46] occurs and a negative resistance regime is observed after the "breakdown" through avalanche ionisation. This formation of a high conduction filament may be explained by the growth of a small higher conductivity region through attraction of current as described in Section 5.42 i). Another possible explanation is the minimising of the entropy production.[103] This theory suggests that a filament is produced because the overall power dissipated in the device will be less than in the case of uniform conduction over the whole contact area.

If the anode contact is a sufficiently good heat sink the power dissipated in the region of the anode, which attracts the largest electric field within the device, will be quickly conducted away and the device temperature will remain low. A threshold type of switching characteristic will be observed. The negative resistance is associated with the formation of a temporary filament.

If the anode contact is a poor heat sink the temperature in the

vicinity of the anode could rise to such an extent that "mass transfer" or phase changes[56] can take place. This permanent change in the structure of the semi-conductor or glass can be initiated by "breakdown" or filament formation, both of which will result in raising the temperature in small regions of the device.

The growth of a permanent filament which is a result of a phase change, progresses from the anode. As the filament grows the anode could be considered to exist at its tip as the filament will be highly conductive. The region of high electric field and high temperature which forces the filament to grow, is pushed ahead of the filament as it grows. The filament thus grows until the cathode is encountered. The formation of this filament is observed to result in a memory type of switching characteristic.

The filament is ruptured by application of a fast current pulse which quickly raises the filament temperature. The filament is cooled quickly as the surrounding film is still close to ambient temperature. The filament recrystallises to a high resistivity state.

7.53 Effect of series resistance

Figures 45 and 46 show the current-voltage characteristics displayed during switching under forward and reverse biases respectively. The multitude of states observed is the result of the application of a sequence of saw-tooth voltage waveforms during switching.

The device states will be defined as follows

"OFF" state	A super-linear characteristic, $I \alpha V^n$ where $n \geq 1$. This state has the same trends observed in the formed device but may have higher conductance. This state is ohmic at low biases.
"ON" state	A sub-linear characteristic, $I \alpha V^n$ where $n \leq 1$. This state is also ohmic at low biases.
"Intermediate" state	A mixture of super and sub-linear regions in the characteristic. This state lies between the ON and OFF states.

Figure 45 shows a transition between an ON state, through a higher resistance ON state, two intermediate states, and an OFF state before switching to an OFF state which is stable to the applied voltage wave-form. The transition is caused by applying a signal which successively exceeds the current threshold in each of the transition states. This partial switching of the device allows the switching mechanism to be observed closely: if instead of the saw-tooth voltage wave-form a constant current signal was to be applied, the switching would be in a single step as shown in Figure 44.

Each of the transition states is stable at low current levels and the device will remain in the state even when the signal is removed.

The "path" of switching is determined in part by the series resistance to the device - as discussed in Chapters 5 and 6.

Series resistance results in constant current during switching if the series resistance is much greater than the device resistance, i.e. the current is determined by the series

resistance and is essentially independent of the change in device resistance during switching. Low series resistance will result in the current falling as the device switches from ON to OFF as the total resistance of the circuit increases significantly during switching. Figure 47 compares the effect of low and high series resistances when the same threshold voltage is applied to the device. The reduction in switching current as a result of the low series resistance, brings about device switching to a low resistance OFF state rather than the high resistance OFF state which is possible during constant current switching.

Figure 46 shows switching from the OFF to ON state which is also dependent on the series resistance, R_S. Here constant current switching will only result in partial switching of the device. If switching to a low resistance ON state is required, then the switching current must be allowed to rise, and this is possible only with a low series resistance.

7.54 Switching to the ON state

Figure 48 shows the relationship between the magnitude and duration of switching pulses for a device in the OFF state. The switching results in a significant permanent reduction in the device resistance, though the device may not switch completely into an ON state. Application of pulses with less magnitude or shorter duration can result in threshold switching, i.e. upon the removal of the pulse voltage the device reverts to the original OFF state. From Figure 48 it can be seen that switching is possible with long pulses at low voltages, but for very short pulses the threshold voltage increases significantly.

FIGURE 48

Reverse Bias Threshold Voltage as
a function of Pulse Duration

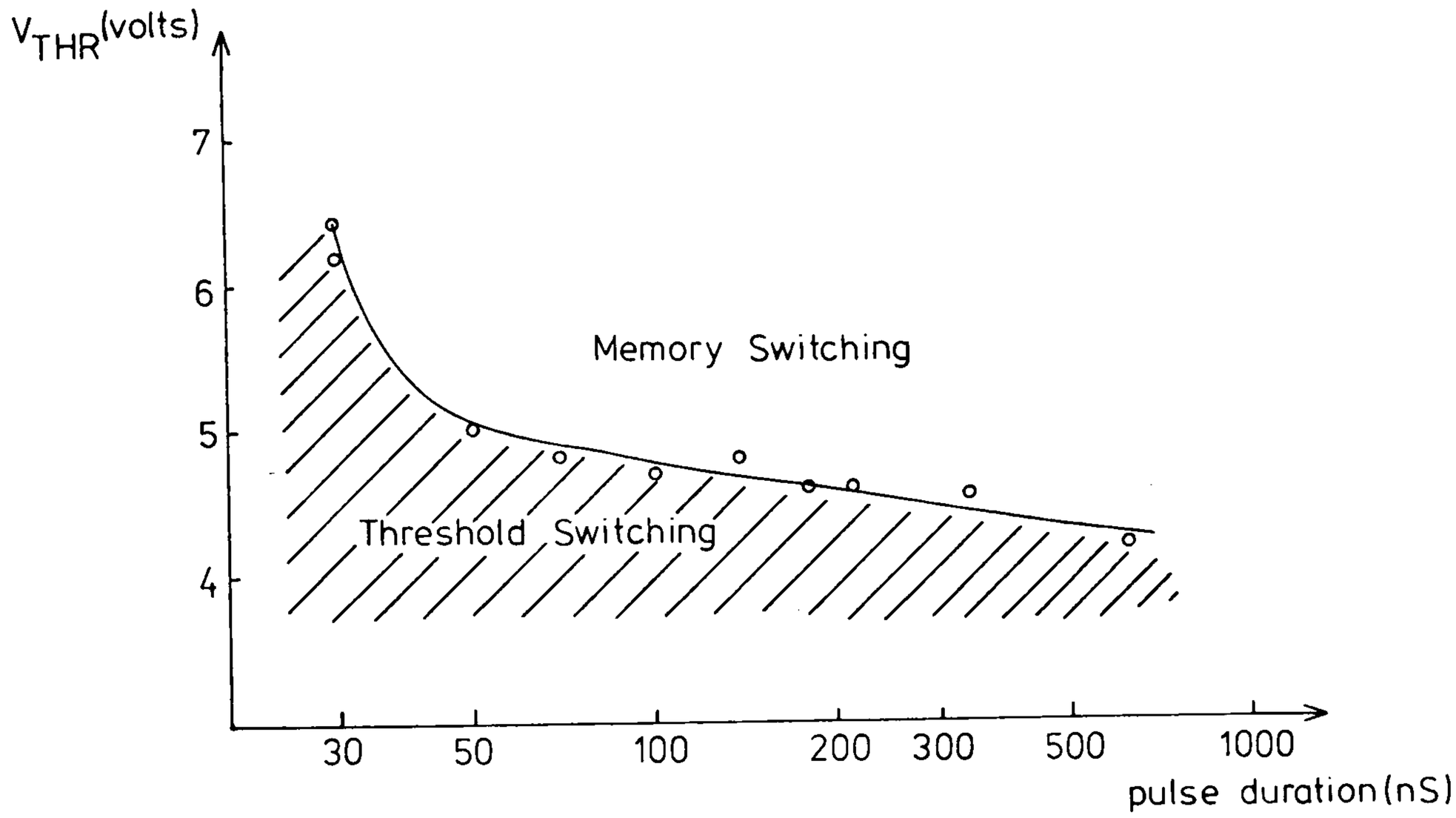
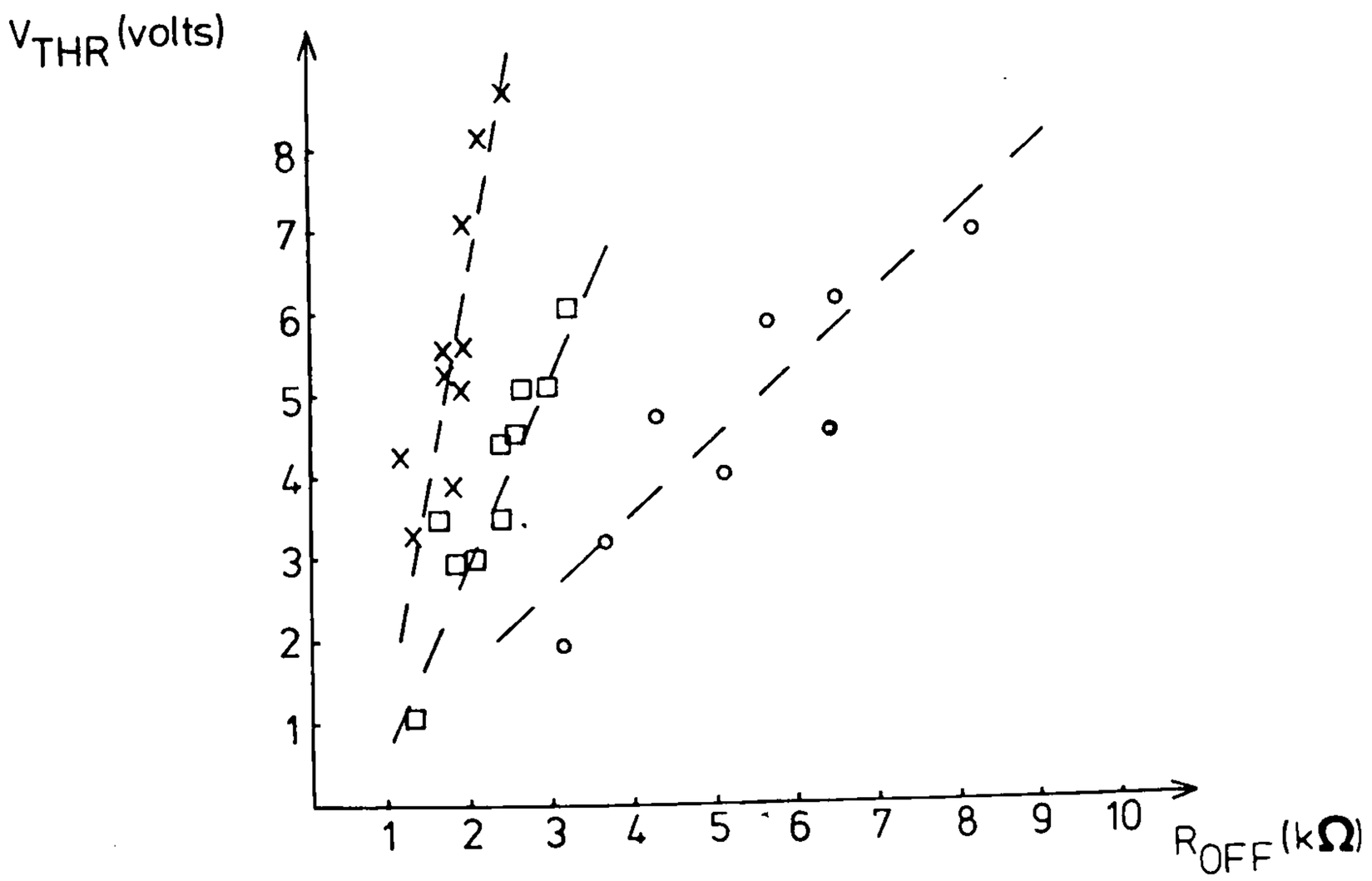


FIGURE 49

Reverse Bias Threshold Voltage as a function
of the OFF State Resistance



This result is consistent with the formation of a temporary filament which converts to a permanent filament if sufficient time is allowed.[39,40,51] Increasing the magnitude of the applied voltage decreases this critical time.[40]

Threshold switching has been observed for switching pulses of a duration of less than 20nS but memory switching has only been observed with pulses of a duration greater than 30nS. Typically, switching in glass memory devices is completed in several microseconds but this can be reduced to nanoseconds by applying voltages in excess of V_{THR}.[40]

Figure 46 shows switching characteristics which are also consistent with the formation of permanent filaments.[56] The original OFF state is modified by the partial or incomplete formation of a permanent filament and its resistance is lowered by the short-circuiting effect of the filament growth. The lower resistance OFF and ON states show the progressive increase in filament growth reducing the size of the high resistivity region between the filament tip and the cathode. Eventually the resistance of the filament is greater than the resistance of the remaining high resistivity region and an ON state is produced.

The threshold voltage, V_{THR}, is proportional to the resistance of the OFF state, R_{OFF}, as shown in Figure 49 for three devices - R_{OFF} measured at zero bias. The OFF state resistance is a function of the switching cycle and a portion of filament may remain after incomplete switching from the ON state. The incomplete filament lowers the OFF state resistance as well as reducing the effective thickness of the high

resistivity layer. This reduces the voltage required to produce the necessary electric fields for ionisation breakdown, i.e. V_{THR} is reduced.

The formation of permanent filaments may be partially explained by the recrystallisation[40,56] and slow cooling of the CdS heated by current flow. The cooling of the filament region, after recrystallisation has been initiated, is critical to the region's resistivity. Slow cooling will result in the formation of a highly conductive region, whereas fast cooling can result in the filament region returning to a high resistivity state similar to its original state. Fast cooling may be caused by the rapid removal or reduction of the applied voltage. The familiar "lock on" time[40,43,51] is the time necessary for the complete filament to grow between the electrodes. If the applied voltage is reduced below a threshold during this time the device will revert to an OFF state.

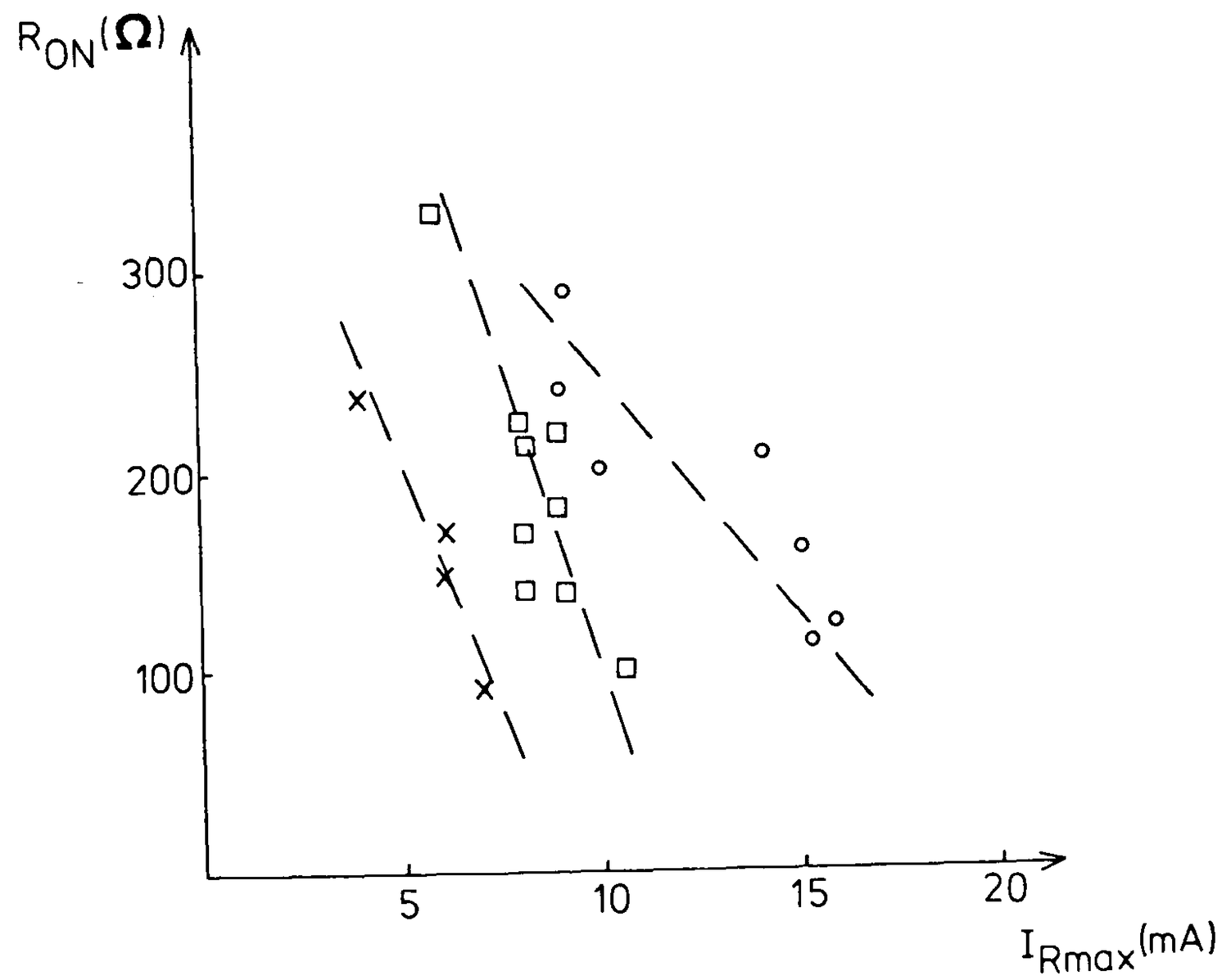
Even though the switching to the temporary filament may be electronic in origin and very fast, the formation of a permanent filament is a slower process dependent on thermal effects.

7.55 The ON state

Figure 50 shows the dependence of the ON state resistance, R_{ON}, on the maximum current flow during switching, I_{Rmax}, for three devices. Using I_{Rmax} as a switching parameter has the advantage that it is the result of the interaction between the series resistance and the applied voltage, V_a. R_{ON} decreases as I_{Rmax} increases. This relationship is consistent with the current density of the temporary filament, J_F, being constant[38,51,60] during permanent filament formation.

FIGURE 50

ON State Resistance as a function
of the maximum Reverse Bias Current
during Switching



Large switching currents thus result in large cross-sectional area filaments as the resistivity of the filament, ρ_F, is approximately constant.[51]

$$R_{ON} \alpha \rho_F A_F^{-1} \text{ and } I_{Rmax} = J_F A_F$$

$$\text{which gives } R_{ON} \alpha \frac{\rho_F}{I_{Rmax}}$$

A_F is the area of the filament

The temperature dependence proved difficult to measure as step changes in conductivity occur, but over a limited temperature range the ON state exhibited a metal-like temperature dependence, i.e. resistance increased with increasing temperature. This result is consistent with other researchers'[48,51] measurements. At high currents the filament will increase in temperature and this will result in an increase in resistance, and thus a sub-linear type of characteristic.

Figure 41 shows two ON states which were produced in the same device after consecutive switching cycles. Both states are ohmic at low forward and reverse biases, but at higher biases the characteristics become sub-linear. The lower resistance ON state begins to become sub-linear at higher voltages. This suggests that the temperature in the lower resistance filament is less at the same device voltage, even though the current density and resistivity are expected to be the same in both cases.

The typical resistance of the ON state is between 50 and 300 Ω and as a result of this the capacitance was not measurable. White light did not appear to affect the conductance

except when it was sufficiently intense to heat the device. This is in contrast to normal CdS which is very sensitive to light.

Devices with thin metal electrodes can exhibit scarring of small regions of the electrode surface. This is associated with the high localised filament temperatures[52,104] and is evidence of the importance of good heat conductive electrodes, and indeed the existence of filaments of smaller cross section than the whole contact.

The ON state resistance was found to be independent of the OFF state resistance, which confirms the dependence of the ON state upon the switching technique. ($\frac{R_{OFF}}{R_{ON}}$ varies between 4 and 40 in most devices.)

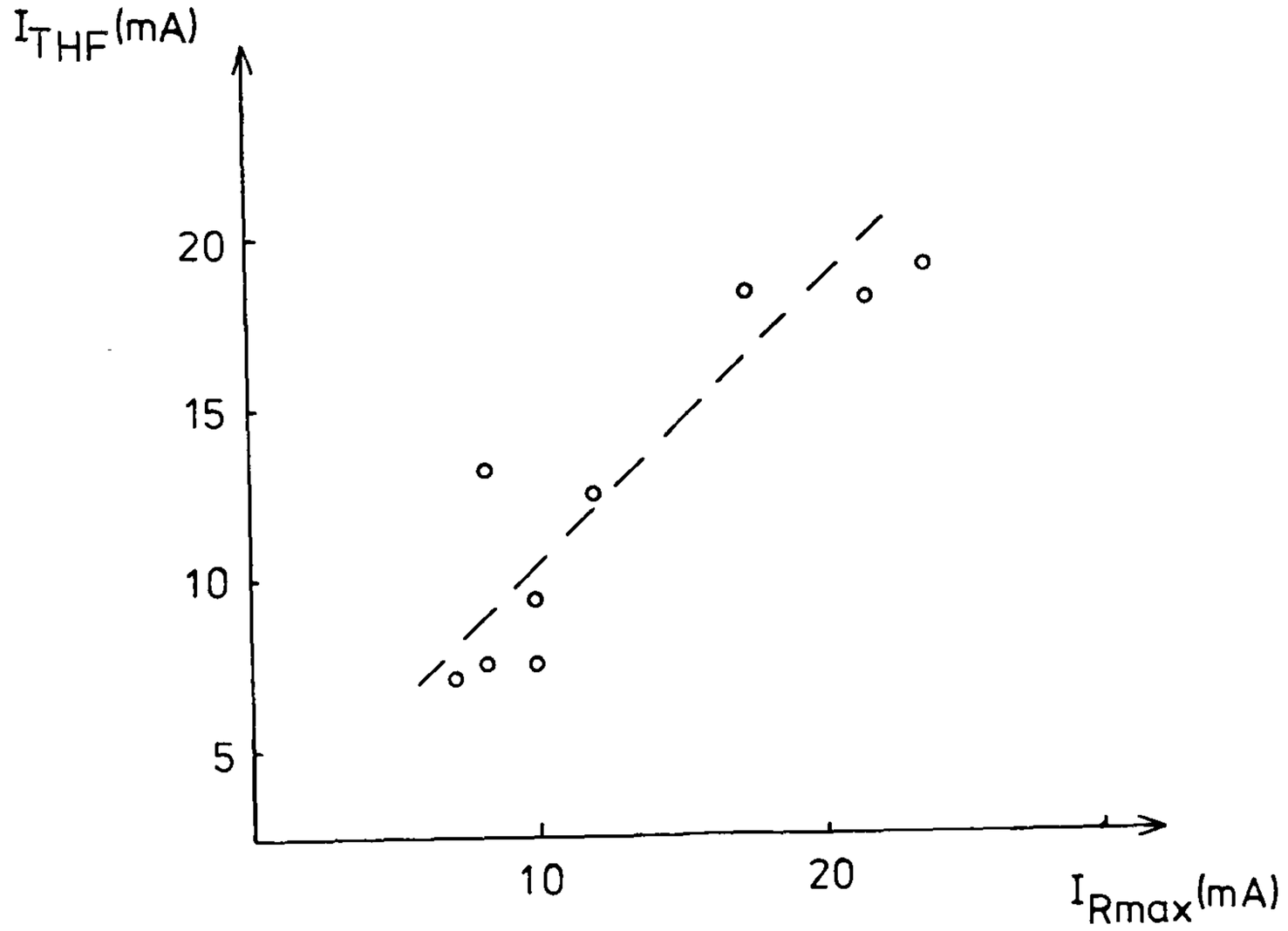
7.56 Switching to the OFF state

Switching from the ON to the OFF state occurs at a current threshold, I_{THF}. I_{THF} has a very clear relationship to I_{Rmax} as shown by Figure 51: I_{THF} approximately equals I_{Rmax}. Thus switching back to the OFF state occurs when the filament is ruptured by the same current density that caused its formation. The critical current density, which also determined the cross section area of the filament, may have an associated critical temperature. At this critical temperature recrystallisation may occur.

Switching to the OFF state is dependent on the rate of increase of the applied voltage. Switching is observed to occur with greater ease (i.e. more effectively) if the voltage is increased rapidly towards the threshold. If the voltage is increased slowly the device can switch to a low resistance OFF state or to a lower resistance ON state.

FIGURE 51

Forward Bias Threshold Current as a function of the maximum Reverse Bias Current during Switching



These observations may be understood by considering the rupturing of the ON state filament. Switching is the result of the filament region recrystallising due to local temperature in excess of a critical temperature. If the current in the filament rises quickly the rest of the device will still remain near the ambient temperature and will effectively "quench" the recrystallisation zone. The current is then redistributed over a greater cross section area of the device and the current density falls below the critical level. If the current in the filament rises slowly the whole device is heated as the current density approaches the critical level. This will result in either an increase in filament size as recrystallisation and slow cooling result in filament formation, or incomplete filament rupture as the cooling of the recrystallisation zone is only partially effective.

This partial switching is probably encouraged by the liklihood that the filament is not of constant cross-section area throughout its length. This will be a result of the variation of current during filament formation. The narrower sections of the filament will rupture first and the wider sections may remain if the current density is not sufficiently large.

Switching to the OFF state has also been observed under reverse bias, which agrees with the above theory, but this polarity of switching is not as consistent as forward bias switching.

Two OFF states of the same device are shown on Figure 41. The more conductive OFF state has a larger ohmic characteristic and this is consistent with the existence of a remnant of the permanent filament short circuiting part of the high resistivity CdS.

7.57 Polarity of switching

Switching to the ON state occurs consistently under reverse bias. Switching to an ON state is possible under forward bias but the ON state has such a low resistance that it becomes impossible to return to an OFF state. Threshold switching is consistently observed under forward bias and the device can stand much higher currents under forward bias.

These observations suggest that a fundamental difference exists in the device under forward and reverse biases. Under high values of bias a region of high electric field exists at the anode where the power dissipation is greatest. Inhomogeneous CdS may result in the electric field at one electrode being greater than at the other electrode under the same but reverse bias. The power dissipation will be greater for the same bias near the electrode with the higher electric field. Greater power dissipation can result in higher temperatures and thus recrystallisation becomes more likely. Higher electric fields, which result in avalanche breakdown, are observed under forward bias, but temperatures do not increase sufficiently for recrystallisation to occur.

Another possibility is that the asymmetry of switching is due to the difference in thermal conductance of the two electrodes. CdS has a low thermal conductivity which is typical of some glasses.[63] Both Germanium and Copper contacts have much higher thermal conductivities than CdS, and if the region of greatest heat dissipation is near the electrode, the temperature in this region depends on the efficiency of the electrode in removing heat. If permanent switching is the result of high

temperature then the switching occurs when the Copper is the anode. This implies that the Germanium is a better heat sink than the Copper contact.

Copper has a thermal conductivity coefficient six times greater than Germanium[63] and this would suggest that the Copper contact is the better heat sink - at least initially. The Copper contact is however very much thinner than the Germanium, i.e. 2μm compared with 0.5mm, and therefore its temperature will rise to that of the CdS in a short time. The Copper contact will then cease to be an effective heat sink as heat can only be conducted away at a slow rate by the surrounding air.

It is interesting to note that the device needs to dissipate typically 40 mW during switching and this power is sufficient to raise the temperature of the Copper contact by 100^{o}C in 10mS. (This calculation is based on the heat capacity[105] of a Copper contact 1mm^{2} area and 2μm thick.)

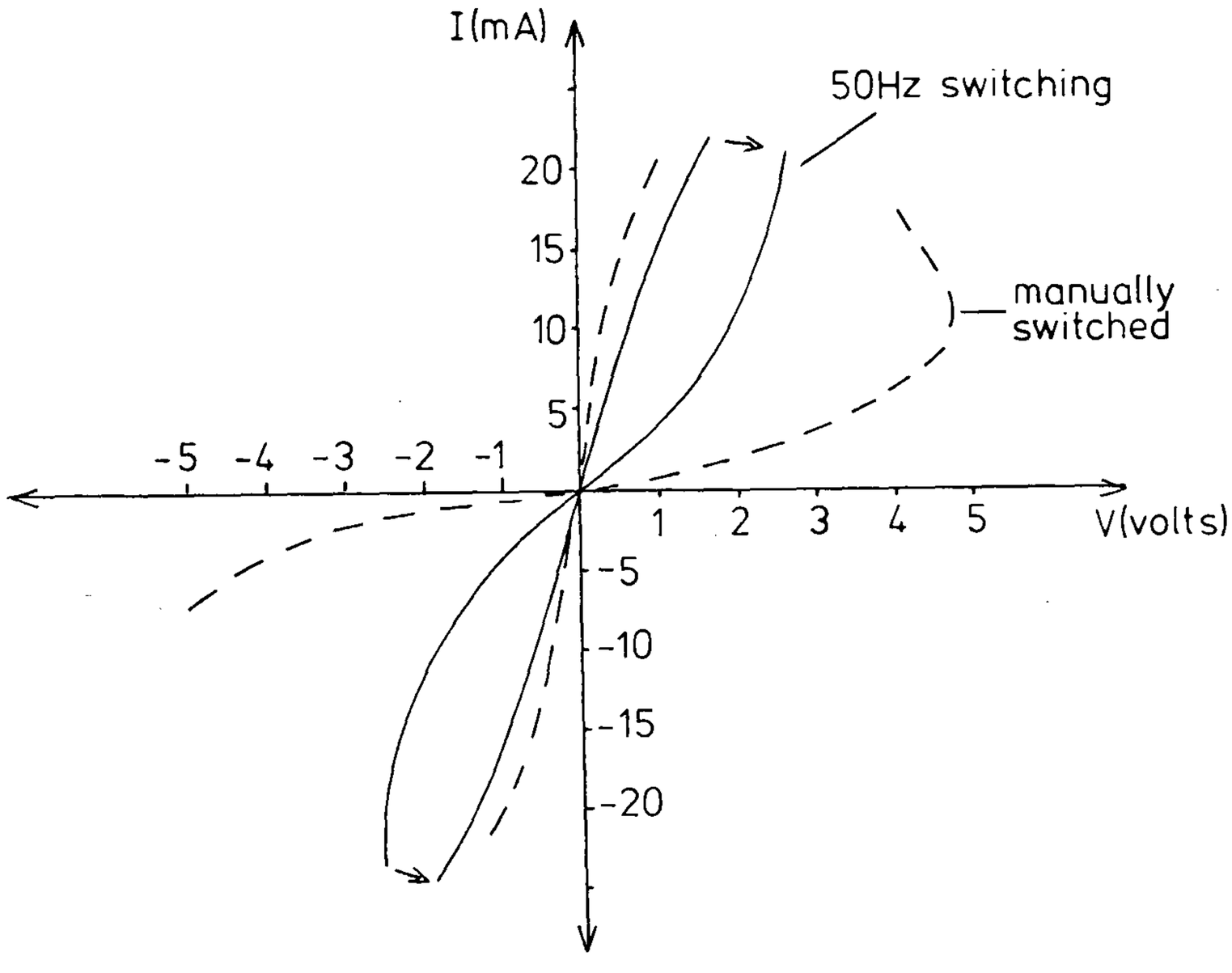
7.58 Continuous cycle switching

Figure 52 shows the current-voltage characteristic of a device continuously switched by a 50Hz voltage sine wave and the characteristic of the same device switched manually. The continually switched device is subjected to a signal which allows approximately 10mS for the device to switch. On the other hand the manually switched device is subjected to a signal which allows as much as a second for switching to be completed.

Difficulty was encountered in sustaining continuous memory switching for prolonged periods: it was always necessary to make small adjustments to the applied voltage or the external

FIGURE 52

Current Voltage Characteristic of Cycle Switching under a 50Hz sine wave voltage



circuit to re-initiate switching. Continuous switching for periods of 30 seconds was typical. At higher frequencies continuous switching became progressively more difficult to sustain. The ratio of the OFF to ON state resistance at zero bias, $\frac{R_{OFF}}{R_{ON}}$, was found to decrease with increasing frequency - the maximum value for $\frac{R_{OFF}}{R_{ON}}$ was observed by manual switching.

As described in the previous sections, the state into which a device switches depends on the current flow during the process of switching. When the device is subjected to a continuously changing voltage, the current flow during switching is determined not only by the series resistance but also by the time dependence of the voltage.

If the applied voltage in reverse bias is not kept above a critical value for a period greater than the "lock on" time, then permanent filament formation will be incomplete. Similarly, if the applied voltage in forward bias is applied too quickly after the device has been subjected to high currents, then the filament may not be completely ruptured. This will be due to the temperature of the device being too high to allow the rapid cooling necessary for high resistivity recrystallisation.

These two time dependent effects will result in incomplete switching, which is observed as low values for $\frac{R_{OFF}}{R_{ON}}$. Even though temporary filaments may be formed very quickly by electronic processes, permanent filaments are formed and destroyed by slower thermal processes.

It is possible that faster memory switching can be achieved if short voltage pulses are applied rather than the continuous

sine wave. Formation of a permanent filament has been shown to begin within 30nS (See Section 7.54), when a sufficiently large pulse is applied. A shorter time may be possible for filament rupture as this process requires rapid cooling rather than the slow cooling of formation. Sufficient delay is necessary however, between filament formation and rupture to allow the device to cool. The delay between formation and rupture is a function of the power dissipation during and after filament formation, and is a crucial factor in determining the maximum switching rate.

7.60 SUMMARY

In this chapter the device electrical characteristics have been presented and discussed in terms of several models.

The strong frequency dispersion observed in the virgin and OFF states is attributed to the interaction of the impedance of a junction between the Germanium and interface region and the impedance of the CdS film. The "forming" of the device from the virgin to the OFF state not only removes the effect of the Germanium junction but also "penetrates" a low conductivity region of the CdS film. Space-charge-limited currents are the result of the capture of electrons injected into the CdS to form a dominant fixed space charge.

Switching to and from the ON state is the result of the formation and destruction respectively of highly conductive filaments. The switching characteristics are more dependent on the physical properties of the device and the external switching circuit than on the electrical properties, whereas the virgin and OFF state characteristics depend on the electrical properties of the device.

CHAPTER 8

8.00 EFFECTS OF DEVICE FABRICATION ON ITS ELECTRICAL CHARACTERISTICS

8.10 INTRODUCTION

In this chapter the dependence of the device's electrical characteristics on the method of its fabrication is investigated. As previously discussed, temperature during evaporation, condensation rate and film thickness, can affect profoundly the electrical characteristics of the film. The electrical characteristics of any device fabricated from the film will also be affected by these parameters and the type of contacts made to the film.

8.20 DEVICE FABRICATION

All the devices were fabricated by the evaporation of CdS on to (100) Germanium doped with Gallium and all had 1.0mm^2 Copper contacts evaporated on to the CdS film at room temperature. Samples G and I had in addition, devices with Aluminium and Chromium contacts of the same area as the Copper. All the Germanium substrates were polished and cleaned in an identical manner.

At least four devices of each type were fabricated and tested on every sample to ensure representative results.

Samples A, B and C

These three samples have substrates with 10^{13}, 10^{16} and 10^{19}cm^{-3} Gallium dopings respectively. The CdS film was evaporated on to all three substrates during the same evaporation. The substrate temperature during the evaporation was 185^{o}C and

the condensation rate was 2250Å/min. A 7.2μm thick film was condensed on to all the substrates. Contacts were evaporated on to all three samples at the same time.

Samples D, E and F

These three samples have substrates with $10^{19}cm^{-3}$ Gallium dopings. Substrate temperatures during the evaporation were 145, 130 and 95°C and condensation rates were 3360, 3120 and 3120Å/min respectively. Films 8.4, 7.8 and 7.8μm thick respectively were condensed. Contacts were evaporated on to all three samples at the same time.

Sample G

This sample has a substrate with $10^{19}cm^{-3}$ Gallium doping. Substrate temperature during evaporation was 65°C, condensation rate was 4800Å/min, and a 12μm thick film was produced.

Sample H

This sample has a substrate with $10^{19}cm^{-3}$ Gallium doping. Substrate temperature during evaporation was 180°C, condensation rate was 273Å /min, and a 4.5μm thick film was produced.

Samples I and J

These samples have substrates with $10^{19}cm^{-3}$ Gallium doping. Substrate temperature during evaporation was 172°C for both devices, and condensation rates were 1765 and 2640Å/min respectively. Films 3 and 6.6μm thick respectively were produced. The Copper contacts were evaporated on to both samples simultaneously.

Table I summarises these fabrication parameters for all the devices.

TABLE I

Device	Germanium Substrate Doping	Substrate Temperature during Condensation	Rate of Condensation	CdS film Thickness	CdS Contact
	cm^{-3}	Deg C	Å/min	μm	
A	10^{13}	185	2250	7.2	Copper
B	10^{16}	185	2250	7.2	Copper
C	10^{19}	185	2250	7.2	Copper
D	10^{19}	145	3360	8.4	Copper
E	10^{19}	130	3120	7.8	Copper
F	10^{19}	95	3120	7.8	Copper
G(i)	10^{19}	65	4800	12.0	Copper
(ii)	10^{19}	65	4800	12.0	Chromium
(iii)	10^{19}	65	4800	12.0	Aluminium
H	10^{19}	180	273	4.5	Copper
I(i)	10^{19}	172	1765	3.0	Copper
(ii)	10^{19}	172	1765	3.0	Chromium
(iii)	10^{19}	172	1765	3.0	Aluminium
J	10^{19}	172	2640	6.6	Copper

Device	C_1	G_1	C_2	G_2	ϵ_{eff}	σ_{eff}
	pF	$\mu\mho$	pF	$\mu\mho$		$\mu\mho/m$
A	450	3.7	83	16	66	115
B	1600	5.3	130	77	105	554
C	2100	5.3	172	102	139	734
D	1900	123.0	46	123	43	1033
E	2600	426.0	41	128	36	998
F	3600	400.0	51	85	45	663
G(i)	20700	1695.0	40	109	54	1308
(ii)	19200	1642.0	43	111	58	1332
(iii)	2435	44.0	72	44	97	528
H	1270	286.0	97	307	49	1382
I(i)	3270	859.0	148	681	50	2043
(ii)	2450	696.0	171	677	58	2031
(iii)	1600	145.0	178	283	60	849
J	2900	1032.0	93	453	69	2990

8.30 VIRGIN STATE CHARACTERISTICS

Figures 53, 54 and 55 show the log (Capacitance) and log (Conductance) versus log (Frequency) characteristics for all devices with Copper contacts. Figures 56 and 57 show the log (Capacitance) versus log (Frequency) characteristics for samples G and I resoectively with Copper, Aluminium and Chromium contacts. All measurements were taken at room temperature, i.e. between 18 and 20°C.

Table I shows the parameters C_1, G_1, C_2 and G_2, which were deduced from the characteristics by the analysis technique described in Section 7.32.

When the characteristics of two devices of the same type are compared, as much as a 20% difference could be observed in low frequency capacitance and conductance, and up to a 10% difference in high frequency measurements.

All devices show capacitance and conductance proportional to the area of the contact to the CdS film. This is shown in Figure 56 which provides a comparison between the same type of device with $1.0mm^2$ and $3.5mm^2$ contacts.

The high values deduced for C_1 and G_1 again suggest the existence of a junction region dominating the low frequency response. C_2 and G_2 appear to be of the correct order of magnitude to represent the CdS film.

From the geometry of the device it is possible to calculate ϵ_{eff}, the effective permittivity, and σ_{eff}, the effective conductivity, of the CdS film, i.e.

FIGURE 53

Log (C) and Log (G)
versus Log (f) for Devices
A, B and C

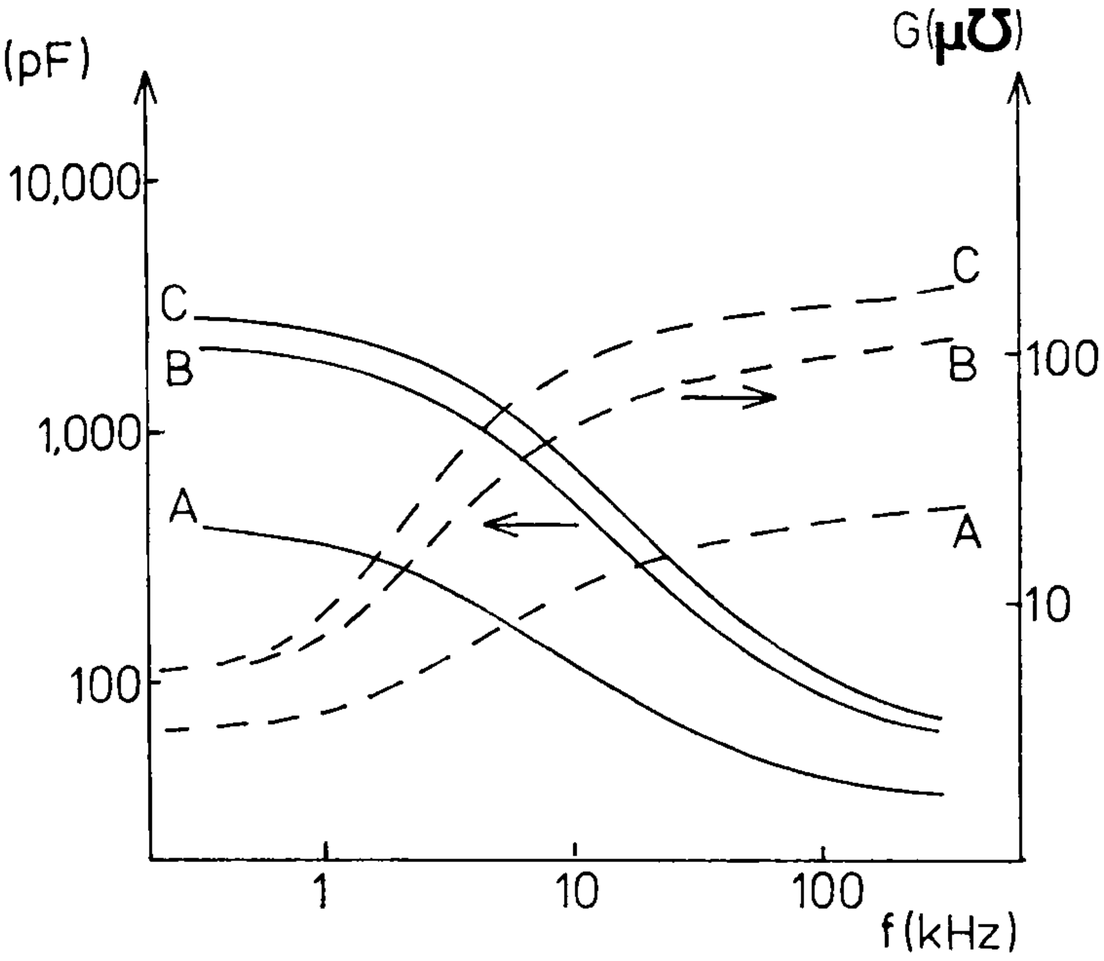


FIGURE 54

Log (C) and Log (G)
versus Log (f) for Devices
D, E, F and G

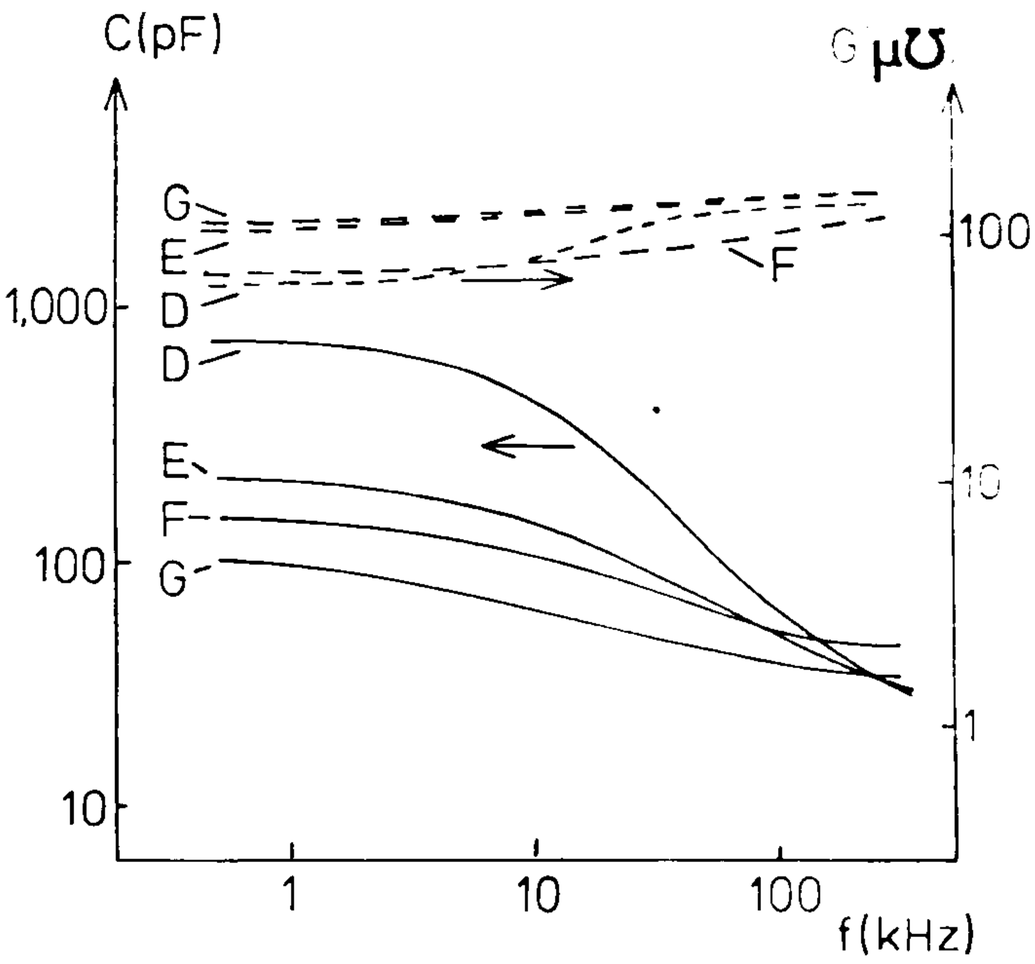


FIGURE 55

Log (C) and Log (G)
versus Log (f) for Devices
I and J

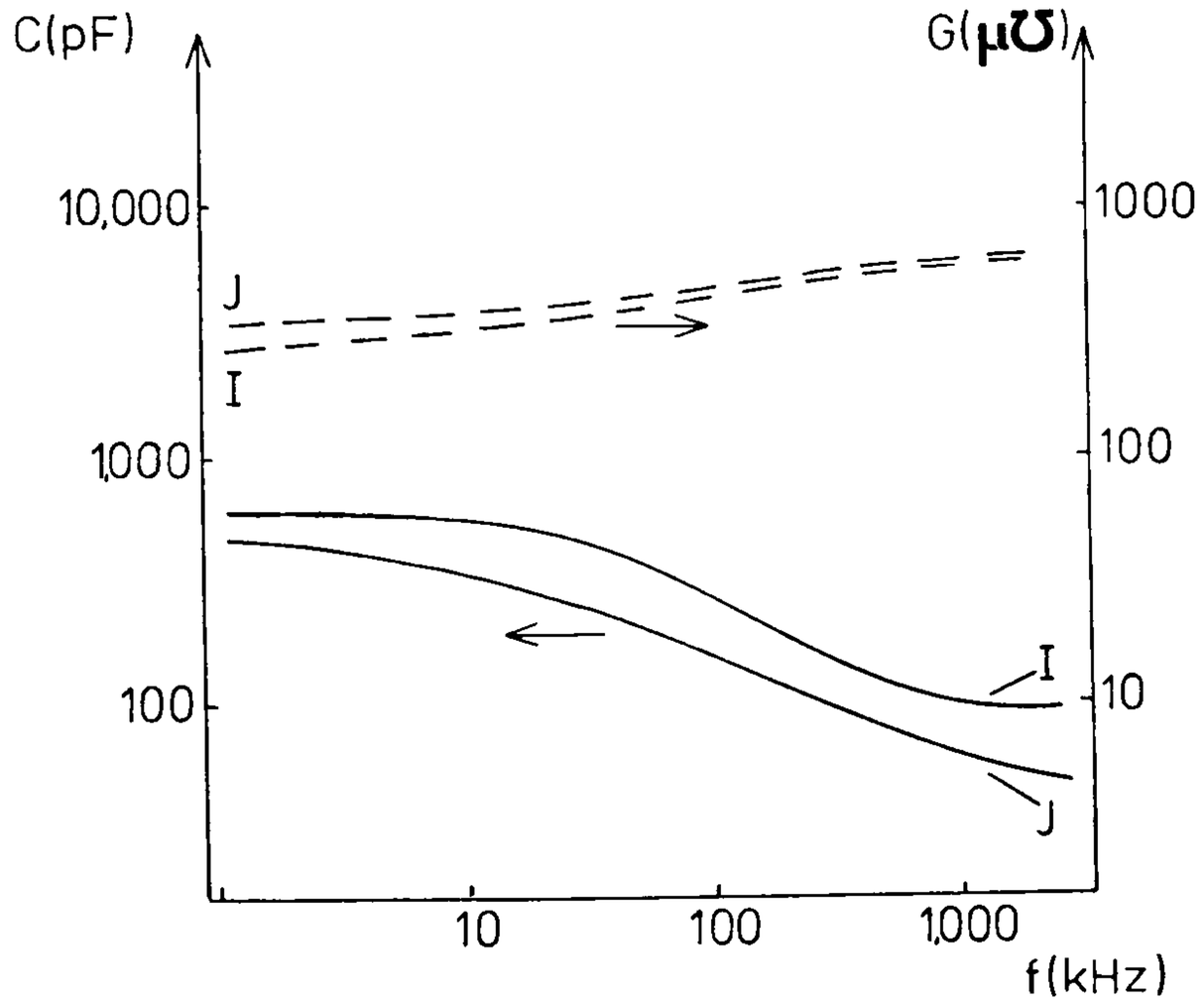


FIGURE 56

Log (C) versus Log (f) for Device G

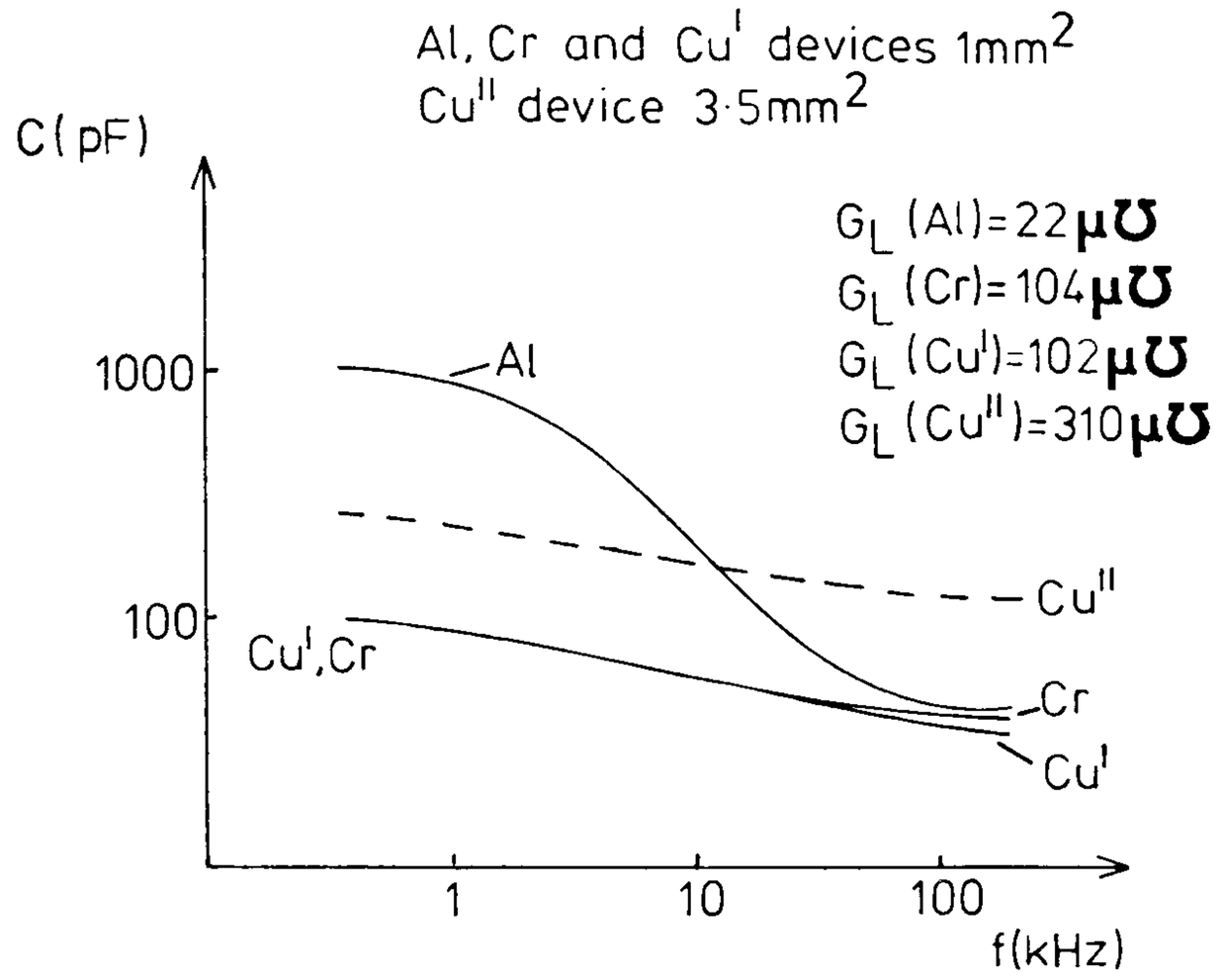
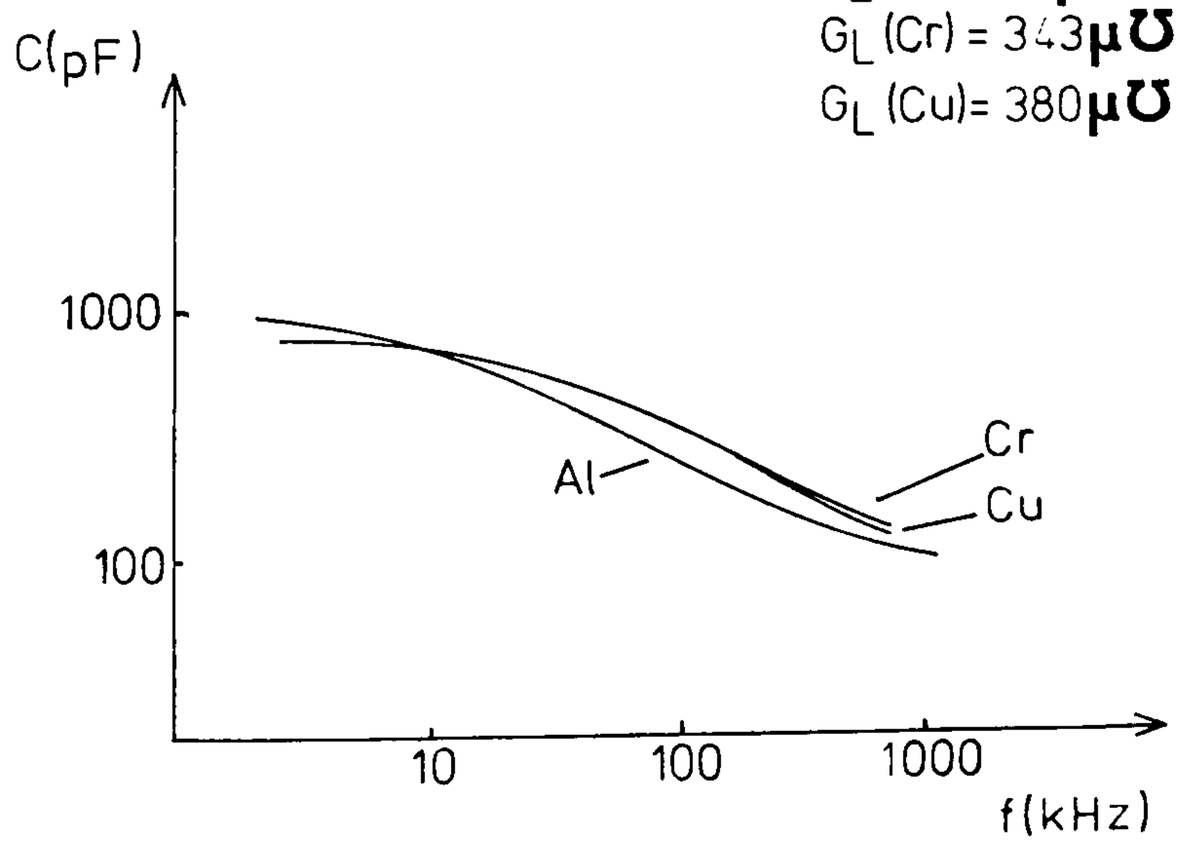


FIGURE 57

Log (C) versus Log (f) for Device I



$$\epsilon_{eff} = \frac{C_2 d}{A \epsilon_o} \qquad \sigma_{eff} = \frac{G_2 d}{A}$$

where d is the thickness of the film, A is the contact area, and ϵ_o is the permittivity of free space.

ϵ_{eff} and σ_{eff} are calculated for each film and the results are also shown on Table I.

8.31 Effect of film thickness

Figures 58 and 59 show the correspondence between film thickness and C_2 and G_2 respectively for all devices with Copper contacts, regardless of the other fabrication variables. The general trend is the expected relationship - both C_2 and G_2 being inversely proportional to film thickness. The broken lines in Figures 58 and 59 correspond to

$$C_2 = \epsilon_o \epsilon_{eff} \frac{A}{d} \quad \text{and} \quad G_2 = \sigma_{eff} \frac{A}{d}$$

$$\text{where } \epsilon_{eff} = 54 \quad \text{and} \quad \sigma_{eff} = 1100\ \mu\mho/m$$

Conductance shows a greater deviation from the expected relationship for thinner films, and the thinner films appear to have higher conductivity than the thicker films.

Apart from devices B and C, the capacitance corresponds closely to the expected trend. Devices B and C are special only in their high substrate temperature during condensation, and this will be shown in Section 8.35 to affect ϵ_{eff} significantly. The high absolute value of ϵ_{eff} (ϵ_r for CdS has a maximum of 11 at low frequencies) will be discussed in Section 8.36.

The results of this section show that in general, C_2 and G_2

FIGURE 58

C_2 versus Film Thickness

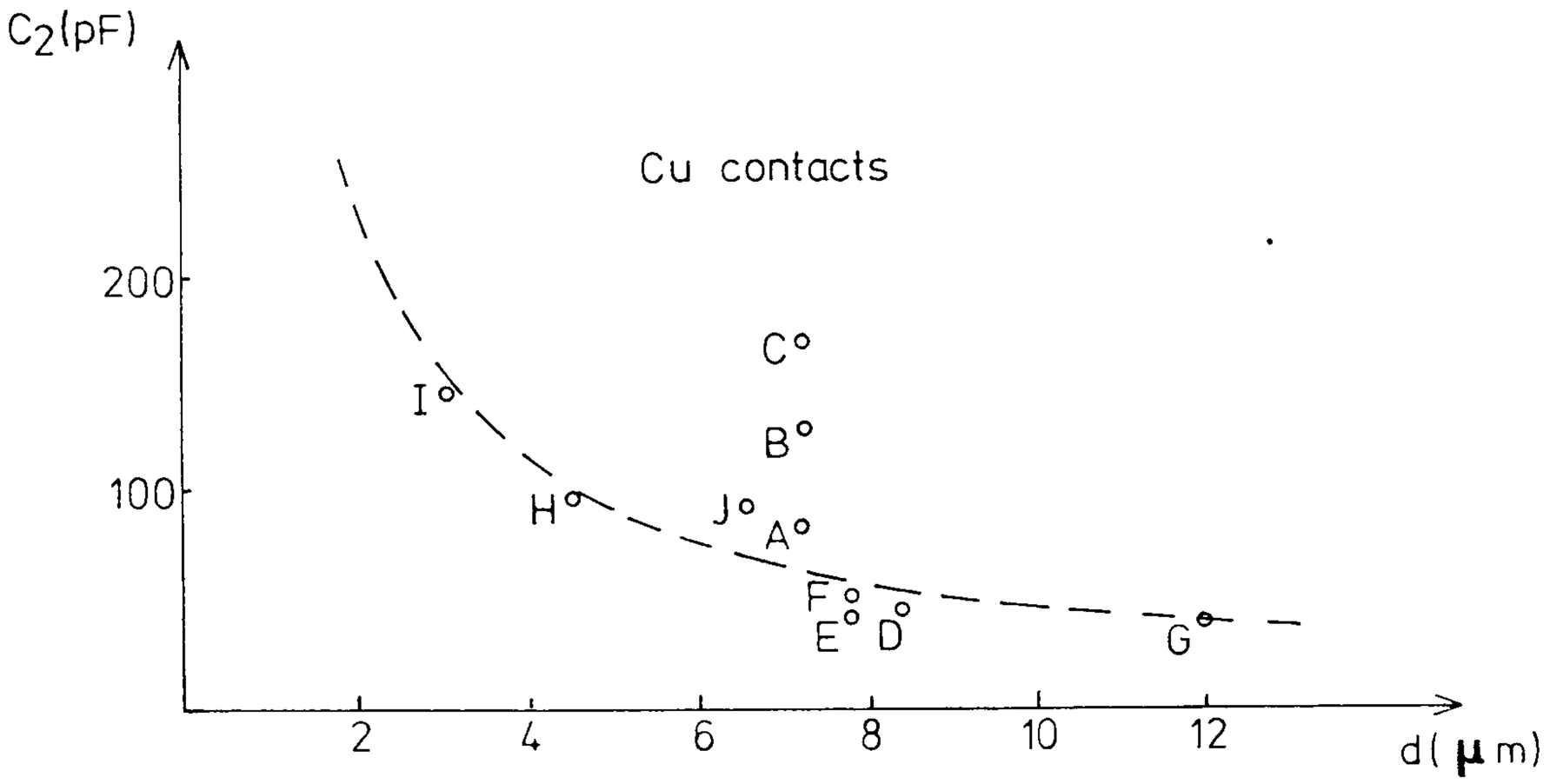
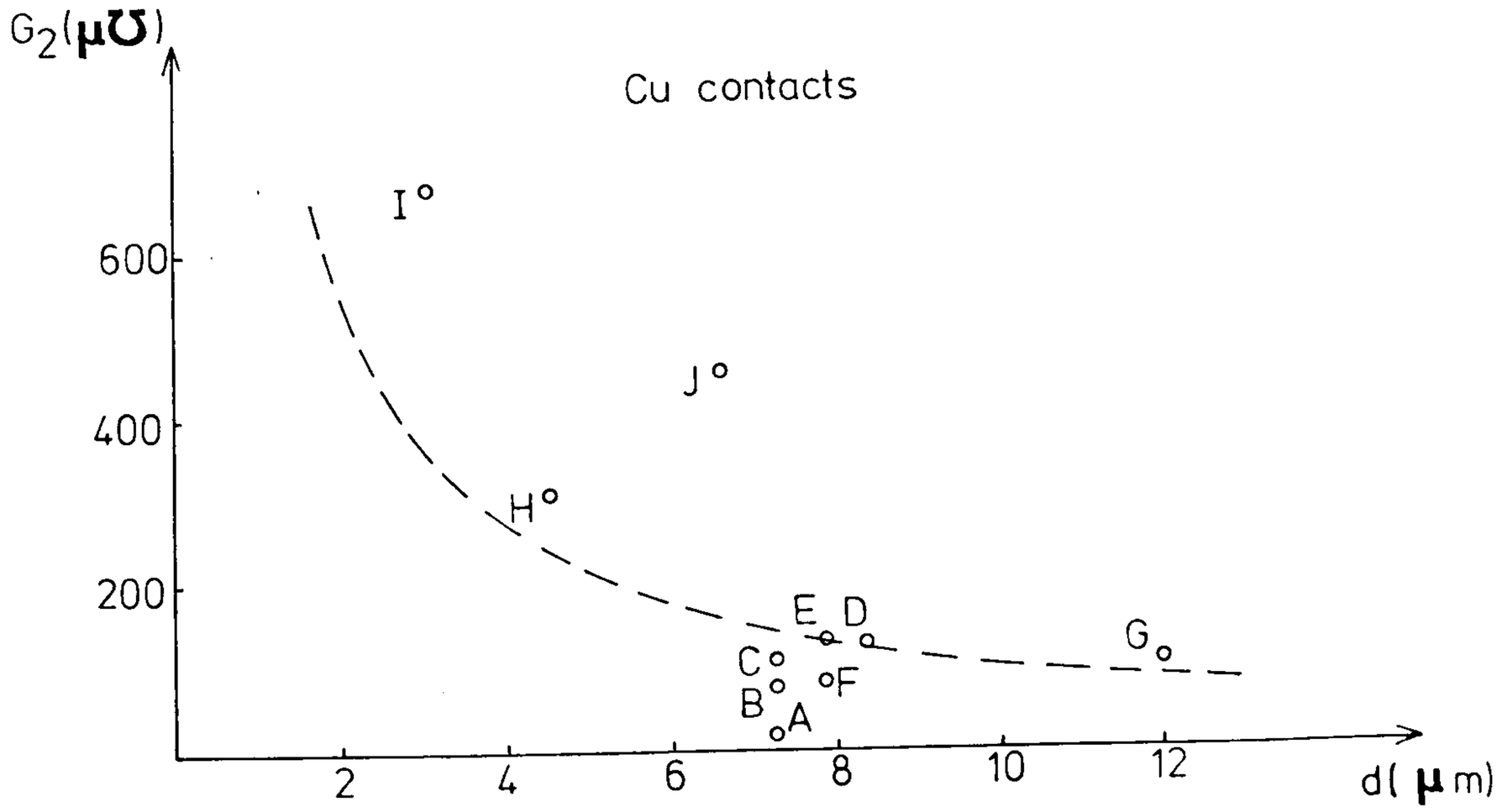


FIGURE 59

G_2 versus Film Thickness



represent the electrical parameters of the film. The results also show that all the other fabrication variables, except possibly substrate temperature, do not have as strong an effect on C_2 and G_2 as film thickness.

8.32 Effect of substrate doping

Devices A, B and C in Table I appear to show increasing junction capacitance, C_1, as a result of increased substrate doping. This is consistent with the theory that a junction exists between the Germanium substrate and the interface region.

If the film evaporated simultaneously on all three substrates was identical, and the electrical contact to all three was also identical, it would be expected that C_2 and G_2 for all three devices would be identical. However, a clear trend is observed of ϵ_{eff} and σ_{eff} increasing as substrate doping increases. This indicates that

a) doping of the substrate affects the growth and therefore the electrical characteristics of the film;

or b) doping of the substrate affects the electrical contact between substrate and film;

or c) both a) and b) apply.

8.33 Effect of condensation rate

Figures 60 and 61 show ϵ_{eff} and σ_{eff} as functions of the film condensation rate for all devices with Copper contacts.

Devices H, I and J have similar substrates, substrate temperatures and contacts. By comparing ϵ_{eff} for these three devices it can be seen that there is only a weak dependence on the condensation rate over the range 270Å/min to 2640Å/min. σ_{eff}, however, shows a stronger dependence - a significant increase in conductivity with increasing condensation rate.

FIGURE 60
ε_{eff} versus Condensation Rate

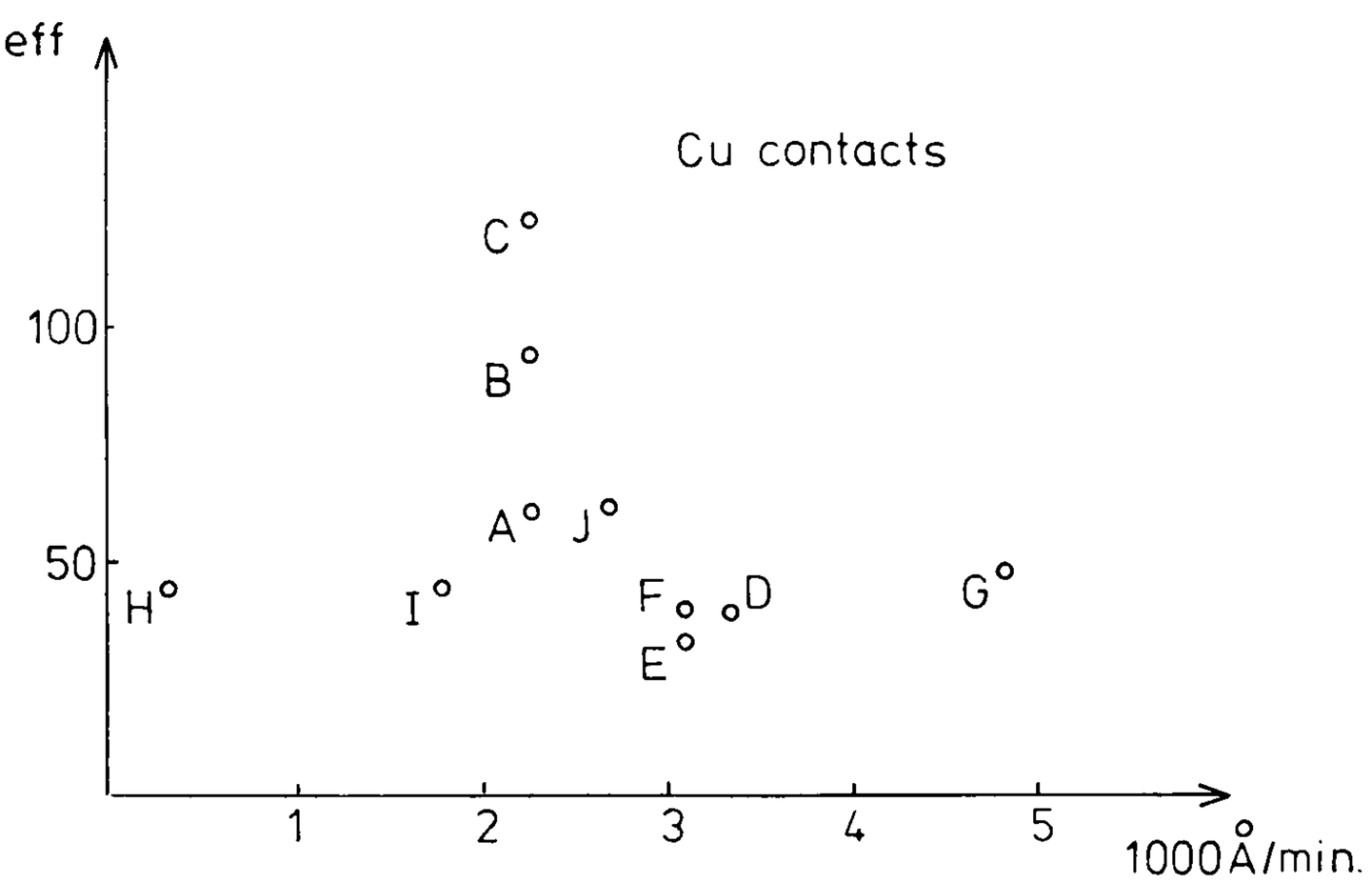
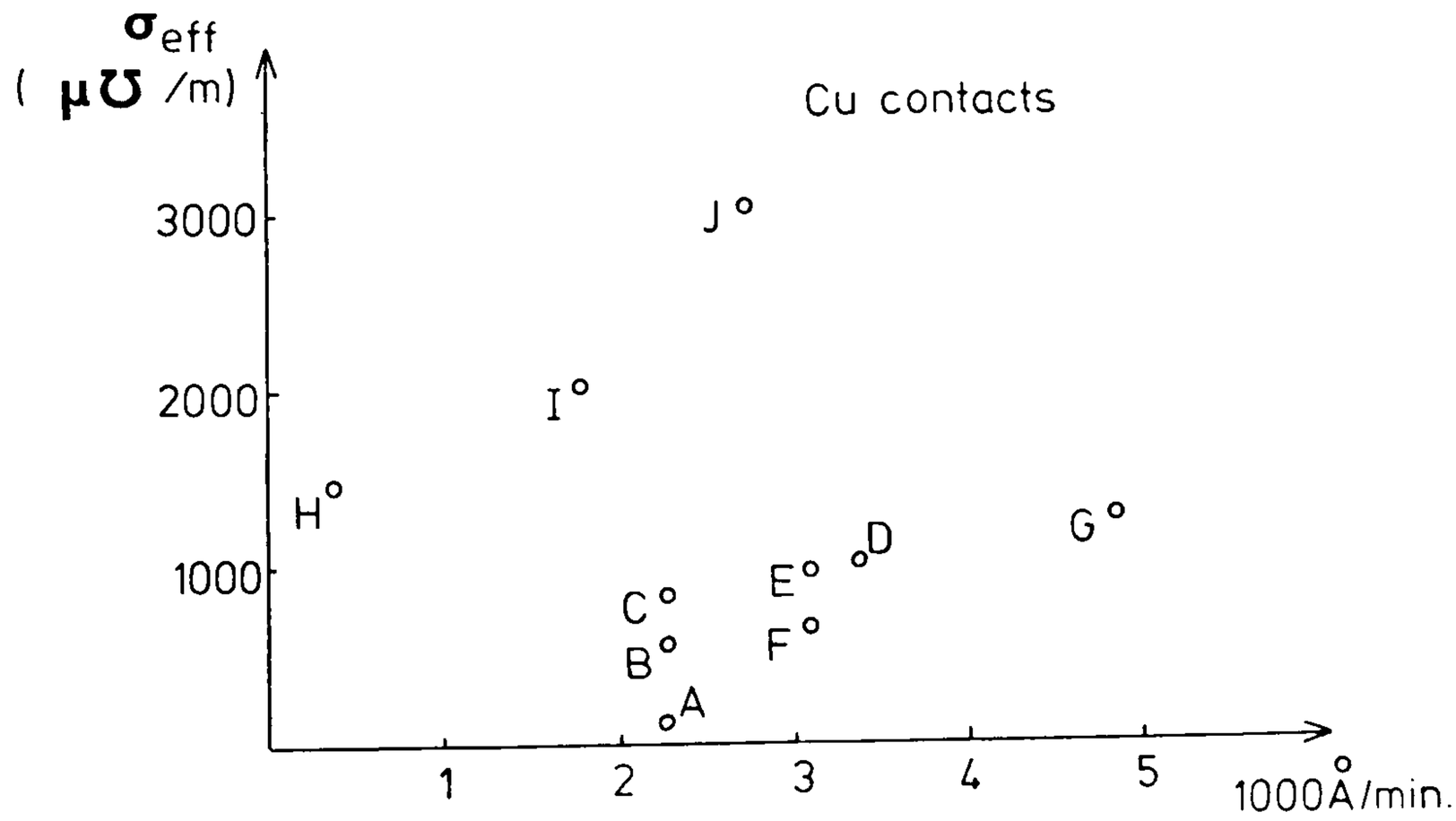


FIGURE 61
σ_{eff} versus Condensation Rate



From Chapter 3 it is known that film structure depends inter alia on condensation rate. When the film structure changes, its electrical parameters and the effect of electrical contacts to the film also change, so that it is not possible to deduce the causes of the observed trend from this evidence alone.

8.34 Effect of contact type

Samples G and I each have three types of contact to the CdS, viz. Copper, Aluminium and Chromium. Sample G has a substrate temperature of 65°C during the film evaporation and Sample I a temperature of 172°C.

It can be seen from Table I that the Copper and Chromium contacts have a similar effect on both samples, but Aluminium contacts result in a higher, low frequency capacitance and a much lower conductivity. Not only are C_1 and G_1 affected by the use of Aluminium contacts instead of Copper or Chromium, but also ϵ_{eff} and σ_{eff}. This is an indication that

a) ϵ_{eff} and σ_{eff} do not necessarily represent the permittivity and conductivity of the film alone:

b) Aluminium is making more of a rectifying contact to the CdS than are the Copper and Chromium. This is possibly due to the formation of an Aluminium Oxide layer on the surface of the CdS film:[77]

c) the Aluminium rectifying barrier - in comparison with the Copper and Chromium - is larger for lower substrate temperatures.

8.35 Effect of substrate temperature

Figures 62 and 63 show the relationship between substrate temperature and ϵ_{eff} and σ_{eff} respectively.

FIGURE 62
ε_{eff} versus Substrate Temperature

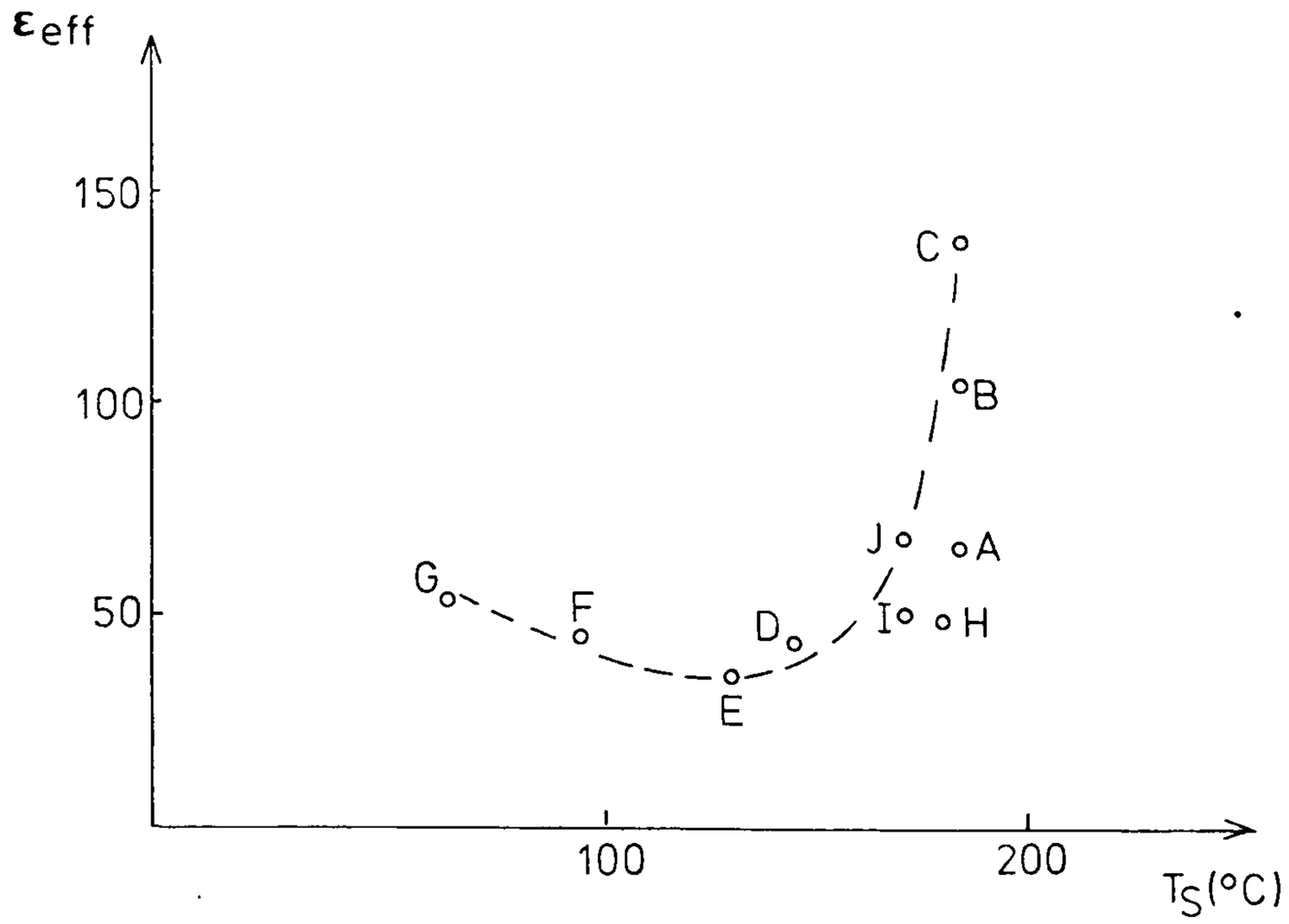
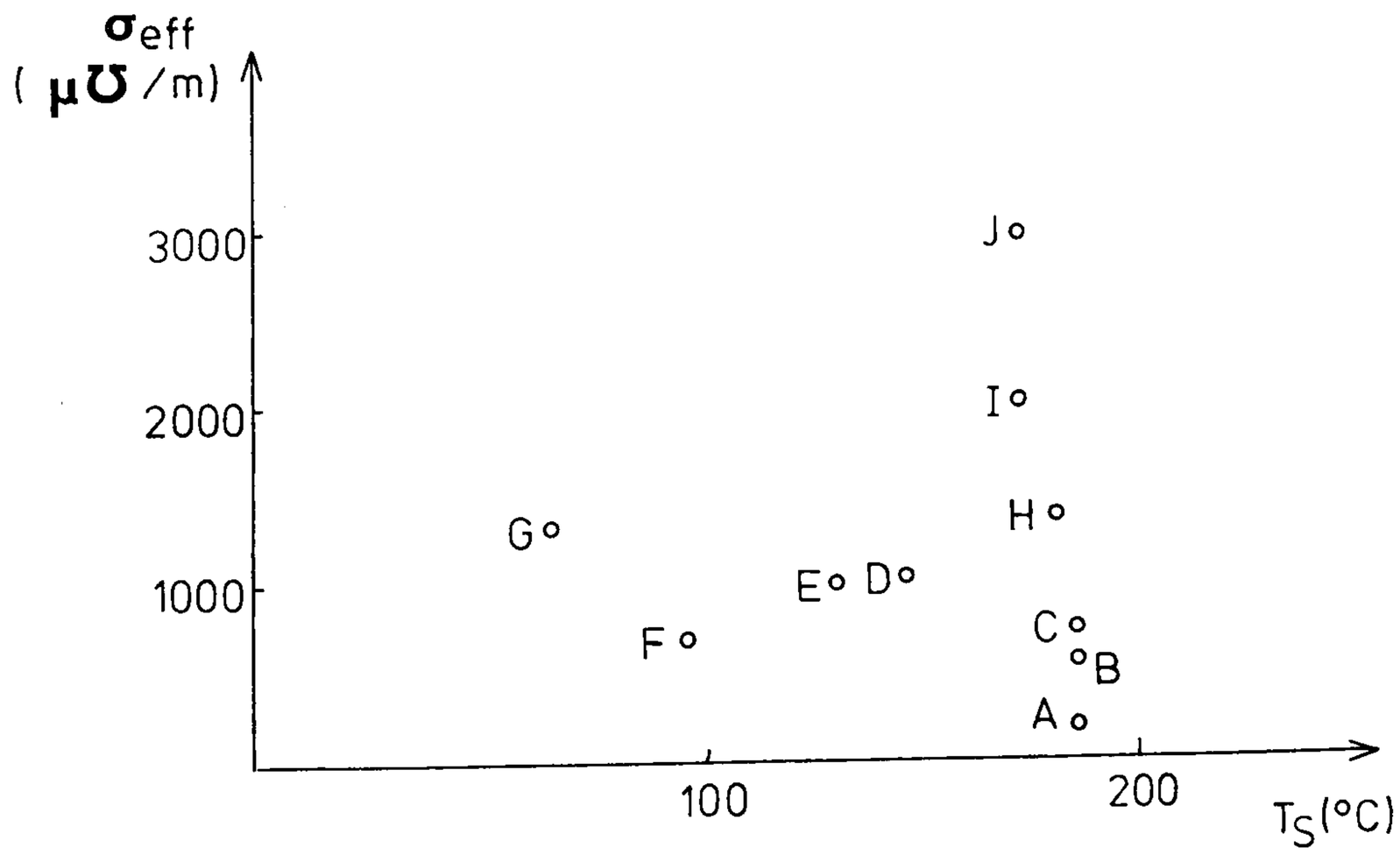


FIGURE 63
σ_{eff} versus Substrate Temperature



Devices D, E and F have similar condensation rates, thicknesses, substrates and contacts. Comparing their ϵ_{eff} and σ_{eff} there appears to be no strong dependence on substrate temperature. If from Section 8.33 we can assume only a weak dependence of ϵ_{eff} on condensation rate, then Devices C, G and J can be added for comparison. A clear trend can now be observed, ϵ_{eff} decreases to a minimum near 130°C and then increases at an increasing rate.

8.36 Discussion

It has been shown that C_2 and G_2 are dependent on film thickness in such a way as to suggest that they represent the capacitance and conductance of the CdS film. The effective permittivity calculated for the CdS films however, is as much as twelve times the permittivity of CdS, i.e. $\epsilon_r(CdS) = 11$ at low frequency.

The metal contact to CdS film has been shown to affect ϵ_{eff} and σ_{eff} significantly. If Copper does not make a purely ohmic contact to the CdS film, then the impedance of this barrier can increase ϵ_{eff} and decrease σ_{eff}. But if the impedance of this barrier is significant in comparison with the whole CdS film then ϵ_{eff} and σ_{eff} would not be directly dependent on film thickness.

The effective permittivity of a film can be increased[106] if the film contains regions of differing conductivities. For example, consider a film with two regions - Region 1 is a fraction x of the whole volume of the film and has a conductivity σ_1, and Region 2 makes up the rest of the film and has a conductivity σ_2. From Appendix IV at frequencies less than f_1

$$\epsilon_{eff} = \epsilon_r \frac{\sigma_1^2(1-x) + \sigma_2^2 x}{(\sigma_1(1-x) + \sigma_2 x)^2}, \qquad \sigma_{eff} = \frac{\sigma_1 \sigma_2}{\sigma_1(1-x) + \sigma_2 x}$$

The effective impedance of the film can approximate to the impedance of the fraction of the film which has low conductivity, i.e. (1-x). If $\sigma_1 >> \sigma_2$ and $\sigma_1(1-x) >> \sigma_2 x$ then

$$\epsilon_{eff} \approx \frac{\epsilon_r}{1-x}, \qquad \sigma_{eff} \approx \frac{\sigma_2}{1-x}$$

$$\text{and} \quad f_1 \approx \frac{(\sigma_1 \sigma_2 (1-x))^{\frac{1}{2}}}{2\pi \epsilon_o \epsilon_r}$$

For example, if $\epsilon_{eff} = 12\ \epsilon_r$, then this film would have 8.3% of its volume made up of the low conductivity region.

The dependence of the overall capacitance and conductance of such a film on film thickness is a function of the distribution of these conductivity regions. There are three simple types of distribution.

a) Evenly distributed conductivity regions. In this case the overall capacitance and conductance will be inversely proportional to the film thickness.

b) Initial layers of much higher conductance than subsequent layers. In this case the capacitance and conductance will tend to be inversely proportional to the film thickness as the thickness increases.

c) Initial layers of a much lower conductance than subsequent layers. In this case the capacitance and conductance would remain approximately constant with increasing film thickness.

In Section 8.31 the overall capacitance and conductance was

shown to be inversely proportional to film thickness as the thickness was increased. Thinner films appear to have higher conductivity, which may indicate that b) above is the type of distribution. The dependence of capacitance and conductance on thickness rules out c) but not necessarily a).

To sum up, the film appears to consist of regions of different conductivity. The initial layers may have a higher conductivity than subsequent layers and a mixture of conductivities exists within each layer. The theory for the simplest model predicts that a film, which has $\epsilon_{eff} = 54$ has a high conductivity region in 80% of its volume.

Regions of different phases and conductivities are commonly observed in CdS films - as discussed in Chapters 3 and 4. Typically the layers of film nearest to the substrate have the highest resistivity.[5,35] The results in this section indicate an opposite trend.

The effect of substrate temperature and condensation rate on the device characteristics is very complex unless the electrical contacts to the film can be made ohmic. The trends observed are likely to be a combination of the variation of the film's electrical characteristics and those of the Germanium and metal contacts.

8.40 SWITCHING STATE CHARACTERISTICS

In contrast to the virgin state characteristics the switching characteristics appear relatively independent of the fabrication parameters. Most of the criteria by which a device's switching characteristics can be judged depend directly on

the method of switching rather than the fabrication parameters of the device. The device switching is a result of the formation and destruction of filaments, which are not produced during fabrication.

Devices A to J could be made to switch - some more easily than others and some for longer periods than others. The following observations were made

a) Devices with CdS films less than 2μm thick only switch a few times before assuming a permanent very low resistance "ON" state.

b) Devices with metal contacts to the CdS less than 0.5μm thick could only be switched a few times before assuming a permanent very low resistance "ON" state.

c) Devices with Germanium substrates doped below $10^{16} cm^{-3}$ required higher forming voltages and higher switching currents.

b) has been discussed previously in relation to the efficiency of the electrodes in dissipating the heat produced during filament formation and destruction. The causes of a) and c) are not known at present.

No dependence of R_{ON}, R_{OFF}, I_{Rmax} or I_{THF} on the condensation parameters was identified, but this was expected as the current flow was filamentary even in the OFF state.

A dependence of V_{TF} on the condensation parameters was expected as this factor was dependent on film thickness and electron mobility, which in turn was dependent on the condensation parameters. However, no clear trend was discerned from the results. This may be due to the fact that electron

mobility is a complex function of all the condensation parameters, as discussed in Chapter 4.

CHAPTER 9

9.00 CONCLUSIONS

This work has shown that the structure of the CdS films grown is typical of evaporated semi-conductor films. The CdS films became more epitaxial with increasing film thickness and substrate temperature and with decreasing condensation rate. The CdS films contain both sphalerite and wurzite phases - the sphalerite phase dominating at high substrate temperatures and for thicker films. The films are columnar and crystallite size increases with increasing substrate temperature and film thickness.

Two critical parameters of CdS condensation have been identified and measured. The "sticking coefficient" for CdS on glass or Germanium was measured to be 100% up to 200°C and decreasing below 5% at temperatures above 300°C. The critical impinging rate for condensation of CdS on to NaCl at 200°C was measured to be 140 ± 60Å/min.

It has been concluded that the film's structural quality could be improved by the use of the "three temperature" rather than the single source method of evaporation. The "three temperature" method allows greater control of the condensation rate and the proportions of Cadmium and Sulphur in the vapour. High quality films require low condensation rates, higher vacuums and greater standards of cleanliness. The film structure could be further improved if the Germanium substrate surface was free of all impurities and this can be accomplished

by vacuum cleaving the substrate prior to CdS condensation.

The device would be improved if the Copper contact could be evaporated on to the CdS film without exposure to the atmosphere.

Improvements to the quality of the CdS film and the device fabrication techniques will doubtless improve the reproducibility of the device's virgin state characteristics, but it is open to debate whether the switching characteristics would be equally improved. The production of a uniform film and the removal of impurities from the junction regions may abolish the need to form the device into a switchable state.

Device switching appears to depend on the complex interaction between applied voltage, external circuit series resistance, and the thermodynamics of the device and its surroundings. The change of conductance observed as a result of switching is attributed to the formation and destruction of highly conductive filaments within the CdS film. Threshold switching is the result of the formation of temporary filaments by electrical breakdown, and memory switching results from the formation of permanent filaments by the slower recrystallisation which follows electrical breakdown.

The electrical characteristics of the virgin and OFF states depend on the electrical properties of the CdS film, but the ON state characteristics depend on the electrical properties of the filament formed by switching.

Two theories are offered to explain the polarity of the memory switching observed. Both theories assume that switching is

initiated by high temperatures near the anode where the electrical field is greatest. The non-uniformity of the CdS film could lead to higher heat dissipation at one electrode than at the other at the same but reverse bias. On the other hand, the electrodes have different thermal conduction efficiencies, and this means that one electrode can limit the temperature of the CdS more effectively than the other.

It was expected that by changing the device fabrication parameters, e.g. substrate temperature, the switching characteristics would be modified - but this has been shown not to be the case for the range of devices tested. It has been found that switching characteristics are more dependent on the method of switching than on fabrication parameters. The virgin state, on the other hand, shows a clear dependence on the fabrication parameters.

The work has shown that epitaxial, evaporated, CdS films can support switching in an identical manner to amorphous glass devices in spite of considerable physical and electrical differences.

APPENDIX I

The full equations for the overall admittance of two regions in series each with a parallel capacitance and conductance

Region 1 has capacitance C_1 conductance G_1

Region 2 has capacitance C_2 conductance G_2

The overall admittance $Y_T = G_T + jwC_T$

$$G_T = \frac{(w/w_1)^2 + 1}{(w/w_2)^2 + 1} \cdot \frac{G_1 G_2}{G_1 + G_2}$$

$$C_T = \frac{(w/w_3)^2 + 1}{(w/w_2)^2 + 1} \cdot \frac{G_2^2 C_1 + G_1^2 C_2}{(G_1 + G_2)^2}$$

$$w_1 = \left[\frac{G_1 G_2 (G_1 + G_2)}{G_2 C_1^2 + G_1 C_2^2}\right]^{\frac{1}{2}}$$

$$w_2 = \frac{G_1 + G_2}{C_1 + C_2}$$

$$w_3 = \left[\frac{G_2^2 C_1 + G_1^2 C_2}{C_1 C_2 (C_1 + C_2)}\right]^{\frac{1}{2}}$$

Assuming positive values for the parameters C_1, C_2, G_1 and G_2 and $C_1 \geq C_2$ and $G_1 \leq G_2$

$$w_1 \leq w_2 \leq w_3$$

At low frequency $w \ll w_1$

$$G_T(w_{low}) = \frac{G_1 G_2}{G_1 + G_2}$$

$$C_T(w_{low}) = \frac{G_2^2 C_1 + G_1^2 C_2}{(G_1 + G_2)^2}$$

At high frequency $w >> w_3$

$$G_T(w_{high}) = \frac{C_2^2 G_1 + C_1^2 G_2}{(C_1 + C_2)^2}$$

$$C_T(w_{high}) = \frac{C_1 C_2}{C_1 + C_2}$$

APPENDIX II

The full equations for the admittance of two regions in series one with parallel capacitance and conductance and the other with only conductance.

Region T has capacitance C_T conductance G_T
Region S has conductance G_S

The overall admittance $Y_D = G_D + jwC_D$

$$G_D = \frac{(w/w_4)^2 + 1}{(w/w_5)^2 + 1} \cdot \frac{G_T G_S}{G_T + G_S}$$

$$C_D = \frac{1}{(w/w_5)^2 + 1} \cdot \frac{C_T G_S^2}{(G_T + G_S)^2}$$

$$w_4 = \left[\frac{G_S(G_S + G_T)}{C_T^2}\right]^{\frac{1}{2}}$$

$$w_5 = \frac{G_T + G_S}{C_T}$$

APPENDIX III

Capacitance of a metal semiconductor junction with two doping regions

Consider a metal semiconductor junction with doping of N_a from the interface to x_a and doping of N_b greater than x_a. From Poisson's equation for the depletion region of n-type semiconductor

$$0 \leq x \leq x_a \quad \frac{d^2\psi}{dx^2} = -\frac{e}{\epsilon} N_a \quad , \quad x \geq x_a \quad \frac{d^2\psi}{dx^2} = -\frac{e}{\epsilon} N_b$$

where ψ is the potential and N_a and N_b are donor densities.

Integrating gives

$$0 \leq x \leq x_a \quad \frac{d\psi}{dx} = -\frac{e}{\epsilon} N_a(x + A) \quad , \quad x \geq x_a \quad \frac{d\psi}{dx} = -\frac{e}{\epsilon} N_b(x + B)$$

The boundary conditions are (i) $\frac{d\psi}{dx} = 0$ at x_λ, i.e. the electric field is zero just outside the depletion region, and (ii) $\frac{d\psi}{dx}$ is continuous at x_a. From these boundaries conditions we find

$$A = x_a \left(\frac{N_b}{N_a} - 1\right) - x_\lambda \frac{N_b}{N_a}$$

and $$B = -x_\lambda$$

Integrating $\frac{d\psi}{dx}$ gives

$$0 \leq x \leq x_a \quad \psi = -\frac{e}{\epsilon} N_a\left(\frac{x^2}{2} + Ax + C'\right) \quad , \quad x \geq x_a \quad \psi = -\frac{e}{\epsilon} N_b\left(\frac{x^2}{2} + Bx + D\right)$$

The boundary conditions are (i) $\psi = 0$ at $x = 0$, i.e. the potential at the interface is assumed zero. (ii) ψ is continuous at x_a, and (iii) $\psi = V_s$ at $x = x_\lambda$.

Applying these boundary conditions we find

$$C' = 0 \quad \text{and} \quad D = \frac{x_\lambda^2}{2} - \frac{\epsilon V_s}{e N_b}$$

This gives

$$x_\lambda = \left[\frac{2 V_s \epsilon}{e N_b} + x_a^2 \left(1 - \frac{N_a}{N_b}\right) \right]^{\frac{1}{2}}$$

The capacitance per unit area can be calculated from

$$C = \frac{\epsilon}{x_\lambda} = \left(\frac{e \epsilon N_b}{2}\right)^{\frac{1}{2}} \left(V_s + \frac{e x_a^2}{2\epsilon} (N_b - N_a)\right)^{-\frac{1}{2}}$$

V_s the potential at x_λ is the sum of the diffusion potential V_D and the applied voltage - V (forward bias designated positive)

$$\text{thus} \quad C = \left(\frac{e \epsilon N_b}{2}\right)^{\frac{1}{2}} \left(V_D - V + \frac{e x_a^2}{2\epsilon} (N_b - N_a)\right)^{-\frac{1}{2}} \qquad \text{——— a)}$$

The above equation simplifies to the classical equation for metal-semiconductor junction capacitance for $x_a = 0$ or $N_a = N_b$.
The equation is only valid for applied voltages which ensure $x_\lambda \geq x_a$.

If $x_\lambda \leq x_a$ then $C = \left(\frac{e \epsilon N_a}{2}\right)^{\frac{1}{2}} \left(V_D' - V\right)^{\frac{1}{2}}$.

From equation a) $\qquad \frac{dC^{-2}}{dV} = \frac{2}{e \epsilon N_b} \qquad x_\lambda > x_a$

The slope of the C^{-2} versus V characteristic is determined by the doping of the semiconductor for $x > x_a$. $C^{-2} = 0$ however does not directly allow the diffusion voltage to be calculated.
At $C^{-2} = 0$ equation a) simplifies to

$$V_D = V_I + \frac{e x_a^2}{2\epsilon} (N_a - N_b)$$

Experimentally V_I can be determined but unless the capacitance - voltage characteristic is known for voltages which result in $x_\lambda < x_a$ then V_D cannot be deduced.

APPENDIX IV

Effective permittivity and conductivity of material with two regions of differing conductivities.

Consider a material of thickness d sandwiched between metal contacts of area A. The material consists of two types of region - a fraction x has σ_1 conductivity and the remainder, (1 - x), has σ_2 conductivity - the permittivity ϵ_r is the same for both regions. The total capacitance, C_T, and conductance, G_T, between the two contacts is frequency dependent. The two regions will be assumed to be uniformly distributed in the plane of the contacts - the distribution normal to the plane need not be defined.

The total admittance of the film will be the addition of Y_1 and Y_2, which represent the sum of all the Regions 1 and 2.

$$Y_1 = \sigma_1 \frac{A}{xd} + jw\epsilon \frac{A}{xd}, \quad Y_2 = \sigma_2 \frac{A}{(1-x)d} + jw\epsilon \frac{A}{(1-x)d}$$

Then the total capacitance is

$$C_T = \frac{(w/w_3)^2 + 1}{(w/w_2)^2 + 1} \cdot \frac{\epsilon A}{d} \cdot \frac{\sigma_1{}^2(1-x) + \sigma_2{}^2 x}{(\sigma_1(1-x) + \sigma_2 x)^2}$$

and the total conductance is

$$G_T = \frac{(w/w_1)^2 + 1}{(w/w_2)^2 + 1} \cdot \frac{A}{d} \cdot \frac{\sigma_1\sigma_2}{\sigma_1(1-x) + \sigma_2 x}$$

w_1, w_2 and w_3 are constants dependent on σ_1, σ_2 and ϵ.

The frequency, f_1, at which frequency dependence begins to show

$$f_1 = \frac{w_1}{2\pi} = \frac{1}{2\pi\epsilon}\left[\frac{\sigma_1\sigma_2(\sigma_1(1-x) + \sigma_2 x)}{\sigma_2(1-x) + \sigma_1 x}\right]^{\frac{1}{2}}$$

If $f < f_1$ the frequency dependent part of the equations for C_T and G_T can be set to 1.

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