"Design, fabrication and testing of a novel W-Band monolithic millimetre-wave integrated circuit mixer"

A thesis submitted to the Faculty of Engineering of the University of Glasgow for the degree of Doctor of Philosophy

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Abstract

This thesis presents the design, fabrication and testing of a novel 94GHz monolithic millimetre-wave integrated circuit mixer. The motivation for this work was to develop a high-yield, simple, circuit design using a monolithic approach to enable ultimate integration with a low noise amplifier to form a downconverter. The novel mixer design used Coplanar Waveguide (CPW) and Slotline as the transmission line elements and Gallium Arsenide pseudomorphic High Electron Mobility Transistor diodes as the mixing elements.

An extensive literature search was done to identify what had already been done at 94GHz. From this a mixer circuit was designed and a mmWIC fabrication process was developed from the existing University of Glasgow FET process. The use of a CPW-Slotline transition, used to achieve phase difference between the RF and LO signals at the mixing diodes, is reported for the first time in a monolithic circuit at W-Band.

Many different diodes were fabricated and tested and equivalent circuit models were extracted from s-parameter measurements. The factors which affect the diode circuit models such as diode dimensions, substrate choice and fabrication procedure were varied. A comparison was made between expected and measured values.

The mmWIC fabrication process used electron beam lithography, photolithography, wet/dry etching and both e-beam metal evaporation and electroplating. Several steps in the fabrication process were modified from the basic University of Glasgow FET process. Considerable time was spent on trying to minimise ohmic contact resistance through the use of different metallisations and anneal temperatures/times. The anode level was also considered very important in order to minimise diode parasitics, and a "pyramidal" shaped anode process using a tri-layer resist combination was successfully implemented. In addition, an extra layer of copolymer was included in the existing "T-gate" process to enable twice as much metal to be lifted-off thus reducing the effects of metallic resistance. An investigation of the possible effect of

elastic strain arising from the anode metallisation on the GaAs was undertaken and this showed that such strain was negligible.

Full characterisation of all the mmWIC passive circuit components (ie filters, capacitors and CPW-Slotline transitions) was done using s-parameter measurements. The final mixer circuit was tested using a W-Band network analyser as the RF signal and a Gunn oscillator as the LO source and the measured conversion loss of 10dB was comparable to other passive mixers presented in the literature. It was not possible to measure the noise figure of the mixer but some consideration was given to the possible sources/effects of system noise.

This mixer design could be easily integrated with a LNA or antenna to form a complete mmWIC downconverter. A new material structure was grown which would enable an optimum diode structure and an optimum FET structure to be monolithically integrated on the same substrate. However, insufficient time was available for implementation of such a circuit.

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Contents

Chapter 1

Introduction

1.1 Introduction

The research which constitutes this thesis was done with the aim of demonstrating a novel high frequency monolithic mixer design, capable of ultimate integration with a low noise amplifier to form a complete monolithic downconverter. Microwave and millimetre-wave monolithic integrated circuits (MMICs and mmWICs respectively) are ICs that are designed to operate in the frequency ranges from 1 to 30GHz (MMICs) and 30 to 300GHz (mmWICs). These circuits combine components such as capacitors, resistors, transmission lines, diodes and field-effect transistors (i.e. active and passive circuit functions) on a single substrate whereas the more commonly used hybrid circuit technology refers to transmission lines which are printed on a dielectric substrate (such as alumina) with chips and discrete components such as capacitors and resistors mounted thereon.

It is possible to "tune" hybrid circuits by, for example, taking out an individual transistor and replacing with another but as circuit complexity increases this creates many problems. Very little post-fabrication tuning is possible using monolithic circuits, so the monolithic approach requires two important criteria to be satisfied - a) right first time design; b) a fabrication process which has a high final electrical yield. MMICs and mmWICs have the same benefits for microwave systems designers that silicon VLSICs offer to low frequency digital system designers. The most obvious advantages are: elimination of parasitics due to packaging; ability to design individually both active and passive components; small size and weight; low costs for large volume production.

There are now many potential commercial applications for MMICs and mmWICs such as spectrum analysers, network analysers, mobile phones, home satellite systems, frequency synthesizers and medical equipment. Recently, the automotive

industry is an area where mmWICs are being used both in collision avoidance systems and intelligent cruise control and these applications are being actively pursued by Daimler Benz, Volkswagen, Siemens and Thomson in the USA, and NEC and Toyota in Japan [1.1,1.2,1.3,1.4]. Cellular telephone networks and personal communication networks operating in the frequency range around 1.8-2GHz and wireless local area networks are high volume markets whilst the applications of MMICs in satellite communications are many. Global positioning systems operate in the 1-2GHz frequency range and Direct Broadcast Satellite systems typically use a 12GHz Gallium Arsenide (GaAs) MMIC frequency downconverter. There is still much potential for the use of mmWICs in the military sector, where phased-array radar systems, electronic warfare, missile guidance, and signal intelligence are only some of the possible applications [1.5].

GaAs is preferred to Silicon for microwave/millimetre-wave ICs because of its greater electron mobility (resulting in faster device operation) and its semi-insulating properties which allow natural isolation of adjacent devices without the need for an isolation barrier (such as Silicon Dioxide). However, the costs of processing GaAs circuits are much greater than Silicon and these costs are further increased by the need to use high quality substrates (normally grown by molecular beam epitaxy (MBE) or metal-organic chemical vapour deposition (MOCVD)) for mmWICs. Indium Phosphide (InP) substrates are also used in the production of mmWICs and, although InP technology is not yet as mature as GaAs, these offer potentially higher device performance. The main disadvantages of InP substrates are that they are more expensive than GaAs, more fragile and have a relatively low Schottky barrier height with most metals (0.3-0.4eV).

Major MMIC manufacturers such as GEC and TRW make use of **microstrip** technology , typically with wafers thinned to around one hundred microns. Microstrip is a well characterised transmission line for use in MMICs but requires backside processing as illustrated in Figure 1. This is necessary in order to be able to ground components from the top to the bottom surface of the wafer. Connection is made through the substrate by means of a "via hole".

Coplanar Waveguide (CPW) is an alternative to microstrip and eliminates the need for via holes by having all conductors in the same plane - see Figure 1. Another advantage of CPW over microstrip can be seen by considering a given substrate, where the substrate height, dielectric constant (ε_r) and interconnect metallisation are fixed, and a 50 Ohm impedance is required. The CPW characteristic impedance is a function of the ratio of the central conductor width to gap width , and this can be maintained at a constant value whilst the dimensions of the gap/conductor are varied. This means that transmission lines can be made with dimensions similar to those of monolithic devices on semiconductor substrates, e.g. transistors and diodes. This is not possible using microstrip where, for the given substrate and interconnect metallisation, there is only one width of the signal line that will yield the desired 50 Ohm impedance. At the University of Glasgow there has been an ongoing project to characterise passive CPW components and to build a component library which should enable CPW-based MMICs to be manufactured with good correlation between actual and predicted results.

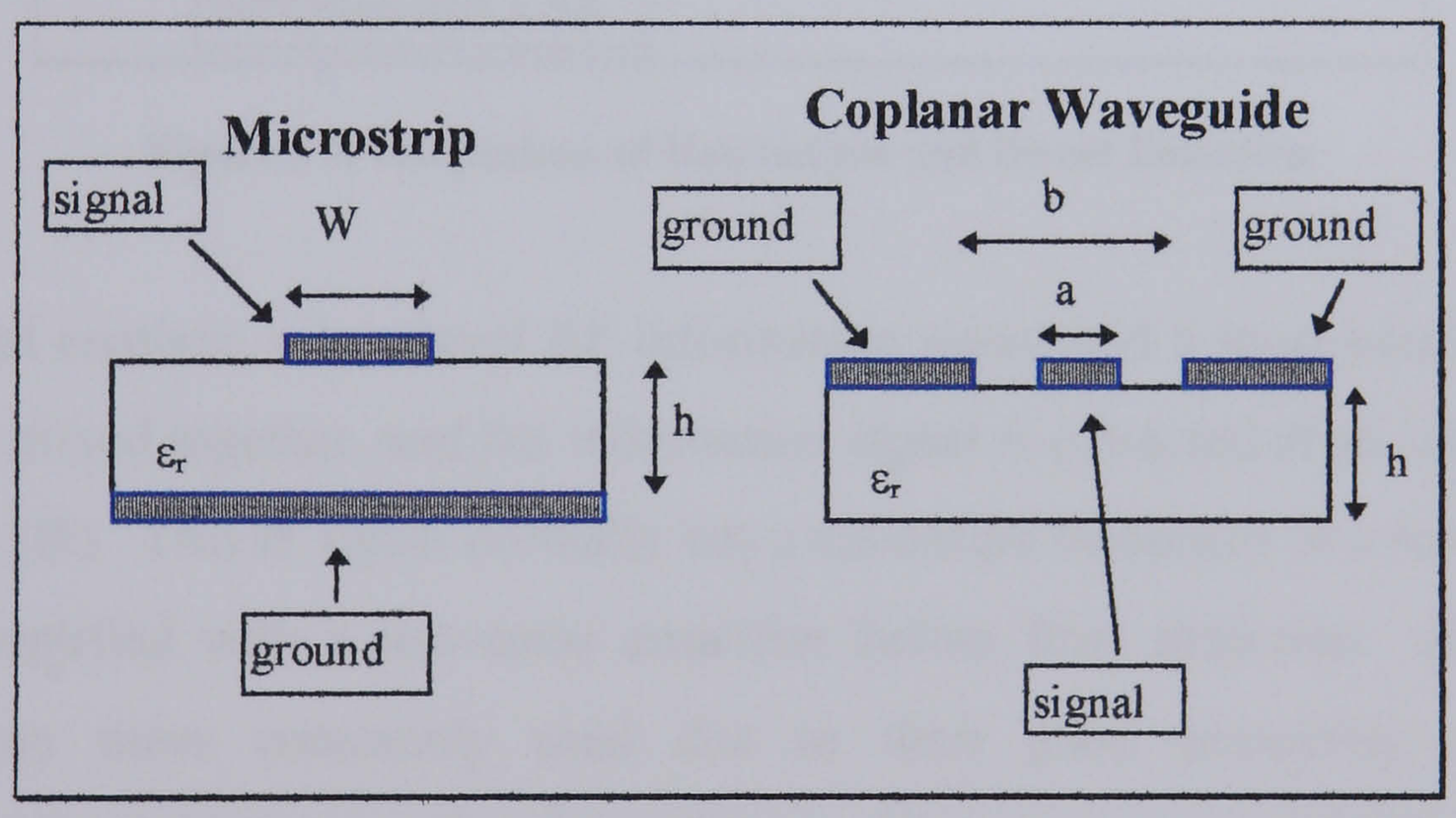

Figure 1 A comparison between microstrip and coplanar waveguide

1.2 MMIC/mmWIC Receivers

In MMIC/mmWIC receiver applications, the two most common ways of extracting the desired information from an incoming RF signal are : 1) Heterodyne detection 2) Direct Detection. These are illustrated below in Figure 2 and are explained as follows:

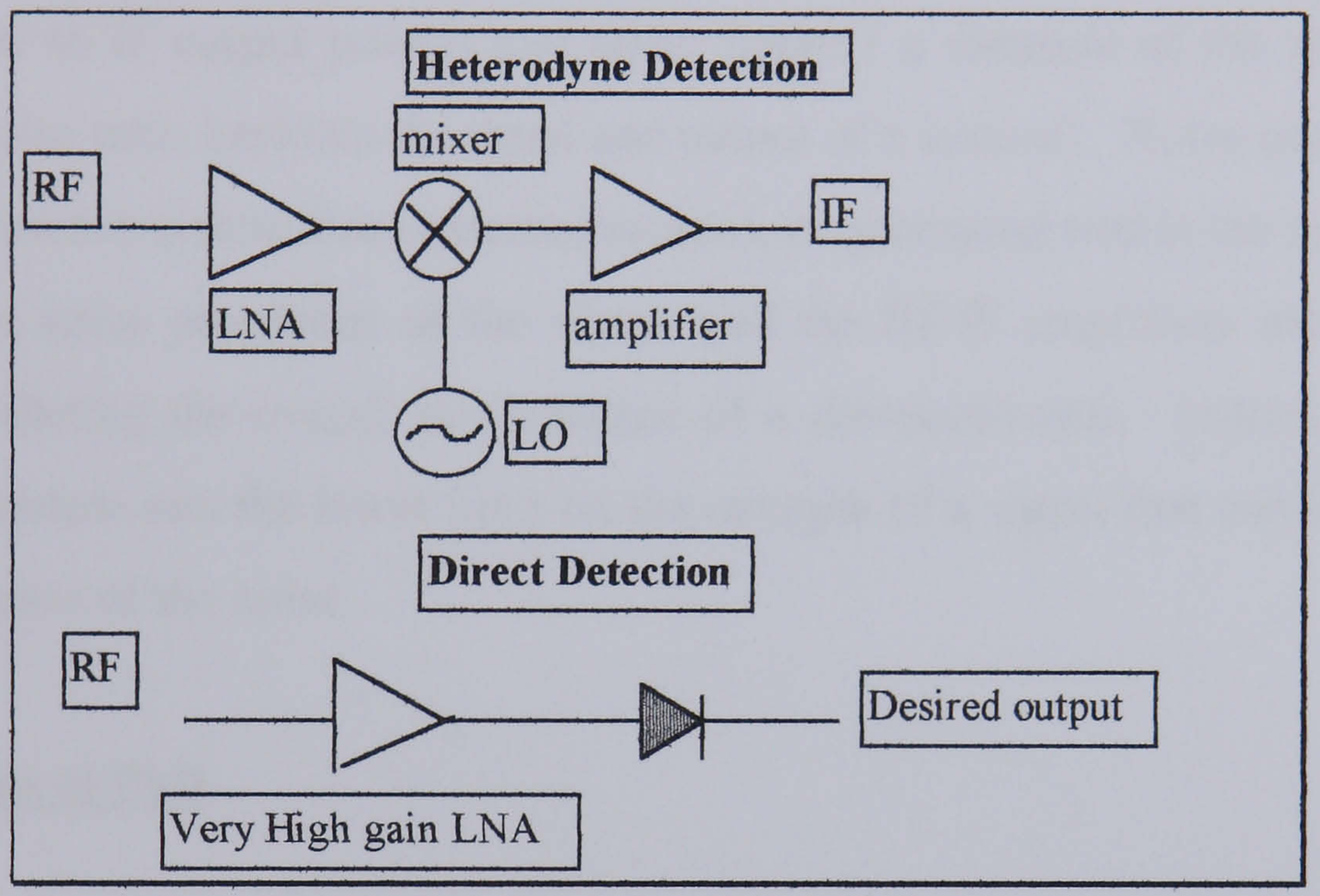

Figure 2 A comparison of Heterodyne and Direct Detection

In a typical receiver, a low-level RF information signal and a local oscillator (LO) signal are mixed together, and the information signal is extracted at an intermediate frequency (IF). This IF signal normally has a maximum frequency of a few GHz and can be amplified with a low-noise amplifier before final detection. Heterodyne systems are more commonly used due to their good sensitivity and noise characteristics and have the advantage of being able to tune over a band by changing the LO frequency, without the need for a high-gain, wideband amplifier.

The alternative to this form of receiver is the direct detection system. Such a system does not require LO power, has a wide bandwidth and is simple. However, Schottky-diode sensitivity is low. This can be improved by placing a high quality low noise amplifier (LNA) before the diode. The theory behind these two forms of detection is given in Chapter 2 on Mixer Theory/Design.

It was decided to use the heterodyne detection scheme for this project. The direct detection system requires a very high gain LNA before the diode detector and, since a considerable amount of research has already been done into designing such LNAs (see section 1.4), it was thought more useful to concentrate on mixer design.

Mixer performance is measured in terms of conversion loss (the ratio of available RF input power to IF output power) and noise figure (a measure of the reduction in signal-to-noise ratio between the input and output of a system). Noise can be passed into a microwave system from external sources, or generated within the system itself so both the noise properties of the mixer **and** the RF/IF amplifiers are important when considering the overall performance of a downconverter. Indeed, the noise level of a system sets the lower limit on the strength of a signal that can be detected in the presence of the noise.

1.3 Synopsis of PhD

The approach which was adopted during the course of this research project was to build upon the previous work done at the University of Glasgow towards the development of a CPW-based MMIC process for millimetre-wave frequencies. To this end, a novel mixer was designed for use at 94GHz, fabricated and tested. There is still much research ongoing towards the development of complete downconverter circuits which combine amplification and mixing on a single chip. The mixer circuit in this project used CPW and Slotline as the transmission line elements and also included GaAs pseudomorphic High Electron Mobility Transistor (pHEMT) diodes as the mixing components.

The specific frequency of 94GHz was chosen for this project as it is one of three "windows" in the electromagnetic spectrum where microwave/millimetre-wave signals are only attenuated slightly by the atmosphere. This is clearly evident in Figure 3, shown overleaf. As illustrated, microwave/millimetre-wave signals are attenuated by the atmosphere due to absorption by water vapour and molecular

oxygen. However, at the specific frequencies of 35, 94 and 140GHz this absorption is only 0.02, 0.1 and 0.2 dB/km respectively. Therefore, these frequencies have been used for communication systems such as millimetre-wave imaging systems (passive target seekers and weather surveillance), and vehicle collision avoidance systems. W-Band (75-110GHz) communication systems have larger RF bandwidth and better range resolution than systems operating at 35GHz. Since there are many reports of low noise amplifiers using GaAs pHEMT devices at 94GHz (see section 1.4), it was decided that this material structure and frequency should be used in the project.

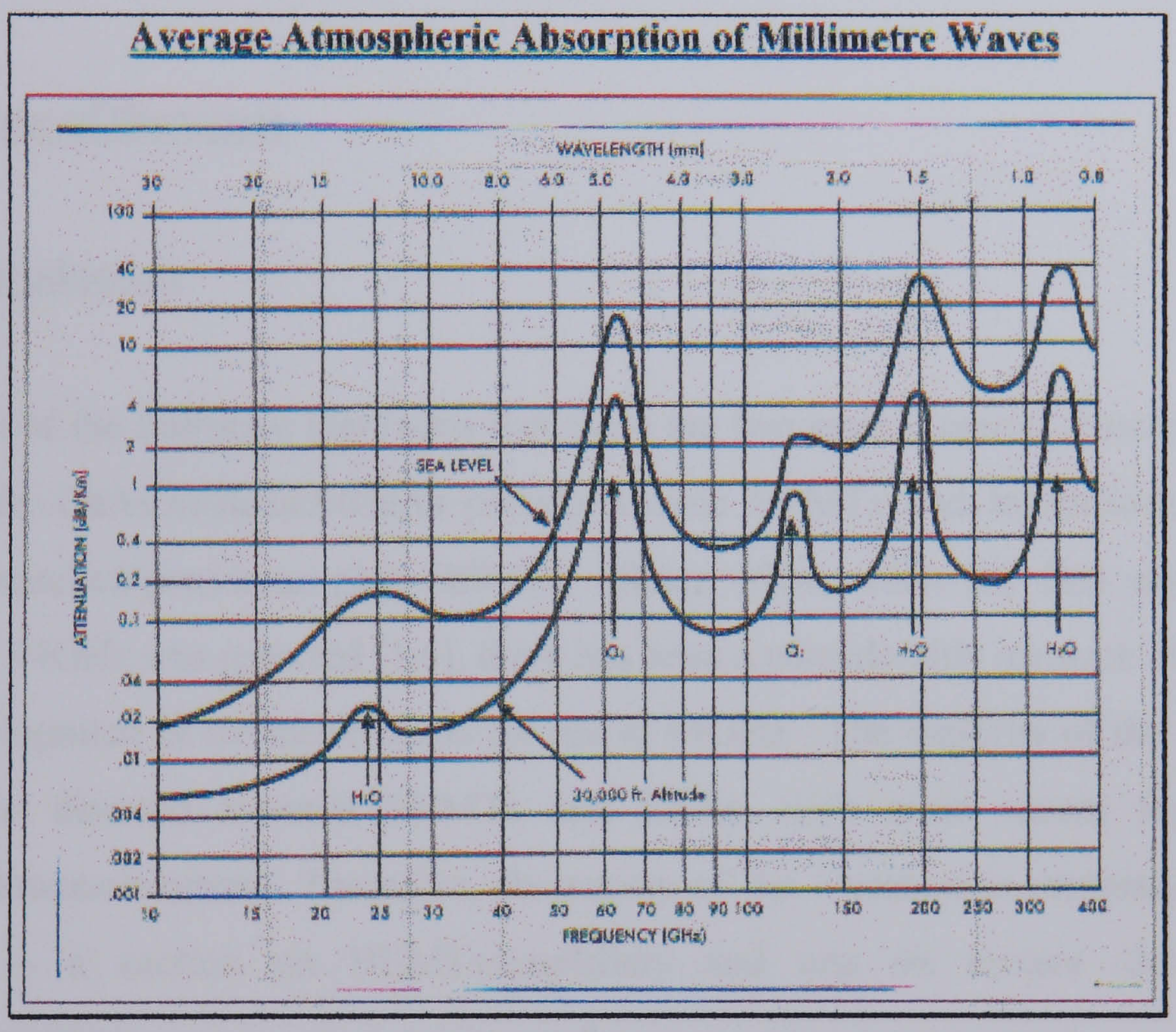

Figure 3 Atmospheric Absorption of Millimetre Waves

It is also possible to build systems using frequencies where the atmospheric attenuation is very high. One example of this is spacecraft-to-spacecraft communication at 60GHz. This frequency has the advantages of a large bandwidth and small antennas with high gains and, since the atmosphere is very lossy at 60GHz, the possibility of interference from earth is greatly reduced.

The research strategy was firstly, to design a mixer circuit for use at 94GHz, secondly, to fabricate and characterise its individual active and passive elements and

the complete mixer circuit at 26GHz in order to develop a suitable fabrication process, and, finally, to fabricate and test the mixer design, along with its individual active and passive elements, at 94GHz. Ultimately, the mixer design should be capable of integration with a pHEMT based low noise amplifier on the same substrate to form a complete downconverter.

Mixer performance is normally evaluated in terms of conversion loss **and** noise figure. However, no equipment was available for the measurement of noise figure although the possible effects of noise are considered in Chapter 2.

1.4 Review of literature

1.4.1 Introduction

A search of the literature highlights that there are two main material structures used at 94GHz: GaAs/InGaAs/AlGaAs pseudomorphic HEMTs and InP/InGaAs/InAlAs lattice matched/pseudomorphic HEMTs. Since 1984, when the first **monolithic** mixer at 94GHz was reported [1.6], there has been a considerable research effort into the development of devices/circuits for use at 94GHz. The majority of the research has been directed towards HEMTs and LNAs, with more recent reports of mixers/downconverters. Therefore, the survey of the literature is presented in two sections - a section on HEMTs/amplifiers and one on mixers /detectors / downconverters.

1.4.2 HEMTs/Amplifiers

This section highlights the developments in amplifiers/individual transistors without going into detail about different amplifier designs. Its purpose is to indicate values of gain/noise figure which can be expected from amplifiers which could be integrated with mixers/diodes to form downconverters/detectors.

In **1986** the **General Electric Company (GE), Syracuse** reported transistor amplification for the first time @ 94GHz [1.7]. A single-stage amplifier using 0.25μm AlGaAs/GaAs HEMT technology gave a small-signal gain of 3.6dB. By **1989 GE** [1.8] had developed a 0.1μm gate-length, AlGaAs/InGaAs/GaAs pHEMT giving 5.1dB gain with 3dB associated noise figure at 94GHz.

TRW, in 1990, reported the successful fabrication of 0.1μm gate length GaAs pHEMTs for W-Band operation [1.9], and in [1.10] they improved upon this initial performance by reporting a device with a maximum gain of 9.6dB @ 94GHz. In the same year the development cycle continued with **GE**, in [1.11], describing a 0.15μm InAlAs/InGaAs/InAlAs/InP lattice-matched HEMT process which gave 6.6dB gain, 1.4dB noise figure @ 93GHz. Following on from this [1.12], they also reported the development of two-stage amplifiers using the same InP technology with a resultant gain of 11.5+/-0.4dB from 88-96GHz and a minimum noise figure of 3.2dB. They compared this with the fabrication of a two-stage GaAs-based amplifier which had a gain of 9.7dB and a noise figure of 4.2dB @ 93GHz and used 0.15μm AlGaAs/InGaAs/GaAs pHEMTs. These amplifiers used microstrip interconnects.

The first report of a MMIC using **Coplanar Waveguide** (CPW) interconnects instead of **microstrip** was published in 1990 by the **Varian Research Center** [1.13]. This single-stage 94GHz InP MMIC amplifier used lattice-matched InGaAs/InAlAs HEMTs with 0.1μm mushroom gates and had a gain of 6.4dB. In **1991 TRW** demonstrated the fabrication of a two-stage LNA which gave a gain of 13.3dB @ 94GHz using 0.1μm **T-gate** planar doped GaAs pHEMTs and microstrip [1.14].

After this initial period when many new material structures and improvements in lithography enabled rapid progression, the focus switched to reducing HEMT noise figures. In **1992 TRW** [1.15] had further improved the W-Band performance of its HEMTs by the introduction of a 0.1μm T-gate **pseudomorphic** InAlAs/InGaAs/InP HEMT which gave 8.2dB gain and 1.3dB noise figure at 95GHz. Also in 1992, **TRW** reported a three-stage LNA (using microstrip) based on 0.1μm InGaAs/GaAs

pHEMTs which had a small signal gain of 21dB @ 94GHz with 3.5dB noise figure [1.16]. In **1993** [1.17] **TRW** reported the development of a two-stage W-Band CBCPW (conductor backed CPW where the backside of the wafer is metallised to provide a more durable chip) low-noise amplifier using AlGaAs/InGaAs/GaAs HEMT devices. The same year, they designed a four-stage InP HEMT balanced amplifier (75-110GHz) which a measured gain of 23+/3 dB over the entire W-Band [1.18].

The Martin Marietta Labs, Maryland, in **1994,** [1.19] used four-stage LNAs with GaAs pHEMT/CPW technology to achieve a gain of 30.8dB @ 94GHz. **TRW, in 1995,** [1.20] had developed a seven-stage LNA based on GaAs pHEMTs giving a gain of 40dB, the highest to date while in [1.21] a 175mW two-stage power amplifier was reported using the same technology.

In **1997** [1.22], the **University of Massachusetts** published a conference paper on a six-stage InP amplifier (90 to 140GHz). **TRW**, in [1.23], had already developed a three-stage 155GHz monolithic InP based HEMT amplifier whilst in [1.24] they published a paper on the development of a two-stage monolithic W-Band power amplifier using a 0.1μm GaAs pHEMT process.

These developments in amplifier/HEMT technology are tabulated overleaf. Conclusions to be drawn from this analysis are:

1) There has been a steady progression from hybrid to monolithic circuits.
2) GaAs pHEMTs are the more mature technology, ahead of InP HEMTs.
3) Almost all LNAs have been implemented using microstrip.

Performance Summary of W-Band LNAs/transistors Table 1.1

Device Technology	No. of Devices	Gain/NF (dB)	Construction/Reference
GaAs HEMT	1	3/NA @ 94GHz	Hybrid, [1.7]
GaAs pHEMT	1	5.1/3 @ 94GHz	N/A, [1.8]
GaAs pHEMT	1	4.7/2.5 @ 92.5GHz	N/A, [1.9]
GaAs pHEMT	1	6.3/2.1 @ 93.5GHz	N/A, [1.10]
InP HEMT	1	6.6/1.4 @ 93GHz	N/A, [1.11]
GaAs pHEMT	2	9.7/4.2 @ 94GHz	Hybrid, [1.12]
InP HEMT	2	11.5/3.2 @ 94GHz	Hybrid, [1.12]
InP HEMT	5	6.4/N/A @ 94GHz	CPW, distributed amplifier, [1.13]
GaAs pHEMT	2	13.3/5.5 @ 94GHz	monolithic, 2-stage, [1.14]
GaAs pHEMT	1	7.3/N/A @ 94GHz	power devices, [1.25]
GaAs pHEMT	8	49/6.5 @ 94GHz	8-stage, monolithic, [1.26]
InP HEMT	2	14.2/2.6@92GHz	2-stage, hybrid, [1.15]
GaAs pHEMT	2	12/4.2-4.8@92-96GHz	monolithic, [1.17]
InP pHEMT	4	23/6 @ 94GHz	monolithic, [1.18]
GaAs pHEMT	3	10/N/A@94GHz	monolithic, power, [1.27]
GaAs pHEMT	3	21/6.2 @ 77GHz	monolithic, CPW, [1.28]
GaAs pHEMT	4	30.8/4 @ 94GHz	monolithic, [1.19]
GaAs pHEMT	2	10.4/5.9 @ 91GHz	monolithic, [1.29]
GaAs pHEMT	6	NA	monolithic, [1.20]
GaAs pHEMT	2	7/N/A@90GHz	monolithic, power, [1.21]
InP HEMT	6	NA	monolithic, [1.22]
InP HEMT	3	NA	monolithic, [1.23]
GaAs pHEMT	2	NA	monolithic, power, [1.24]

1.4.3 Mixers/Detectors/Downconverters

Within this section, different mixer/detector designs are described in order to demonstrate what has been done and to justify the mixer design which was used for this project. However, detailed mixer theory is not given here but instead is included in Chapter 2.

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In **1989 TRW (California)** , in [1.30], described the design and performance of a 94GHz 0.1μm AlGaAs/GaAs HEMT mixer (hybrid) using microstrip. A schematic of this mixer design is shown below in block diagram form.

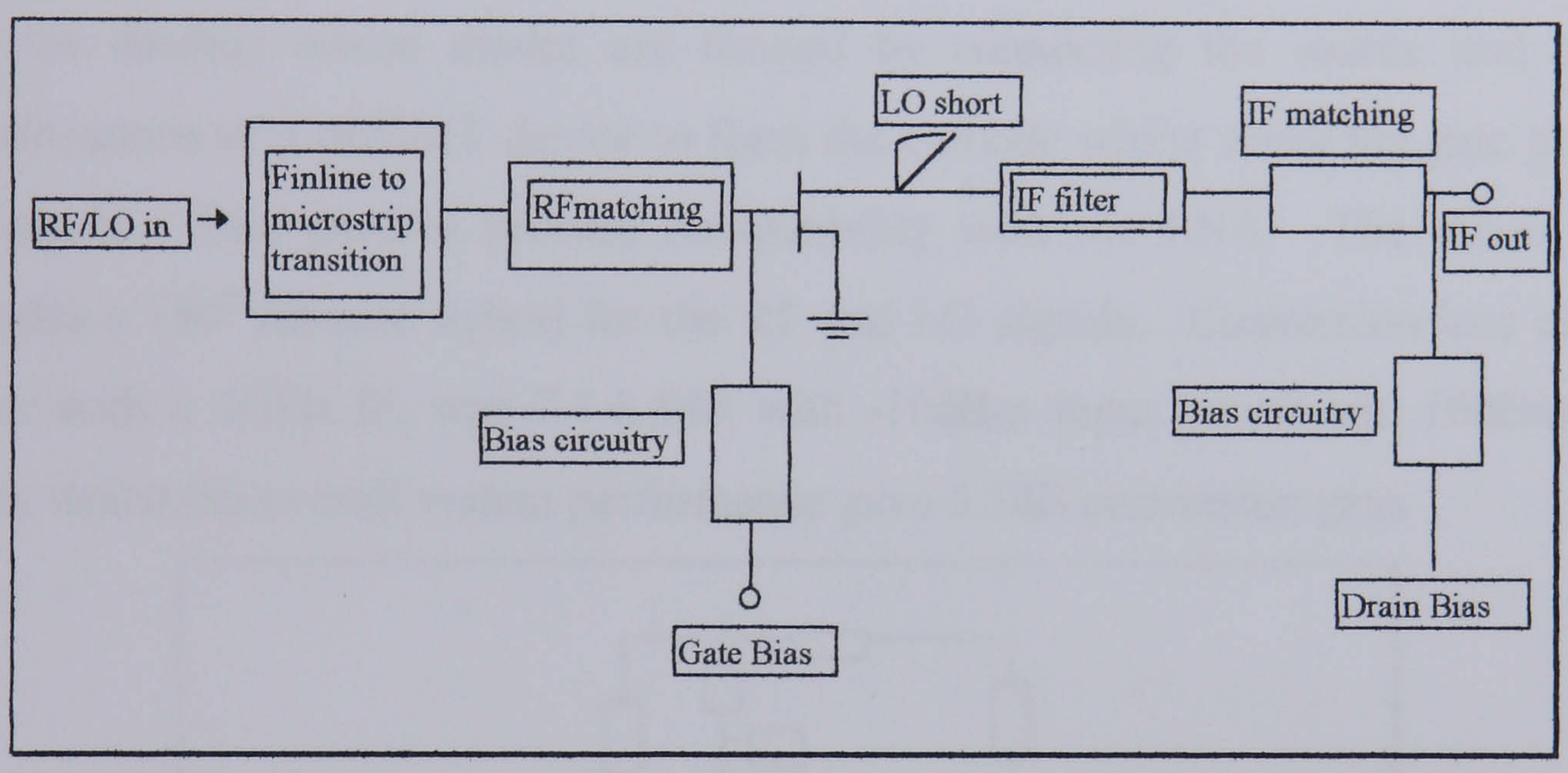


Figure 4 Block Diagram of a HEMT mixer[1.30]

The operation of the circuit is based on the modulation of the HEMT's transconductance and drain current by the LO signal which is assumed to be much larger than the RF signal. The use of the FET in an active mixer format requires bias circuitry.

In **1990, The University of Michigan** [1.31] described the development of the first W-Band monolithic mixer using a InAlAs/InGaAs/InP HEMT process. Measured performance was 13.5dB conversion loss with only -6dBm LO drive @ 95GHz. The mixer design was of the same form as shown in Figure 4 and used microstrip.

In **1991 TRW** [1.32] reported the first **active** mixer giving a conversion gain at W-Band. The mixer was based on 0.15 μm T-gate lattice-matched InAlAs-InGaAs-InP

HEMTs and was exactly the same design as shown in Figure 4. The inevitable progression from these developments was the drive towards integration of monolithic amplifiers/mixers to form complete downconverters and [1.33,1.34,1.35], describe the design, fabrication and evaluation of W-Band downconverters based on both GaAs pHEMT and InP HEMT technology by **TRW**. The downconverter described in [1.33] consists of a 2-stage hybrid LNA and the same active mixer design shown in Figure 4. The system described in [1.34,1.35], was the first example of a true monolithic downconverter as it combined on a single chip, an RF amplifier and mixer. The mixer design is known as singly-balanced (see Chapter 2 for exact description) and is shown in schematic form below. This is a passive mixer (no DC bias for diodes) whose diodes are formed by connecting the source and drain metallisations of a pHEMT device to form the cathode whilst using the gate pad as the anode. This ensures process compatibility with the LNA. The mixer also includes a 180^0 rat-race hybrid for the RF and LO signals. Conversion loss of the mixer with a 1GHz IF, was 7.5-8.5dB with -10dBm input power and 10dBm LO drive, whilst the overall system performance gave 5.5dB conversion gain.

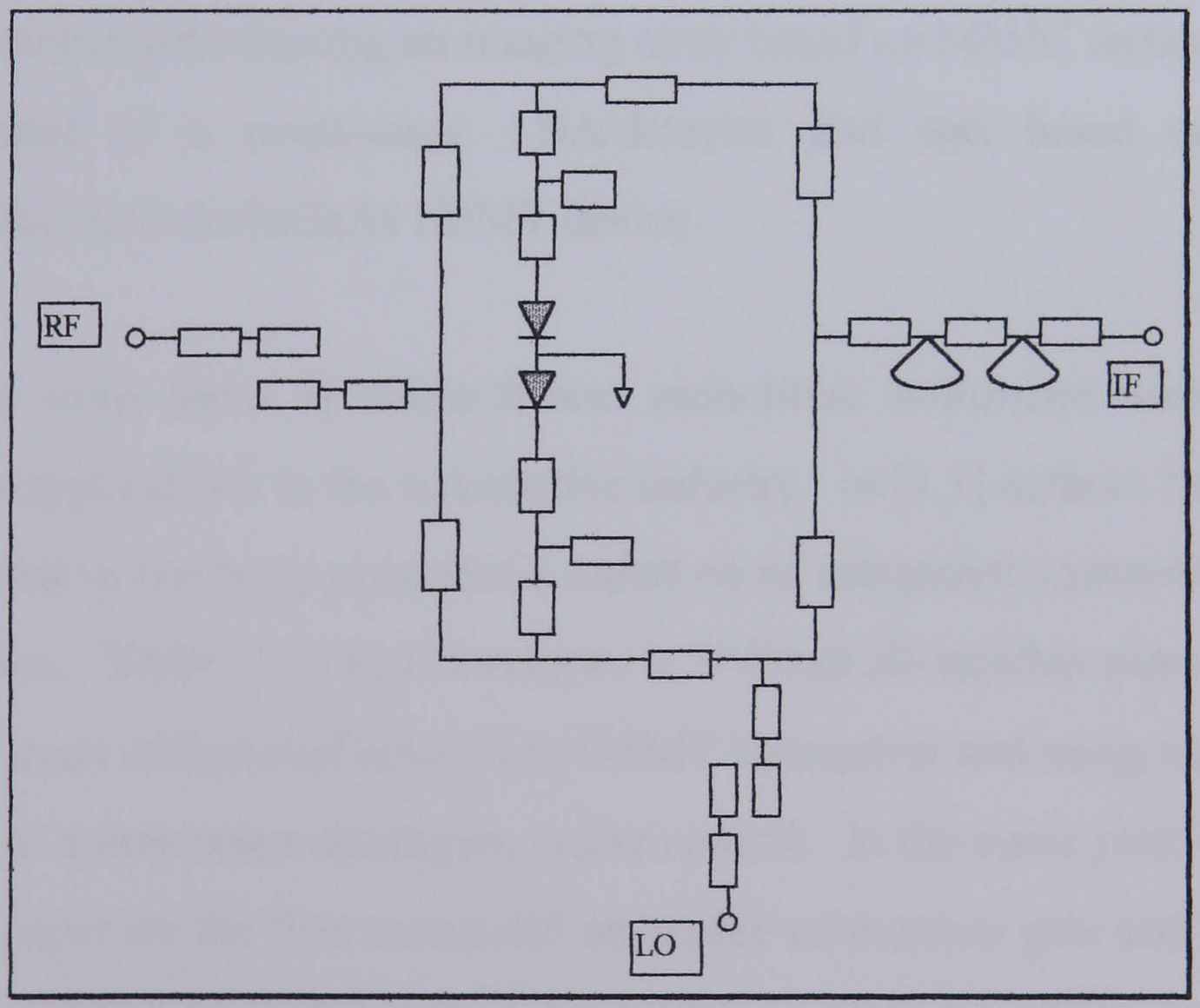


Figure 5 Schematic form of mixer in [1.34,1.35]

By **1993 TRW** had designed and fabricated W-Band direct detection systems [1.36,1.37]. These circuits were again based on 0.1 μm InGaAs pseudomorphic HEMT technology and consisted of two or three stage LNAs followed by a diode

detector. The Schottky diode was formed by connecting together the source and drain of a FET to form the cathode and the gate fingers to form the anode. Applications for such circuits are in passive imaging systems and radiometers. In [1.38] researchers at the **University of Michigan** demonstrated a W-Band dual-gate HEMT mixer using InAlAs/InGaAs HEMT technology (microstrip). This mixer showed a conversion loss of 3dB with 5dBm LO power and had RF-to-LO isolation better than 17dB. The design is basically similar to that shown in Figure 4 but the second gate of the FET ensures excellent RF-to-LO isolation without the need for a microstrip-to-finline transition. In [1.39] they also presented the experimental characteristics of InAlAs/InGaAs/InP HEMT active mixers (using microstrip) giving a conversion gain of 0.9dB with 2dBm (very low) LO power.

By **1994 the Fraunhofer Institute** [1.28], with their publications on the design and fabrication of MMICs for automotive applications (76-77GHz), were the first major research lab to focus on CPW based MMICs. Their mixer presented in this paper was an active HEMT mixer. **TRW**, in [1.40], developed another direct detection system by designing/fabricating an imaging array based on MMIC technology. Each pixel consisted of a seven-stage LNA/detector and was based on a 0.1μm pseudomorphic AlGaAs/InGaAs HEMT device.

By **1995** the main focus of research was monolithic millimetre wave integrated circuits with applications in the automotive industry. In [1.1] authors from **Daimler Benz Research** in Germany presented a report on an integrated transmitter for use in crash detection. **TRW** [1.2] had developed a W-Band all-weather automotive radar based on a 0.1μm AlGaAs/InGaAs/GaAs HEMT transceiver and using microstrip, for the purpose of autonomous intelligent cruise control. In the same year, TRW [1.41] presented a paper on the first successful **on-wafer** conversion gain and noise figure measurements taken on a downconverter MMIC at W-Band. This downconverter used AlGaAs/InGaAs/GaAs HEMT technology (same design as in [1.34,1.35]) and the measured conversion gain was 7.5-8.5dB, whilst the noise figure was 6.5-7.5dB for an IF signal in the range 40-400MHz. In [1.20], TRW described the fabrication of a monolithic W-Band six-stage low noise amplifier/detector, using 0.1μm

passivated pseudomorphic AlGaAs/InGaAs/GaAs HEMT technology. Also, in [1.42] they presented the first monolithic W-Band transceiver with front-end switching receiver for FMCW radar application.

Whilst **1996** was notable for its lack of publications on W-Band MMICs, by **1997**, the **Fraunhofer Institute, Germany** published more papers on MMIC designs for automotive applications. In [1.43], they described the development of integrated transmit and receive MMICs based on a 0.15μm pHEMT process, whilst in [1.44], they had demonstrated fully integrated W-Band heterodyne receivers using the same technology. The receiver MMIC of [1.43] is shown in block diagram form below. A branch-line coupler (see Chapter 2) was used to balance the RF and LO signals at the diodes. The diodes used the same HEMT layout as mentioned previously ([1.34]) and the mixer gave a conversion loss of 10dB for an LO power of 8dBm. Two types of CPW MMIC mixers are mentioned in [1.44]: balanced diode and resistive HEMT mixer. The resistive HEMT mixer differs from the active HEMT mixer by having the LO signal applied to the gate and the RF signal to the drain. The IF signal is filtered from the drain, whilst no DC bias is used and the channel operates as a time-varying resistance.

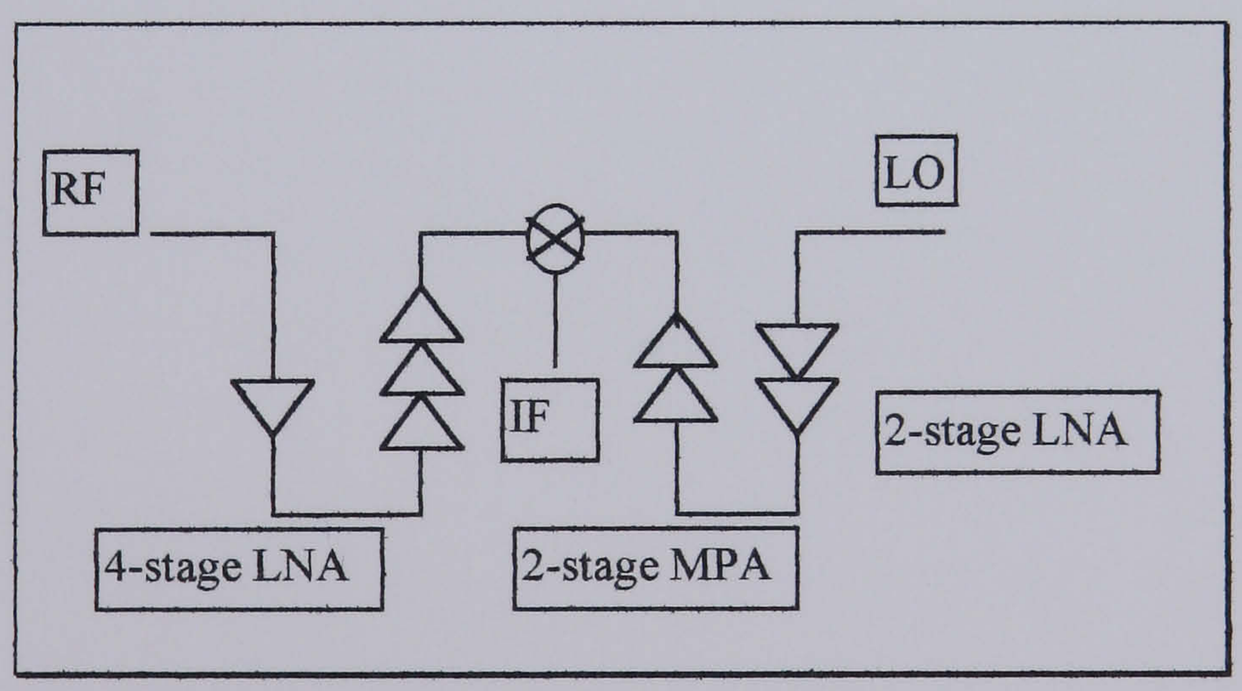


Figure 6 Receiver MMIC from [1.43]

The Hughes Research Labs, in [1.45], present a comparison of three different W-Band mixer designs using InP HEMT/microstrip technology: a) active HEMT b) resistive HEMT c)rat-race diode mixer (using HEMT diodes). The active HEMT mixer gave a conversion loss of 2dB @ 1GHz IF (9.7dBm LO power), the resistive

HEMT mixer gave 9dB loss (3.4dBm LO power) and the rat-race diode mixer gave 10dB loss (10.6dBm power).

These developments in mixers/detectors/downconverters are tabulated overleaf. The important conclusions from this analysis are:

1) There has been a steady progression from hybrid to monolithic circuits.
2) GaAs pHEMTs are the more mature technology.
3) Almost all circuits have been implemented using microstrip.
4) Direct Detection systems have become an alternative to the conventional heterodyne systems, using high gain LNAs and Schottky barrier diodes.
5) Many of the downconverters combine a two or three stage amplifier with a mixer. The overall conversion gain is often due to the high gain LNA rather than the mixer.
6) Active FET mixers offer the possibility of conversion gain. However, additional bias circuitry is required.

Performance summary of W-Band mixers/detectors/downconverters - Table 1.2

Device Technology	Mixer Circuit	Conversion loss/ NF	Construction/Reference
GaAs based HEMT	Single-ended active mixer	5.8 / 12.4dB	hybrid, [1.30]
InP pHEMT	Active mixer	13dB / N/A	monolithic, [1.31]
InP HEMT	Active mixer	2.4 dB gain / 7.3dB	hybrid, [1.32]
GaAs pHEMT	Downconverter	5.5 dB gain / 6.7dB	monolithic,[1.34,1.35]
InP HEMT	Downconverter	17.8dBgain / 3.6dB	monolithic, 2-stage amp and active mixer,[1.33]
GaAs pHEMT	Downconverter	18dB gain / 4.6dB	3-stage LNA, monolithic IRM, [1.46]
GaAs pHEMT	Downconverter	7-9dB gain / 6dB	monolithic, [1.47]
InP HEMT	Active mixer	0.9dB / N/A	monolithic, [1.39]
InP HEMT	Downconverter	11dB gain / 4.9dB	hybrid. [1.48]
InP HEMT	Dual gate mixer	3dB / N/A	monolithic, [1.38]
GaAs pHEMT	Diode detector	N/A	monolithic LNA + diode, [1.36]
GaAs pHEMT	Diode detector	N/A	monolithic LNA + diode, [1.37]
GaAs pHEMT	Direct detection	N/A	monolithic,imaging array, [1.40]
GaAs pHEMT	Transceiver	N/A	monolithic, [1.2]
GaAs pHEMT	Downconverter	7.5-8.5dB gain / 6.5dB	MMIC, [1.41]
GaAs pHEMT	Transceiver	N/A	monolithic, [1.43]
GaAs pHEMT	Downconverter	13dB gain / 6.5dB	monolithic, CPW, [1.44]
InP HEMT	Mixers	0.8dB/10dB 9dB/NA 10dB/NA	Three monolithic designs, using microstrip; resistive HEMT, active HEMT and resistive diode[1.45]

1.4.4 Justification for the project

High quality LNAs have been successfully designed and fabricated using both GaAs and InP substrates, although GaAs pHEMTs are more common. As a result MMIC / mmWIC downconverters are realisable giving overall conversion gain. In terms of mixer design, compatibility with LNA technology is important to enable monolithic integration. Therefore, both HEMTs or HEMT diodes could be used as the mixing element(s). Often, these mixing elements are biased to achieve optimum device performance but this requires additional circuitry. Resistive mixers would also be simple to implement (with a low LO power requirement) but the realisation of *balanced* (see Chapter 2) mixers is more difficult using FETs than diodes. Implementation of such circuits using CPW, rather than microstrip, would make for easy processing and enable CPW-Slotline transitions to be used as an alternative to couplers for RF-LO isolation in a balanced mixer format.

Therefore, it was decided to design, fabricate and test a diode mixer circuit which was compatible with LNA technology, required no bias circuitry and used CPW. The removal of bias circuitry and the use of CPW-Slotline transitions instead of conventional couplers (such as branch-line or rat-race) reduces chip size and the number of on-chip components thus enabling a high-yield, simple design. The specification for desired conversion loss was 10dB based on the foregoing literature search.

1.5 Project Outline

Chapter 2 describes basic mixer theory and the details of the novel mixer design. Since mmWIC diodes are the most important components in the mixer circuit, there is considerable detail on diode design and layout. Also included in this chapter is the layout and theory of the passive elements used in the mixer design such as CPW filters, CPW-Slotline transitions, MIM and interdigitated capacitors.

Chapter 3 contains all the fabrication details for mmWICs and highlights the process developments that were made to the basic University of Glasgow FET process. A description of how individual devices were fabricated for characterisation purposes is also given.

All results from the testing of individual components and completed mmWICs are given in **Chapter 4**. Conclusion and suggestions for further work arising from this project are given in **Chapter 5**.

Chapter 1 References

[1.1] A. Stiller, E.M. Biebl, J.F. Luy, K.M. Strohm, J. Buechler: "A monolithic integrated Millimeter Wave Transmitter for Automotive Applications" - IEEE Transactions on Microwave Theory and Techniques, Vol.43, No.7, July 1995, pages 1654-1657.

[1.2] K.W. Chang, H. Wang, G. Shreve, J.G. Harrison, M. Core, A. Paxton, M. Yu, C.H. Chen, G.S. Dow : "Forward-looking Automotive Radar Using a W-Band Single-Chip Transceiver" - IEEE Transactions on Microwave Theory and Techniques, Vol.43, No. 7, July 1995, pages 1659-1666.

[1.3] F. Ali, J.B. Horton :"Introduction to Special Issues on Emerging Commercial and Consumer Circuits, Systems and Their applications" - IEEE Transactions on Microwave Theory and Techniques, Vol.43, No.7, July 1995, pages 1633-1637.

[1.4] H. Meinel : "Commercial Applications of Millimeter Waves, History, Present Status, Future Trends" - IEEE Transactions on Microwave Theory and Techniques, Vol.43, No.7, July 1995, pages 1639-1652

[1.5] P.H.Ladbrooke : "MMIC Design:GaAs FETs and HEMTs" (Artech House, Norwood, MA, 1989) Chapter 2.

[1.6] L.T. Yuan : "94GHz Planar GaAs Monolithic Balanced Mixer" - IEEE Microwave and Millimeter-wave Monolithic Circuits Symposium Digest, 1984, pages 70-73.

[1.7] P.M. Smith, P.C. Chao, K.H.G. Duh, L.F. Lester, B.R. Lee : "94GHz Transistor Amplification using an HEMT" - Electronics Letters, 17th July 1986, Vol.22, No.15, pages 780-781.

[1.8] P.C. Chao, K.H.G. Duh, P.Ho, P.M. Smith, J.M. Ballingall, A.A. Jabra : "94GHz Low Noise HEMT" -Electronics Letters, 13th April 1989, Vol.25, No.8, pages 504-505.

[1.9] K.L. Tan, R.M. Dia, D.C. Streit, A.C. Han, T.Q. Trinh, J.R. Velebir, P.H. Liu, T. Lin, H.C. Yen, M. Sholley, L. Shaw : "Ultralow Noise W-Band Pseudomorphic InGaAs HEMTs" - IEEE Electron Device Letters, Vol.11, No.7, July 1990, pages 303-305.

[1.10] K.L. Tan, R.M. Dia, D.C. Streit, T. Lin, T.Q. Trinh, A.C. Han, P.H. Liu, P.D. Chow, H.C. Yen : "94-GHz 0.1μm T-Gate Low Noise Pseudomorphic InGaAs HEMTs", IEEE Electron Device Letters, Vol.11, No.12, December 1990, pages 585-587.

[1.11] P.C. Chao, A.J. Tessmer, K.H.G. Duh, P. Ho, M.Y. Kao, P.M. Smith, J.M. Ballingall, S.M.J. Liu, A.A. Jabra : "W-Band Low-Noise InAlAs/InGaAs Lattice-matched HEMTs", IEEE Electron Device Letters, Vol.11, No.1, January 1990, pages 59-61.

[1.12] K.H.G. Duh, P.C. Chao, P. Ho, A. Tessmer, S.M.J. Liu, M.Y. Kao, P.M. Smith, J.M. Ballingall : "W-Band InGaAs HEMT low noise amplifiers"- 1990 IEEE MTT-S Digest, pages 595-598

[1.13] R. Majidi-Ahy, M. Riaziat, C. Nishimoto, M. Glenn, S. Silverman, S. Weng, Y.C. Pao, G. Zdasiuk, S. Bandy, Z. Tan : "94GHz InP MMIC Five-Section Distributed Amplifier"- Electronics Letters, 18th January 1990, Vol.26, No.2, pages 91-92

[1.14] K.L. Tan, H. Wang, D.C. Streit, P.H. Liu, R.M. Dia, A.C. Han, D. Garske, S. Bui, J.K. Liu, T.S. Lin, G.S. Dow, P.D. Chow, J. Berenz : "High Performance W-Band Low-Noise Pseudomorphic InGaAs HEMT MMIC Amplifiers" - Electronics Letters, 20th June 1991, Vol.27, No.13, pages 1166-1167

[1.15] P.D. Chow, K. Tan, D. Streit, D. Garske, P. Liu, R. Lai : "W-Band and D-Band Low Noise Amplifiers using 0.1 micron pseudomorphic InAlAs/InGaAs/InP HEMTs" - 1992 IEEE MTT-S Digest, pages 807-810

[1.16] H. Wang, T.N. Ton, K.L. Tan, G.S. Dow, T.H. Chen, K.W. Chang, J. Berenz, B. Allen, P. Liu, D. Streit, G. Hayashibara, L.C.T. Liu : "An Ultra Low Noise W-Band Monolithic Three-Stage Amplifier Using 0.1μm Pseudomorphic InGaAs HEMT technology" - 1992 IEEE MTT-S Digest, pages 803-806

[1.17] T.N. Ton, H. Wang, S. Chen, K.L. Tan, G.S. Dow, B.R. Allen, J. Berenz : "W-Band Monolithic pseudomorphic AlGaAs/InGaAs/GaAs HEMT CBCPW LNA" - Electronics Letters, 30th September 1993, Vol.29, No.20, pages 1804-1805

[1.18] H. Wang, R. Lai, S.T. Chen, J. Berenz : "A monolithic 75-110GHz Balanced InP-Based HEMT amplifier" - IEEE Microwave and Guided Wave Letters, Vol.3, No.10, October 1993

[1.19] D.W. Tu, P. Berk, S.E. Brown, N.E. Byer, S.W. Duncan, A. Eskandarian, E. Fischer, D.M. Gill, B. Golja, B.C. Kane, S.P. Svensson, S. Weinreb : "High Gain Monolithic p-HEMT W-Band Four-stage low noise amplifiers"-IEEE 1994 Microwave and Millimeter-wave Monolithic Circuits Symposium, pages 29-32

[1.20] D.C.W. Lo, G.S. Dow, B.R. Allen, L. Yujiri, M. Mussetto, T.W. Huang, H. Wang, M. Biedenbender : "A Monolithic W-Band High-Gain LNA Detector for Millimeter Wave Radiometric Imaging Applications"- 1995 IEEE MTT-S Digest, pages 1117-1120

[1.21] H. Wang, Y. Hwang, T.H. Chen, M. Biedenbender, D.C. Streit, D.C.W. Lo, G.S. Dow, B.R. Allen : "A W-Band Monolithic 175mW power amplifier"- 1995 IEEE MTT-S Digest, pages 419-422

[1.22] S. Weinreb, P.C. Chao, W. Copp : "Full-waveguide band, 90 to 140GHz MMIC Amplifier module" -1997 IEEE MTT-S Digest, pages 1279-1280

[1.23] H. Wang, R. Lai, Y.C. Chen, Y.L. Kok, T.W. Huang, T. Block, D. Streit, P.H. Liu, P. Seigel, B. Allen : "A 155GHz Monolithic InP-Based HEMT amplifier" - 1997 IEEE MTT-S Digest, pages 1275-1278

[1.24] P. Huang, E. Lin, R. Lai, M. Biedenbender, T.W. Huang, H. Wang, C. Geiger, T. Block, P.H. Liu : "A 94GHz Monolithic High Output Power Amplifier" - 1997 IEEE MTT-S Digest, pages 1175-1178

[1.25] D.C. Streit, K.L. Tan, R.M. Dia, J.K. Liu, A.C. Han, J.R. Velebir, S.K. Wang, T.Q. Trinh, P.D. Chow, P.H. Liu, H.C. Yen : "High Gain W-Band Pseudomorphic InGaAs power HEMTs" - Electron Device Letters, Vol.12, No.4, April 1991, pages 149-150

[1.26] H. Wang, G.S. Dow, B.R. Allen, T.N. Ton, K.L. Tan, K.W. Chang, T. Chen, J. Berenz, T.S. Lin, P.H. Liu, D.C. Streit, S.B. Bui, J.J. Raggio, P.D. Chow : "High Performance W-Band Monolithic Pseudomorphic InGaAs HEMT LNAs and Design/Analysis Methodology" -IEEE Transactions on Microwave Theory and Techniques, Vol.40, No.3, March 1992, pages 417-426

[1.27] S.W. Duncan, A. Eskandarian, D. Gill, B. Golja, B.Power, D.W. Tu, S. Svensson, S. Weinreb, M. Zimmerman, N. Byer : "Compact High Gain W-Band and V-Band Pseudomorphic HEMT MMIC Power Amplifiers" - IEEE 1994 Microwave and Millimeter-wave Monolithic Circuits Symposium, pages 33-36

[1.28] M. Schlechtweg, W. Reinert, A. Bangert, J. Braunstein, P.J. Tasker, R. Bosch, W.H. Haydl, W. Bronner, A. Hulsmann, K. Kohler, J. Seibel, R. Yu, M. Rodwell : "High Performance MMICs in Coplanar Waveguide technology for commercial V-Band and W-Band application" - IEEE 1994 Microwave and Millimeter-Wave Monolithic Circuits Symposium, pages 81-84

[1.29] T. Kashiwa, N. Tanino, H. Minami, T. Katoh, N. Yoshida, Y. Itoh, Y. Mitsui, T. Imatani, S. Mitsui : "Design of W-Band Monolithic Low Noise Amplifiers using accurate HEMT modelling" - 1994 IEEE MTT-S Digest, pages 289-292

[1.30] P.D. Chow, D. Garske, J. Velebir, E. Hshieh, Y.C. Ngan, H.C. Yen : "Design and Performance of a 94GHz Mixer" -1989 IEEE MTT-S Digest, pages 731-734

[1.31] Y. Kwon, D. Pavlidis, M. Tutt, G.I. Ng, T. Brock : "W-Band Monolithic Mixer using InAlAs/InGaAs HEMT" - GaAs IC Symposium, 1990, pages 181-185

[1.32] D.C. Streit, K.L. Tan, R.M. Dia, A. Han, P.H. Liu, H.C. Yen, P.D. Chow : " High Performance W-Band InAlAs-InGaAs-InP HEMTs" - Electronics Letters, 20th June 1991, Vol.27, No.13, pages 1149-1150

[1.33] P.D. Chow, K. Tan, D. Streit, D. Garske, P. Liu, H.C. Yen : "Ultra low noise High Gain W-Band InP-Based HEMT Downconverter" - IEEE MTT-S Digest 1991, pages 1041-1044

[1.34] K.W. Chang, H. Wang, K.L. Tan, S.B. Bui, T. Chen, G.S. Dow, J. Berenz, T. Ton, D.C. Garske, T.S. Lin, L.C.T. Liu : "A W-Band Monolithic Downconverter" - IEEE Transactions on Microwave Theory and Techniques, Vol.39, No.12, December 1991, pages 1972-1978

[1.35] K.W. Chang, H. Wang, T.H. Chen, K. Tan, J. Berenz, G.S. Dow, A.C. Han, D. Garske, L.C.T. Liu : "A W-Band Monolithic Pseudomorphic InGaAs HEMT Downconverter" - IEEE 1991 Microwave and Millimeter-wave Monolithic Circuits Symposium, pages 55-58

[1.36] H. Wang, W. Lam, T.N. Ton, D.C.W Lo, K.L. Tan, G.S. Dow, B. Allen, J. Berenz : "A Monolithic W-Band Preamplified Diode Detector" - IEEE MTT-S Digest 1993, pages 365-368

[1.37] G.S. Dow, T.N. Ton, H. Wang, D.C.W Lo, W. Lam, B. Allen, K. Tan, J. Berenz : "A W-Band MMIC Direct Detection Receiver for Passive Imaging System" - IEEE MTT-S Digest 1993, pages 163-166

[1.38] Y. Kwon, D. Pavlidis, P. Marsh, G.I. Ng, T. Brock, D.C. Steit : "A Miniaturized W-Band Monolithic Dual-Gate InAlAs/InGaAs HEMT mixer" - GaAs IC Symposium 1993, pages 215-218

[1.39] Y. Kwon, D. Pavlidis, P. Marsh, G. Ng, T.L. Brock : "Experimental Characteristics and Performance Analysis of Monolithic InP Based HEMT mixers at W-Band" - IEEE Transactions on Microwave Theory and Techniques, Vol.41, No.1, January 1993, pages 1-7

[1.40] D.C.W. Lo, L. Yujiri, G.S. Dow, T.N. Ton, M. Mussetto, B.R. Allen : "A W-Band Direct-Detection Radiometric Imaging Array" - IEEE 1994 Microwave and Millimeter-wave Monolithic Circuits Symposium, pages 41-44

[1.41] E.W. Lin, D.C.W. Lo, H. Wang, T.W. Huang, M. Biedenbender, G.S. Dow, B. Allen : "On-wafer testing of a W-Band HEMT Image-Rejection Downconverter MMIC" - 1995 IEEE MTT-S Digest, pages 1479-1482

[1.42] D.C.W. Lo, K.W. Chang, R. Lin, E.W. Lin, H. Wang, M. Biedenbender, G.S. Dow, B.R. Allen : "A single-chip W-Band Transceiver with Front-End Switching Receiver for FMCW Radar Applications"-1995 IEEE MTT-S Digest, pages 873-876

[1.43] L. Verweyen, A. Bangert, H. Massler, T. Fink, M. Neumann, R. Osorio, T. Krems, T. Jakobus, W.H. Haydl, M. Schlechtweg : "Compact Integrated Coplanar T/R modules for automotive applications", 1997 IEEE MTT-S Digest, pages 243-246

[1.44] W.H. Haydl, L. Verweyen, T. Jakobus, M. Neumann, A. Tessmann, T. Krems, M. Schlechtweg, W. Reinert, H. Massler, J. Rudiger, W. Bronner, A. Hulsmann, T. Fink : "Compact Monolithic Coplanar 94GHz Front Ends" - 1997 IEEE MTT-S Digest, pages 1281-1284

[1.45] R.S Virk, L. Tran, M. Matloubian, M. Le, M.G. Case, C. Ngo : "A Comparison of W-Band MMIC mixers using InP HEMT technology" - 1997 IEEE MTT-S Digest, pages 435-438

[1.46] K.W. Chang, H. Wang, T.N. Ton, T. Chen, K.L. Tan, G.S. Dow, G.M. Hayashibara, B.R. Allen, J. Berenz, P.H. Liu, D.C. Streit, L.C.T. Liu: "A W-Band Image-Rejection Downconverter" - IEEE Transactions on Microwave Theory and Techniques, Vol.40, No.12, December 1992, pages 2332-2336

[1.47] H. Wang, K.W. Chang, T.N. Ton, M. Biedenbender, S.T. Chen, J. Lee, G.S. Dow, K.L. Tan, B.R Allen :"High Yield W-Band Monolithic HEMT Low Noise Amplifier and Image Rejection Downconverter chips" - IEEE Microwave and Guided Wave Letters, Vol.3, No.8, August 1993, pages 281-283

[1.48] H. Yoshinaga, K. Masuda, S. Tagaki, B. Abe, K. Shibata, H. Kawasaki, H. Tokuda, I. Tokaji :"A 94GHz-Band Low Noise Downconverter" - 1993 IEEE MTT-S Digest, pages 779-782.

Chapter 2

Mixer Theory & Design

2.1 Introduction

This chapter describes basic mixer theory and the design of the mmWIC which was fabricated in this project. It begins by contrasting the two approaches of heterodyne and direct detection systems. Following on from this the theory of Schottky diodes is presented and the importance of the diode parameters is highlighted. Mixer conversion loss and noise figure are then discussed with consideration being given to how these factors affect the IF amplifier. A comparison of single diode mixers and balanced mixers is then given to illustrate why the balanced mixer design was chosen.

The second part of the chapter presents the mixer circuit design. This includes all components such as diodes, capacitors, filters and transitions. Particular emphasis is placed on the minimisation of diode parasitics through the choice of diode geometry, fabrication procedure and material structure.

2.2 mmWIC mixers and detectors

2.2.1 Heterodyne systems

The mixer, shown in Figure 2 as part of a heterodyne system, is basically a multiplier. This is illustrated in Figure 7 which shows an ideal multiplier with two sinusoids applied to it. The signal applied to the RF port has a carrier frequency ω_s and a modulation waveform A(t). The LO signal is an unmodulated sinusoid at frequency ω_p. The mixer is said to be pumped when the LO is applied. The sum frequency is rejected by the IF filter, leaving only the difference.

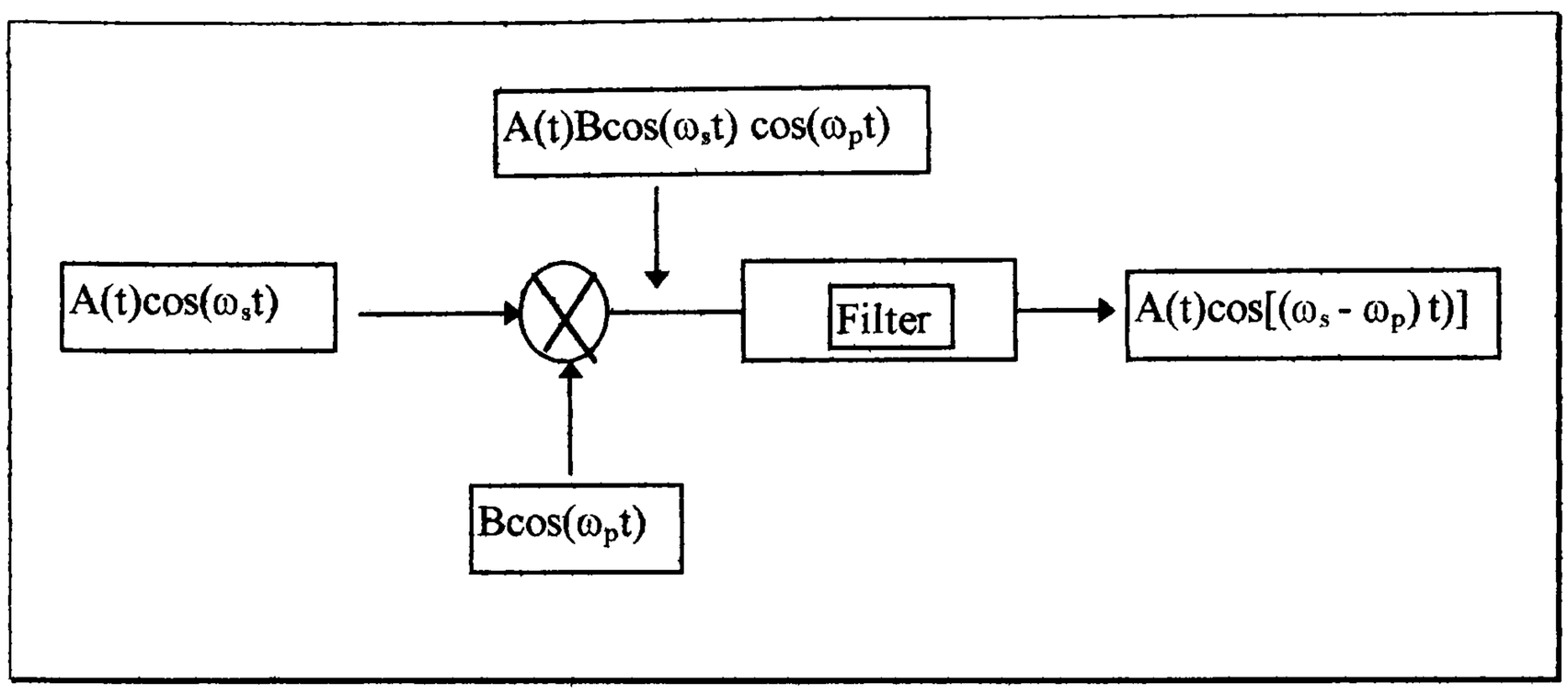


Figure 7 Block Diagram illustrating that a mixer is a multiplier

Any nonlinear device can be used to perform multiplication in a mixer. In resistive mixers, a nonlinear resistance is used while in parametric devices a nonlinear capacitance or inductance does this task. However, the use of a nonideal multiplier results in mixing products other than the desired output. This output must be filtered from the other mixer products. In practice, almost all μwave and mm-wave mixers use Schottky diodes.

The use of a nonideal multiplier can be illustrated by describing the I/V characteristic of the nonlinear device by a power series;

$$I = a_0 + a_1 V + a_2 V^2 + a_3 V^3 + \ldots . \quad \textbf{(1)}$$

where V is equal to the sum of the two inputs in Figure 7.

Taking the first three terms of the power series then:

$$I = a_0 + a_1 (A(t)\cos\omega_s t + B\cos\omega_p t) + a_2 (A(t)\cos\omega_s t + B\cos\omega_p t)^2 \quad \textbf{(2)}$$

Expanding the brackets from the third term gives:

$$A(t)^2 \cos^2 \omega_s t + 2A(t)B\cos\omega_s t \cos\omega_p t + B^2 \cos^2 \omega_p t \quad \textbf{(3)}$$

This simplifies to :

$$\frac{1}{2}A(t)^2(1+\cos 2\omega_s t)+A(t)B(\cos(\omega_s-\omega_p)t+\cos(\omega_s+\omega_p)t)+\frac{1}{2}B^2(1+\cos 2\omega_p t) \quad \textbf{(4)}$$

Collecting the a_1 and a_2 terms from equation **(2)** gives the following spectrum in Figure 8 (if it is assumed that the voltage of the modulated input signal is much smaller than that of the LO, and ignoring the image response):

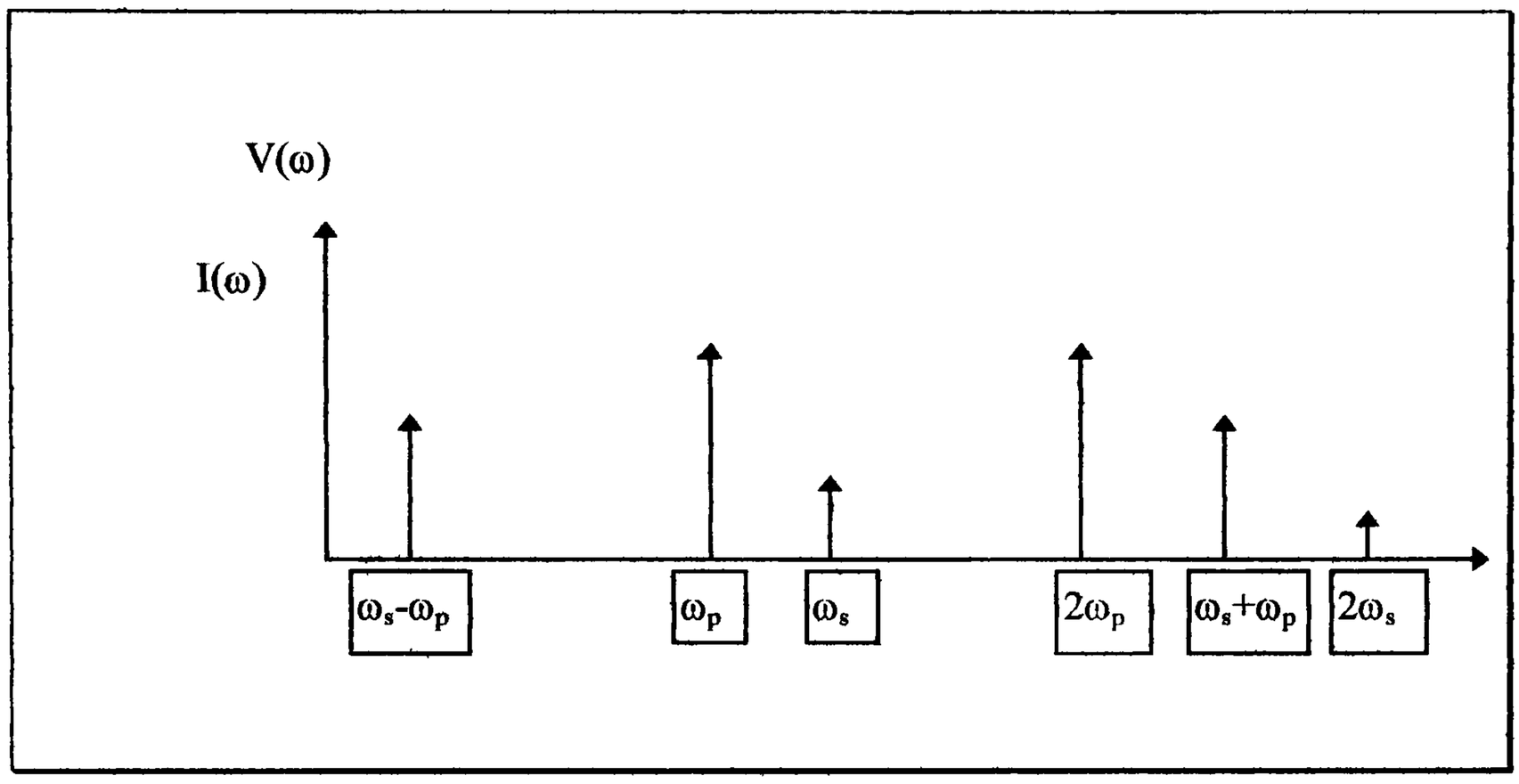


Figure 8 Small signal mixing frequencies

2.2.2 Direct Detection System

Shown below is a block diagram of a typical direct detection system.

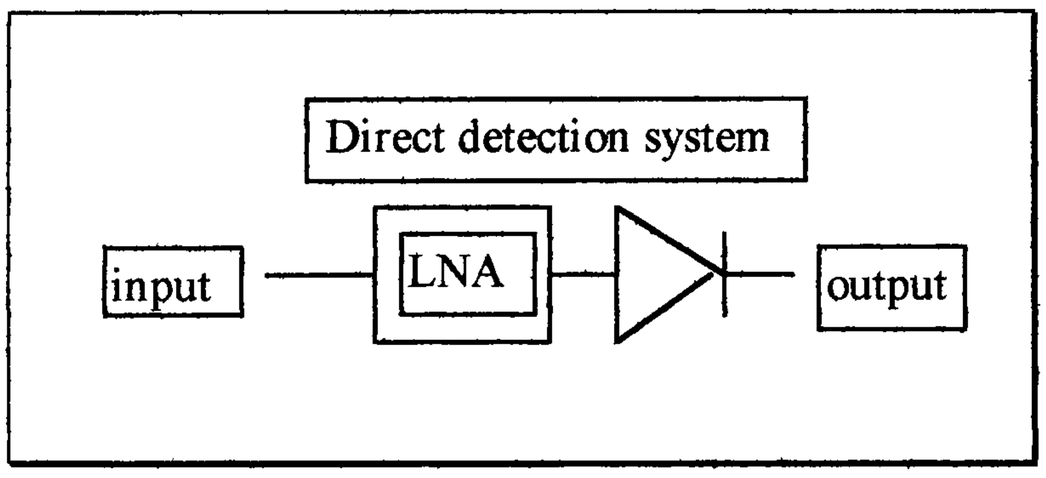


Figure 9 Direct Diode Detector

In a detector application, the nonlinearity of a diode is used to demodulate an amplitude modulated RF carrier. So the diode voltage can be expressed as follows:

$$v(t)=v_o(1+m\cos\omega_m t)\cos\omega_o t \quad \textbf{(5)}$$

where ω_m is the modulation frequency, ω_o is the RF carrier frequency ($\omega_o >> \omega_m$) and m is defined as the modulation index.

Using this in equation **(1)** gives:

$$I = a_0 + a_1(v_0(1+m\cos\omega_m t)\cos\omega_0 t) + a_2(v_0(1+m\cos\omega_m t)\cos\omega_0 t)^2 \quad \textbf{(6)}$$

Expanding the second term of **(6)** gives:

$$a_1(v_0\cos\omega_0 t + v_0\frac{m}{2}(\cos(\omega_m+\omega_0)t + \cos(\omega_m-\omega_0)t) \quad \textbf{(7)}$$

Simplifying the third term of **(6)** gives:

$$a_2(v_0(\cos\omega_0 t + m\cos\omega_m t\cos\omega_0 t))^2 \quad \textbf{(8)}$$

Expanding **(8)**:

$$a_2 {v_0}^2[\frac{1}{2}(1+\cos 2\omega_0 t)\{1+2m\cos\omega_m t + \frac{m^2}{2}(1+\cos 2\omega_m t)\}] \quad \textbf{(9)}$$

Fully evaluating equation **(9)** gives:

$$\frac{1}{2}a_2{v_0}^2[(1+\cos 2\omega_0 t + 2m\cos\omega_m t + m\cos(2\omega_0-\omega_m)t + m\cos(2\omega_0+\omega_m)t + \frac{m^2}{2} \\ \frac{m^2}{2}(\cos 2\omega_0 t) + \frac{m^2}{2}(\cos 2\omega_m t) + \frac{m^2}{4}\cos(2(\omega_0-\omega_m)t) + \frac{m^2}{4}\cos(2(\omega_0+\omega_m)t)] \quad \textbf{(10)}$$

The frequency spectrum of the output current (from **(6)**)is shown below.

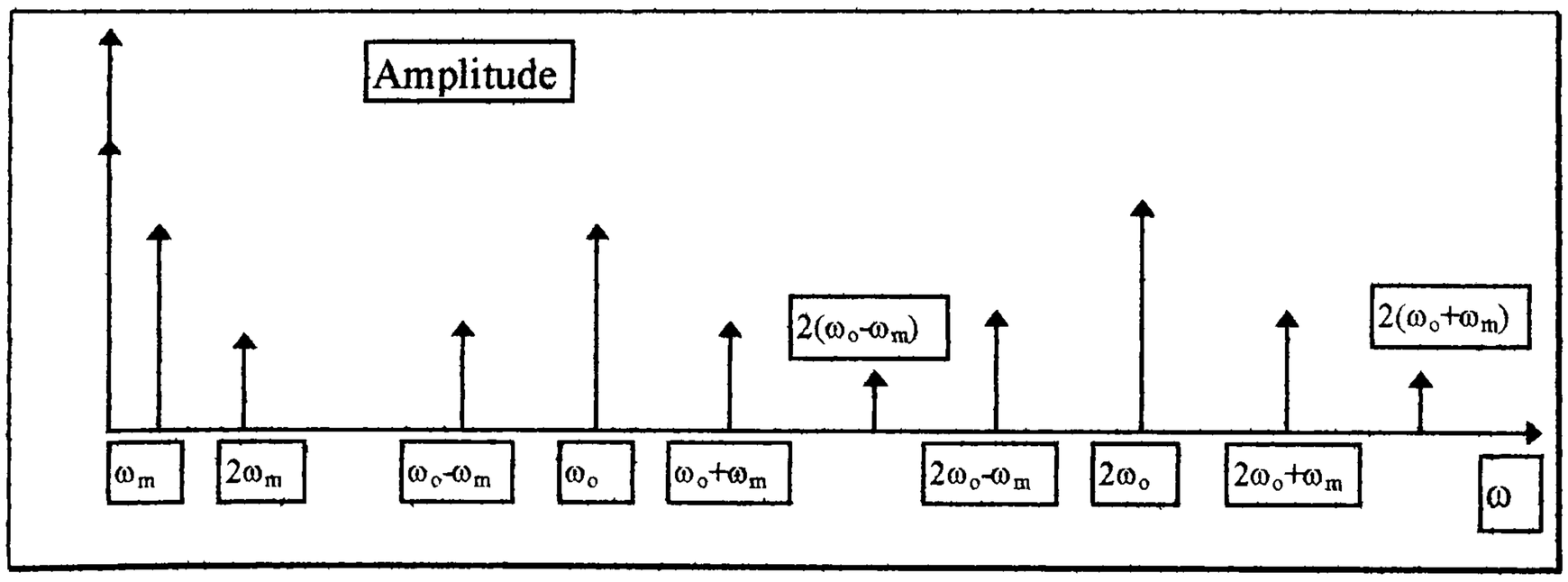


Figure 10 Output spectrum of a detected AM modulated signal

The desired demodulated output of frequency ω_m is easily separated from the undesired components by a low-pass filter. The amplitude of the output current is

proportional to the power of the input signal. This is only possible over a restricted range of input powers, as if it is too large then small-signal conditions no longer apply and the output will become saturated.

2.3 Schottky Diodes

2.3.1 Introduction

Almost all millimetre-wave receivers use Schottky-barrier diode mixers, which rectify by means of a metal-to-semiconductor junction. These diodes are majority carrier devices and so do not suffer from the charge-storage effects that limit the switching speed of *pn* junction diodes. It is thus easier to achieve a low shunt capacitance (C_{jo}) and series resistance (R_s) using Schottky diodes (see section 2.3.3). This is important since it is necessary to use a diode with a cutoff frequency f_c ($=1/(2\pi R_s C_{jo})$) much higher than the signal frequency. This is necessary in order not to lose a substantial amount of power in the series resistance, and also to minimise the effects of the displacement current through the diode capacitance which will modify the diode current and so have an effect on conversion loss. This is illustrated in Figure 11 below, which shows the displacement current through the diode capacitance($\mathbf{i_c}$), and the current through the resistive part of the junction ($\mathbf{i_r}$) [2.30].

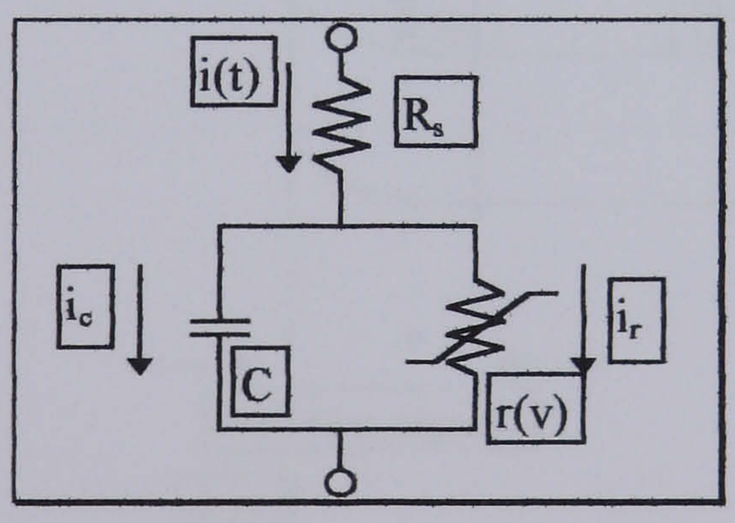


Figure 11 Model of a nonpurely resistive diode

Gallium Arsenide diodes exhibit superior performance to silicon diodes due to higher electron mobility and saturation velocity which allow lower series resistance, for a specific junction capacitance. FET mixers are also becoming more common and they have the advantage over diode mixers of being able to provide several decibels of conversion gain. The main reason for the increasing use of FET mixers is that they are compatible with the MMIC technology of FET amplifiers. FET mixers are normally operated as active circuits, with the LO and RF signals applied

to the gate and, with the IF filtered from the drain. The LO signal modulates the FET's transconductance to produce mixing.

2.3.2 Schottky Barrier Diode Operation

The Schottky-barrier diode is formed between a metal contact (the anode) to a semiconductor (the cathode). Rectification takes place due to the difference in work function between the metal contact and semiconductor. *N*-type semiconductors are preferred over *p*-type due to their increased carrier mobility which results in lower values of diode series resistance. In order to understand the use of Schottky diodes in mixers it is necessary to consider their **I/V characteristics, junction capacitance** and **series resistance**. Shown in Figure 12 is the energy band structure of the Schottky diode.

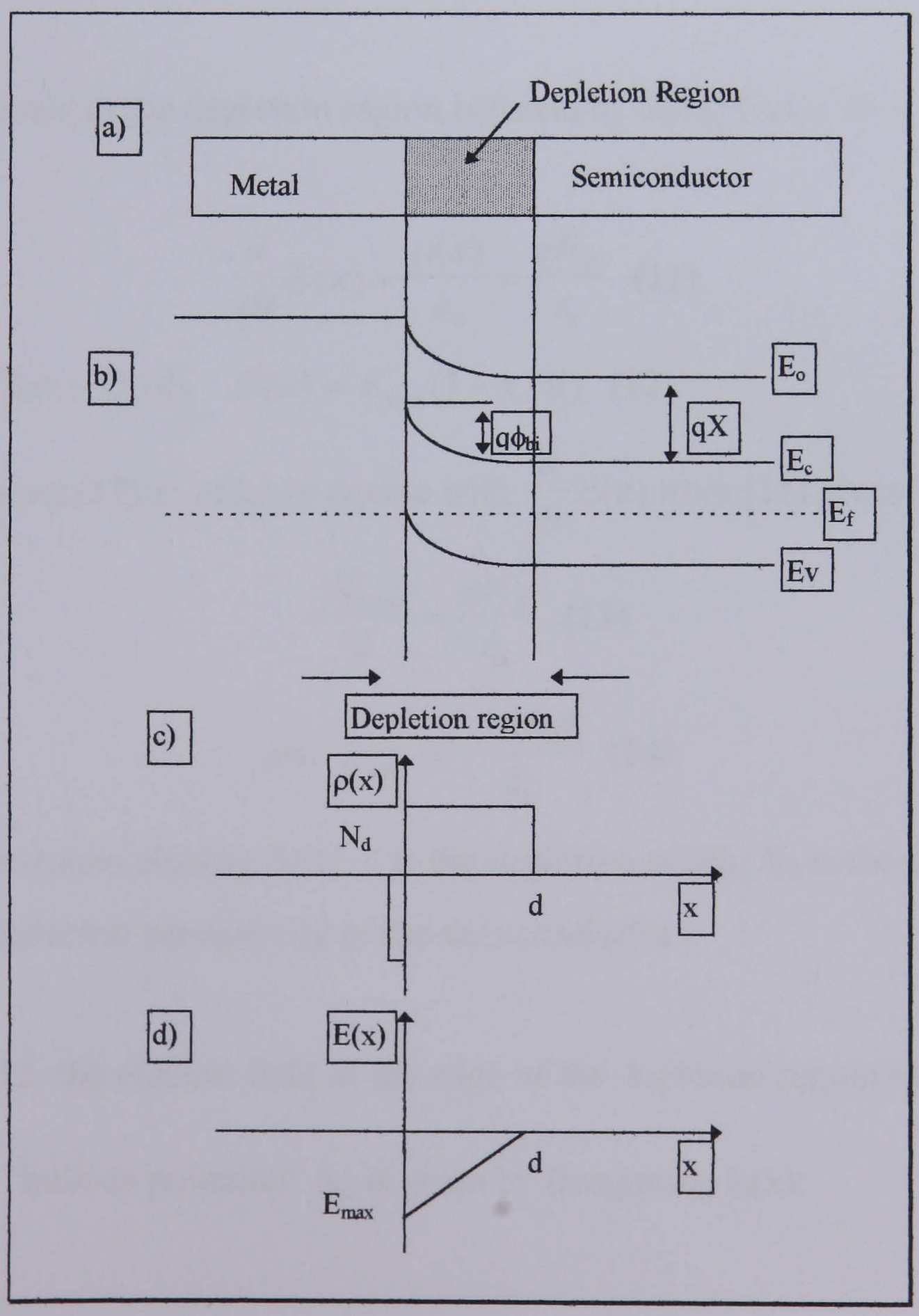


Figure 12 Energy band diagram of a typical Schottky diode

A depletion region is created between the metal and semiconductor when mobile electrons leave the semiconductor and collect on the metal surface. There exists a "built-in potential" across the depletion region (ϕ_{bi}), which is equal to the difference in work functions between the semiconductor and metal. This region has no mobile carriers and the fixed positive charge supports the potential difference between the metal and semiconductor. This depletion region is, therefore, an area of stored charge and in order to determine its capacitance it is necessary to find the quantity of charge that has been moved. The charge density in the depletion region is known because the depletion region's charge comes from donor atoms, all of which are ionized. Therefore the charge density is equal to the doping density. Junction area is known but the width of the depletion region must be determined in order to calculate total charge.

The Electric Field in the depletion region is found by using Gauss' law.

$$\frac{d}{dx}E(x) = \frac{\rho(x)}{\varepsilon_s} = \frac{qN_d}{\varepsilon_s} \quad \textbf{(11)}$$

where from Figure 12 (d), $E(x) = E_{\max}(1 - x/d)$ **(12)**

So differentiating **(12)** in order to equate with $\frac{d}{dx}$E(x) from **(11)** gives

$$\frac{-E_{\max}}{d} = \frac{qN_d}{\varepsilon_s} \quad \textbf{(13)}$$

$$\text{and } E_{\max} = \frac{-qN_d d}{\varepsilon_s} \quad \textbf{(14)}$$

E_{max} is the maximum electric field, d is the depletion width, N_d is the doping density and ε_s is the dielectric permittivity of the semiconductor.

From Figure 12, the electric field at the edge of the depletion region must be zero as $\frac{d\phi}{dx}$=0. The "built-in potential" ϕ_{bi} is given by integrating E(x):

$$\phi_{bi} = E_{\max}\int(1-\frac{x}{d})dx \quad \textbf{(15)}$$

$$\phi_{bi} = -\frac{qN_d d}{\varepsilon_s}[0-(d-\frac{d^2}{2d})] \quad \textbf{(16)}$$

$$\phi_{\text{bi}} = \frac{qN_d d^2}{2\varepsilon_s} \quad \textbf{(17)}$$

where depletion depth, d is

$$d = \sqrt{\frac{2\phi_{bi}\varepsilon_s}{qN_d}} \quad \textbf{(18)}$$

The depletion charge, which relates directly to junction capacitance, is given by:

$$Q_j = qAdN_d \quad \textbf{(19)}$$

where A is the junction area. This is illustrated in the simple diagram below.

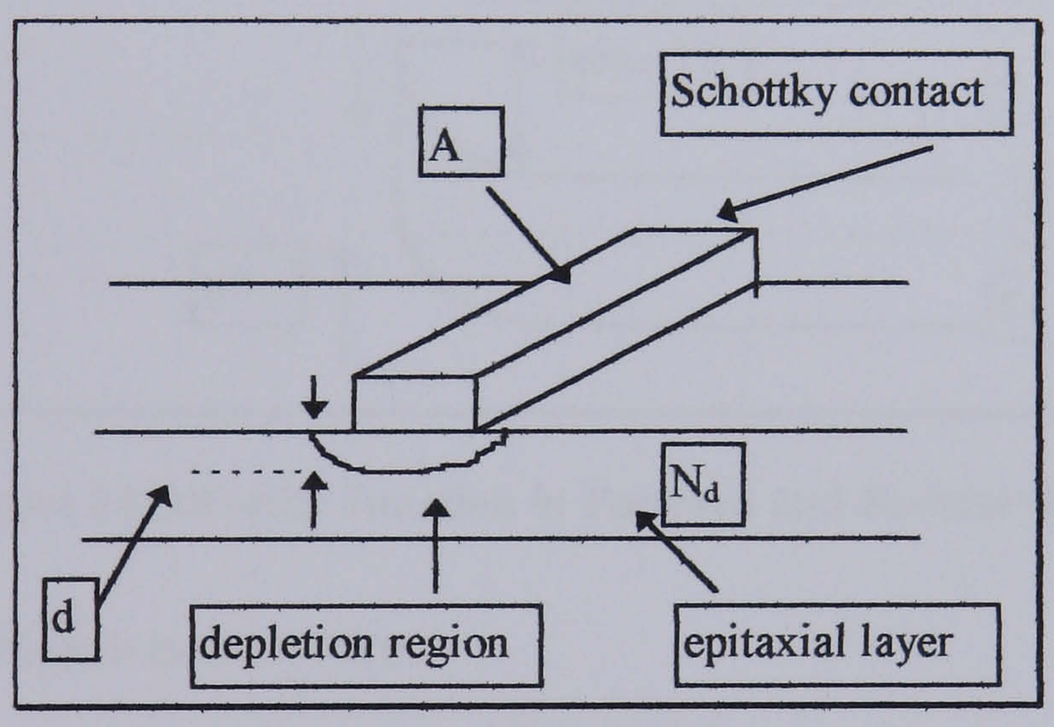


Figure 13 Simplified diagram of a Schottky contact

The figure above shows a small, rectangular anode on an epitaxially grown semiconductor. It is important to note that fringing fields from the metal to semiconductor will alter the diode capacitance. One other important factor for the pHEMT (see Section 2.7.2) diodes used in this project, is that the effect that a small gate has on the channel beneath it diminishes as the gate becomes smaller. This is due to the fact that a given region of 2DEG is not only affected by the gate that lies immediately above it, but also by the surface of the material on either side of the gate [2.28]. So as the gate becomes smaller, the surface surrounding it becomes more important to device performance.

Figure 14, below, shows a Schottky junction under forward and reverse bias. The expressions derived for E(x), E_{max}, Q_j and d are still valid for the biased diode if ϕ_{bi} is replaced with (ϕ_{bi}-V).

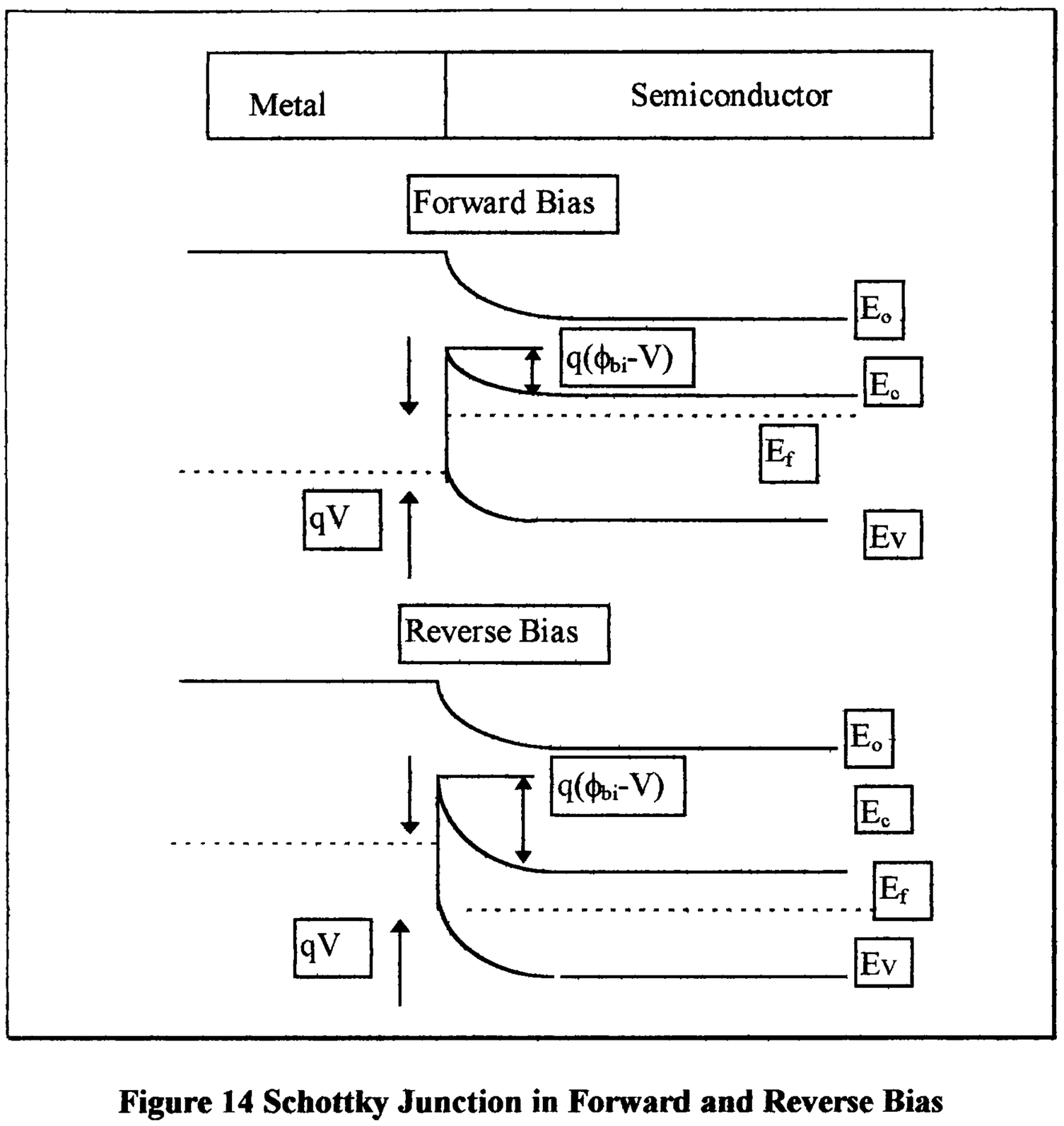


Figure 14 Schottky Junction in Forward and Reverse Bias

The junction capacitance is therefore:

$$\frac{dQ_j}{dV} = C(V) = W\sqrt{\frac{q\varepsilon_s N_d}{2(\phi_{bi}-V)}} = \frac{W\varepsilon_s}{d} \quad \textbf{(20)}$$

This is often written as:

$$C(V) = \frac{C_{jo}}{\sqrt{1-\frac{V}{\phi_{bi}}}} \quad \textbf{(21)}$$

where C_{jo} is the junction capacitance at zero bias voltage.

The derivation for junction current is from [2.1]. Principally, electron conduction occurs by thermionic emission over the barrier. At zero bias, this emission happens equally in both directions so that there is no net current. In forward bias, electron energy is increased relative to the barrier height, therefore electron emission from the

semiconductor to the metal is increased. In the opposite direction, the current remains the same as the barrier height is constant.

Electron density at the junction, n_1 ,is given by:

$$n_1 = N_d \exp(\frac{-q\phi_{bi}}{KT}) \quad \textbf{(22)}$$

under zero bias. The current in each direction is equal, and must be proportional to this electron density. If bias is applied, the potential barrier becomes ϕ_{bi}-V and so the density of forward-conducted electrons is

$$n_2 = N_d \exp(\frac{-q(\phi_{bi} - V)}{KT}) \quad \textbf{(23)}$$

The junction current is proportional to the difference between these densities and is given in the following equation:

$$I(V) = I_0(\exp(\frac{qV}{\eta KT}) - 1) \quad \textbf{(24)}$$

This is known as the **ideal diode equation**. The parameter η is called the diode *ideality factor* and should be as close to 1 as possible. As η increases so the diode's nonlinearity decreases. This can be justified by considering the deviations from this ideal equation in terms of: a) Schottky Barrier Lowering; b) surface imperfections; c) tunnelling.

Firstly, the equation **(24)** can be re-arranged to give the equation:

$$\eta = \frac{q}{KT} \Delta V \log(e) \quad \textbf{(25)}$$

a) One of the assumptions in the derivation of **(24)** was that the barrier height remained constant under all conditions of applied voltage. This barrier height, in fact, varies with applied voltage because conduction electrons in the semiconductor experience a force from their image charges in the metal. This force attracts the electrons towards the metal surface, and so effectively lowers the barrier height (voltage-dependent deviations from ideal behaviour are then possible).

b) In order to obtain good I/V characteristics, the semiconductor surface on which the junction is fabricated must be very clean. Such factors as the formation of undesired chemical compounds between junction metal and semiconductor, (possibly arising from the dry etch process if the anode is recessed) or damage to the crystal structure caused by the deposition of the junction metal will increase the diode ideality factor.

c) Thermal emission is not the only mechanism by which electrons can cross the potential barrier at the junction. Quantum mechanical tunnelling through the barrier is also possible and this can have a significant effect on the diode I/V characteristic, especially at high doping densities (η increases).

2.3.3 Diode equivalent circuit model

In order to study the use of Schottky diodes in mixers it is necessary to have a circuit model that is valid for both large and small signal analysis. Such a model is shown in Figure 15, and consists of a nonlinear resistance and capacitance representing the junction and a series resistance. This simplified model does not include package parasitics. The junction capacitance C_{jo} and series resistance R_s are parasitic elements in this equivalent circuit and it is advantageous to minimise both these quantities in order to ensure low mixer conversion loss [2.2]. A figure of merit commonly used for mixer diodes is cutoff frequency f_c, given by the equation

$$f_c = \frac{1}{2\pi R_s C_{jo}}. \quad \textbf{(26)}$$

In large-signal analysis (such as calculating the LO waveforms in a mixer) the diode nonlinear model is used as shown. In small-signal analysis the I/V and C/V characteristics of the diode are linearized around the large-signal voltage and so the junction conductance and capacitance are treated as linear, time-varying elements. This is necessary as the RF and IF voltage components are small compared to the large-signal LO voltage.

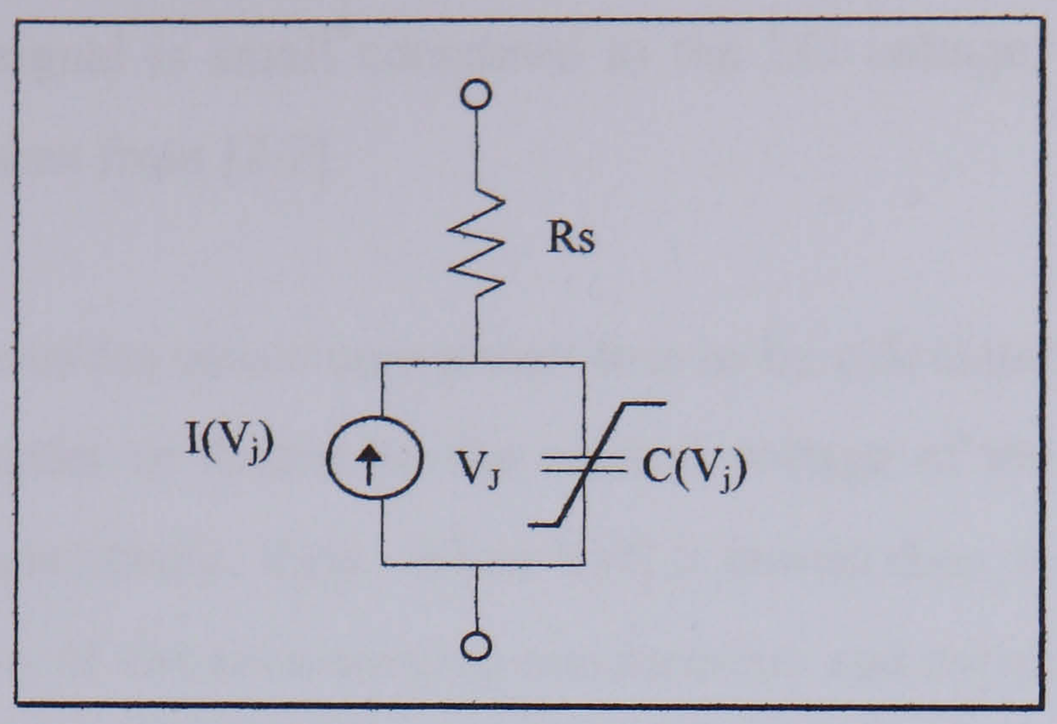


Figure 15 Schottky Diode Equivalent circuit

To provide some benchmark for the diodes to be fabricated in this work, table 2.1 shows values of series resistance and junction capacitance for mixer diodes described in the literature.

Diode parameters Table 2.1

Series Resistance(Ω)	**Junction Capacitance(fF)**	**Reference, Diode Formation**
18	16	[1.34] GaAs pHEMT diodes, 0.1μm length, 2 fingers, 8μm width
10	13.2	[2.3] GaAs diode, FET layout, 4 fingers, 0.5μm length, 10μm width
2.5	250	[2.2] Beam Lead Diodes
8	18	[2.4] Planar, Hybrid Schottky Diode
10	25	[2.5] Mott Diode
6	6	[2.6] Schottky Diode

A detailed description of different diode designs is given in Section 2.6.

2.3.4 Diode mixer theory & calculation of mixer conversion loss

In the analysis which follows, it is assumed that the LO voltage serves only to vary the diode's small-signal junction conductance and capacitance, and that frequency conversion occurs via these linear, time-varying small-signal elements. This is valid

if the applied RF signal is small compared to the LO voltage. The mixer theory presented here is taken from [2.7].

The theory which enables mixer conversion loss to be calculated begins with large-signal analysis in order to determine the control voltage of the nonlinear junction conductance and capacitance, $V_j(t)$. When $V_j(t)$ is known then, it is used in the small small signal analysis of the time-varying conductance and capacitance to determine conversion loss. This is illustrated below, and in Figure 16:

The junction I/V characteristic is:

$$I(V_j) = I_o(\exp(\frac{qV_j}{\eta KT}) - 1) \quad \textbf{(27)}$$

and the small-signal junction conductance is:

$$g(V_j) = \frac{d}{dV_j} I(V_j) = \frac{q}{\eta KT} \exp(\frac{qV_j}{\eta KT}) \quad \textbf{(28)}$$

The junction capacitance $C(V_j)$ is:

$$C(V_j) = \frac{C_{jo}}{\sqrt{1 - \frac{V_j}{\phi_{bi}}}}. \quad \textbf{(29)}$$

This capacitance is defined as the incremental change in depletion region charge that results from a change in junction voltage:

$$C(V_j) = \frac{dQ_d}{dV_j} \quad \textbf{(30)}$$

The large-signal current in the capacitor, $I_c(t)$ is:

$$I_c(t) = \frac{dQ_d}{dt} = C(V_j(t)) \frac{d}{dt} V_j(t) \quad \textbf{(31)}$$

where $V_j(t)$ is the large-signal junction voltage.

In the small-signal analysis (which is used to calculate conversion loss), the capacitor is treated as a linear, time-varying element.

So,

$$C(t)=C(V_j(t)) \quad \textbf{(32)}$$

$$i_c(t) = \frac{d}{dt}C(t)v(t) = C(t)\frac{d}{dt}v(t) + v(t)\frac{d}{dt}C(t) \quad \textbf{(33)}$$

where v(t) is the small-signal junction voltage.

R_s, the diode series resistance, is treated as a linear quantity.

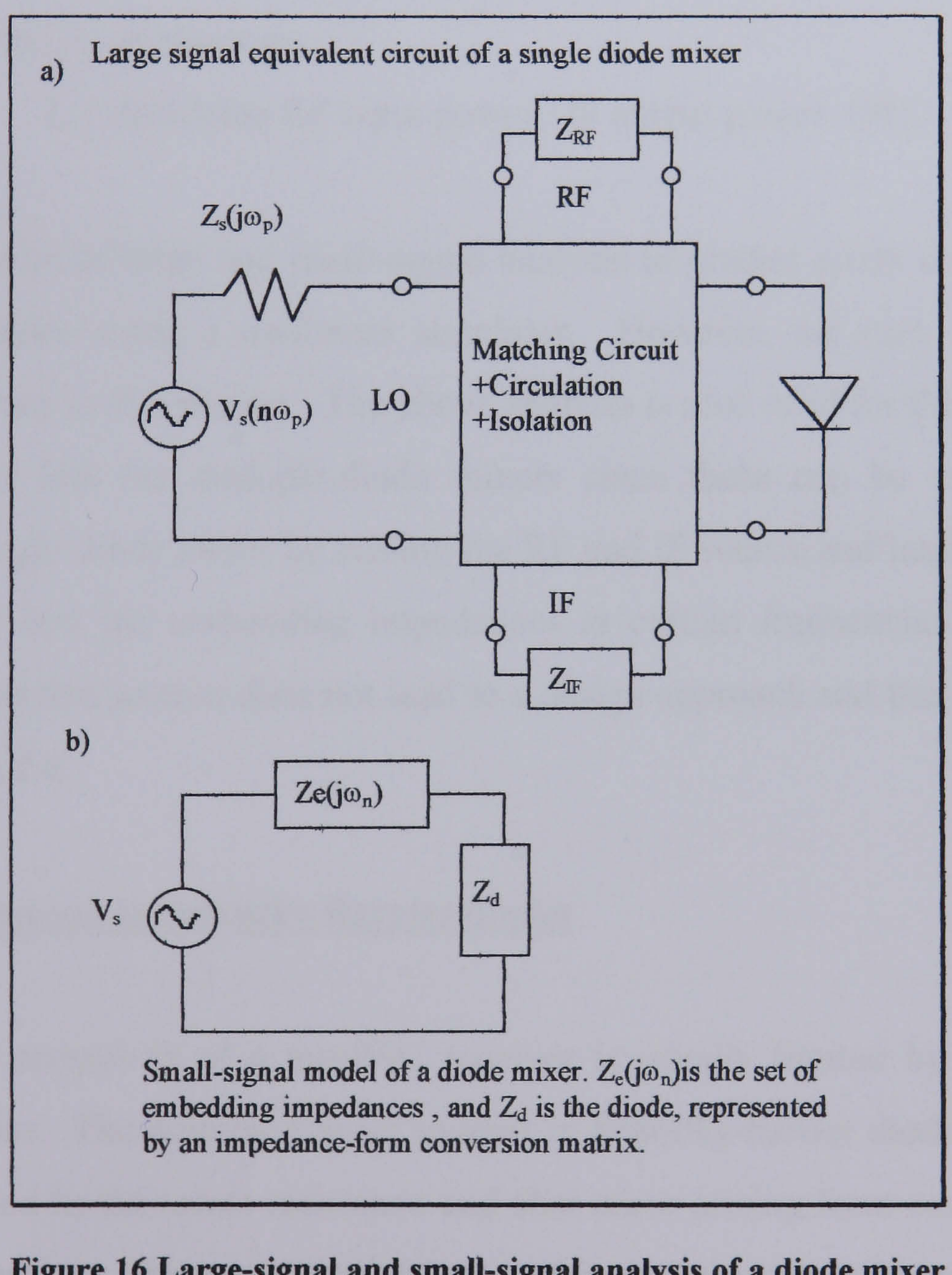


Figure 16 Large-signal and small-signal analysis of a diode mixer

Mixer conversion loss is found using the equivalent circuit shown in Figure 16(b). $Z_e(j\omega_n)$ is the set of embedding impedances at the mixing frequencies ω_n. These impedances are found by "looking back" into the network from the diode's

terminals. The magnitude of the voltage is found from the available power and $Z_e(j\omega_s)$, where ω_s is the excitation frequency:

$$V_s = \sqrt{8P_{av}\,\mathrm{Re}(Z_e(j\omega_s))} \quad \textbf{(34)}$$

$$P_{av} = \frac{V_s^{\,2}}{8\mathrm{Re}(Z_e(j\omega_s))} \quad \textbf{(35)}$$

The output power at the mixing frequency ω_n is:

$$P_n = 0.5\left|I(\omega_n)\right|^2 \mathrm{Re}(Z_e(j\omega_n)) \quad \textbf{(36)}$$

Therefore, mixer conversion loss is calculated from :

$$L_c = \frac{P_{av}}{P_n} \quad \textbf{(37)}$$

In simpler terms, L_c is given as:

L_c= Available RF input power / IF output power **(38)**

The computation of large and small-signal analysis to predict mixer conversion loss is normally done using a nonlinear simulator. However, no such software was available for use in this project. The above analysis is also valid for the computation of conversion loss for multiple-diode mixers since these can be reduced to an equivalent single-diode mixer by scaling the RF and IF source and load impedances, the LO level and the embedding impedances at certain frequencies. The mixer theory given in this section does not lead to a design approach and this is the subject of the section 2.4.

2.3.5 Noise sources in Schottky Barrier diodes

The ultimate sensitivity of a mmWIC receiver is usually limited by its internally generated noise. The dominant noise sources in Schottky-barrier diodes are thermal noise generated in the series resistance and shot noise arising from carrier emission across the junction. There are other effects such as hot-electron noise and intervalley scattering noise in GaAs which may influence mixer performance in poorly designed diodes.

Shot noise occurs in Schottky junctions because its current consists of a series of pulses that occur as each electron crosses the junction. The transit time in Schottky diodes is short so that the current waveform can be seen as a series of random impulses. Although the average number of pulses per second is constant, (and proportional to the dc current) the random nature of the impulses causes the instantaneous current to vary with time. These fluctuations in the junction current are a noise process.

The mean-square shot noise current in a forward-biased diode is given by:

$$\overline{i^2} = 2qI_jB \quad \textbf{(39)}$$

where q is the electron charge, I_j is the current in the resistive part of the junction and B is the bandwidth.

The other significant noise source is thermal noise in the series resistance. Thermal noise is present in any medium that dissipates power and has a temperature above absolute zero. Its source is the random, thermal agitation of electrons. Although thermal noise is frequency dependent, at frequencies below the submillimeter and temperatures above a few Kelvins, the noise power available from a resistor is a function of bandwidth and temperature and **not** frequency.

A resistor behaves as if it were noiseless and has a mean-square open-circuit noise voltage of :

$$\overline{v^2} = 4KTBR \quad \textbf{(40)}$$

so the available noise power in a bandwidth B is given by:

$$P_n = KTB \quad \textbf{(41)}$$

where R is the resistance, K is Boltzmann's constant, and T is absolute temperature.

2.4 Mixer Design

2.4.1 Internally-generated mixer noise

Before proceeding to discuss the most common forms of mixer design, it is important to consider the properties of mixers that will affect overall system performance. Some of these properties such as spurious signals and responses, intermodulation and saturation will be discussed in section 2.4.2. This section concentrates on how the mixer's noise will affect the operation of a complete receiver and the theory here is taken from [2.27]. These two sections together provide background to the discussion on different mixer types in 2.4.3.

Any noisy microwave component can be characterised by its noise figure, F, which is a measure of the input signal-to-noise ratio divided by the output signal-to-noise ratio.

This is defined as:

$$F = \frac{S_i / N_i}{S_o / N_o} \quad \textbf{(42)}$$

where S_i, N_i are the input signal and noise powers and S_o, N_o are the output signal and noise powers. The input noise power is assumed to be the noise power resulting from a matched resistor at $T_o = 290K$, so that $N_i = KT_oB$.

The signal-to-noise ratio is a measure of the ratio of the desired signal power to undesired signal power and so is dependent on the signal power. When noise and a desired signal are applied to the input of a noisy network, the output noise power will be increased more than the output signal power, so that the output signal-to-noise ratio will be reduced.

Figure 17 shows noise power N_i and signal power S_i being fed into a noisy two-port network.

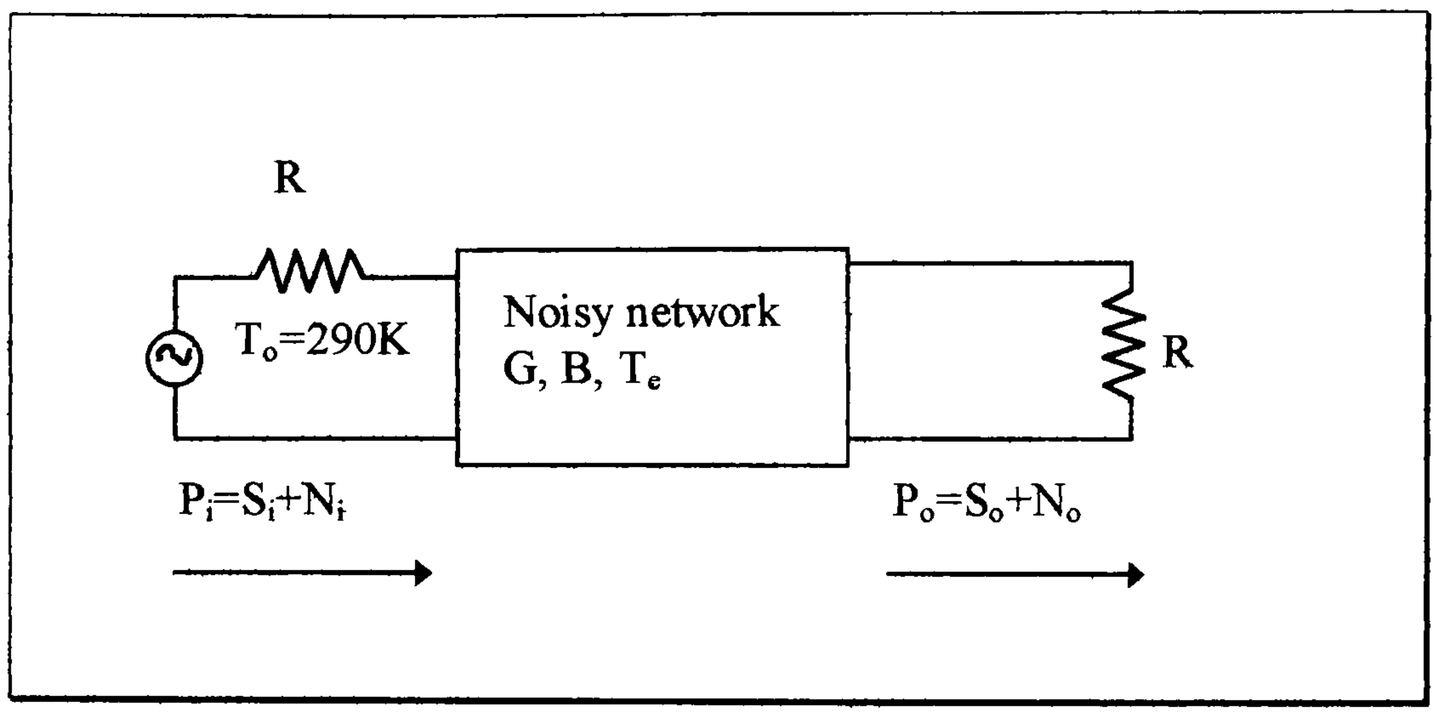


Figure 17 Determining the noise figure of a noisy network

The network is characterised by its gain, G, bandwidth B, and noise temperature T_e. Its noise figure is given by:

$$F = 1 + \frac{T_e}{T_o} \quad \textbf{(43)}$$

For a network which has an overall loss, L, (rather than gain G) at a temperature T, the noise figure is given as:

$$F = 1 + (L-1)\frac{T}{T_o} \quad \textbf{(44)}$$

In order to find the noise figure of a microwave system consisting of a cascade of several stages, it is possible to use the noise figure of individual stages as follows:

$$F_{cas} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \ldots\ldots \quad \textbf{(45)}$$

This idea is further demonstrated in Figure 18 below. In this case the noise figure of the cascaded system would be equal to the first two terms of equation **(45)**.

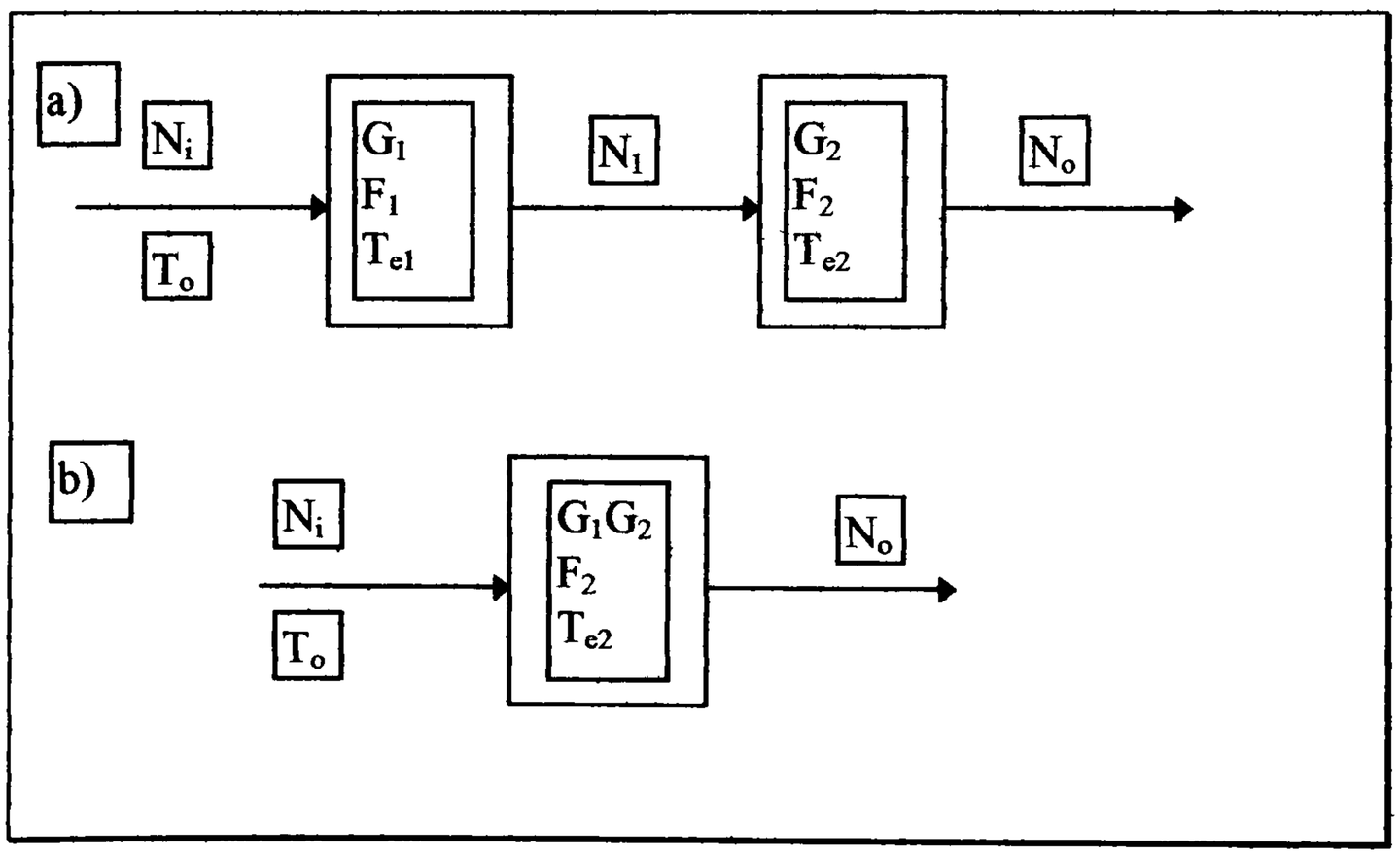


Figure 18 Noise Figure and equivalent noise temperature of a cascaded system

To analyse the overall effect of noise on a microwave receiver, consider the model shown in Figure 19, where P_t is the transmitter power, G_t and G_r are the transmit and receive antenna gains and R is the distance between the antennas. It is desired to find P_r the power received at the receiver. This is given in equation **(46)**.

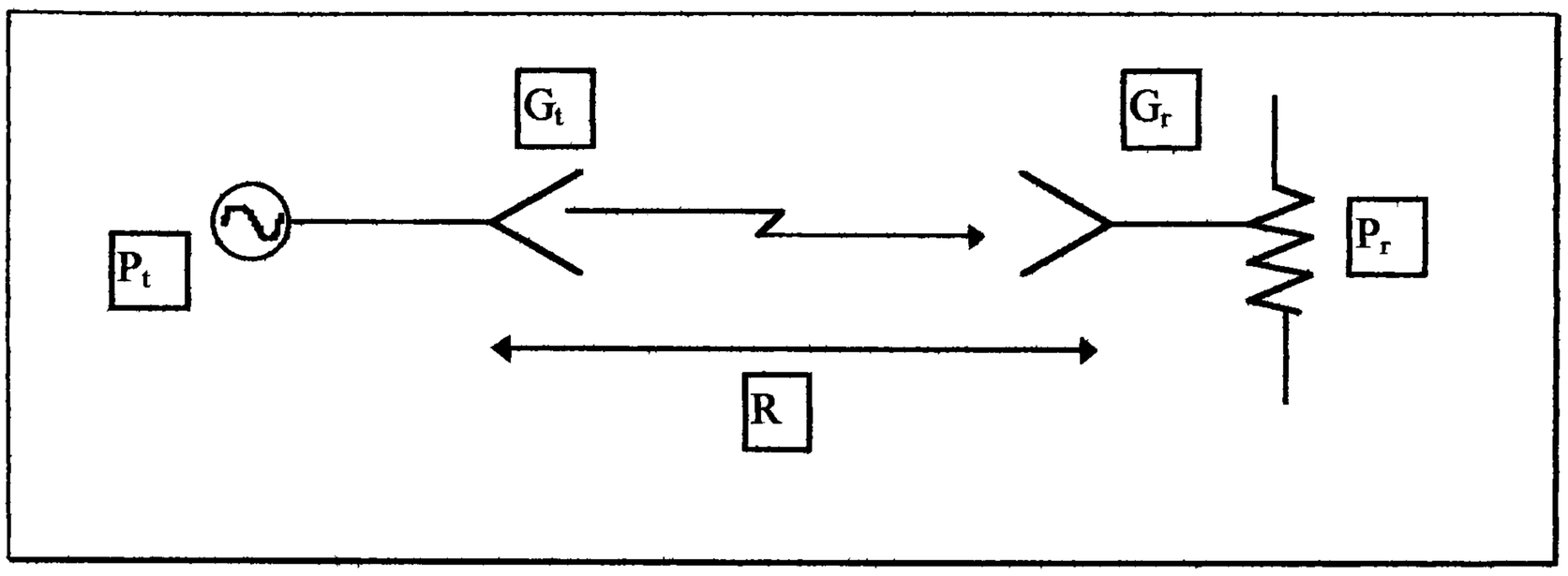


Figure 19 Simplifier microwave radio link

$$P_r = P_t \frac{G_t G_r \lambda^2}{(4\pi R)^2} \quad \textbf{(46)}$$

This is known as the *Friis power transmission equation.* It is the noise characteristics of the receiver that is of interest here. Therefore, consider the entire receiver shown below in Figure 20:

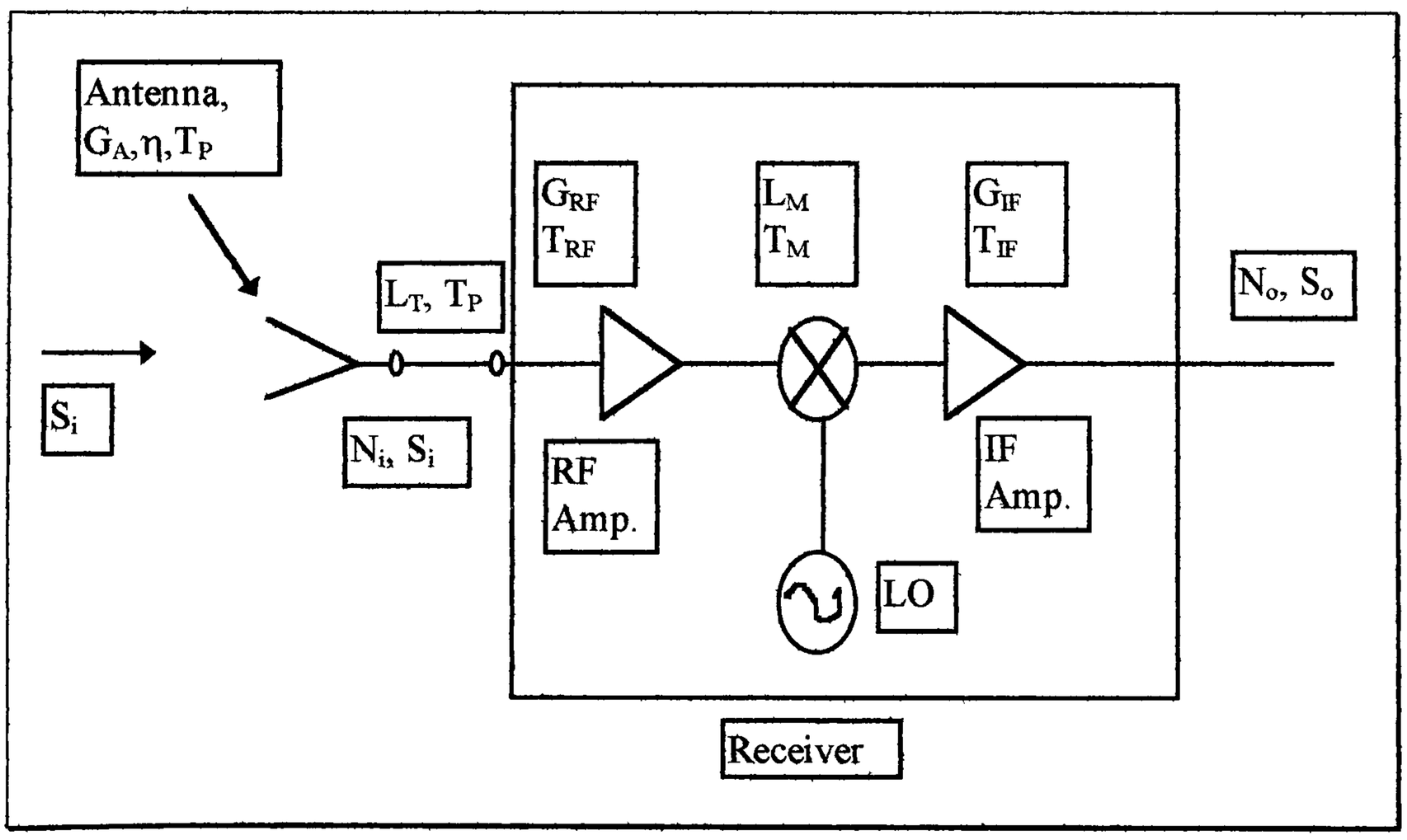


Figure 20 Noise analysis of a microwave receiver

From Figure 20, the total noise power at the output will be due to contributions from the antenna pattern, the loss in the antenna, the loss in the transmission line, and

from the receiver components. The noise power determines the minimum detectable signal level for the receiver.

The receiver components consist of an RF amplifier with gain G_{RF} and noise temperature T_{RF} , a mixer with an RF-to-IF conversion loss factor L_M and noise temperature T_M , and an IF amplifier with gain G_{IF} and noise temperature T_{IF}. Noise temperatures are related to noise figures by the equation:

$$T = (F - 1)T_0 \quad \textbf{(47)}$$

The equivalent noise temperature of the receiver can be written as:

$$T_{REC} = T_{RF} + \frac{T_M}{G_{RF}} + \frac{T_{IF} L_M}{G_{RF}} \quad \textbf{(48)}$$

Including the noise temperature of the transmission line connecting the antenna to the receiver (which has a loss L_T and a physical temperature T_P) :

$$T_{TL} = (L_T - 1)T_P \quad \textbf{(49)}$$

and so the noise temperature of the transmission line and receiver cascade is:

$$T_{TL+REC} = T_{TL} + L_T T_{REC} \quad \textbf{(50)}$$

Then the input noise at the antenna is:

$$N_i = KBT_A \quad \textbf{(51)}$$

where T_A is the antenna noise temperature and B is the system bandwidth. If S_i is the received power then the input signal-to-noise ratio at the antenna terminals is S_i/N_i.

The output signal power is:

$$S_o = \frac{S_i G_{RF} G_{IF}}{L_T L_M} = S_i G_{SYS} \quad \textbf{(52)}$$

G_{SYS} is defined as the system power gain.

The output noise power is

$$N_o = [N_i + KBT_{TL+REC}]G_{SYS} \quad \textbf{(53)}$$

$$= KB(T_A + T_{TL+REC})G_{SYS} \quad \textbf{(54)}$$

$$= KBT_{SYS}G_{SYS} \quad \textbf{(55)}$$

where T_{SYS} is defined as the overall system noise temperature.

The output signal-to-noise ratio is:

$$\frac{S_o}{N_0} = \frac{S_i}{kBT_{SYS}} \quad \textbf{(56)}$$

From this theory, it can be seen that the low-noise amplifier-mixer stage is the most critical in terms of overall noise figure. When choosing a mixer for this application to minimise overall noise figure, the combination of RF amplifier, mixer and LO must minimise noise passed to the IF stage whilst at the same time maximising the desired signal. So it is important to use low-noise components to keep losses to a minimum. After the mixer, the IF amplifier must have high gain with a narrow bandwidth and this leads to less noise power than if a high-gain RF amplifier were used alone. From equation **(48)**, the noise temperature of the IF amplifier is dependent on both mixer conversion loss and RF gain. Additionally, the use of an IF amplifier minimises the effect of 1/f noise. This section on noise figure also highlights the importance of choosing a mixer configuration which will minimise its contribution to the overall receiver noise figure.

2.4.2 System considerations for mixer performance

Mixer sensitivity is usually limited by this internally generated noise [2.8], but there are other practical factors which affect the performance of a mixer more than noise. These are listed below:

a) **AM noise in the LO** - the LO signal is often generated at a subharmonic of the required LO frequency and then multiplied to the desired frequency. The multiplier requires a high input level so it is necessary to amplify the signal at the subharmonic frequency. This adds noise, known as **AM noise,** or amplitude noise.

b) **Phase Noise** - this arises from low-frequency noise processes in the local oscillator. Little can be done to reduce this **phase noise**.

c) **Internally-generated spurious signals** - these are normally caused by the frequency synthesiser used to generate the LO signal.

d) **Intermodulation and saturation** - **intermodulation** is caused by the nonlinearities in the diode generating additional mixing components. **Saturation** is caused when the RF input level approaches the LO level , thus invalidating the small-signal assumption.

e) **Spurious responses** - these are caused by a harmonic of the LO other than the one used for the frequency translation.

2.4.3 Mixer types

Shown below in Figure 21 is a comparison of the basic format of the two most common forms of mixer - single-device and balanced mixers:

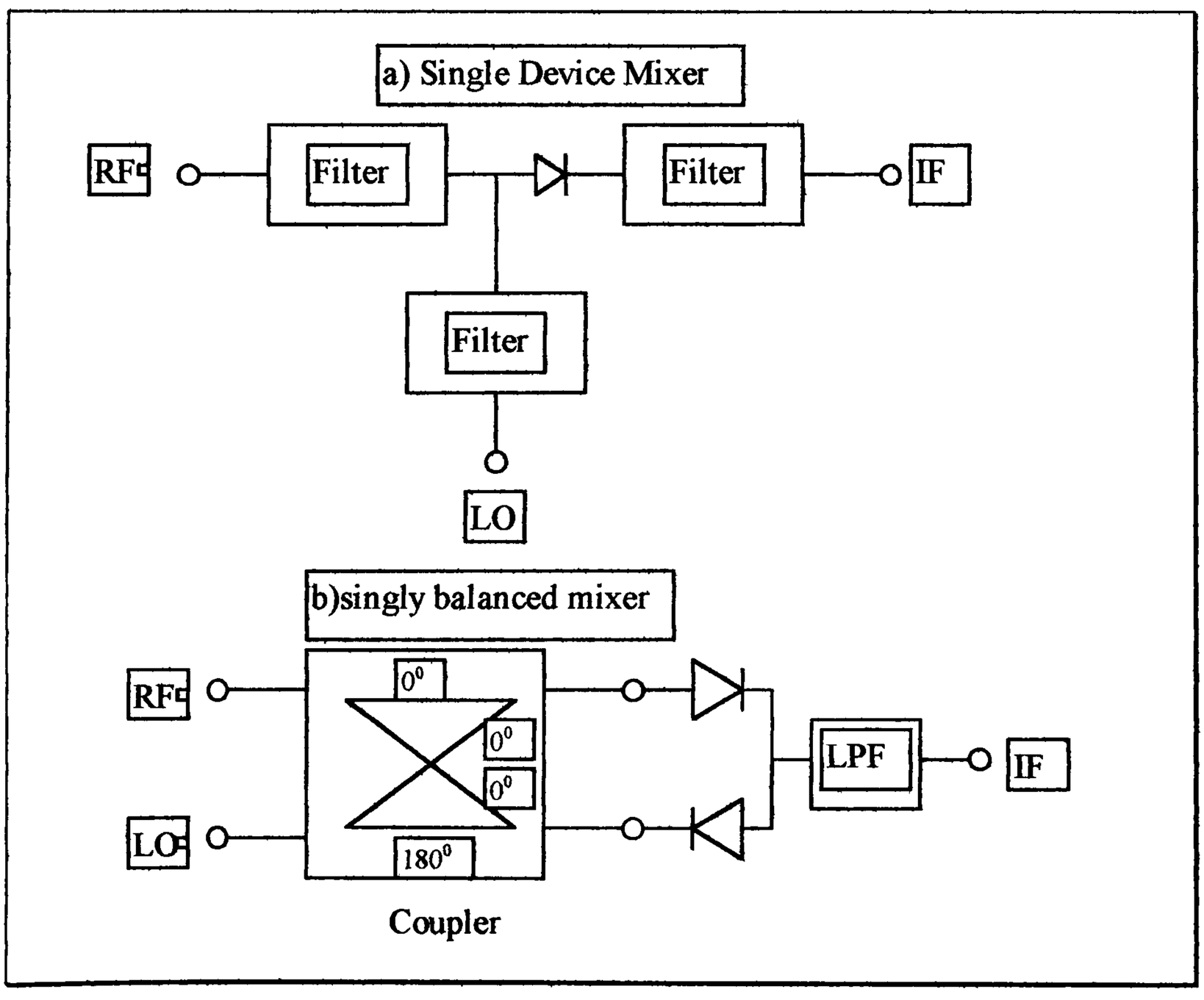


Figure 21 Comparison between single-device and balanced mixers

The design of single device mixers involves matching to the diode at LO, RF and IF frequencies. Therefore, it is necessary to determine the diode's input and output impedances at each mixing frequency. A typical design methodology used is as follows [2.9]:

1) Estimate diode junction capacitance, C_{jo}
2) Design the RF/LO matching circuit to match the diode's junction resistance
3) Design the IF matching circuit to match the diode's IF impedance
4) Adjust the diode DC bias and LO level to minimise conversion loss

Balanced mixers have several important advantages over single-device mixers:

a) RF and LO are inherently isolated
b) AM noise from the LO source is rejected
c) Improved power-handling capability
d) Certain spurious responses are rejected

From the theory for cascaded noise from Section 2.4.1, the properties of the balanced mixer should reduce the output noise figure from the overall mixer stage (ie the mixer + LO).

The main disadvantages of balanced mixers are:

1) poorer conversion performance than a single diode mixer (because it is difficult to apply DC bias or optimise the circuit without disturbing some of the advantages listed above).
2) More LO power is needed to drive the increased number of diodes.

In general balanced mixers can be either *singly balanced* or *doubly balanced.* Singly balanced mixers normally use two devices while doubly balanced mixers typically use at least four.

Figure 22 illustrates the operation of a singly balanced mixer (see Figure 21(b)). The RF voltages are in phase at the diodes as are the junction conductance waveforms of

the diodes. Hence the voltage and current components in the diodes are also in phase at the IF frequency.

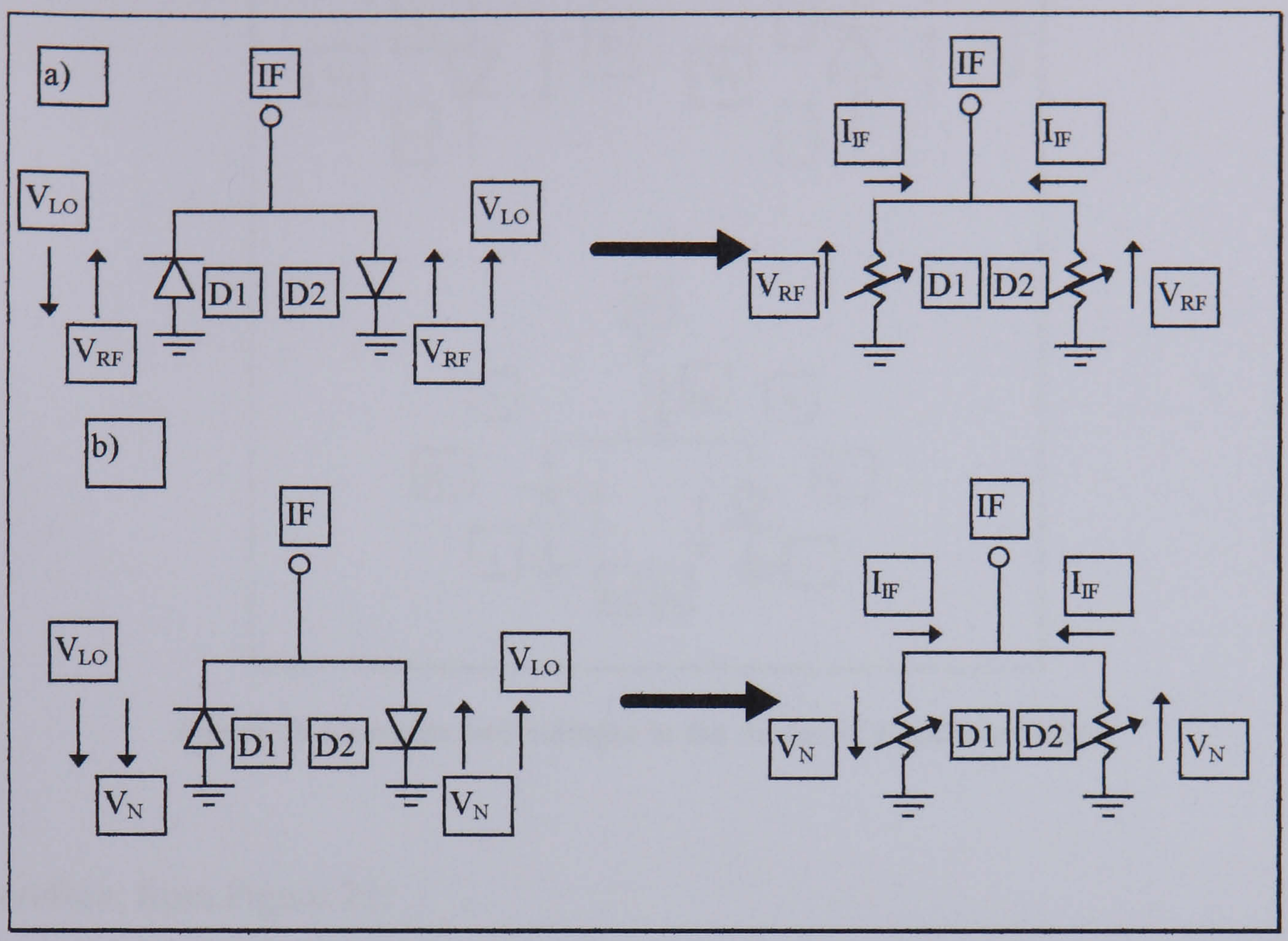


Figure 22 LO and RF phases in the balanced mixer

In Figure 22(b) the LO noise voltage components are 180^0 out of phase and so AM noise and certain spurious signals (not phase-modulated spurious signals) are cancelled.

The theory behind this is as follows and is illustrated in Figure 23:

The diode I/V characteristic is:

$$I_1 = aV_1 + bV_1^2 + cV_1^3 + \ldots. \quad \textbf{(57)}$$

V_1 is the total ac voltage across the diode (the RF plus the LO voltage)

If the diode is reversed then only the applied voltage is reversed,

$$I_2 = -aV_2 + bV_2^2 - cV_2^3 + \ldots. \quad \textbf{(58)}$$

and so the IF current, I_{IF}

$$I_{IF} = I_1 - I_2 \quad \textbf{(59)}$$

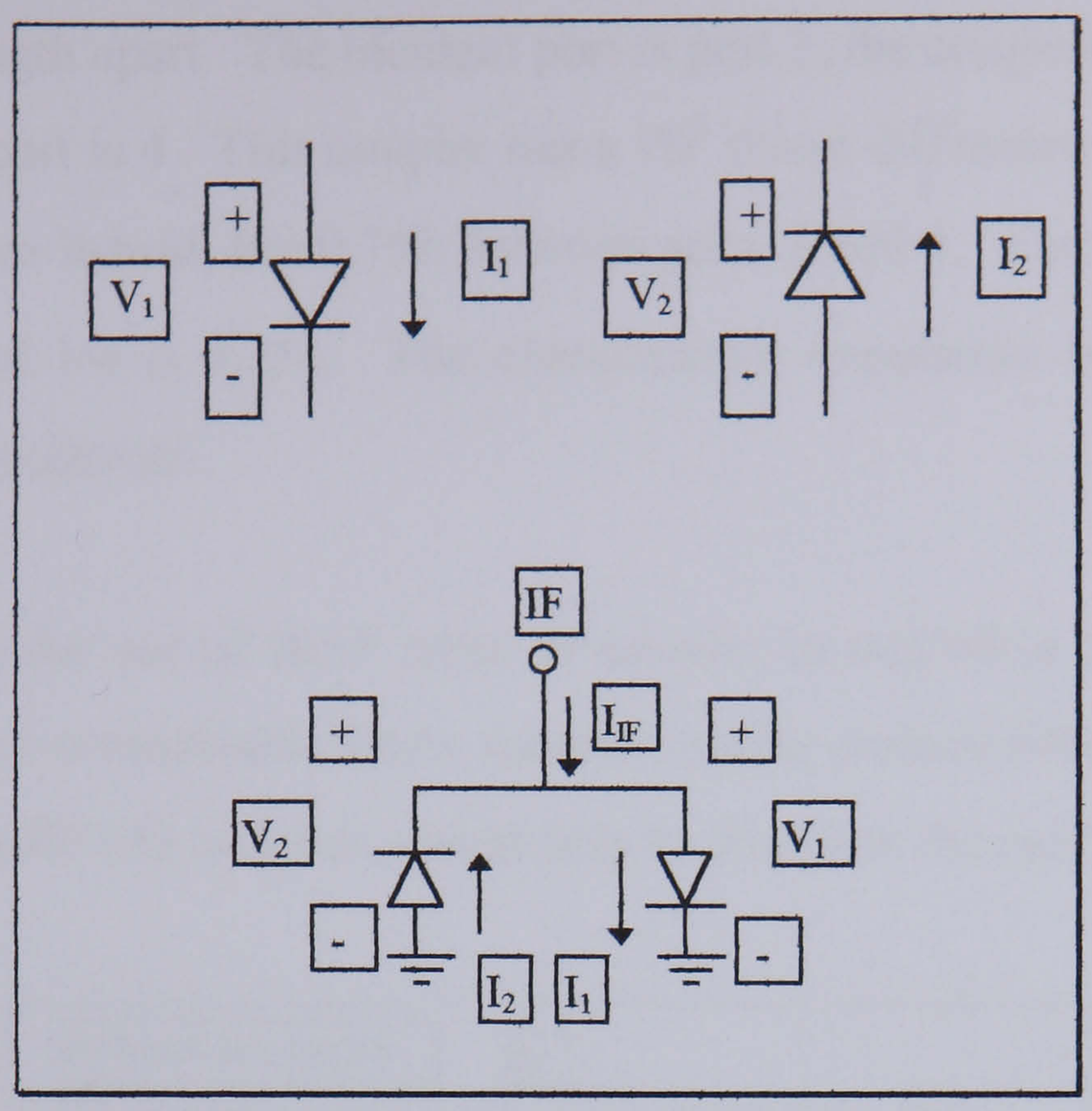


Figure 23 Currents and voltages in the diodes of a balanced mixer

Therefore, from Figure 23:

$$V_1 = -V_L\cos(\omega_p t) + V_{RF}\cos(\omega_p t) \quad \textbf{(60)}$$

$$V_2 = V_L\cos(\omega_p t) + V_{RF}\cos(\omega_p t) \quad \textbf{(61)}$$

Substituting equations **(60)** and **(61)** into **(57)** and **(58)** respectively, and then calculating the IF currents from **(59)** (take the a and b terms for simplicity) gives:

$$I_1 - I_2 = a2(V_{RF}\cos\omega_p t) + b(2V_L V_{RF}(1+\cos 2\omega_p t)) \quad \textbf{(62)}$$

This indicates clearly that the quadratic term contributes to the mixing process.

It is also possible to create a balanced mixer with the diodes having the same orientation. However, such a design would require a 180^0 IF hybrid. The advantage of such a design would be that DC bias could be used for the diodes.

The coupler, illustrated in Figure 21 (b), which is necessary to achieve phase difference between the RF and LO signals at the two diodes, may take several forms such as the rat-race hybrid or branch line coupler (see Figure 24). The branch-line coupler shown consists of two lines, coupled by two quarter wavelength lines, spaced

a quarter wavelength apart. The incident port is port 1, the coupled ports are 2 and 3 and the isolated port is 4. This coupler has a 90^0 phase difference between coupled ports. The rat-race hybrid, has 0.75λ between ports 2 and 4. The distance between ports 2-3, 3-1 and 1-4 is 0.25λ. The characteristic impedance of the ring is $\sqrt{2}$ times the port impedances.

It is obvious that the use of these types of coupler in mmWICs to achieve RF-LO isolation consumes considerable GaAs substrate space, even at 94GHz, so alternative ways of obtaining RF-LO isolation would help to minimise the mmWIC size.

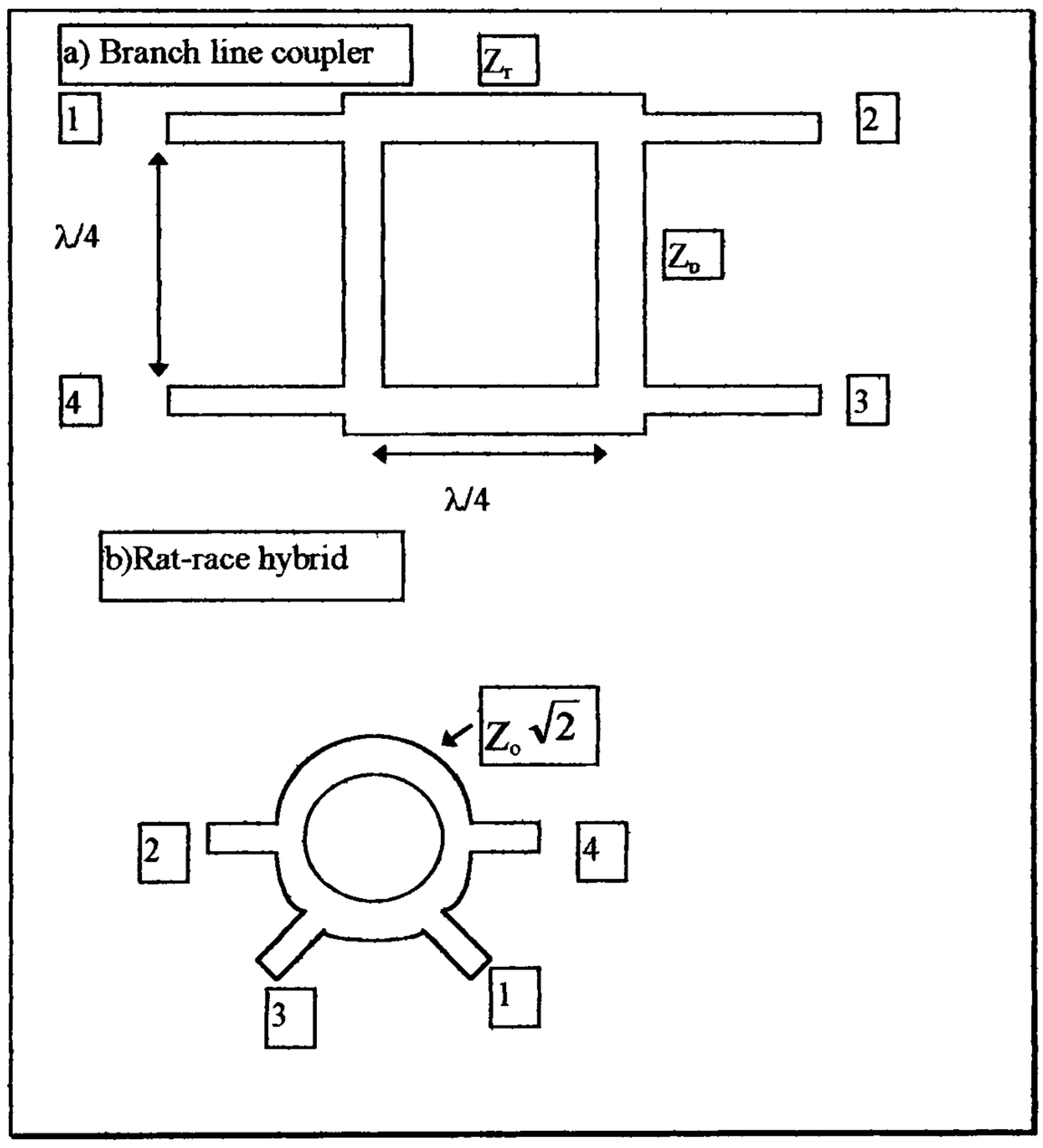


Figure 24 Illustration of typical mmWIC couplers

An example of a typical doubly balanced mixer is given in Figure 25. The advantages of doubly balanced mixers are that they provide inherent isolation between all ports, rejection of LO noise and spurious signals, and broadband operation. Their disadvantages are that they require at least four diodes and two hybrids whilst requiring greater LO power than both single-diode and singly balanced mixers.

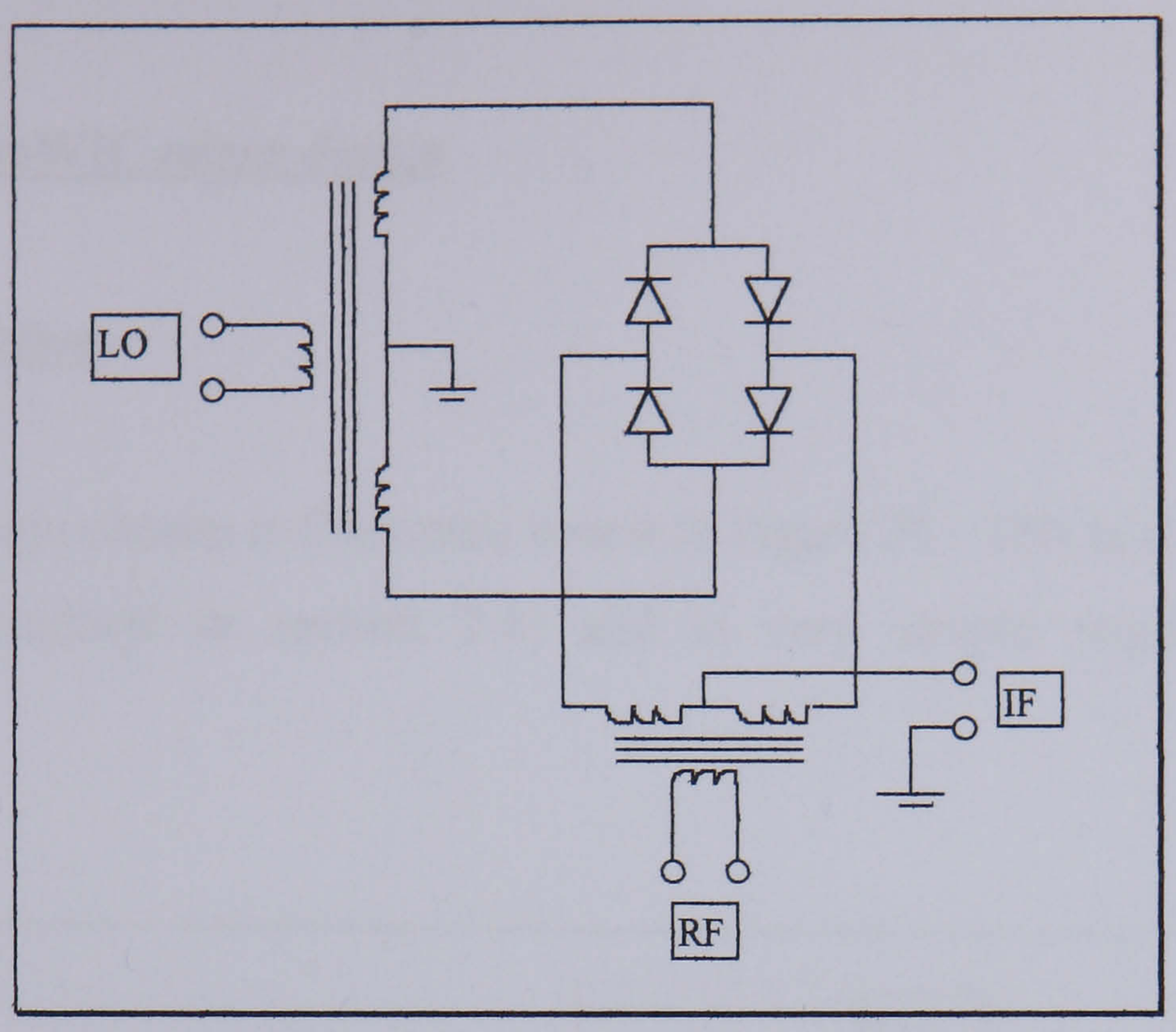


Figure 25 Doubly Balanced Mixer

2.5 94GHz mmWIC mixer design

2.5.1 Introduction

The mixer design chosen is illustrated below in Figure 26. This is a singly balanced mixer (as described in section 2.4) and is very simple requiring very few components.

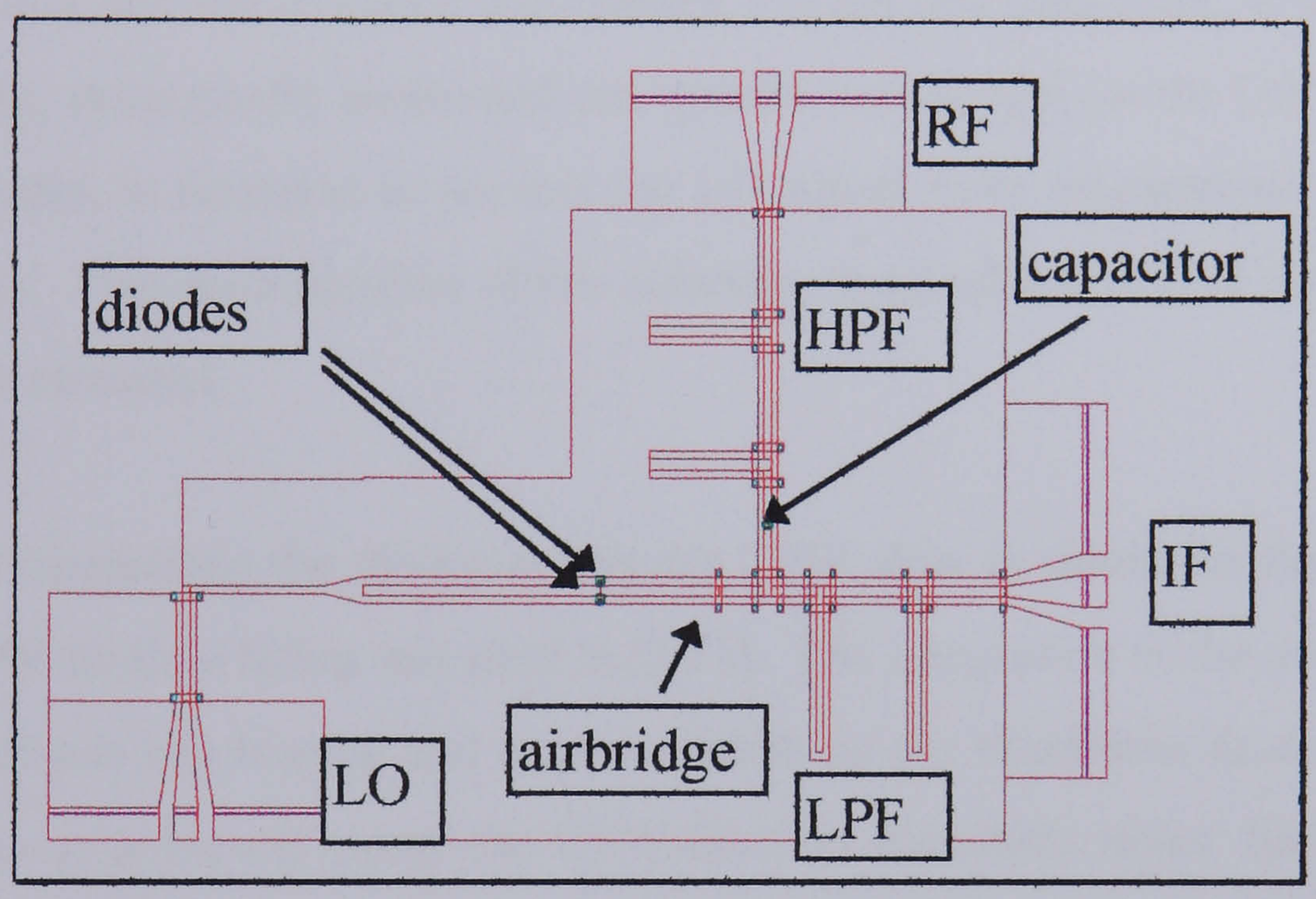


Figure 26 Schematic Layout of the 94GHz mmWIC mixer

2.5.2 Circuit operation

Referring to the circuit layout shown in Figure 26, the LO signal is input via a CPW-Slotline transition. The LO signal propagates along CPW, then to slotline and back to CPW, exciting a balanced mode in the CPW (see section 2.8). The RF signal is input via a high pass filter and so excites an unbalanced mode in the CPW (see section 2.8). Thus the RF and LO signals will be in phase at one of the diodes and out of phase at the other so providing the benefits of a singly balanced mixer. The RF signal is prevented from propagating out of the IF port via the low pass filter, by the presence of a capacitor (either MIM or interdigitated). This is important

because, although it is possible to design high and low pass filters individually, the interactions between the two must also be considered.

As the RF signal propagates along towards the diodes, note that at the transition from Slotline to Coplanar Waveguide the RF signal sees an open circuit to the unbalanced CPW mode. Therefore, the two diodes are positioned a half wavelength (at the RF frequency) from the transition so that the RF signal cannot propagate any further. Alternatively, the two diodes could be placed exactly at the Slotline-CPW transition. The LO signal excites a balanced mode in CPW and so at the diodes the RF and LO signals can mix and the IF signal must return, via the low pass filter, to the IF port. The airbridge, strategically positioned one quarter wavelength (at the LO frequency) from the diodes, is intended to prevent the LO signal from propagating out the RF and LO ports. The exact position of this airbridge is calculated so that the LO signal will be short circuited.

The idea of integrating the diodes across the CPW slots is similar to that in [2.10] whilst a CPW-Slotline balun was used in [2.11]. The integration of the diodes across the slots prevents any biasing and imposes limits on the maximum diode size. RF-LO isolation is achieved using the CPW-Slotline transition rather than a hybrid coupler, whilst RF-IF isolation is achieved using a capacitor. The individual circuit component design is now given.

2.6 Diode Design

2.6.1 Diode layout

A good Schottky junction requires a lightly doped, thin epitaxial layer grown on a heavily doped substrate. The ohmic contact (ie cathode) can be made to this heavily doped substrate, as shown below in Figure 27. Since the high conductivity buffer layer extends under the epilayer, current uniformity is good and series resistance is low. The anode is formed on the edge of the mesa and connection is made to the substrate using an airbridge.

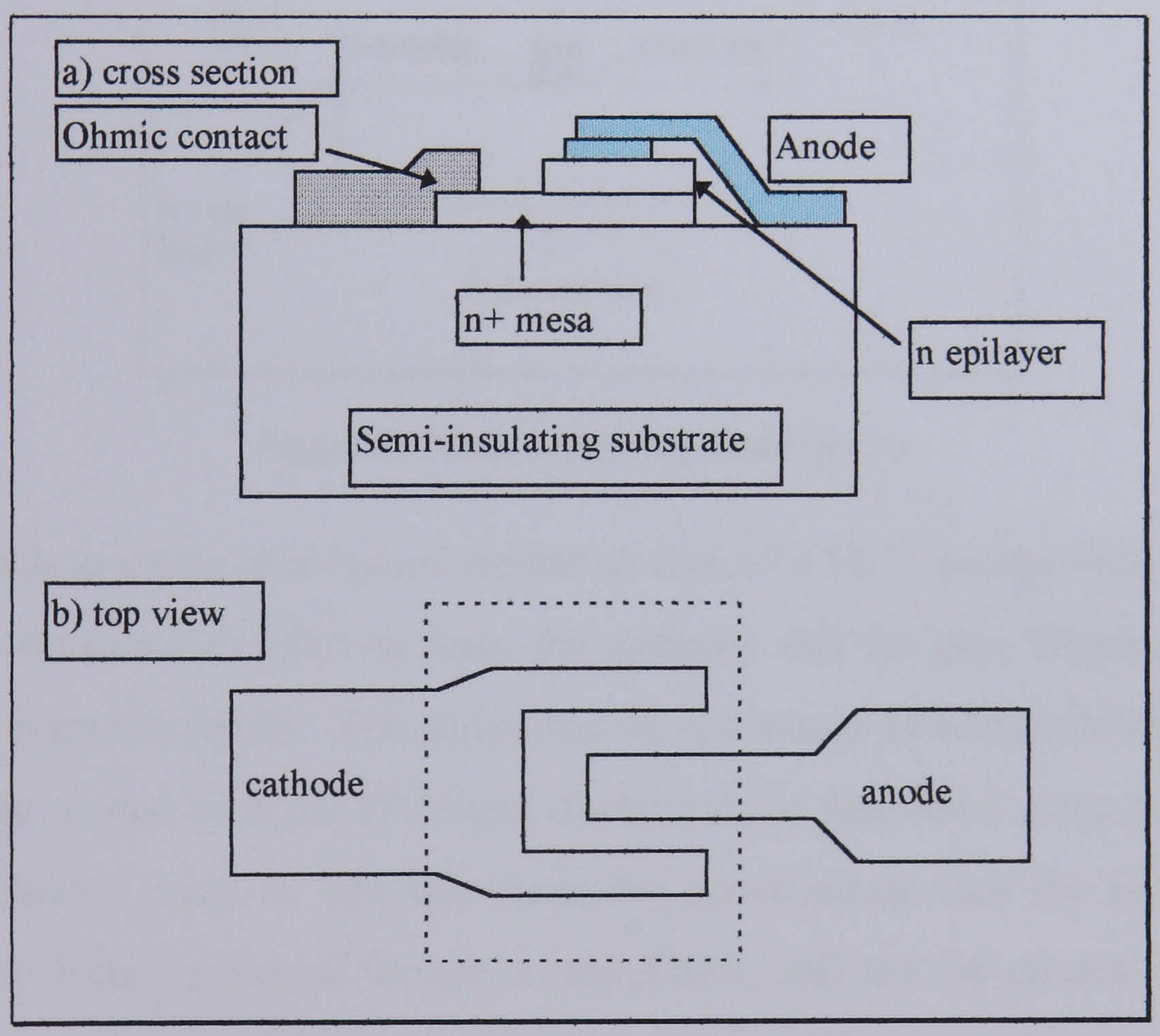


Figure 27 Good Schottky Diode design

However, such a layer structure is unsuitable for integration with FETs, which have the heavily doped and lightly doped layers the other way around (see section 2.7). The diode design most easily integrated with FETs is given in Figure 28 (for a two-finger diode).

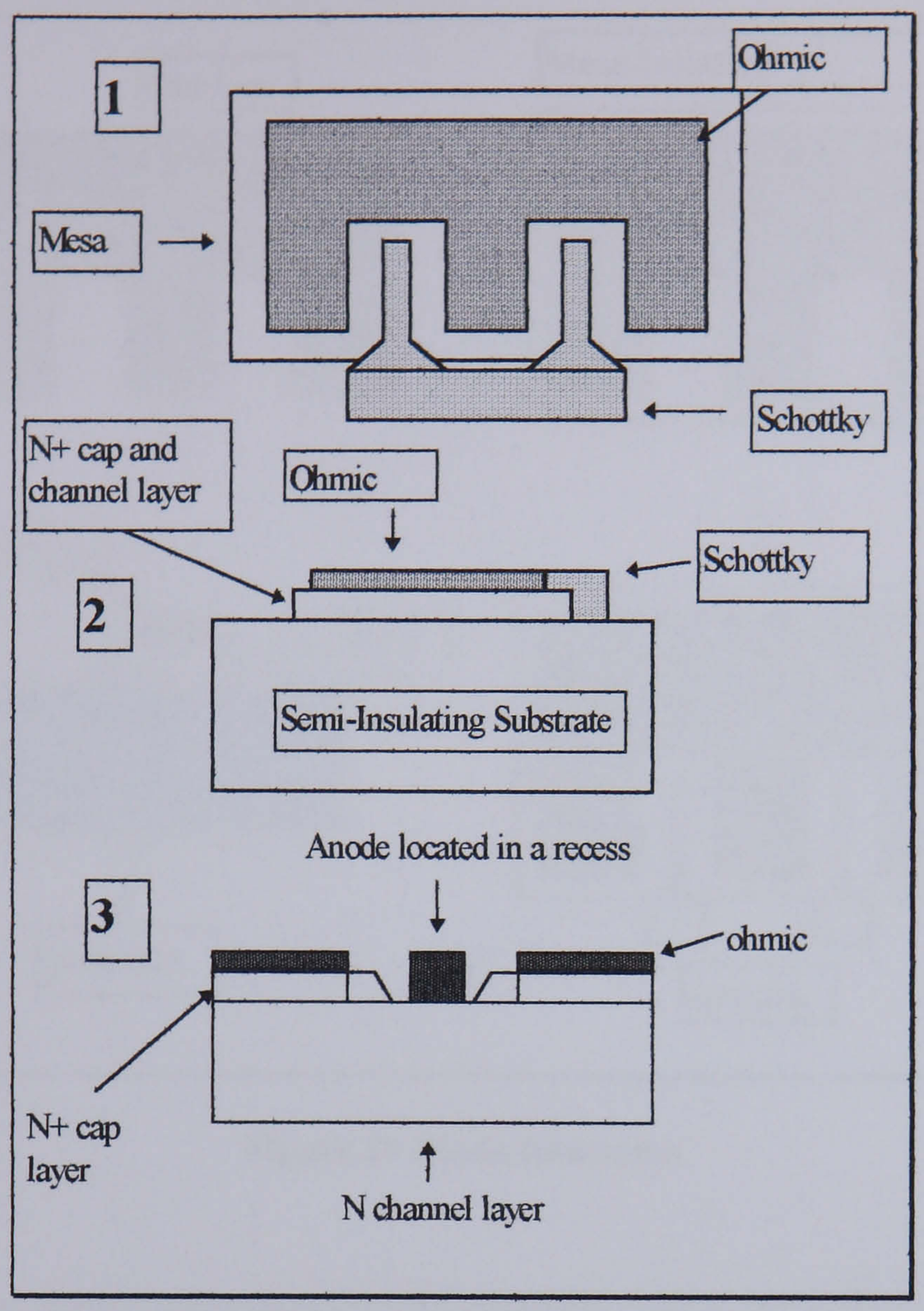


Figure 28 Diode design and cross section

This basically consists of a layout similar to that of a FET, except with the source and drain connected together to form the **cathode** and the gate fingers connected together to form the **anode.** The design has the advantage of compatibility with FET technologies so that both the FETs and diodes can be fabricated using one process. However, diodes made in this way have the disadvantage that the FET material structure has been optimised for use in amplifiers, and not for diodes. The ohmic metal forms a contact with the heavily doped $\mathbf{n^+}$ cap layer, which is necessary for low contact resistance. In order that a good Schottky contact can be achieved, the anode metal forms a barrier with the n-channel layer of the FET structure - therefore the anode is often located in a recess (ie the $\mathbf{n^+}$ cap layer is etched away and the anode is directly deposited on the n-channel layer). The doping of the $\mathbf{n^+}$ cap layer and control of the width and depth of the recess are important in order to minimise series resistance.

The diode fabrication process is illustrated in Figure 29 overleaf:

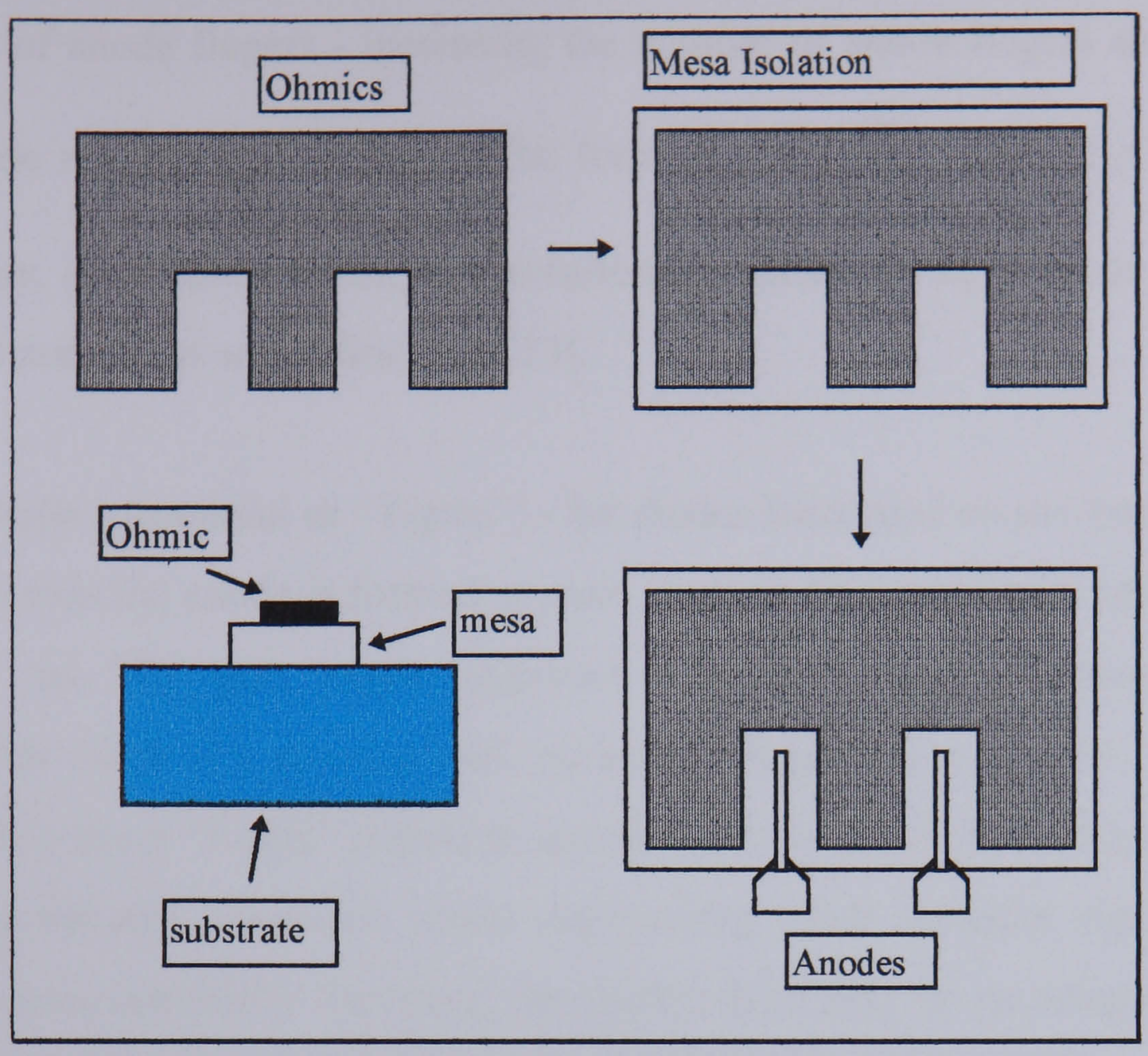


Figure 29 Diode formation

In order to find out how diode parameters/characteristics are affected by such factors as material choice, dimensions and other processing/design features, the variables listed below were investigated. The purpose of these investigations were to find the optimum diode characteristics, and to attempt to "engineer" a diode (using basically a FET material structure) that is comparable in performance to one that may be used in a typical hybrid circuit at W-Band.

a) anode-cathode spacing - this is a trade off between minimising series resistance (which requires small anode-cathode spacing) and parasitic capacitance (which requires large anode-cathode spacing).

b) anode width - as the total anode area (A) is increased then the diode's junction capacitance should increase. Referring to [2.2], diode series resistance should decrease as junction area increases by an approximate $1/\sqrt{A}$ relation.

c) anode length - the above explanation for anode width also applies here.

d) number of anode fingers - increasing the number of anode fingers should affect the anode resistance according to the formula: $R = \frac{\rho Z_g}{3hL_g m}$ where ρ is metallic resistivity, Z_g is anode width, h is metallisation thickness, L_g is anode length and m is the number of anode fingers [2.13].

e) anode shape (pyramidal or "T-gate") - for diodes fabricated on the same substrate as FETs then the anode is formed at same stage as FET gate level which use "T-gates". As FET gate lengths approach 0.2μm, the gate resistance becomes intolerably large if a conventional, pyramidal shaped gate is used. Therefore, most FETs use a "T-gate" profile to increase the overall cross-sectional area thus reducing metallic resistance whilst maintaining small footprint dimensions for faster device operation. However, for diodes there may be no advantage gained by having a "T-shaped" anode at small anode finger lengths.

f) Ohmic metallisation (recipe, anneal time and temperature) - the requirements here are to minimise the contact resistance whilst keeping a uniform morphology.

g) Wet etch/dry etch recess/No recess - to enable ultimate integration with FETs in a MMIC downconverter, it would be preferable to use a dry etch process for anode recessing. It is known that dry etching can induce damage in III-V semiconductors [2.12] and, although recess offset is less controllable by wet etching, a wet etch process was used in diode formation to provide a comparison with values of series resistance from dry etched diodes. It was also not clear whether there was any advantage to be gained from recessing the anode contact except perhaps for a better ideality factor due to the higher doping of the cap layer.

h) GaAs MESFET or pHEMT - although GaAs pHEMTs are almost universally used at W-Band for amplifiers, GaAs MESFETs have been used at lower frequencies [2.14] and a comparison of diode performance between these two material structures was thought useful.

i) pHEMT electron mobility - an increase in electron mobility will correspondingly reduce the resistivity of material between anode and cathode and therefore should result in lower values of series resistance.

j) Alternative diode layout - cross shaped anode - practical diodes consist of a small anode on a large semiconductor surface and so electric field near the edge of the metal anode is greater than the field in the centre. Therefore, the current density is greatest at the edge of the junction and so series resistance depends more on the junction periphery than area.

2.6.2. Diode Parasitics

As discussed earlier in Section 2.3, the two important diode parasitics are junction capacitance and series resistance. A description of these two diode parameters is now given.

2.6.2.1 Series Resistance

Figure 30 shows the sources of series resistance associated with the chosen diode layout.

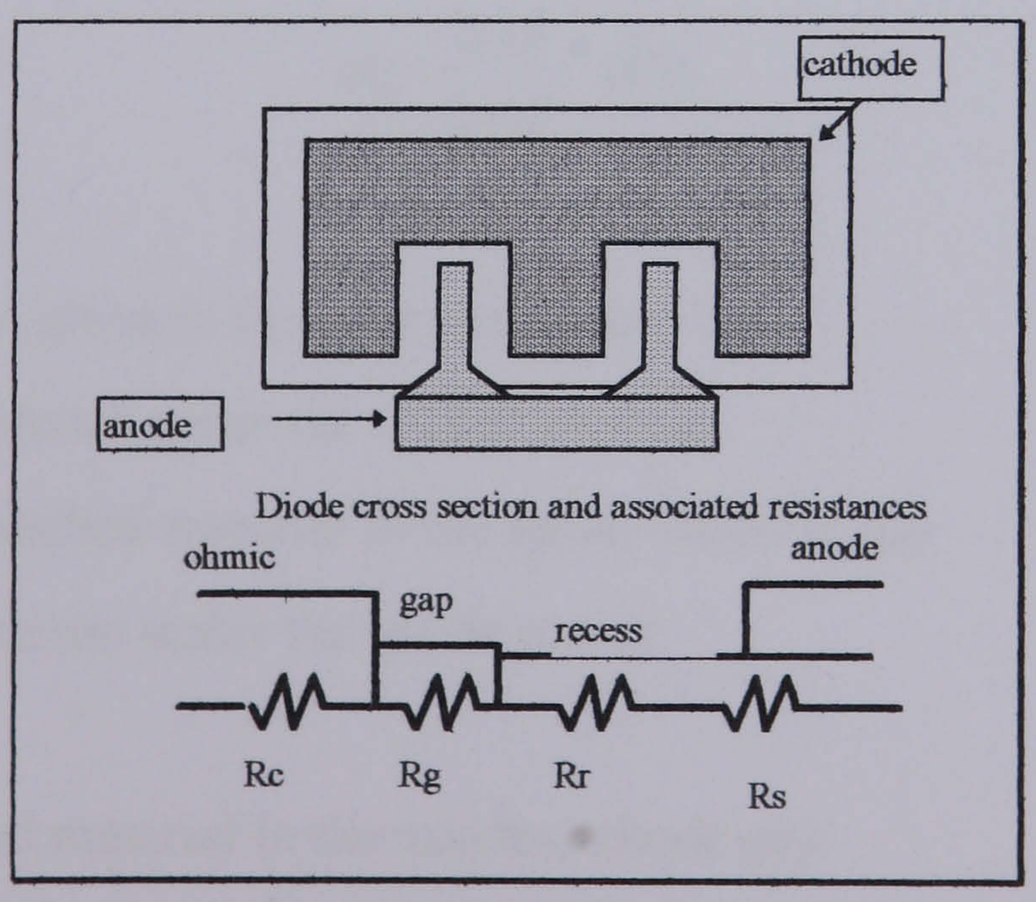


Figure 30 Diode cross section and associated resistances

From Figure 30, the following quantities are defined:

Rc - Ohmic contact resistance

Rg - resistance of unetched material in anode-cathode gap

Rr - resistance of anode recess offset region

Rs - spreading resistance under the anode

Rm - metallic resistance of the anode

n-number of anode fingers

With the exception of anode metal resistance, all values of resistance depend only on anode width, not the number of anode fingers. The spreading resistance is distributed, and so effectively divided by three. [2.13]

Total resistance is:

$$R_t = R_m + [R_c + R_g + R_r + (R_s/3)]/2 \quad \textbf{(63)}$$

$$R_c = \rho_c / w_g n \quad \textbf{(64)}$$

$$R_g = \frac{l_o \rho_u}{w_g n} \quad \textbf{(65)}$$

$$R_r = \frac{l_r \rho_e}{w_g n} \quad \textbf{(66)}$$

$$R_s = \frac{l_g \rho_e}{2 w_g n} \quad \textbf{(67)}$$

The other quantities given in the above equations are:

ρ_c - resistivity of material under the Ohmic contact

ρ_u - resistivity of unetched material in the anode-cathode gap

ρ_e - resistivity of material under the anode recess

w_g - anode width

l_o- length of unetched material in the anode-cathode gap

l_r - length of recess between the anode metallisation and the unetched material in the anode-cathode gap

l_g - length of anode finger

Possible ways of reducing the diode series resistance would be as follows:

1) $\mathbf{R_m}$ - In order to reduce the metallic resistance, the cross sectional area of the gate metallisation could be increased.
2) $\mathbf{R_c}$ - contact resistance coulde be reduced by optimising the Ohmic contact recipe and the annealing conditions.
3) $\mathbf{R_g}$ could be reduced by minimising the anode-cathode separation.
4) Both $\mathbf{R_r}$ and $\mathbf{R_s}$ could be reduced by careful control of anode recess offset and the anode length.

2.6.2.2 Junction Capacitance

From [2.13], the capacitance per finger for a Schottky diode is:

$$C = \frac{\varepsilon Z L}{d}\left(1 + \frac{2d}{L} - \frac{4d}{L+2d}\right) \text{ F} \quad \textbf{(68)}$$

where Z is anode width, L is anode length, and d is depletion depth.

The most obvious way of reducing diode junction capacitance is to minimise junction area. However, this is a trade-off with minimising series resistance.

2.7 Material Structures for use in the project

2.7.1 Introduction

As mentioned earlier in section 1.3, the most mature technology used at 94GHz is the GaAs pseudomorphic HEMT. The basis of the project was to manufacture mixer circuits suitable for integration with LNAs to form a downconverter. Therefore, a GaAs pHEMT structure was used along with the GaAs MESFET structure, already well characterised at the University of Glasgow. In fact, the FET fabrication process developed at Glasgow has largely been optimised for the manufacture of MESFETs. Both the pHEMT and MESFET material structures used in the project were grown by **MBE** (molecular beam epitaxy) at the University of Glasgow. A simple explanation of these material structures is now given.

2.7.2 GaAs pseudomorphic HEMT

In order to understand how the **P**seudomorphic **H**igh **E**lectron **M**obility **T**ransistor (**pHEMT**) can be used as a diode it is necessary to examine its structure:

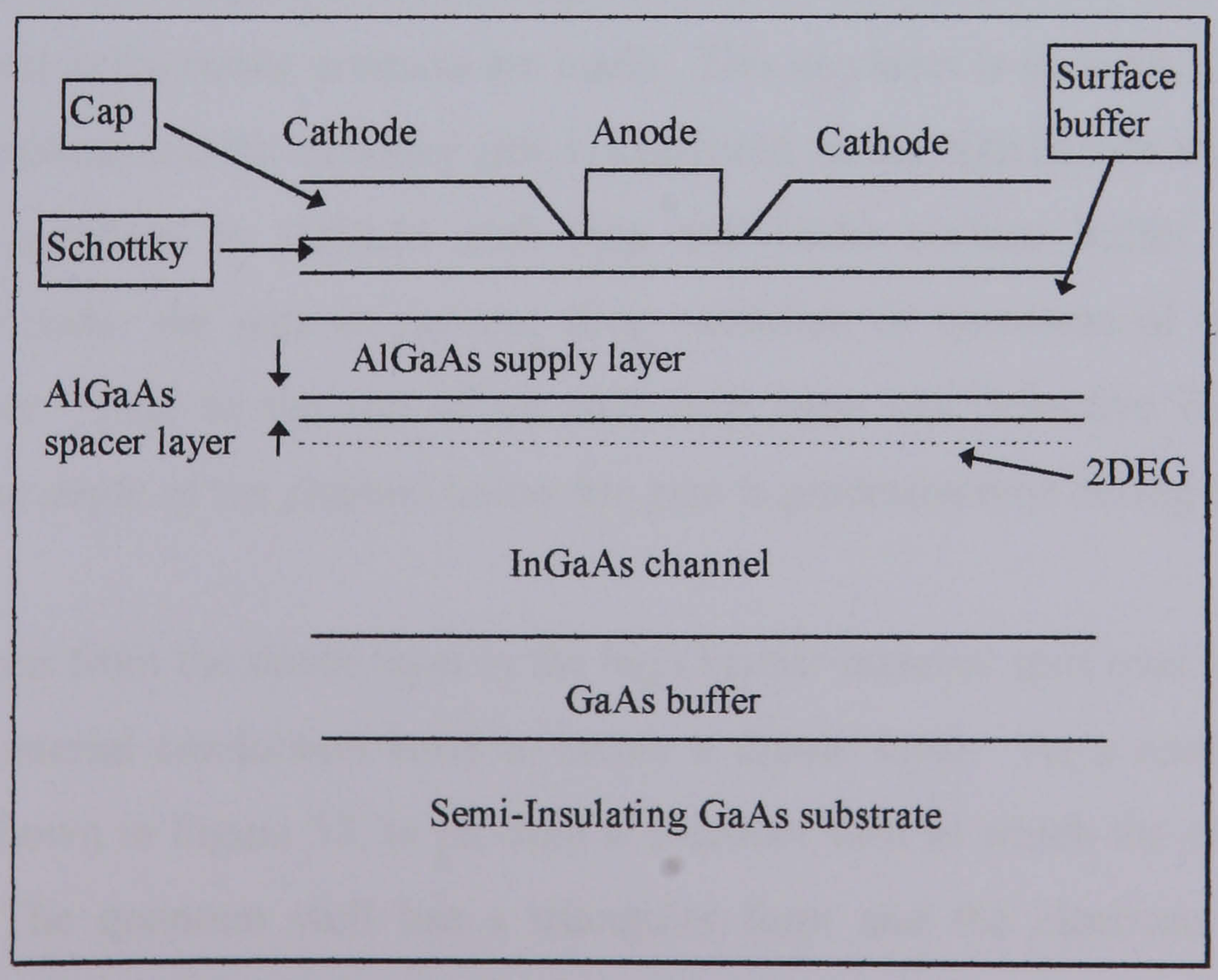


Figure 31 Pseudomorphic High Electron Mobility Transistor

The layers which comprise this material structure are detailed below:

GaAs pseudomorphic HEMT - Table 2.2

Layer thickness	Layer	Description
30nm	$4x10^{18}cm^{-3}$ GaAs	cap
5nm	$Al_{0.3}Ga_{0.7}As$	etch stop
2.5nm	GaAs	surface buffer
10nm	$Al_{0.3}Ga_{0.7}As$	barrier
	$7x10^{12}$ cm^{-2} Si	delta doping
5nm	$Al_{0.3}Ga_{0.7}As$	spacer
10nm	$In_{0.2}Ga_{0.8}As$	channel
600nm	GaAs	buffer

Figure 31, along with Table 2.2, show the structure of the GaAs pHEMT grown at the University of Glasgow [2.15]. Upon the semi-insulating layer, a thick buffer is grown to prevent substrate impurities from affecting device performance. The thin, undoped $In_{0.2}Ga_{0.8}As$ is a strained, pseudomorphic channel layer. A heterostructure is formed by a thin $Al_{0.3}Ga_{0.7}As$ spacer layer, with the remaining barrier material on top. The 5nm $Al_{0.3}Ga_{0.7}As$ layer is used to physically separate donor atoms from the channel thus increasing electron mobility. Finally, a heavily doped GaAs cap layer is grown to which the ohmic contacts are made. This cap layer is typically etched away using dry etching and the Schottky gate is deposited on the high barrier material. For reliability purposes an AlGaAs etch stop and GaAs surface buffer layer were introduced under the gate to prevent deep oxidation or corrosion of the AlGaAs supply layer. Due to the use of an etch stop layer and Selective Reactive Ion Etching, the depth of the channel below the gate is predetermined during growth.

The electrons from the donor layer in the high barrier material spill over into the low bandgap material conduction band to create a dipole layer. As a result the band bends as shown in Figure 32, to produce a quantum well in which the electrons are trapped. The quantum well has a triangular form and the electrons have two-

dimensional properties (ie they are free to move in the plane of the device but are confined in the growth direction).

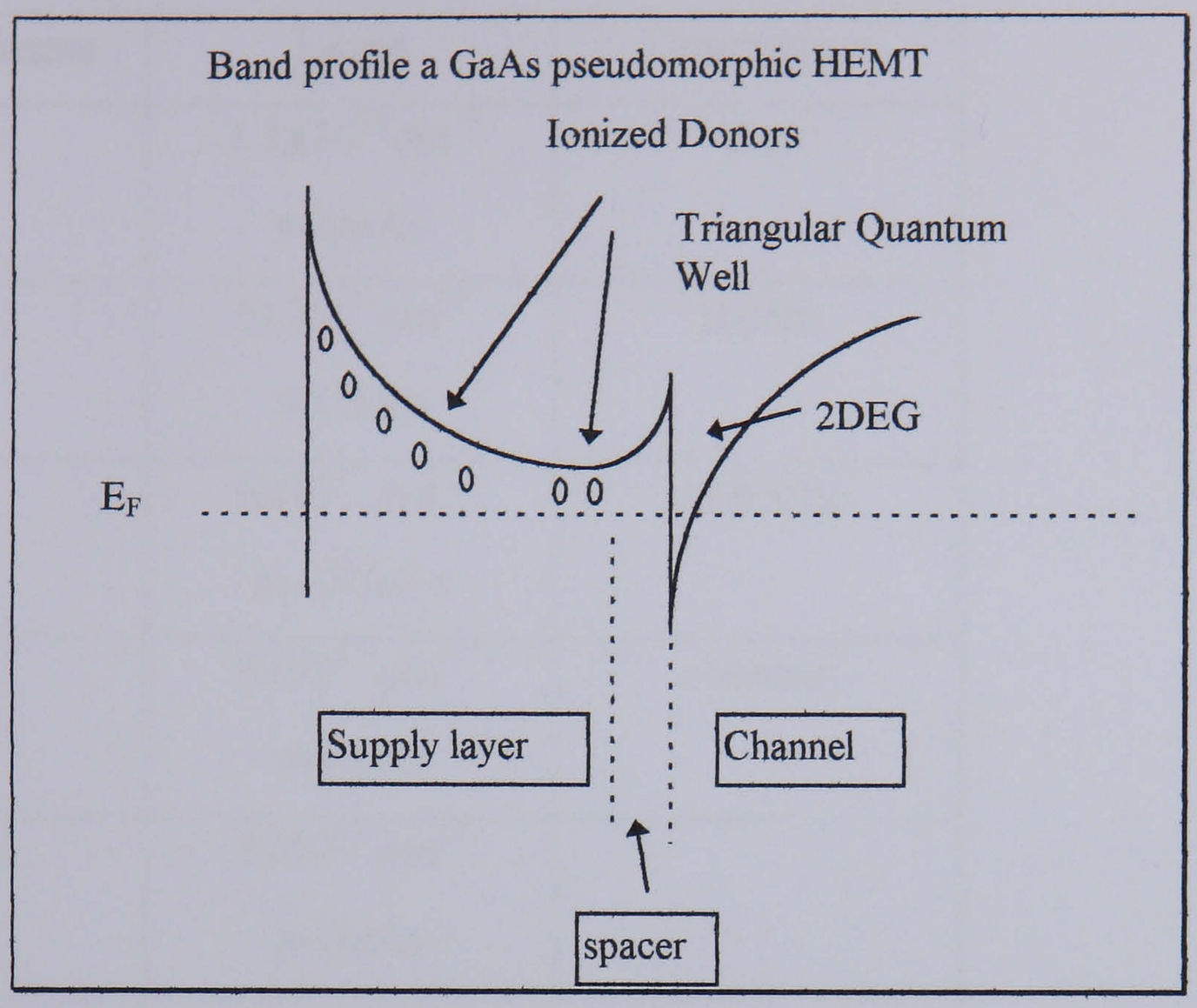


Figure 32 Energy Band Diagram of a HEMT

2.7.3 GaAs MESFET

In comparison to the pHEMT, the **M**etal **S**emiconductor **F**ield **E**ffect **T**ransistor **(MESFET)** is a simpler structure. As illustrated below in Figure 33, the basic MESFET structure comprises an epitaxially grown channel on an undoped substrate, separated by a buffer layer.:

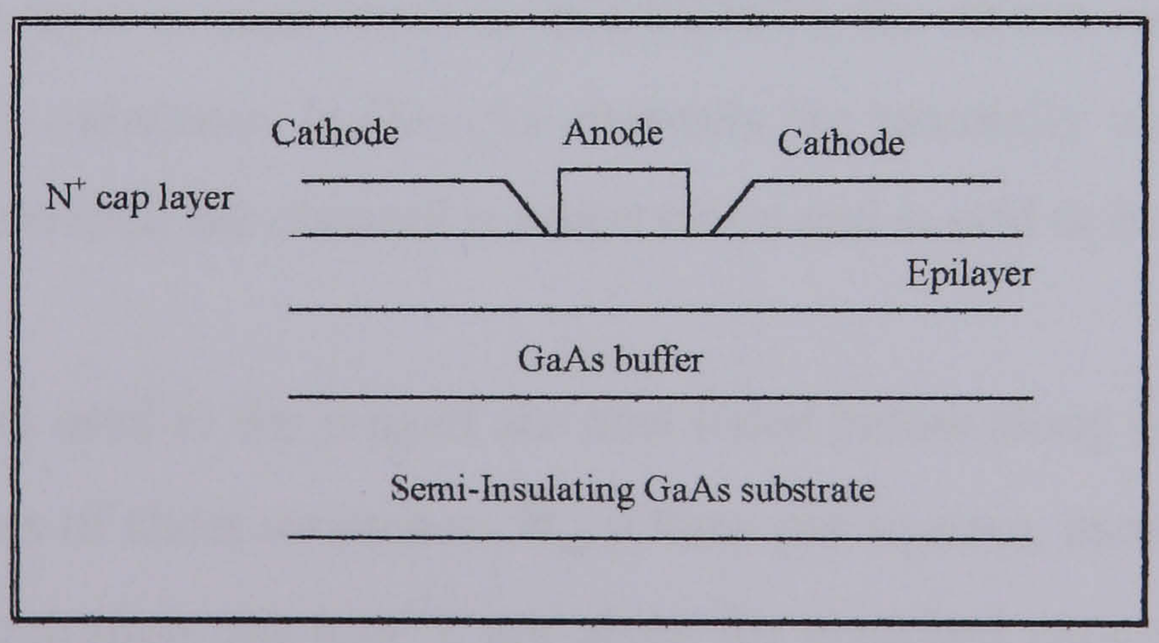


Figure 33 Metal Semiconductor Field Effect Transistor

The layers used in this are detailed below:

GaAs MESFET - Table 2.3

Layer thickness	Layer	Description
15nm	$1.1x10^{18}cm^{-3}$ n-GaAs	cap
24nm	$5x10^{17}$ cm^{-3} n-GaAs	recess
5nm	$5x10^{17}$ cm^{-3} n-AlGaAs	etch stop
56nm	$5x10^{17}$ cm^{-3} n-GaAs	channel
100nm	$5x10^{15}$ cm^{-3} p-GaAs	
100nm	undoped GaAs	

Key advantages of the GaAs pHEMT over the more conventional MESFET are:

a) High mobility due to the elimination of scattering caused by ionized impurities. Due to the physical separation of dopants from the free electrons, mobility is improved. This improved mobility enables the device to have low resistance between the source and gate region.

b) Use of high quality material in the channel. Normally, materials such as InAs cannot be used in MESFETs as these narrow bandgap materials are defect prone, but when only a thin layer is used (such as in a HEMT), the device can be quite robust [2.16]. On GaAs substrates $In_xGa_{1-x}As$ channels are generally used . In the case where x is non zero then the channel is under strain and is said to be *pseudomorphic.*

The various layers used in the project are now listed below along with their material properties. Values of sheet resistance, $\mathbf{R_{sh}}$ (Ohms per square), mobility, μ (cm^2/Vs), and carrier concentration, $\mathbf{n_{sh}}$ (cm^{-2}), are given for unetched material, material with the cap layer etched by wet etching and material with the cap layer etched by dry etching.

GaAs pHEMT unetched - Table 2.4

Layer	In%	Al%	spacer	R_{sh}	n_{sh}	μ
A933	30	20	2.5			
B720	30	20	2.5	391	$1.03x10^{13}$	1600
A1006	30	20	2.5			
A1143	30	20	2.5		$7.6x10^{12}$	1750
A1144	30	20	2.5			
A1158	30	20	2.5			
A1159	30	20	2.5			
A1166	30	20	2.5	386	$9.7x10^{12}$	1670
A1168	30	30	5	270	$5.4x10^{12}$	4300
A1188	30	30	5	286	$5.6x10^{12}$	3920
A1189	30	30	5	194	$10.2x10^{12}$	3130

GaAs pHEMT wet-etched / dry etched - Table 2.5

	Wet etched			**Dry etched**		
Layer	**R_{sh}**	**n_{sh}**	**μ**	**R_{sh}**	**n_{sh}**	**μ**
A933		$2.4x10^{12}$	4000		$9.6x10^{11}$	5300
B720						
A1006	235	$1.8x10^{12}$				
A1143		$2x10^{12}$	2750			
A1144		$2x10^{12}$	2850			
A1158		$3.17x10^{12}$	2555			
A1159		$2.81x10^{12}$	2648			
A1166	1040	$1.9x10^{12}$	3180			
A1168	430	$2.6x10^{12}$	5720			
A1188	470	$2.5x10^{12}$	5330	860	$1.43x10^{12}$	5120
A1189				870	$1.27x10^{12}$	5650

GaAs MESFET Wet etched - Table 2.6

Layer	R_{sh}	n_{sh}	μ
A966	585	$3.1x10^{12}$	3500
A999	392	$4x10^{11}$	3254
A1049	525	$3.64x10^{12}$	3266
A1050	512	$3.58x10^{12}$	3414

2.8 Passive Circuit Elements

2.8.1 Introduction

The passive circuit elements used in the project were metal-insulator-metal (MIM) capacitors, interdigitated capacitors, Coplanar Waveguide -Slotline baluns and Coplanar Waveguide filters. Some work had already been done on characterising Coplanar MIM capacitors in the Ultrafast Systems Group at the University of Glasgow [2.17]. Coplanar Waveguide - Slotline baluns have been characterised only up to 35GHz as reported in the literature [2.18]. Also, there are no reports of Slotline being used at 94GHz in monolithic circuits. This offers some justification for designing, fabricating and testing these circuit elements individually in order to understand fully their use in the eventual mmWIC.

2.8.2 Transmission Lines

2.8.2.1 Coplanar Waveguide

A cross section of Coplanar Waveguide is shown overleaf in Figure 34. It consists of a centre strip with two ground planes located parallel to and in the plane of the strip. The dimensions shown in the diagram are designed to achieve a CPW impedance of 50Ω. The choice of a 50 micron ground-ground spacing for CPW was based upon information in [2.21]. Structural dimensions are critical - depending on substrate thickness and ground plane width, higher order modes can propagate. To prevent this (S+2W) should be less than $\lambda/2$, while ground plane extent should be greater than 5(S+2W). Reducing substrate thickness, increases the cutoff frequency of the first higher order mode above the highest frequency of interest. However, reducing the substrate thickness also increases the coupling to the quasi-TEM microstrip-like mode - a compromise is essential.

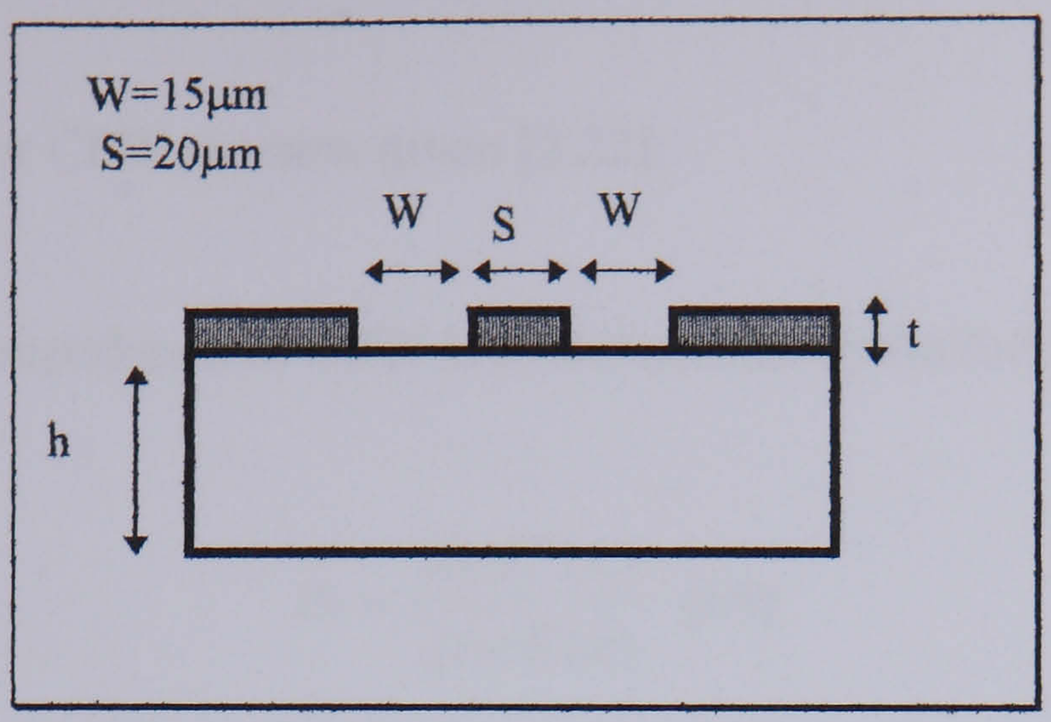


Figure 34 Cross section of Coplanar Waveguide

There are two modes of propagation in Coplanar Waveguide that are important to understand for use in the proposed mixer design. These two modes are known as balanced and unbalanced modes and are shown in Figures 35 and 36.

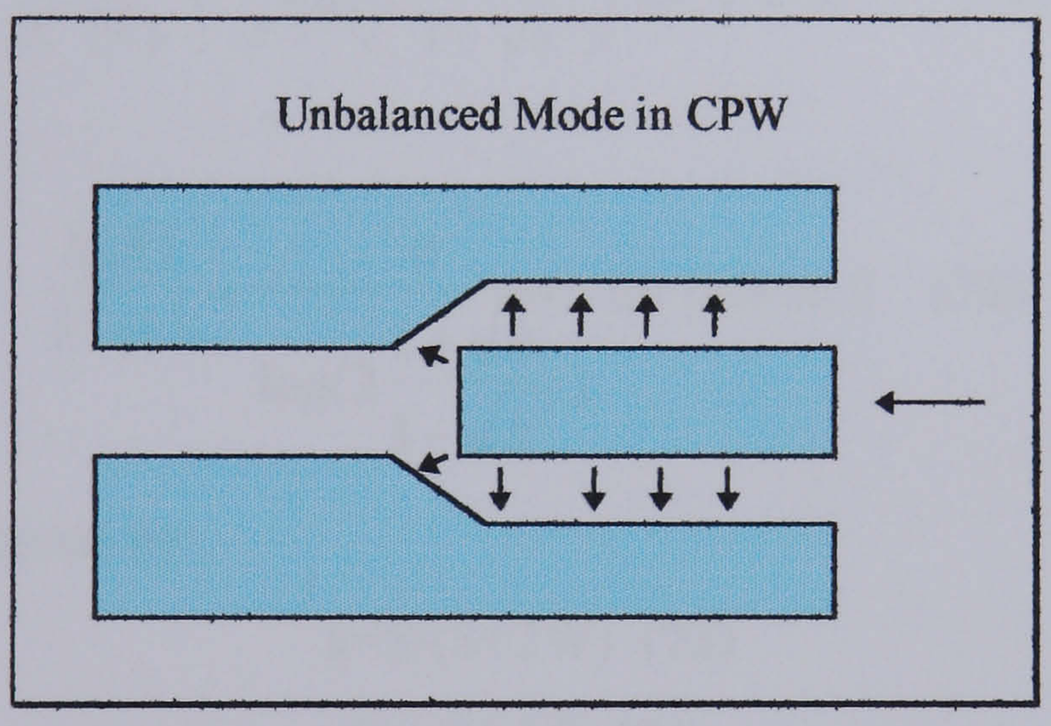


Figure 35 CPW - Unbalanced mode

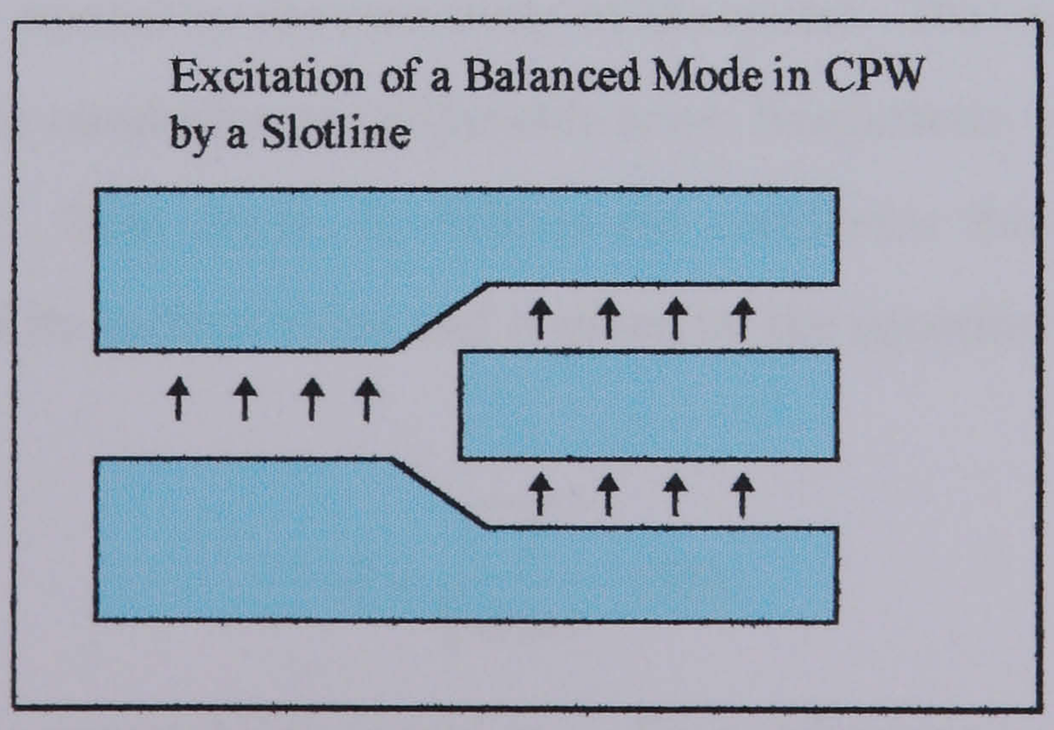


Figure 36 CPW - Balanced mode

Design equations for CPW are now given [2.22]:

The characteristic impedance of CPW is calculated using the following expression:

$$Z_0 = \frac{30\pi K'(k)}{\sqrt{\varepsilon_{eff}}\,K(k)} \quad \textbf{(69)}$$

where ε_{eff} is given by

$$\varepsilon_{eff} = (\varepsilon_r + 1)/2 \quad \textbf{(70)}$$

ε_r is the substrate permittivity

K(k)/K′(k) can be estimated using the formula:

$$\frac{K(k)}{K'(k)} = \frac{1}{\pi}\log\left(2\frac{1+\sqrt{k'}}{1-\sqrt{k'}}\right) \text{ for } 0.7<k<1 \quad \textbf{(71)}$$

$$\frac{K(k)}{K'(k)} = \frac{\pi}{\log(2\frac{1+\sqrt{k'}}{1-\sqrt{k'}})} \text{ for } 0<k<0.7 \quad \textbf{(72)}$$

where k and k′ are given by:

$$k=S/(S+2W) \quad \textbf{(73)}$$

$$k'=\sqrt{(1-k^2)} \quad \textbf{(74)}$$

The metal thickness, t, is chosen to be more than 3 times the skin depth to minimise losses in conductor caused by the resistivity of the metal. The signal is concentrated at the surface of the conductor at millimeter-wave frequencies and falls with depth into the conductor. Skin depth, δ, defines the conductor thickness at which the signal falls to 1/e of its surface value and is given by the equation:

$$\delta = \sqrt{\frac{2}{\omega\mu\sigma}} \quad \textbf{(75)}$$

where μ is magnetic permeability (equal to μ_o for nonferromagnetic materials) , ω is the frequency and σ is conductivity.

2.8.2.2 Slotline

A cross section of Slotline is shown below in Figure 37. It consists of two strips, both in the same plane, of metal separated by a narrow slot. In a slotline, the wave propagates along the slot with the major electric field component being in the direction across the slot in the plane of metallisation on the dielectric substrate. The mode of propagation is non-TEM (almost transverse electric). Note, however, that there is no low frequency cut-off because slotline is a two conductor structure. Equations for slotline impedance from the literature are as follows [2.19,2.20] (note that these are exactly as given in the literature):

1) For $0.02 < W/h < 0.2$

$$\lambda_s/\lambda_0 = 0.923-0.448\log\varepsilon_r+0.2W/h - (0.29W/h+0.047)\log(h/\lambda_0 x10^2) \quad \textbf{(76)}$$

$$Z_{os}=72.62-35.19\log\varepsilon_r+50\frac{(W/h-0.2)(W/h-0.1)}{W/h} + \log(W/hx10^2)[44.28-19.58\log\varepsilon_r]$$

$$- [0.32\log\varepsilon_r-0.11+W/h(1.07\log\varepsilon_r+1.44)] \,.\, (11.4-6.07\log\varepsilon_r-h/\lambda_0 x10^2)^2 \quad \textbf{(77)}$$

Also

$$(h/\lambda_0)_c=0.25/\sqrt{\varepsilon_r-1} \quad \textbf{(78)}$$

2) For $0.2<W/h<1$

$$\lambda_s/\lambda_0 = 0.987-0.483\log\varepsilon_r+W/h(0.111-0.0022\varepsilon_r) - (0.121+0.094W/h-0.0032\varepsilon_r) \,.$$

$$\log(h/\lambda_0 x10^2) \quad \textbf{(79)}$$

$$Z_{os}=113.91-53.55\log\varepsilon_r+1.25W/h(114.59-51.88\log\varepsilon_r)+20(W/h-0.2)(1-W/h)-[0.15$$

$$+0.23\log\varepsilon_r+W/h(-0.79+2.07\log\varepsilon_r)].[10.25-5\log\varepsilon_r+W/h(2.1-1.42\log\varepsilon_r-h/\lambda_o x10^2]^2 \quad \textbf{(80)}$$

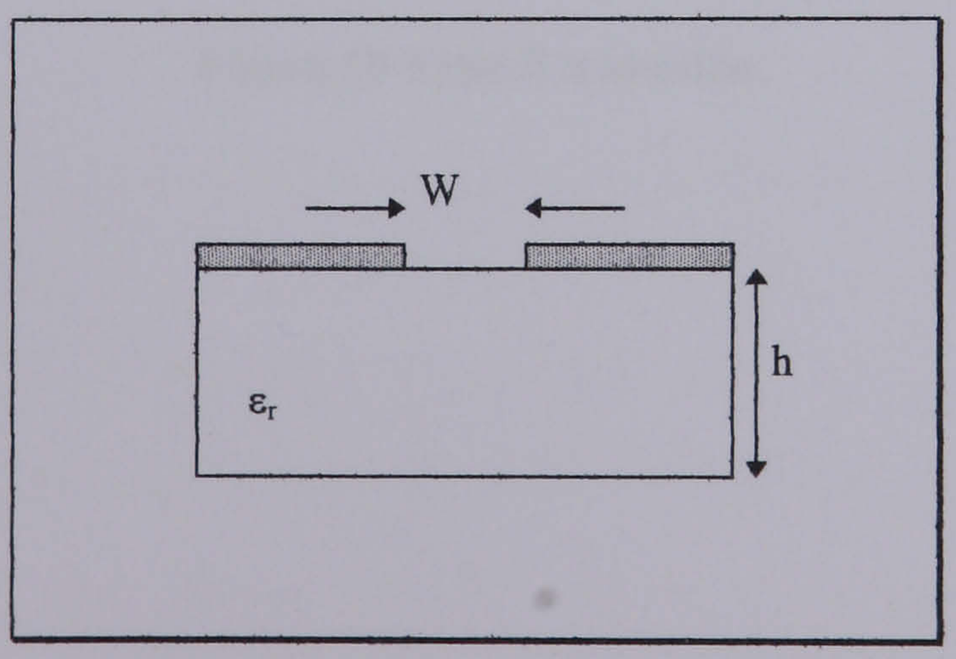


Figure 37 Cross Section of Slotline

2.8.3 Coplanar Waveguide-Slotline Transitions

As explained earlier in section 2.8.2.2, Slotline can be used to excite a balanced mode of propagation in CPW. However, as will be seen later in Chapter 4, the microwave test probes are in CPW format so it is necessary to use a CPW-Slotline transition to drive the slotline. Transitions of this type have been described in the literature [2.23],[2.24] and [2.25]. These are shown in Figures 38,39 and 40.

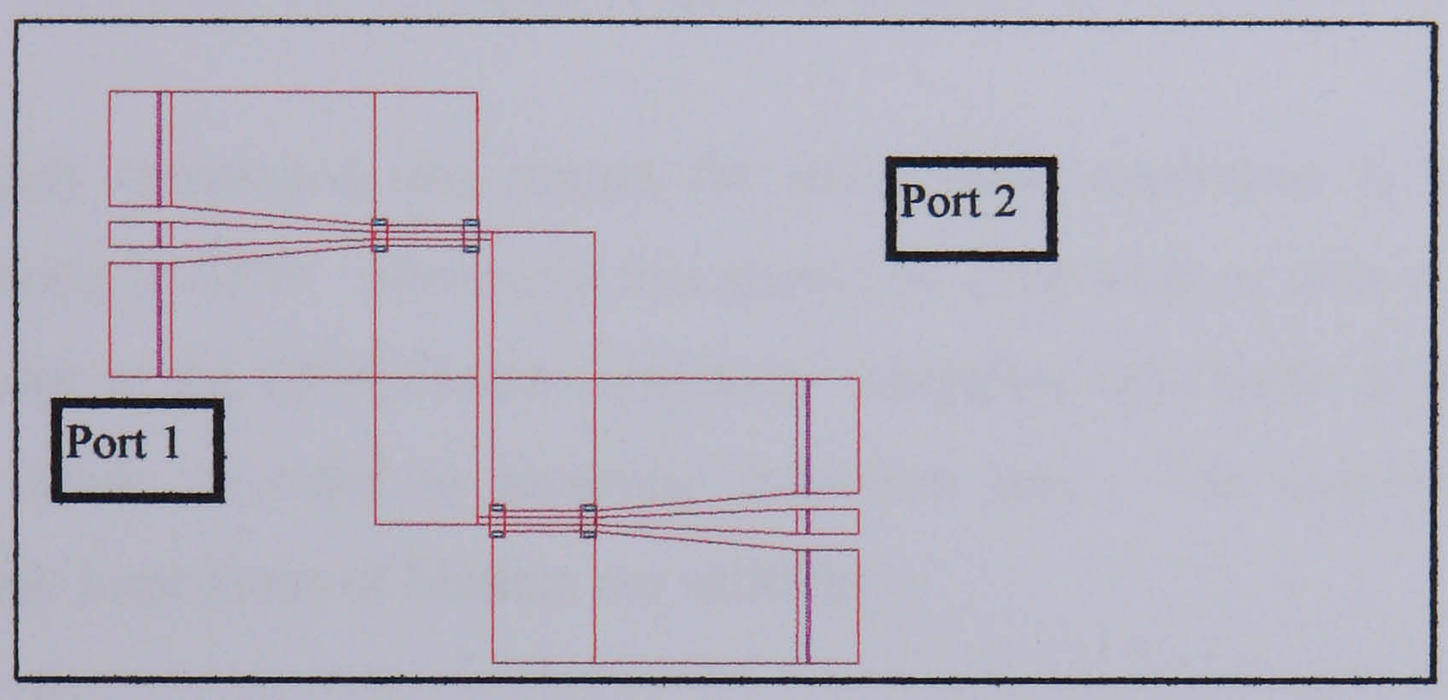


Figure 38 Type A transition

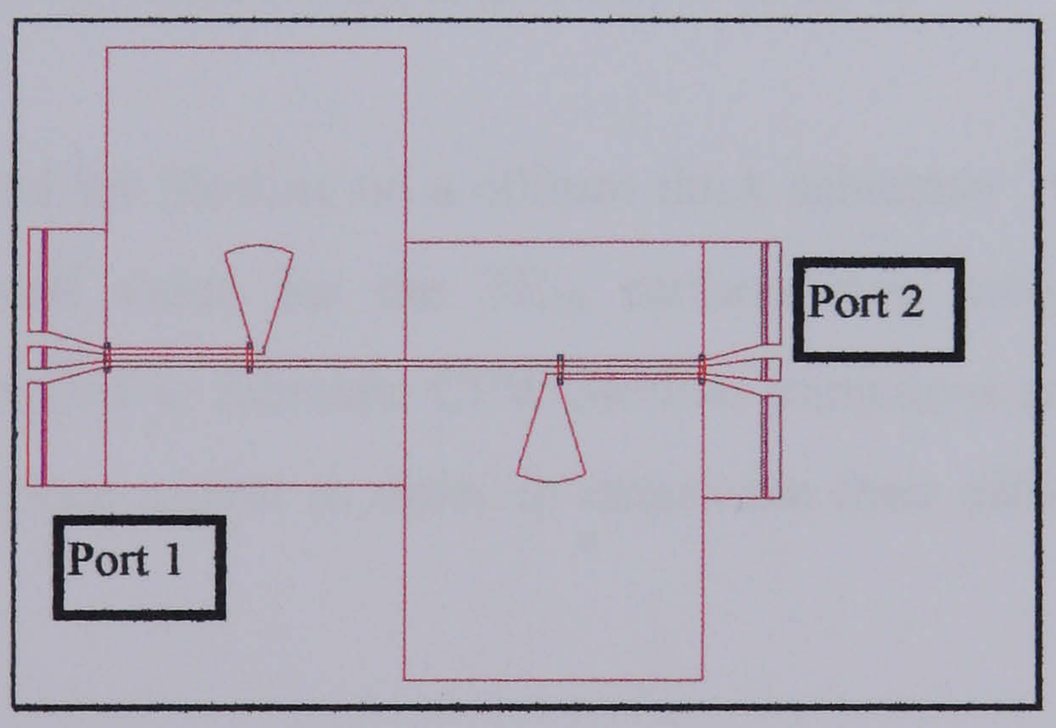


Figure 39 Type B transition

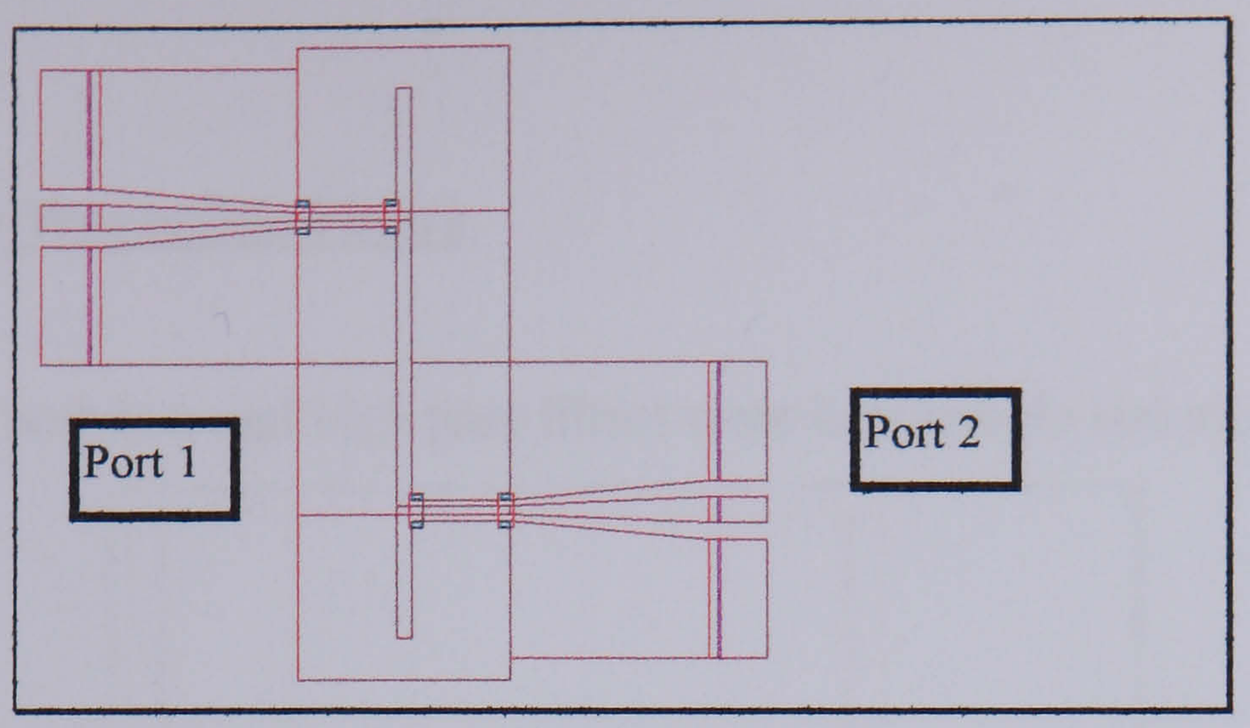


Figure 40 Type C transition

As previously mentioned, the reason for using these transitions is to excite a balanced mode in CPW. Obviously this should be done with as little of the signal being lost due to the CPW-Slotline transition Therefore the choice of Slotline gap should be made in order to minimise transition loss. The equations for the characteristic impedance of Slotline are valid for:

$9.7<\varepsilon_r<20$ - a)

$0.02<W/h<1$ - b)

$0.01<(h/\lambda_o)<(h/\lambda_o)_c$ - c) where $(h/\lambda_o)_c$ is given by $0.25/(\varepsilon_r-1)^{1/2}$

It is c) that is invalid for Slotline on a 400μm thick substrate. The quantity $(h/\lambda_o)_c$ represents the cut-off value for the TE_{10} surface-wave mode on the Slotline. Therefore it was decided to fabricate CPW-Slotline transitions and vary the Slotline width and ground plane extent in order to determine their effect on the transition loss.

The length of the slotline stub in each of the transitions of type B and C, was $\lambda/4$ at the centre frequency of the transition. The transitions were made in a back-to-back format as it was not possible to isolate and measure a single transition (ie the measurement probes are in CPW format). This measurement gives a good indication of the expected insertion loss and match into the transition at the centre frequency. However, it does not give an entirely accurate assessment of the bandwidth of a single transition, as the interaction between the two stubs changes as the separation between them differs.

2.8.4 Coplanar Waveguide Filters

The designs of both low and high pass filters were kept simple and are shown below:

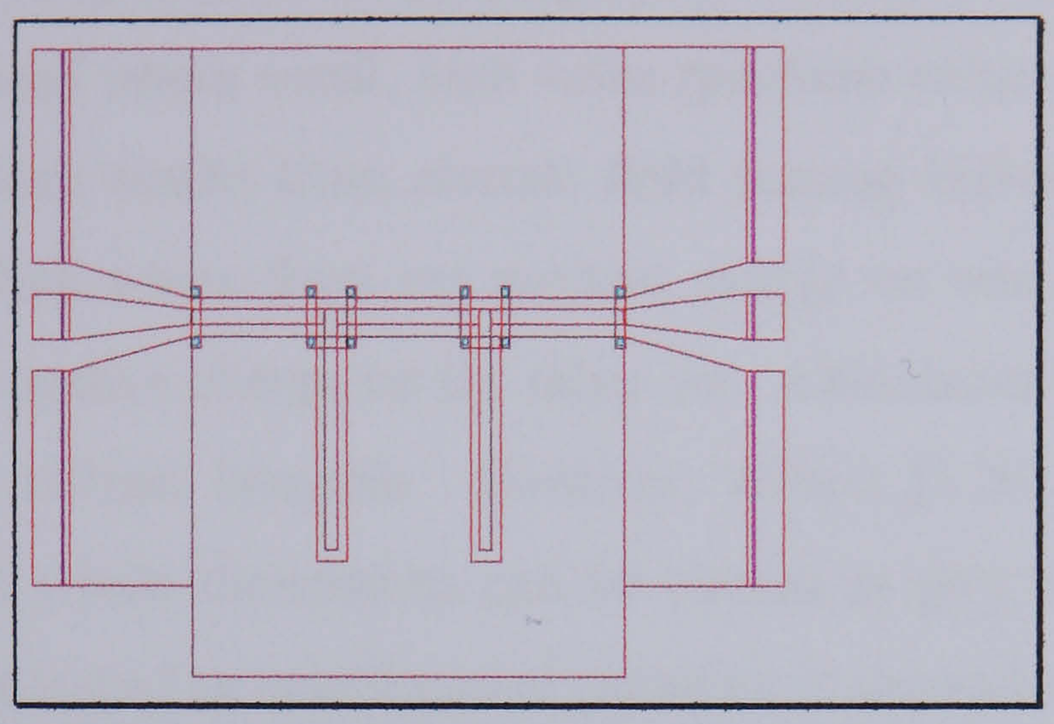


Figure 41 Low pass filter

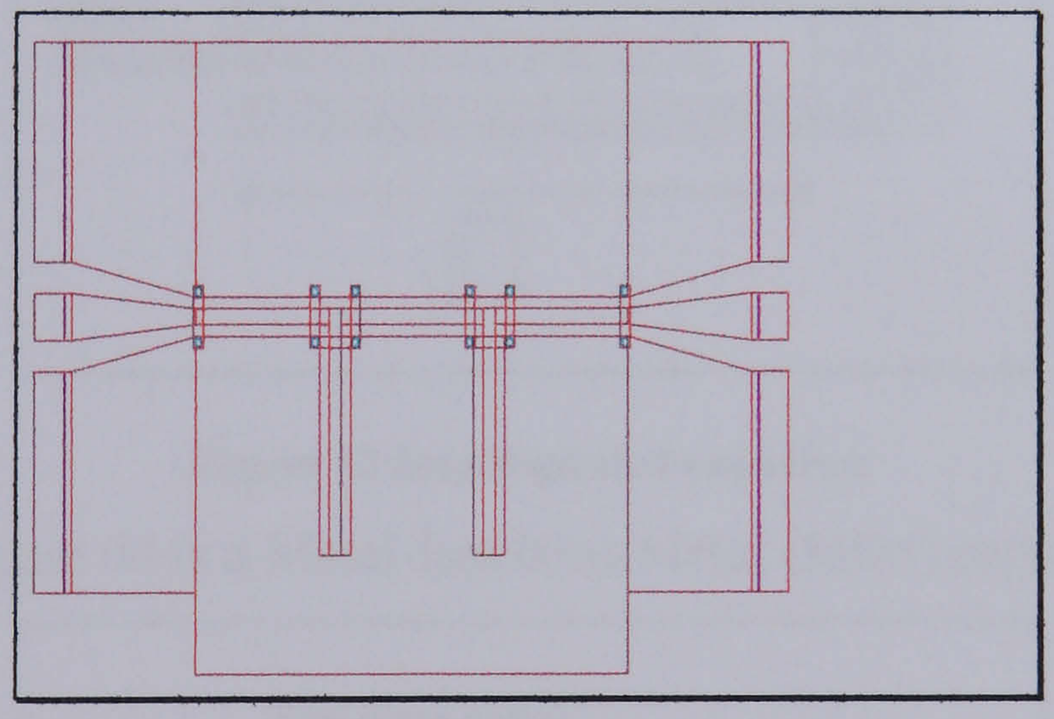


Figure 42 High Pass Filter

The CPW stubs shown above were designed to be $\lambda/4$ at the centre frequency (94GHz) of the transition. The high pass filter is simply a transpose of the low pass filter. The inclusion of the airbridges around the "T" junctions and the separation of the stubs in the filters (200μm) were based on information in [2.29].

2.8.5 Capacitors

Both Metal-insulator-metal and interdigitated capacitors were used. Interdigitated capacitors have the advantage of simplifying the fabrication process (see Chapter 3) and are generally used where small, high value precision values of capacitance are required. Capacitance results from electric field passing between the two sets of fingers. Electric field arises from net positive charge on one set of fingers, and terminates on net negative charge on the other set. Calculation of the capacitance can be done using elliptic integrals. However, Wilson [2.26], provides a set of design curves from which dimensions can be chosen to give a required value of capacitance. The layout of an interdigitated capacitor is shown below.

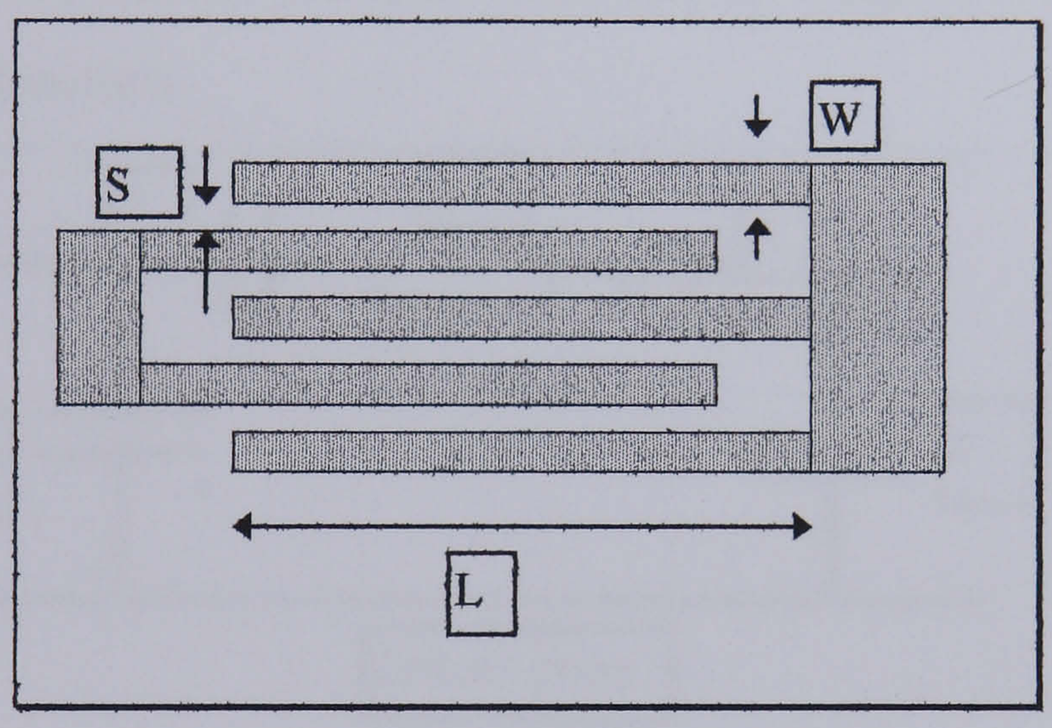


Figure 43 Interdigitated capacitor

Shown below in Figure 44 is a Metal-Insulator-Metal (MIM) capacitor.

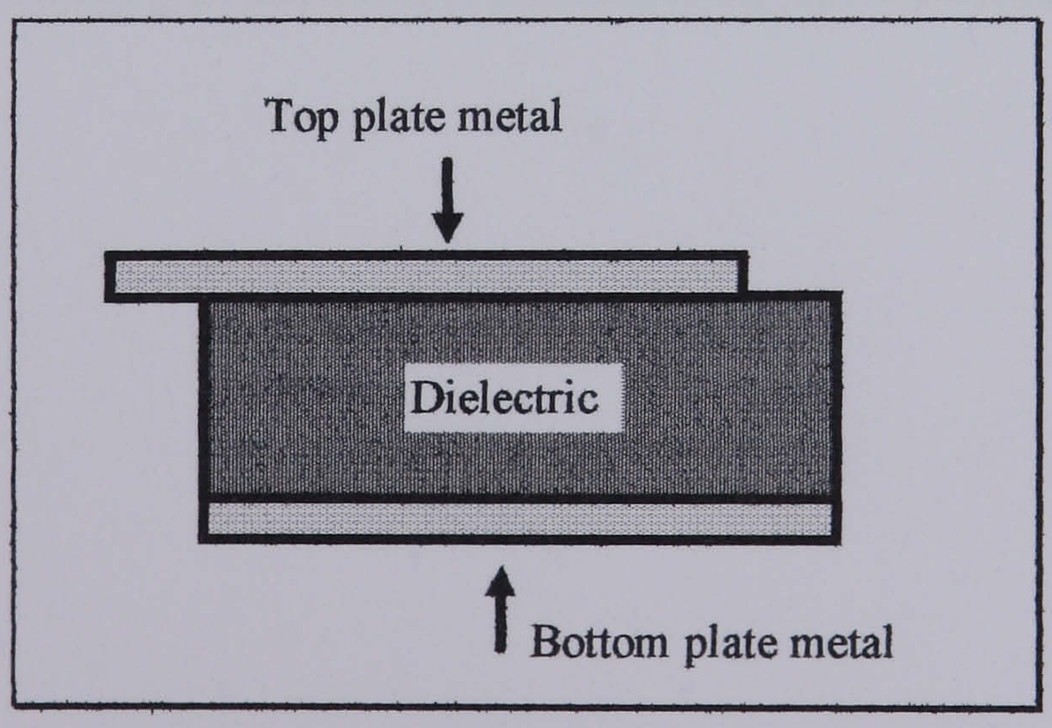


Figure 44 MIM capacitor

The capacitance of a MIM capacitor can be approximated as follows:

$$C(pF) \approx \varepsilon_0 \varepsilon_r A/d \quad \textbf{(81)}$$

where ε_0 is the free space permittivity, ε_r is the relative dielectric constant, **A** is the capacitor top plate and **d** is the dielectric thickness. This classical expression is an approximation and omits capacitance due to fringing fields.

Shown below in Figure 45 is the equivalent circuit for both interdigitated and MIM capacitors. In the case of interdigitated capacitors the inductance, L arises from the magnetic field created by the passage of current through the capacitor. The resistance, R, relates to series loss in the fingers. Capacitors C_1 and C_2 represent the capacitance of the finger array to ground.

In the case of MIM capacitors, the series resistance R results from both the top and bottom plates. The parasitic inductance is due to magnetic field forming loops around the whole structure.

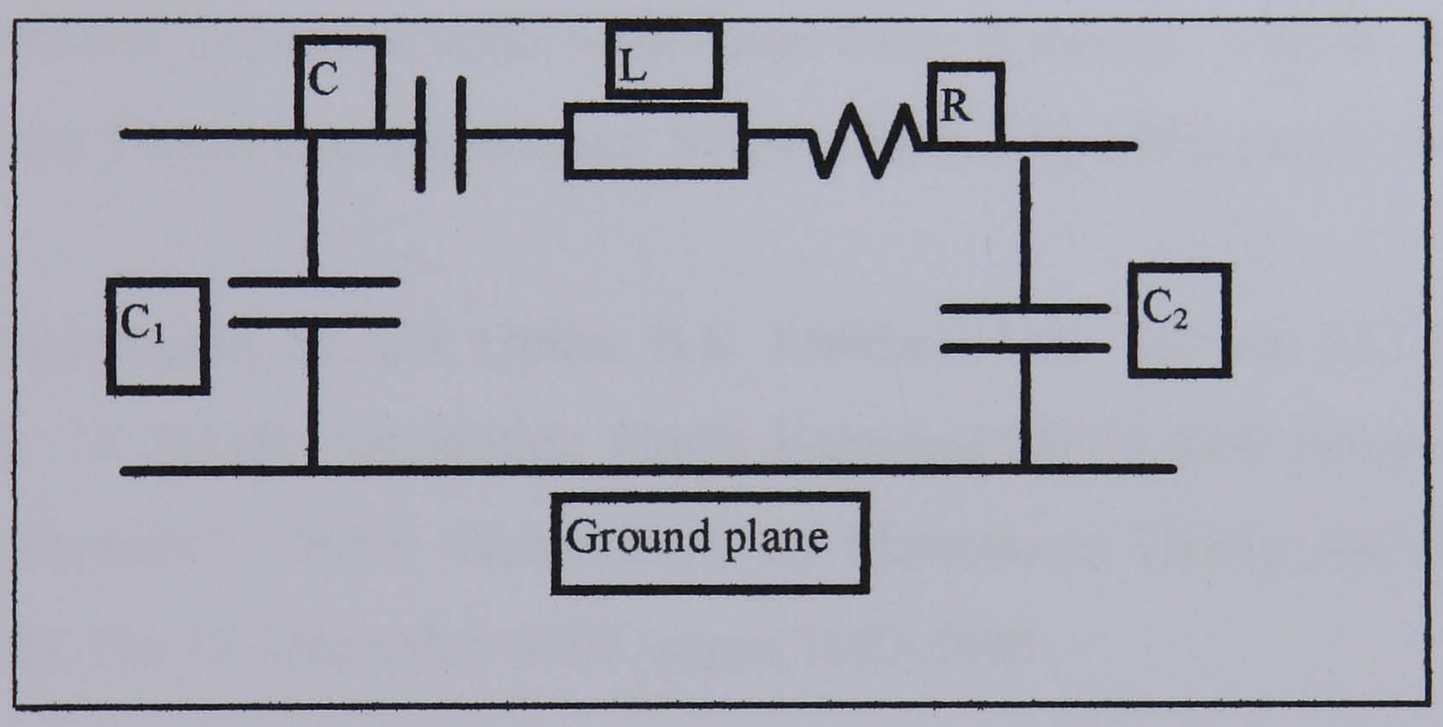


Figure 45 Equivalent circuit of interdigitated and MIM capacitors

Chapter 2 References

[2.1] S.A.Maas :"Microwave Mixers" (Artech House, Norwood, MA, 1993), Chapter 2.

[2.2] B. Schuppert: "Analysis and Design of Microwave Balanced Mixers" - IEEE Transactions on Microwave Theory and Techniques, Vol.MTT-34, No.1, January 1986, pages 120-128.

[2.3] D. Blackwell, H.G. Henry, J.E. Degenford, M. Cohn : "94GHz subharmonically pumped MMIC mixer" - 1991 IEEE MTT-S Digest, pages 1037-1039.

[2.4] G.P. Gauthier, W.Y. Ali-Ahmad, T.P. Budka, D.F. Filipovic, G.M. Rebeiz : "A Uniplanar 90GHz Schottky-Diode Millimeter-Wave Receiver" - IEEE Transactions on Microwave Theory and Techniques, Vol.43, No.7, July 1995, pages 1669-1672

[2.5] S.J. Nightingale, M.A.G. Upton, B.K. Mitchell, U.K. Mishra, S.C. Palamateer, P.M. Smith :"A 30GHz Monolithic Single Balanced Mixer with Integrated Dipole Receiving Element" - IEEE Transactions on Microwave Theory and Techniques, Vol. MTT-33, No.12, December 1995, pages 1603-1609.

[2.6] W.L. Bishop et al : "A novel Whiskerless Schottky Diode for Millimeter and Submillimeter Wave applications" - IEEE MTT-S International Microwave Symposium Digest, 1987, p607.

[2.7] S.A.Maas :"Microwave Mixers" (Artech House, Norwood, MA, 1993), Chapter 4.

[2.8] S.A.Maas :"Microwave Mixers" (Artech House, Norwood, MA1993), Chapter 5.

[2.9] S.A.Maas :"Microwave Mixers" (Artech House, Norwood, MA, 1993), Chapter 6.

[2.10] "A 30GHz Monolithic Single Balanced Mixer with Integrated Dipole Receiving Element" - IEEE Transactions on Microwave Theory and Techniques, Vol. MTT-33, No.12, December 1985, pages 1603-1609.

[2.11] T. Chen, T. Ton, G.S. Dow, K. Nakano, L.C.T. Liu, J. Berenz : "A Q-Band Monolithic Balanced Resistive HEMT mixer Using CPW/Slotline Balun" -IEEE Journal of Solid State Circuits, Vol.26, No.10, October 1991, pages 1389-1394.

[2.12] S. Murad, M. Rahman, N. Johnson, S. Thoms, S.P. Beaumont, C.D.W. Wilkinson : "Dry etching damage in III-V semiconductors", Journal Vac.Sci.Technol, Nov/Dec 1996, pages 3658-3662.

[2.13] P.H.Ladbrooke, "MMIC Design:GaAs FETs and HEMTs" (Artech House, Norwood, MA, 1989) ,

[2.14] K.Elgaid, "A monolithic Ka-Band Downconverter",PhD thesis, University of Glasgow, 1998.

[2.15] N.I. Cameron, M.R.S. Taylor, H. McLelland, M. Holland, I.G. Thayne, K. Elgaid, S.P. Beaumont : "A High Performance, High Yield, Dry-etched, Pseudomorphic, HEMT for W-Band use", IEEE MTT-S Digest, 1995.

[2.16] J. Singh, "Semiconductor Devices" (McGraw-Hill, New York, 1994), Chapter 8

[2.17] D. Edgar, K. Elgaid, F. Williamson, S. Ferguson, I.G. Thayne, M.R.S Taylor, S.P. Beaumont : "W-Band On Wafer measurement of Active and Passive Devices". IEE Colloquium on Microwave Measurements, IEE London, Feb. 1999.

[2.18] K. Elgaid, D. Edgar, S. Broadfoot, S. Ferguson, M. Taylor, S. Beaumont :"Compact low loss coplanar waveguide to slotline transition for mmWIC applications" - Electronics Letters, 29th August 1996, Vol.32, No.18, pages 1677-1678

[2.19] S.B. Cohn : "Slotline on a dielectric substrate" - IEEE Transactions on Microwave Theory and Techniques, Vol. MTT-17, No.10, October 1969, pages 768-778

[2.20] R. Garg, K.C. Gupta : "Expression for Wavelength and Impedance of Slotline" - IEEE Transactions on Microwave Theory and Techniques, August 1976, page 532

[2.21] W.H. Haydl, A. Tessmann, K. Zuefle, H. Massler, T. Krems, L. Verweyen, J. Schneider, " Models of coplanar Lines and Elements over the Frequency Range 0-120GHz" : European Microwave Conference Digest, pp 996-1000, 1996.

[2.22] K.C. Gupta, R. Garg, I.J. Bahl :"Microstrip Lines and Slotlines" (Artech House, Norwood, MA, 1979), Chapters 5-7.

[2.23] "Uniplanar MIC Balanced Multiplier - a proposed new structure for MICs"- IEEE Transactions on Microwave Theory and Techniques, Vol. MTT-35, No.12, December 1987, pages 1363-1368

[2.24] E. Vourch, M. Drissi, J. Citerne, V.F. Hanna : "A Full-wave analysis of Coplanar Waveguide-Slotline Transition", IEEE MTT-S Digest, 1994, pages 1309-1312.

[2.25] T.Q. Ho, S.M. Hart :"A Broad-band Coplanar Waveguide to Slotline Transition" - IEEE Microwave and Guided Wave Letters, Vol.2, No.10, October 1992, pages 415-416

[2.26] K. Wilson : "Other circuit elements for MMICs", GEC Journal of Research, 126-133, 1986

[2.27] D.M Pozar: "Microwave Engineering" (John Wiley & Sons, New York, 1998), Chapters 10 & 12.

[2.28] J.H. Davies, J.A. Nixon, "Fluctuations in submicrometer semiconducting devices caused by the random position of dopants", Phys. Rev. **39**(5), 3423-3426, 1989.

[2.29] R. Shimon, D. Scherrer, D. Caruth, J. Middleton, H. Hsia, M. Feng, " Accurate Passive Component Models in Coplanar Waveguide for 50GHz MMICs", IEEE MTT-S Digest, 1997, pages 769-772.

[2.30] L.Mancia, G.B. Stracca : "Effects of the Diode junction capacitance on the conversion loss of Microwave mixers", IEEE Trans. Commun., vol. COM-22, pp 1428-1435, Sept, 1974.

Chapter Three

Fabrication

3.1 Introduction

This chapter describes the processes used to fabricate monolithic millimetre-wave integrated circuits. It is split into two distinct sections. The first section (3.2) describes the basic processes common to the original FET process such as electron beam lithography, photolithography and metallisation techniques. The second section (3.3) describes the entire fabrication process and emphasises the considerable developments made to the existing FET process to enable a high-yield mmWIC fabrication process to be realised. Fabrication details for individual devices such as diodes, filters and capacitors are also included.

3.2 Basic Fabrication Techniques

3.2.1Electron Beam Lithography & Photolithography

3.2.1.1 Introduction

Lithography is the process of transferring patterns to a thin layer of radiation-sensitive material (resist) covering the surface of a semiconductor wafer. These resist patterns define the regions of the integrated circuit such as contacts or interconnects and are not permanent features of the final device. Figure 46 below illustrates the basic steps in any lithography process. The two forms of lithography used in this work were Electron Beam Lithography(EBL) and Photolithography.

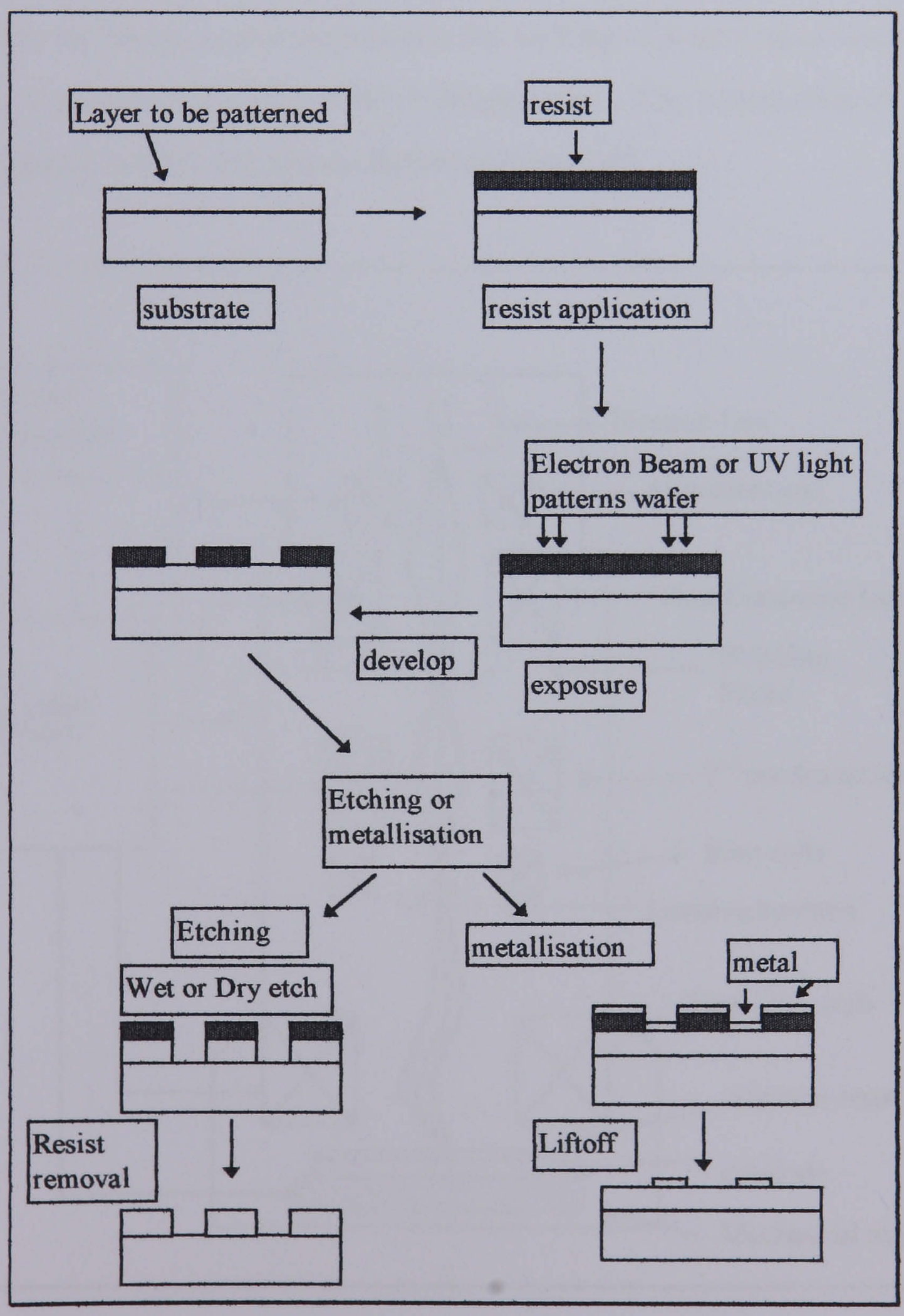


Figure 46 Basic Lithography steps

3.2.1 2 Electron Beam Lithography

Electron Beam Lithography (EBL) was the chosen technique used for mmWIC fabrication primarily because its high resolution was needed for the anode level of the diode. It was used in all other processing steps, except for airbridge formation (see Section 3.3.7), in order to ensure excellent registration from one layer to the next. The major advantage of EBL over photolithography (apart from the obvious ability to define smaller feature size) is that pattern definition is controlled by computer and so it is a relatively easy task to convert data from a CAD package to drive the electron beamwriter. This system is flexible and means minor modifications in design do not necessitate the writing of a new mask each time. The EBL system used was the Leica EBPG5 Beamwriter. The schematics of an electron beam lithography system are shown below in Figure 47.

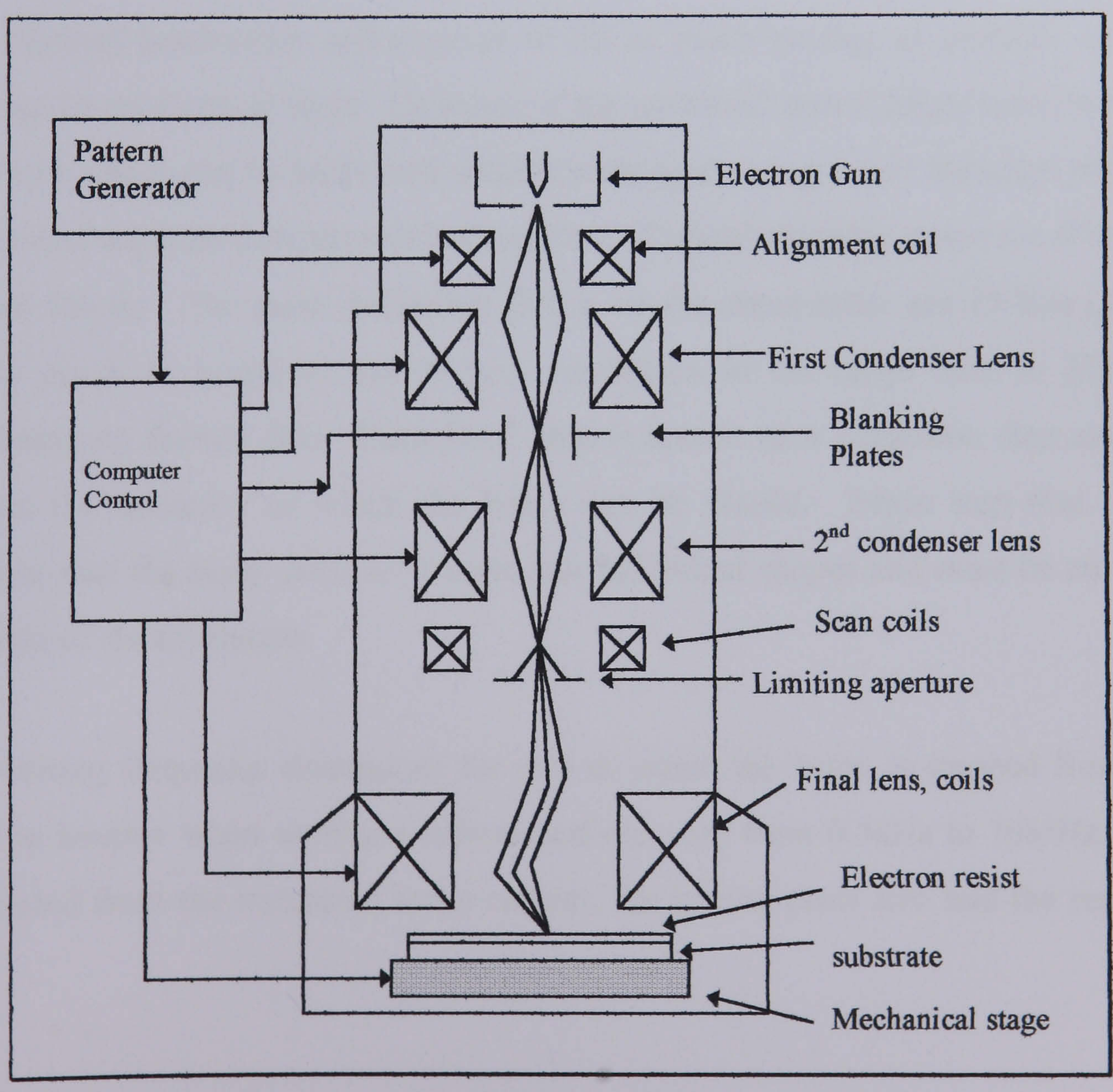


Figure 47 Simplified diagram of an electron beam lithography system

A basic description of how this system works is given below including features specific to the LEICA EBPG5:

In order to obtain the desired pattern on the wafer surface after development, the appropriate area on the substrate must be exposed to the electron beam. The EBPG5 uses the vector scan principle with a gaussian beam, ie a beam with a gaussian cross-sectional variation in current density. This approach gives the smallest beam size and hence the smallest features. The **spot size** is the size of the focussed electron beam. The term vector scan refers to the fact that the beam is scanned only across the areas of interest so that between individual shapes which need to be exposed the beam is blanked. To enable the developer to remove the unwanted resist, the solubility of the resist must be changed by a sufficient amount during e-beam exposure. This requires a certain number of electrons known as the **dose**.

The electron beamwriter will attempt to do as much writing as possible without moving the mechanical stage. However, if the patterned area is larger than the block size (area which can be addressed without moving the stage) then the stage must be moved and adjacent patterns stitched together. Typical stitching errors are 40nm for 800μm blocks. The main deflection DACs on the beamwriter are 15 bits (32000 usable pixels in **x** and **y**) and so give **resolution** in the range 5nm to 312.5nm depending on feature size. Each DAC step is known as a resolution step and this defines the accuracy to which the beam can be placed. Beam step size is the distance that the beam steps as it scans out individual shapes and must be an exact multiple of the resolution.

The writing frequency determines the rate at which the beam is stepped from one pixel to another when writing a pattern and can vary from 0.5kHz to 10MHz. It is calculated from the measured beam current, the known pixel size and the required dose.

3.2.1.3 Electron Beam resists

The following electron beam resists were used in the fabrication process:

1) Poly-Methyl Methacrylate (PMMA)

2) A co-polymer of Methyl Methacrylate and Methacrylic acid (P(MMA/MAA))

PMMA is a polymer which consists of a long chain of molecules. The electron beam breaks these chains and thus lowers the molecular weight (Figure 48) of the PMMA. The developer then removes the areas of resist which are of lower molecular weight in a selective process. P(MMA/MAA) has a greater sensitivity than PMMA. The developer used was a mixture of 4-methyl pentan-2-one (MIBK) and Propanol (IPA). The ratio of these two compounds determines the selectivity/contrast of the process.

These are both positive electron beam resists so that the exposed areas are removed by the developer solution (as opposed to negative resists where the unexposed area is removed by the developer). The lithographic process begins by coating the substrate with a layer of PMMA (dissolved in a solvent - either Chlorobenzene or Xylene) dispensed using a pipette and then spun on sample at high speed (4000-6000rpm). The sample is then baked at 180^0C in order to evaporate the solvent leaving a PMMA coating. After e-beam exposure and development, there should be a "window" in the resist which can be used either for etching or deposition. Generally, for all metallisation steps, a bi-layer resist system was used to aid the lift-off process (see section 3.2.2).

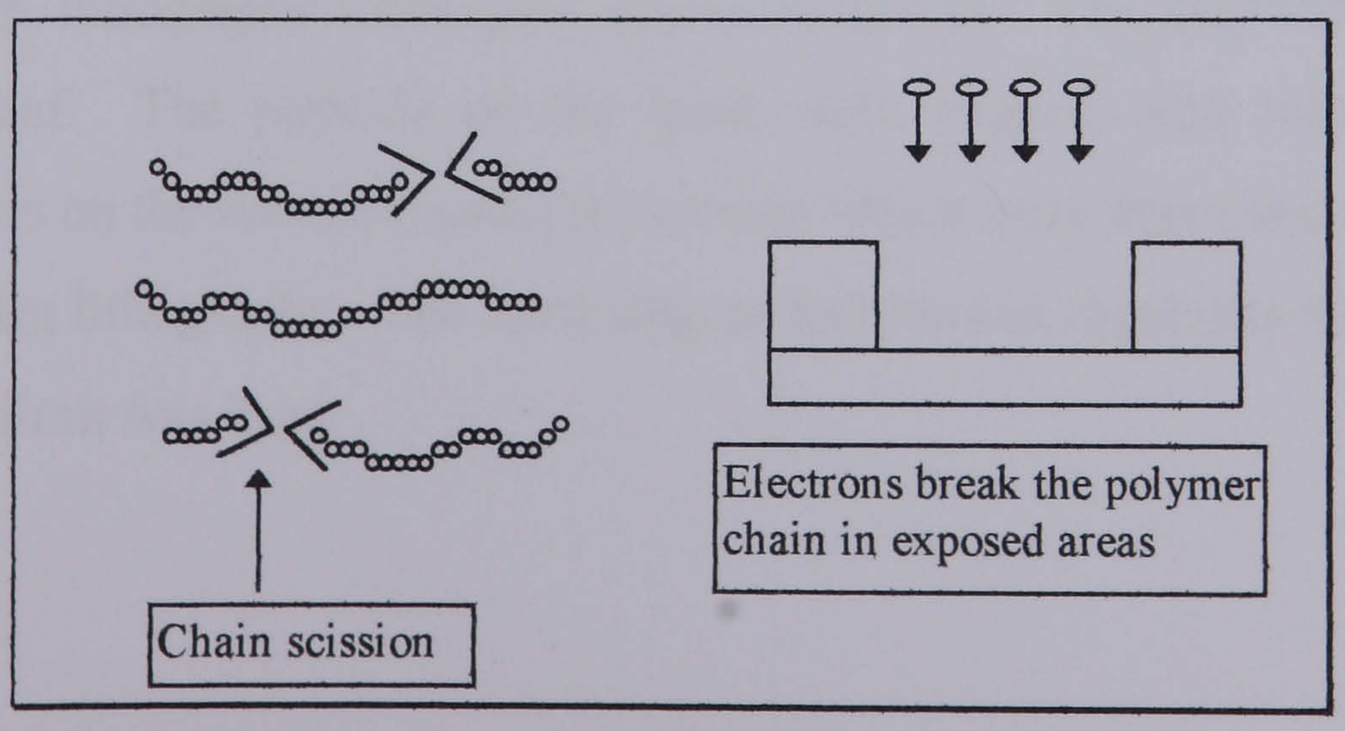


Figure 48 Positive Resist [3.1]

3.2.1.4 Photolithography

Photolithography uses Ultraviolet (UV) light instead of electrons to pattern the resist. In this case the resist must be radiation-sensitive - photoresist. Shipley photoresist was used in this project which is a positive resist. It consists of three components: a photosensitive compound, a base resin, and an organic solvent. Before exposure, the photosensitive compound is insoluble in the developer solution. After exposure, the photosensitive compound absorbs radiation in the exposed areas, changes its chemical structure and becomes soluble in the developer solution.

A simple diagram of how the mask aligner, used for photolithography, worked is shown below.

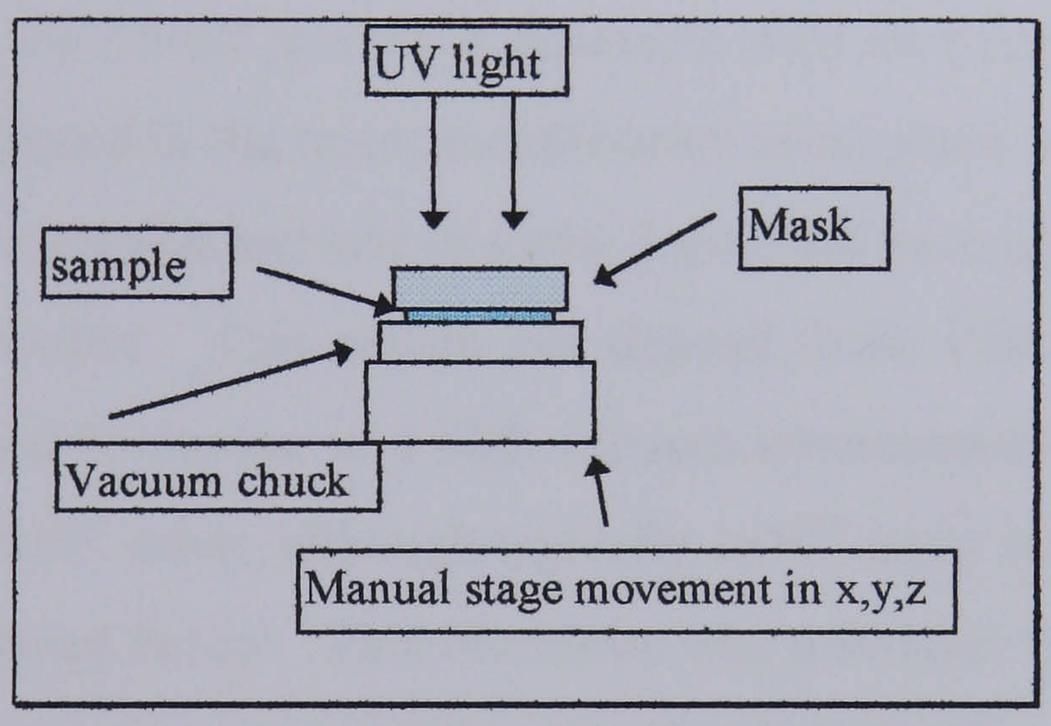


Figure 49 Mask aligner for photolithography

The stage was manually aligned with the mask before the substrate was brought into hard contact with the mask. The masks were designed and patterned using the electron beam lithography techniques described earlier. The alignment scheme is shown overleaf. The patterns on the mask were aligned with reference to the previous layers on the substrate using the crosses which were deposited at the marker level of e-beam lithography. The mask aligner had limited capability for alignment - the practical limit was 2μm.

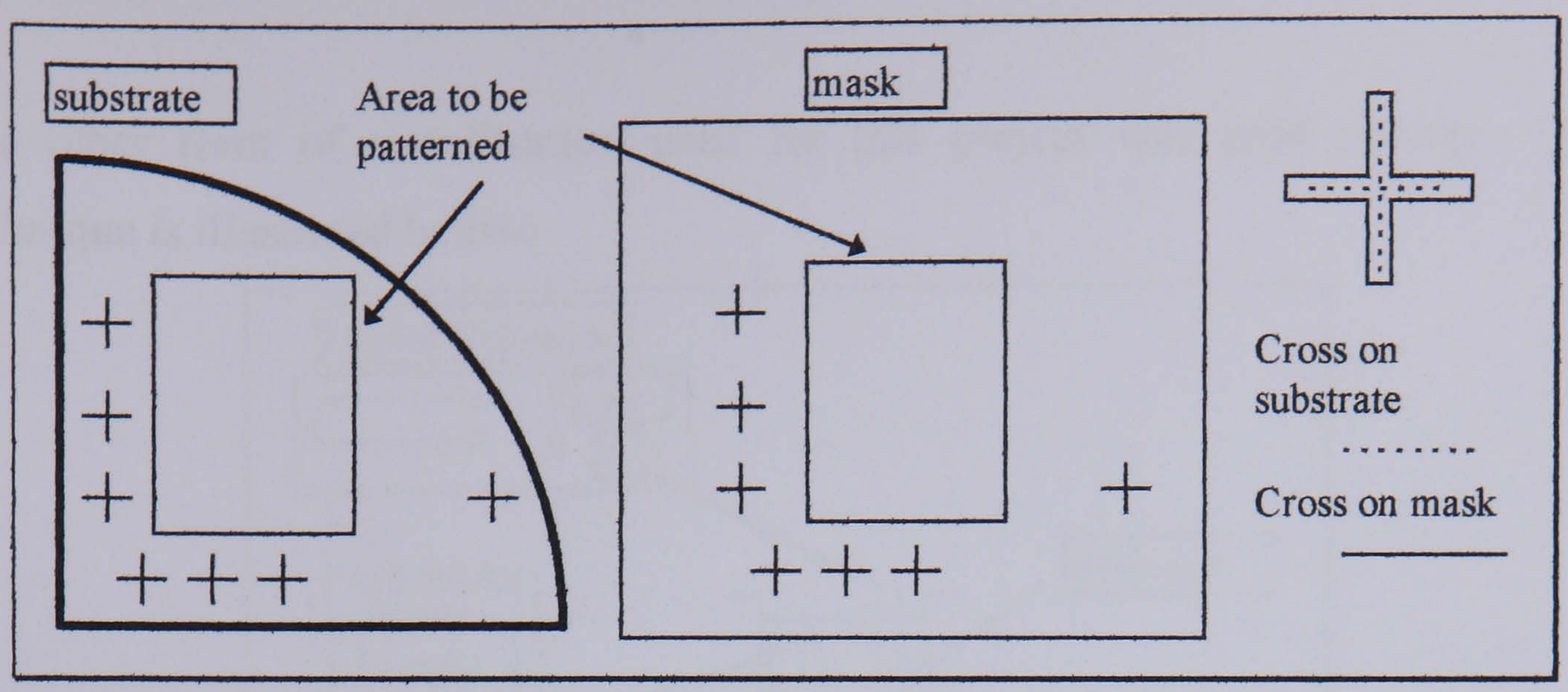


Figure 50 Airbridge Alignment

3.2.2 Metallisation

A feature of PMMA is that is can be easily removed from a substrate using acetone. This aids greatly in the lift-off process, a technique used for pattern transfer. Once a window has been opened in the resist, metallisation takes place using a Plassys MEB 450 Evaporator. The amount and rate of metal deposition were controlled by a quartz crystal thickness monitor. This system can deposit Gold, Palladium, Germanium, Nickel, Titanium and Nichrome in a high vacuum environment which can achieve pressures such as $2x10^{-7}$ mbar, although typically $1x10^{-6}$ mbar is adequate. The lift-off process is illustrated below. This illustrates why a bi-layer resist profile is used for metallisation steps - to ensure a undercut profile for lift-off.

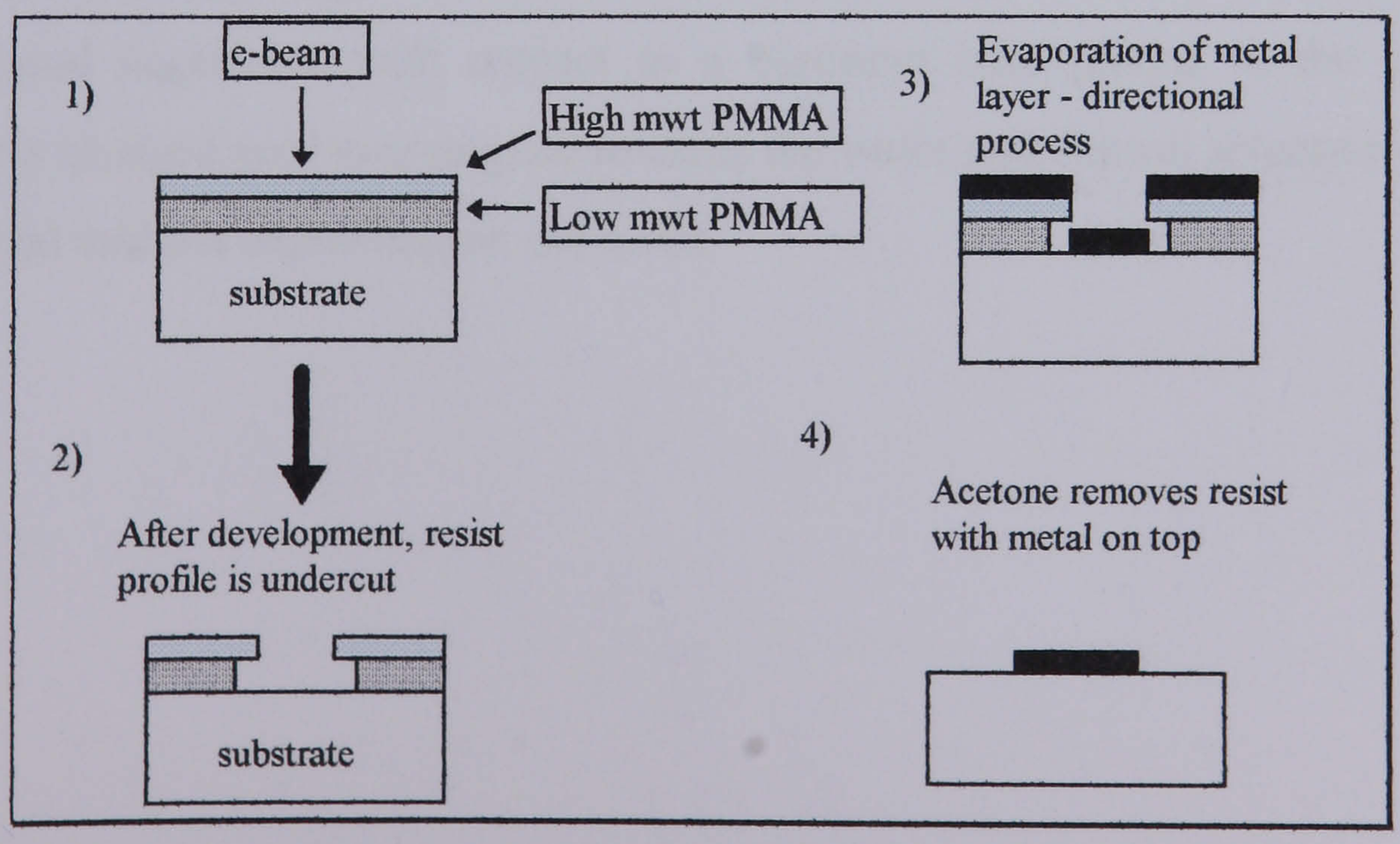


Figure 51 Lift-off process

The other form of metallisation used for this project was gold plating. This technique is illustrated below:

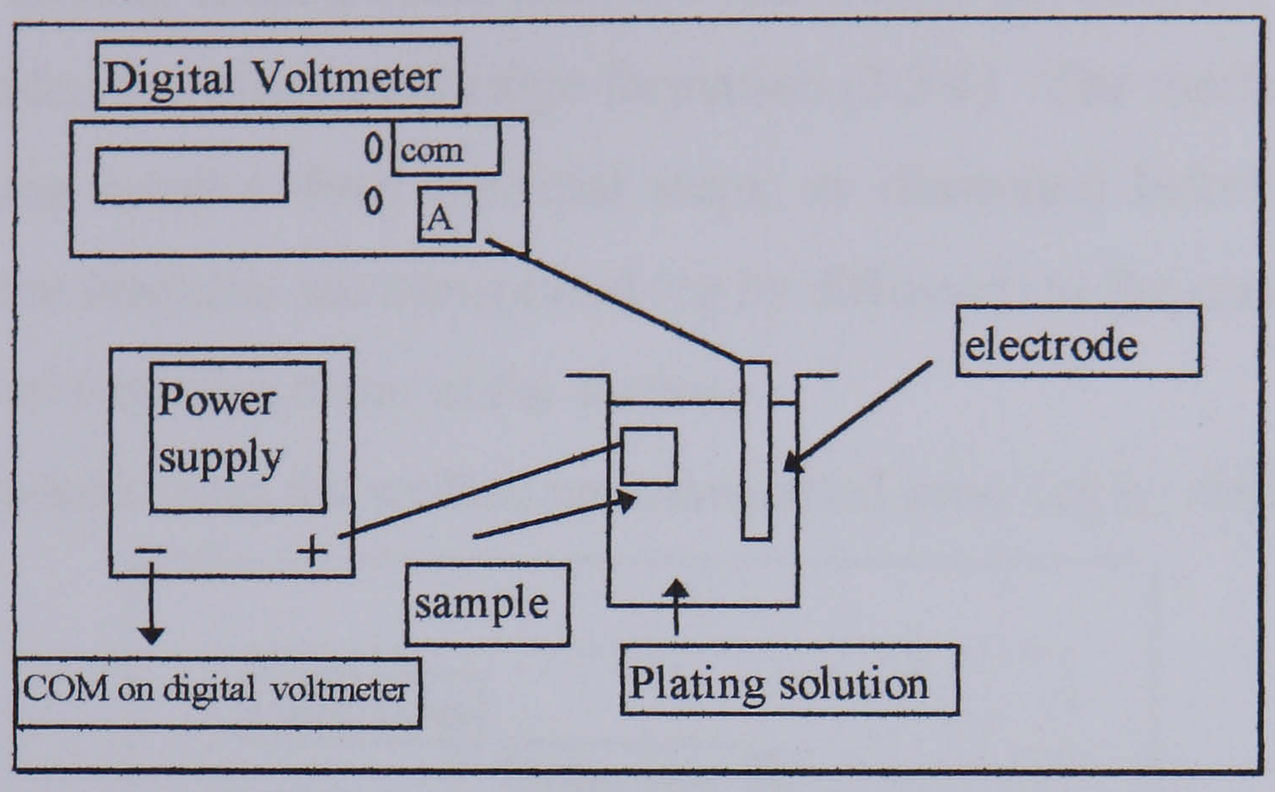


Figure 52 Au plating set-up

The sample to be plated is attached to a copper plate using wax. A mixer agitates the solution during plating. The plating current required is calculated using the formula:

(Area of copper plate - Area of sample) x (Current Density)

Plating for 20 minutes @ 50C with 100rpm spin speed will give a plating thickness of 2 microns for a current density of 0.013mA/mm.

The basic Au plating process is as follows: Firstly, a thin layer of seed metal is deposited over the wafer. A layer of photoresist is then patterned above the seed layer uncovering metal where the plating is required. The wafer is placed in an electrolytic solution of gold and has electrical contact made to the seed layer. It is then biased negatively with respect to a platinum wire placed in the solution. Positively charged gold ions migrate towards the wafer and deposit selectively on the seed metal without depositing on the resist.

3.2.3 Wet and Dry etching

Wet chemical etching is used in the mmWIC fabrication process, for both electrical isolation of diodes and also in airbridge formation (3.3.8). The mechanisms for wet chemical etching involve three essential steps, as illustrated below in Figure 53. These are : 1) the reactants are transported (eg by diffusion) to the reacting surface

2) chemical reactions occur at the surface

3) the products from the surface are transported away (eg by diffusion).

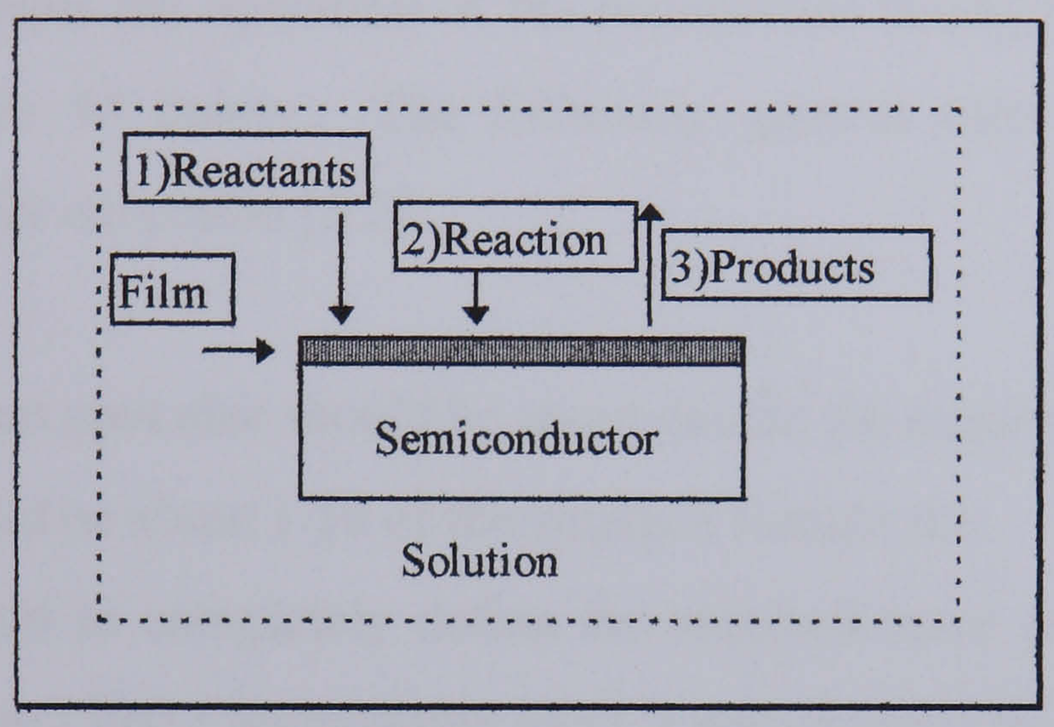


Figure 53 Wet chemical etching

Dry etching usually involves a plasma discharge struck in a chamber containing low pressure reactant gases. The wafer is then etched by chemical means, or by bombardment of the wafer, or by a combination of the two. The technique used in this project for anode recess etching was Selective Reactive Ion Etching. This technique uses the kinetic energy of ions or radicals formed to offer some directionality to the etch process. Pressure is normally low (0.01-0.1Torr). The substrate rests on the cathode which is DC isolated. With an RF plasma, electron bombardment builds up a negative bias on this electrode which in turn leads to a substantial ion bombardment. The relatively long mean free path at these low pressures ensures near normal incidence for ion bombardment and so gives good anisotropy.

3.2.4 E-Beam Exposure Method

Firstly, pattern designs were formed on a PC using a standard design package called Wavemaker (WAM). Subsequently, these patterns were then fractionated into a suitable form for use by the beamwriter using CATS software. A job file was formed using BWL which tells the beamwriter what spot size, resolution, exposure dose, beam energy, etc to use. This file is then transferred to the host computer RVF which directly controls the operation of the beamwriter during processing. This is illustrated in Figure 54 below. The following general rules were followed in preparing the jobs for execution [3.2]:

1) The electron beam **spot size** should be about double the required resolution.
2) **Resolution** should be about 1/10 of the smallest feature size.
3) The **dose** required to completely define the required resist pattern after a fixed development time (30s) / temperature (23^0C) was decided by an initial exposure test for each process step.
4) Beam energy was fixed at 50kV.

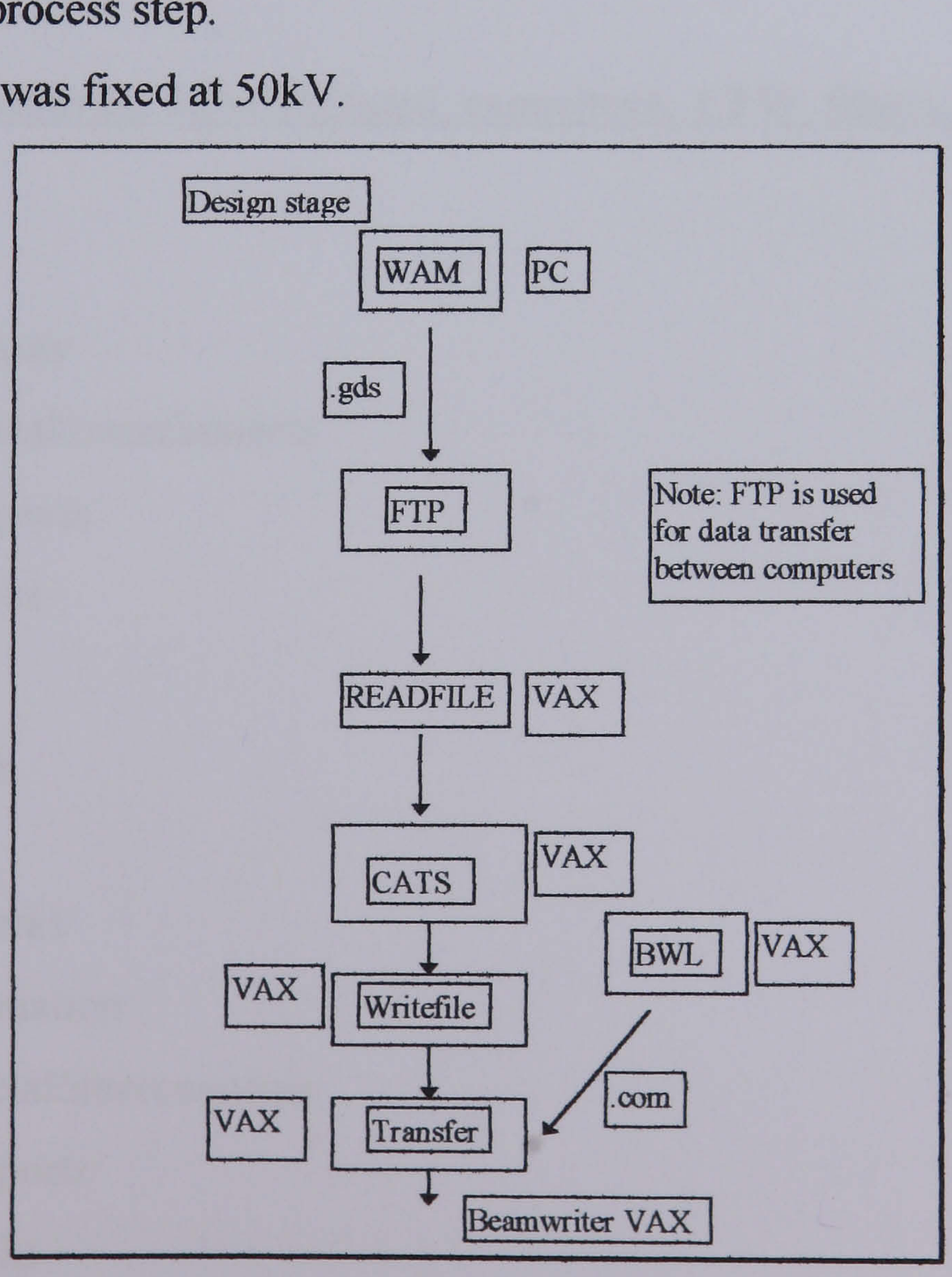


Figure 54 Data flow for use of beamwriter

3.3 mmWIC Fabrication process

3.3.1 Overview

The mixers consisted of five levels of electron beam lithography and two levels of photolithography for circuits using interdigitated capacitors and six layers of EBL and two levels of photolithography for circuits using MIM capacitors. The following steps were necessary:

MIM circuits

1) Alignment marks
2) Ohmic contacts
3) Mesa Isolation
4) Dielectric Deposition
5) Anode contacts
6) Final layer metal/interconnects
7) Airbridge supports
8) Airbridge tracks

Interdigitated circuits, Individual diodes

1) Alignment marks
2) Ohmic contacts
3) Mesa Isolation
4) Anode contacts
5) Final layer metal/interconnects
6) Airbridge Supports
7) Airbridge Tracks

Calibration standards, Interdigitated capacitors, CPW filters, CPW -Slotline transitions

1) Alignment marks
2) Final layer metal/interconnects
3) Airbridge supports
4) Airbridge tracks

MIM capacitors

1) Alignment marks
2) Dielectric formation
3) Final layer metal/interconnects
4) Airbridge supports
5) Airbridge tracks

3.3.2 Alignment Marks

3.3.2.1 Introduction

The alignment marks used are shown below in Figure 55. This a standard process for alignment markers within the FET group at the University of Glasgow. These were used to allow the alignment of the isolation, ohmic, dielectric, anode and bondpad levels. The requirements for this level were that the marker surface was smooth, that at least 100nm Au should be deposited and that the marker shape was clear and distinct.

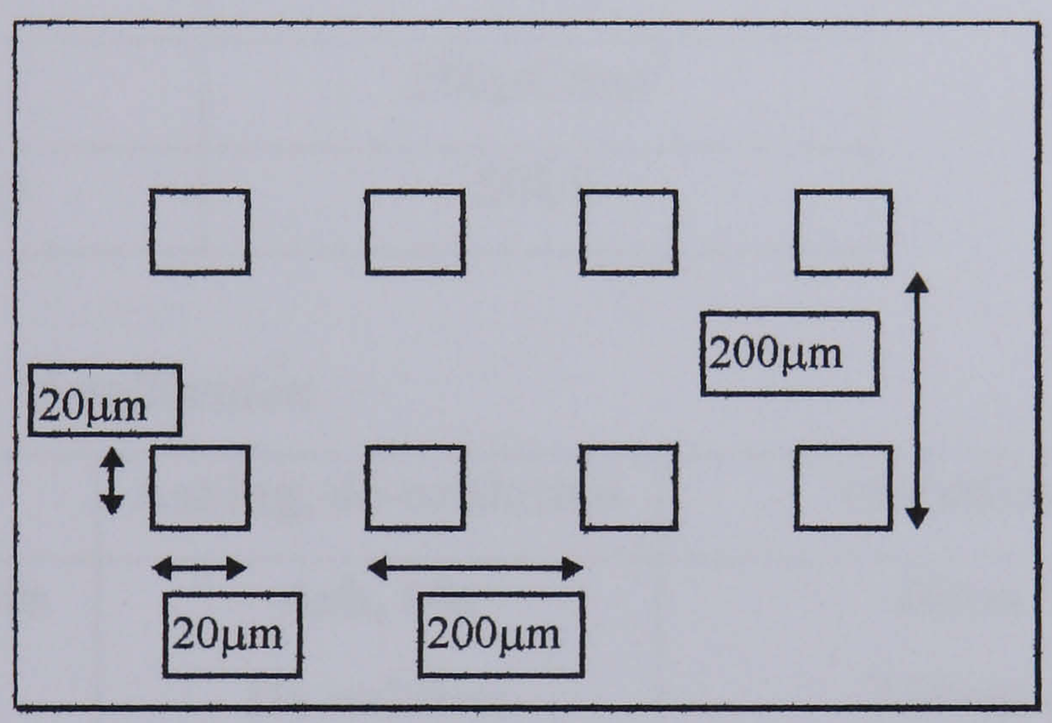


Figure 55 Alignment markers for e-beam lithography

Each marker was 20µm square and was separated (centre-to-centre) by 200 µm from the adjacent marker. The marker metallisation was initially NiCr/Au and subsequently Ti/Au as this was found to adhere better to the substrate. The resists used will now be defined using nomenclature familiar to others in the Nanoelectronics group at the University of Glasgow.

BDH - 85000 molecular weight PMMA

ELV - 350000 molecular weight PMMA

ALD - 120000 molecular weight PMMA

ALD replaced BDH around April 1996. The resist thickness was related to the percentage weight of PMMA in the casting solvent.

3.3.2.2 Process details

a) ***Resist application***

	1st Layer Resist	2nd Layer Resist
Resist Type/Thickness	**12% BDH/ALD(600nm)**	**4% ELV(100nm)**
Spin Speed/Time	**5000rpm for 60s**	**5000rpm for 60s**
Bake Time/Temperature	**1 hour@180°C**	**2 hours@180°C**

b) ***Exposure Step***

Spot size	**300nm**
Resolution	**150nm**
Dose	**250μC/cm^2**
Beam Energy	**50kV**

c) ***Development & Metallisation***

Development	Ashing, de-oxidation	Metallisation
1:1 IPA:MIBK, 30s **Rinse IPA, 30s** **Blow Dry N_2**	**Ash, 60s** **De-oxidise:** **4:1 H_2O/HCl, 30s** **Rinse IPA, 30s** **Blow Dry N_2**	**20nm Ti** **130nm Au** **Lift-off:** **Acetone(45°C), 30mins** **Rinse IPA, 30s** **Blow Dry N_2**

.

The above processing details were standard to the existing FET process and no significant process changes were necessary during this project. It should be noted, however, that there was some margin for over-development by as much as 5s. Also written at this level was the bottom plate of the capacitor for circuits which used MIM capacitors.

3.3.2.3 Alignment to subsequent levels

The alignment scheme shown below was used during all processing.

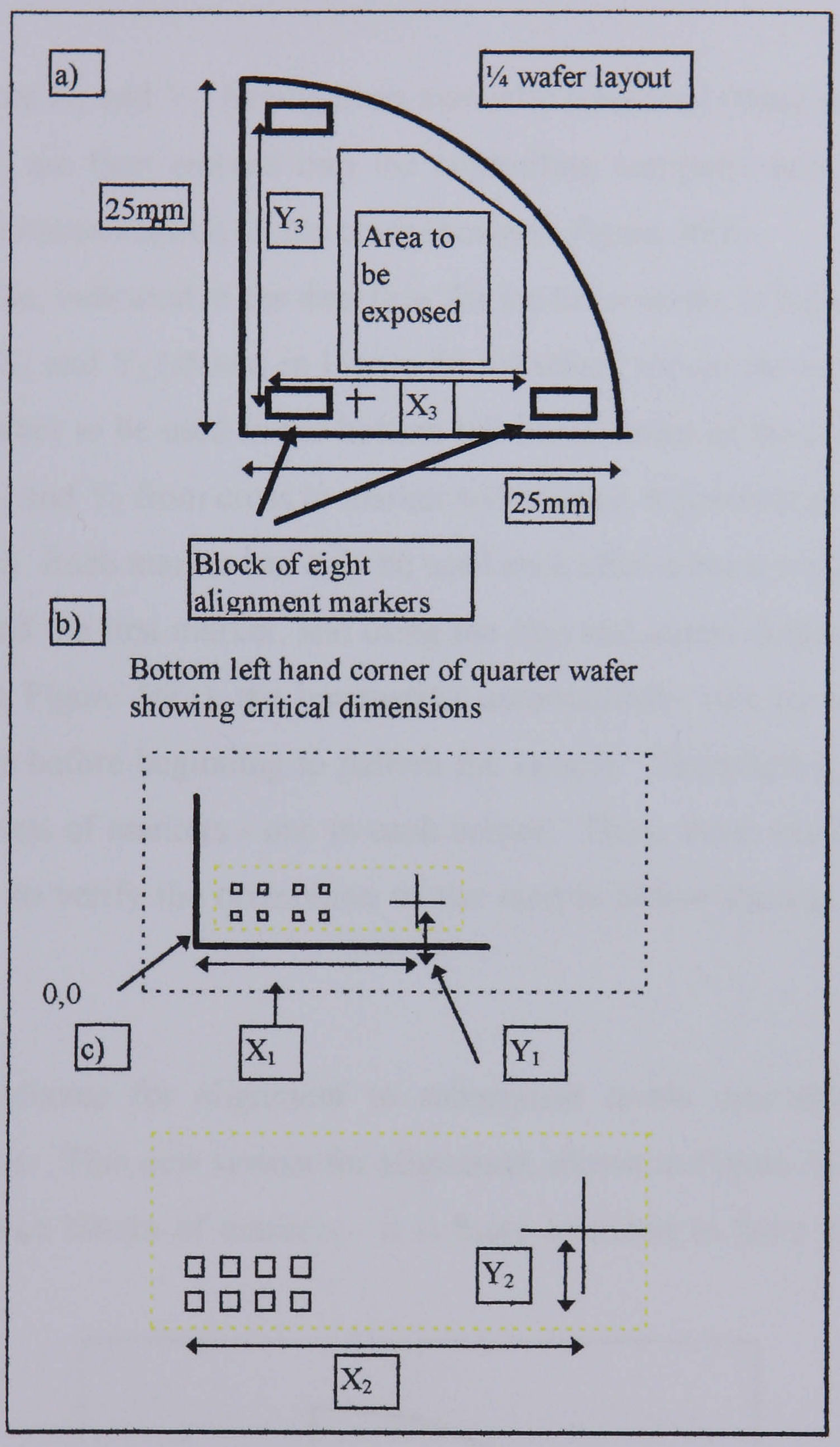


Figure 56 Alignment to subsequent levels

The basic alignment scheme using the EBPG5 for all processing is explained as follows:

As can be seen from Figure 56 a) all substrates used were ¼ of a 2 inch wafer. In each of the three corners of the ¼ wafer, is a block of eight alignment marks

identical to those shown in Figure 55. The important dimensions are shown in Figure 56 b) and c). The procedure for alignment is now described:

1) Firstly, the beamwriter operator manually finds the 0,0 position indicated in Figure 56(b). This corresponds to the bottom left hand corner of the quarter wafer.
2) The distances X_1 and Y_1, having been manually measured (mm) under an optical microscope, are then entered into the controlling computer and the beam will move to a position centred on the cross shown in Figure 56(b).
3) The BWL file, indicated in the data flow for the beamwriter in Figure 54, contains the values X_2 and Y_2 (shown in Figure 56 c)) which moves the electron beam to the first marker to be used in the bottom left hand corner of the substrate. These values of X_2 and Y_2 from cross to marker will change depending on which marker is to be used. Each marker can only be used once after e-beam exposure.
4) Having found the first marker, and using the step and repeat distance (X_3 and Y_3) indicated in Figure 56(a), the beamwriter automatically will try to find another two markers before beginning to pattern the sample. Therefore it is adequate to have three sets of markers - one in each corner. These three markers enable the beamwriter to verify the orientation of the sample before starting to pattern the wafer.

This marker scheme for alignment to subsequent levels was altered from the standard scheme. This new system for alignment, shown in Figure 56 (a), differs by having only three blocks of markers - it is more common to have many blocks as shown below:

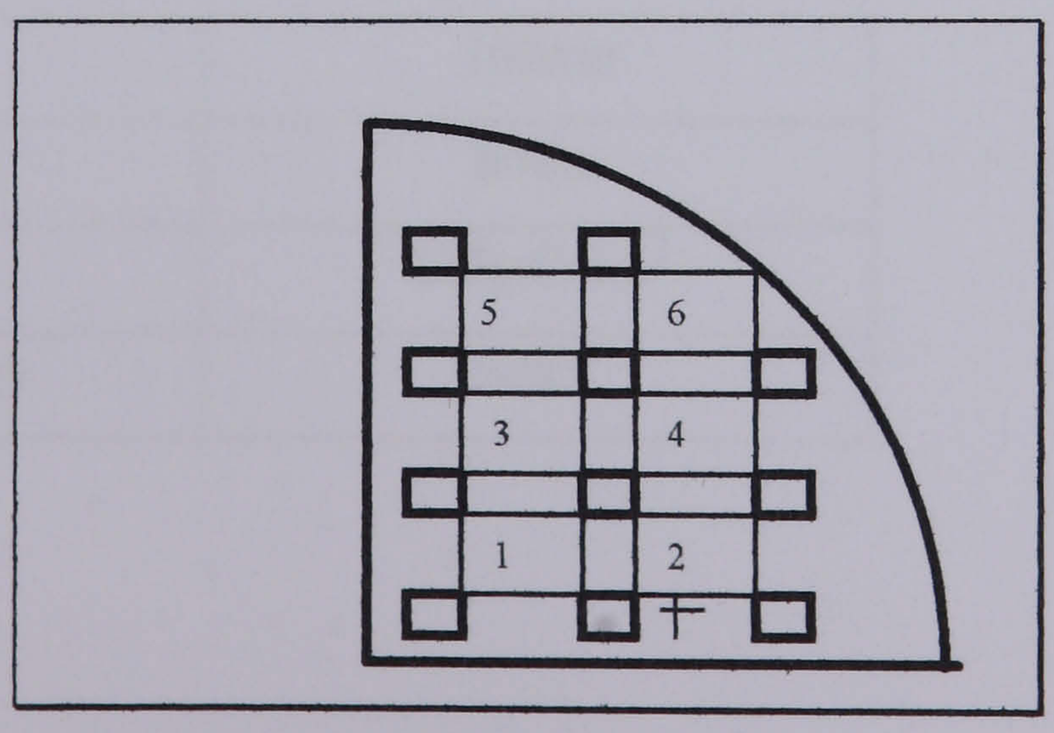


Figure 57 Marker scheme for FET process

The marker scheme shown in Figure 57 has six separate areas to be patterned and the beamwriter will find the markers for each separate blocks before patterning them. However, the writing time for the patterns used in this project was such that the marker scheme shown in Figure 56(a) is adequate and allows more area on the ¼ wafer for devices.

3.3.3 Ohmic Contacts

3.3.3.1 Introduction

This process had previously been optimised for use with GaAs MESFETs but not for GaAs pHEMTs. Therefore a considerable amount of experimentation was done on different combinations of metals and anneal times/temperatures and the results/description are presented.

3.3.3.2 Process Details

a) ***Resist application***

	1st Layer Resist	**2nd Layer Resist**
Resist Type/Thickness	**12% BDH/ALD(600nm)**	**4% ELV(100nm)**
Spin Speed/Time	**5000rpm for 60s**	**5000rpm for 60s**
Bake Time/Temperature	**1 hour@180°C**	**2 hours@180°C**

b) ***Exposure Step***

Spot size	**160nm**
Resolution	**80nm**
Dose	**225μC/cm^2**
Beam Energy	**50kV**

c) *Development & Metallisation*

Development	Ashing, de-oxidation	Metallisation
1:1 IPA:MIBK, 30s	**Ash, 60s**	**14nm Au**
Rinse IPA, 30s	**De-oxidise:**	**14nm Ge**
Blow Dry N_2	**4:1 H_2O/HCl, 30s**	**14nm Au**
	Rinse IPA, 30s	**11nm Ni**
	Blow Dry N_2	**240nm Au**
		Lift-off:
		Acetone(45^{o}C), 30mins
		Rinse IPA, 30s
		Blow Dry N_2

To reduce contact resistance the wafer was then annealed using a **Jipelec** rapid thermal annealer (RTA). The annealing recipe used was:

10s ramp in N_2, 20s @ 310C, 10s ramp in N_2, 60s @ 360C, 10s ramp in N_2.

It should be noted that during the exposure step the resolution was changed from an initial value of 150nm (from the FET process) to 80nm to ensure that the ohmic contact definition was exact.

3.3.3.3 Process optimisation

The object of these experiments was to minimise ohmic contact resistance. The metallisation given in 3.3.3.2 (previously optimised for GaAs MESFETs), was taken as the reference against which the other ohmic recipes were compared. In order to be able to optimise the process it is necessary to understand the theory behind ohmic contacts.

3.3.3.3.1 Theory of Ohmic Contacts

An ohmic contact is defined as "a source of carriers with non-negligible internal resistance R_c, but one which obeys Ohm's law for current densities of interest"-[3.4]. An energy band diagram of an ohmic contact is shown below in Figure 58.

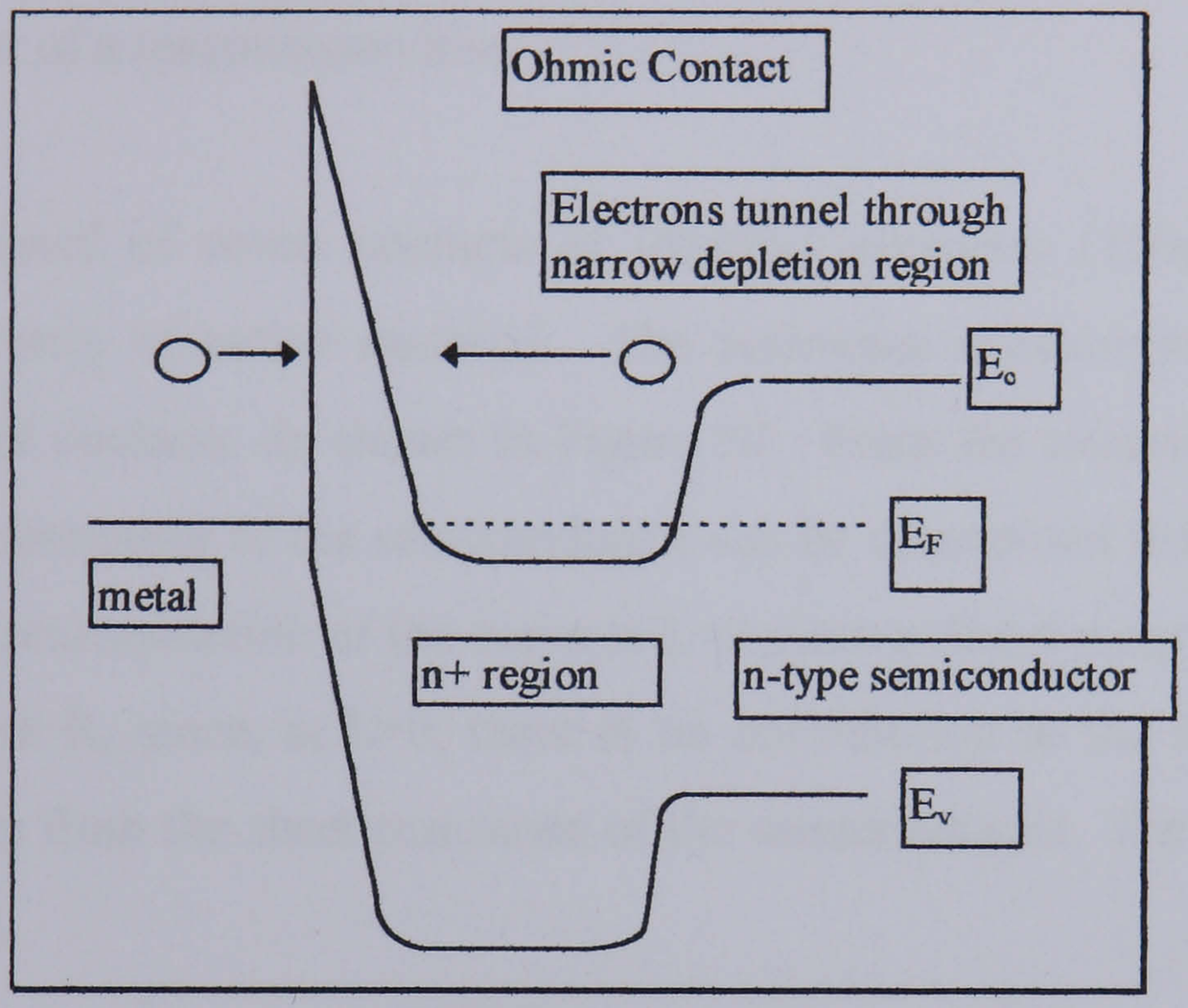


Figure 58 Energy Band Diagram of Ohmic contact

The two main current transport mechanisms associated with metal-semiconductor barriers - a) thermionic emission of carriers over the metal-semiconductor barriers b) tunnelling through the space charge region at the metal-semiconductor interface. On lightly doped substrates the thermionic emission dominates whilst on heavily doped substrates the tunnelling is dominant. Since the barrier height on GaAs is essentially independent of the barrier metal, the approach generally adopted to make an ohmic contact is to heavily dope the interface region between the semiconductor and the metal thus reducing depletion width to a minimum. If the depletion width is made sufficiently narrow then the electrons can tunnel through the barrier quite easily. A practical approach normally used for making low resistance Ohmic contacts is to use alloying to produce heavily doped regions. The most common ohmic recipe for GaAs is Au-Ge-Ni where the Ge diffuses in near the surface causing a very heavily doped n-region which is then contacted by the Ni-Au. The exact

nature of how this combination creates a good working ohmic contact is, however, not completely understood.

3.3.3.3.2 TLM - Transmission Line Model

The tool used in the analysis of planar ohmic contacts was the transmission line model (TLM)[3.3]. In this model the contacts are modelled as a distributed circuit analogous to that of a transmission line.

The TLM consisted of seven contacts of identical geometry (150μm x 150μm) patterned on a strip of active material. The resistance measurements are made between adjacent contacts, as shown in Figure 59. From the resulting R_t versus L graph the sheet resistance of the semiconductor can be determined from the slope of the curve. Also, extrapolation of the curve to L=0 gives a direct measurement of the contact resistance R_c since, at L=0, there is no contribution to the total resistance between contacts from the sheet resistance of the semiconductor. For more detailed theory, see [3.4].

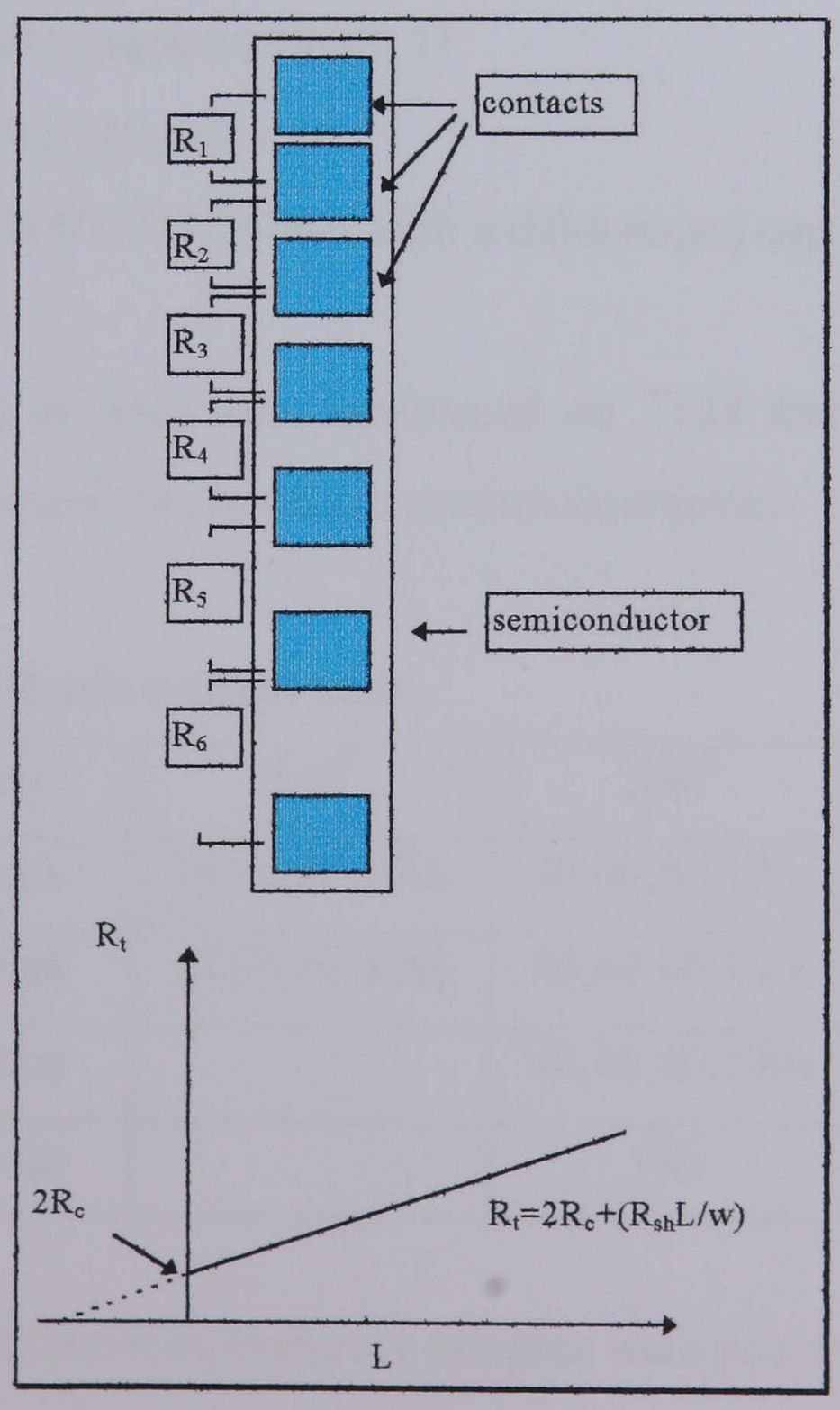


Figure 59 Transmission Line Test Structure

3.3.3.3.3 Ohmic metallisations

The initial recipe used was *Au/Ge/Au/Ni/Au:14/14/14/11/240nm* [3.5]. Previously measured values of contact resistance using this recipe with GaAs pHEMT devices gave R_c in the range 0.05-0.25 Ωmm (these measurements were done by Nigel Cameron at the University of Glasgow [3.8]), with an average of 0.15 Ωmm . From the published literature on ohmic contacts to GaAs, there are two basic combinations of metals - Pd/Ge and Au/Ge/Ni (with occasionally Ti included). It was decided to concentrate on the latter combination as this was already used in the existing process.

After a survey of the literature on Au/Ge/Ni/(Ti) ohmic contacts it was decided to try these four different metallisations:

a)Ge/Ni/Au/Ti/Au 70/140/50/20/70nm [3.6]

b)Ni/Ge/Au/Ti/Au: 10/13/26/50/100nm[3.7]

c)Au/Ge/Ni/Au:14/14/11/240nm [3.3]

d)Au/Ge/Au/Ni/Au:14/14/14/11/240nm with a delta doped cap layer

The following matrix of tests were performed on TLM test structures to try and identify possible improvements in ohmic contact resistance.

Table 3.1 Matrix of Ohmic contact tests

Anneal Temperature	**340^0**	**360^0**	**380^0**
Recipe a) anneal times	40,60,80,100s	40,60,80,100s	40,60,80,100s
Recipe b) anneal times	40,60,80,100s	40,60,80,100s	40,60,80,100s
Recipe c) anneal times		40,60,80,100s	
Recipe d) anneal times		60s	

For each recipe/anneal time/temperature 4 samples were processed to ensure that a reasonable spread of results was obtained.

a) For the Ge/Au/Ni/Ti/Au combination the measured values of R_c and R_{sh} are shown below versus anneal time and temperature.

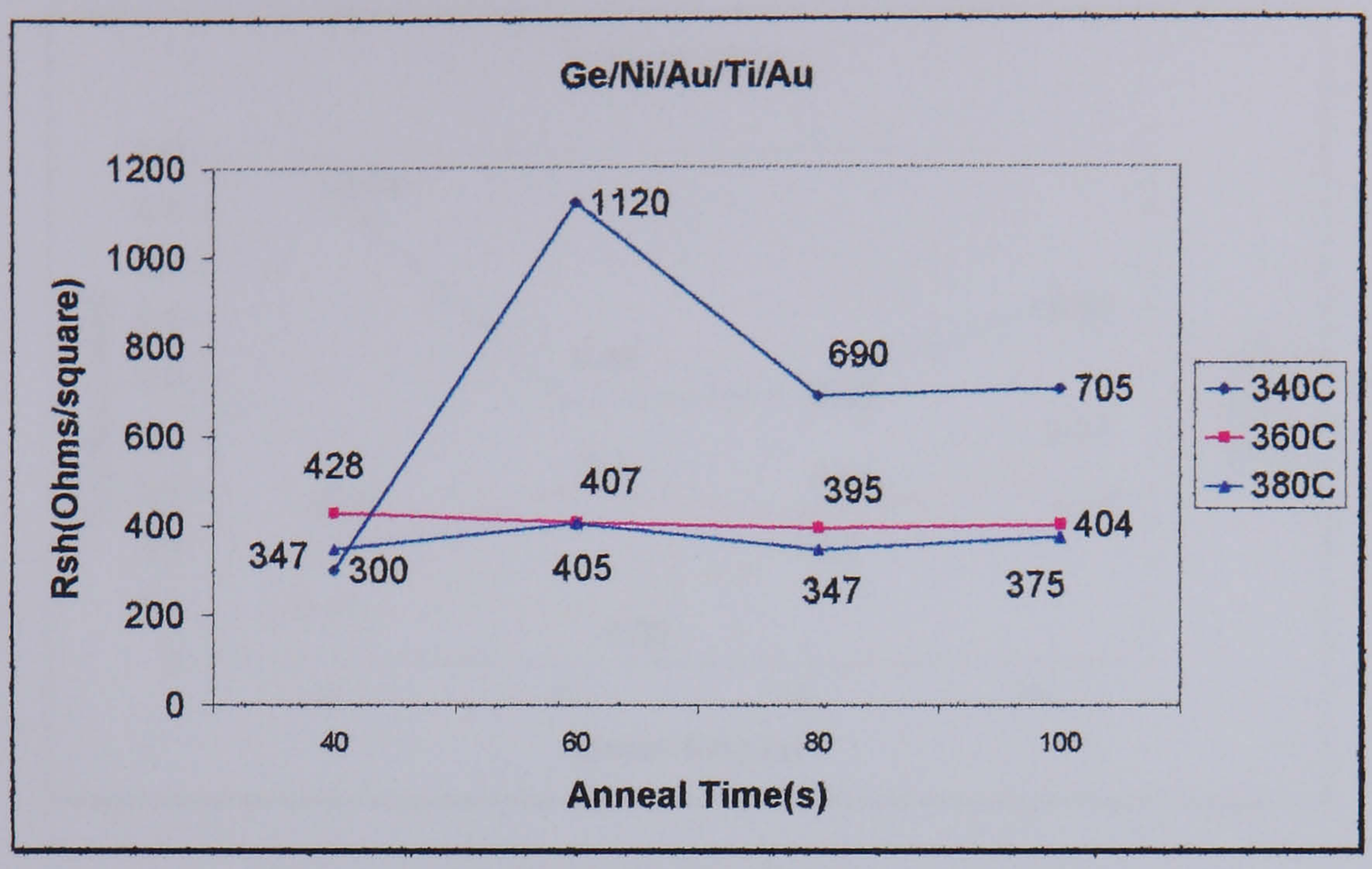


Figure 60 Rsh for Ge/Au/Ni/Ti/Au combination

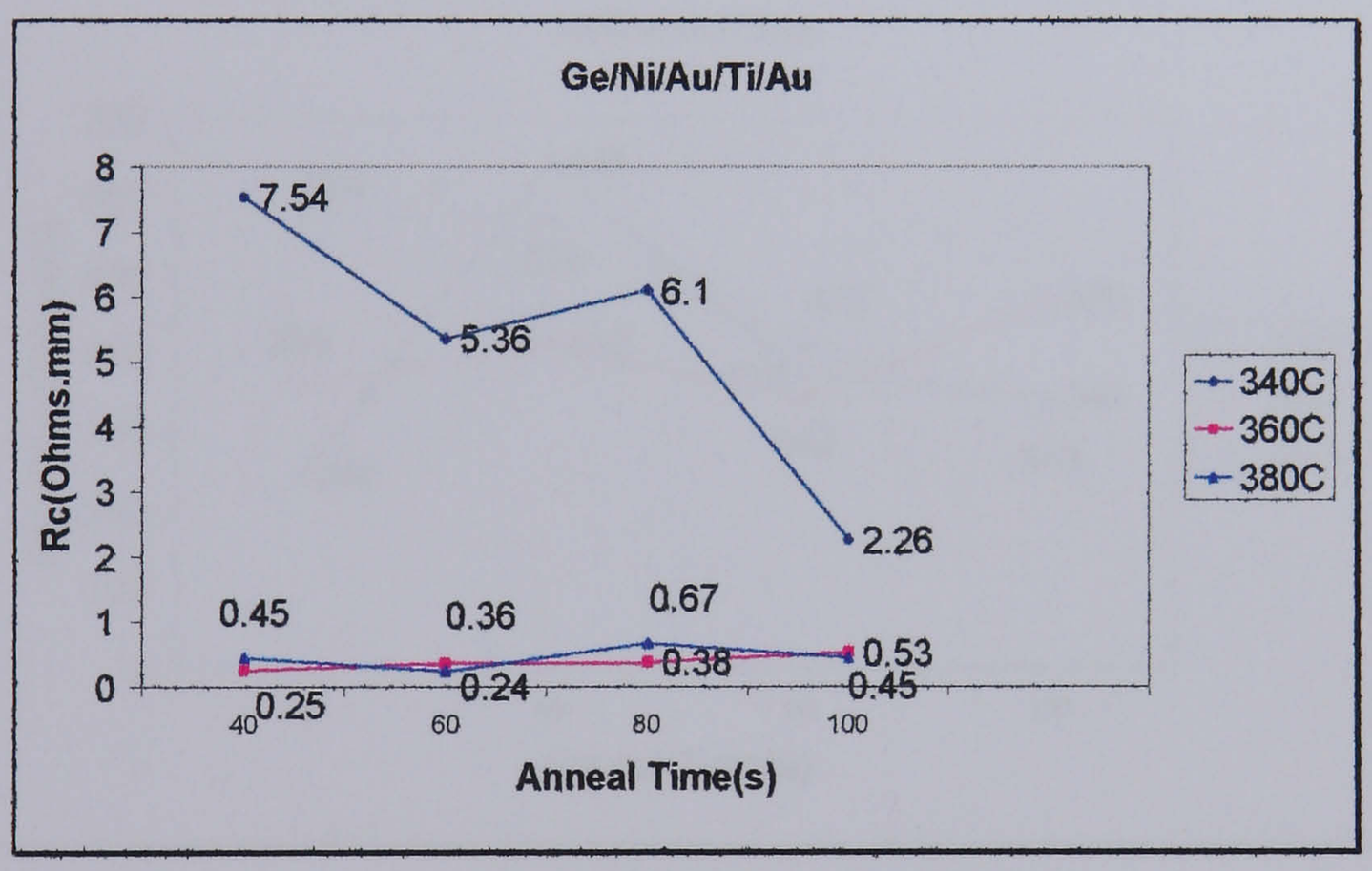


Figure 61 Rc for Ge/Au/Ni/Ti/Au combination

The values obtained for R_c were worse than that previously obtained using the original recipe. Values for R_{sh} are dependent on substrate properties and therefore the wide variation in values shown in Figure 60 must be attributed to measurement error.

b) For the Ni/Ge/Au/Ti/Au combination the measured values of R_c and R_{sh} are shown below versus anneal time and temperature.

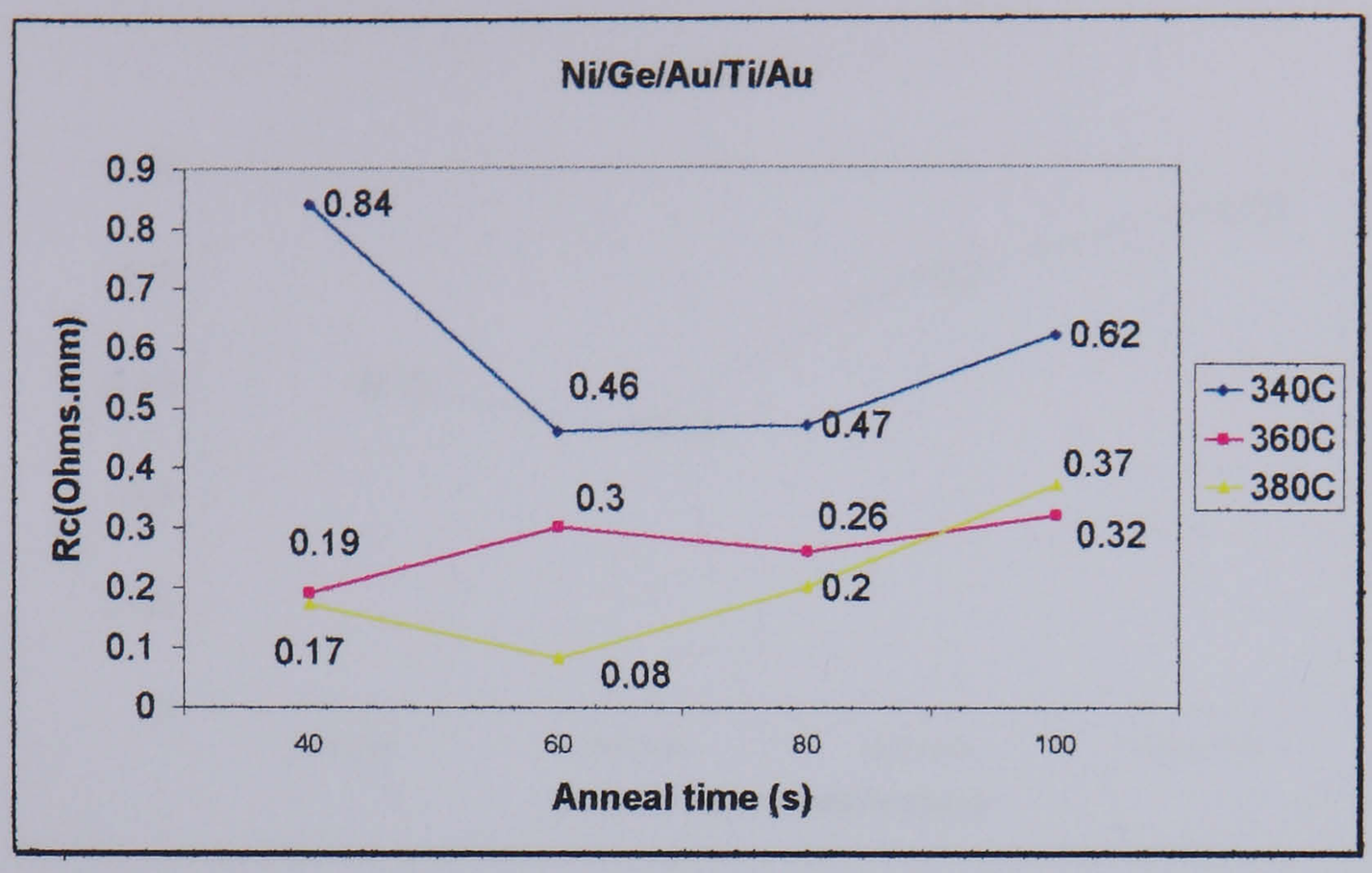


Figure 62 Rc for Ni/Ge/Au/Ti/Au combination

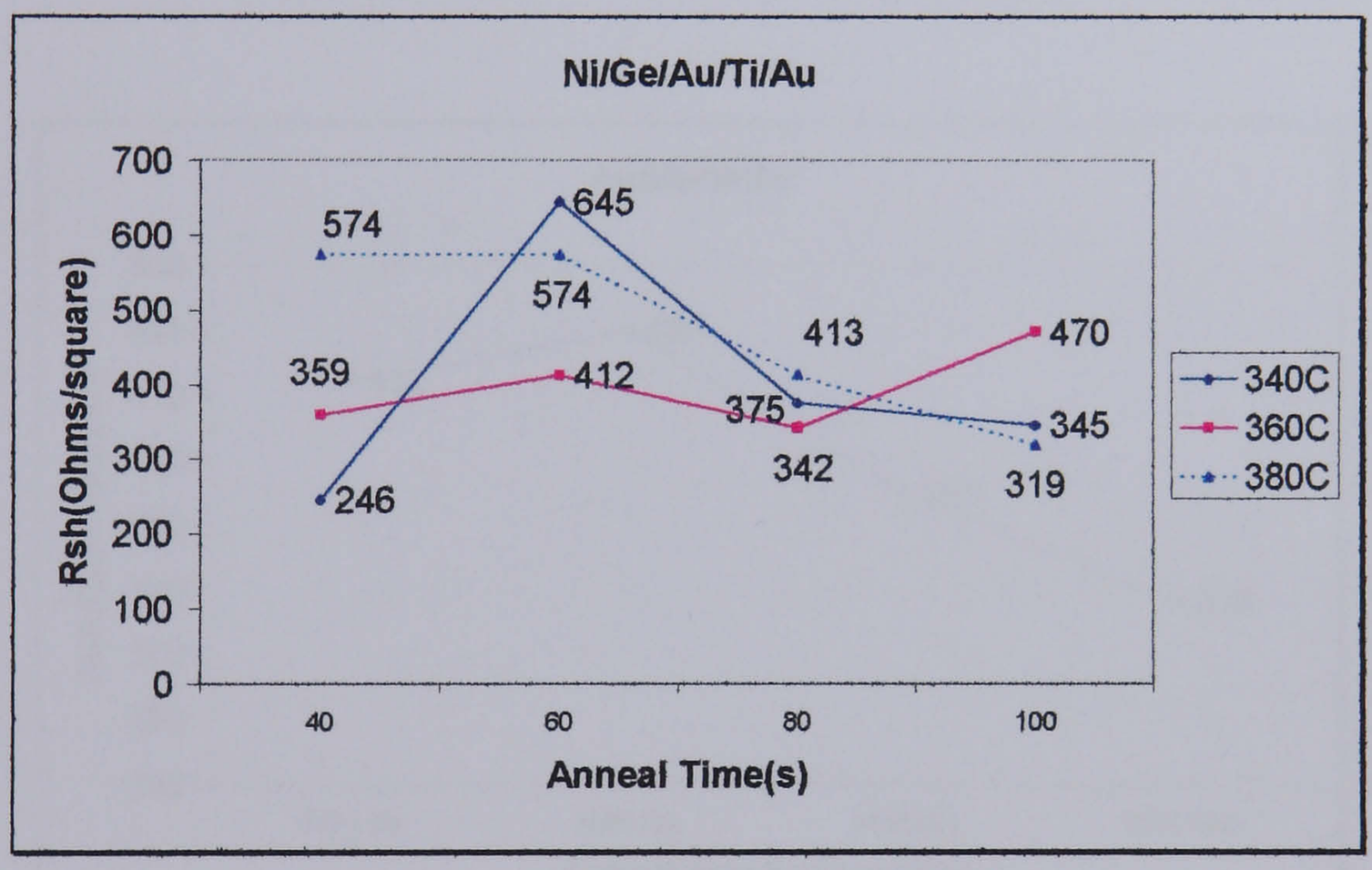


Figure 63 Rsh for Ni/Ge/Au/Ti/Au combination

Contact resistance values of 0.08 Ωmm were obtained for an anneal temperature of 380^{0}C and an anneal time of 60s. This represents an improvement in value of R_c from the previously measured average, though it is recognised that this was only for 4 samples (compared to the 20 samples used by N. Cameron). Again, note that measurement error is probably responsible for the large variation in R_{sh} from Figure 63.

c) For the Au/Ge/Ni/Au combination the measured values of R_c and R_{sh} are shown below versus anneal time and temperature.

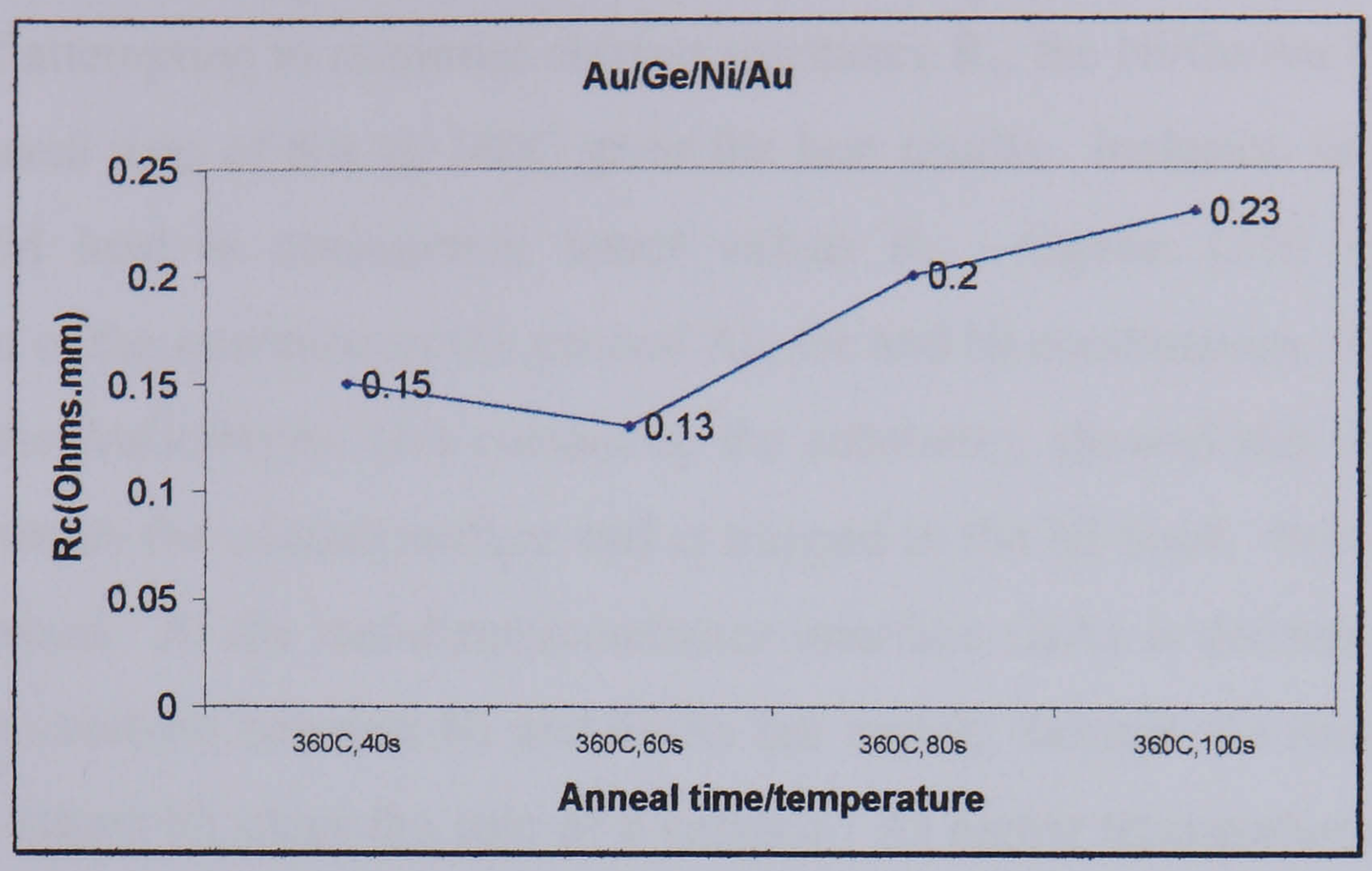


Figure 64 Rc for Au/Ge/Ni/Au combination

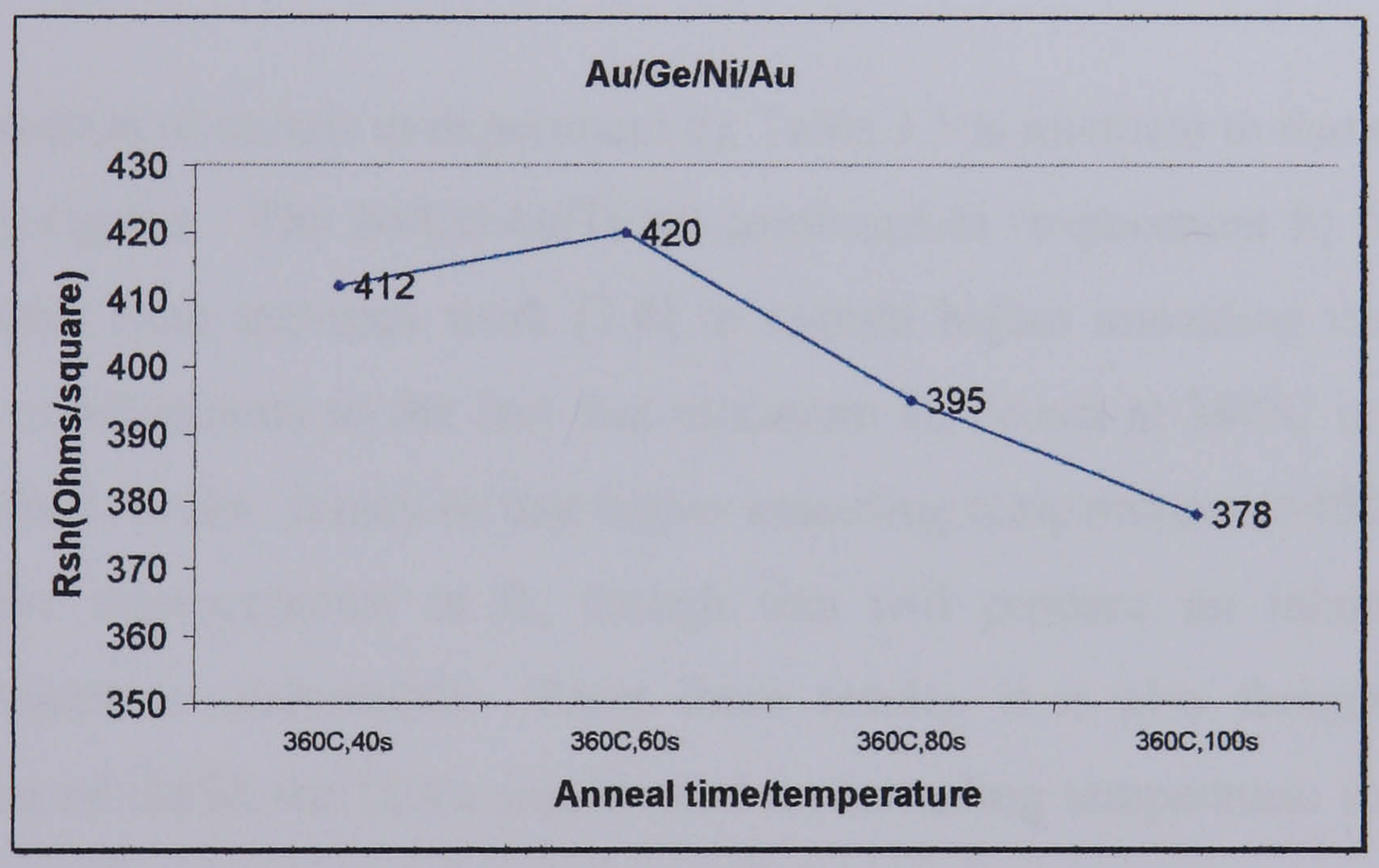


Figure 65 Rsh for Au/Ge/Ni/Au combination

These results represent no significant improvement on those obtained using the original recipe.

d) The contact resistance obtained using the original recipe with a delta doped cap layer was 0.12 Ohms.mm with a sheet resistance of 180 Ohms per square.

3.3.3.3.4 Discussion of Results

In terms of attempting to minimise contact resistance R_c, the Ni/Ge/Au/Ti/Au recipe with an anneal time of 60s @ 380C gives the best results. Inclusion in the process flow should lead to consistently lower values R_c. Ogawa [3.9] offers some explanation of the operation of the general Au, Ge and Ni combination. His analysis, given for the AuGe/Ni/Au (Au contacting the substrate), showed that at 300^0C Ge diffuses towards the contact surface and is trapped in the Ni layer. Some of the Ni diffuses inward. At the metal-semiconductor interface GaAs is decomposed partly through the reaction between Ni and GaAs but mainly through the reaction of Au with GaAs where Ni plays the role of a catalyst. At higher temperatures (nearer to 400^0C) the Ge, which was trapped at the surface diffuses inwards and is partly captured by NiAs. The rest of the Ge is considered to be doped into the GaAs.

The combination of metals in experiment c), Table 3.1 is identical to that used in the analysis by Ogawa. The Ni/Ge/Au/Ti/Au combination (experiment b) from Table 3.1) is known from previous work [3.4] to require higher annealing temperatures than other combinations so the fact that minimum R_c occurs at 380^0C is consistent with published results. It may be that higher annealing temperatures (>400^0C) would yield further improvements in R_c though this will produce an inhomogeneous interface which is undesirable. From these results, it is also thought that the combination of Ge/Ni/Au/Ti/Au would need an annealing temperature in excess of 400^0C to provide suitably low values for contact resistance.

The results from d) show that the inclusion of a delta doped cap layer improves the contact resistance of the standard Au/Ge/Au/Ni/Au recipe to 0.12 Ohms.mm. Therefore, if the Ni/Ge/Au/Ti/Au metallisation was used in combination with a delta doped cap layer, values of R_c could be further improved.

3.3.4 Isolation

Electrical isolation of the diode was achieved using the mesa technique (see Figure 66). Current is confined by etching away material everywhere except on the active device areas. The anode fingers have to be able to "climb" over the edge of the mesa to form a connection to the active material so the height of the mesa must be carefully controlled. If it is too high then the anode metallisation may be insufficient to surmount the mesa. Alternatively if it is too low then the mesa may not be able to provide adequate isolation between adjacent devices. Therefore, the height of the mesa was monitored using a Talystep and electrical measurements were made to ensure that isolation was sufficient. Note that very little modification was necessary to this step of the process.

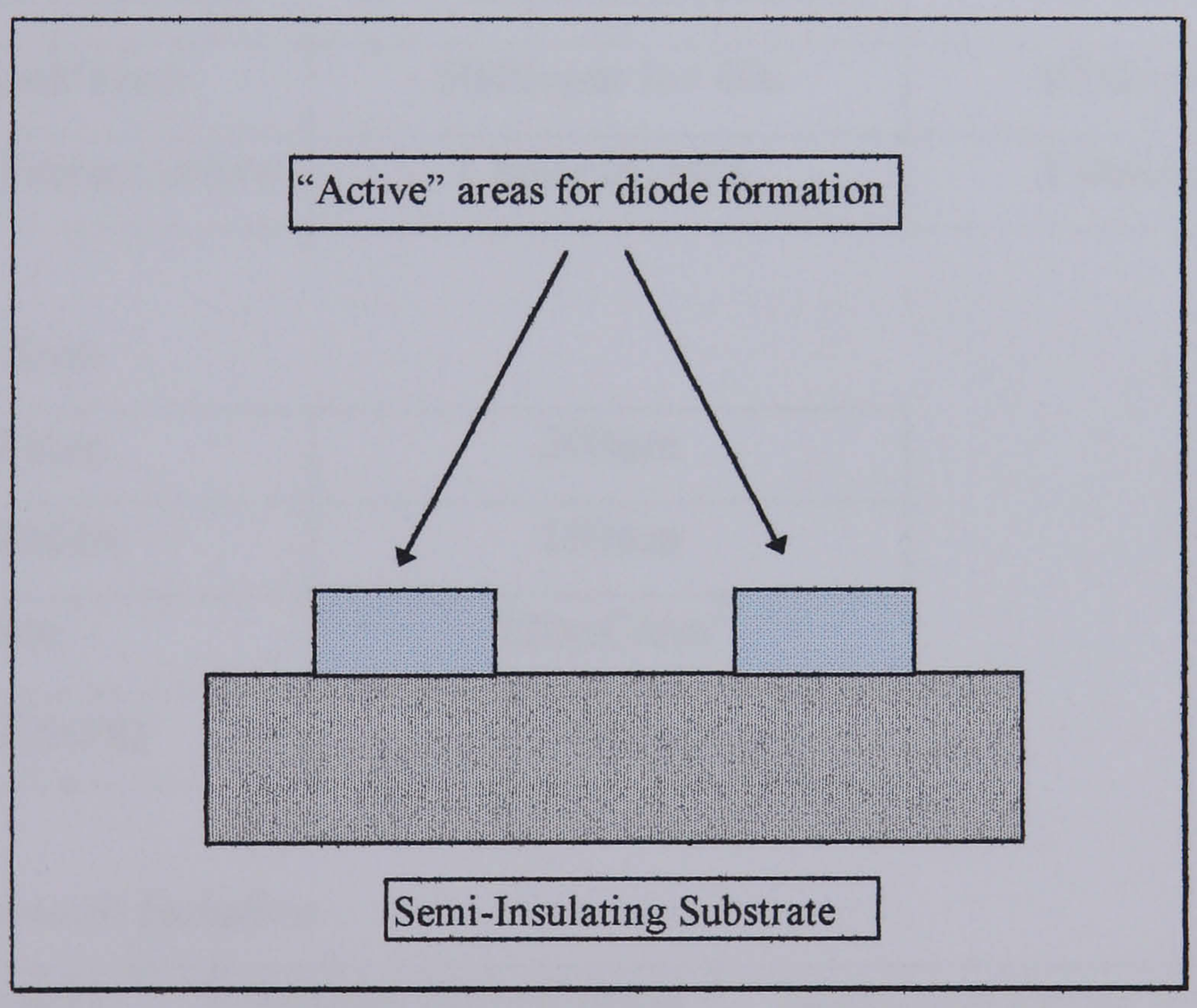


Figure 66 Mesa Isolation - cross section

PMMA was used in the mask for isolation but unlike all other processing steps (with the exception of Si_3N_4 etching in circuits using MIM capacitors), it was necessary to expose all other areas of the wafer except for the active "mesa" areas. This was essential as all the epitaxial layers had to be etched away to prevent nearby active devices from interacting. This was obviously time consuming. It was essential that the mesa area extended beyond the ohmic metal to prevent this being attacked by the

wet chemical etchant. A boundary of one micron was essential. This is shown in Figure 67.

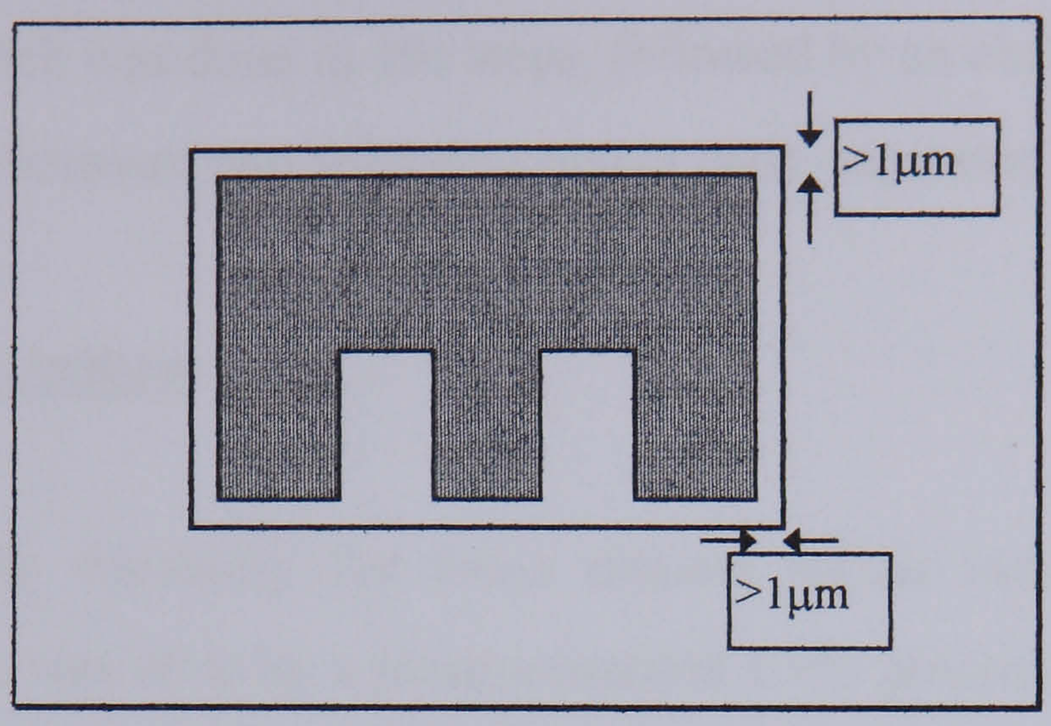


Figure 67 Mesa Isolation - Top view

Process Details:

a) ***Resist application***

	1st Layer Resist	2nd Layer Resist
Resist Type/Thickness	**12% BDH/ALD(600nm)**	**4% ELV(100nm)**
Spin Speed/Time	**5000rpm for 60s**	**5000rpm for 60s**
Bake Time/Temperature	**1 hour@180°C**	**2 hours@180°C**

b) ***Exposure Step***

Spot size	**300nm**
Resolution	**150nm**
Dose	**220μC/cm²**
Beam Energy	**50kV**

c) ***Development & Isolation***

Development	Ashing, de-oxidation	Isolation&Resist Strip
1:1 IPA:MIBK, 30s **Rinse IPA, 30s** **Blow Dry N_2** **Bake 120°C, 30mins**	**Ash, 60s** **De-oxidise:** **4:1 H_2O/HCl, 30s** **Rinse IPA, 30s** **Blow Dry N_2**	**Wet etch,10s steps:** **H_2O:H_2O_2:NH_3 - 200:1:1** **Resist Strip:** **Acetone(45°C), 30mins** **Rinse IPA, 30s** **Blow Dry N_2**

Process notes

The isolation wet etch was done in 10s steps, followed by an electrical measurement until the resistance between two adjacent contact pads, separated by 5μm, was of the order of 10^9 Ohms.

3.3.5 Dielectric Deposition

This step was only necessary for those circuits which used MIM capacitors. Deposition of Si_3N_4 was done by a plasma-assisted CVD process (see [3.1] for more details).

Process Details:

a) Si_3N_4 deposition - 150 nm

b) *Resist application*

	1st Layer Resist	2nd Layer Resist
Resist Type/Thickness	**12% BDH/ALD(600nm)**	**4% ELV(100nm)**
Spin Speed/Time	**5000rpm for 60s**	**5000rpm for 60s**
Bake Time/Temperature	**1 hour@180°C**	**2 hours@180°C**

c) Exposure Step

Spot size	**300nm**
Resolution	**150nm**
Dose	**220μC/cm²**
Beam Energy	**50kV**

d) Development & Etching

Development	Ashing, de-oxidation	Isolation&Resist Strip
1:1 IPA:MIBK, 30s **Rinse IPA, 30s** **Blow Dry N_2** **Bake 120°C, 30mins**	**Ash, 60s** **De-oxidise:** **4:1 H_2O/HCl, 30s** **Rinse IPA, 30s** **Blow Dry N_2**	**Dry etch SF_6 - endpoint** **Resist Strip:** **Acetone(45°C), 30mins** **Rinse IPA, 30s** **Blow Dry N_2**

Process notes

Similar to the mesa isolation step, it was necessary to expose all other areas of the wafer except for the capacitor areas. Note that it was often necessary to dip the wafer in Buffered HF after dry etching to remove small areas of remaining Si_3N_4. No electrical measurements were performed to assess the impact of the SF_6 dry etch process on the substrate.

3.3.6 Anode

3.3.6.1 Overview

A considerable amount of development was necessary to this stage as the original process used "T-gates". Therefore a process for developing "pyramidal" shaped anodes was necessary **using the tri-layer resist scheme** to ensure compatibility with amplifier fabrication. In addition, a new four-layer resist combination was developed to enable thicker metal to be deposited and lifted-off thus reducing metallic resistance. Also, a significant study of the existence of elastic strain, caused by the anode on the semiconductor surface, showed that any such strain was negligible at room temperature - in marked contrast to much lower temperatures as demonstrated by Davies and Larkin.

3.3.6.2 Pyramidal Anode

As the philosophy of this thesis was to work towards the complete monolithic integration of amplifier and mixer on single substrate then all anode levels were made using the tri-layer resists scheme normally associated with FET processing.

Process Details:

a) ***Resist application***

	1st Layer Resist	2nd Layer Resist	3rd Layer Resist
Resist Type/Thickness	**4% ELV(100nm)**	**9% COPOLY**	**2.5% BDH/ALD**
Spin Speed/Time	**5000rpm for 60s**	**5000rpm for 60s**	**5000rpm for 60s**
Bake Time/Temperature	**1hour@180^{O}C**	**1hour@180^{O}C**	**12 hours@180^{O}C**

b) ***Exposure Step***

Spot size	**20nm**
Resolution	**10nm**
Base Dose	**100μC/cm^2**
Beam Energy	**50kV**

c) ***Development & Metallisation***

Development	Dry Etching	Metallisation
2.5:1 IPA:MIBK,30s **Rinse IPA, 30s** **Blow Dry N_2**	**Gas Flows:** **$SiCl_4$:1.2sccm** **SF_4:8.2sccm** **O_2:0.1sccm** **Pressure:145mT** **RF power:17W** **Time:90-120s**	**15 nm Ti** **15 nm Pd** **160nm Au** **Lift-off:** **Acetone(45^{O}C), 30mins** **Rinse IPA, 30s** **Blow Dry N_2**

.

<u>Process notes</u>

The base dose shown in the development stage was increased depending on the desired anode length as follows:

0.2μm -600μC/cm^2

0.5μm -500μC/cm^2

0.8μm -400μC/cm^2

These doses were decided upon after a series of exposure tests. It was necessary to bake the final layer of resist for 12 hours (minimum), to prepare the tri-layer resist for exposure. The resolution and spot size were necessarily small as the minimum feature size was small and were the same as the original process. The initial metallisation was Ti/Au but it was found that after being subjected to the high temperatures of the subsequent level of processing (Final layer metal/interconnects) the Au could diffuse through the Ti and alter the Schottky barrier characteristics. Therefore, Pd was incorporated as a barrier to prevent this reaction from taking place.

The etch time was adjusted to recess the contact properly. This was controlled by etching a test sample, patterned with many long pyramidal anodes on the same substrate as the actual circuits, and measuring the anode recess offset using a SEM micrograph. To see why this was necessary, some description of the etching process is helpful.

The width of the anode recess and the offset(the distance between the gate metal and the recess edge) have a considerable effect on the diode series resistance. This can be seen from Figure 30, as the resistivity of the etched region between anode and cathode is greater than the unetched region. The selective reactive ion etching process for anode recessing, used $SiCl_4/SiF_4$ and a small amount of O_2. It was the O_2 that had a strong influence on the lateral etch rate and, since the mass flow controller for O_2 was unreliable, the actual offset had to be checked using a test sample before each circuit wafer was etched. Using this combination of $SiCl_4/SiF_4/ O_2$, the oxygen enhances the formation of volatile Cl_x species, and so reduces the formation of polymeric deposits on the etched surface.

Several different experiments were performed after development and prior to metallisation and these are detailed overleaf. This was done due to poor mechanical yield at this process step.

1) Ashing, dry etch, metallisation

2) Oxidise, dry etch, metallisation

3) Dry etch, oxidise, metallisation

4)Dry etch, wet etch, metallisation

In processing terms the experiments 1) to 4) worked as follows:

1) Lift-off excellent.

2) Lift-off excellent.

3) Lift-off excellent.

4)Lift-off very poor.

Therefore, it can be concluded that in processing terms, it would be possible to incorporate any of the following steps: 1) Ash before dry etch; 2) Oxidation before dry etch; 3) Oxidation after dry etch. The purpose of the ash step is generally to remove any resist deposits remaining on the wafer after development. It was previously believed that this step might not be suitable for such fine dimensions as are used at the anode level. The oxidation steps before and after dry etch were experimented with simply to clean the wafer surface. Similarly, the wet etch step was tried to remove any deposits left after the dry etch step. However, no assessments to find out the possible impact of any of these experiments on electrical characteristics were performed.

3.3.6.3 T-shaped anode

To reduce the resistance of the anode fingers as anode length is reduced, a T-gate structure can be used. This technique is often deployed in the manufacture of high-frequency FETs and is illustrated in Figures 68,69,70.

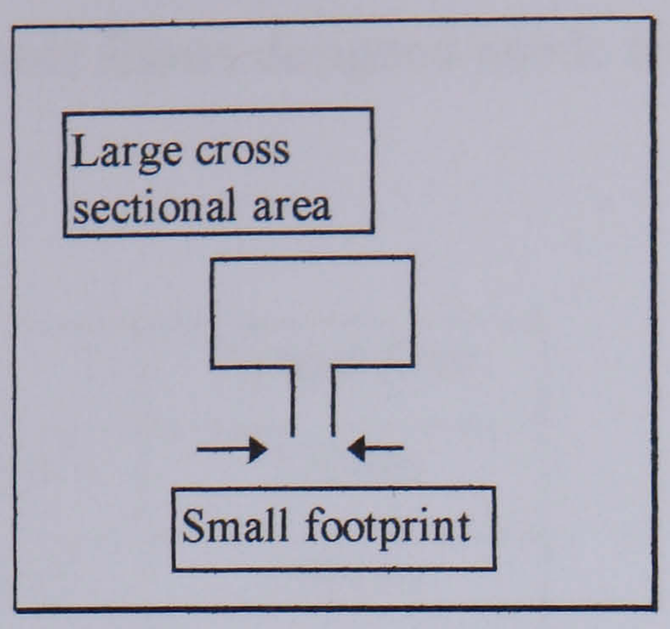


Figure 68 T-gate structure

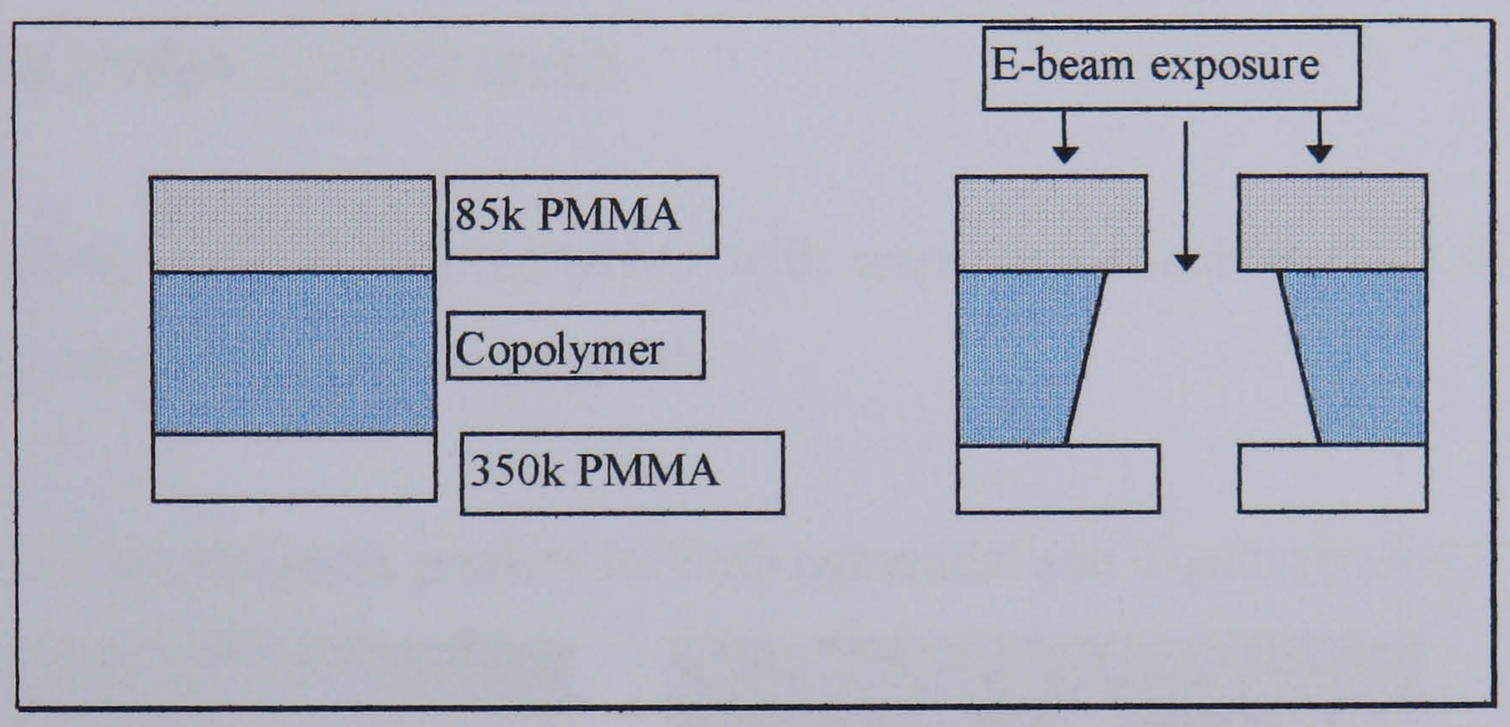


Figure 69 T-gate resist profile

The doses assigned to the particular patterns were as follows:

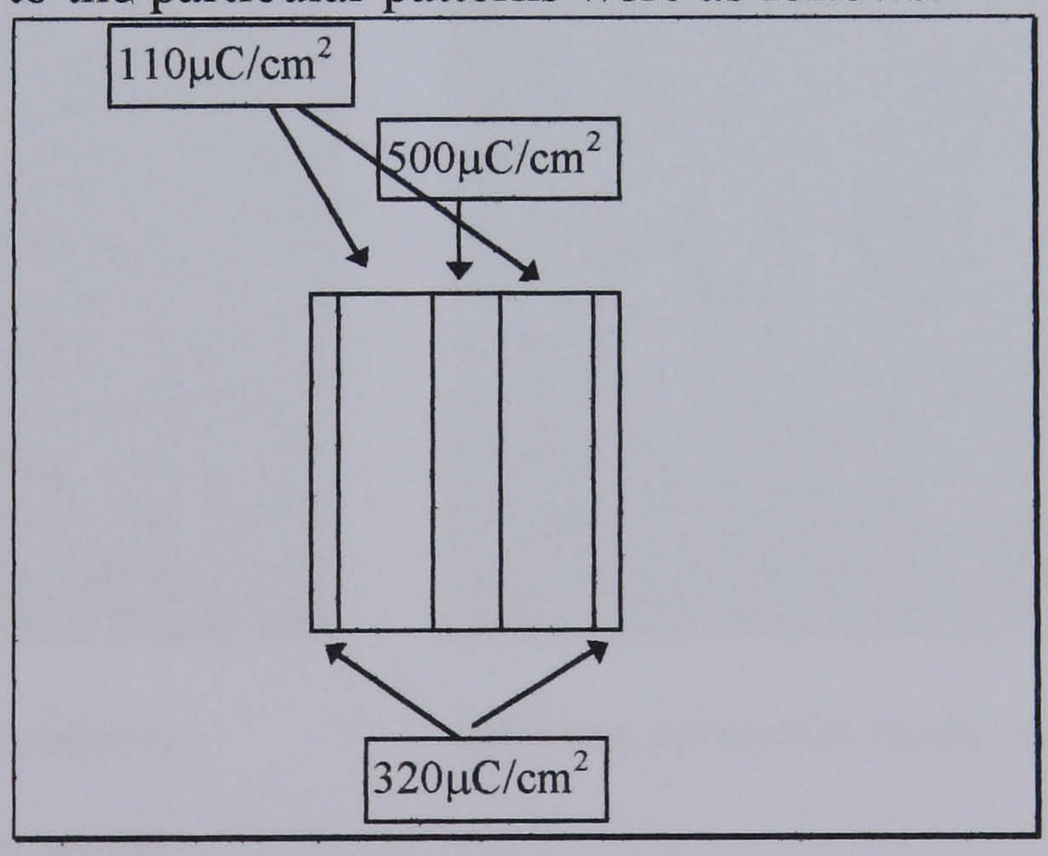


Figure 70 T-gate Exposure Doses

The bottom, anode length defining layer is a thin layer of 350k mw PMMA. The middle layer was a thick layer of a co-polymer of methylmethacrylate and methacrylic acid which has a greater sensitivity than PMMA. The top layer was a thin layer of 85k mw PMMA, used to provide an overhanging resist profile and so make lift-off easier. Note that the centre dose of 500μC/cm^2 was for an anode length

of 200nm. The following table shows designed anode length, dose and actual anode length:

Table 3.2 Anode lengths

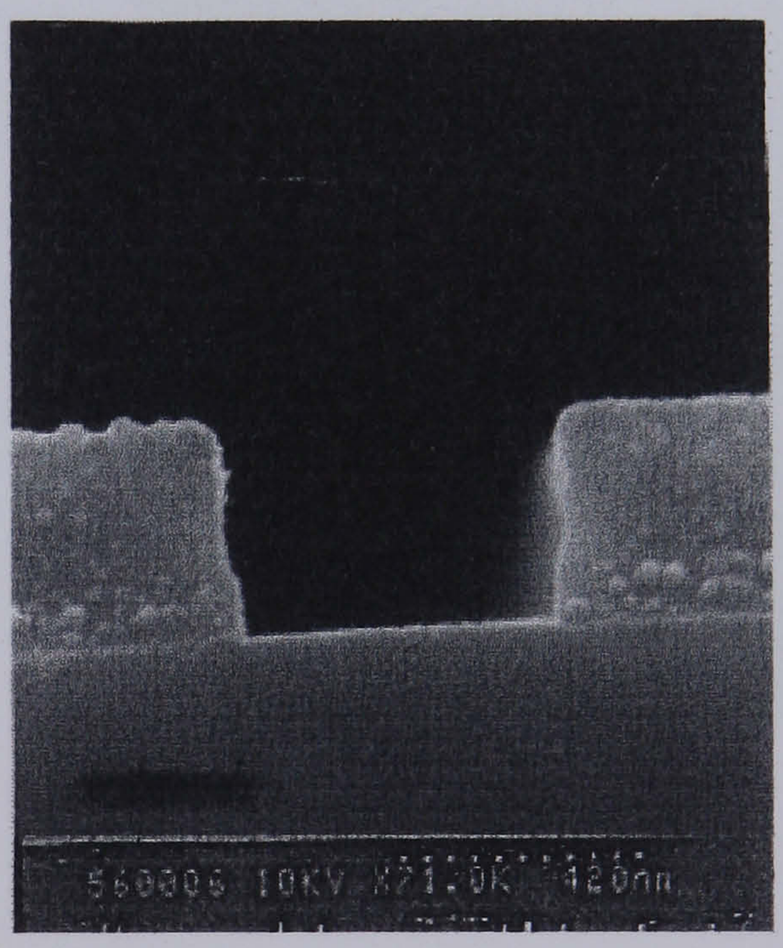
Design size	Dose	Actual Size
40nm	600μC/cm^2	120nm
120nm	500μC/cm^2	200nm
200nm	400μC/cm^2	280nm

3.3.6.4 Wet etching of anode recess

This was done using $H_2SO_4/H_2O_2/H_2O$ with respective concentrations of 1:1:200. Etching was done for a fixed time of 60s.

Shown below are the resist profiles for both pyramidal and T-gate anodes.

Figure 71 a) 200nm pyramidal anode resist profile



b)500nm pyramidal anode resist profile

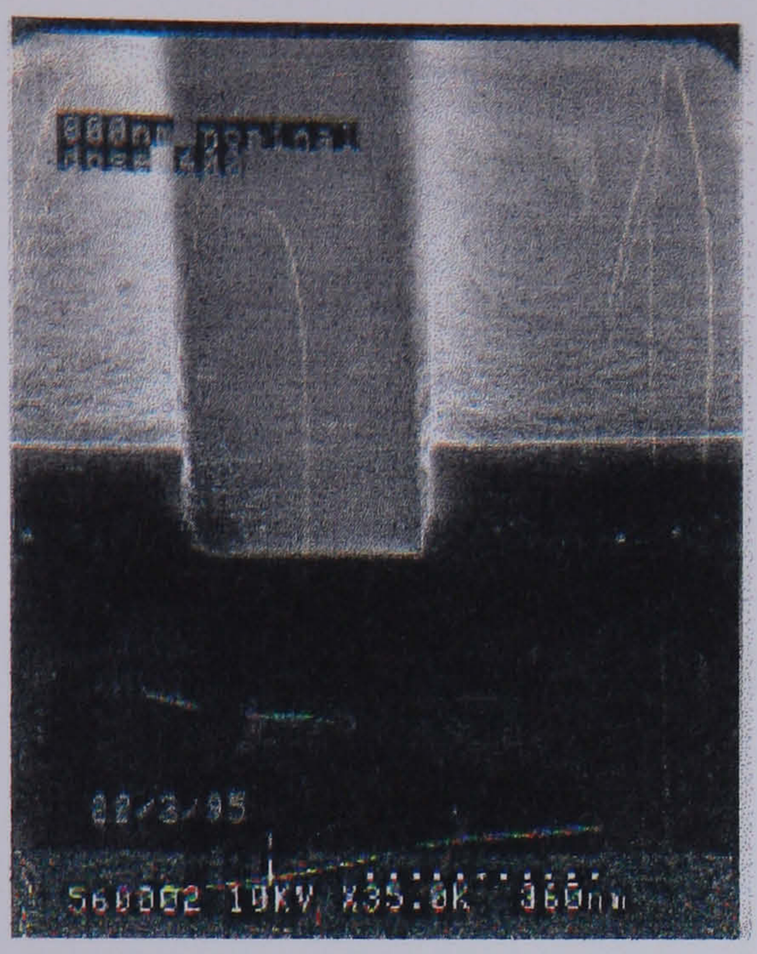
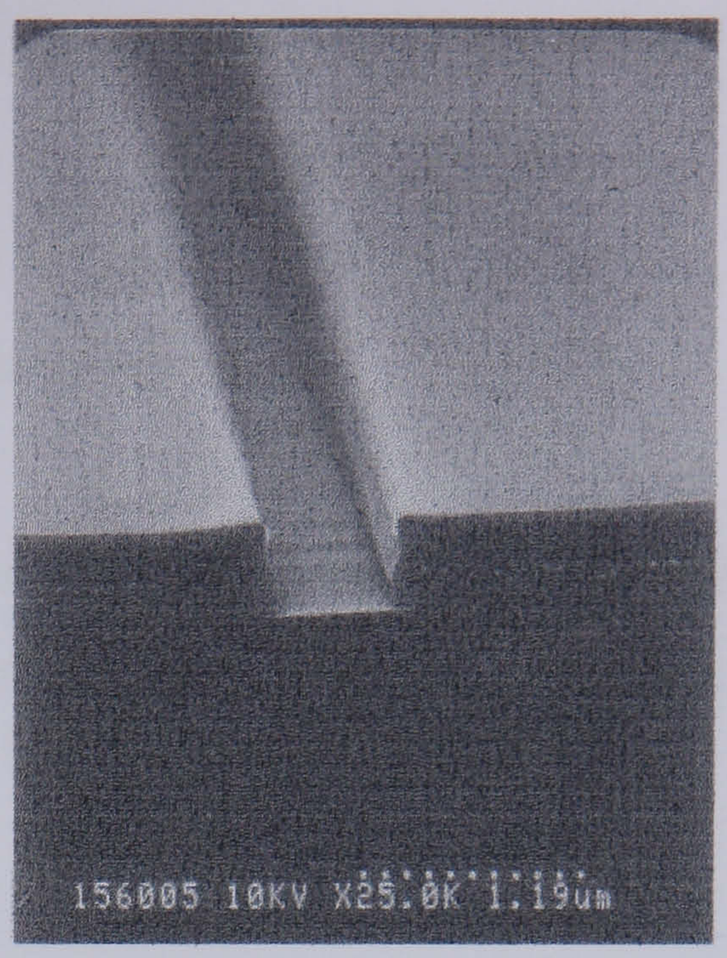


Figure 72 a) 800nm pyramidal anode resist profile



b)500nm pyramidal anode dry etch resist profile

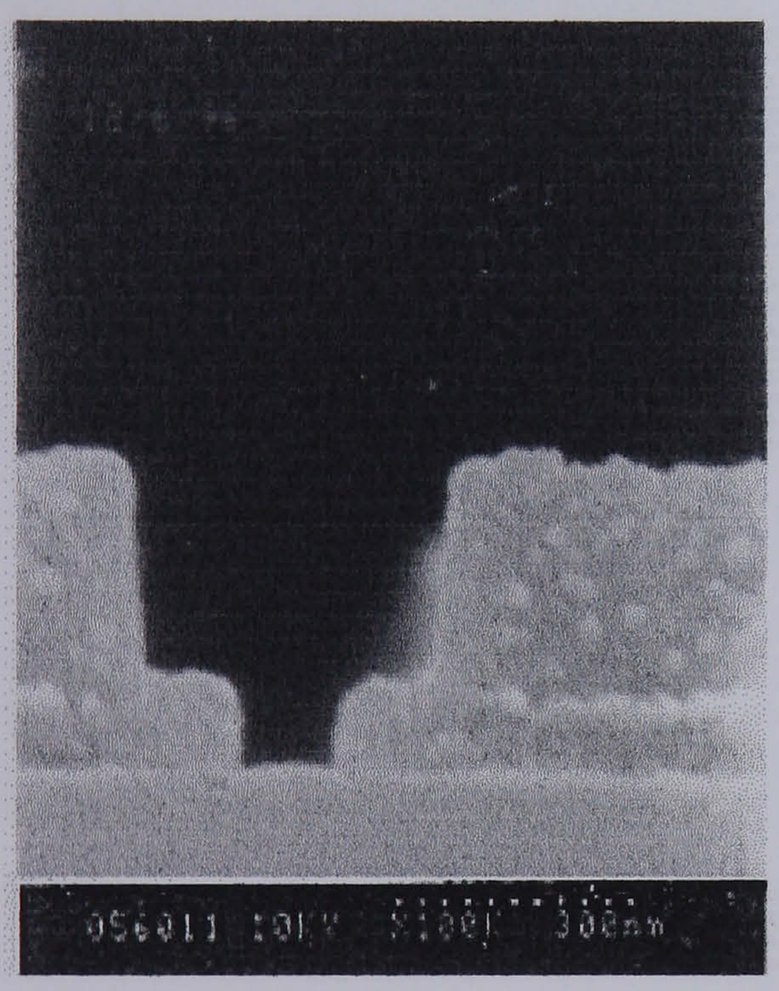
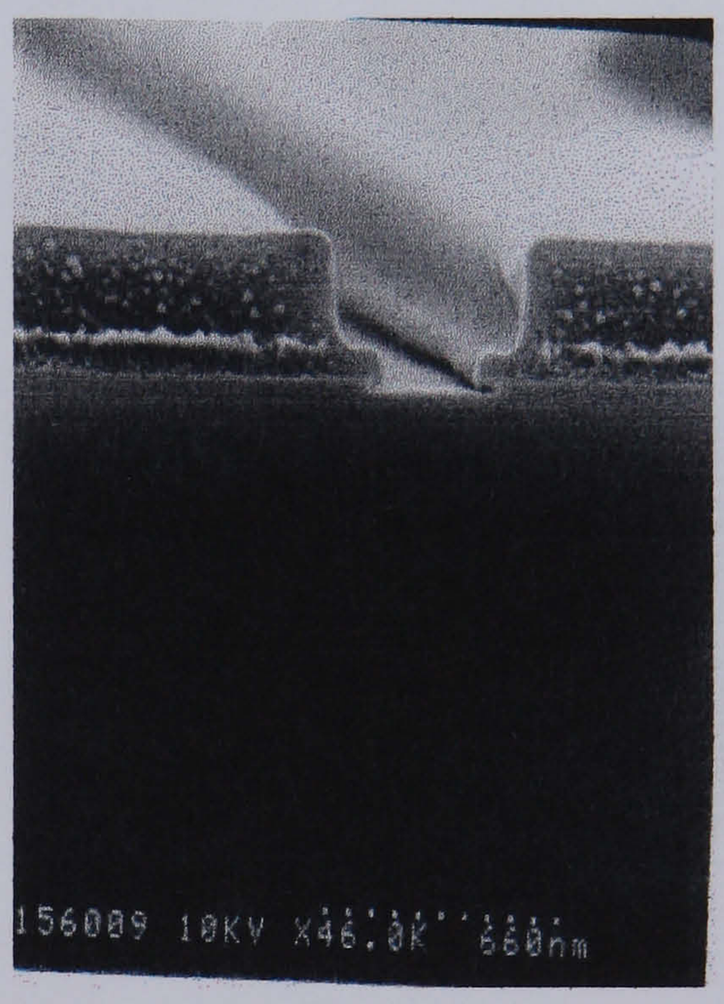


Figure 73 a)T-gate resist profile



b)Dry etched, recessed T-gate

The details of this "T-gate" process were common to the existing FET process. One disadvantage of this system was that it allowed only 160nm Au to be safely lifted-off, thus giving the profile shown in Figure 75. A new process was developed which allowed twice as much Gold to be deposited and lifted-off at the anode metallisation step. This will result in a decrease in the anode metallic resistance although no measurements were done to confirm this. The changes to the fabrication process were relatively simple and are now described:

Spin 4%ELV for 60s at 5000rpm and bake for 1 hour at 180C

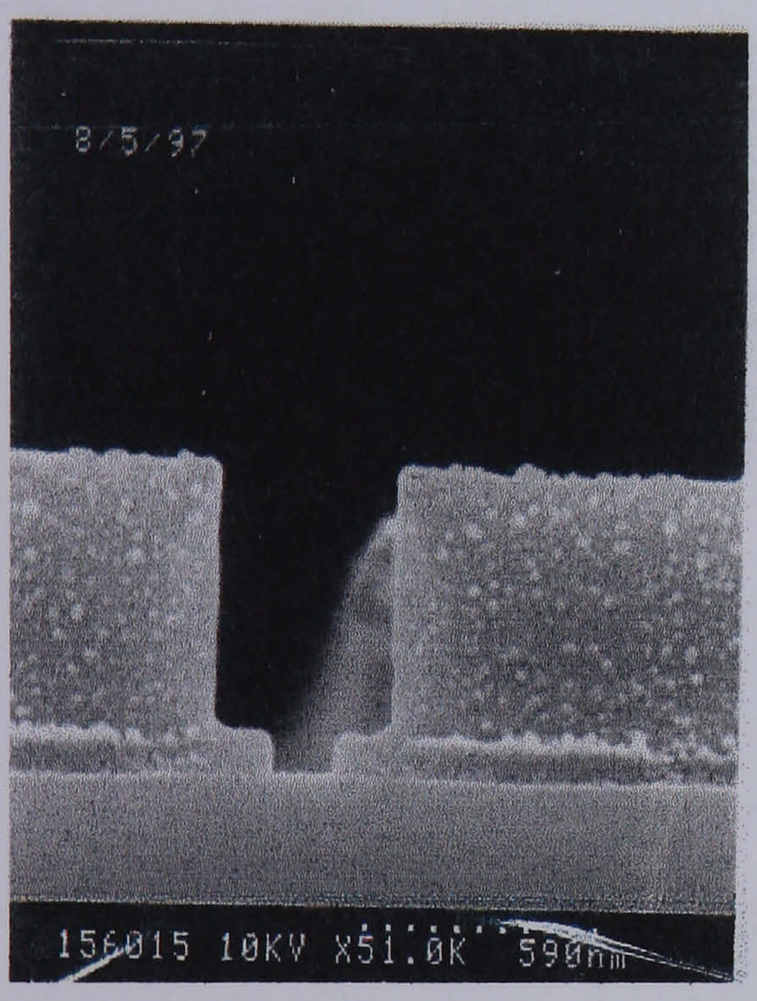
Spin 9%COPOLY for 60s at 5000rpm and bake for 1 hour 180C

Spin 9%COPOLY for 60s at 5000rpm and bake for 1 hour 180C

Spin 2.5%BDH/ALD for 60s at 5000rpm and bake overnight

Exposure doses are as follows: Centre dose is 400,500,600μC/cm^2 (depending on anode width for pyramidal and "T-gate" profiles), edge dose is 340μC/cm^2 and middle dose is 150μC/cm^2.

The profile of both unmetallised and metallised structures are shown below.



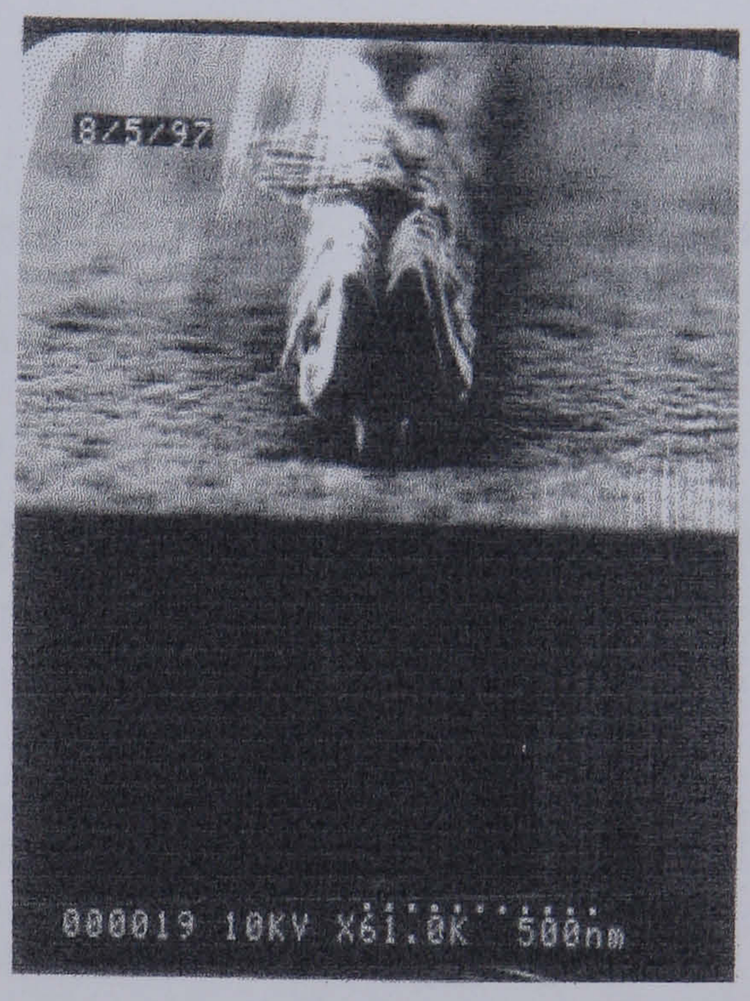


Figure 74 a)Thicker T-gate resist profile

b) 300nm Au anode

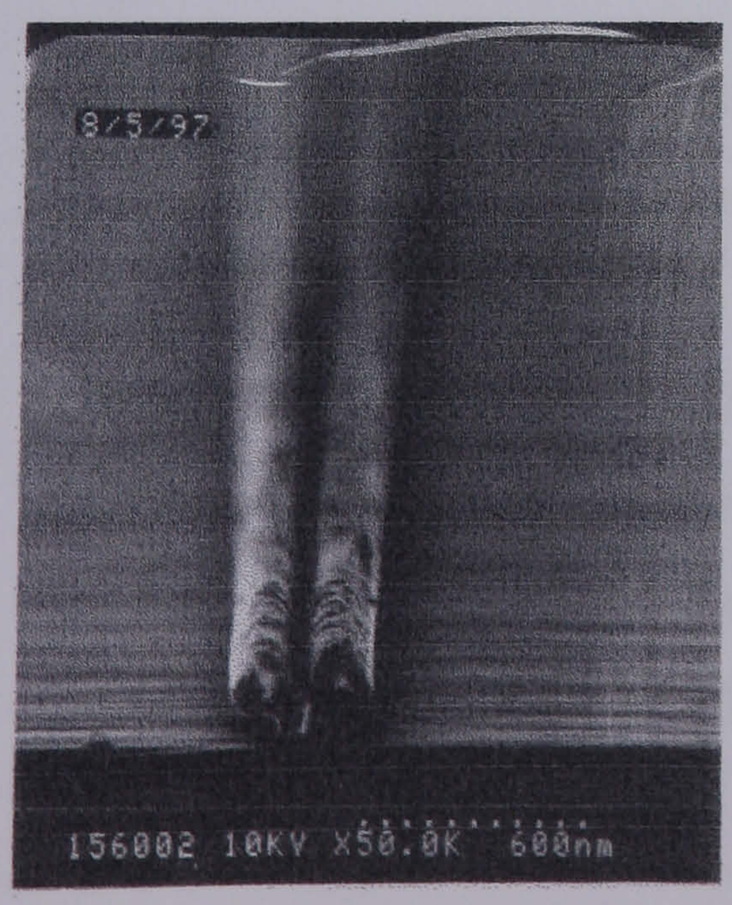


Figure 75 160nm Au anode

3.3.7 Final layer metal/Interconnects

The final layer metal/interconnect level was used for both DC and RF testing but due to the high frequencies involved and the subsequent signal attenuation due to the *skin effect*, it was necessary to deposit as much Au as possible in order to minimise conductor losses during testing. Therefore, a thick resist profile was required for this step.

Process Details:

a) ***Resist application***

	1st Layer Resist	**2nd Layer Resist**
Resist Type/Thickness	**15% BDH/ALD(1400nm)**	**4% ELV(100nm)**
Spin Speed/Time	**5000rpm for 60s**	**5000rpm for 60s**
Bake Time/Temperature	**1 hour@120°C**	**2 hours@120°C**

b) ***Exposure Step***

Spot size	**300nm**
Resolution	**150nm**
Dose	**250μC/cm^2**
Beam Energy	**50keV**

c) ***Development & Metallisation***

Development	**Ashing, de-oxidation**	**Metallisation**
1:1 IPA:MIBK, 30s **Rinse IPA, 30s** **Blow Dry N_2**	**Ash, 60s** **De-oxidise:** **4:1 H_2O/HCl, 30s** **Rinse IPA, 30s** **Blow Dry N_2**	**50nm NiCr** **400nm Au** **Lift-off:** **Acetone(45°C), 30mins** **Rinse IPA, 30s** **Blow Dry N_2**

3.3.8 Airbridge process

The airbridge process was used to connect Coplanar Waveguide ground planes together. This standard process existed as part of the FET process and no significant changes were necessary, although comments 2) and 3) at the end of the process notes were observed during fabrication. Figure 76 is a schematic diagram of the airbridge process used at the University of Glasgow. This is an all photolith process with no e-beam lithography steps.

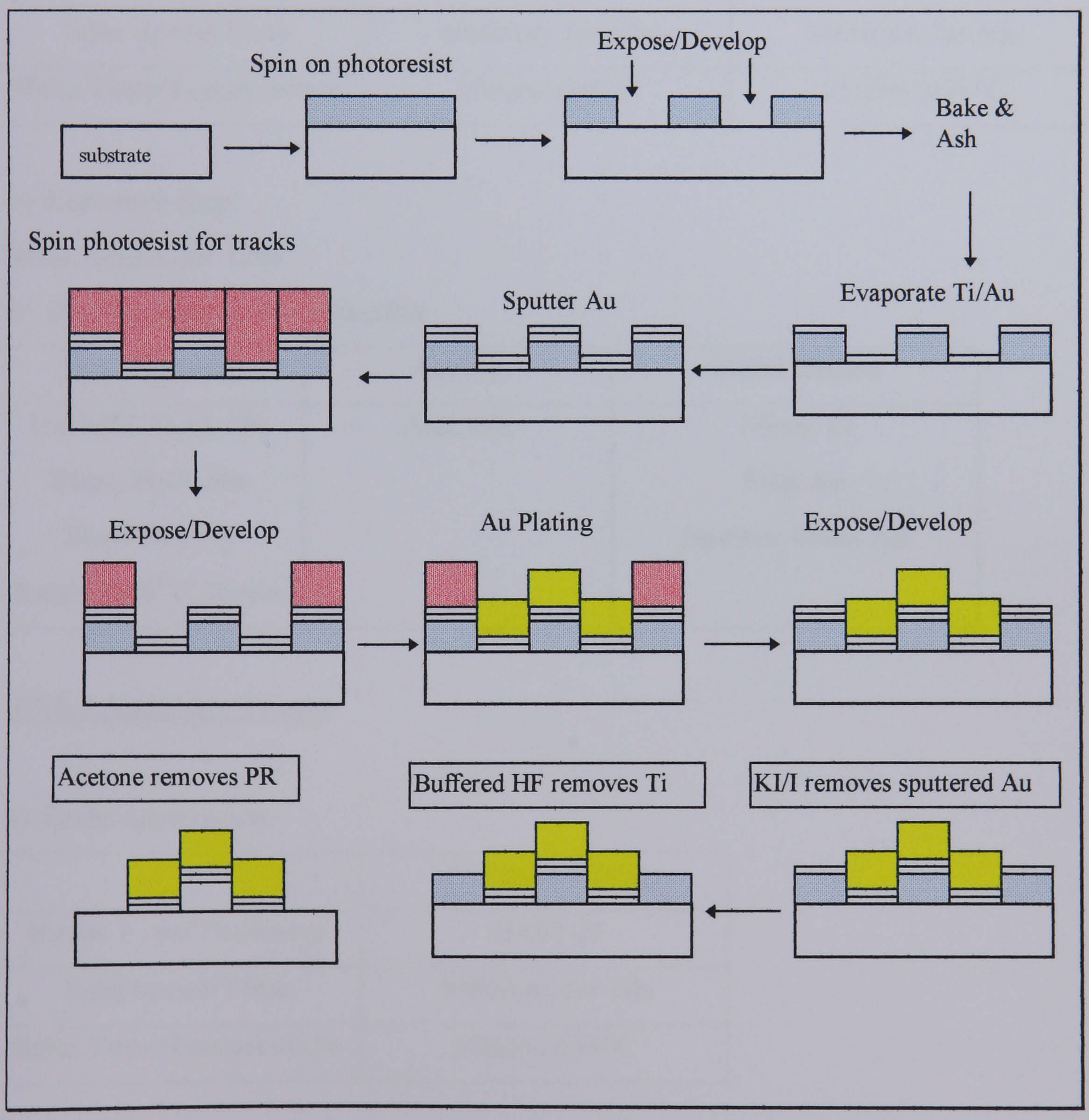


Figure 76 Airbridge process

The fabrication process itself was quite complex and it was necessary to complete all processing within two days to ensure successful fabrication otherwise the photoresist lifetime will adversely affect the resist profile.

3.3.8.1 Airbridge Supports

Process Details:

a) ***Resist application***

	1st Layer Resist	2nd Layer Resist
Resist Type/Thickness	**S1400-37**	**S1400-37**
Spin Speed/Time	**4000rpm for 60s**	**4000rpm for 60s**
Bake Time/Temperature	**15mins@90°C**	**15mins@90°C**

b) ***Exposure Step***

Mask aligner for 120s

c) ***Development & Metallisation***

Development	Ashing	Metallisation
1:4 S351:H_2O, 60s **Rinse H_2O, 30s** **Blow Dry N_2** **Bake@120°C,30min**	**Ash, 60s**	**50nm Ti** **5nm Au** **Sputter 40nm Au**

3.3.8.2 Airbridge Tracks

a) ***Resist application***

	1st Layer Resist
Resist Type/Thickness	**S1400-31**
Spin Speed/Time	**3000rpm for 60s**
Bake Time/Temperature	**15mins@90°C**

b) ***Exposure Step***

Mask aligner for 60s

c) *Development & Metallisation*

Development	Ashing	Metallisation
1:1 S1400-31 **dev:H_2O, 60s** **Rinse H_2O, 30s** **Blow Dry N_2**	**Ash, 60s**	**Plate 2μm Au**

d) Strip

Flood Expose	Development	Ashing	Etch
Mask aligner, 30s	**1:1 S1400-31** **dev:H_2O, 60s** **Rinse H_2O, 30s** **Blow Dry N_2**	**Ash, 60s**	**KI/I, 10s (Au etch)** **Buff. HF 10:1, 30s(Ti etch)** **Ash, 60s.** **Resist Strip: acetone@45^oC** **Rinse IPA** **Blow Dry N_2**

Process notes

Important points to note about this process were as follows:

1) It was necessary to spin two layers of resist at the support level in order to create airbridges of sufficient height to avoid shorting.

2) During the hardbake step of the support level, it was important to bake the sample for no longer than thirty minutes to ensure that the photoresist could be removed by acetone.

3) During the Buffered HF step of the airbridge track level, it was important to observe the endpoint when the Ti dissolved, and then to over etch for 5 seconds to ensure that there was no residue left on the substrate.

Shown below is a SEM micrograph of a completed airbridge.

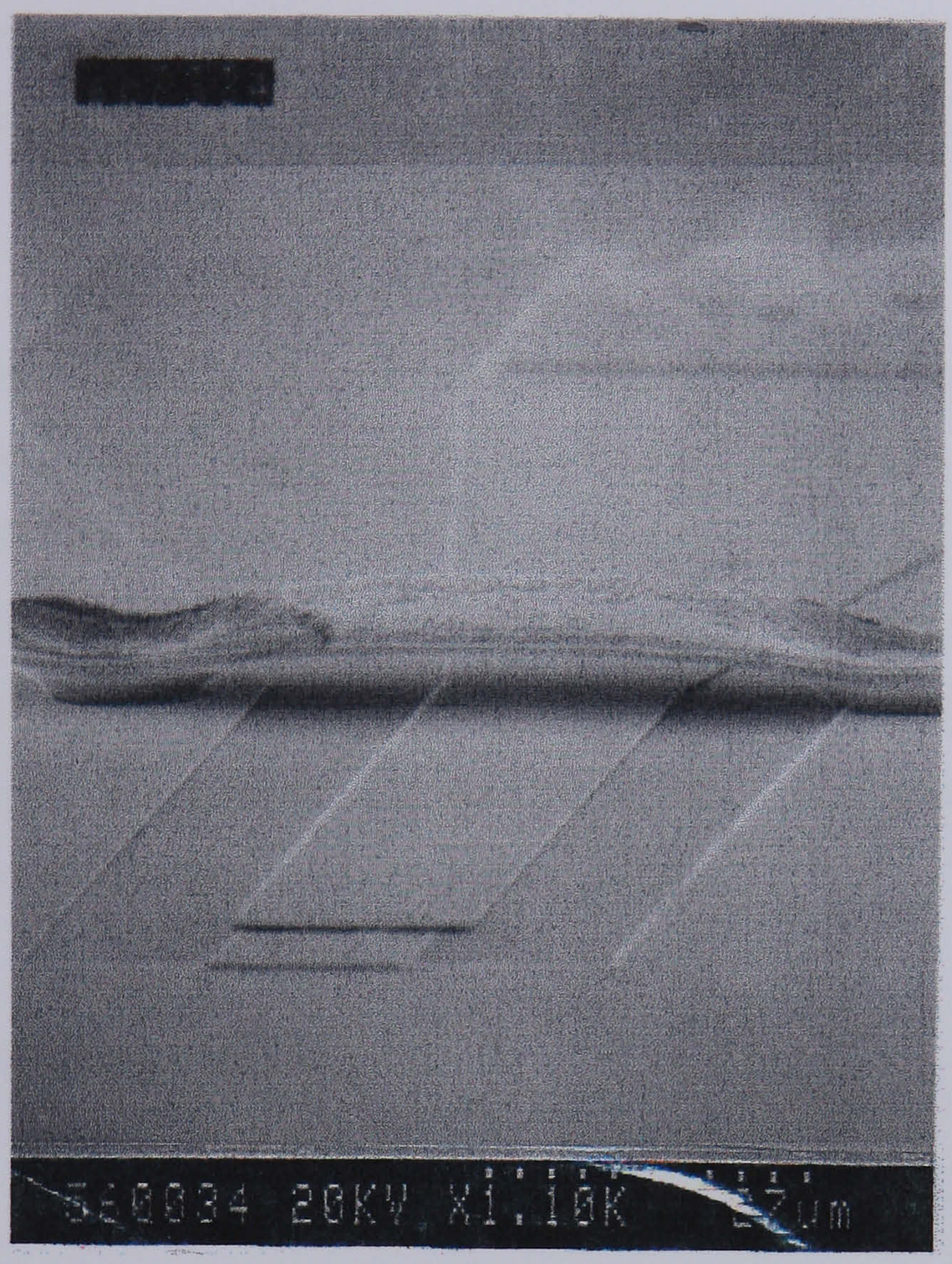


Figure 77 SEM micrograph of a completed airbridge

3.3.9 Fabrication of individual test structures

3.3.9.1 Strain Resistance TLM structures

Experiments were performed in order to determine the possible contribution of a strain resistance arising from the diode's anode fingers and the results of these are presented in Chapter 4. Listed here is the fabrication process for these test structures. This fabrication process was developed specifically for these experiments, using guidelines for lithography from Dr Steve Thoms at the University

of Glasgow and from the processing experience gained by the author during the course of the project.

These test structures consisted of three levels of electron beam lithography:

1) Alignment marks/Ohmic contacts
2) Electrical Isolation
3) Gate level

The ohmic contacts and markers were combined into one level to speed up fabrication. This is not normally done as annealed ohmics do not make good alignment marks for the LEICA EBPG5. For this reason the ohmic contacts were not annealed until after the isolation, leaving only one layer to be written using annealed ohmics as alignment marks. The processing for the gate level could undoubtedly be optimised. However, the first attempt gave reasonable mechanical yield and was sufficient in order to allow measurements to be performed.

3.3.9.2 Alignment marks / Ohmic contacts

Process Details:

a) ***Resist application***

	1st Layer Resist	**2nd Layer Resist**
Resist Type/Thickness	**12% BDH/ALD(600nm)**	**4% ELV(100nm)**
Spin Speed/Time	**5000rpm for 60s**	**5000rpm for 60s**
Bake Time/Temperature	**1 hour@180°C**	**2 hours@180°C**

b) ***Exposure Step***

Spot size	**160nm**
Resolution	**80nm**
Dose	**225μC/cm^2**
Beam Energy	**50kV**

c) *Development & Metallisation*

Development	Ashing, de-oxidation	Metallisation
1:1 IPA:MIBK, 30s **Rinse IPA, 30s** **Blow Dry N_2**	**Ash, 60s** **De-oxidise:** **4:1 H_2O/HCl, 30s** **Rinse IPA, 30s** **Blow Dry N_2**	**14nm Au** **14nm Ge** **14nm Au** **11nm Ni** **240nm Au** **Lift-off:** **Acetone(45^{O}C), 30mins** **Rinse IPA, 30s** **Blow Dry N_2**

3.3.9.3 Electrical Isolation

Process Details:

a) *Resist application*

	1st Layer Resist	2nd Layer Resist
Resist Type/Thickness	**12% BDH/ALD(600nm)**	**4% ELV(100nm)**
Spin Speed/Time	**5000rpm for 60s**	**5000rpm for 60s**
Bake Time/Temperature	**1 hour@180^{o}C**	**2 hours@180^{o}C**

b) *Exposure Step*

Spot size	**300nm**
Resolution	**150nm**
Dose	**220μC/cm^2**
Beam Energy	**50kV**

c) *Development & Isolation*

Development	Ashing, de-oxidation	Isolation&Resist Strip
1:1 IPA:MIBK, 30s **Rinse IPA, 30s** **Blow Dry N_2** **Bake 120^{O}C, 30mins**	**Ash, 60s** **De-oxidise:** **4:1 H_2O/HCl, 30s** **Rinse IPA, 30s** **Blow Dry N_2**	**Wet etch,10s steps:** **H_2O:H_2O_2:NH_3 - 200:1:1** **Resist Strip:** **Acetone(45^{O}C), 30mins** **Rinse IPA, 30s** **Blow Dry N_2**

To reduce ohmic contact resistance the wafer was then annealed using a **Jipelec** rapid thermal annealer(RTA). The annealing recipe used was:

10s ramp in N_2, 20s @ 310C, 10s ramp in N_2, 60s @ 360C, 10s ramp in N_2.

3.3.9.4 Gate Level

Process Details:

a) *Resist application*

	1st Layer Resist	2nd Layer Resist
Resist Type/Thickness	**4% ALD(100nm)**	**4% ELV(100nm)**
Spin Speed/Time	**5000rpm for 60s**	**5000rpm for 60s**
Bake Time/Temperature	**1 hour@180^{o}C**	**2 hours@180^{o}C**

b) *Exposure Step*

Spot size	**10nm**
Resolution	**20nm**
Dose	**300μC/cm^2**
Beam Energy	**50kV**

c) *Development & Metallisation*

Development	De-oxidation, Dry etching	Metallisation
3:1 IPA:MIBK, 30s **Rinse IPA, 30s** **Blow Dry N_2**	**De-oxidise:** **4:1 H_2O/HCl, 30s** **Rinse IPA, 30s** **Blow Dry N_2** **Gas Flows:** **$SiCl_4$:1.2sccm** **SF_4:8.2sccm** **O_2:0.1sccm** **Pressure:145mT** **RF power:17W** **Time:105s**	**Ti/Pd/Au** **Lift-off:** **Acetone(45^{O}C), 30mins** **Rinse IPA, 30s** **Blow Dry N_2**

Whilst the ohmic and isolation steps were identical to the mmWIC fabrication process, the gate level had to be developed for the fabrication of these superlattice structures. The fundamental changes made were as follows:

a) A bi-layer resist process was used. This combination of resists gave a total resist thickness of 200nm, which was sufficient for the thin metallisations used.

b) The dose used was 300μC/cm^2. This was chosen, after exposure tests, to completely develop out the superlattice gates, although the larger probe pads connecting these gates together were not developed out fully. Therefore the probe pads did not lift-off properly. The solution to this would be to give these pads a different dose.

c) The dry etch process to recess the gates used a fixed etch time of 105s. This time had to be carefully controlled to prevent adjacent recess areas connecting together.

Shown below are the profiles of the superlattice gate structure before and after etching.

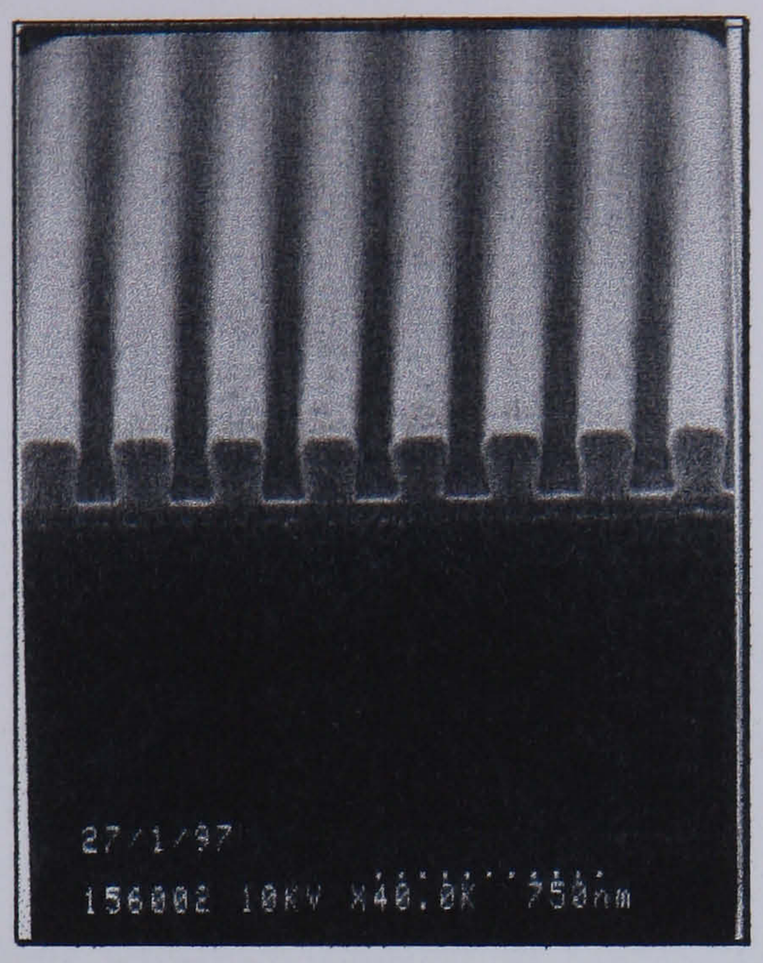


Figure 78 Superlattice gate profile before etching

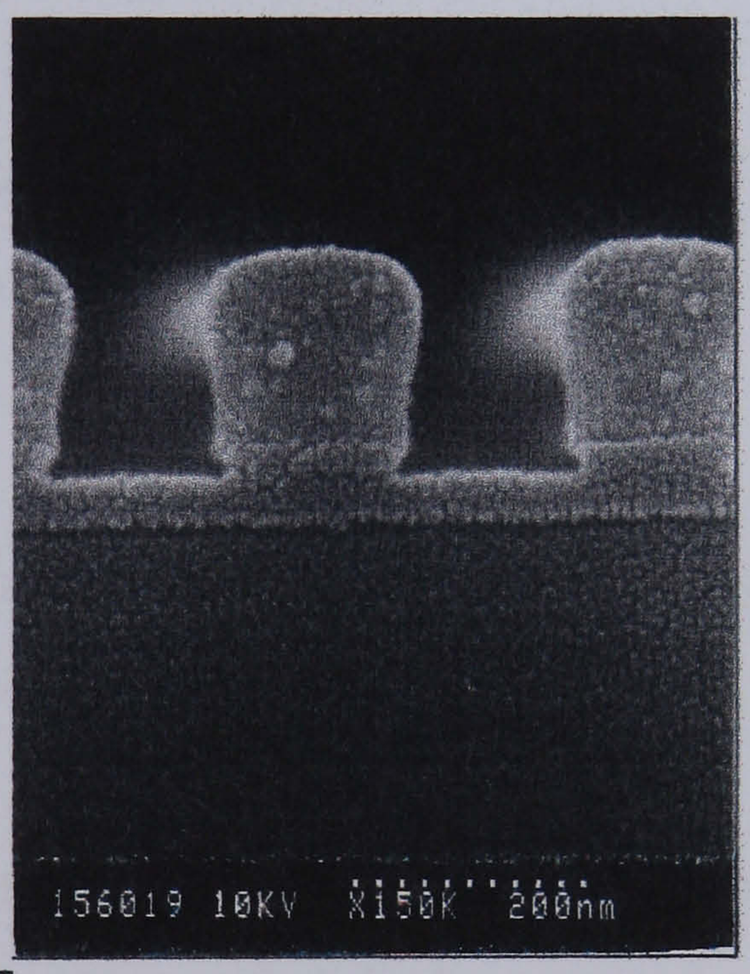


Figure 79 Etched profile of a superlattice gate

Chapter 3 References

[3.1] S.M. Sze : "Semiconductor Devices - Physics and Technology" (J. Wiley & Sons, New York, 1985), Chapter 11.

[3.2] S.Thoms, Internal training document, University of Glasgow, 1994.

[3.3] W.Patrick: " The fabrication of very short gate-length GaAs Field Effect Transistor Devices", PhD thesis, University of Glasgow, 1985.

[3.4] D.C. Look: "Electrical Characterisation of GaAs materials and Devices", (J. Wiley & Sons, Chichester, 1989), Chapters 1 & 2.

[3.5] P.A. Verlangieri, M. Kuznetsov, M.V. Schneider :"Low resistance ohmic contacts for microwave and light wave devices" - IEEE Microwave and Guided Wave Letters, Vol.1, No.3, pp51-53, 1991

[3.6] Y. Kwon, D. Pavlidis, M. Tutt, G.I. Ng, T. Brock: "W-Band monolithic mixer using InAlAs/InGaAs HEMT", GaAs IC symposium, 1990, pages 181-185

[3.7] W.L. Chen :"Ohmic contact study for quantum effect transistors and heterojunction bipolar transistors with InGaAs contact layers", Journal of Vaccum Science and Technology, pp 2354-2360., Nov-Dec 1992

[3.8] N.I. Cameron, M.R.S. Taylor, H. McLelland, M. Holland, I.G. Thayne, K. Elgaid, S.P. Beaumont : "A High Performance, High Yield, Dry-etched, Pseudomorphic, HEMT for W-Band use", IEEE MTT-S Digest, 1995.

[3.9] M. Ogawa, "Alloying behaviour of Ni/AuGe films on GaAs", Journal of Applied Physics 51, 1980, pages 406-412.

Chapter 4

Results

4.1 Introduction

This chapter presents all the results of the testing of the 94GHz mmWIC mixer circuit, along with the testing of individual components. .Comparison is made between the measured and predicted results.

4.2 Diode measurements

4.2.1 Introduction

In general, the Schottky diode can be characterised by its built-in potential ϕ_{bi}, the zero-voltage junction capacitance C_{jo}, ideality parameter η, current parameter I_o and the series resistance R_s. It was decided to measure the two most important parameters in terms of conversion loss, C_{jo} and R_s, by designing a suitable test structure and then extracting an equivalent circuit model using s-parameter measurements. This was done because it is the RF performance of these diodes that will affect mixer conversion loss. DC I/V characteristics nevertheless are useful to determine η and I_o which give some indication of diode quality.

4.2.2 S-parameter measurements

S-parameters [4.1,4.2] are reflection and transmission coefficients. Transmission coefficients are commonly called gains or attenuations, while reflection coefficients are directly related to VSWR's and impedances. Figure 80 shows the basic idea.

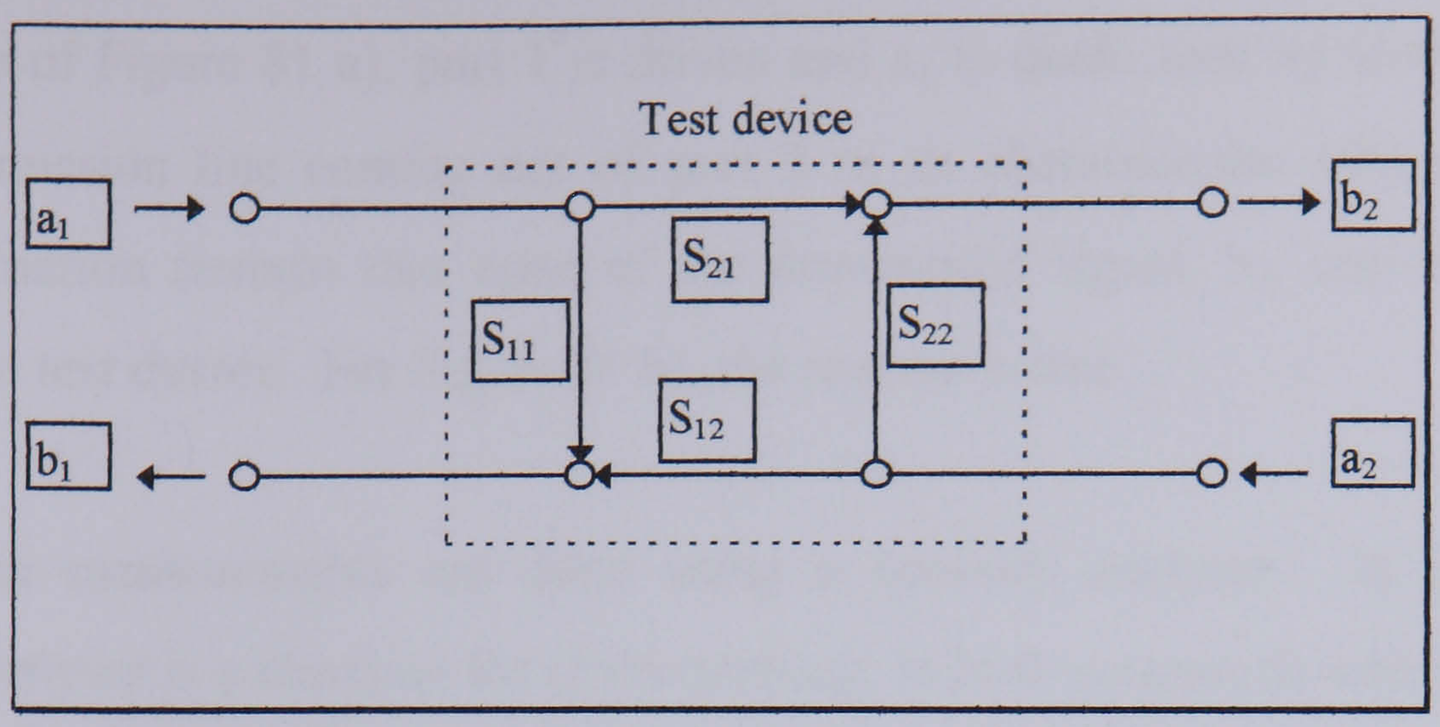


Figure 80 S-parameters

In Figure 80, "a" and "b" are the incident and reflection parameters, respectively. A signal a_1 is partially reflected at port 1 and the rest of the signal is transmitted through the device and out of port 2. The fraction of a_1 that is reflected at port 1 is S_{11} and the fraction of a_1 that is transmitted is S_{21}. Similarly, the fraction of a_2 that is reflected at port 2 is S_{22} and the fraction S_{12} is transmitted. The signal b_1 leaving port 1 is the fraction of a_1 that was reflected at port 1 and the fraction of a_2 that was transmitted from port 2. This gives the equations:

$$b_1 = s_{11}a_1 + s_{12}a_2$$
$$b_2 = s_{21}a_1 + s_{22}a_2$$

When a_2=0 then $s_{11} = \frac{b_1}{a_1}$ and $s_{21} = \frac{b_2}{a_1}$ and when a_1=0 then $s_{12} = \frac{b_1}{a_2}$ and $s_{22} = \frac{b_2}{a_2}$

Figure 79 below shows the setup for measuring s-parameters.

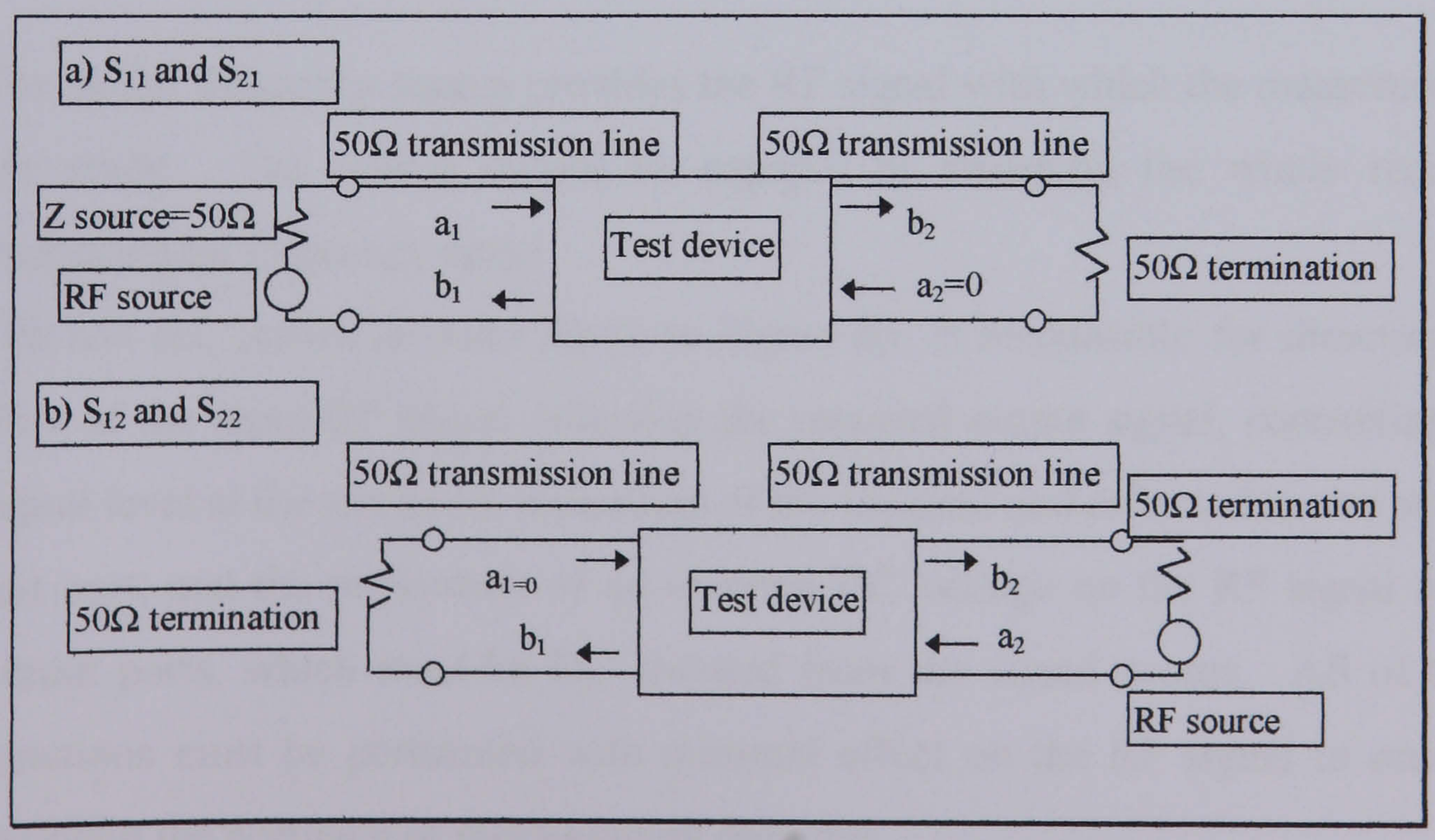


Figure 81 Measurement of s-parameters

In the case of Figure 81 a), port 1 is driven and a_2 is made zero by terminating the 50Ω transmission line coming out of port 2 in its characteristic 50Ω impedance. This termination ensures that none of the transmitted signal, b_2, will be reflected towards the test device. For Figure 81 b), the reverse is true.

S-parameter measurements are done using a network analyser. In principle, a network analyser is a machine for characterising, in both magnitude and phase, an n-port network, usually a two-port network. Figure 82 shows the main elements of a typical network analyser.

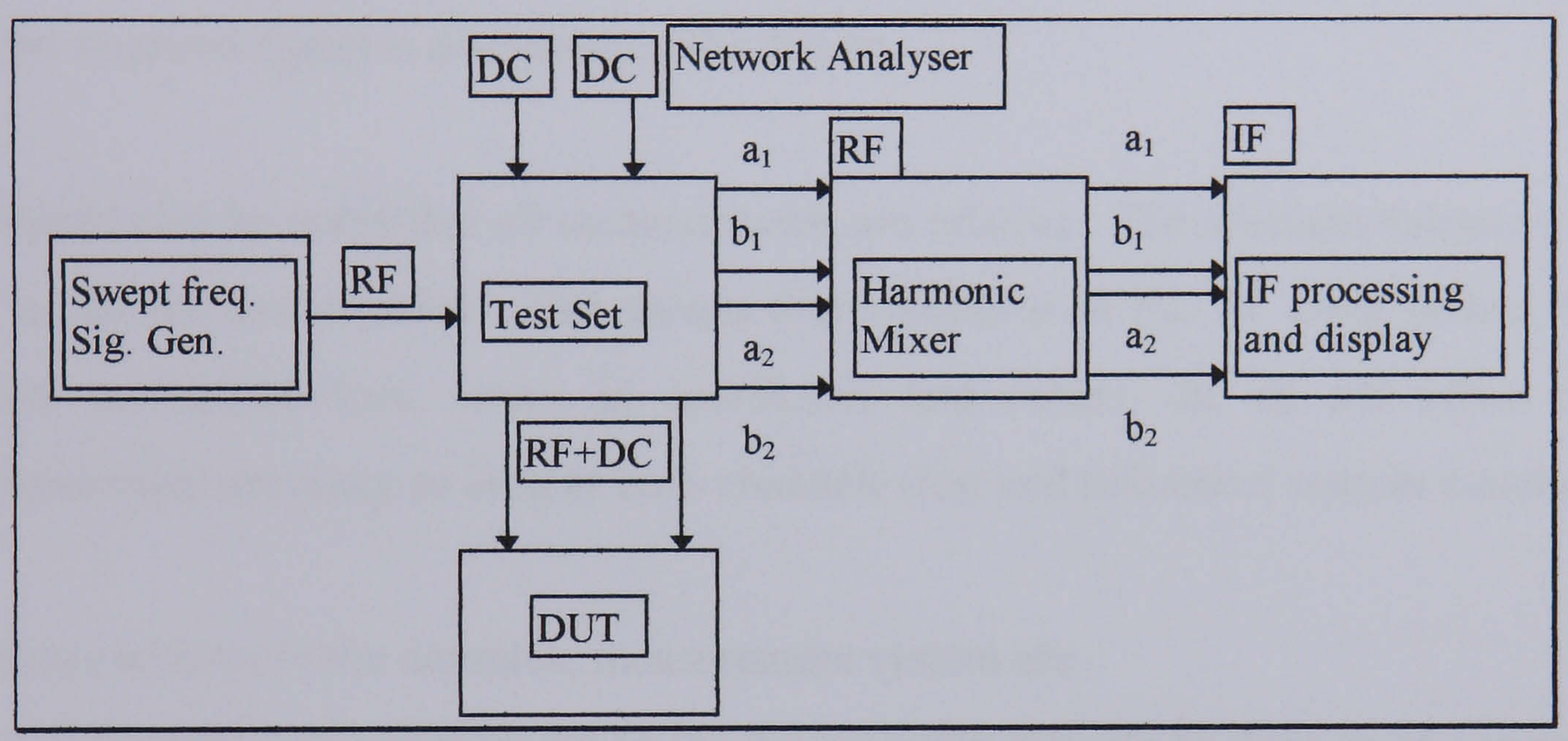


Figure 82 Network Analyser

The functions of each part of the analyser are outlined below:

1) The swept frequency source provides the RF signal with which the measurements are made. The source should be capable of sweeping the whole required measurement frequency range.
2) The test set, shown in more detail in Figure 83, is responsible for directing the flow of the input RF signal, selecting the required output signal, controlling the signal level at the test ports, separation of the incident and reflected waves at each test port, and the imposition of an external DC voltage on the RF signal at the output ports, which must be DC isolated from the signal source. All of these functions must be performed with minimal effect on the RF signal in order to maintain the accuracy of measurement required.

3) The chosen reference and test signals are then mixed down to the IF frequency in the harmonic mixer. The mixers are double-balanced in order to accurately maintain the magnitude and phase ratios of the two signals.
4) The IF section performs the division test ÷ reference and amplifies the signal before display. On older machines the IF section contains variable phase shifters and amplifiers to allow calibration of the system. Newer models use ADCs to convert the signal into a number, and extensive processing of this signal can then be performed in software, including error correction, reference plane movement, comparative measurements, Fourier transformation into the time domain. Lastly, the required signal is displayed on the screen.

It should also be noted that all measurements are relative. The absolute values of a_1, b_1, a_2, b_2 are not required. This means that variations of the RF input power, the mixer conversion loss, losses in connectors and cables, etc do not affect the measurement accuracy so long as both channels (test and reference) remain matched.

Sources of error in the complete measurement system are:

a) Placement of wafer probes to the device under test can be done to an accuracy of only a few microns at best. This introduces errors in the s-parameter measurements due to loss of accurate magnitude and phase information.
b) Losses in the cables connecting the network analyser to wafer probes.
c) Losses in the wafer probes.
d) There may be some loss of signal due to S_{11} & S_{22}(a small fraction of power may not be transmitted to the device under test but instead will be reflected).
e) At mm-wave frequencies the signal flow is concentrated in the surface layer of the conductor. The current density is maximum at the surface of the conductor and decreases exponentially with depth into the conductor. The penetration of the current flow is defined by the skin depth, δ, which is the thickness of the layer of the conductor at which the current density has fallen to 1/e of its surface value. So some loss will be incurred due to the finite metallisation thickness.

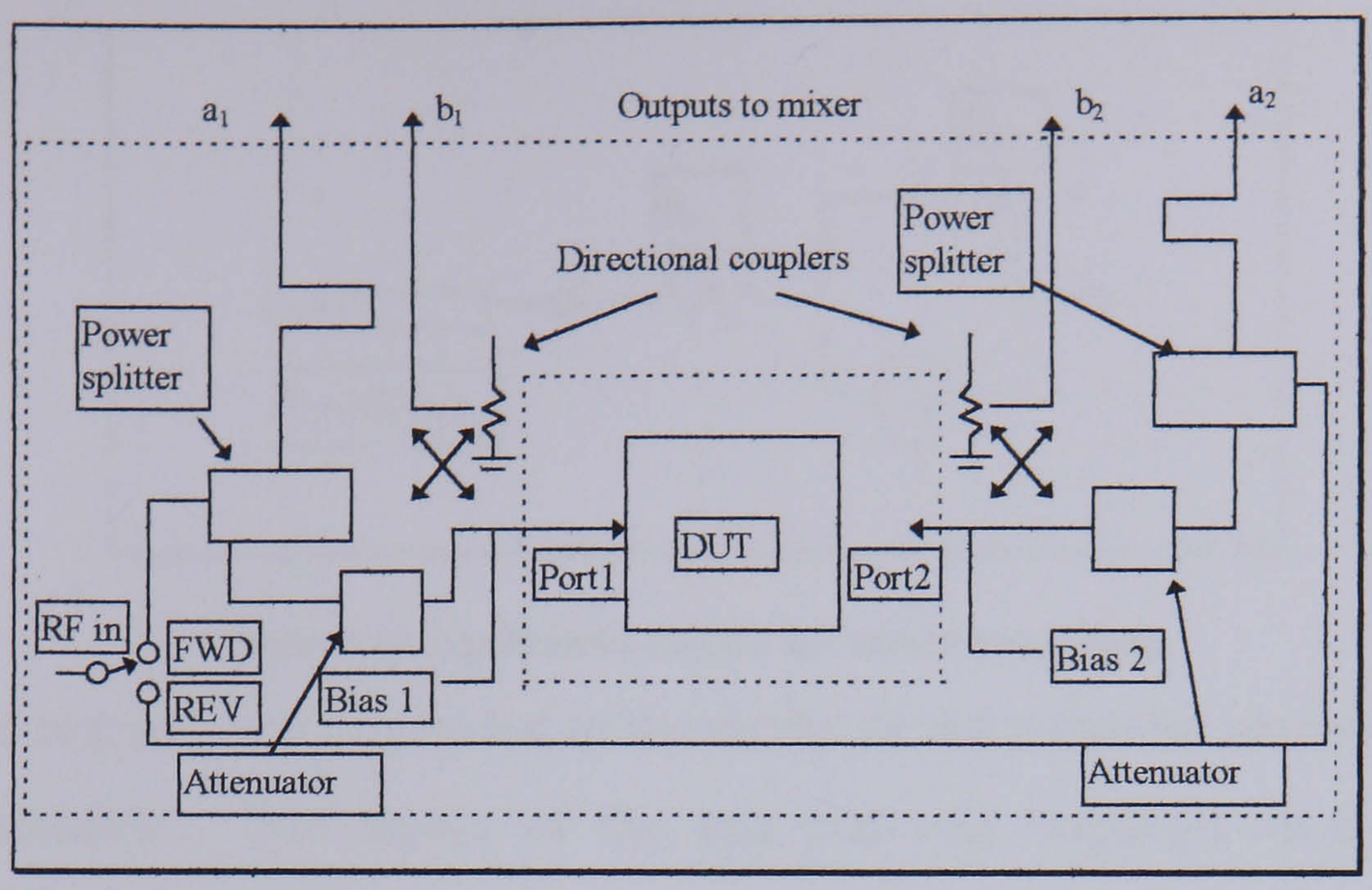


Figure 83 S-parameter test set

4.2.3 Diode test structure

To enable diodes to be fully characterised at both DC and RF frequencies, the test fixture shown below was used. It basically consists of three probe pads (which are compatible with CPW probes for on-wafer testing), which are tapered down to the standard CPW dimensions, followed by a length of transmission line with the diode placed at the end of the length of line which is then shorted. This allows the s-parameter measurement of S11, from which an equivalent diode circuit model can be extracted.

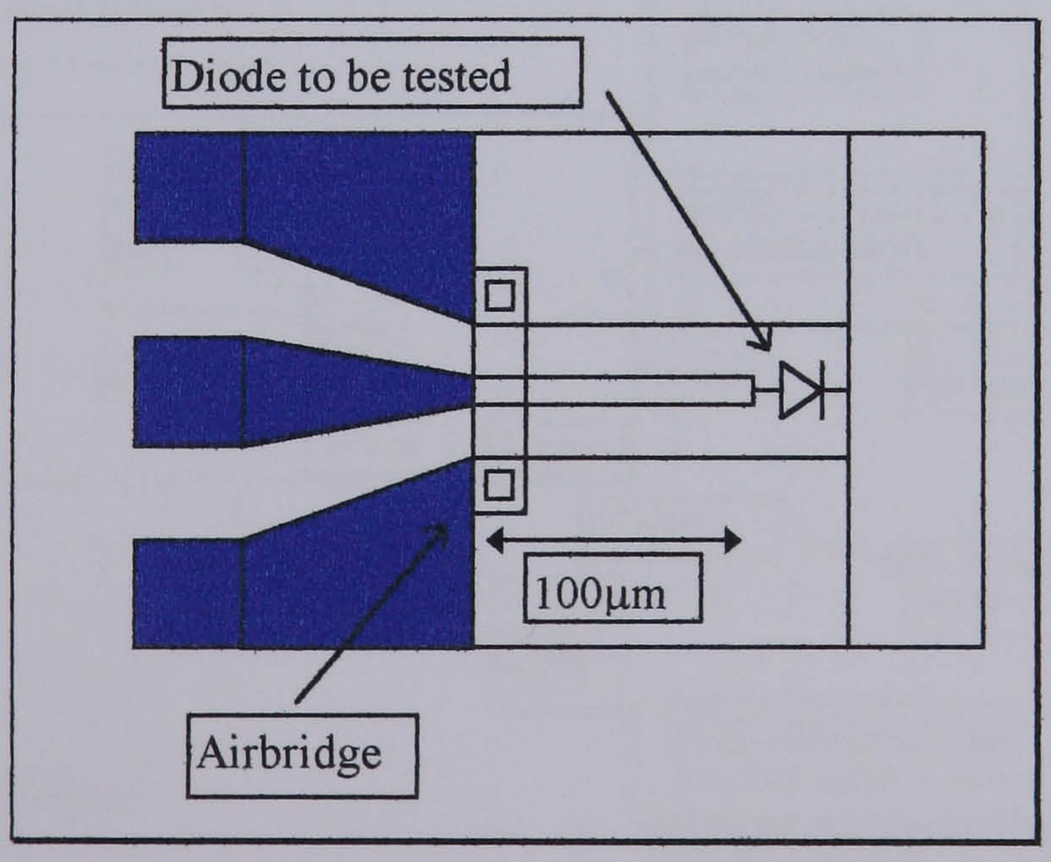


Figure 84 Diode test fixture

The equivalent circuit model for the test fixture shown in Figure 84 is shown overleaf.

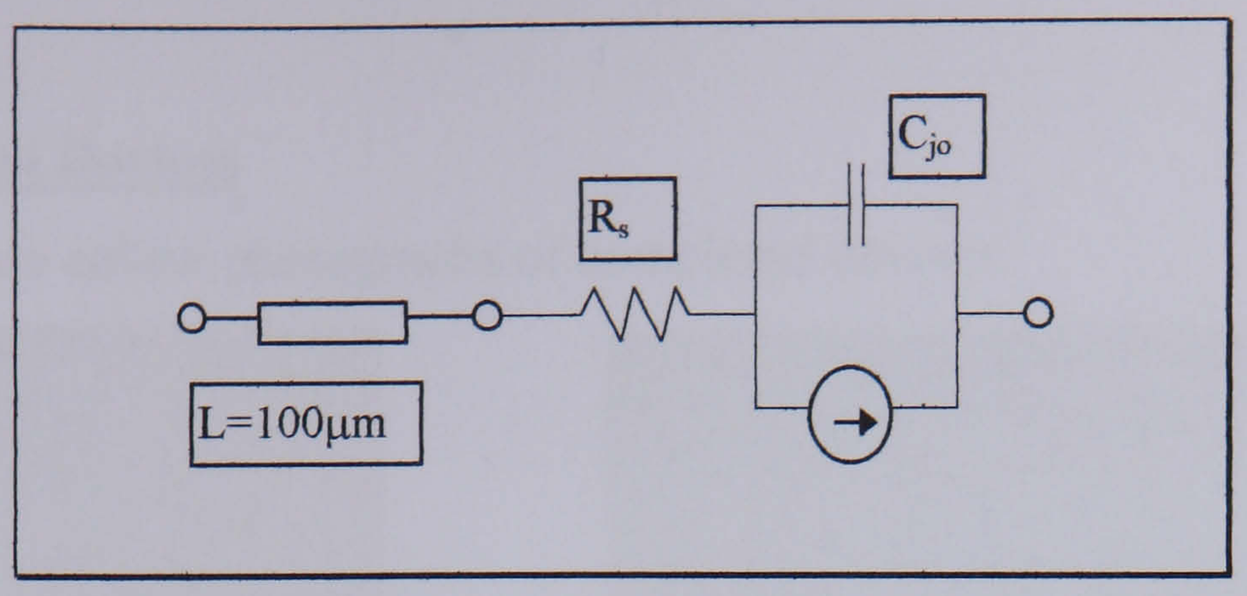


Figure 85 Equivalent circuit for diode modelling

The tapered test pad is not included in the model as the reference planes are defined during calibration. The layout of the test pad was originally designed at the University of Glasgow by J.Adams [4.4]. Measurements on diodes were done using the Wiltron 360B network analyser, and diodes were measured from 67-110GHz. Before use, the network analyser was calibrated using the LRL (line-reflect-line) calibration technique. This was chosen ahead of the more commonly used SOLT (short-open-load-through) because of the difficulty in fabricating reliable 50Ω loads. The calibration components for SOLT are a short circuit, an open circuit, an accurate 50Ω resistor and a short length of CPW. The LRL technique involves the measurement of two through lines (100 and 500 μmlong) and a short circuit [4.5].

A schematic of the test and measurement set-up is given below.

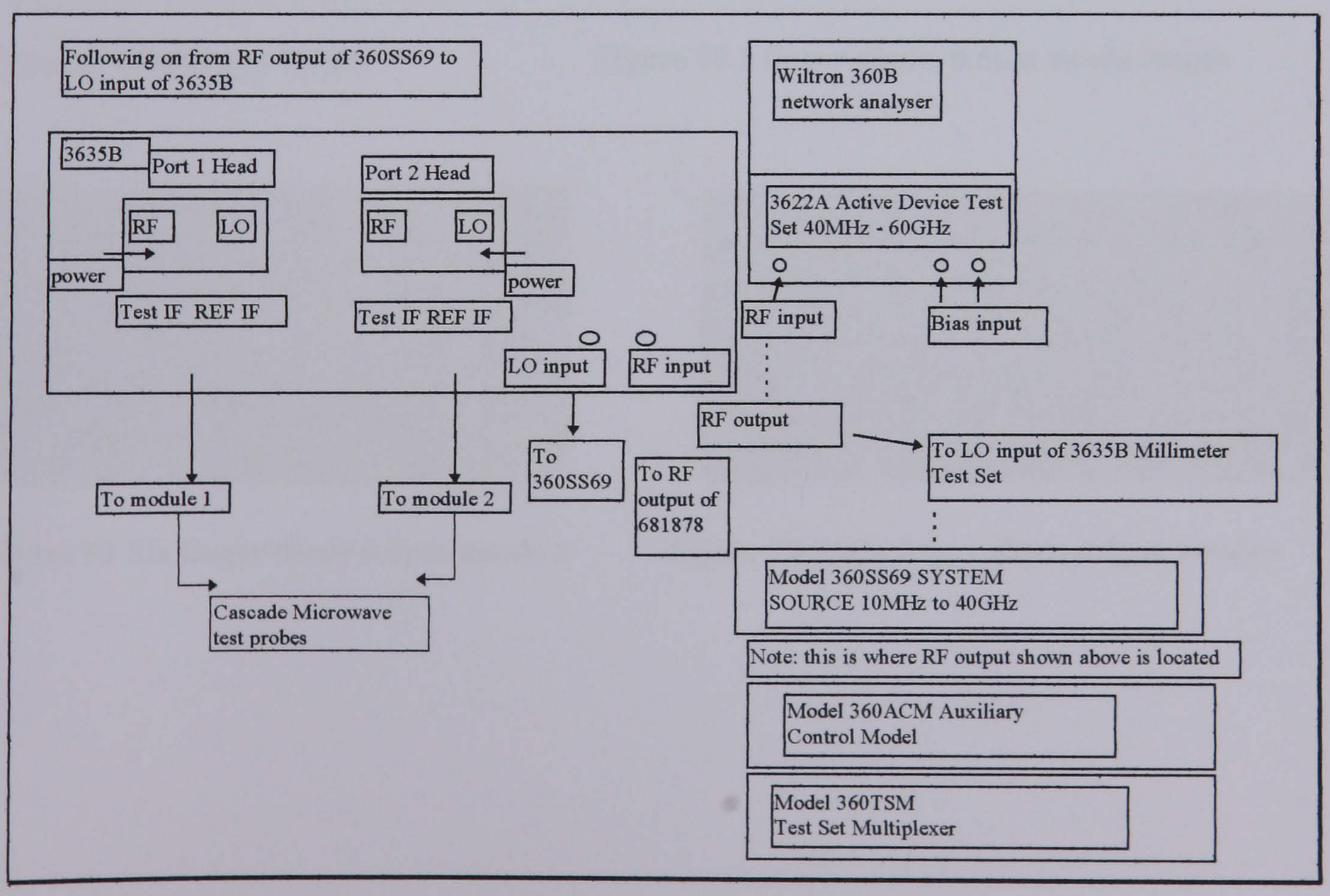


Figure 86 W-Band test and measurement set-up

4.2.4 Completed Devices

Shown below are colour photographs of completed devices:

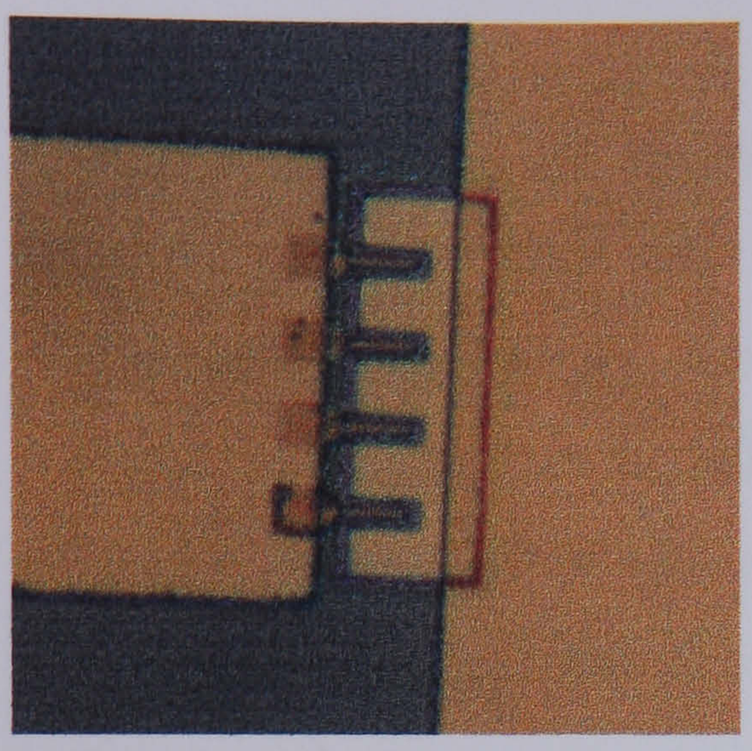


Figure 87 4 finger diode, 0.2μm anode length

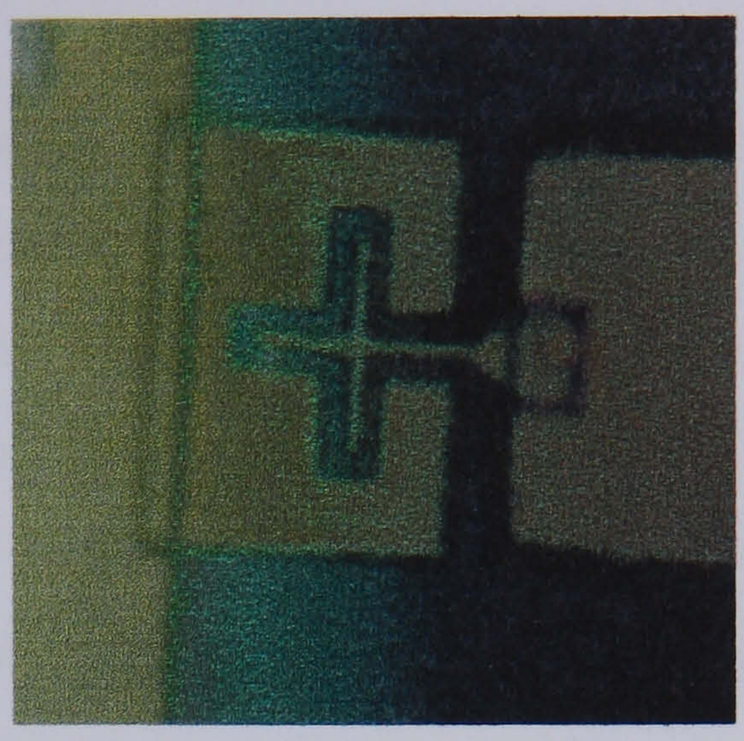


Figure 88 T-shaped anode

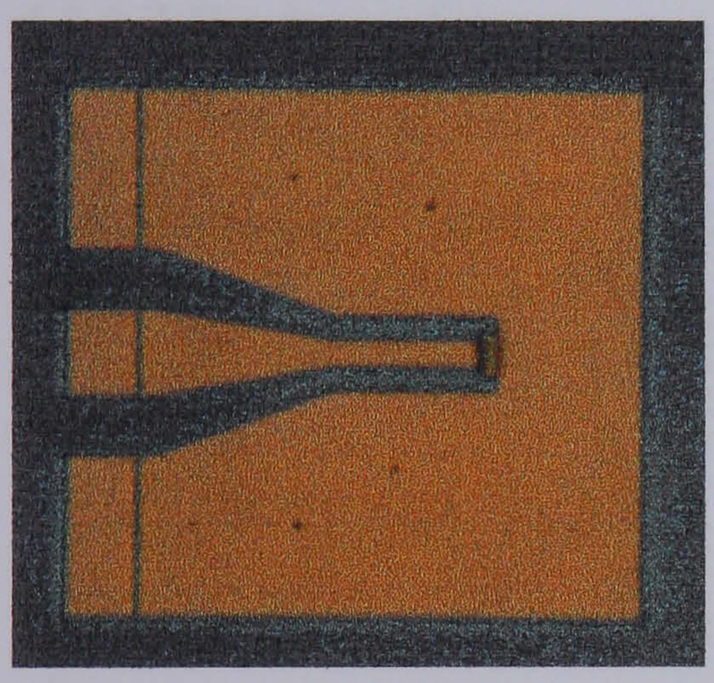


Figure 89 Diode test fixture

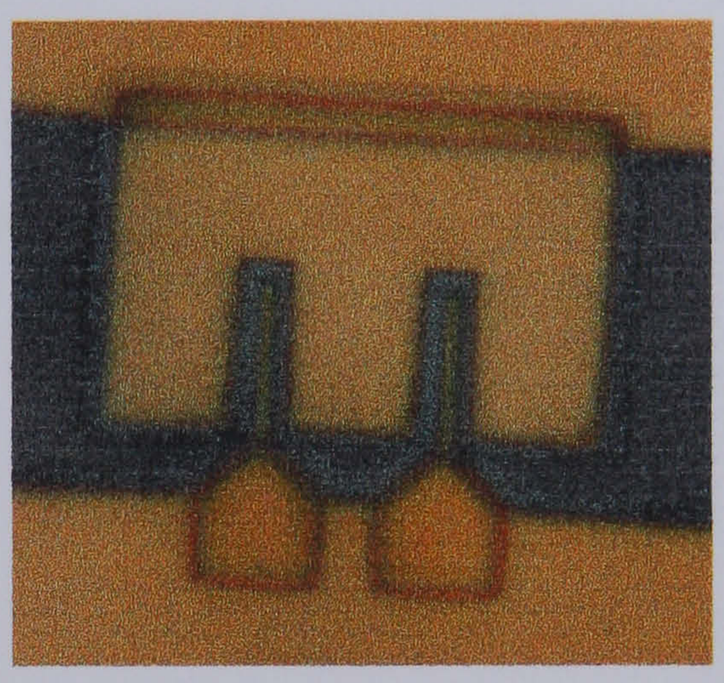


Figure 90 2 finger diode, 0.5μm anode length

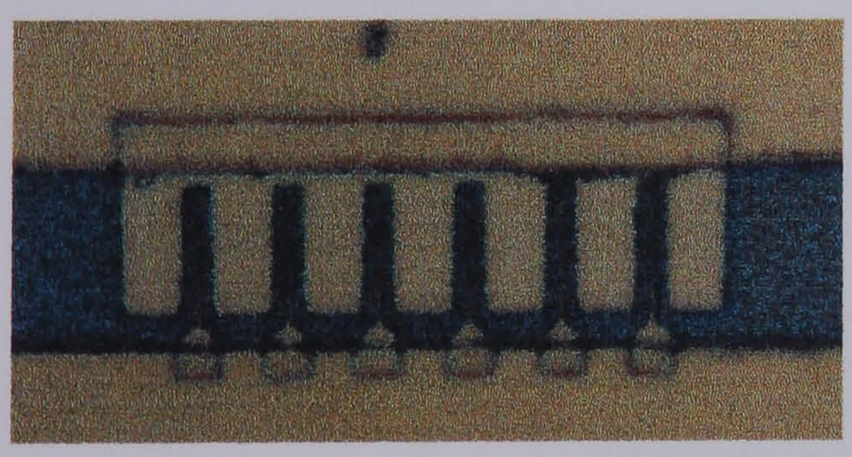


Figure 91 Six finger diode 0.5μm anode l.

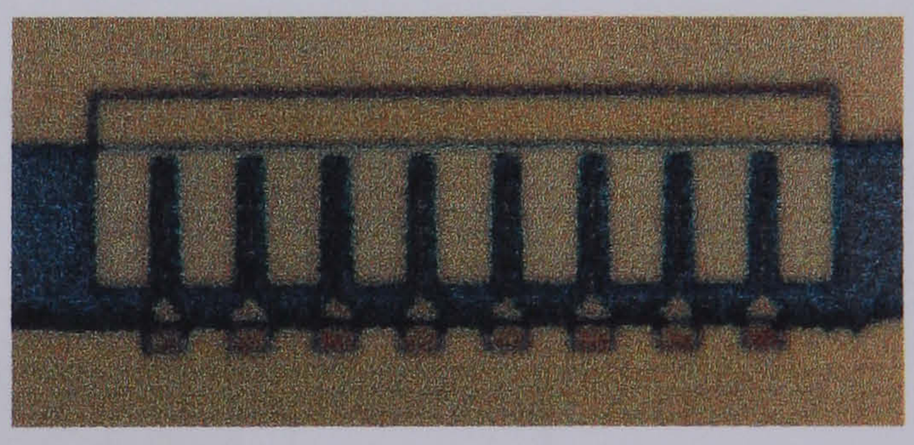


Figure 92 Eight finger diode 0.5μm anode l

4.2.5 Diode Equivalent Circuit models from S-parameter measurements

4.2.5.1 Introduction

A very large number of diodes were fabricated on several different pHEMT and MESFET layers. After the s-parameter measurement of diode test fixtures, equivalent circuit models were extracted using **Touchstone**, a linear software package for microwave modelling. This involved creating an equivalent circuit model identical to that in Figure 85, and then varying the values of C_{jo} and R_s (so as to in effect vary S_{11}) until measured and predicted values of S_{11} were equal. The junction conductance was modelled as a very large resistance (1GΩ).

4.2.5.2 Diode models

The following nomenclature is used when describing diode dimensions:

AxBxCxD:

A - number of diode fingers

B- Anode width

C- Anode length

D- Anode-Cathode separation

These are shown below in Figure 93. B,C and D are given in microns.

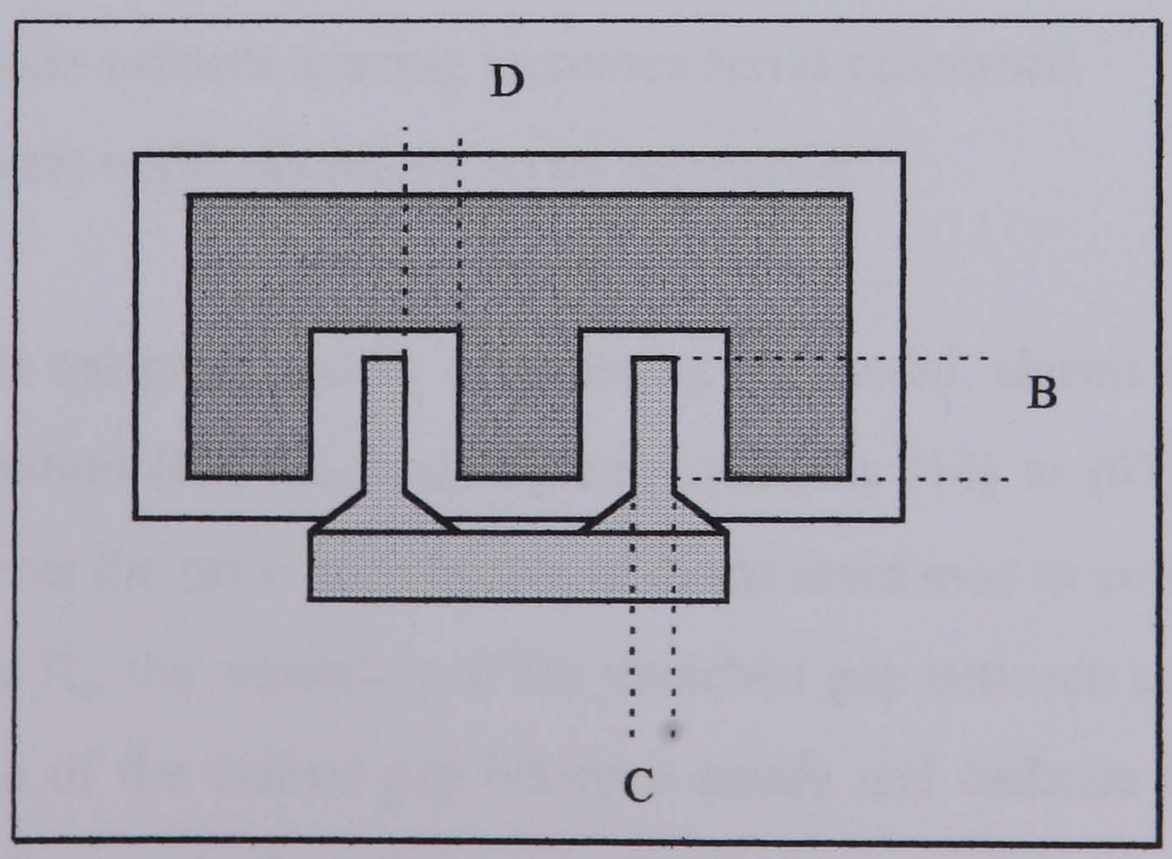


Figure 93 Diode dimensions

Diode characterisation was done at RF frequencies (67-110GHz). The important parameters to determine are series resistance and junction capacitance. The results of RF testing are now given, firstly illustrating how diode series resistance varies with different diode layout (with comparison of measured versus predicted values) and, secondly, how junction capacitance compares with predicted values.

Varying anode width and anode-cathode spacing

The graph shown below illustrates the effect of varying the anode-cathode spacing and anode width. The diodes were fabricated on GaAs pHEMT and the anodes were recessed by dry etching.

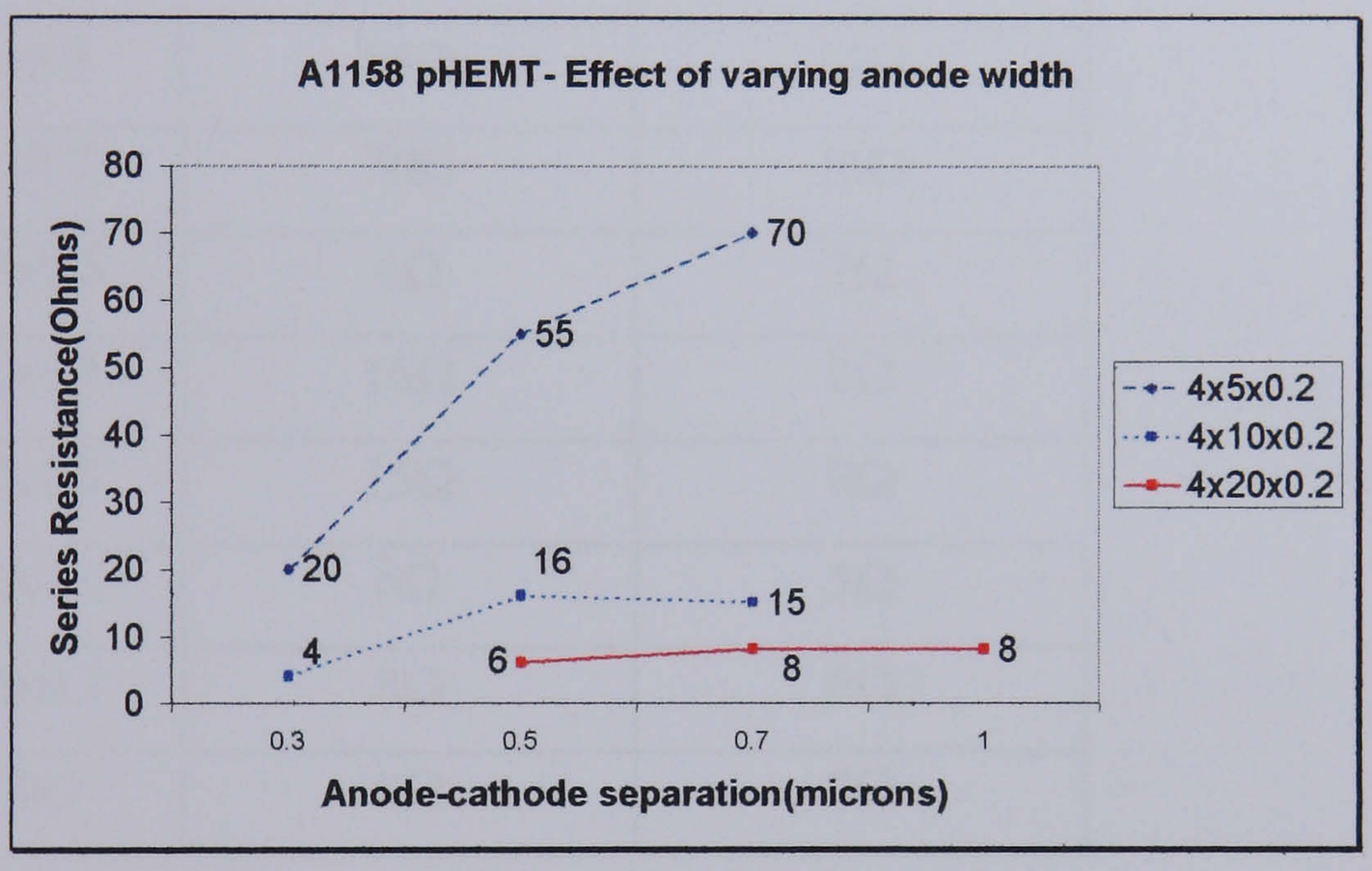


Figure 94 Diodes on A1158

Therefore:

1) Increasing anode-cathode spacing increases series resistance.
2) Increasing anode width decreases series resistance.

Both these results are predicted by considering the model, shown in Figure 30, and expressed in equation **(63)** (and subsequent equations **(64)** to **(67)**) of Chapter 2. This model presents the principal sources of diode resistance as consisting of: ohmic contact resistance R_c, the resistance of the unetched gap between anode and cathode R_g, the resistance of the etched gap between anode and cathode R_r, the spreading resistance under the anode R_s and the metallic resistance of the anode R_m. Each of

these contributions to series resistance can be seen (from equations **(64)-(67)**)to be inversely proportional to anode width. Therefore, increasing anode width decreases series resistance. Also, increasing the length of the unetched material between anode and cathode will increase the contribution of R_g thus increasing the overall value of series resistance.

Shown below is a table of measured versus predicted results (using the equation **(63)**).

Table 4.1 Measured and predicted values of R_s

Diode	Measured	Predicted
4x5x0.2x0.3	20Ω	12Ω
4x5x0.2x0.5	55Ω	14Ω
4x5x0.2x0.7	70Ω	16Ω
4x10x0.2x0.3	4Ω	7Ω
4x10x0.2x0.5	16Ω	8Ω
4x10x0.2x0.7	15Ω	9Ω
4x20x0.2x0.5	6Ω	5Ω
4x20x0.2x0.7	8Ω	6Ω
4x20x0.2x1	8Ω	7Ω

From Table 4.1, in general the values of measured resistance are different from the predicted values using the model from Figure 30. This is almost certainly due to the 0.2μm "pyramidal" anode shape resulting in an intolerable metallic resistance. It is common for such short FET gate lengths to use a "T-gate" profile instead. The difference between measured and predicted values of resistance is worse for smaller anode widths as there is a lower limit to the junction area, beyond which edge effects, which are the result of having a small anode on a large semiconductor surface, cause the fringing electric field near the edge of the metal anode to be greater than the field in the centre. Therefore, current density is greatest at the edge of the junction and so series resistance depends strongly on junction periphery.

Varying the number of anode fingers

The graph below illustrates the effect of varying the number of anode fingers.

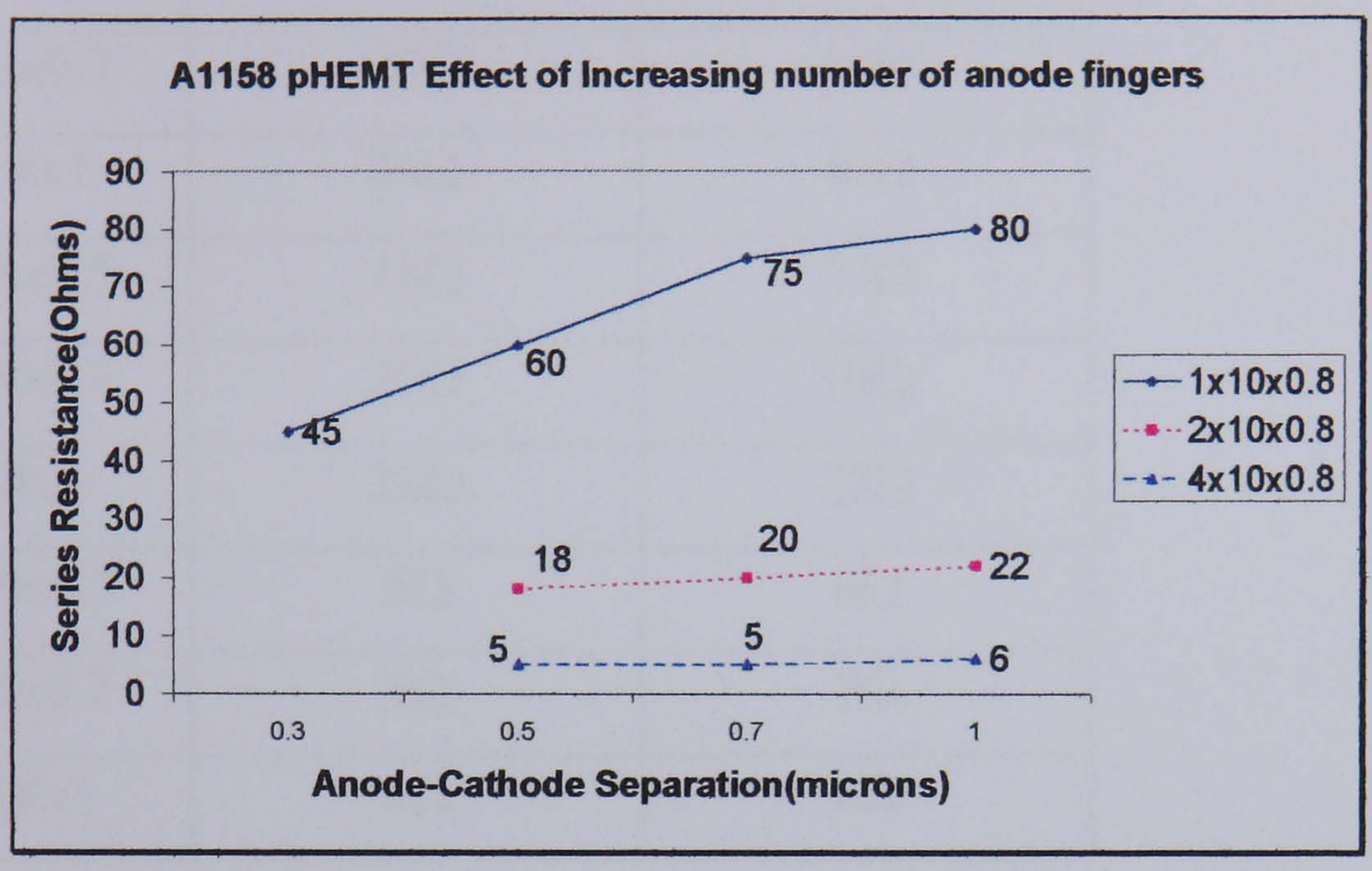


Figure 95 Diodes on A1158

From Figure 95:

1) Increasing the number of anode fingers, reduces the diode series resistance. This is predicted from the model in Figure 30. With the exception of metallic resistance, the contributions of resistance arising from the etched/unetched sections between the anode and cathode R_g and R_r respectively, the anode spreading resistance R_s and the contribution from the ohmic contacts R_c are all inversely proportional to the number of anode fingers. It should be noted, however, that this is because increasing the number of anode fingers increases the total anode width. Shown in table 4.2 are the measured against predicted results.

Table 4.2 Measured and predicted values of R_s

Diode	Measured	Predicted
1x10x0.8x0.3	45Ω	26Ω
1x10x0.8x0.5	60Ω	30Ω
1x10x0.8x0.7	75Ω	34Ω
1x10x0.8x1	80Ω	40Ω
2x10x0.8x0.5	18Ω	17Ω
2x10x0.8x0.7	20Ω	19Ω
2x10x0.8x1	22Ω	22Ω
4x10x0.8x0.5	5Ω	6Ω
4x10x0.8x0.7	5Ω	7Ω
4x10x0.8x1	6Ω	8Ω

The results for one finger diodes show no correlation between measured and predicted values of resistance. The results for both two and four finger diodes show good correlation. However, the diode shown in Figure 88 with the cross-shaped anode had a measured series resistance of 28Ω, significantly less than other 1 finger diodes. This indicates that increasing junction periphery relative to area reduces series resistance. For the one finger diodes, the effects of the surrounding semiconductor become more important and the resultant edge effects (discussed earlier on page 136) make it more difficult to predict accurately the diode resistance. The results for the two and four finger diodes indicate that the model for resistance from Figure 30 and equations **(64-67)** provides a good prediction of actual measured resistance.

Effect of varying anode length

Figure 96 shows the effect of varying the anode length on series resistance. It is evident that there is a large reduction in series resistance obtained by increasing anode length from 0.2μm to 0.5μm or 0.8μm. This is due to the large increase in metallic resistance caused by having such a short length of anode, and the fact that

the surrounding semiconductor surface has a greater impact on the short anode length devices. Modelling of diode resistance is again shown to be accurate for 0.5μm and 0.8μm anode lengths (using **(63-67)**) from Table 4.3.

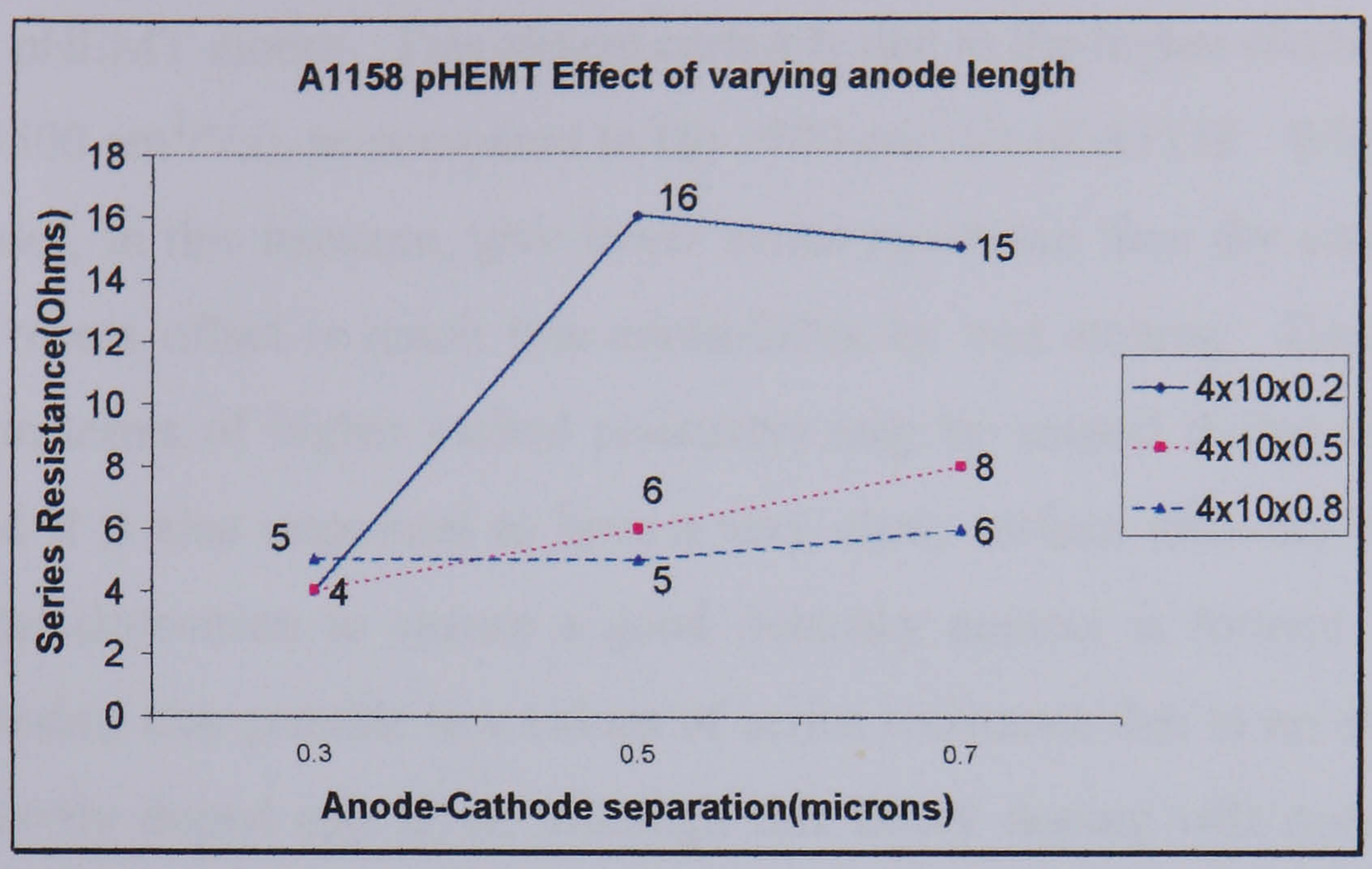


Figure 96 Diodes on A1158

Table 4.3 Measured and predicted values of R_s

Diode	Measured	Predicted
4x10x0.2x0.3	4Ω	7Ω
4x10x0.2x0.5	16Ω	8Ω
4x10x0.2x0.7	15Ω	9Ω
4x10x0.5x0.3	4Ω	5Ω
4x10x0.5x0.5	6Ω	6Ω
4x10x0.5x0.7	8Ω	7Ω
4x10x0.8x0.3	5Ω	5Ω
4x10x0.8x0.5	5Ω	6Ω
4x10x0.8x0.7	6Ω	7Ω

Effect of varying anode fabrication techniques

Figure 97 shows a comparison of series resistance for different anode fabrication techniques. This compares diodes formed on GaAs pHEMT layer A1159, whose anodes were dry etched, wet etched and unetched prior to Schottky metallisation. There is also a comparison with GaAs MESFET diodes formed on layer A966. It is

evident that for the diode dimensions chosen, the dry etched pHEMT results in larger series resistance than corresponding wet etch and non-recessed pHEMT diodes. Also, in this instance GaAs MESFET diodes give smaller values of resistance than dry-etched pHEMT diodes. This almost certainly due to the higher electron mobility of A966 (3500 cm^2/Vs), as compared to the 2500 cm^2/Vs of A1159. Whilst, the wet etched diodes, in this instance, give lower series resistance than dry etched diodes, the anode recess offset is much less controllable by wet etching. Damage to the substrate (in terms of higher etched resistivty) may be caused during the dry etch process and it is also important to have a very clean surface after dry etching and before metal deposition to ensure a good Schottky contact is formed. The non-recessed diodes, also provide low values of series resistance due to no anode recess and the heavily doped cap layer, although this heavy doping will result in much higher values for diode junction capacitance.

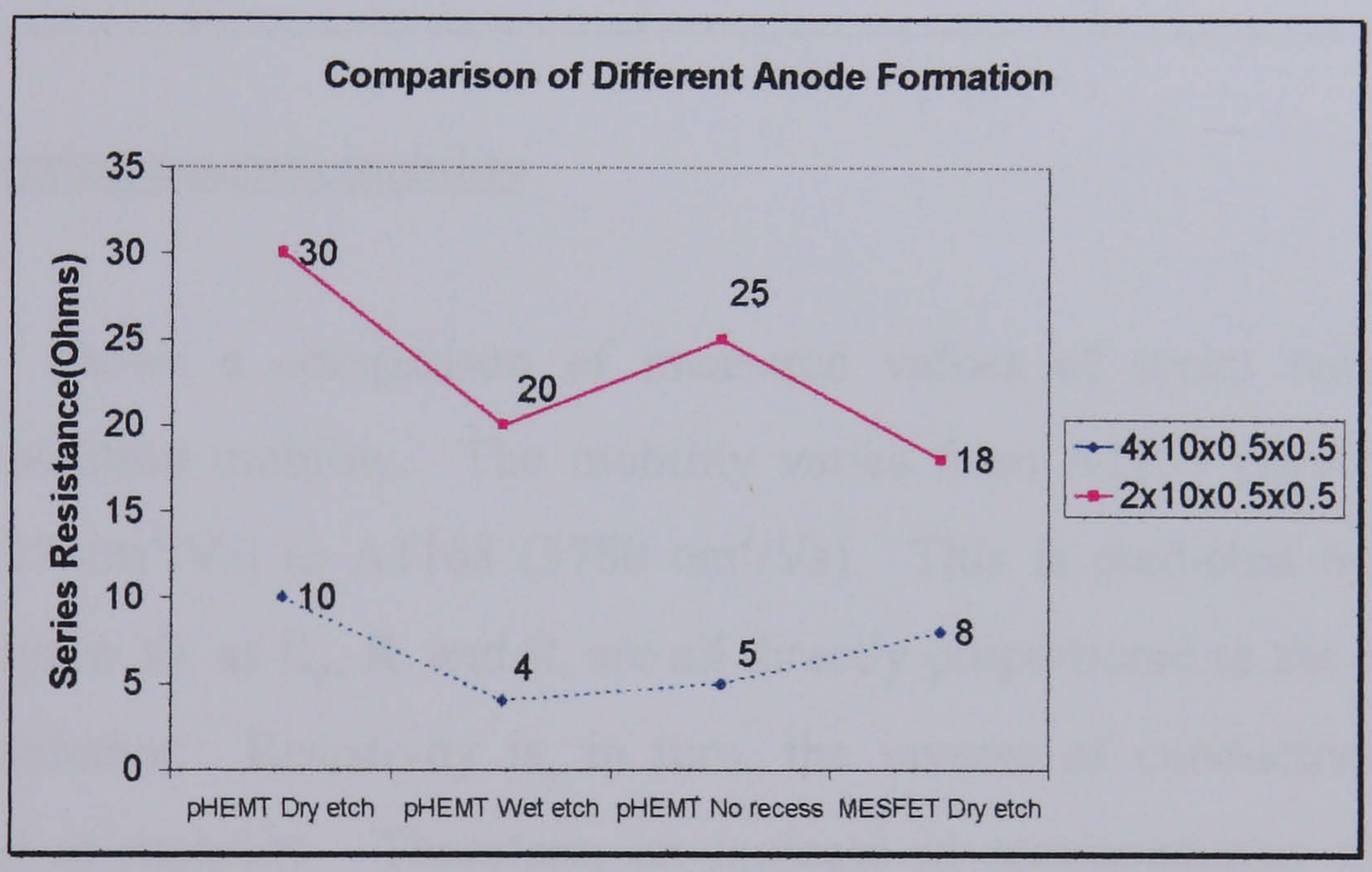


Figure 97 Diode series resistance for different anode formation

Conclusions on different anode fabrication techniques

Although in this instance, the dry etched recessed pHEMT diodes show larger values of resistance then both wet etch and non recessed diodes, it was decided to use them in the mmWIC mixer circuit to allow ultimate integration with LNAs.

Table 4.4 Measured and predicted values of R_s

Diode	Anode type	Measured	Predicted
2x10x0.5x0.5	MESFET,dry	18Ω	13Ω
4x10x0.5x0.5	MESFET,dry	8Ω	7Ω
2x10x0.5x0.5	pHEMT, dry	30Ω	12Ω
4x10x0.5x0.5	pHEMT, dry	10Ω	6Ω
2x10x0.5x0.5	pHEMT, wet	20Ω	12Ω
4x10x0.5x0.5	pHEMT, wet	4Ω	6Ω
2x10x0.5x0.5	pHEMT, no recess	25Ω	12Ω
4x10x0.5x0.5	pHEMT, no recess	5Ω	6Ω

Effect of varying electron mobility

Figure 98 shows a comparison of measured values of series resistance with increasing electron mobility. The mobility varies from A1159 (2680 cm^2/Vs) to A1166 (3125 cm^2/Vs) to A1168 (5780 cm^2/Vs). This is predicted by the simple model in Figure 30, as R_g, R_r and R_s are all directly proportional to the resistivity of the semiconductor. Resistivity is, in turn, the inverse of conductivity which is proportional to mobility. Therefore, an increase in semiconductor mobility will correspond to a decrease in resistivity thus reducing overall series resistance.

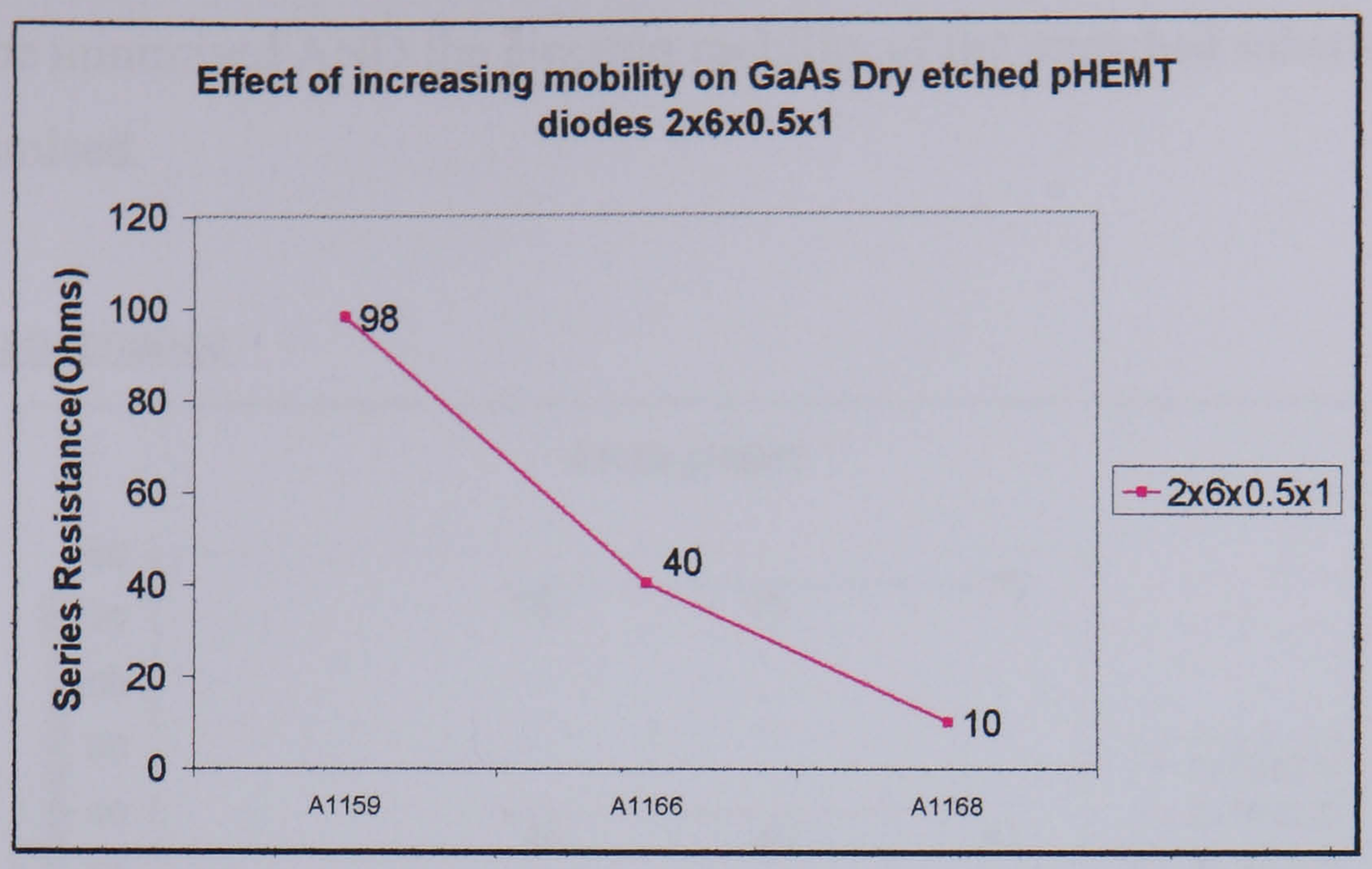


Figure 98 Effect of increasing mobility on Series resistance

Conclusions on Diode series resistance

1) From equations **(63-67)**, the biggest contributions to diode series resistance are from the contact resistance R_c and the resistance of the unetched material in the anode-cathode gap.
2) It has been shown here that (anode width x number of anode fingers) should be made as large as possible to minimise resistance. However, it is desirable to maximise the number of anode fingers rather than simply use a diode with one very long anode finger. There also seems to be a minimum anode width (between 5 and 10μm), below which the resistance in each finger becomes intolerable.
3) Anode length should not be below 0.5μm to avoid metallic resistance causing very large contributions to series resistance. T-shaped anodes should be used for anode lengths below 0.5μm.
4) GaAs pHEMT dry-etched diodes should be used for ease of processing. However, wet etched and non recessed diodes give lower values of series resistance. The disadvantage of these two techniques is that for eventual integration of a mixer with an amplifier, they would introduce an extra step to the fabrication process, unless wet etching was used for transistor recessing.
5) Whilst some attempt was made to minimise ohmic contact resistance, as described in Chapter 2, the other main contribution to series resistance is from the unetched material in the anode-cathode gap. Therefore, anode-cathode spacing

should be minimised AND the electron mobility of the unetched substrate should be maximised.

Junction Capacitance

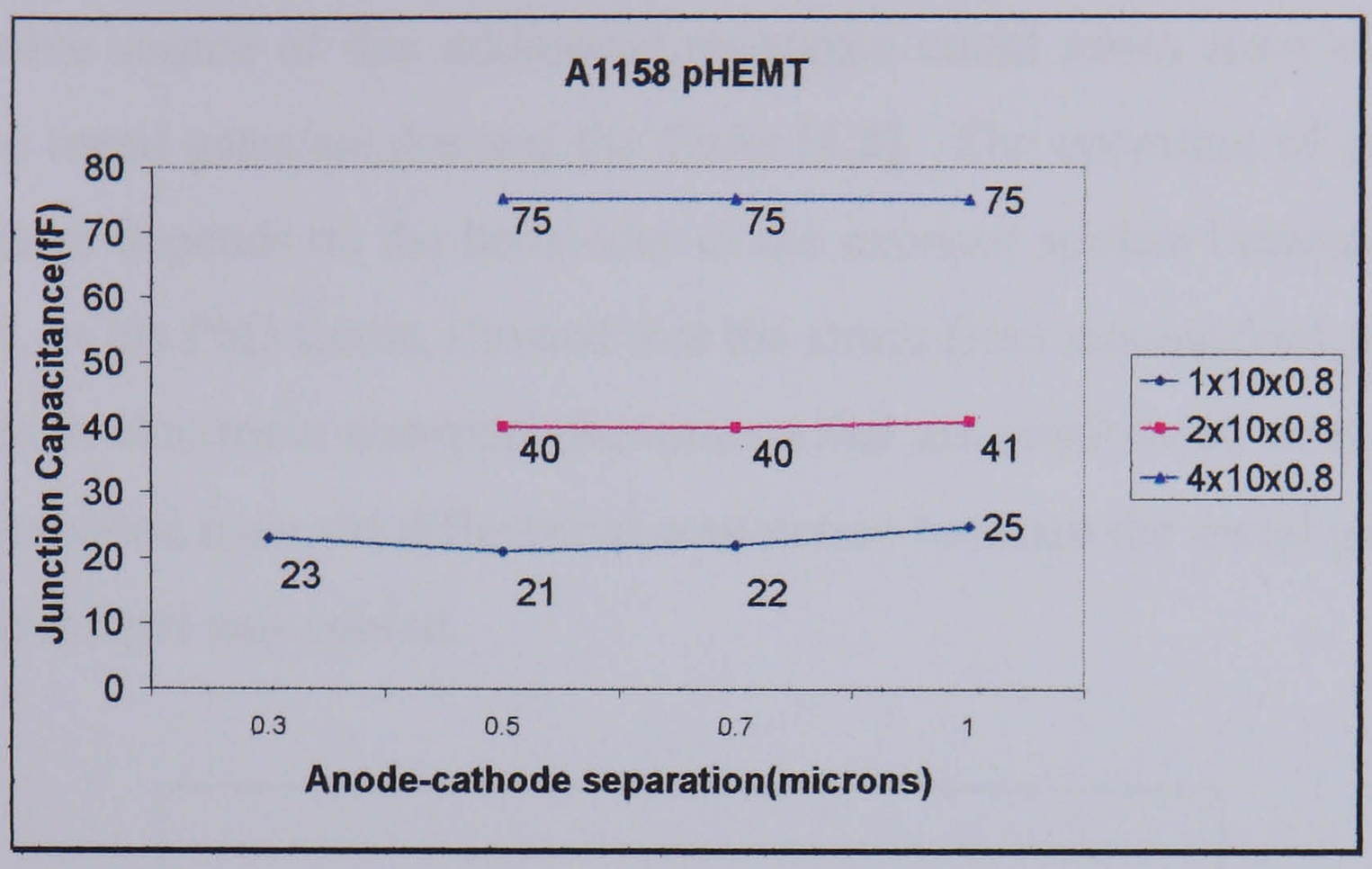


Figure 99 Diode Junction Capacitance versus anode area

Figure 99 above, illustrates that junction capacitance almost scales with junction area - ie doubling the number of anode fingers, doubles the capacitance. However, almost no difference is observed by varying the anode-cathode spacing indicating that inter-electrode geometric capacitance is small. Shown below is a table of measured versus predicted values of junction capacitance (see section 2.6.2.2) for different anode areas:

Table 4.5 Measured and Predicted values of C_s

Diode	Measured	Predicted
1x10x0.8x0.3	23fF	20 fF
1x10x0.8x0.5	21fF	20 fF
1x10x0.8x0.7	22fF	20 fF
1x10x0.8x1	25fF	20 fF
2x10x0.8x0.5	40fF	40 fF
2x10x0.8x0.7	40fF	40 fF
2x10x0.8x1	41fF	40 fF
4x10x0.8x0.5	75fF	80 fF
4x10x0.8x0.7	75fF	80 fF
4x10x0.8x1	75fF	80 fF

4.2.5.3. Investigation of the existence of "strain" resistance

In the initial stage of diode testing (ie before process was optimised), it was found that most diodes had higher than expected values of series resistance. It was thought that a possible source of this additional resistance could result from elastic strain between the metal gates/anodes and the GaAs [4.8]. The operation of devices with patterned gates depends on the behaviour of the exposed surface between the gates. Cusco [4.9], in his PhD thesis, showed that the strain from mismatched gates cannot be neglected in electronic transport phenomena that are sensitive to weak potentials. This strain resulted from the differential contraction between the metal gates and the GaAs as the sample was cooled.

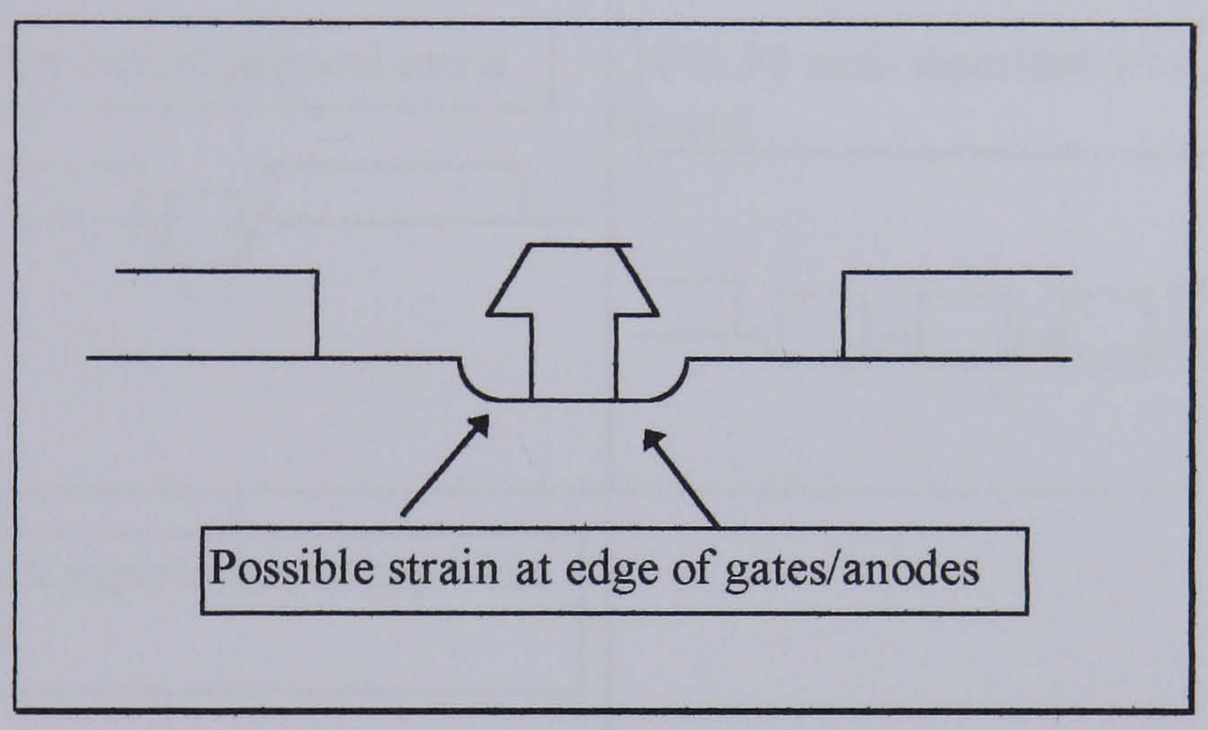


Figure 100 Recessed T-gate structure

To investigate the possible existence of such "strain" induced resistance it was necessary to use a superlattice structure. The superlattice provides a one-dimensional periodic potential experienced by the electrons as they travel from source to drain. The periodic potential is provided by a pattern of parallel striped metal gates on the surface, perpendicular to the direction in which the electrons travel.

Two basic structures were fabricated on A1158 pHEMT material.

1) TLM structures with four different gate widths: 10, 20, 30 and 40 microns - these structures were solid gates located in a recess.

2) TLM structures with four "different" superlattice gates - 10, 20, 30 and 40 microns. The period of the superlattice structures was 100nm with 200nm separation, however, the actual lengths after fabrication were 120nm and 180nm respectively.

These structures are shown below in Figure 101.

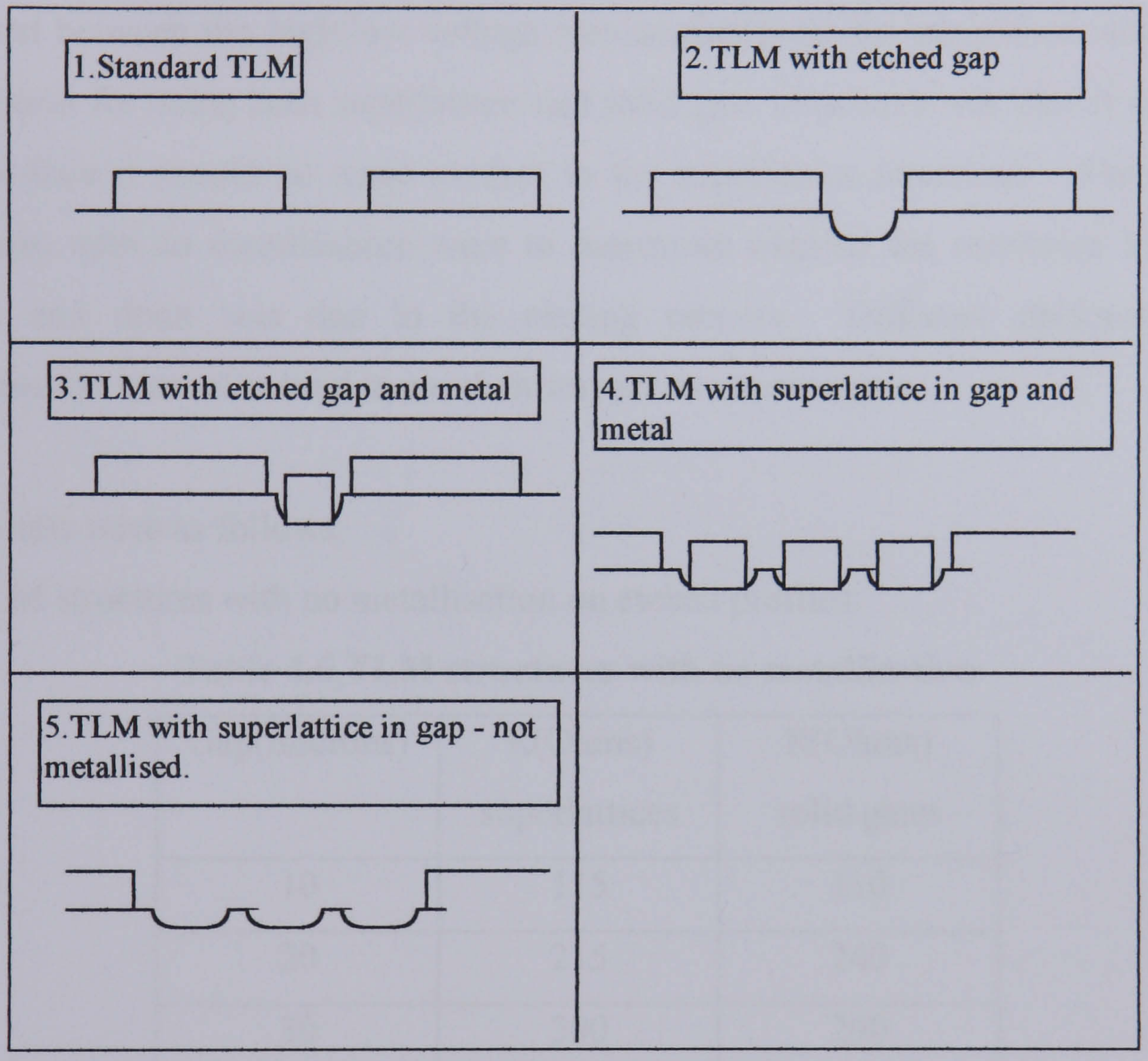


Figure 101 Test structures to monitor the effect of stress on gates/anodes

The following tests were performed:

1) Structures 2) and 5) were dry etched then resistance measurements made without any metallisation.

2) Structures 3) and 4) were dry etched, metallised with different gate thicknesses and then resistance measurements were performed.

The actual resistance measurements were made using a semiconductor parameter analyser - HP4145. These involved simply doing a DC FET measurement with one probe on the source (one TLM ohmic pad), one on the drain (one TLM ohmic pad) and one on the gate(either solid gate or superlattice gate). No gate bias was applied. Measurements were performed at both large voltages (2V from drain-source) and also at small voltages (0.1V drain-source). The smaller voltage measurements allowed data to be extracted on the unmetallised structures but little difference was observed between the high/low voltage measurements on the metallised structures. The reason for using both superlattice and solid gate structures was that if strain is present then it should be more evident in the superlattice structures. The etched structures with no metallisation were to determine whether the resistance between source and drain was due to the etching process. Different thicknesses of metallisation were also tried to see their impact on elastic strain.

The results were as follows:

For TLM structures with no metallisation on etched profiles:

Table 4.6 TLM structures with no metallisation

Gap(microns)	R(Ohms) superlattices	R(Ohms) solid gates
10	115	110
20	215	240
30	300	290
40	390	380

For TLM structures with 15/15/15nm Ti/Pd/Au

Table 4.7 TLM structures with metallisation

Gap(microns)	R(Ohms) superlattices	R(Ohms) solid gates
10	163	130
20	243	260
30	323	370
40	430	520

For TLM structures with 15/15/50nm Ti/Pd/Au

Table 4.8 TLM measurements with metallisation

Gap(microns)	R(Ohms) superlattices	R(Ohms) solid gates
10	125	?
20	250	?
30	333	?
40	500	?

The ? indicate that measurements were not possible due to poor lift-off during processing.

For TLM structures with 15/15/80nm Ti/Pd/Au

Table 4.9 TLM structures with metallisation

Gap(microns)	R(Ohms) superlattices	R(Ohms) solid gates
10	154	148
20	217	196
30	333	243
40	425	338

<u>Conclusions on the existence of "strain" resistance</u>

The results obtained from the TLM structures with solid gates were unreliable due to poor lift-off. Conclusions from the measurements on the superlattice structures are as now given. In order to compare actual and predicted measurement values, further analysis is required. This is given overleaf.

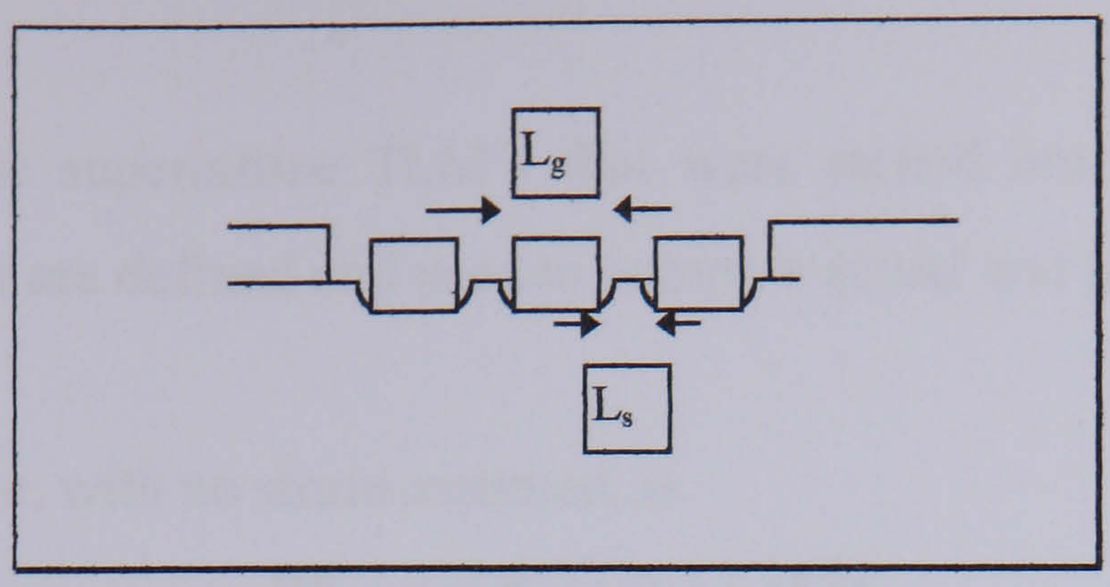


Figure 102 Strain test structures

From Figure 102:

$\mu = 2550\ cm^2/Vs$

W = 100 μm -width of ohmic contact

$q = 1.6x10^{-19}C$

Lg = 0.12μm - superlattice gate length

Ls = 0.18μm - spacing between superlattice gates

Rst - strain related resistance per gate

In order to predict what value of strain resistance may be present, an iterative process can be used. Therefore, if the distance between the contacts is increased from, say,1 to 40 microns in steps of 1μm, then such an iterative process can be performed. Before proceeding it is necessary to define the following extra quantities:

Using the equation for R_t from **(63)**: Rt=Rm+[Rc+Rg+Rr+(Rs/3)]/2

where:

l_r is the length of the etched recess

R_n is the resistance due to the etched, unmetallised regions.

l_c is the length of the unetched material between recess and ohmic contact.

R_c is the resistance of the unetched material between recess and ohmic contact. It is assumed that the ohmic contact resistance is included in this value for this analysis.

l_g is the length of the metallised gate.

R_g is the resistance due to the metallisation on top of etched material.

To conclude on the superlattice TLM's that were etched but not metallised, the following equations are defined and used to compare actual and predicted results.

Estimated resistance, with no strain assumed, is

$$RR_{ngi} = (l_r R_n + l_c R_c).i \quad \textbf{(82)}$$

Estimated resistance with strain assumed due to etching,

$$RR_{ng2i} = (l_r R_n + l_c R_c + 2).i \quad \textbf{(83)}$$

Similarly, for superlattice TLM's that were etched and metallised;

Estimated resistance, with no strain assumed, and metallisation is:

$$RR_{ngi} = (l_r R_n + l_c R_c + (l_r - l_g) R_n).i \quad \textbf{(84)}$$

Estimated resistance, with strain assumed due to etching/metallisation, is

$$RR_{ngi} = (l_g R_g + (l_r - l_g) R_n + l_c R_c + 2).i \quad \textbf{(85)}$$

Therefore the predicted values of resistance from equations **(82)** and **(83)** were as follows:

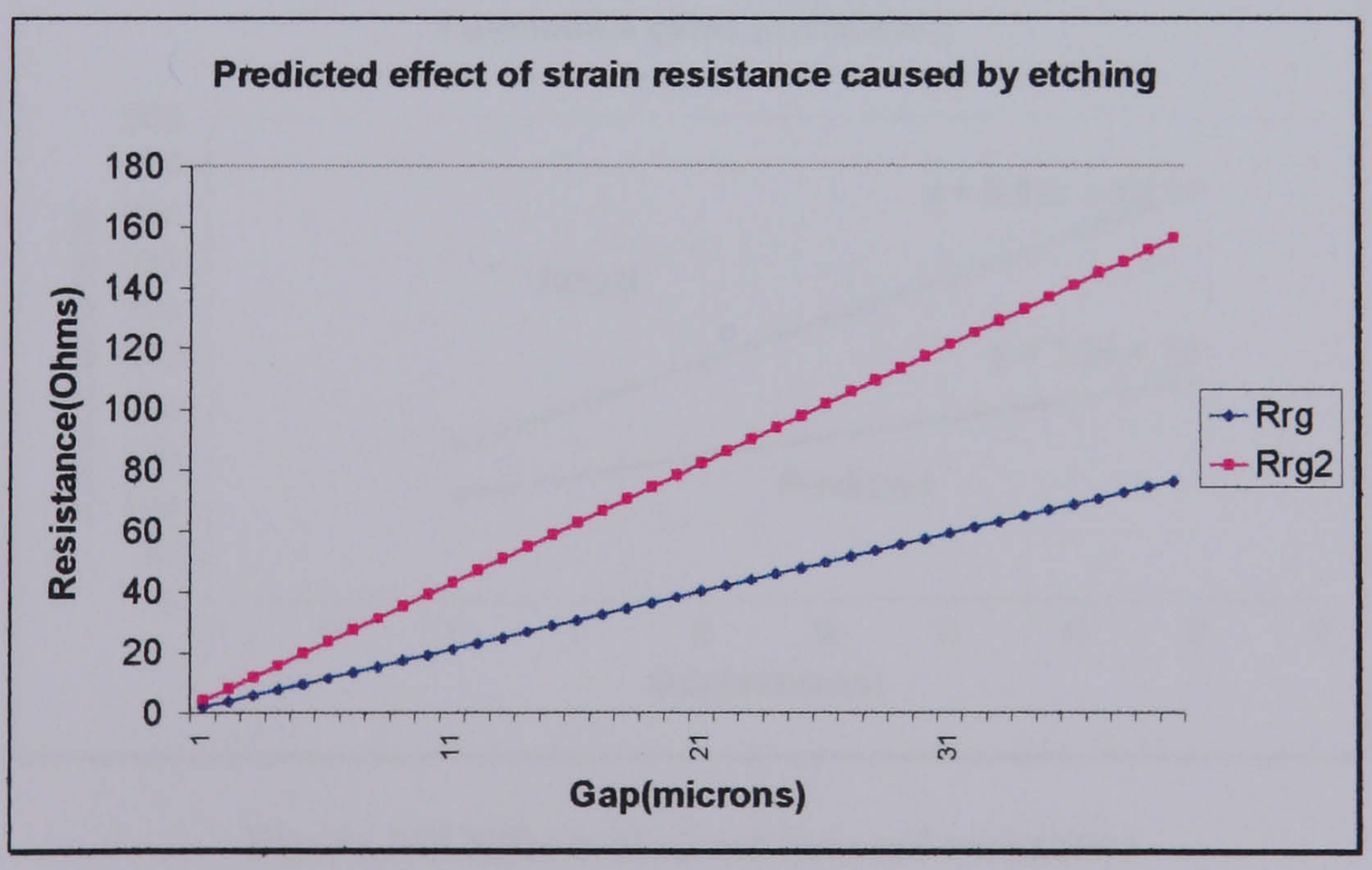


Figure 103 Predicted strain resistance caused by etching

From this graph it can be seen that a contribution of 2Ω per gate caused by etching would cause a significant increase in overall resistance.

Similarly, for metallised structures from equations **(84)** and **(85)**:

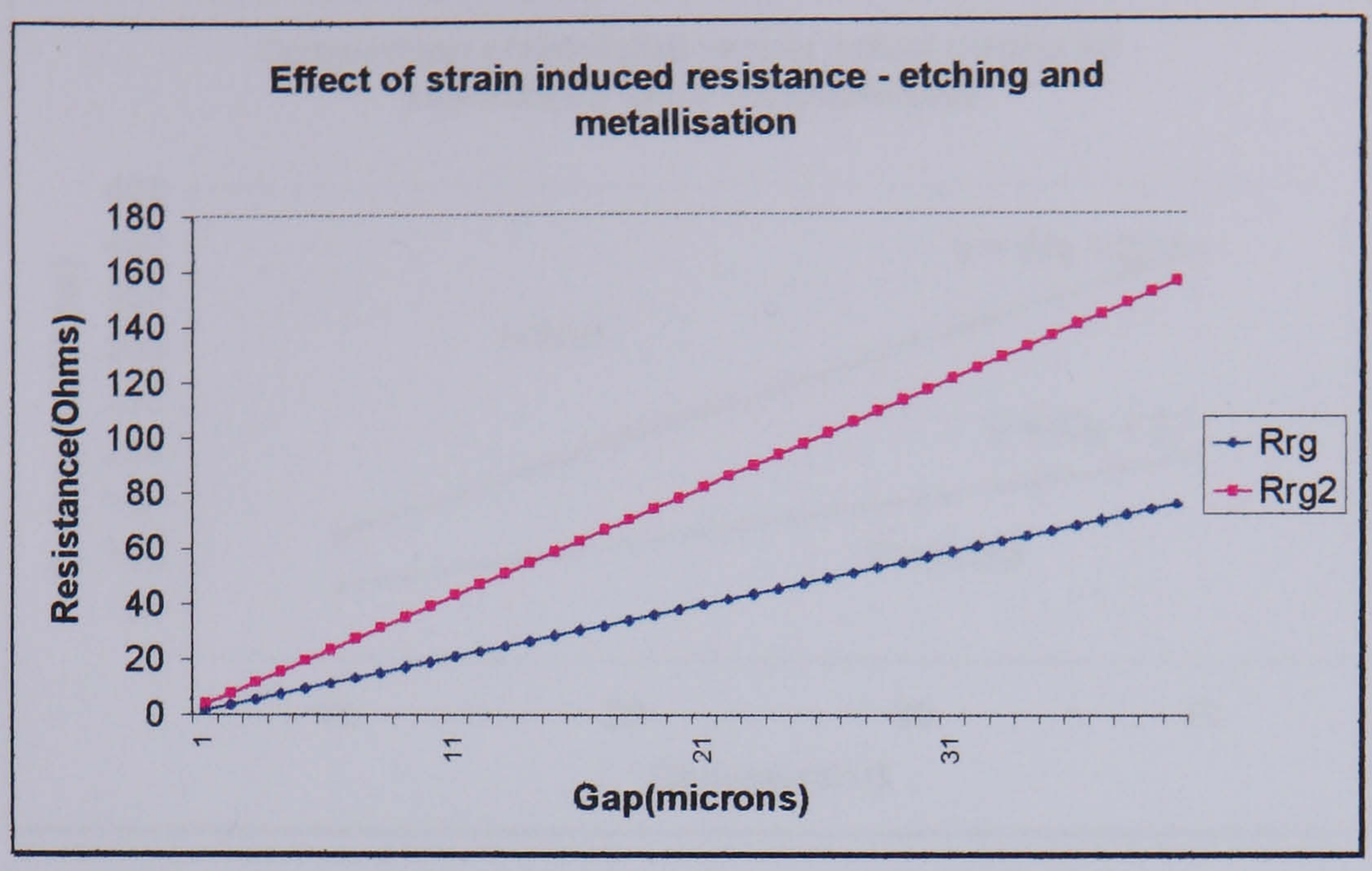


Figure 104 Predicted Strain induced by etching and metallisation

The important point to determine from these measurements was whether the additional resistance was due to etching or the "strain" effect of the metal on semiconductor.

Comparison of measured and predicted results.

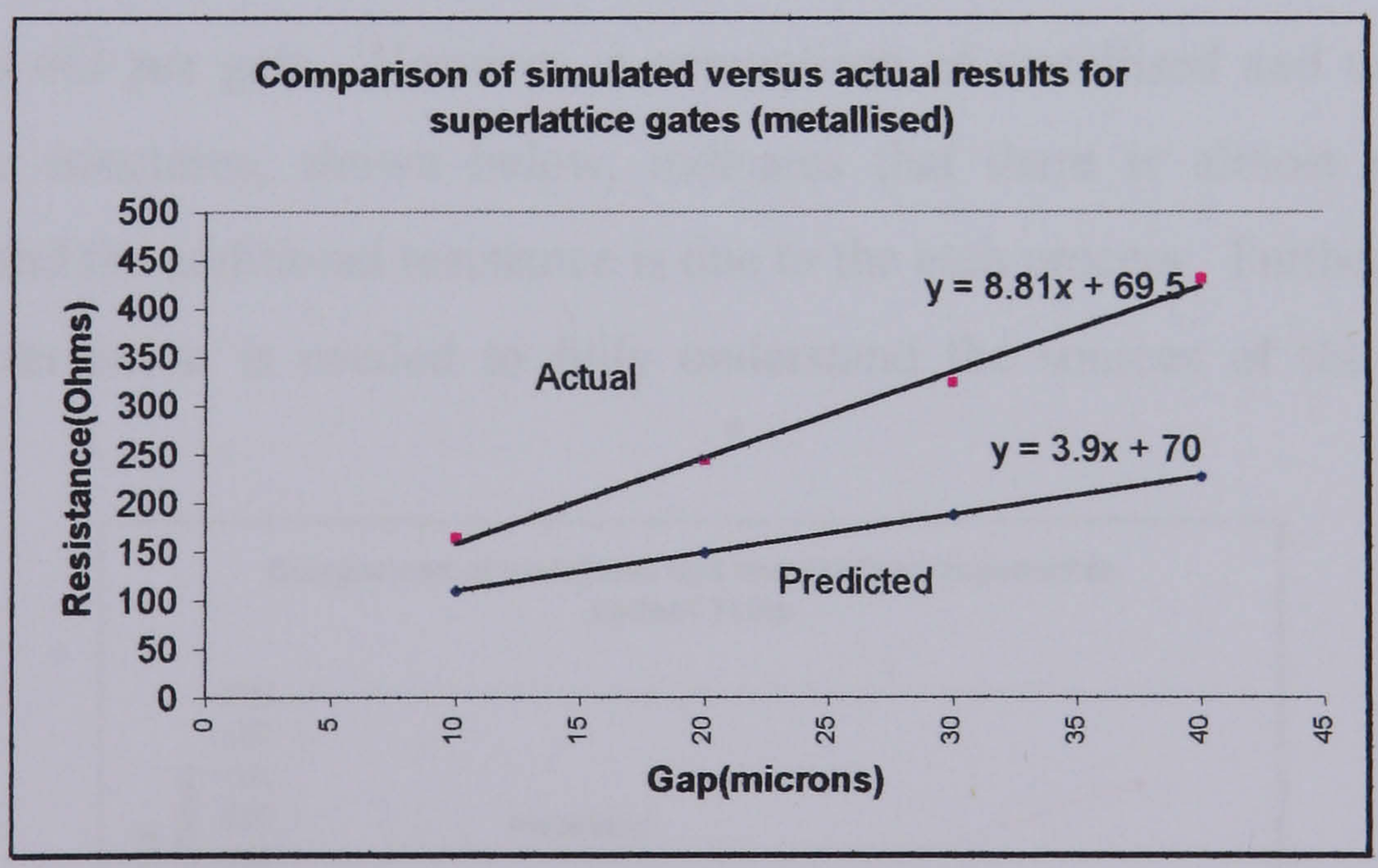


Figure 105 Effects of strain induced resistance

From Figure 105 it can be seen that there exists a significant additional resistance, in excess of 2Ω per gate strip for etched, metallised structures.

However, for unmetallised structures, the same effect is evident:

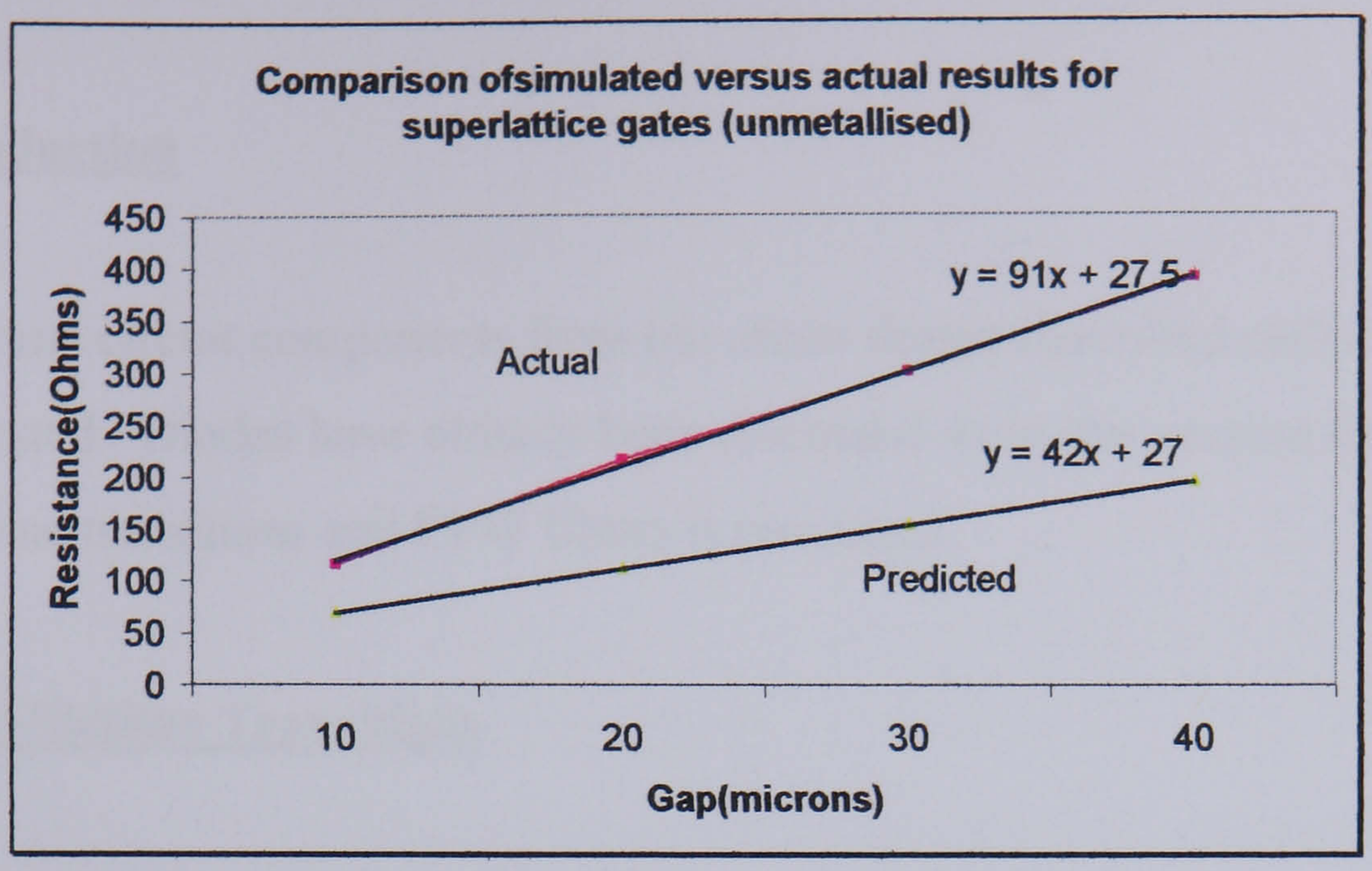


Figure 106 Effects of strain induced resistance

A direct comparison of etched, metallised structures and etched, unmetallised structures is shown below in Figure 107.

Conclusions on strain induced resistance

There is a possibility that a component of strain resistance due to metallisation exists (from equations **(83 & 85)** it is assumed to be around 2Ω). However, in the experiments performed this component of resistance may be in excess of 2Ω, in fact as much as 6Ω per gate. However, a comparison of metallised and unmetallised superlattice structures, shown below, indicates that there is almost no "strain" resistance and the additional resistance is due to the etch process. Further modelling and characterisation is needed to fully understand the sources of this additional resistance.

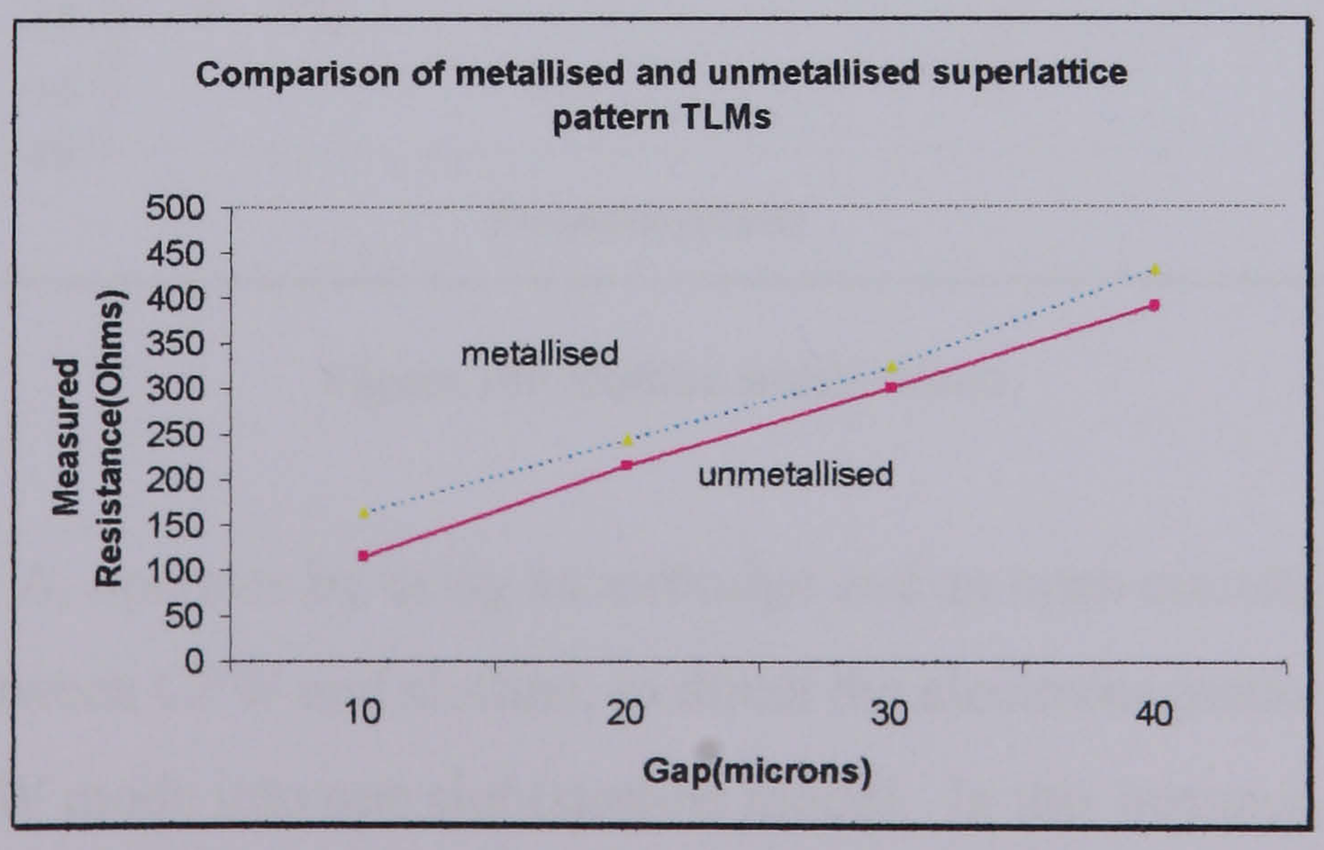


Figure 107 Comparison of metallised and unmetallised structures

4.3 Testing of Passive Circuit Elements

4.3.1 Introduction

The individual circuit components from the mixer design described earlier in Section 2.5 were tested. Diodes have already been discussed so in this section the testing of CPW-Slotline transitions and CPW filters is presented.

4.3.2 CPW-Slotline Transitions

In Section 2.8.3, three different designs for a CPW-Slotline transition were given. The most important point about these transitions is to calculate the loss that can be expected in the transition.. However, the optimisation of such transitions is a detailed topic in itself and only initial investigations were performed.

Starting with transition type A (see Figure 38), the Slotline width was increased from 15 to 20 and then to 25μm. The results of the transition loss are now given:

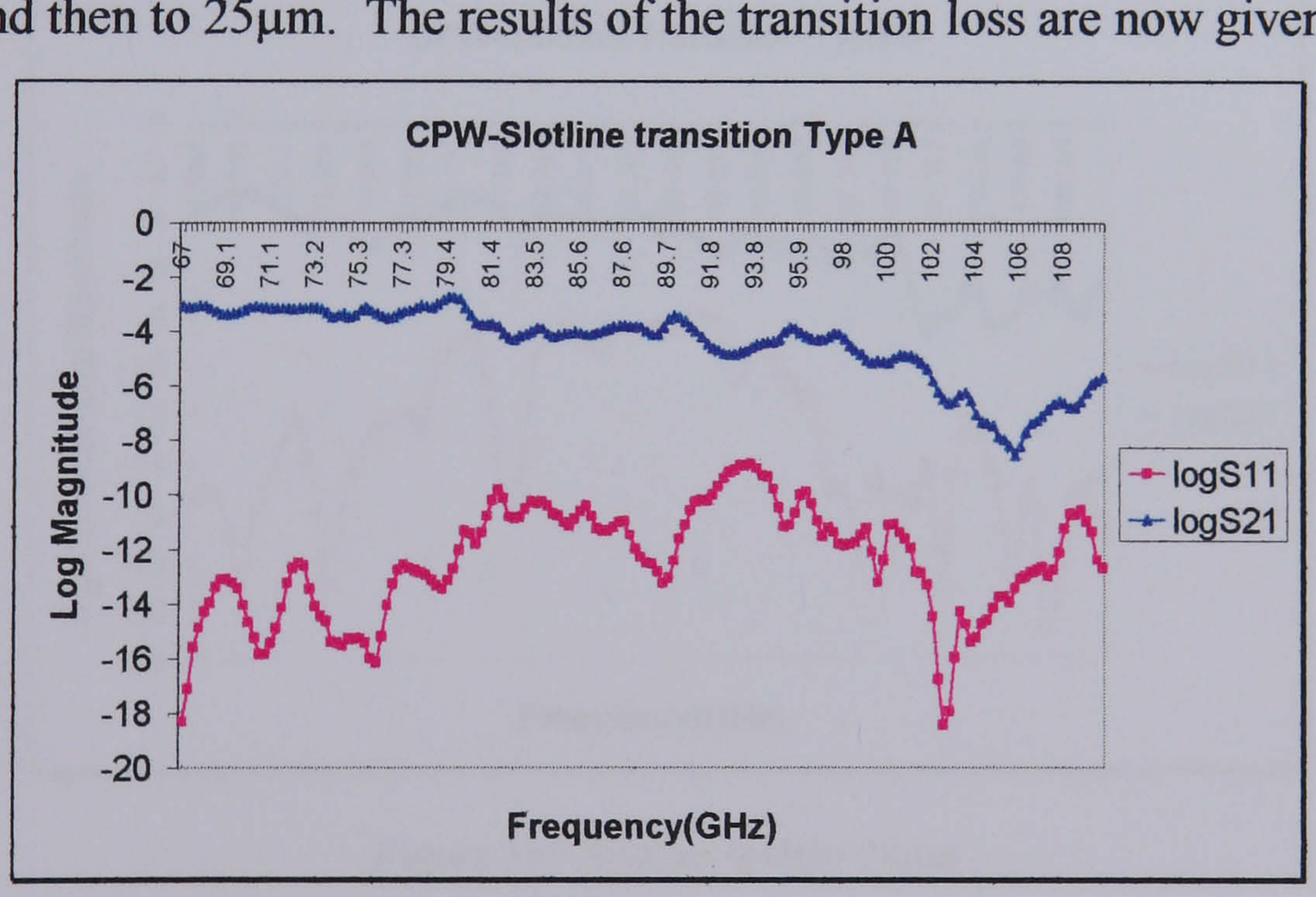


Figure 108 Slotline width=15μm

Transition type A, operates by using an airbridge and an open circuit, located right at the junction between CPW and slotline, to direct the electromagnetic field in the two slots of the CPW mode into one slot (slotline mode). In this instance, with a slotline gap width of 15μm, the loss in each transition (modified to take into account losses

in the probes and cables of 1.4dB) was 2.3dB @94GHz. There are several possible reasons why this transition has such losses:

a) The positioning of wafer probes is not entirely accurate and this leads to some loss of accurate magnitude/phase information (may be accurate to around 10μm).
b) The position of the airbridge, located at the CPW-Slotline junction, may not be exact enough to concentrate all of the electromagnetic field propagating in the CPW into the slotline. The accuracy of the positioning of this airbridge, effectively determined by the limits of the photolithographic process, was between 5 and 10μm. Therefore, this may mean that the combination of open circuit and airbridge is not efficient in directing the signal from CPW to slotline and a significant amount of the signal may be reflected.
c) It is not known what the value of slotline impedance for a gap width of 15μm is, so there may be mismatch losses between CPW and slotline. This is discussed overleaf.

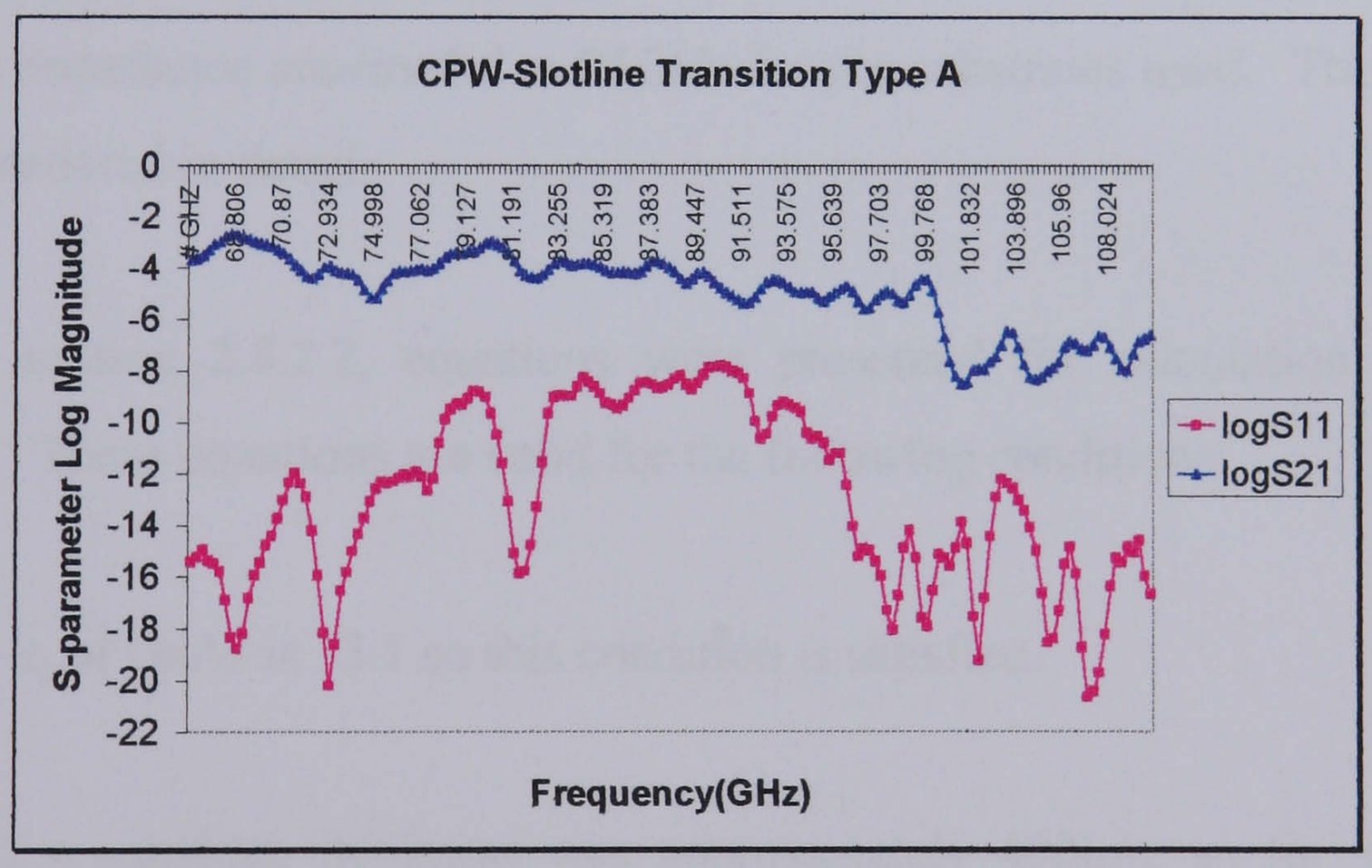


Figure 109 Slotline width=20μm

Similar losses are obtained for a slotline gap width of 20μm, and points a), b) and c) listed above are also valid for these measurements (shown in Figure 109) with, once again, the slotline impedance not being known.

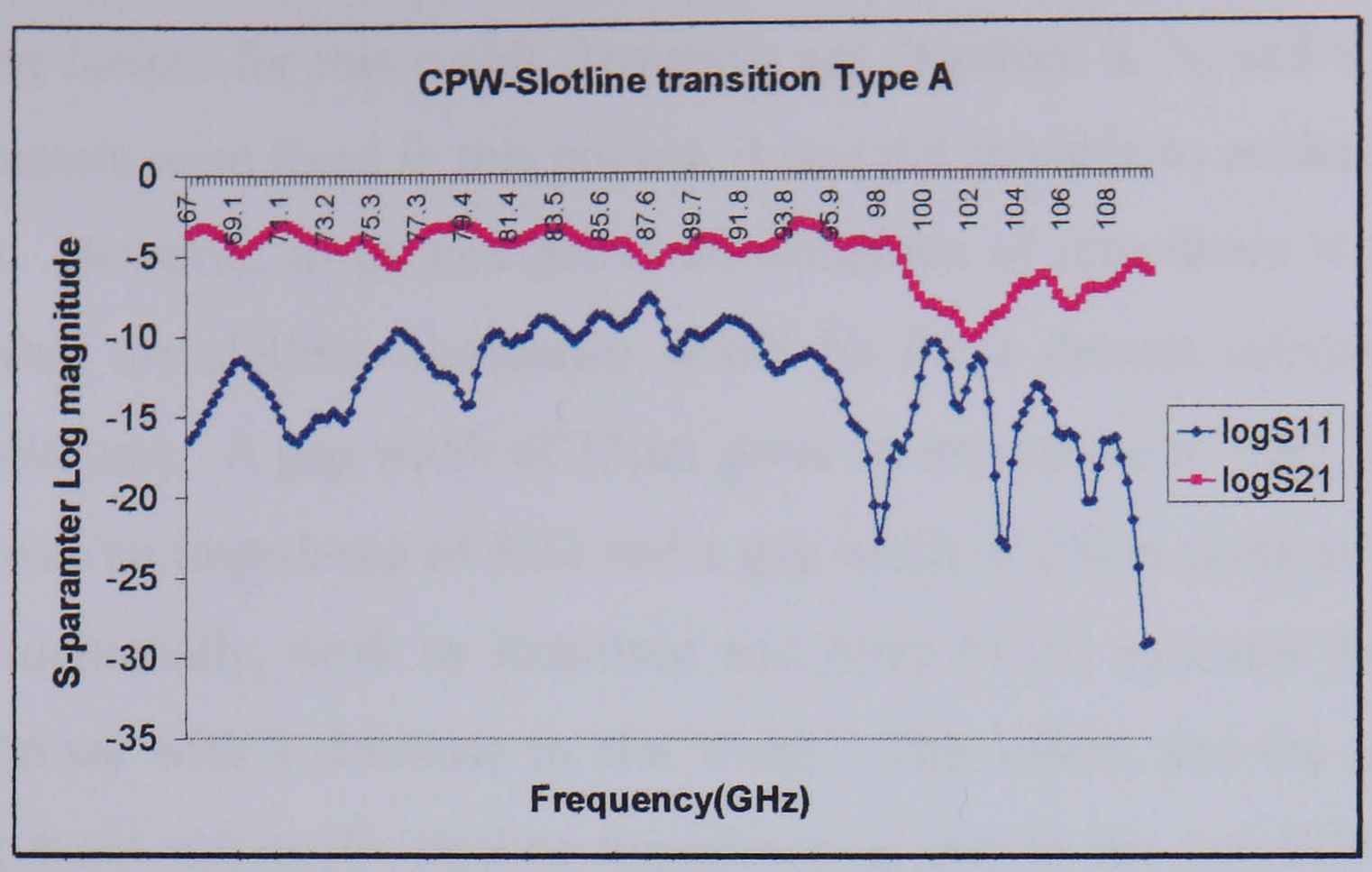


Figure 110 Slotline width=25μm

From the measurements shown in Figures 108,109 and 110, the slotline gap of 25μm gives the smallest back-to-back insertion loss of 3.4dB @ 94GHz. Adjusting this loss to take into account the measured losses in the cables and probes of 1.4dB, the loss due to each transition is 1dB. It is not possible to say if this slotline gap gives an impedance closer to 50Ω than the gaps of 15 and 20μm as the published equations for slotline impedance are invalid at 94GHz for the substrates used. This point will now be considered in detail.

Earlier, in section 2.8.2.2, equations were presented for calculation of slotline impedance. These equations are valid for the following conditions:

$9.7<\varepsilon_r<20$ - ε_r of GaAs is 13.1 so this condition is satisfied.

$0.02<W/h<1$ - substrate thickness was approximately 400μm, so for slotline gap widths of anything from 10μm to just under 400μm are valid.

$0.01<(h/\lambda_o)<(h/\lambda_o)_c$ - where $(h/\lambda_o)_c$ is given by $0.25/(\varepsilon_r-1)^{1/2}$. **It is this condition that is not satisfied for a 400μm thick GaAs substrate at 94GHz**. The calculated value of $(h/\lambda_o)_c$ (The quantity $(h/\lambda_o)_c$ represents the cut-off value for the TE_{10} surface-wave mode on the slotline) is 0.07 while the value of (h/λ_o) is 0.125.

The limiting factors for this cutoff frequency are therefore h, λ_0 and ε_r. Since all three parameters were fixed in this project, it was not possible to evaluate the exact impedance. However, to try and get some indication of impedance it is useful to consider what the slotline impedance would be for a thinner substrate (200μm instead of 400μm). A gap width of 15μm gives an impedance of 50Ω, a gap width of 20μm gives an impedance of 42Ω and a gap width of 25μm gives an impedance of 25Ω. Additionally, work by Robinson and Allen [4.10] indicates that losses in slotline increase with a decrease in slot width. This effect, and the difficulty in calculating exact values for slotline impedance, is due to the non-TEM nature of slotline propagation, which is quasi-TE and strongly dispersive.

It was decided that knowledge of the measured insertion loss was sufficient information for this project, so no further increases were made to the slotline gap as this would then begin to approach the CPW ground-ground spacing.

Effect of length of Slotline on transition loss

To assess the importance of the length of slotline to the transition loss, the transition type A was used. Additional lengths of slotline of 100, 200 and 400μm were inserted between the back-to-back transitions of type A. The results of these tests are now given:

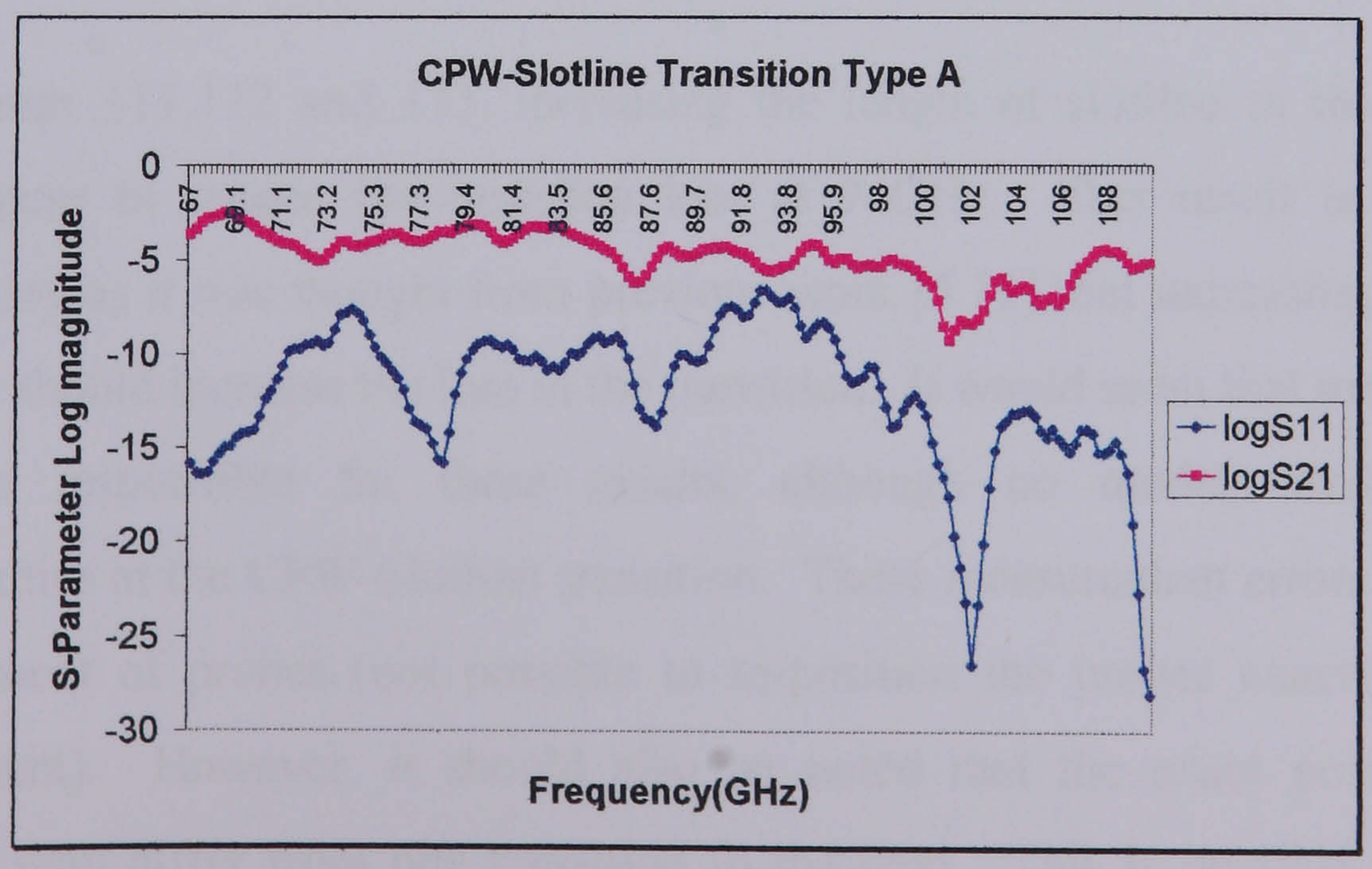


Figure 111 Transition Type A + 100μm Slotline

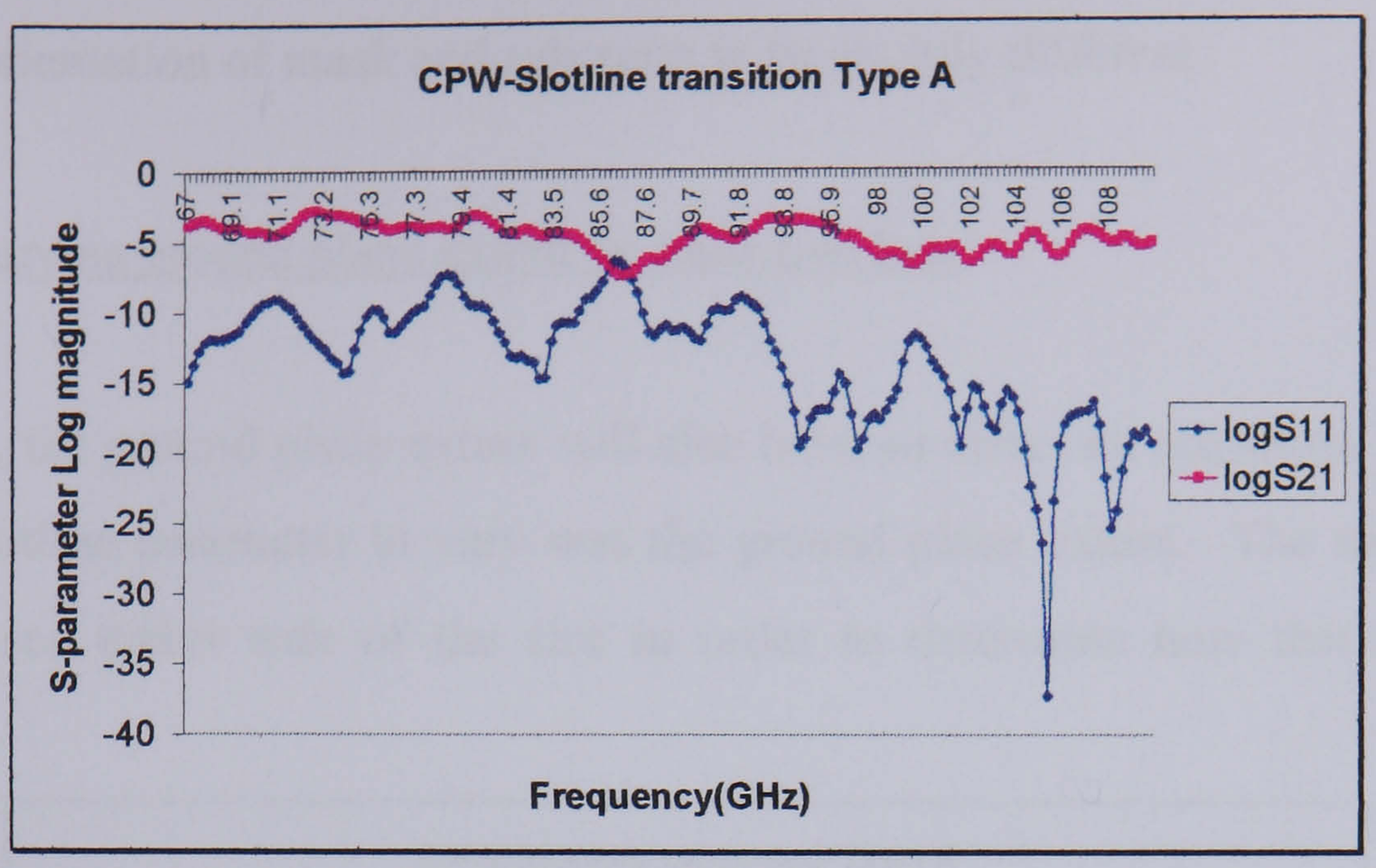


Figure 112 Transition type A + 200μm Slotline

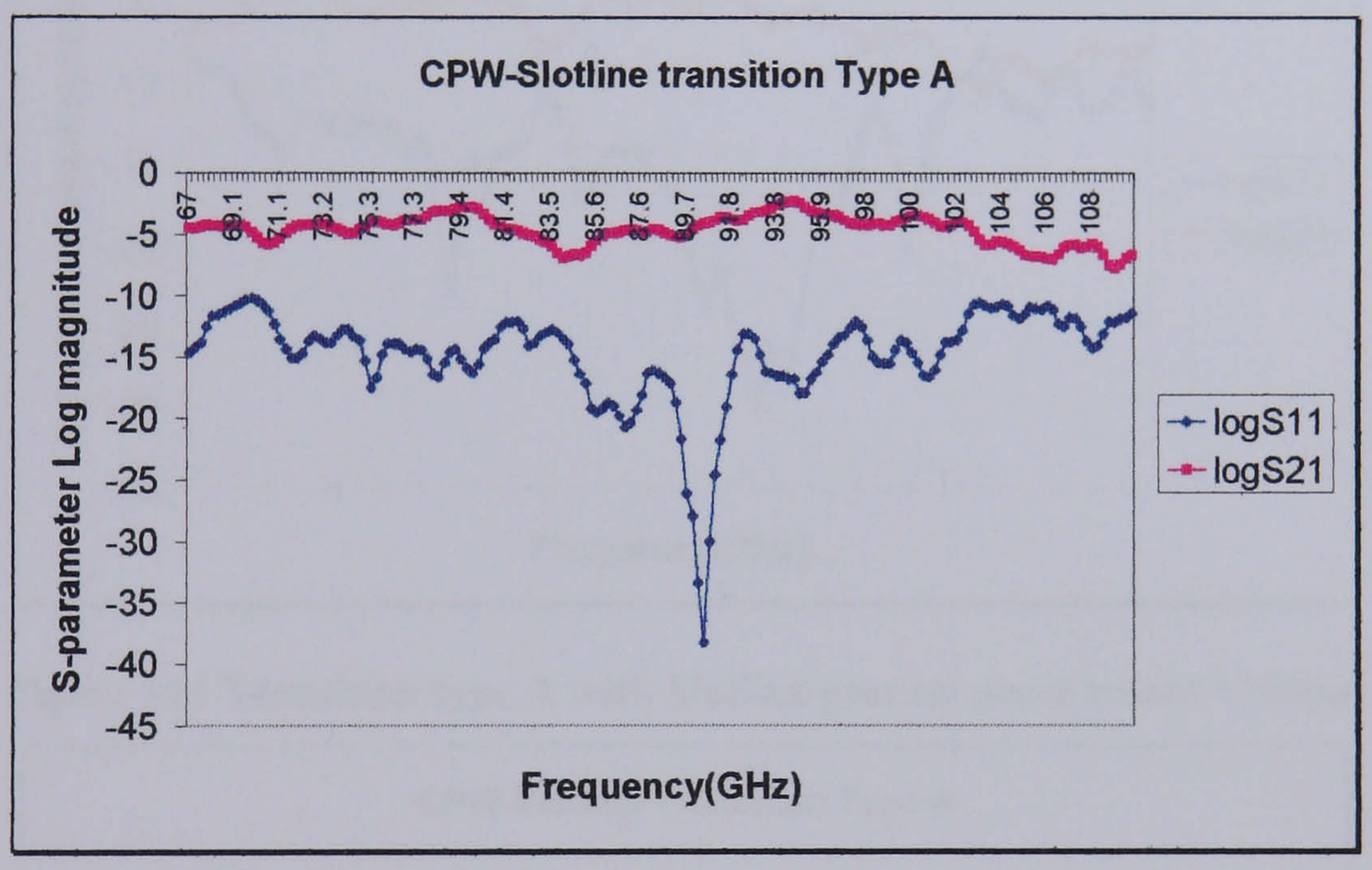


Figure 113 Transition Type A + 400μm Slotline

From Figures 111,112 and 113, increasing the length of slotline in the transition would appear to reduce the insertion loss at 94GHz. This result is somewhat contradictory as it was thought from previous work [4.10] that increasing the length of slotline should increase the loss in the transition. It would seem that measurement errors are responsible for these results, although no models exist for the discontinuities at the CPW-Slotline transition. These measurement errors arise from the placement of probes (not possible to re-position the probes exactly for each measurement). However, it should also be noted that the exact positioning of airbridges may differ from one transition to the next. This is possible due to the

manual alignment of the airbridges during the photlithographic process , which may cause the orientation of mask and substrate to be slightly different.

Effect of varying ground plane extent on transition loss

From [4.7], the ground plane extent will also have an effect on transition loss and so the next slotline parameter to vary was the ground plane extent. The metallisation was increased either side of the slot in order to determine how this affects the transition.

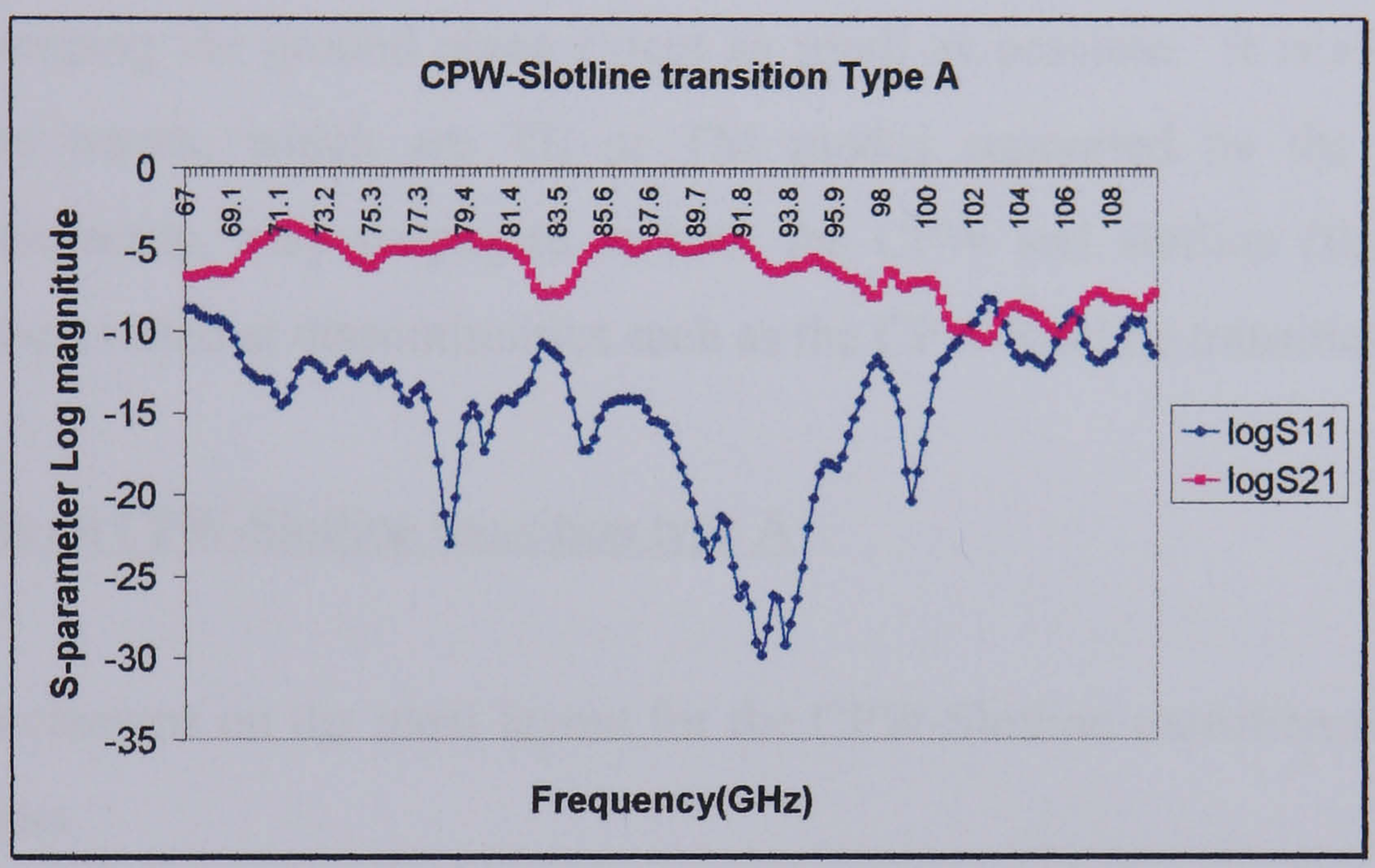


Figure 114 Transition type A with Slotline ground plane extent +100μm

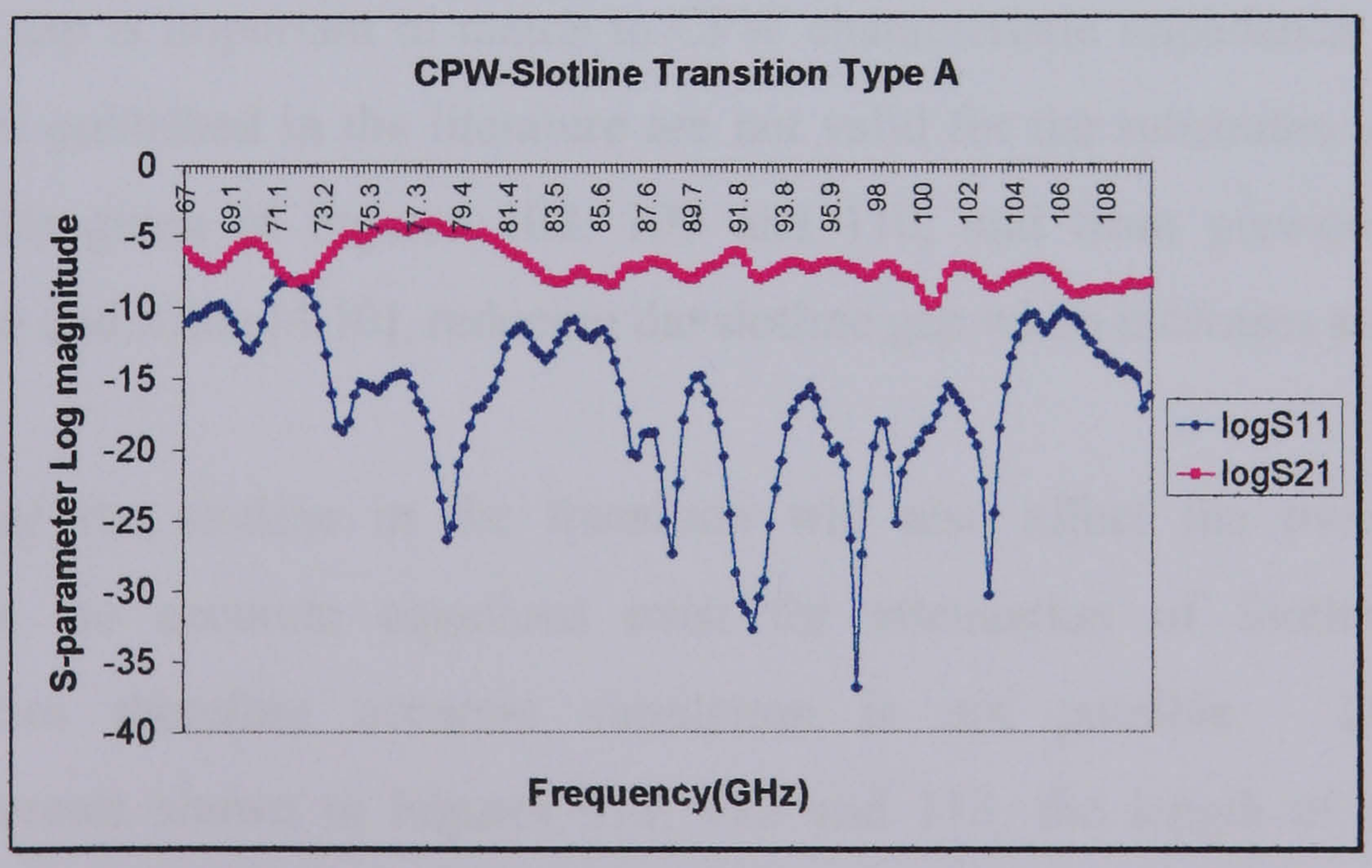


Figure 115 Transition type A with Slotline ground plane extent +300μm

From Figures 114 and 115, increasing the slotline ground plane extent, increases transition loss. The normal measurement errors of cable/probe losses and probe

positioning are also applicable here. To fully understand the reasons for this it is necessary to discuss some of the possible modes of propagation in both CPW and slotline.

During on-wafer measurements, the measurement chuck ensures that the transmission lines are effectively conductor backed. Thus a parasitic, quasi-microstrip mode of propagation can exist [4.11] with the CPW (or slotline) ground plane acting as microstrip line and the measurement chuck acting as the microstrip ground plane. Increasing the substrate thickness would reduce these parasitic modes, as would keeping the ground plane extent as small as possible. It is also possible that surface waves, which are TE or TM modes supported by the effectively grounded dielectric, may propagate in both the CPW and slotline (these surface waves can be excited at discontinuities such as the CPW-Slotline transition).

Conclusions on CPW-Slotline transition type A

Overall conclusions on the ideal layout for the CPW-Slotline transition to minimise transition loss:

1) Slotline gap is important to match to CPW characteristic impedance. However, equations published in the literature are not valid for the substrates used. From the results given in Figures 108, 109 and 110, and from previous work by Robinson and Allen [4.10], reducing the slotline gap width increases attenuation.

2) Length of the slotline in the transition will also affect the transition loss. However, no accurate equations exist for attenuation of Slotline at high frequencies therefore accurate simulation is not possible. Despite the measurements shown in Figures 111, 112 and 113, the length of the slotline should be kept to a minimum to enable a compact transition to be realised (although modelling of the discontinuities at the transition would be useful).

3) Increasing the slotline ground plane extent increases the transition loss, due to the resultant increase in parasitic modes of propagation such as quasi-microstrip and surface modes. Ground plane extent should, therefore, be kept to a minimum.

Other types of CPW-Slotline transition

The other transitions described in Section 2.8, offer some form of tuning to compensate for the discontinuity at the CPW-Slotline transition. Indeed, transition types A, B & C are all essentially the same type of transition. Type A provides a 90^{O} open circuit at the transition, type B uses a slotline radial stub with an angle less than 90^{O} and type C uses a simple, rectangular slotline stub. The performance of the transitions with $\lambda/4$ radial and rectangular slotline stubs at the junction of the transition are now presented.

Transition type B from Section 2.8, uses a radial stub to direct as much of the CPW signal to the Slotline. Three different angles for the stubs were tested.

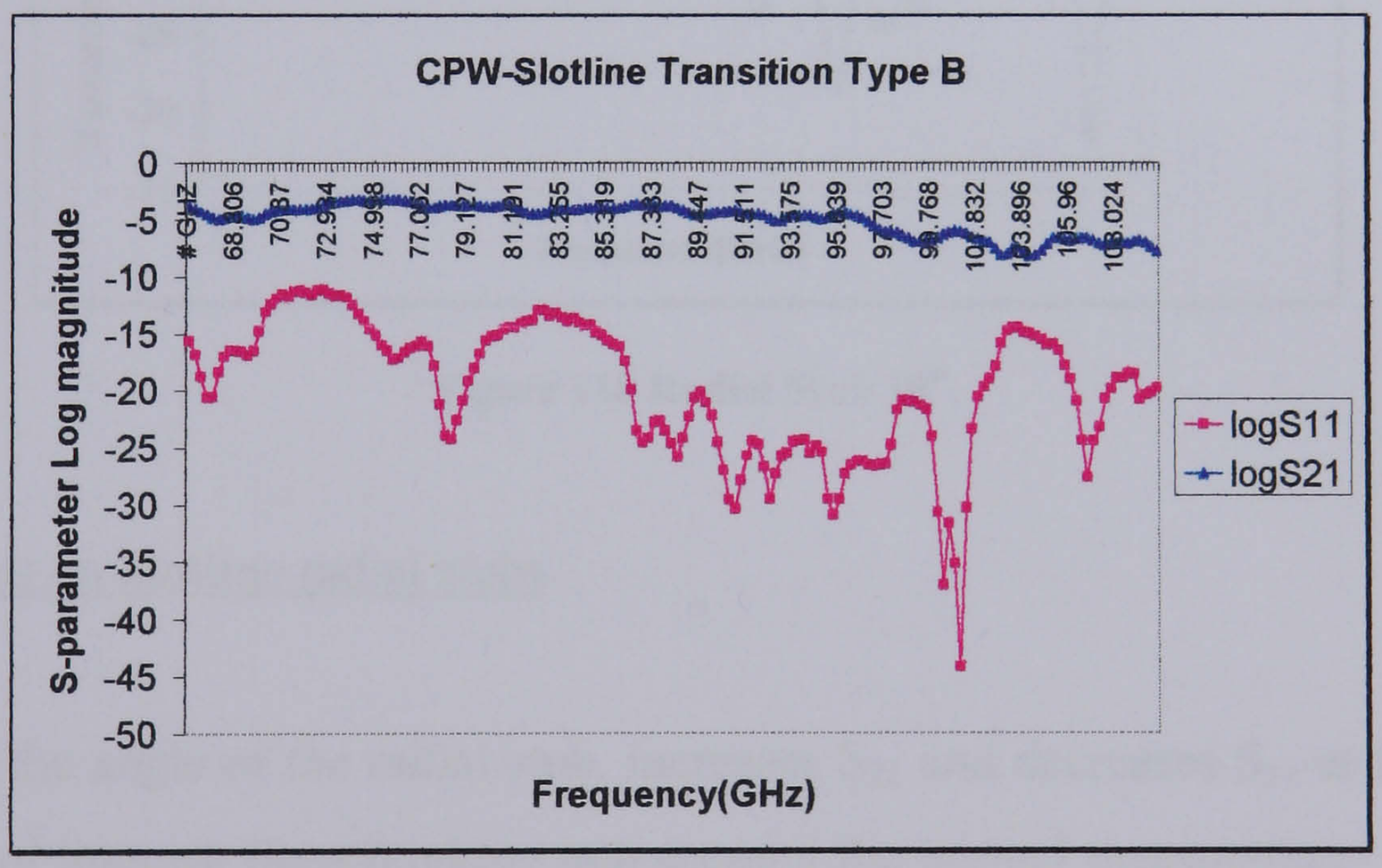


Figure 116 Radial Stub 30°

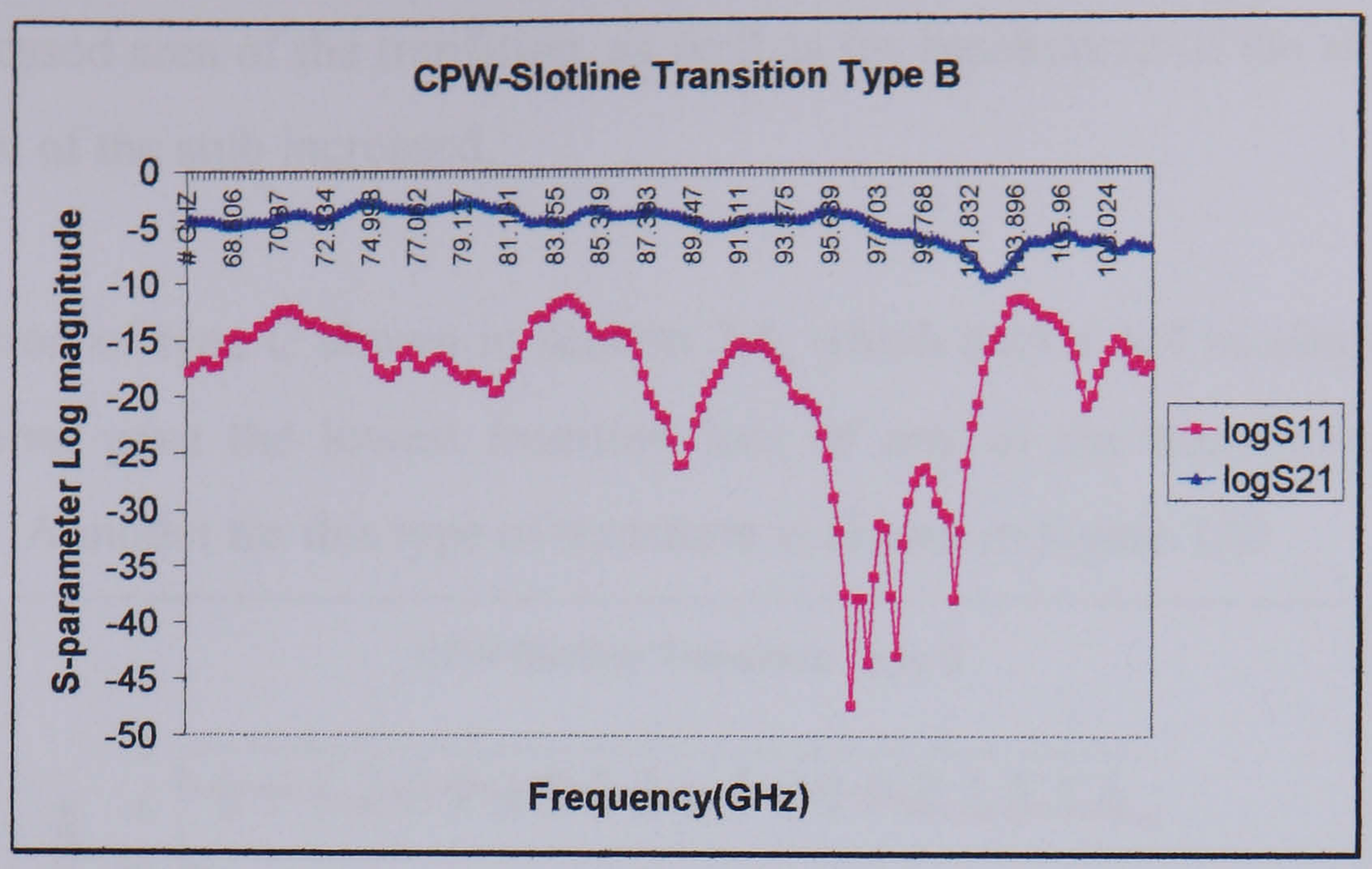


Figure 117 Radial stub 40°

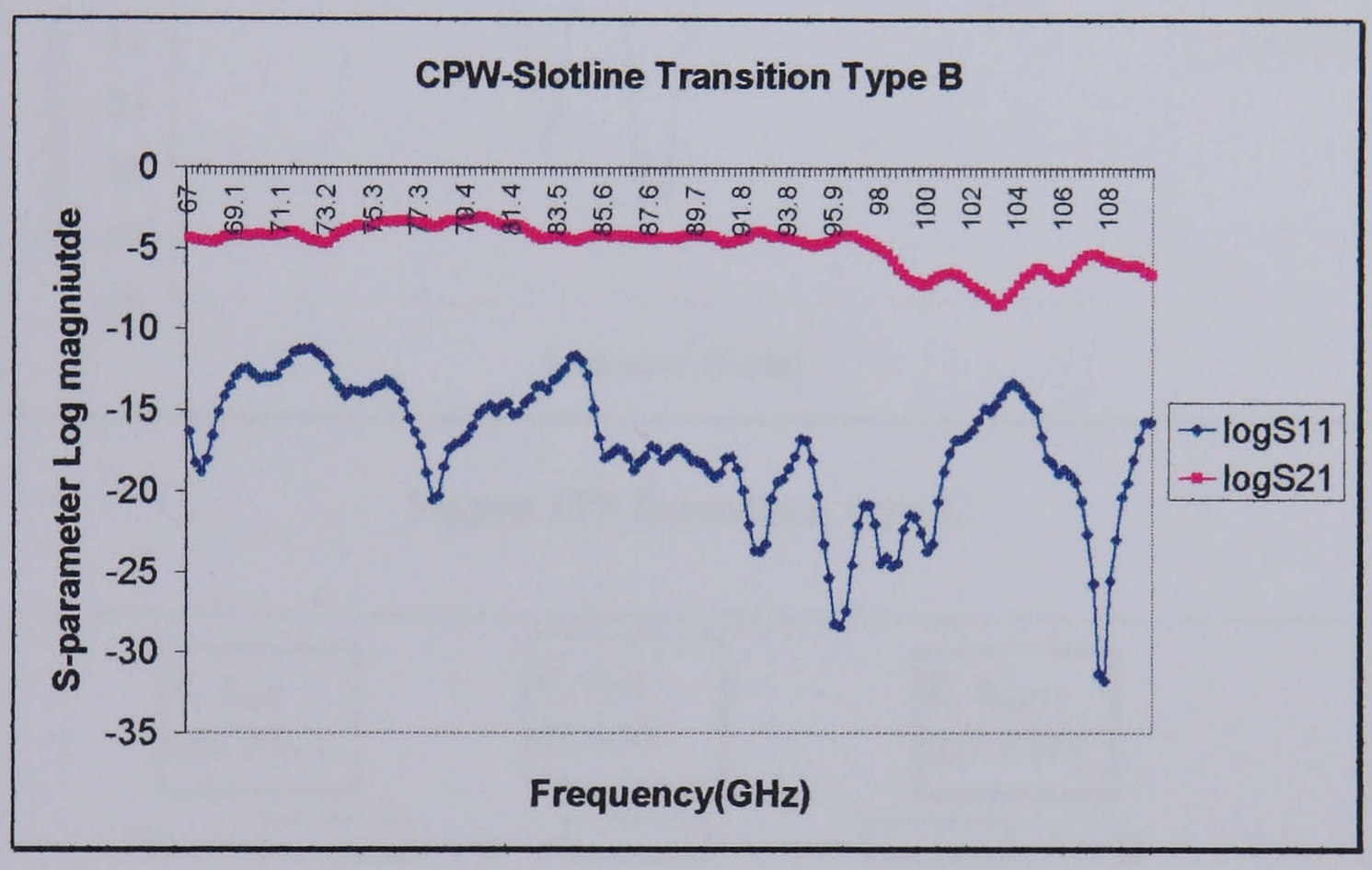


Figure 118 Radial Stub 10°

Conclusions on Slotline radial stubs

Increasing the angle of the radial stub, increases S_{21} and decreases S_{11} at the chosen frequency of interest, though taking into account the normal measurement errors and the difficulty in accurate probe placement, this observation may not always be valid. The question also arises as to whether there is an angle for the radial stub, above which transition loss increases ? From [4.11], the primary benefit of this type of transition using radial stubs was to increase the transition bandwidth. This type of transition was found to be more susceptible than transition type A to parasitic moding, particularly as the angle increased above 45^{O}. The moding was partly due

to the increased area of the transition, as well as the breakdown of the slotline mode as the angle of the stub increased.

The transition of type C shown in section 2.8, which uses a λ/4 rectangular stub at the transition, gave the lowest insertion loss of any of the transitions that were fabricated. A model for this type of transition is shown in Figure 120.

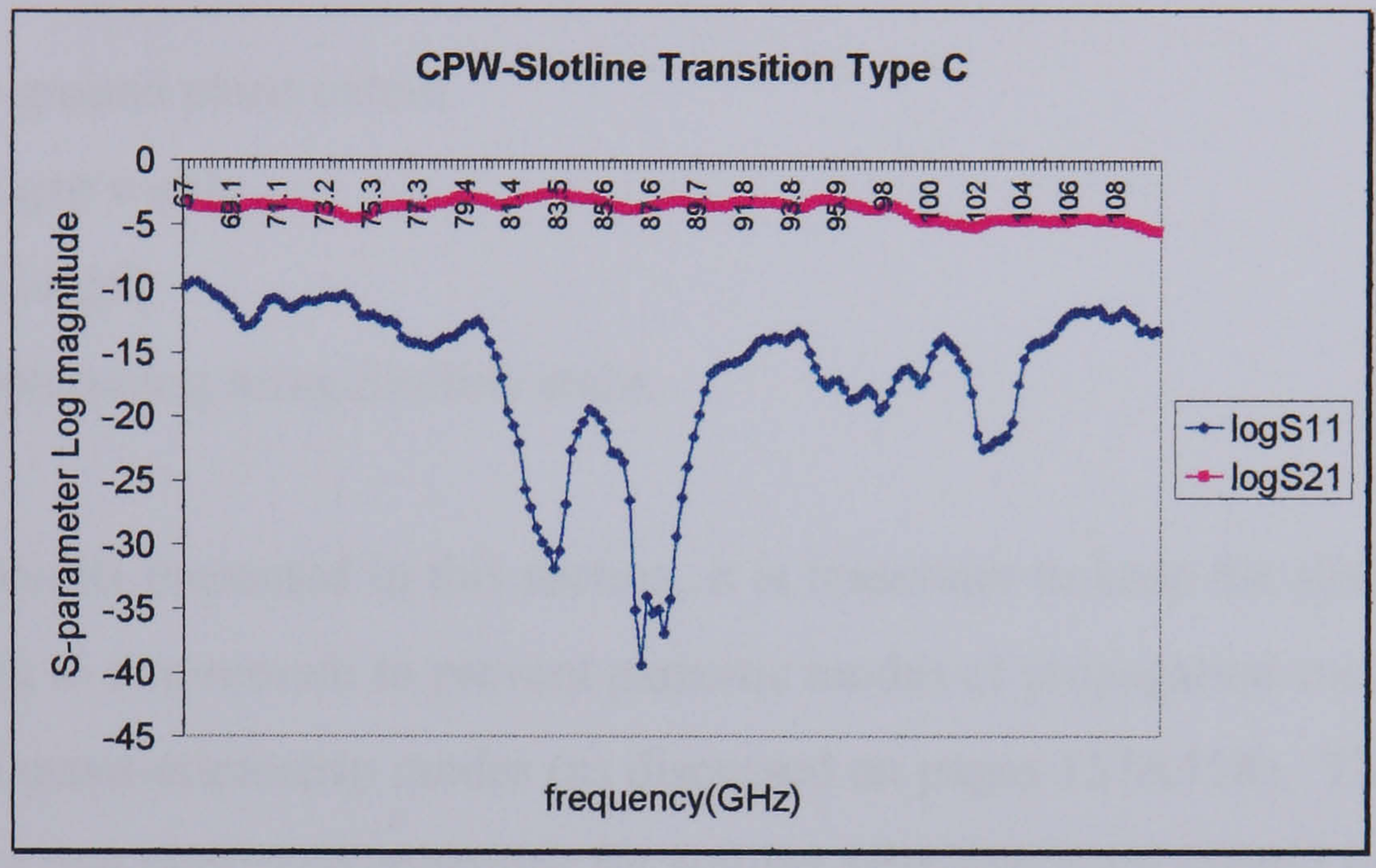


Figure 119 Transition type C

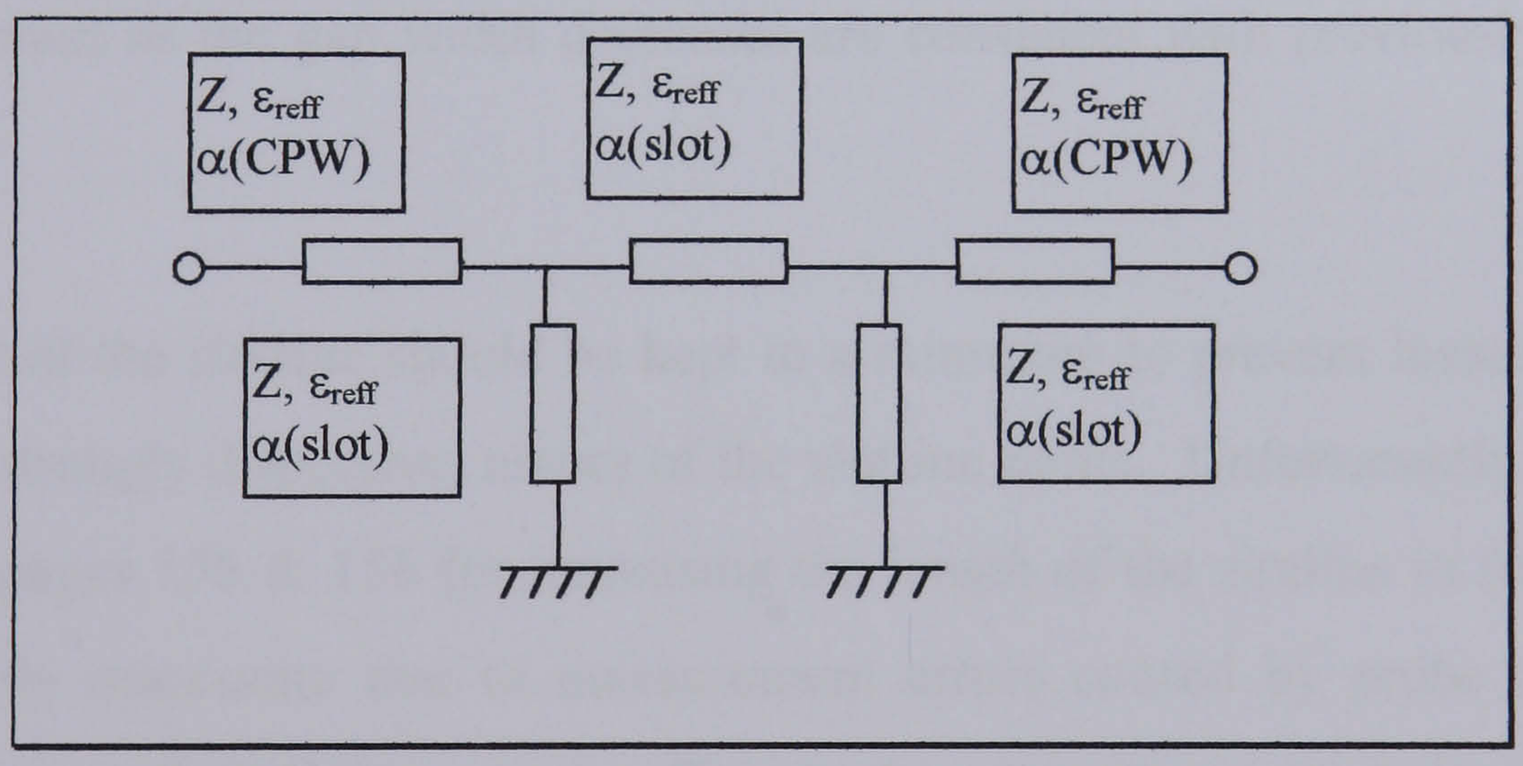


Figure 120 Model of CPW-Slotline transition

This transition is effective in ensuring that most of the electromagnetic field is concentrated into the slot. More sophisticated transitions use a CPW λ/4 open circuit stub in addition to the slotline short circuit. Since the slotline impedance and attenuation is not known, it was not possible to use the model in Figure 120 to provide a graph of measured versus predicted performance for this type of transition.

4.3.3 Summary of Results from CPW-Slotline transitions

Whilst there is considerable scope for the analysis of these transitions, the approach taken here was that it was important to know the loss in the chosen transition and to understand what factors may affect this loss. These factors are:

1) Slotline ground plane extent.
2) Slotline gap width
3) Slotline length
4) Transition tuning using Slotline stubs.

From the results presented in this section, it is important to keep the slotline ground plane extent to a minimum to prevent parasitic modes of propagation such as surface modes and quasi-microstrip modes (as discussed on pages 157&158). Though it has been shown that published equations for slotline impedance are invalid for the GaAs substrates used in this project, the general results (see pages 154&155) that slotline losses increase as the gap width decreases are consistent with previously published results.

The length of the slotline should be kept to a minimum to prevent losses due to the quasi-TE, strongly dispersive, nature of the slotline mode. Unfortunately, the results shown on pages 155 & 156 for increasing the length of the slotline in the transition are probably inaccurate due to measurement errors caused by probe positioning. Transition types B & C prove more effective than transition type A in directing the electromagnetic field from CPW to slotline. In particular, transition type C proves efficient due to the use of a short circuit slotline stub for tuning. The angle of the radial stub of transition type B is important - as the angle increases parasitic modes increase due to the partial breakdown of the slotline mode and the increased area of the transition.

So as a result it was decided to keep the slotline ground plane extent to a minimum (200μm based on CPW ground plane extent). The slotline gap width was chosen to

be 25μm, although it was recognised that this may not correspond to a perfect impedance match with CPW. The length of the slotline section was chosen to be as short as possible to minimise chip size.

4.3.4 Filters

The results of testing the high and low pass filters shown in Section 2.8 are given below:

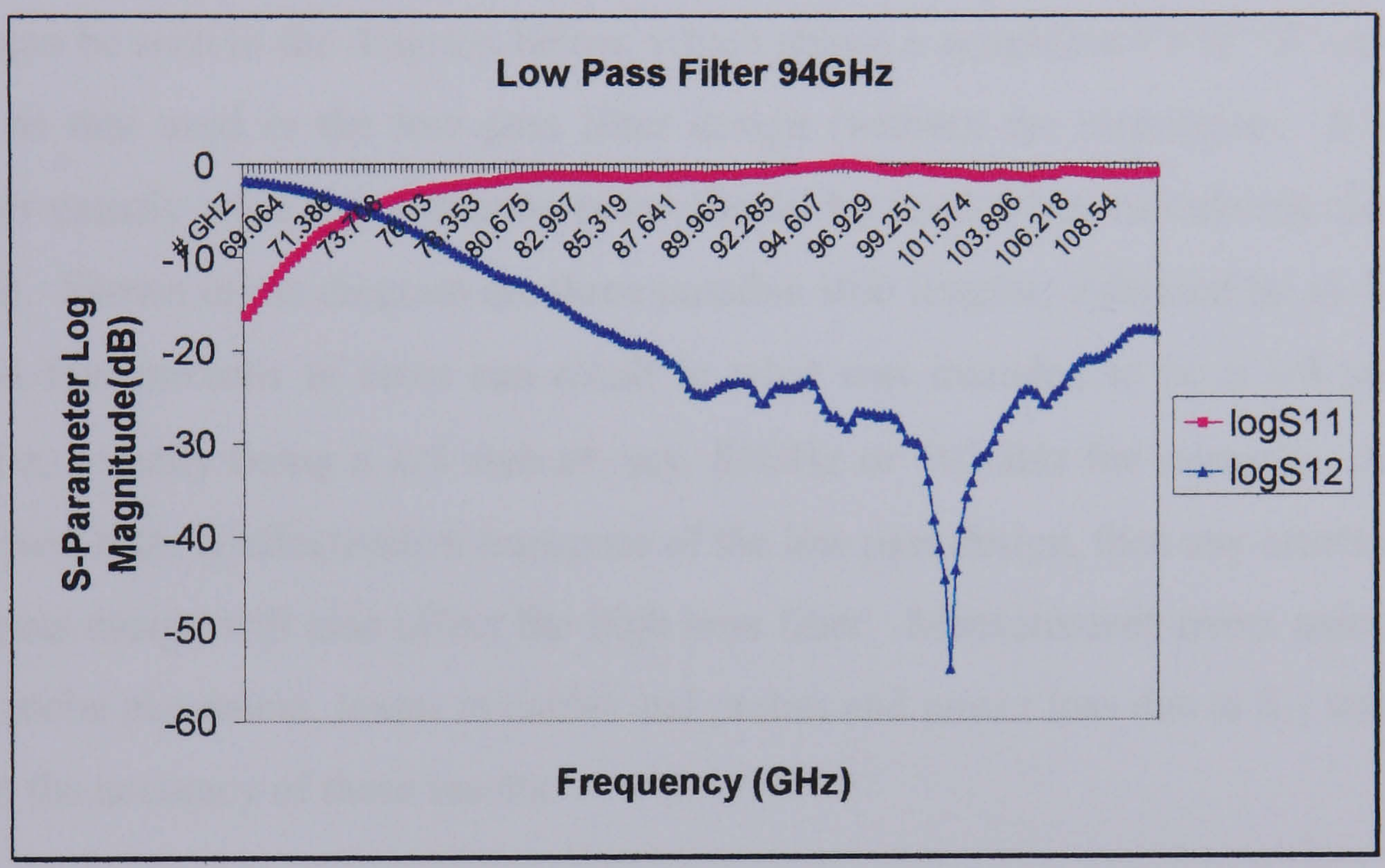


Figure 121 Low pass filter @ 94GHz

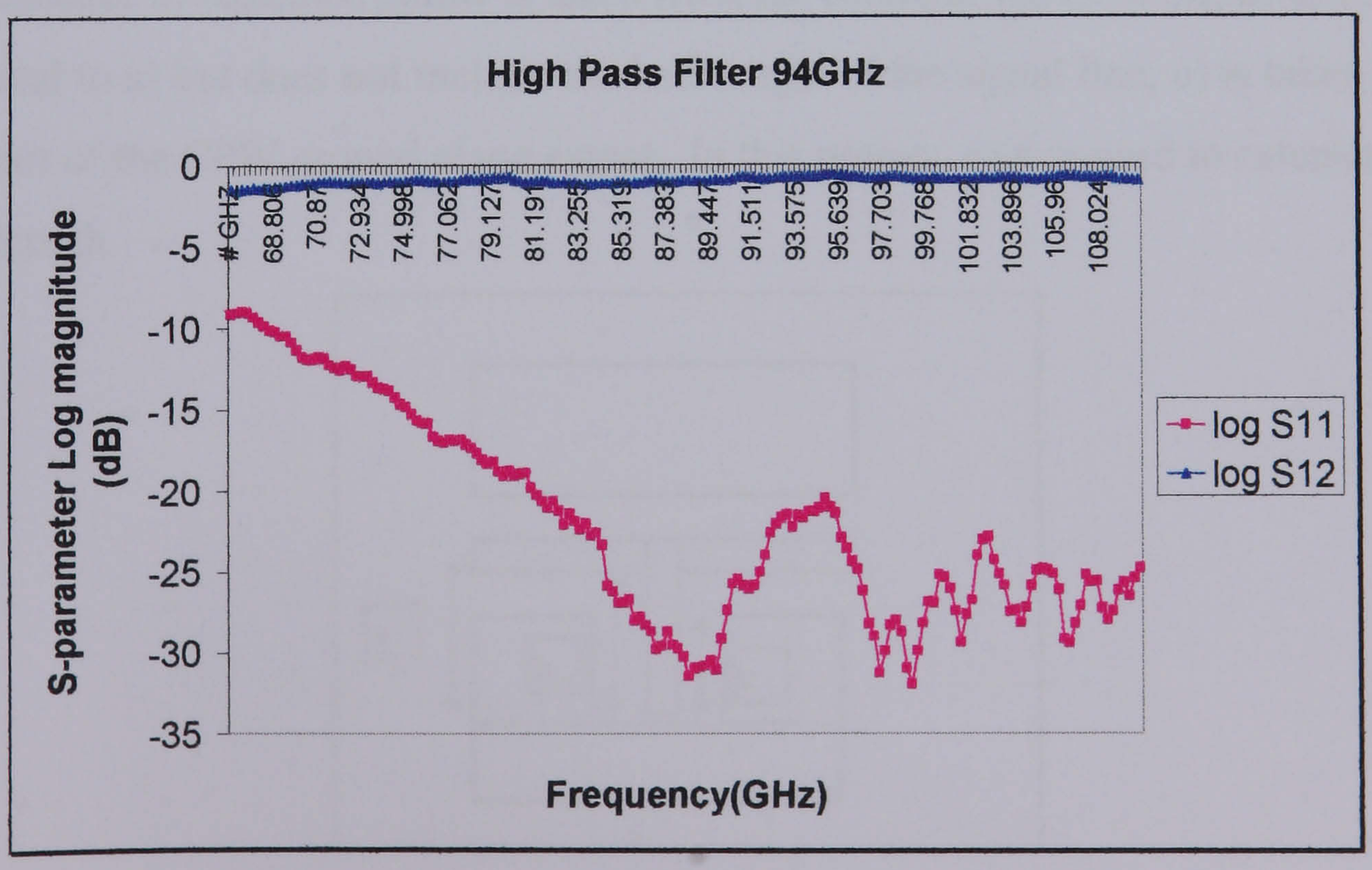


Figure 122 High Pass Filter @ 94GHz

From the plots in Figures 121 &122, the low and high pass filters broadly perform the functions that they are designed to do - the low pass filter rejects almost all of incident signal (S12 is -30dB @ 94GHz) while the high pass filter passes almost all of the incident signal (S12 is -0.8dB @ 94GHz). In the case of the low pass filter, the maximum signal filtering occurs at around 101GHz and not 94GHz. The reason for this is the uncertainty in exactly where to take as the starting point for the $\lambda/4$ open circuit stub.

This can be seen in the diagram below, which shows a simplified CPW "T" junction such as that used in the low pass filter design (without the airbridges). It is not known exactly what the reference point should be used when calculating the stub length. Shown in the diagram are three possible stub lengths, indicated by a), b) and c). A few microns of error can result in what was intended to be a $\lambda/4$ stub @ 94GHz, actually being a $\lambda/4$ stub at, say, 85GHz or 102GHz for example. As the high pass filter is effectively a transpose of the low pass design, then any errors in the low pass design will also affect the high pass filter. Measurement errors associated with probe placement, losses in cables and probes and power loss due to S_{11} will also affect the accuracy of these results.

The distance a) indicated below is taken from the centre of the CPW signal line; b) is identical to a) but does **not** include the half length of the signal line; c) is taken from the start of the CPW ground plane extent. In this project, c) was used to calculate the stub length.

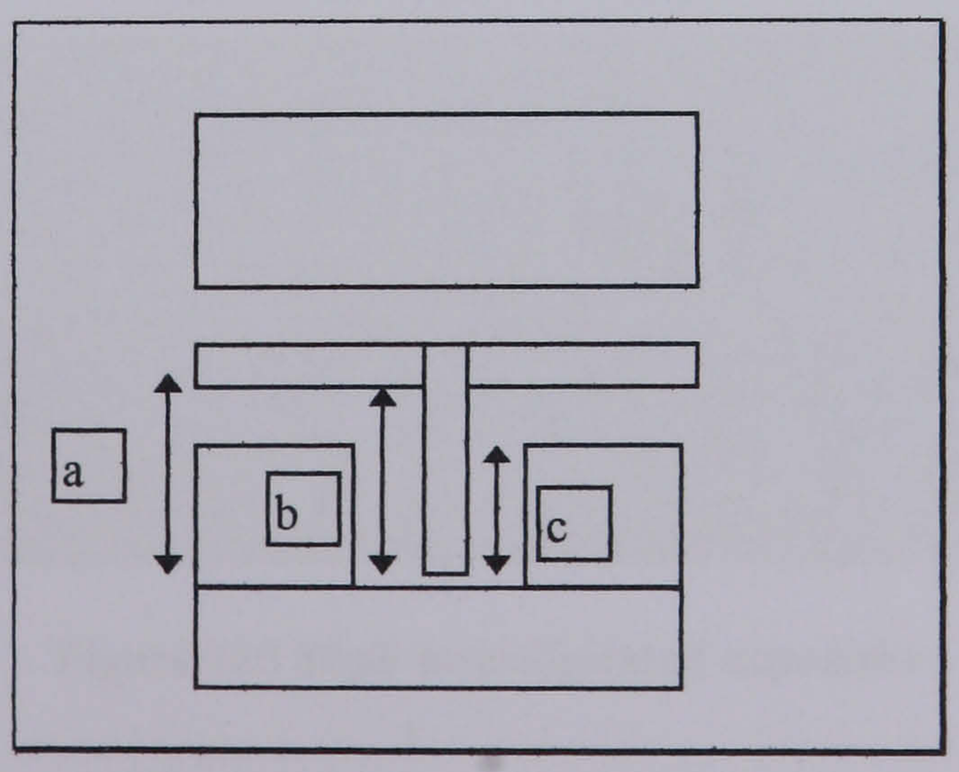


Figure 123 Simplfied diagram of CPW "T" junction

4.3.5 Capacitors

Shown below are colour photographs of the completed MIM and interdigitated capacitors used in the project. The design equations for these are given in section 2.8.5. Considerable work has been done on modelling MIM capacitors at the University of Glasgow [4.7]. Therefore little time was spent modelling these structures. Designed values for these capacitors were 80fF. Measured values of capacitance were 78fF for the MIM capacitor and 80fF for the interdigitated capacitor.

In the case of the MIM capacitor, the dimensions were:

From equation **(81)**, ε_r is 5.57 for Si_3N_4, ε_o is 8.85×10^{-12}, d is 150nm Si_3N_4, leaving the capacitor width to be 20μm and length 12μm.

In the case of the interdigitated capacitor, the finger length was 150μm, finger width was 2μm and spacing was 2μm.

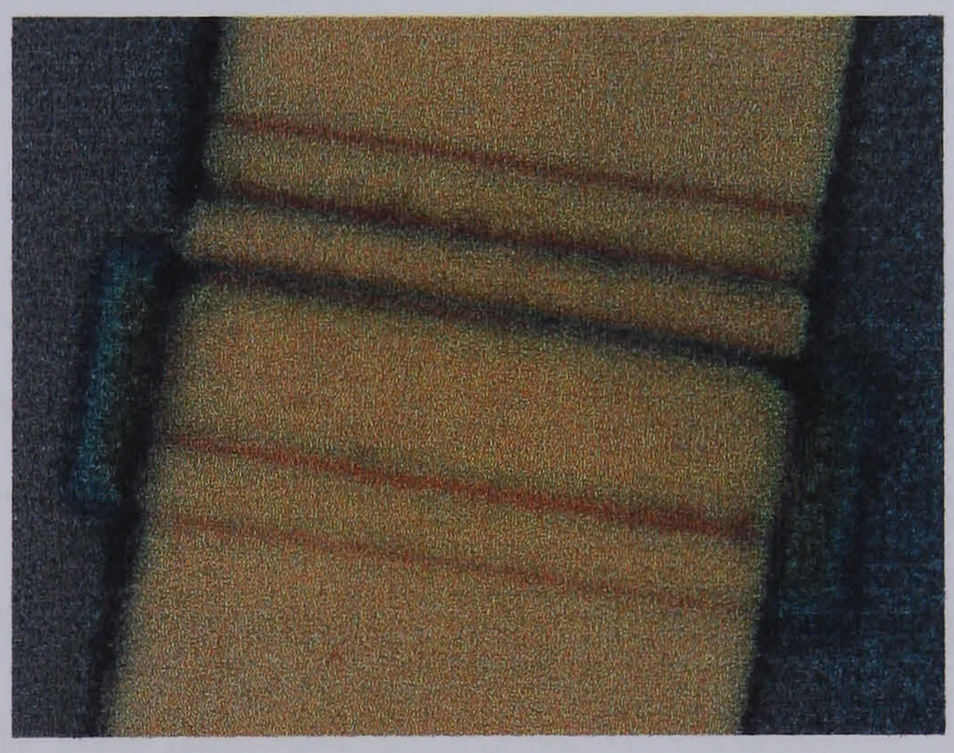


Figure 124 80pF MIM capacitor

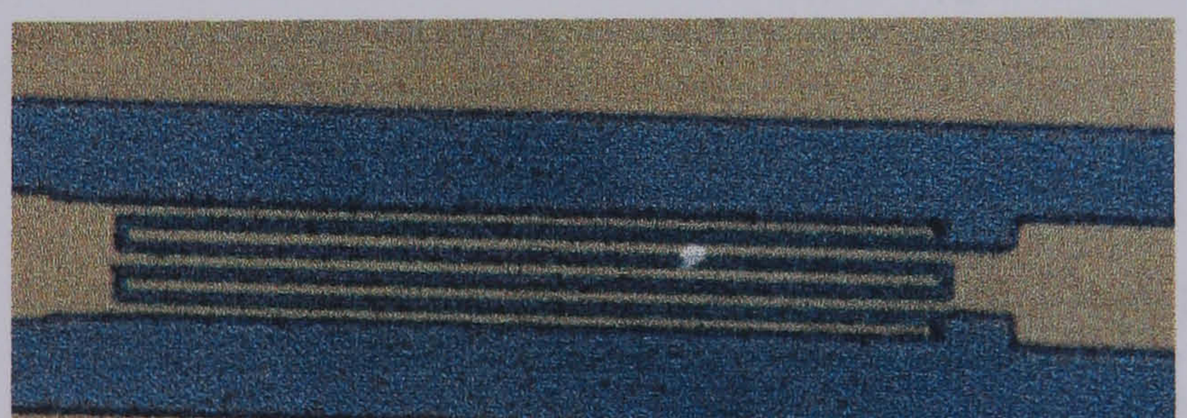


Figure 125 80pF interdigitated capacitor

4.4 mmWIC mixer testing

4.4.1 Introduction

Using the data obtained by testing individual diodes and passive circuit elements, several different mixers were designed, fabricated and tested. The initial approach adopted was to select the diode layout which gave the highest measured cutoff frequency. Therefore the mixers were based around dry-etched diodes, with anode length of 0.5μm, anode width of 10μm, with an anode -cathode spacing of 0.5μm. The number of anode fingers was **four**. Around these diodes, the standard circuit design shown in Figure 126 was designed. Initially, it was decided to employ the CPW-Slotline transition type A in these circuits for simplicity and to minimise chip size, although other transitions give lower insertion loss. It was necessary to have the three ports, RF, LO, and IF at 90^0 to each other due to the probe station layout. This same layout was fabricated on different layers to determine the effect that diode cutoff frequency/series resistance had on mixer conversion loss.

Although no nonlinear, microwave software was available to simulate the predicted mixer performance, two basic simulations were done to give an idea of possible mixer performance. The first of these was done using the simple SPICE program given in Appendix 4.A. Using values of Rs=2Ω and Cjo=8fF a mixer conversion loss of better than 10dB was possible at 5GHz IF frequency. However, it should be noted that only the section of the mixer indicated in Figure 126 was used for the simulation - no filters or CPW/Slotline transitions were included.

The output of this simulation is also given in Appendix 4.A. This plot shows the RF signal at 95GHz, the LO signal at 90GHz and the IF frequency at 5GHz. The difficulty in accurately simulating the CPW transmission line using this simple version of SPICE and the omission of any IF circuitry limit the accuracy of this simulation. However, taking the available RF input voltage at 95GHz (3.2mV) and the IF output voltage at 5GHz (1.1mV) and assuming RF and IF source impedances

of 50Ω, the conversion loss is then given by $10\log((V_{rf}^2)/(V_{if}^2))$, which works out at around 9.3dB.

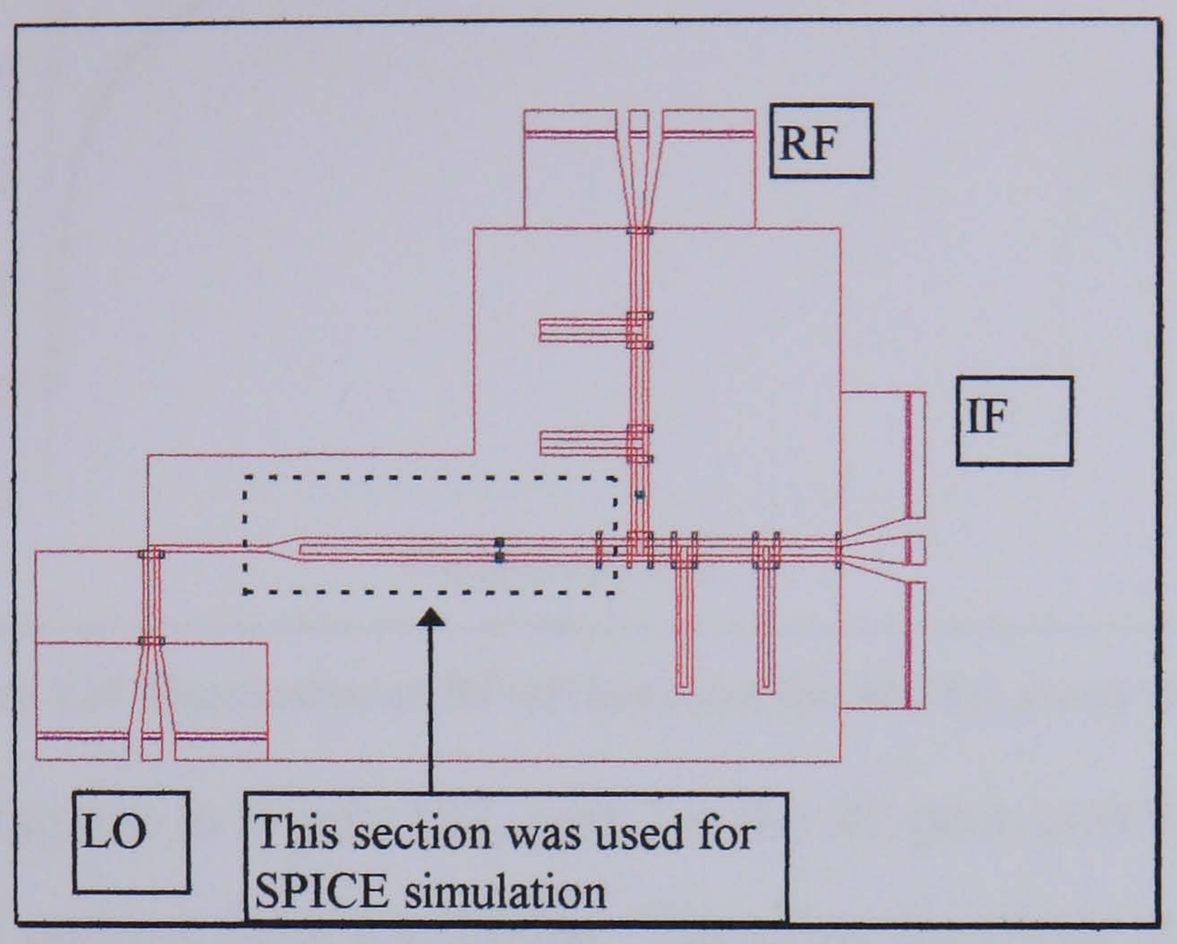


Figure 126 94GHz mixer layout -SPICE simulation

The second simulation evaluated the value of capacitance necessary to ensure RF-IF isolation. This simulation used TOUCHSTONE and the section of circuit shown in Figure 127 was modelled. This assumed that mixing takes place at the diodes and treated the circuit as a three port network. From this, a capacitance of 80fF provided an RF-IF isolation of greater than 20dB. This simulation is shown in Figure 128.

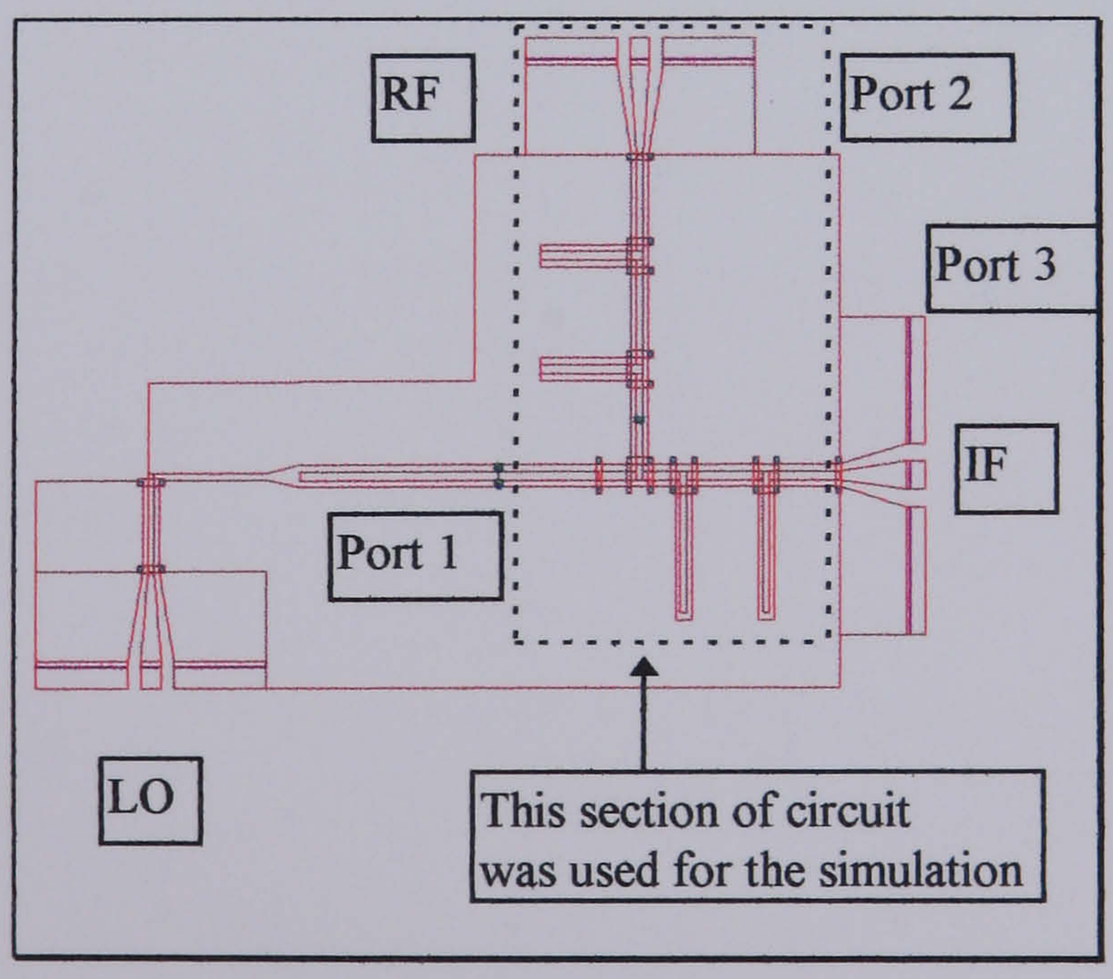


Figure 127 94GHz mixer layout TOUCHSTONE simulation

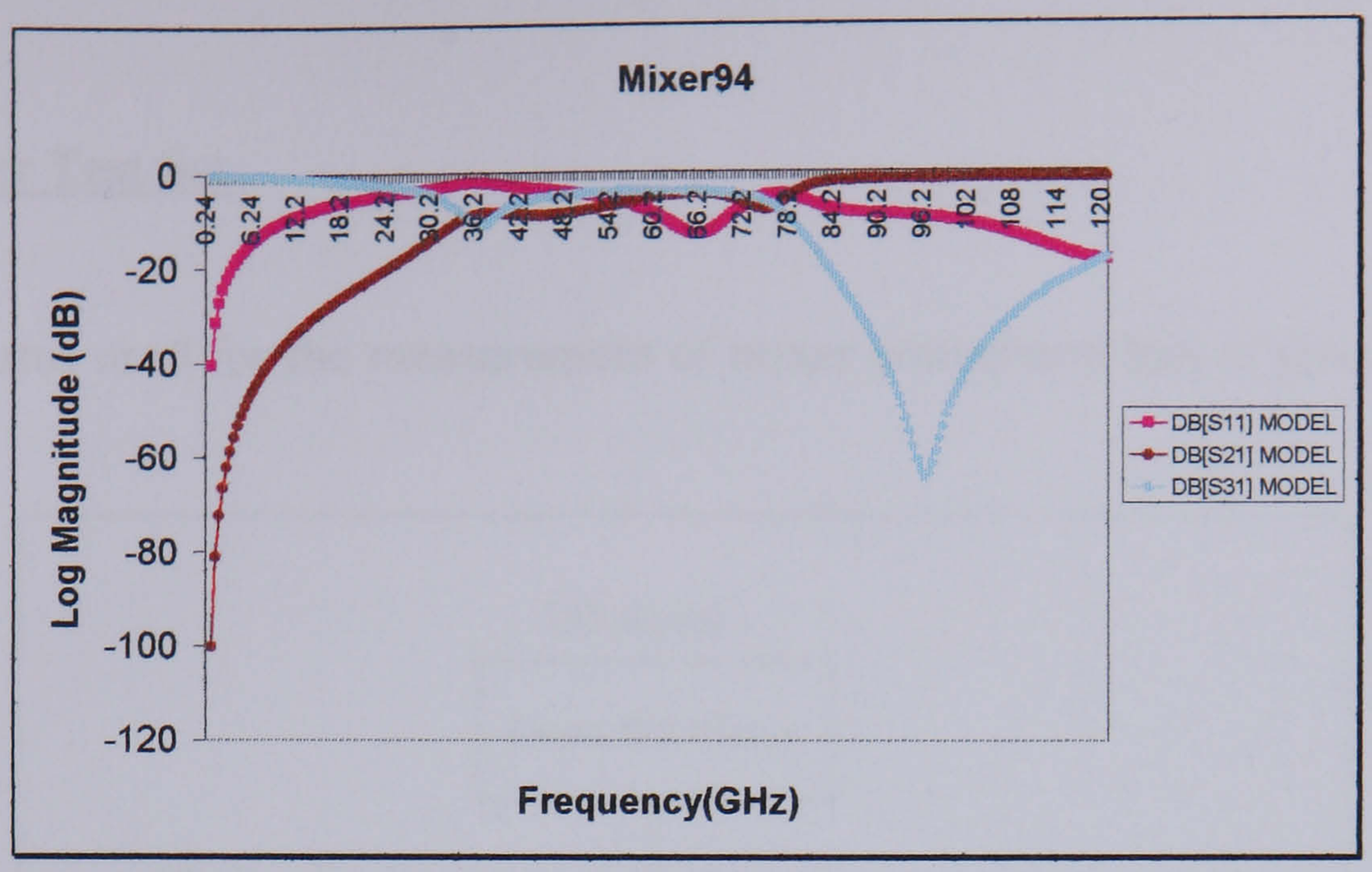


Figure 128 Simulation of RF-IF isolation for 94GHz mixer design

Referring to the diagram in Figure 127, port 2 is the RF port, port 3 is the IF port and port 1 is the signal coming from the diodes. Therefore the diode performance is not considered in this simulation.

4.4.2 Mixer Test Set

The apparatus used for the measurement of mixer conversion loss is given in Figure 129.

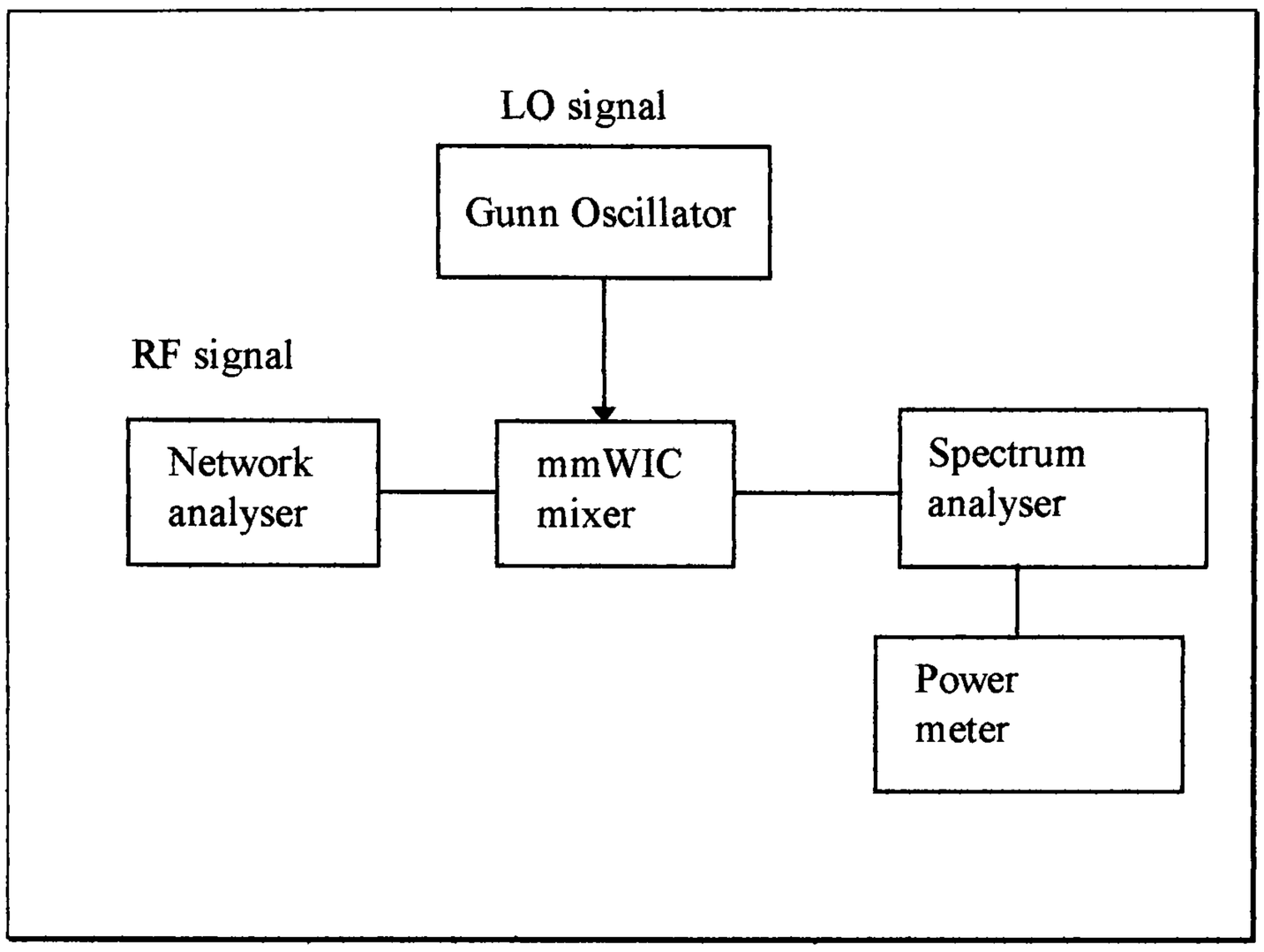


Figure 129 Mixer test setup

The RF input is provided from the W-Band test set. The power level at 94GHz was -15dBm. The LO signal was provided from a Gunn oscillator (Farran Technology), capable of providing up to 16dBm output power, with a centre frequency of 94GHz+/-1GHz. The output IF signal was read using a power meter (HP 437B), whilst the spectrum analyser indicated where mixing signals existed.

4.4.3 Completed circuits

Colour photographs of two completed mixer circuits are given overleaf. The circuit shown in Figure 130 uses the CPW-Slotline transition type A (see Section 2.8) and is identical in design to that shown in the WAM layout of Figure 26. The circuit shown in Figure 131 varies from that of Figure 130 in the following ways:

1) Interdigitated capacitor instead of MIM.
2) CPW-Slotline transition is identical to transition type C, but with no 90^0 bend.

3) Diodes are placed exactly at the Slotline-to-CPW junction instead of λ/2 from the junction
4) Filters are more compact

Thus this comparison illustrates how the basic circuit of Figure 130 can be made more compact.

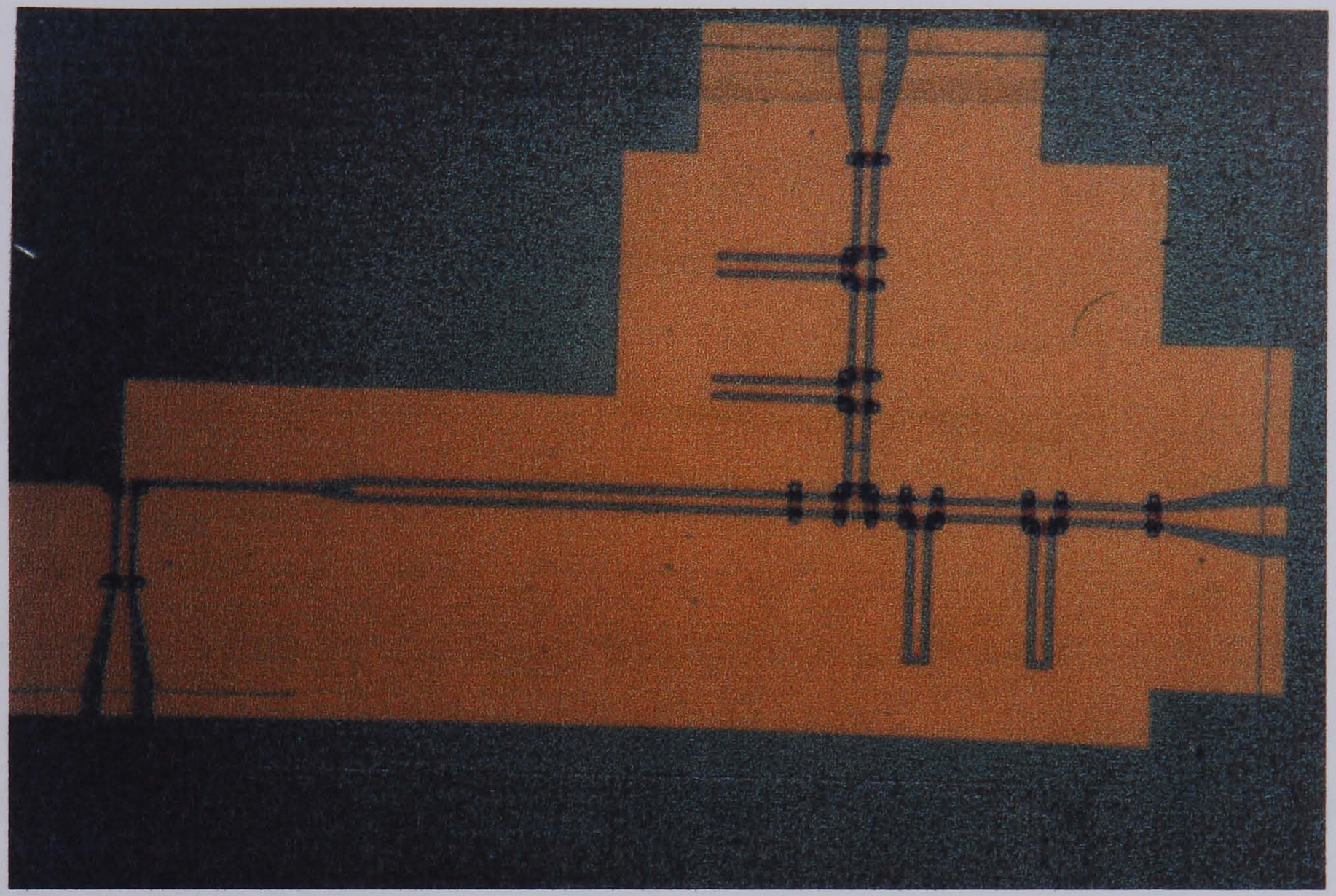


Figure 130 94GHz mixer

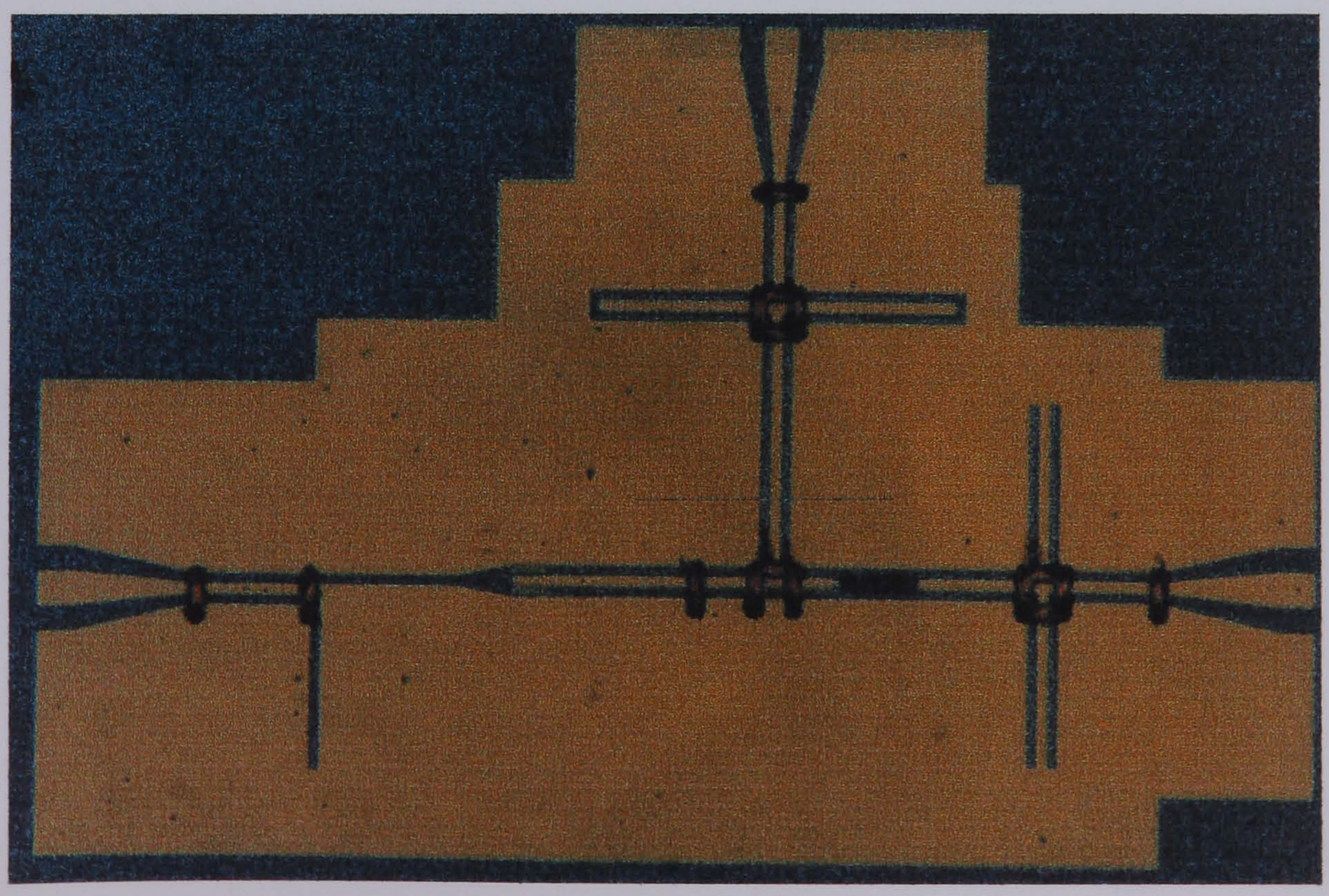


Figure 131 94GHz mixer layout

4.4.4 Testing

Conversion loss was calculated using the knowledge that RF input power was -15dBm, and that the total loss due to probes and cables was 1.4dB. Therefore, the output IF power could be read from the spectrum analyser, confirmed using the power meter, and after taking into account the cable/probe losses, the mixer conversion loss was calculated using the formula given in (**38**), which states that conversion loss is the available RF input power divided by the IF output power. No correction was made for S_{11} - the conversion loss should be reduced if correction is made for S_{11}. No correction was made for possible errors in the spectrum analyser, although the power level was confirmed using a HP power meter. There was good agreement between these two values.

Figure 132 shows the results of the testing of the mixer circuit shown in Figure 130 on pHEMT layer A1158, with four-finger diodes. The LO frequency was fixed at 93GHz, with a maximum LO power of 15 dBm, whilst the RF frequency was varied so as to vary the IF frequency.

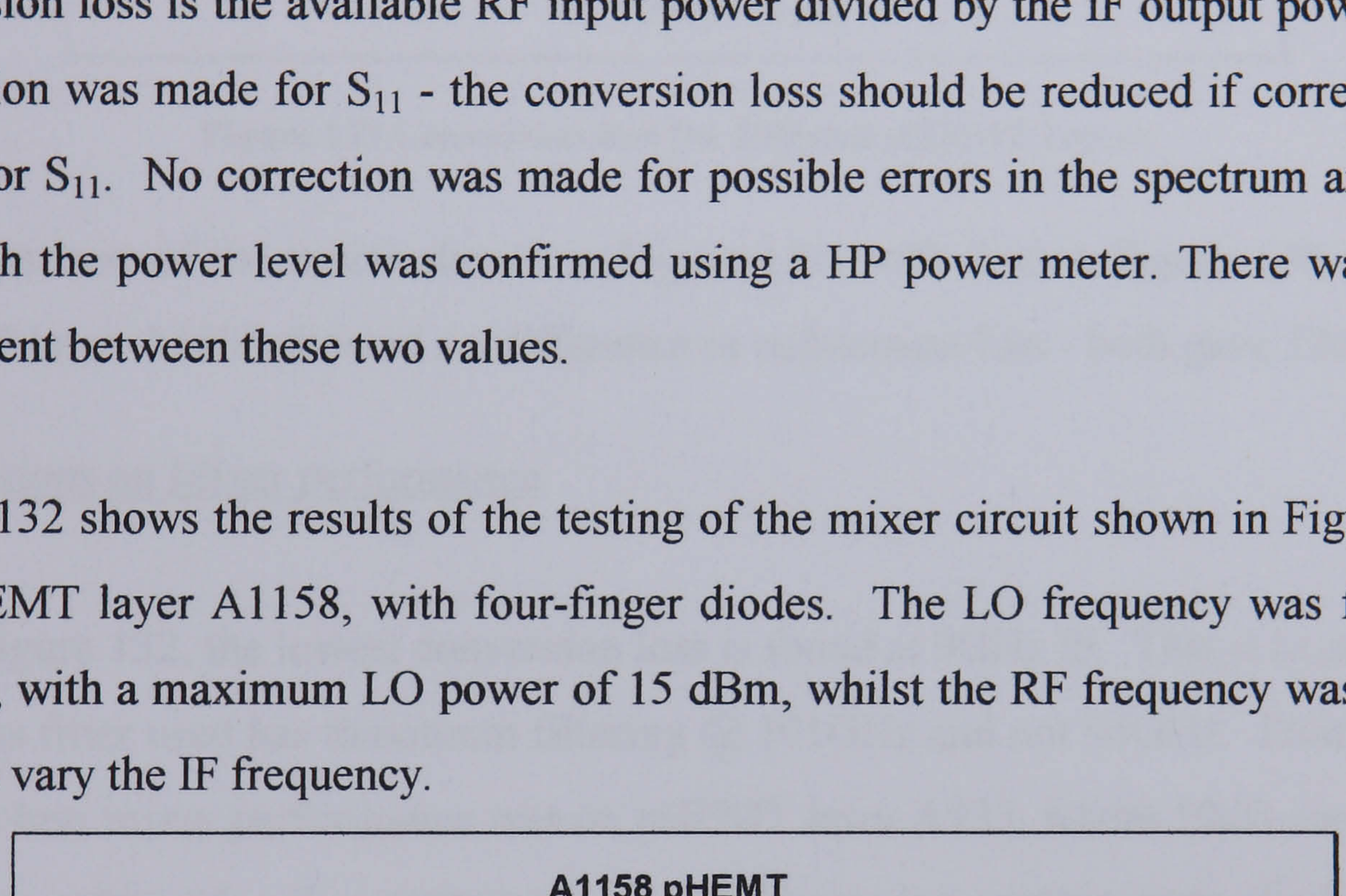


Figure 132 Conversion Loss versus IF frequency A1158

Shown in Figure 133, for the same mixer design is the conversion loss for a fixed IF frequency of 5GHz, LO frequency 94GHz, LO power 15dBm for a number of different pHEMT substrates.

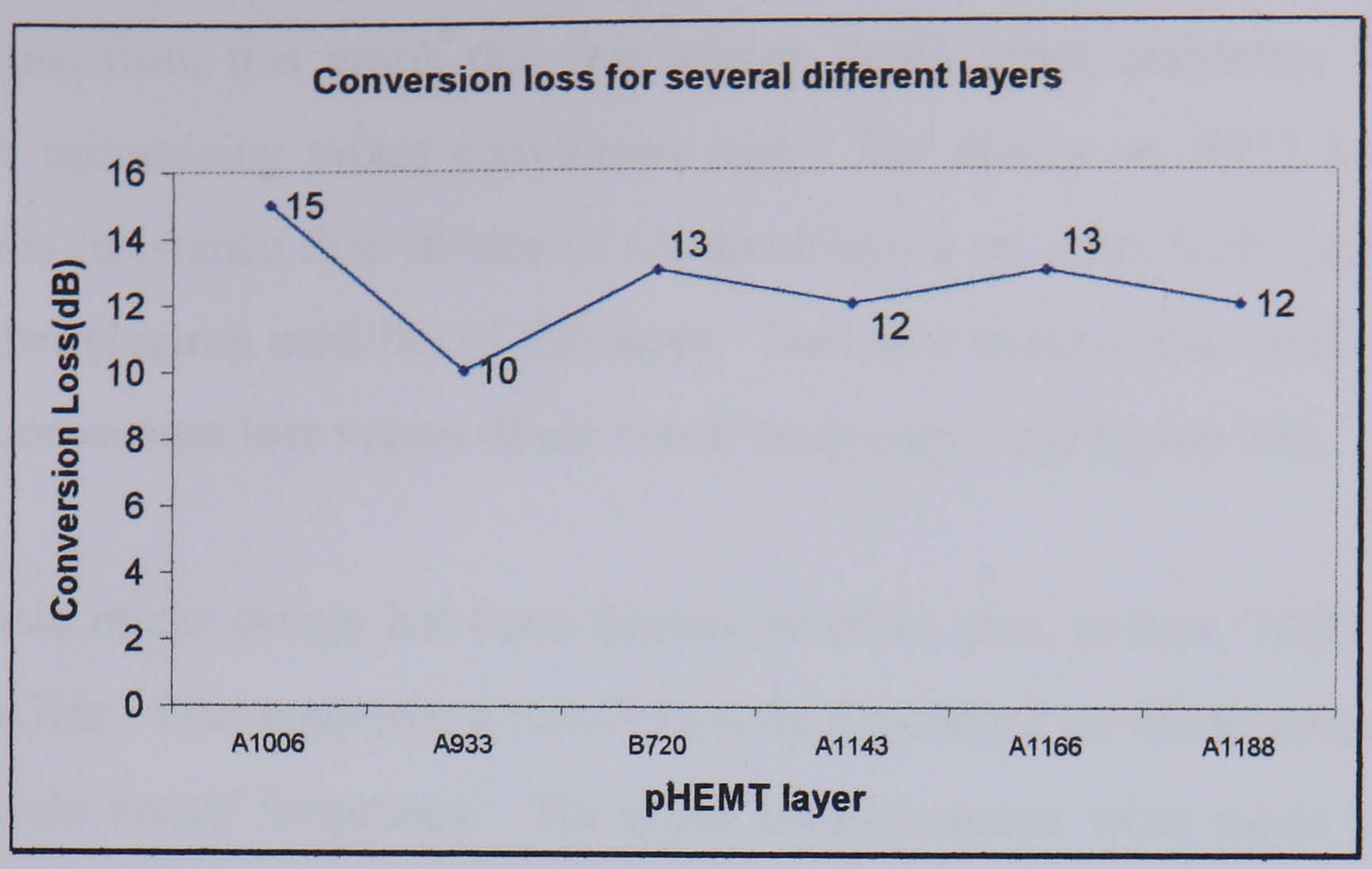


Figure 133 Conversion loss for different pHEMT Layers

A comparison of the mixer shown in Figure 131, with that in Figure 130 both on pHEMT layer A1188 showed no difference in conversion loss - both gave 12dB.

Conclusions on Mixer performance

From Figure 132, the lowest conversion loss is found at 9GHz IF. This is because the low pass filter used has maximum filtering @ 101GHz and not 94GHz. From Figure 133 the best mixer performance was on pHEMT layer A933, where 10dB conversion loss was achieved. A comparison of conversion loss versus both diode cutoff frequency and series resistance is useful.

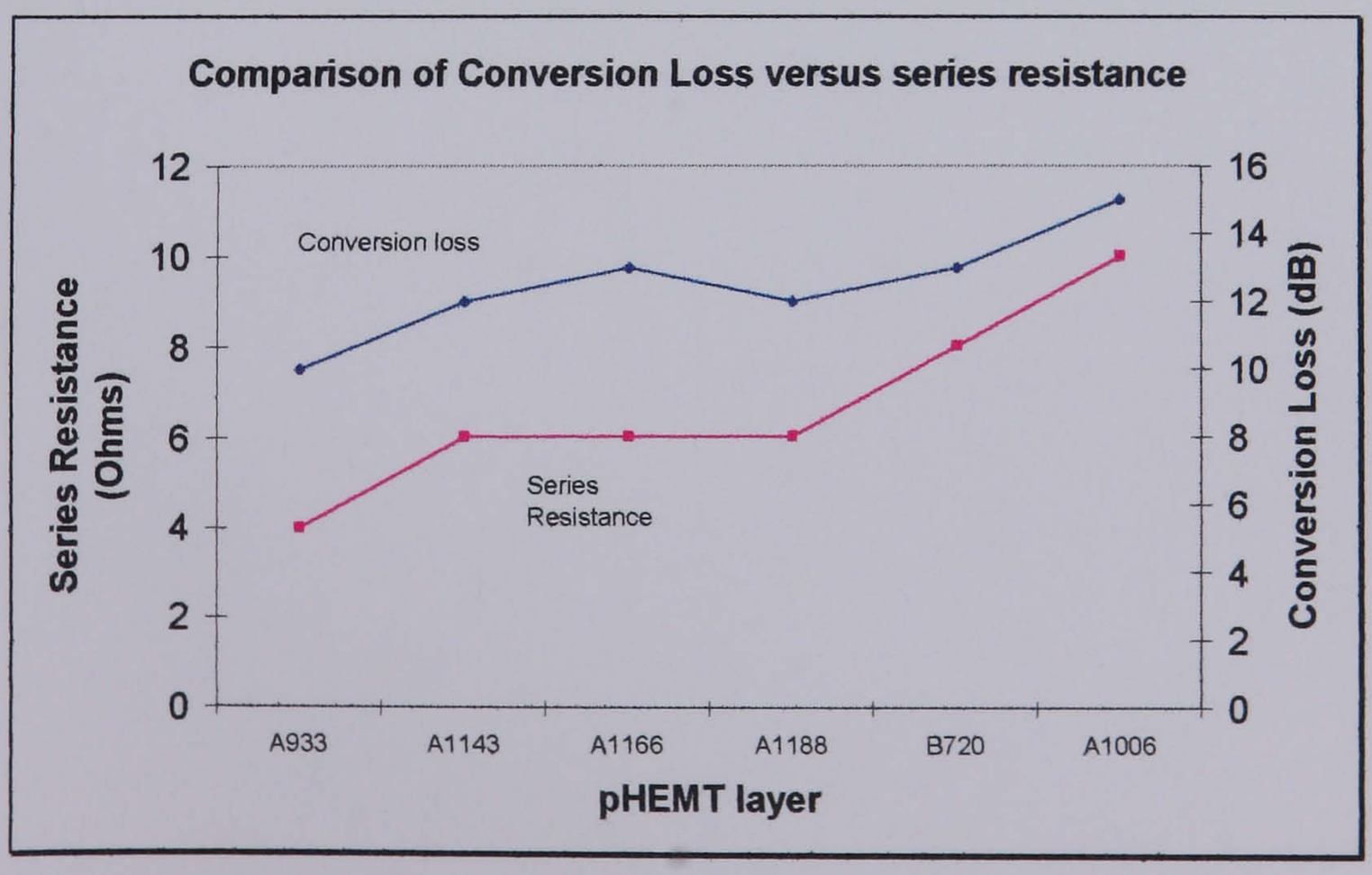


Figure 134 A comparison of measured conversion loss versus diode series resistance

It is obvious from this graph that minimising diode series resistance has a direct impact on minimising mixer conversion loss. The diodes on A933 have a lower diode series resistance than diodes of identical layout on other MBE layers because of the higher electron mobility of this layer. The same trend is also evident for a plot of mixer conversion loss versus diode cutoff frequency - see Figure 135.

So this basic mixer design has been demonstrated to give, at best, 10dB conversion loss @ 94GHz. This conversion loss is heavily dependant on diode series resistance and so diode cutoff frequency. No noise measurements were made so it is not possible to assess the noise figure of this device.

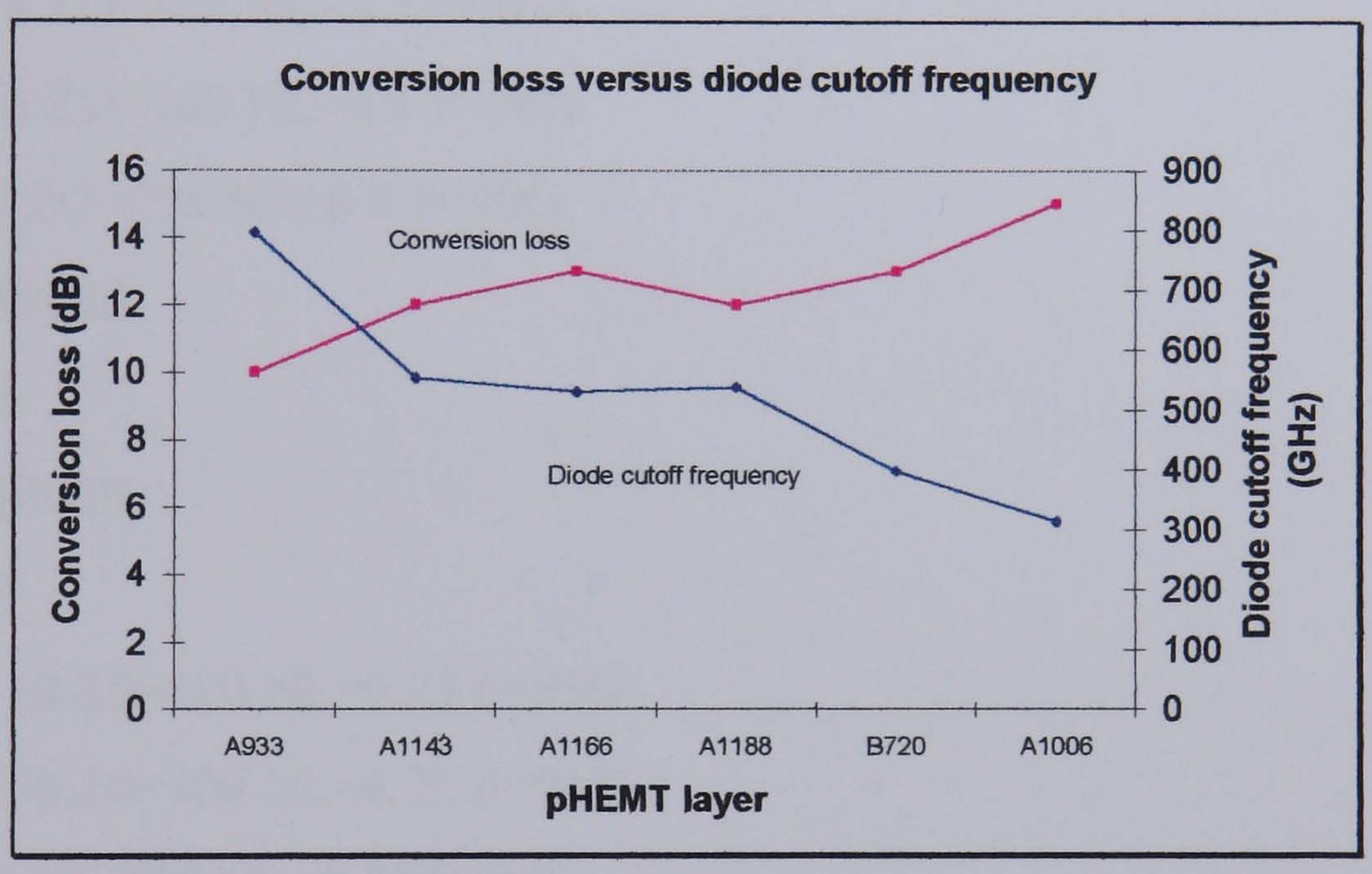


Figure 135 Mixer conversion loss versus diode cutoff frequency

APPENDIX 4.A

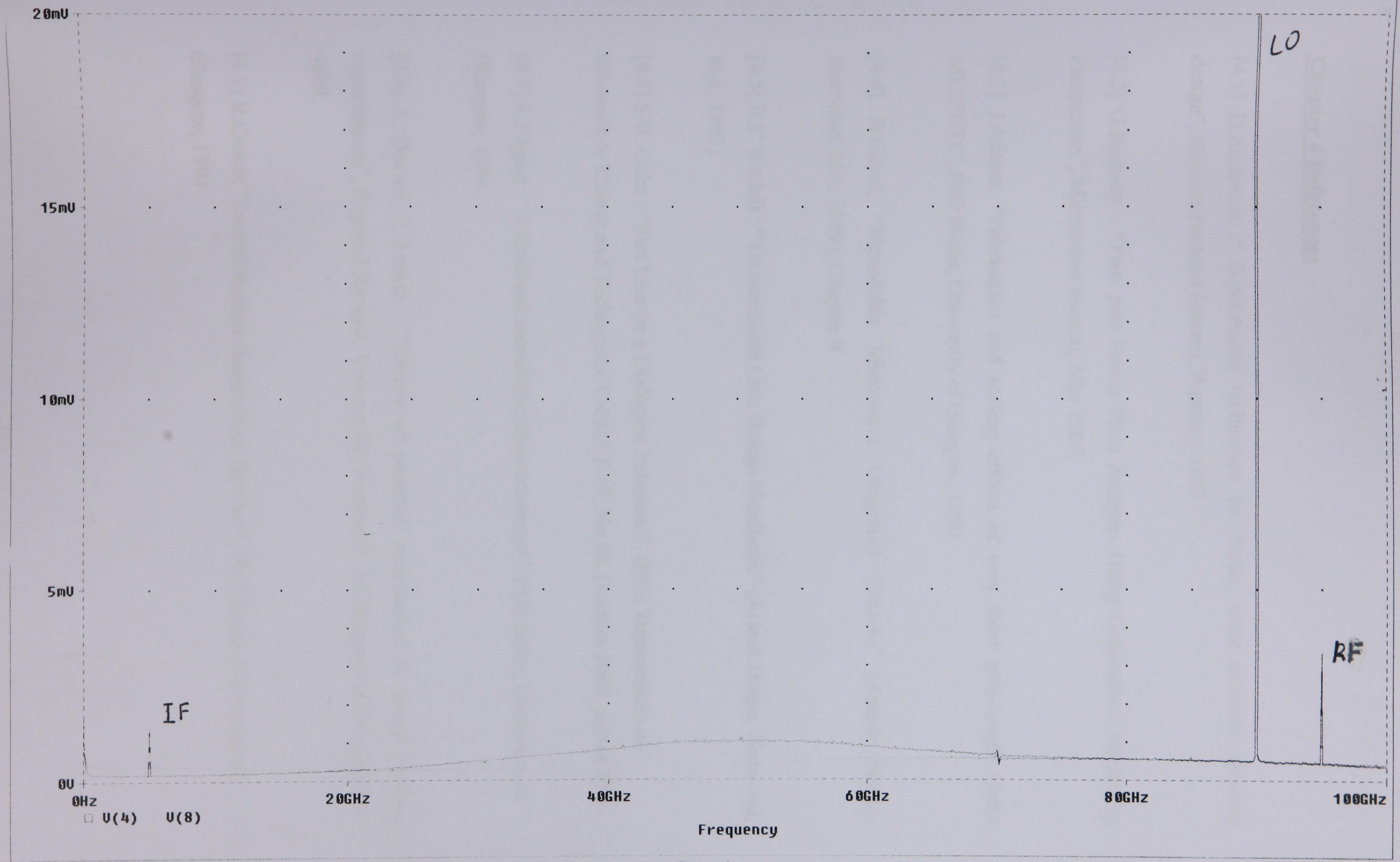
```
.model DMIXER D(Is=60p N=1.15 Rs=2 Xti=2 Eg=.75 Cjo=8fF Vj=.65)

Vrf 1 0 SIN(0.0 0.01 95e9 0 0 0)
Vlo 21 0 SIN(0.0 1.0 90E09 0 0 0)

RRF 1 3 110
CT1 4 0 1.5F
CT2 4 3 1.5F
TM1 3 4 7 8 ZO=100 NL=0.5 F=90G
TM2 4 0 8 0 ZO=100 NL=0.5 F=90G
TP1 3 0 7 0 ZO=220 NL=0.5 F=90G
D1 7 8 DMIXER
CD1 7 8 4F
D2 8 0 DMIXER
CD2 8 0 4F
TM5 7 8 9 10 Z0=100 NL=0.25 F=95G
TM6 8 0 10 0 Z0=100 NL=0.25 F=95G
TP3 7 0 9 0 Z0=220 NL=0.25 F=95G
CLO 20 10 1N
RLO 21 20 50
CS 91 0 1N
RS 9 91 0.5

.OP
.TRAN 1P 1N 0 0.5P.
.PROBE
.END
```

Date/Time run: 12/13/99 20:30:23

94GHz CPW/Slotline mixer

Temperature: 27.0

(B) MIXER94.DAT



Date: December 13, 1999

Page 1

Time: 20:54:50

Chapter 4 References

[4.1] D.Anderson :" S-parameter techniques for faster, more accurate network design", Hewlett-Packard Journal, February 1967.

[4.2] G.Bodway : "Two port Power Flow Analysis Using Generalised Scattering Parameters", Microwave Journal, May 1967

[4.3] J.Adams, "Fabrication and scaling effects of very short gate-length GaAs MESFETs", PhD thesis, University of Glasgow, 1990.

[4.4] R.Goyal, "Monolithic Microwave Integrated Circuits" (Artech House, Norwood, MA, 1989), Chapter 9

[4.5] B.C Wadell : "Transmission Line Design Handbook" (Artech House, Norwood, MA, 1991).

[4.6] S.B. Cohn : "Slot Line on a Dielectric Substrate", IEEE Transactions on Microwave Theory and Techniques,Vol.MTT-17, No.10, October 1969, pp768-778.

[4.7] K.Elgaid : "A Ka-Band monolithic downconverter", PhD thesis, University of Glasgow, 1998.

[4.8] J. Davies, I. Larkin : "Theory of potential modulation in lateral surface superlattices", Physical Review, Volume 49, Number 7, 15 February 1994, pp 4800-4809.

[4.9] R.Cusco: "Lateral Surface Superlattice Devices", PhD thesis, University of Glasgow, 1994

[4.10] G.H. Robinson, J.L. Allen: "Slotline Application to Miniature Ferrite Devices", IEEE Transactions on Microwave Theory and Techniques, Vol.17, 1969, pp 1097-1101.

[4.11] K. Elgaid, D. Edgar, S. Broadfoot, S. Ferguson, M. Taylor, S. Beaumont :"Compact low loss coplanar waveguide to slotline transition for mmWIC applications" - Electronics Letters, 29th August 1996, Vol.32, No.18, pages 1677-1678

Chapter 5

Conclusions and Future Work

5.1 Summary of achievements

5.1.1 Introduction

The aims of the project were:

a) to demonstrate a novel, high frequency monolithic mixer design, capable of ultimate integration with a low noise amplifier to form a complete monolithic downconverter.

b) to develop a high yield fabrication process for this simple mixer design which should be compatible with LNA processing.

c) Conversion loss should be 10dB (worst case) so that the eventual integration with a high-gain LNA allows overall conversion gain of the downconverter.

5.1.2 Achievements

a) A high yield, simple, novel mixer design has been successfully implemented with performance comparable to any of the passive mixers described in the literature (see Chapter 1). As many as 40 working mixers were successfully fabricated and measured out of a possible 50. The mixer fabrication process is compatible with FET processing enabling ultimate integration with FET amplifiers.

b) The considerable work done on the design, layout and modelling of mmWIC diodes, along with the attempts to analyse sources of series resistance, demonstrate the benefits of the monolithic approach to circuit design. The knowledge exists for the circuit designer to tailor the diode to his requirements rather than the "hybrid" approach where the designer will use a diode of given specification and then use matching circuits to complete the design.

c) The use of Coplanar Waveguide instead of microstrip considerably simplifies the fabrication process by eliminating the need for via holes. In addition, the use of a CPW-Slotline transition instead of a hybrid coupler to achieve RF-LO isolation reduces chip size.

d) The first reports of CPW-Slotline transitions being characterised at W-Band are given in this thesis. Although equations in the literature for Slotline characteristic impedance are not valid for 400μm GaAs substrates, some understanding of the parameters affecting transition loss has been achieved.

e) Investigation of the existence of "strain" resistance (this would also be relevant to FET performance) showed that if it does exist, then it is so small as to be negligible.

f) Considerable optimisation of the existing University of Glasgow fabrication process was carried out. The main areas of development were:

   i) Evaluation of different ohmic contact recipes for GaAs pHEMTs, showing that a Ni/Ge/Au/Ti/Au combination (Ni contacting the substrate) gave a contact resistance of 0.08Ωmm over 4 samples, significantly less than the average of 0.15Ωmm obtained using the existing process.

   ii) Modification of the anode/gate level to include "pyramidal" shaped anodes using the tri-layer resist scheme, thus enabling both "T-gates" to be written at the same layer as pyramidal shaped anodes.

   iii) Development of a new "T-gate" process, using an additional layer of copolymer resist to enable thicker metal to be used thus reducing metallic gate resistance.

   iv) Investigation of the possible existence of a strain resistance, caused by the anode metallisation on the semiconductor surface, showed that such resistance was negligible. This is an interesting result as it eliminates a possible source of resistance from the diode model shown in Figure 30.

5.2 Suggestions for future work

There is considerable potential to continue the research which forms this thesis. Ideas for future work are now given:

a) The design of a high gain LNA and ultimate integration with this mixer to form a downconverter would then enable a comparison with direct detection systems to be carried out. A three-stage LNA (InP) has been demonstrated at the University of Glasgow [5.1] and transfer of this design to GaAs should be possible. This LNA design could be modified to include additional stages (probably at least a six-stage LNA) for use in the direct detection system.

b) Integration of a slot antenna with the mixer to form a receiver mmWIC. It would be possible to apply the incoming RF signal to the slot antenna, enabling the balanced CPW mode to be excited directly from antenna-to-slotline-to-CPW rather than via a CPW-Slotline transition. In this instance the RF and LO signals would effectively be interchanged from the designs shown in Figure 130 and 131.

c) A new material structure was designed and grown by MBE at University of Glasgow [5.2] to allow the complete fabrication of a downconverter on a material structure that is optimised for BOTH diodes and FETs. This material structure is shown in Figure 136.

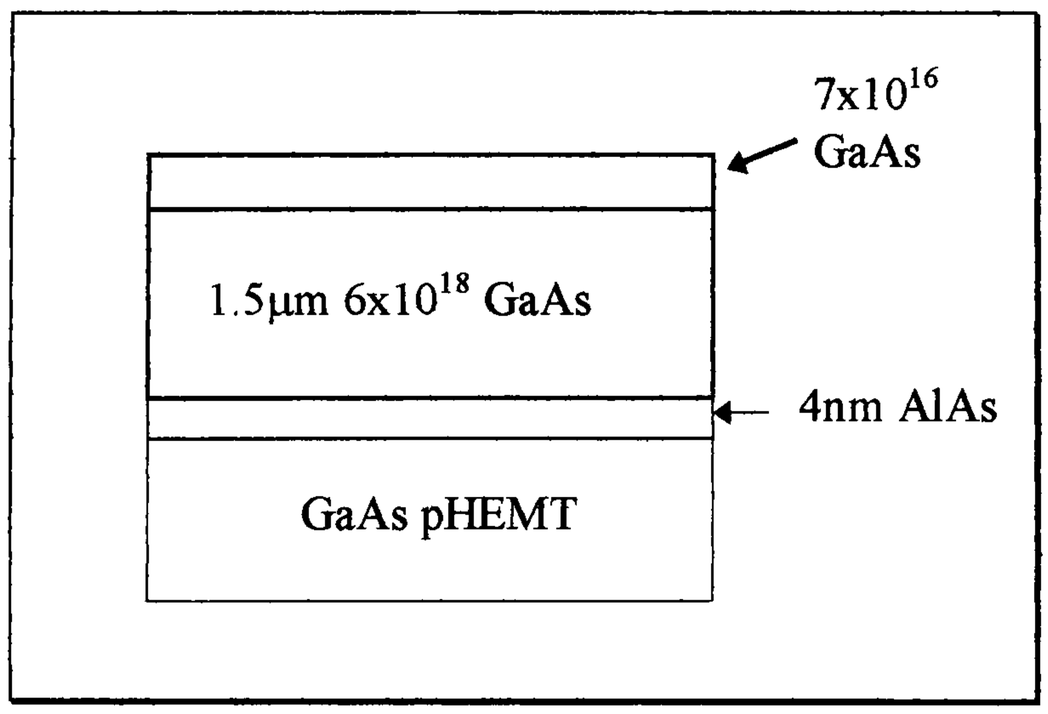


Figure 136 New material structure for mmWIC downconverter

The fabrication process for such a structure would involve more steps than a simple pHEMT substrate. The basic idea is to form the diode using the thin lightly doped GaAs layer for the anode contact and the thicker, heavily doped GaAs for the ohmic

contact. The thin AlAs etch stop layer could then be removed using Buffered Hydrofluoric Acid and the subsequent processing is identical to that of a FET process. Both Wet and Dry etch techniques could be used to remove the excess diode material. Therefore the fabrication process would be as follows:

1) Alignment marks for diodes.
2) Schottky contact anode formation.
3) Etch off the thin epitaxial layer ($7x10^{16}$ GaAs) using wet etch.
4) ohmic contact formation.
5) Etch off the thick layer of heavily doped GaAs using dry etch ($SiCl_4/SF_4$).
6) Remove the etch stop layer using Buffered HF.
7) From here use the normal University of Glasgow FET process.

One obvious disadvantage of this process are the additional steps introduced by forming the diodes and FETs separately. The addition of these extra process steps would have to be justified by a significant increase in circuit performance. The diode layout would be as shown earlier in Figure 27. Planarisation may also be necessary to enable the interconnection of diodes and FETs (since the diodes would be effectively on a 1.5μm mesa).

In conclusion, a novel, high frequency monolithic mixer design has been successfully demonstrated. In addition, a mmWIC fabrication process is now available which will allow integration of this mixer with RF/IF amplifiers to form a complete monolithic downconverter.

Chapter 5 References

[5.1] D.Edgar, H.McLelland, S. Ferguson, N.I. Cameron, M. Holland, I.G. Thayne, M.R.S Taylor, C.R. Stanley, S.P. Beaumont, "150GHz InP Coplanar Waveguide Amplifier", 29th European Microwave Conference, Munich, 1999.

[5.2] H.C. Huang, P. Laux, J.F. Bass, S.W. Chen, T.T. Lee, S. Tadayon, J.L. Singer, J. Kearney, O.A. Aina : "A W-Band Multifunction MMIC"- 1994 IEEE Microwave and Millimeter-wave monolithic Circuits symposium, pages 37-40.