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VLSI-COMPATIBLE PROCESSING AND LOW-VOLTAGE OPERATION OF MULTIEMITTER Si/SiGe HETEROJUNCTION BIPOLAR TRANSISTORS

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Previously we demonstrated a new class of VLSI-compatible multiemitter Si/SiGe/Si *npn* HBTs with enhanced logic functionality. These devices have two (or more) emitter contacts and no base contact. Given a potential difference between any two emitter contacts, one of the emitter-base junctions is forward biased and injects electrons into the base, while the other junction is reverse biased and small controlling current flows by interband tunneling. Because of emitter contact symmetry, the device possesses exclusive *or* functionality. Our first devices provided current gain of ~400 at room temperature, at an operating voltage of ~2 V. Here we present an improved version that operates at 1 V, as well as a multiemitter HBT fabrication sequence that is not only fully compatible with a VLSI BiCMOS process, but even saves several processing steps compared to a standard HBT.

1. Multiemitter HBT Devices

As microelectronic circuits progress towards greater integration, increasing device functionality and decreasing fabrication complexity is crucial. Many proposed systems-on-a-chip combine standard CMOS transistors with enhanced functionality single-electron or tunneling devices, without addressing the exotic materials, nonstandard fabrication or the disparate operating regimes (such as cryogenic temperatures) that many of these devices require. For these reasons, the introduction of such novel devices into mainstream technology in the foreseeable future appears rather unlikely.[1] On the other hand, any device that offers higher performance or functionality that can be inserted into a standard VLSI process takes on considerable technological interest. Hence the rapid acceptance of Si/SiGe heterojunction bipolar transistors (HBTs) that require only minimal modification of standard silicon bipolar processing.

Recently we have demonstrated a multiemitter Si/SiGe HBT variant that is VLSI-compatible, possesses enhanced logic functionality, and yet retains the attractive HBT features of high current gain and very narrow base (promising high-speed operation).[2] The multiemitter HBT was originally proposed in 1994 by Gribnikov and Luryi in the

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Si/SiGe material system[3] and, independently, by Imamura and co-workers in III-V materials.[4] We will consider the operating principles underpinning the multiemitter HBT with the help of Figs. 1 and 2. The schematic layer sequence and cross-section of the *npn* Si/SiGe/Si device is illustrated in Fig. 1(a): two (or more) contacts are fabricated to the *n*-Si emitter and then isolated from each other, so a current between any two emitter contacts can only flow via the base. There is no direct contact to the heavily doped *p*-SiGe base, but there is a standard collector contact. Then, as in Fig. 1, let us ground one emitter and apply a reasonably large positive voltage V_{E2} to the other emitter, as well as a positive collector voltage V_C. The emitter-base junction of the first emitter will be forward-biased and the usual large injected electron current I_{E1} will flow, mostly reaching the base-collector junction and contributing to the collector current I_C. As in a standard HBT, a small fraction of the injected electron current will recombine with the holes in the base, but instead of an ohmic base contact, this hole base current I_{E2} is supplied by interband tunneling in the second, reverse-biased emitter-base junction – see Fig. 1(b). The distribution of V_{E2} between the two junctions (i.e. the potential of the floating base) is determined by the current gain β. Assuming the emitters are identical in area:

$$I_{E1} \approx I_C = \beta I_{E2} \tag{1}$$

The current gain β depends, as in a standard HBT, on the emitter-base doping and the additional valence band barrier due to the Si/SiGe heterojunction. The truly unknown quantity is interband tunneling current I_{E2} in the reverse-biased emitter-base junction. Although this is a problem dating back to the discovery of the tunnel diode by Esaki,[5] there exists at this time no satisfactory quantitative model. The difficulty lies in the fact that in Si-based materials the tunneling is indirect (between states close to the Γ-point in the valence band of the base and the electron dispersion minima in the emitter) and hence requires a large change in momentum due to phonons or impurity scattering, leading to the appearance of adjustable parameters in the expression for the tunneling current.[5,6]

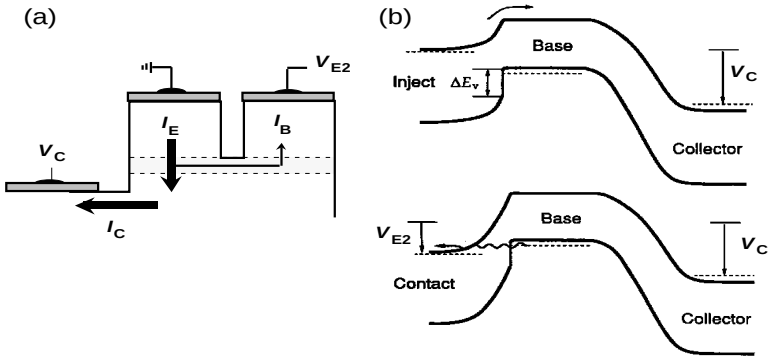

Fig. 1. (a) Schematic layout of the multiemitter *npn* Si/SiGe/Si HBT, with one emitter grounded and the other at a positive bias V_{E2}. (b) Corresponding potential diagrams of the forward-biased (injecting) and reverse-biased (tunneling contact) junctions under bias.

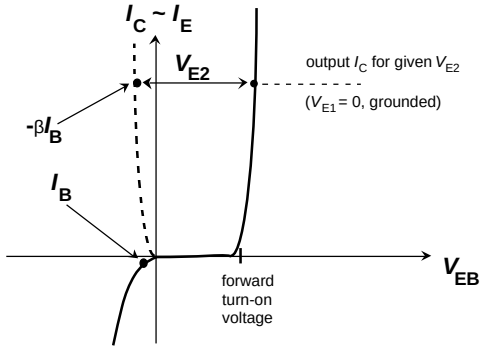

Fig. 2. Solid line shows the schematic emitter-base diode $I(V_{EB})$ from which the output current I_C and transconductance can be predicted. The operating voltage V_{E2} divides between a reverse bias on one of the junctions and a forward bias on the other. At the same time, the injected current in the forward-biased junction equals the reverse-biased tunneling current multiplied by the gain β (dashed line). As a result, a given output current I_C requires an operating V_{E2} that is given by the horizontal (voltage) difference between the forward and gain-multiplied reverse $I(V_{EB})$, as shown.

To see how the tunneling current controls the output current I_C, consider the graphical construction shown in Fig. 2.[7] In the two-terminal diode characteristic $I(V_{EB})$ of the emitter-base heterojunction let us assume that the doping is high enough to lead to a rapid rise in the tunneling current in reverse bias. Then, to determine the collector current I_C corresponding to a given V_{E2}, one finds V_{E2} as the horizontal (potential) difference between the forward bias characteristic and the inverted reverse bias characteristic multiplied by the gain β, see Fig. 2. From this construction it is clear that if the reverse bias tunneling current is large, the required operating voltage V_{E2} falls to approximately the forward turn-on voltage of the emitter-base junction.

Previously, we demonstrated the first, proof-of-concept multiemitter HBTs in $Si/Si_{0.8}Ge_{0.2}$ material.[2] Those devices exhibited good transistor characteristics and excellent current gain β = 400. They also demonstrated the predicted exclusive *or* functionality, with negligible I_C when both emitters were at ground or biased high and the same large I_C when either of the emitters was biased high and the other grounded. However, because of insufficient emitter-base doping ($3x10^{18}$ and $4x10^{19}$ cm^{-3} for emitter and base, respectively), the tunneling current became appreciable only at reverse bias V_{EB} < -1.5 V, resulting in a relatively large operating voltage V_{E2} > 2 V (see Fig. 2). By fabricating HBT structures from Si/SiGe material with a range of higher emitter-base doping values (emitter doping up to 10^{19} cm^{-3} and base doping up to 10^{20} cm^{-3}), we are currently optimizing the HBT design to arrive at low-voltage operation without unduly sacrificing current gain. In the following section we present the data on a multiemitter HBT with a low operating voltage (V_{E2} ~ 1 V), as well as a fully VLSI-compatible BiCMOS process in which the fabrication of multiemitter HBTs is accomplished with fewer processing steps compared to standard Si/SiGe HBTs.

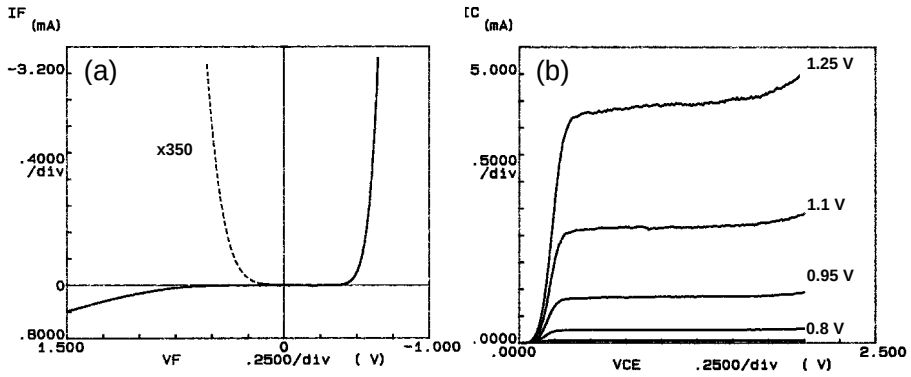

Fig. 3. (a) Emitter-base diode $I(V_{EB})$ characteristic of *npn* Si/ $Si_{0.7}Ge_{0.3}$/Si HBT material (nominally doped 10^{19} and $4x10^{19}$ cm^{-3} in the emitter and base, respectively; emitter contact area ~100x100 μm); dashed line is the reverse-bias part of $I(V_{EB})$ inverted and multiplied by the gain. (b) Transistor $I_C(V_{E2}, V_C)$ characteristics, with V_{E2} stepped from 0.65 to 1.25 V in steps of 0.15 V.

2. Low-Voltage Operation

The HBT material for low-voltage multiemitter devices had a narrow, 20 nm *p*-$Si_{0.7}Ge_{0.3}$ base doped $4x10^{19}$ cm^{-3} and an *n*-Si emitter nominally doped to 10^{19} cm^{-3}. Two emitters of 100x100 μm area, separated by ~5 μm, were fabricated using Pt/Au metal contacts and selective etching down to the base (for details of the HBT design and processing sequence, see Ref. 2). The emitter-base $I(V_{EB})$ diode characteristic of this material is shown in Fig. 3(a). The emitter doping level is still insufficient for a true backward-diode characteristic, probably because of incomplete emitter dopant activation. Still, we observe a reverse current that exceeds 1 μA at $V_{EB} < -0.3$ V (also shown is the reverse-bias characteristic multiplied by the current gain $\beta = 350$ and inverted, compare with Fig. 2). The corresponding room-temperature transistor characteristics $I_C(V_{E2}, V_C)$ are shown in Fig. 3(b). As expected from the emitter-base $I(V_{EB})$, the transistor turns on at about $V_{E2} \sim 0.7$ V and a collector current $I_C \sim 1$ mA is obtained when $V_{E2} \sim 1$ V (whereas $I_C \sim 5$ mA requires $V_{E2} \sim 1.25$ V). If we define a transconductance in this device as $\partial I_C/\partial V_{E2}$ per unit area, these very large devices provide about 500 mS/mm^2 at $V_{E2} = 1$ V (since the device footprint is ~200x100 μm). Transconductance would increase greatly in smaller devices with interdigitated emitter geometry to eliminate current-crowding effects.

3. VLSI-Compatible Processing

Another key requirement is the compatibility with manufacturable VLSI processing. Figure 4 compares the fabrication of a standard Si/SiGe HBT (on the left) and a multiemitter HBT (on the right) using a BiCMOS sequence developed at Lucent.

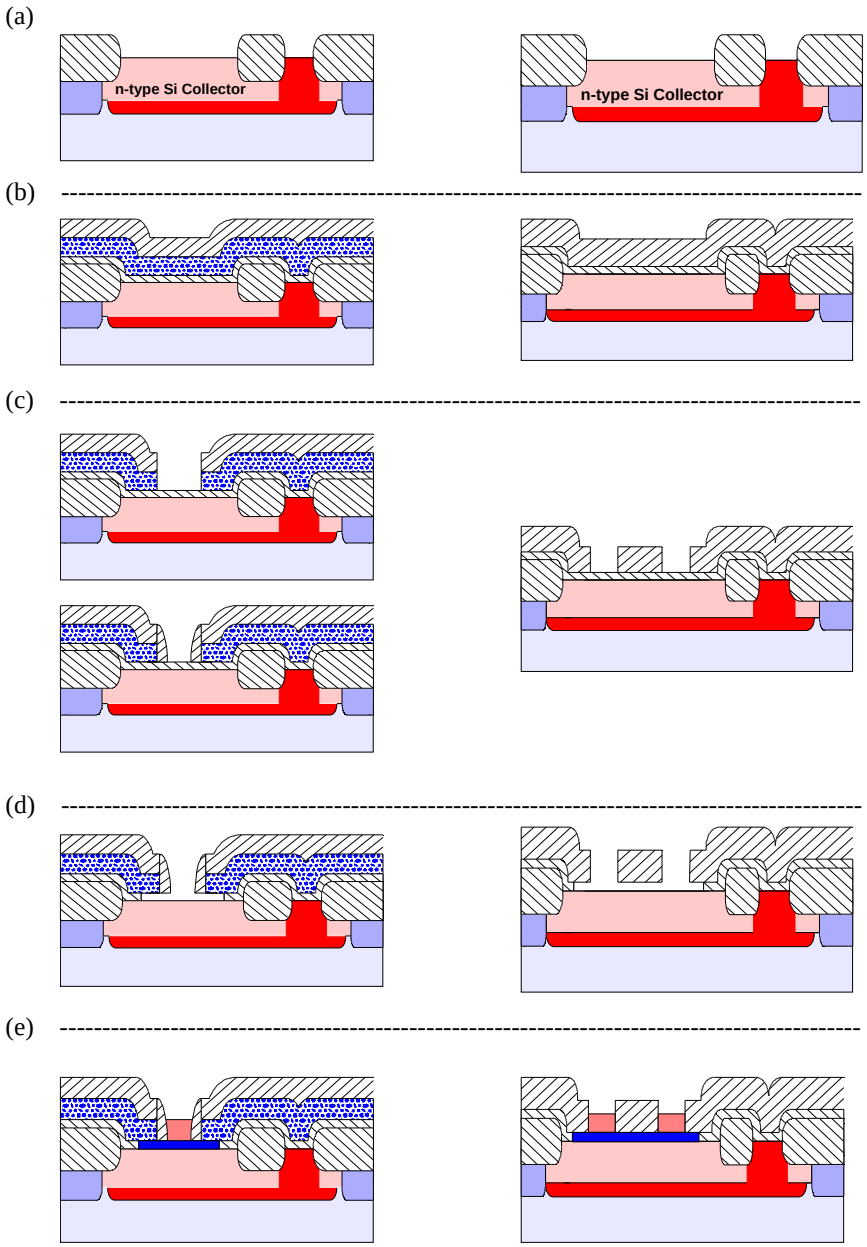

Fig. 4. Side-by-side comparison of standard (left) and multiemitter (right) HBT fabrication in a BiCMOS process: (a) starting point after collector formation; (b) oxide/doped poly-Si/nitride (left) *vs*. oxide/nitride (right) deposition; (c) active area etching and nitride sidewall formation (left) *vs*. no sidewall (right); (d) selective oxide etching; (e) selective epitaxy of *p*-SiGe base and *n*-Si emitter layers.

First, consider the standard HBT: after *n*-Si collector and sub-collector formation (a); the standard HBT requires deposition of an oxide/doped poly-Si/nitride stack (b); etching of the active area window followed by nitride sidewall formation (c); selective wet-etching of the oxide[8] down to the collector (d); and finally selective growth of the *p*-SiGe base and *n*-Si emitter (e) (subsequent passivation and contact formation not shown). Note that the role of the doped poly-Si in step (b) is to provide the base contact to the selectively grown *p*-SiGe base in step (e), while the nitride sidewall formation of step (d) is needed to prevent a short between the base contact poly-Si and the *n*-Si emitter. Now consider the parallel fabrication of the multiemitter HBT, which requires no base contact. Starting with the same *n*-Si collector (a); the oxide/nitride stack is deposited without doped poly-Si (b); the two (or more) active area windows are opened simultaneously, with no nitride sidewall (c); the same selective etch connects the bases as required (d); and finally the *p*-SiGe material is grown selectively followed by *n*-Si emitter growh (e).

The number of lithographic steps required for the multiemitter device is the same as for a standard HBT, but the multiemitter version obviates the need for a doped poly-Si layer for base contacting and the subsequent nitride sidewall formation. At the same time, the multiemitter HBT offers higher logic functionality: exclusive *or* in a single two-emitter device, *ornand* in a three-emitter device[3,7] and so forth.

4. Conclusions

The enhanced functionality of the multiemitter HBT is similar to the *ornand* logic demonstrated by Mastrapasqua and co-workers[9] in multiterminal real-space transfer devices implemented within SiGe technology. However, multiemitter HBTs exhibit higher logic without sacrificing VLSI compatibility: they operate at room temperature with high current drive and excellent gain, and they can be manufactured in a VLSI BiCMOS process. Currently, we are optimizing the HBT design for low-voltage operation. Next we will fabricate small devices for microwave characterization: the multiemitter HBT is expected to suffer from slightly longer emitter delays due to the higher emitter-base capacitance, as heavier emitter doping is required for efficient reverse bias tunneling. Finally and crucially, computer designers should be encouraged to utilize the logic functionality of multiemitter HBTs in their architectures. In particular, an *n*-emitter HBT will switch the output current from high to low when all *n* inputs reach the same logical state – a function that may prove useful in asynchronous designs.

Acknowledgments

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