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Citation: AIP Conference Proceedings **931**, 445 (2007); doi: 10.1063/1.2799415
View online: http://dx.doi.org/10.1063/1.2799415
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New Materials and Structures for Transistors based on Spin, Charge and Wavefunction Phase Control

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Abstract. Naysayers have been claiming for some time now that the dramatic progress of microelectronics in accordance with Moore's law is about to come to a crashing halt. We give examples from novel semiconductor memory and logic devices that indicate that the future is likely to be even more exciting. Conventional Si CMOS may be enhanced by spintronics and quantum interference devices. We will point out metrology needs and opportunities in some of these areas.
Keywords: Nanoelectronics, spintronics, MOSFETs
PACS: 73.63.-b

INTRODUCTION

There is strong interest in enhancing conventional Si CMOS with heterogeneous integration of advanced memory and logic devices. Nanometrology can guide research in these areas because of the novel materials, structures at the nanoscale, and interest in computational state variables such as spin, phase and electron charge.

We have made high-density non-volatile flash memories using SiGeC or metal Self Assembled Quantum Dot (SAQD) floating gates with high-k gate dielectrics. In the area of logic transistors, conventional scaling of bulk CMOS logic devices appears to have been stymied in recent years, leading to a flurry of activity in multi-gate and enhanced channel mobility MOSFETs. With the advent of low leakage and low equivalent oxide thickness (EOT) high-k gate dielectrics, the limitation of Ge MOSFETs of not having a stable high-quality native gate oxide, has been mitigated and high mobility Ge or III-V channel MOSFETs have been demonstrated.

We are also pursuing novel transistors in the Southwest Academy of Nanoelectronics (SWAN) based on controlling spin (spintronics) and relative phase of electron wavefunction (phasetronics).

Flash Memory

Nanoparticles in the floating gate act as electron charge storage sites, and program the bits “0” or “1” depending on the number of electrons stored, which determines the flatband and threshold voltage in these metal oxide semiconductor flash memories. One key advantage of such discontinuous quantum dot array floating gates over conventional *continuous* gate electrodes is that an electrical defect in the underlying tunnel oxide will not be able to discharge the entire array of dots, thereby leading to improved charge storage reliability. However, as the memory cells are shrunk in size, one ends up with a small number of dots in each memory cell, such that statistical variations in the number and spatial location of the dots cause unacceptably large manufacturing variations in the memory cell characteristics. We will, therefore, focus on the growth of *ordered arrays* of SAQDs on high-k tunnel dielectric surfaces, employing chemical/physical vapor deposition or colloidal self-assembly using protein templates **[Fig.1].**

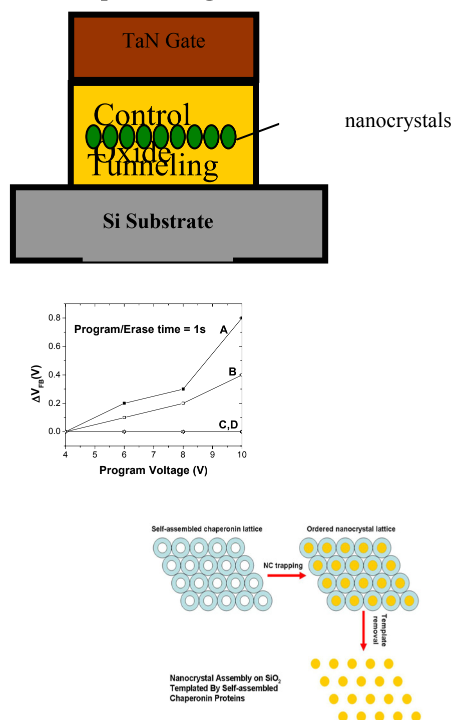

FIGURE. 1. Illustration of chaperonin GroEL based self-assembly scheme from colloidal suspension of semiconductor or metal nanoparticles, and application in non-volatile quantum dot memory.

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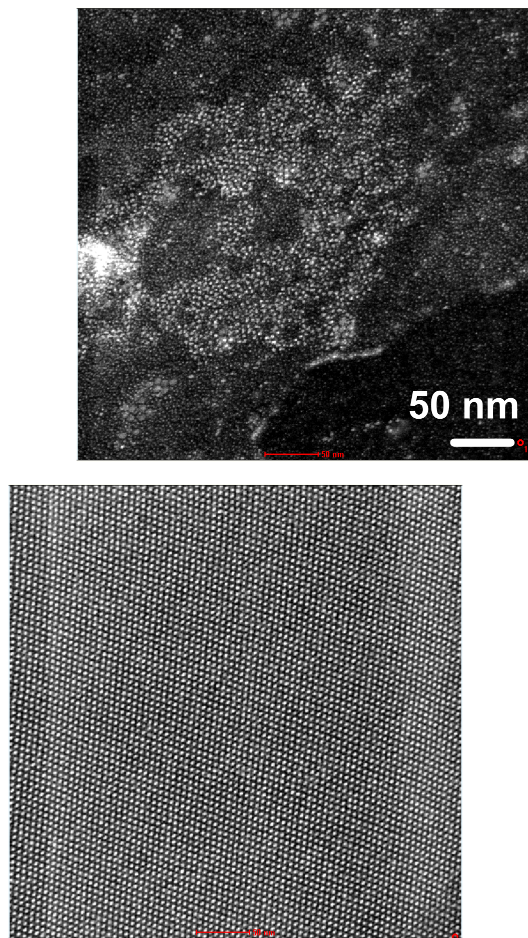

FIGURE 2. STEM images of PbSe nanocrystals self-assembled on silicon tunnel oxide without (top) and with (bottom) a biological chaperonin template, and a colloidal suspension of nanocrystals. These form the floating gate for charge storage in high speed, low voltage, reliable non-volatile flash memory.

We have recently demonstrated that a chaperonin protein lattice can be used as a template to assemble semiconductor and metal nanocrystal arrays for flash memory fabrication [1]. Chaperonins are a group of molecular chaperones that have a large multimeric structure consisting of two stacked rings surrounding a central cavity within which the protein substrate binds. Chaperonins can be self-assembled into a crystalline lattice through non-covalent interactions between the proteins. The interior surface of the chaperonin's central cavity is hydrophobic, which allows semiconductor or metal nanocrystals functionalized with hydrophobic molecules to be trapped site-specifically inside the cavities. Once PbSe or Co nanocrystals are trapped by the chaperonin template, the template is easily removed at 200 C by annealing in O_2, leaving behind a nanocrystal assembly with uniform distribution and a high density of around $1\times10^{12}/cm^2$, and good spatial and size uniformity. Sample A where dots are trapped by the protein and the protein is oxidized away, and B where the protein is retained along with the dots

show significant electron storage, resulting in large flatband shifts which can delineate the “0” and “1” states. Control samples C with just the proteins (without dots) and D without proteins or dots show no ΔV_{FB} [Fig. 1].

There are nanometrolgy needs in characterizing the various interfaces between high-k dielectrics, and the channel or nanoparticles. These traps may be responsible for charge storage, or limit memory endurance and retention. The capacitance of such nanoparticles in the atto-Farad regime must be measured to study Coulomb blockade phenomena.

Transistors

With the advent of low leakage and low equivalent oxide thickness (EOT) high-k gate dielectrics, the limitation of Ge MOSFETs of not having a stable high-quality native gate oxide, has been mitigated and high mobility Ge channel MOSFETs have been demonstrated. Additionally, the lower band gap of Ge with the higher mobility should increase carrier injection from the source to the channel above that of Si. However, bulk Ge MOSFETs are limited by Ge substrates which are more expensive, fragile and have worse thermal conductivity than Si. Germanium channel MOSFETs fabricated on a Si substrate, incorporate the Ge channel either on a *thick* relaxed $Si_{1-x}Ge_x$ buffer layer or a strained Ge-on-insulator (SGOI) substrate, followed by a pure Ge epi layer. However such schemes are expensive and require complex processing. We have studied various schemes to circumvent some of these limitations. In one approach, Ge channels comparable to the inversion layer thickness were grown directly on Si substrates using a low temperature (~370º C) ultra high vacuum-chemical vapor deposition (UHV-CVD). This technique requires neither an expensive starting substrate nor complex thick relaxed buffer layers. Thin (~15nm) compressively-strained selective epitaxial grown (SEG) Ge film were achieved on small open Si active areas by ultra high vacuum-chemical vapor deposition (UHV-CVD). It was subsequently capped with a hafnium oxide gate dielectric at room temperature and then annealed. SEG growth and capping the Ge layers *prior* to thermal processing improve the stability of the layers, and the roughness of the epitaxial films. The compressively-strained Ge PMOSFETs show a ~2X

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enhancements in drive current compared to Si devices.

In a second approach, we have grown Ge:C *partially* strain compensated epitaxial films on Si in order to increase the allowable thermal budgets for MOSFET fabrication, and demonstrated enhanced hole mobilities in pMOSFETs compared to Si devices. To remove the need for thick buffer layers, thermal annealing, or other defect-burying techniques for achieving high-quality Ge-based crystal on Si, this work focuses on the use of thin (< 35 nm), partially-compressively-strained germanium-carbon alloy (Ge:C) layers grown directly on Si by UHVCVD. It has been found that only moderate C contents (≤ 1 at. %) are needed to facilitate high-quality, two-dimensional (2D) growth on Si, and that the Ge:C layers can exhibit enhanced hole mobility over the universal mobility limitation for Si despite detrimental alloy scattering effects.

The Ge:C layers for this work were grown in a custom-built cold-wall UHVCVD system with pre-deposition pressures between 7.0×10^{-10} and 1×10^{-9} Torr [2]. The growth temperatures were between 350 and 500°C. GeH_4 and CH_3GeH_3 precursors were flown simultaneously at a deposition pressure of approximately 5 mTorr. The CH_3GeH_3:GeH_4 gas flow ratio was controlled to determine the amount of C incorporation. Figure 3 shows cross-sectional transmission electron microscopy images of a 30-nm Ge:C layer (~1 at.% C) that was grown on Si with a 6-nm Si capping layer. The Si substrate and Ge:C and Si cap layers are shown in Fig. 3 shows a magnified image of the Ge:C layer. A modified EPD measurement technique was developed by our group for use with very thin films. Based on our measurements, the threading dislocation density is estimated to be around 5×10^5 cm^{-2}. The RMS surface roughness of the films measured by AFM was less than 3Å, which is remarkably smooth for Ge grown directly on Si.

For the pMOSFET fabrication, after removing the wafers from the UHVCVD reactor, HfO_2 and TaN were deposited by DC magnetron sputtering. Ring-type gates (R1=75μm, R2=85μm) were patterned using lithography and reactive ion etching with CF_4. The wafers were then implanted with BF_2 (5×15cm-2, 25 keV). The dopant atoms were activated during a 2 hr., 530°C contact isolation low-temperature oxide (LTO) step, followed by contact patterning and Al metallization. The process was finished with a forming gas anneal at 450°C for 30 min.

C-V and I-V measurements for HfO_2/TaN Ge:C MOS capacitors without a Si cap (SC) show D_{it} was 4.82×10^{11} $eV^{-1}cm^{-2}$ and the leakage current was 3.3×10^{-5} A/cm^2 (at 1V) for EOT=2.3 nm. The SC pMOSFETs show higher gate leakage, which is likely due to the diffusion of Ge and C atoms into the HfO_2 during the post-deposition anneal and the contact isolation LTO step. Increased gate leakage is expected for devices that lack surface passivation.

Figures 4 show I_D-V_{DS} and mobility characteristics for BC and SC Ge:C pMOSFETs compared to Si control devices. At V_{GS}-V_T=-1.0V, high drive currents of 10.8 μA/μm for the BC pMOSFETs and 15.2 μA/μm for the SC pMOSFETs were achieved. Figure 4 shows that the BC devices exhibited a 2× enhancement in I_{Dsat} (V_{GS}-V_T= 1.0V) over the Si control. The I_{on}/I_{off} ratio for the BC devices was 5×10^4. The enhancement for the SC devices over the Si control device was 3× for I_{Dsat}. The I_D-V_{DS} characteristics in Fig. 4 show somewhat degraded behavior in the saturation region compared to the BC devices. The SC devices also had high subthreshold leakage current. These observations can again be attributed to the lack of surface passivation for the SC devices prior to HfO_2 deposition.

The mobility could likely be improved further by reducing the C concentration in the Ge:C layer and improving the interface with the HfO_2. Such Ge-C layers have also been used as templates for MBE growth of III-V semiconductors (GaAs) and MOS structures demonstrated.

The structure and composition of various interfaces needs to be characterized, for example with lattice imaging and aberration-corrected transmission electron microscopy (TEM). Electron energy loss spectroscopy (EELS) can provide information about chemical composition and bonding.

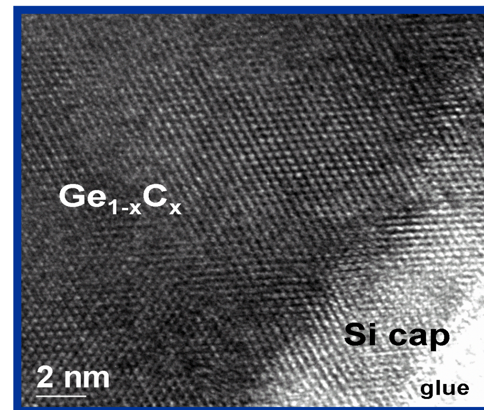

FIGURE 3. Pure Ge on Si growth leads to lots of defects (dislocations and stacking faults); Ge-C on Si growth is epitaxial with few defects.

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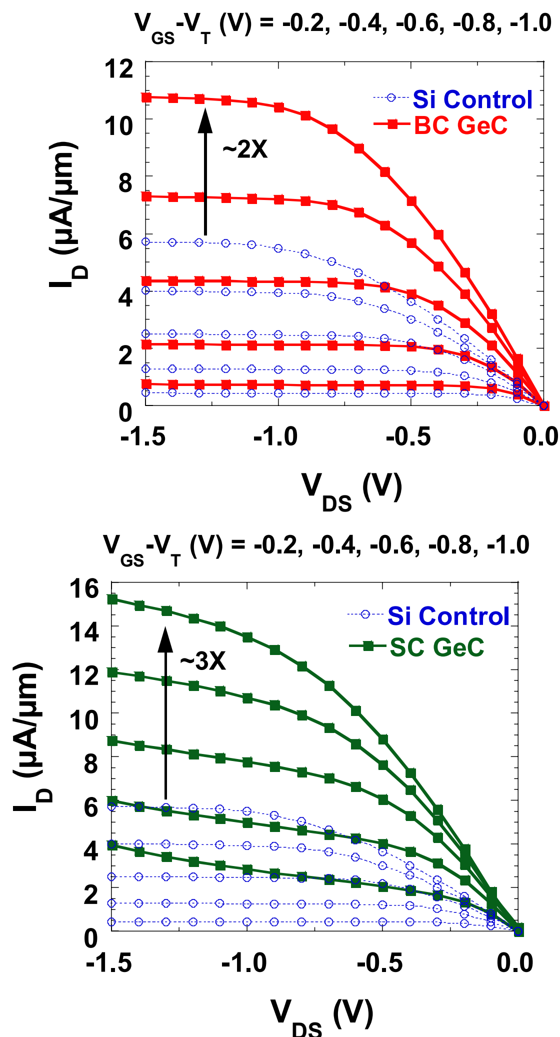

FIGURE 4. Buried channel Ge-C PMOSFETs with a thin Si cap (top) and surface channel devices without a cap (bottom) showing significant enhancement over control Si devices. They use a 5 nm thick hafnia gate dielectric.

In the SWAN research program, we are pursuing a focused *theoretical* and *experimental* effort to develop a new transistor or switch to replace MOSFETs. We have a set of tasks where we explore the use of electron ***spin***, a known weakly-dissipative transport mechanism, as the computational state variable for possible new logic devices. We plan to focus on the Rashba model for the spin Hall effect as a means of obtaining large values of gate control over the spin accumulation for device applications. Additionally, we will explore the use of interlayer ***phase***, another reduced dissipation mechanism, where the spin degree of freedom has been replaced by a 'which layer' degree of freedom, in bilayer systems as a means of creating a wide range of devices from memory and logic to oscillators. We next extend our ***spin*** set of tasks to include the theoretical and experimental examination of magnetic nanoparticles for memory devices. To experimentally verify our theoretical conclusions, we will self-assemble nanoparticles of ferromagnetic metals such as Co using bottom-up (protein ring templates or diblock copolymers), or top down schemes (nanoimprinting) to demonstrate device concepts based on nanomagnet arrays. We plan to develop new many-body tools to examine the possibility of exploiting the Kondo effect or an applied magnetic field in quantum point contacts for *in situ* polarized spin injection. We conclude our ***spin*** analysis by fabricating narrow quantum wires in Si and SiGe and performing low temperature measurements to determine their ability to act as media for our preceding theoretical proposals.

In addition to spin, we have a set of tasks where the ***phase*** of the electronic wavefunction and ***charge*** will be manipulated for new types of devices. For these tasks, we will theoretically and experimentally study nanowires and nanorods. We will theoretically and experimentally examine the use of ***phase*** manipulation in closely spaced nanorods as a means of constructing quantum logic gates. We theoretically examine quantum interference and phonon engineering in nanowires to increase the ballistic length for efficient low-power ***charge*** based devices.

Nanometrology will be key in these studies. For example, the dilute magnetic semiconductors which could be the basis of spintronics are poorly characterized in terms of the interplay of materials quality and magnetism. For the phase interference devices, if scanning probe microscopy techniques could be devised to measure the electron interference patterns in the electron waveguides, it could lead to useful device geometries.

ACKNOWLEDGMENTS

This work was supported by DARPA MARCO, NRI-SWAN, SRC and NSF.

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