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ANALYSIS AND VERIFICATION OF INTEGRATED CIRCUIT THERMAL PARAMETERS

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Abstract. *The paper describes thermal model of an ASIC designed and fabricated in CMOS 0.7 μm (5 V) technology. The integrated circuit consists of analogue and digital heat sources and some temperature sensors. It has been designed to carry out some thermal tests. During tests thermal resistances, capacities, time constants and convection coefficients for different packages, positions and cooling methods were extracted. The parameters of thermal model were used in simulation to compare results with real-world measurements.*

Keywords: thermal resistance, thermal capacity, thermal time constant, CMOS

ANALIZA I WERYFIKACJA PARAMETRÓW TERMICZNYCH UKŁADU SCALONEGO

Streszczenie. *Artykuł opisuje model termiczny układu ASIC zaprojektowanego i sfabrykowanego w technologii CMOS 0,7 μm (5 V). Układ scalony składa się z analogowych i cyfrowych źródeł ciepła oraz czujników temperatury a został zaprojektowany w celu wykonywania testów termicznych. Podczas przeprowadzonych testów zmierzone zostały rezystancja termiczna, pojemność termiczna, termiczna stała czasowa i uogólniony współczynnik konwekcji dla różnych wariantów obudowy, jej położenia i metody chłodzenia. Parametry modelu termicznego zostały użyte w symulacjach w celu porównania wyników z rzeczywistymi pomiarami.*

Słowa kluczowe: rezystancja termiczna, pojemność termiczna, termiczna stała czasowa, CMOS

Introduction

Big power consumption resulting with overheating is an important problem in designing high frequency integrated circuits [6]. As a consequence thermal issues of the circuit work must be considered. That is the reason why precise information on thermal parameters is necessary.

The paper presents proposed thermal model of an integrated circuit. The measurements were done for a test chip consisting of some heat sources and temperature sensors. Presented results were gathered in several different chip configurations. Finally, software has been created for verification of the results calculated by the model. Calculated values of the temperature are compared with ones measured in the chip.

1. Model description

To describe thermal behaviour of the integrated circuit some parameters are needed. In this paper well known analogy between electric and thermodynamic parameters are used. Main parameters (and their units) of this analogy are gathered in Table 1.

Table 1. Parameters of the electrical-thermodynamic analogy

Thermodynamic parameter	Electric parameter
Temperature T [°C]	Voltage U [V]
Power P [W]	Current I [A]
Heat Q [J]	Charge q [C]
Thermal resistance R_{th} [°C/W]	Resistance R [Ω=V/A]
Thermal capacity C_{th} [J/°C]	Capacitance C [F=C/V]
Thermal time constant $\tau_{th} = R_{th}C_{th}$ [s]	Time constant $\tau = RC$ [s]

For purposes of this paper it was assumed that whole area of silicon die is isothermal. This assumption does not make a big mistake and highly simplifies calculations. That can be reasonable from the measurement point of view, what will be explained more precisely in next sections. Based on this basic feature the integrated circuit under tests will be treated as it consists of one thermal resistance R_{th} and one thermal capacity C_{th} [5]. From that point of view thermal resistance can be understood as an amount of power that has to be dissipated in the circuit to increase its temperature to specified value and thermal capacity can be understood as an amount of energy that is stored in the structure of the circuit at this temperature. Such schematic of thermal model is presented in Figure 1. Additionally voltage source T_{amb} represents ambient temperature. It is very important to remember that temperature of the integrated circuit T_{chip} will never be lower than ambient.

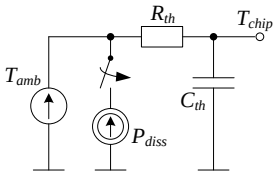

Fig. 1. Schematic diagram of the electrical analogy for thermal model of the integrated circuit

Additional power can be dissipated in the chip after switching on P_{diss}, what will cause change of chip temperature described by (1). Presented structure behaves as an inertial circuit. Pulse change of dissipated power will not cause immediate result but the temperature will rise as exponential function according to (2), where τ is thermal time constant of the integrated circuit and t is time elapsed from the start of pulse change of power dissipation [1].

$$\Delta T = R_{th} P_{diss} \tag{1}$$

$$T_{chip} = T_{amb} + \Delta T\left[1 - \exp\left(\frac{-t}{\tau}\right)\right] \tag{2}$$

Parameters R_{th}, C_{th} and τ of the described model for a specified circuit under test will be calculated in next sections of the paper.

2. Test chip description

The test chip was designed and fabricated in CMOS 0.7 μm technology with 5 V supply voltage. Structure of the integrated circuit is presented in Figure 2 [2]. Elements marked as 'A' are analogue parts while 'D' are digital ones. They play a role of heat sources. Temperature sensors are indicated by 'S' symbols. Both types of heat sources are controlled from outside and are used to dissipate some power in the chip structure. The analogue sources are realized as a big NMOS transistors which drain current (and as a result amount of dissipated power) is controlled by the gate voltage. Digital sources are series of CMOS inverters. When input changes the state of inverters dynamic power losses are dissipated.

Temperature sensors are implemented as Proportional to Absolute Temperature (PTAT) sensors. The PTAT sensor task is to give voltage proportional to the temperature of the chip. Its work is based on the phenomenon that difference between voltages of two diodes or bipolar transistors, which have different areas and conduct the same current, is proportional to the absolute temperature. Implemented structure, presented in Figure 3 has

been chosen because the accuracy is sufficient for this application and presented circuit is easy to implement in CMOS process with planar transistors. The presented PTAT sensor consists of 5 MOS transistors, 2 bipolar transistors and 2 resistors.

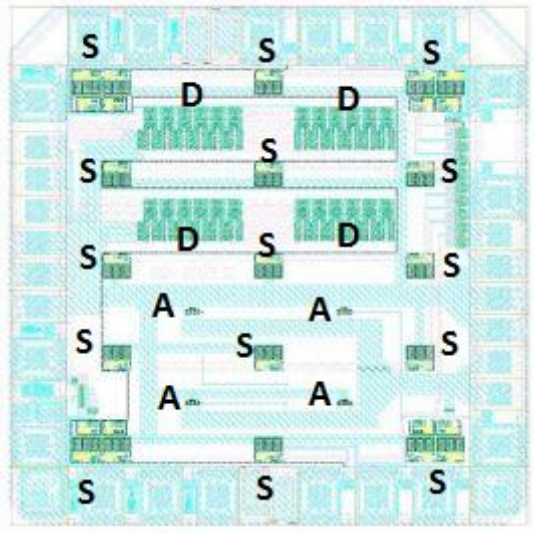

Fig. 2. Topography of the test chip

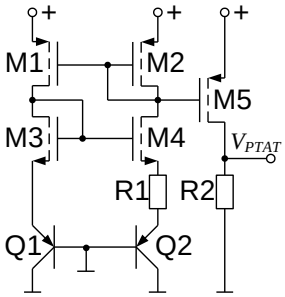

Fig. 3. Schematic diagram of the PTAT sensor

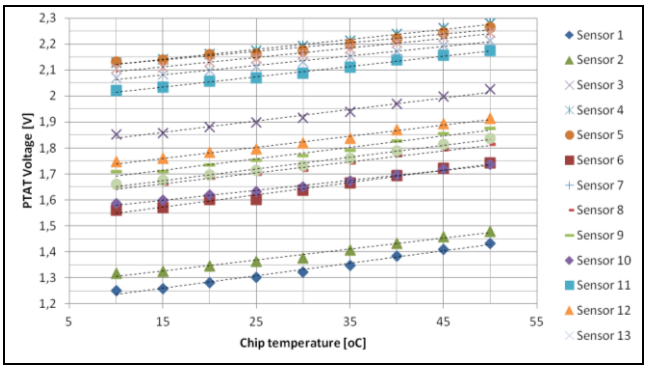

Fig. 4. Measured characteristics of PTAT sensors

The sensor produces voltage given by (3)

$$V_{PTAT} = \frac{W_5}{W_2}\frac{kT}{q}\ln(n)\frac{R_2}{R_1} \tag{3}$$

where W_2 and W_5 are widths of the gates of the M2 and M5 transistors, k is the Boltzmann's constant, T is absolute temperature, q is the charge and n is the ratio between emitter areas of Q1 and Q2 planar transistors [3]. Current conducted by the circuit is limited to prevent self-heating of the sensor. In presented case the temperature sensor was designed using two PNP planar transistors with the emitters area multiplication factor $n = 2$.

The sensors were calibrated in the thermal chamber. Measured characteristics are presented in Figure 4. For further usage one sensor was chosen because of small measurement error and good approximation with linear function as well as its close position to used analogue heat sources.

3. Measurement methodology

In the first approach thermal resistances was calculated. All measurements were done at ambient temperature T_{amb} of about 24 to 26ºC. After dissipating P_{diss} of about 260 mW its temperature raised to T_{chip}. As an effect thermal resistance could be calculated as (4).

$$R_{th} = \frac{T_{chip} - T_{amb}}{P_{dyn}} \tag{4}$$

Information about chip temperature was read from the PTAT output signal. That guaranteed that measured temperature value came directly from the silicon die. After changing power dissipated in the chip thermal time constant τ_{th}, (5), can be read from oscilloscope screen. Assuming that this value is already measured thermal capacity C_{th} of the circuit can be calculated.

$$\tau_{th} = R_{th}C_{th} \tag{5}$$

Because of method of thermal time constant measurement value of the capacity is the least accurate parameter. Resolution of the time constant measurement was 0.5 s. All inconsistencies of the described model are probably caused by this inaccuracy. In the end generalized convection coefficient α can be obtained from:

$$R_{th} = \frac{1}{\alpha S} \tag{6}$$

where S is isothermal area of the chip estimated by means of infrared camera [4].

For better comparison measurements were done for closed package and package without cover so heat convection was better. In addition in open-chip case measurement of silicon die temperature with pyrometer was possible. That enabled good temperature verification method. If it was possible some cooling was also used. For better heat convection a small fan was used and for better heat radiation a small heat sink was mounted on the chip. In all cases test were done in three different orientations of the chip: vertical, horizontal and upside down.

4. Measurement results and discussion

Based on described methodology some tests were done and parameters of the thermal model from Figure 1 were extracted for used integrated circuit. Values of measured thermal resistance, thermal capacity and thermal time constant for different packages, positions and cooling options are gathered in Table 2.

In the case of the chip without coverage the temperature could be verified by other measurement method. For that reason a pyrometer was used. Diameter of the laser point had a comparable size with length of the silicon die of the integrated circuit.

Obviously measured value was temperature of the surface of the chip, not its inside what was indicated by temperature sensors so those two values would differ slightly. Temperature of the edge of silicon should be a little lower. Values obtained with the second method are less accurate. Despite this inconsistence a pyrometer can be used to check validity of previous results. Thermal resistance, capacity and time constant measured by pyrometer for an open package are presented in Table 3. As can be seen results of both measurement methods are similar. If thermal resistance was already calculated by two different measurements methods the heat convection coefficient can be obtained according to (6). Measured values are gathered in Table 4.

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If thermal resistance was already calculated by two different measurements methods the heat convection coefficient can be obtained according to (6). Measured values are gathered in Table 4. After analysis of above tables some conclusions can be done. Firstly, thermal resistance depends on the integrated circuit position. This result can be surprising when compared to electrical analogy but can be explained by heat convection. The lowest value of the thermal resistance for chip positioned vertically is a result of the fact that this position favours laminar motion of the air. By positioning the chip in the way which is good for heat transfer the convection coefficient is rising and as a consequence the thermal resistance is getting smaller. For similar reason R_{th} has the largest value for chip inversed upside down. This conclusion is important for designers of packages for electronic circuits. For thermal reasons the most heating parts should be placed vertically. If it is not possible (for example in small portable devices) additional method of cooling should be implemented to avoid overheating. Another conclusion refers to the thermal capacity which is constant for different chip positions. That means that amount of energy stored in the integrated circuit does not depend on its position.

Table 2. Measured thermal resistance, capacity and time constant for different test cases

Package	Cooling method	Position	Thermal resistance [K/W]	Thermal capacity [J/K]	Thermal time constant [s]
open	none	horizontal	32.90	0.395	13
		vertical	26.96	0.408	11
		upside down	35.64	0.393	14
	fan	horizontal	13.46	0.371	5
		vertical	10.56	0.379	4
		upside down	17.69	0.396	7
closed	none	horizontal	110.73	0.452	50
		vertical	108.20	0.444	48
		upside down	113.79	0.457	52
	fan	horizontal	90.46	0.420	38
		vertical	89.59	0.419	37.5
		upside down	93.38	0.428	40
	heat sink	horizontal	89.23	0.841	75
		vertical	89.24	0.840	75
		upside down	93.49	0.845	79

Table 3. Thermal resistance, capacity and time constant measured by pyrometer for open package case

Cooling method	Position	Thermal resistance [K/W]	Thermal capacity [J/K]	Thermal time constant [s]
none	horizontal	31.17	0.417	13
	vertical	25.81	0.426	11
	upside-down	35.83	0.391	14
fan	horizontal	12.69	0.394	5
	vertical	12.28	0.326	4
	upside-down	19.23	0.364	7

Table 4. Convection coefficient values for different test cases

Package	Cooling method	Position	Convection coefficient [W/m^{2}K]	
			PTAT	Pyrometer
open	none	horizontal	67.55	71.30
		vertical	82.42	86.11
		upside down	62.35	62.01
	fan	horizontal	165.09	175.10
		vertical	210.50	180.90
		upside down	125.59	115.54
closed	none	horizontal	20.07	X
		vertical	20.54	X
		upside down	19.53	X
	fan	horizontal	24.57	X
		vertical	24.80	X
		upside down	23.80	X
	heat sink	horizontal	24.91	X
		vertical	24.90	X
		upside down	23.77	X

It is obvious that usage of a cooling method has an effect in thermal parameters. Used fan had small dimensions to avoid too big changes in measured parameters values. After mounting this device a heat convection was improved (what can be seen in convection coefficient value) and thermal resistance was smaller. That means that a circuit working with an active ventilation method would reach smaller temperature range. Used heat sink, similarly to fan, has quite small size. Its usage resulted with heat radiation improvement. Mounting heat sink did not have impact on thermal resistance but was an additional thermal capacity which caused much larger time constants. Increased value of the thermal capacity understood as an amount of energy Q collected in the device, can be explained by additional mass m of the heat sink mounted on the package according to (7):

$$Q = mc\Delta T \tag{7}$$

where c is specific heat capacity and ΔT is change of the temperature. Important conclusion is that with heat sink chip position does not change any thermal parameter. That is a result

of the fact that with such a big area of mounted device heat convection does not play important role anymore.

The last important conclusion is that thermal behaviour of the circuit is better for an open package. If silicon die has direct contact with the air heat convection is larger. In fact that does not mean that packages without coverage should be used. Such situation was possible in laboratory environment for test purposes. In industrial applications such unprotected circuit would be too fragile and would be destroyed very fast.

5. Parametric analysis

Measured thermal parameters can be a base for theoretical deduction of chip temperature under different working conditions, such as changes of circuit workload (which means power dissipated inside chip package) or environmental conditions (for example changes of ambient temperature). In this section parametric analysis based on parameters from Table 2 will be presented.

For the test purposes 260 mW of power were dissipated in the chip area. Such amount of power was possible to produce by internal analogue heat sources realized as NMOS transistors. When a digital circuit is implemented in specific application the workload can remarkably change in time depending on present tasks that are realized by the circuit. It means that also temperature of the chip would change. Steady state temperature for different amounts of power dissipated in the circuit can be calculated from equation (4) and for open package cases is presented in Figure 5. As can be seen on picture below circuit temperature rises significantly for greater amounts of power. When test amount of 260 mW was applied the difference between package cooled by fan and without any cooling was about 5°C for horizontal package, while for approximately four times bigger amount of power (1 W) the difference rises to over 19.4°C. Such difference is significant value and shows how important is proper cooling of the package.

Figure 6 presents similar analysis for sealed package. Difference between package with and without cooling is also clearly visible, but temperatures of chip cooled with fan and heat sink are very close. It means that type of cooling can be chosen respectively to specific application. The most important is to properly cool the chip, the method of cooling is secondary problem. Another conclusion from the picture is that closed package reaches much higher temperature ranges. For most integrated circuit applications it is assumed that temperature over 100°C endangers proper circuit operation and is treated as overheating. Such situation has to be avoided what proves again importance of proper chip cooling.

Different parameter that has to be taken into account in this analysis is ambient temperature because even for stable workload the environmental conditions can change. Previous calculations were made for ambient temperature equal 25°C. Poorly cooled chip (working for example in small closed container) would have to deal with much higher ambient temperatures.

Equation (4) means that present chip temperature depends linearly on the ambient temperature. The dependence for 260 mW dissipated inside the chip package is presented in Figure 7. Only horizontally placed packages were depicted because the dependence is linear. Other curves are easy to deduce and would only deteriorate the picture readability. Once again a difference of about 5°C between cooled and not cooled packages is clearly seen (for both open and sealed packages).

Similar analysis can be performed for other parameters that affect integrated circuit thermal behavior. The only condition is knowledge of chip thermal parameters for specific configuration.

Presented analysis are only theoretical calculations and have to be verified by real-world measurements, what will be done in next section of this paper.

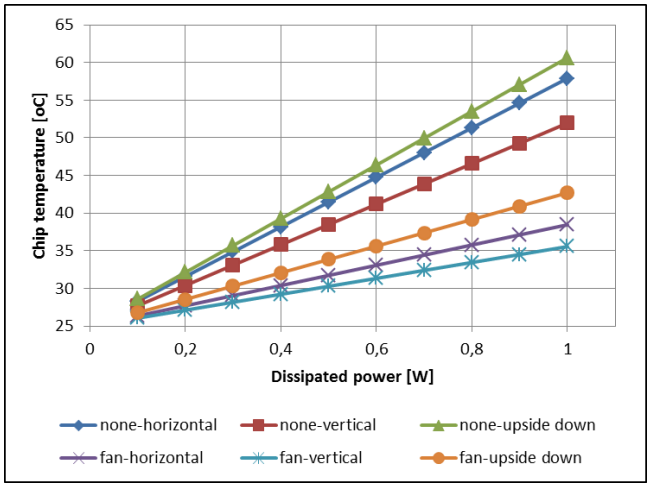

Fig. 5. Chip temperature vs. dissipated power for different open package configurations

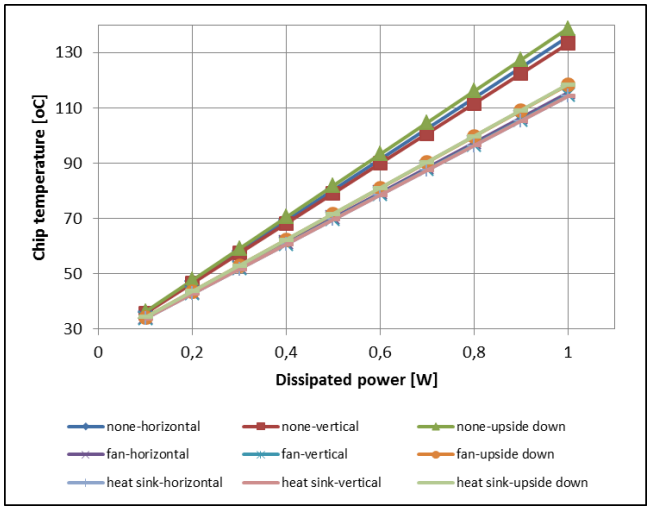

Fig. 6. Chip temperature vs. dissipated power for different closed package configurations

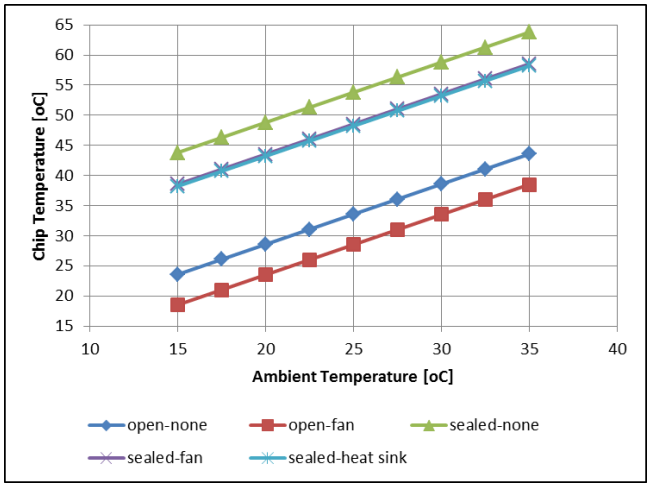

Fig. 7. Chip temperature vs. ambient temperature for different configurations of packages placed horizontally

6. Verification

Values of the parameters of the presented model had to be verified. For those purposes a test system was created. Value of the signal proportional to temperature was read by the ADC (Analogue-to-Digital Converter) built in EFM32G890F128 microcontroller. This value was send from microcontroller to a PC using RS232 standard. Finally, a PC application in LabVIEW environment read the value and presented on the screen. Temperature read directly from the integrated circuit was compared with values calculated by the model. Described verification tool was used to test the integrated circuit with and without cover, in all three positions and with all mentioned cooling methods. In all cases calculated model parameters gave results consistent with temperature values measured directly in the chip. Example of the picture gathered by the program is presented in Figure 8. Picture below presents test of the dissipated power step for open circuit placed horizontally cooled by the fan. Smooth line is temperature value predicted by the model. Values measured in the chip are indicated by the irregular line. Resolution of the temperature measurement is about 0.15°C. Distortions visible in the picture are result of conversion noise and inaccuracy of the ADC (changes in the least significant bit of the converter) as well as noise of the temperature sensor producing the temperature-dependent signal. Filtering distortions from the signal was not implemented to prevent disturbing the dynamics of the measurement process. Despite this noise values obtained directly from the chip and calculations based on model values are consistent, what is clearly seen in the presented figure. This result means that proposed model is suitable and calculated parameters are correct.

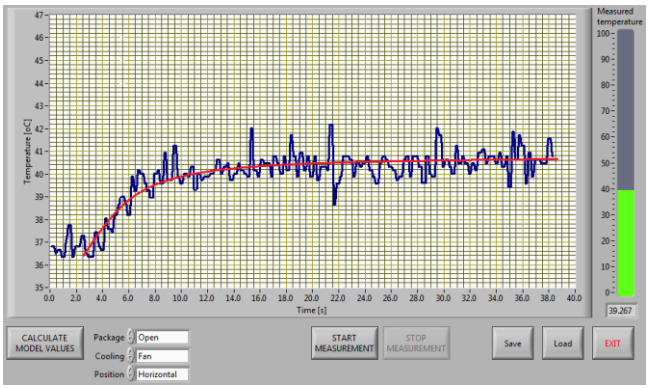

Fig. 8. Exemplary picture of model verification in LabView environment

7. Conclusions

In the paper thermal model of integrated circuit has been proposed. Parameters of described model has been extracted and calculated for a specified test chip designed and fabricated by authors in CMOS 0.7 μm technology. Tests of the circuit were performed for few different configurations: open and closed package of the chip, three different circuit positions (horizontal, vertical and upside down) and three different cooling methods (none, fan and heat sink). Measurements proved that thermal behaviour of the integrated circuit differs for each test case. Proper conclusions have been deduced. Described model have been verified by means of PC application created in LabVIEW environment which compared real-world values of chip temperature and values calculated according to thermal model. Both results were similar. That way it was proved that described model is correct and calculated parameters of the model have values properly calculated.

Thermal model described in the paper is planned to be used in work of the authors who are interested in thermal aspects of low-power integrated circuits. Calculated parameters values will be helpful for future chips design. It is possible that future experiments will correct described model values for better precision.

Acknowledgement

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