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FRACTAL GEOMETRIES IN LATERAL FLUX CAPACITOR DESIGN – EXPERIMENTAL RESULTS

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Abstract. *Capacitance density is increased when lateral flux structures are used in CMOS technologies compared to classic parallel-palate capacitors. Lateral-flux capacitors where designed based on three different fractal geometries. Capacitors are designed with and without special MMC metal layer available in some CMOS technologies for capacitor design. For theoretical analysis verification a special ASIC has been designed and fabricated in UMC 0.18um technology. Presented result are obtained by measurement of 5 ICs. Some capacitor structures have much higher capacitance density than classic parallel-plates capacitor without MMC layer. Few presented structures have higher capacitance density than parallel-plate capacitor made with MMC layer. Capacitors have small process parameters spread.*

Keywords: capacitors, CMOS integrated circuit, fractals

FRAKTALE W PROJEKTOWANIU KONDENSATORÓW Z POPRZECZNĄ POJEMNOŚCIĄ – WYNIKI POMIARÓW

Streszczenie. *W porównaniu do klasycznych kondensatorów z równoległymi okładkami użycie struktur z poprzeczną pojemnością pozwala na zwiększenie gęstości pojemności przy projektowaniu kondensatorów w technologiach CMOS. Kondensatory z poprzeczną pojemnością zostały zaprojektowane na bazie trzech rożnych fraktali. Struktury kondensatorów zostały zaprojektowane z i bez użycia specjalnej warstwy metalu MMC, dostępnej w niektórych technologiach CMOS, do projektowania kondensatorów. Do sprawdzenia teoretycznych rozważań specjalny układ ASIC został zaprojektowany i wykonany w technologii UMC 0.18um. Przedstawione wyniki są efektem pomiarów 5 układów scalonych. Niektóre struktury kondensatorów mają dużo większą gęstość pojemności niż klasyczne kondensatory bez warstwy MMC. Niewiele zaprojektowanych struktur ma większą gęstość pojemności niż kondensatory klasyczne z warstwą MMC. Rozrzut parametrów kondensatorów jest niewielki.*

Słowa kluczowe: kondensatory, układy scalone CMOS, fraktale

Introduction

While designing an ASIC in CMOS technology the space management is crucial. Designer often must struggle to fit in all components of a circuit in a restricted area of an IC. Increasing an available surface generates a considerable cost of fabrication. Analog, mixed-signals and radio frequency circuit require use components that are very area-consuming such as capacitors [4]. If high value of capacitance is required the capacitor occupies area even several times larger than all digital components. Typical CMOS capacitors are made as two layers of metal. Because of relatively thick interlevel oxide layer between plates those capacitors have low capacitance density. This drawback is more burdensome with technology scaling. While every other component in IC gets smaller the capacitors stay relatively the same, because vertical separation of metal layers does not change much in order to avoid cross-talk effects.

Capacitance density is increased when lateral-flux structures are used in CMOS technologies compared to classic parallel-palate capacitors [2]. A cross section of basic structure of a lateral-flux capacitor is presented in figure 1. Metal strips with the same plate number are electrically shorted. This arrangement of plates is much more advantageous with technology scaling. When a new CMOS technology is presented it usually means that smaller element can be designed and circuits are more compact. Lateral spacing between elements, in this case strips of metal creating plates, resulting from design rules are getting smaller, but vertical separation between metal layers and their thickness stay relatively the same. Thus influence of lateral flux on capacitance is growing with each new, smaller technology. Smaller bottom plate of lateral-flux capacitor result in decreased parasitic capacitance between plate and substrate. Additionally some of field lines originating from bottom strips of metal are terminated on neighboring plate instead of on substrate further decreasing parasitic capacitance. Use of lateral-flux structures has proven useful in increasing capacitance density [1, 3, 6]. In [3] achieved density is even several times bigger than of classic capacitor.

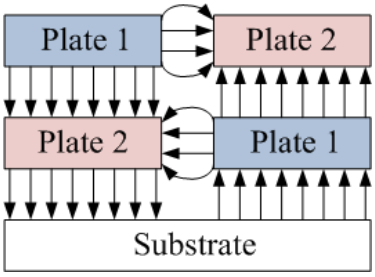

Fig. 1. Structure of lateral flux capacitor with reduction of parasitic capacitance to substrate

Although lateral-flux capacitors have many advantages over classic parallel-plate capacitors they have not replaced them in integrated circuits. In UMC 0.18um CMOS technology, which is the main focus of this paper, a new metal layer was introduced specifically for capacitor design. Layer MMC (Meta to metal Capacitor) is located between last (top) metal layer and second-to-last metal layer. Between MMC layer and lower metal layer there is very thin insulation in form of SiO_2. This layer of insulation is much thinner than between two layers of metal. MMC layer is top plate of MMC capacitor while second-to-last metal layer is bottom plate. Electrical charge is transferred to MMC layer through top metal and VIA. This approach increases significantly the capacitance density of CMOS capacitors. Unfortunately strict design rules regarding this layer are hindering the use of lateral-flux structures. In figure 2 there is presented cross section of lateral-flux structure with use of MMC layer witch marked design rules. Unfortunately publishing exact values of design rules would be a breach of license of the UMC 0.18um technology. Lateral flux is smaller between MMC top plates than metal bottom plated as a result of bigger separation. It is because it is required that MMC layer is enclosed by second to last metal layer by x. The distance between neighboring bottom plates is 0,5x while top plates separation is 5 times bigger. Top-down view of enclosure rule is presented in figure 3.

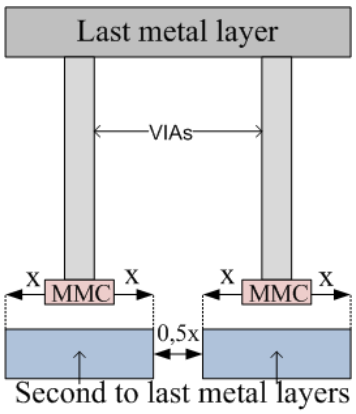

Fig. 2. Localization of MMC metal layer and some of design rules

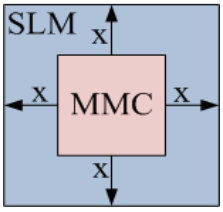

Fig. 3. Top down view of second to last layer and MMC layer with marked enclosure rule

This not only influences lateral-flux but vertical flux as well as area of top plates in lateral-flux capacitors is smaller than area of bottom plates. This paper compares the results of designing fractal lateral flux capacitors with MMC layer and without it.

1. Fractals and quasi-fractal structures

In order to maximize amount of lateral flux a horizontal border between two plates of capacitor need to be as long as possible. One can achieve that by using some fractals as a template for designing a structure. Fractals are self-similar mathematical patterns. Often they are very complicated and not translatable to CMOS topography. As most of fractals are curve based a quasi-fractals structures needs to be designed for implementation. For this three fractals where chosen. Hilbert curve, Peano Curve and Sierpiński fractal which CMOS designs we presented in [4]. They are all space-filling curves and have infinite length in finite area while their fractal number, describing their complexity, is infinite. In [1] capacitor was designed after Koch curve and in [3] Hilbert curve was used, but no direct comparison with other fractal structures was made.

Fractal lines are used as borders between adjacent plates. 11 capacitors where implemented in ASIC:

- Two reference capacitors: one, classic with plates made of two regular metal layers 4 and 5 – called Reference MIM (Metal Insulation Metal), second one is parallel plate MMC capacitor (Referace MMC). All other capacitors will be compared to these two.
- Three capacitors based on three fractals with low complexity number made from two metal layers 4 and 5 – called Hilbert MIM L, Peano MIM L, Siepiński MIM L. Top view of their layouts are presented in, respectively, figure 4, 5, 6.
- Three capacitors based on three fractals with low complexity number made with use of MMC layer – called Hilbert MMC L, Peano MMC L, Sierpiński MMC L. As their design is very similar to MIM L capacitors their layout are not shown.
- Three capacitors based on three fractals with high complexity number made from two metal layers 4 and 5 – called Hilbert MIM H, Peano MIM H, Siepiński MIM H. Their layouts are presented in, respectively, figure 7, 8, 9. In these structures plates are made from thinnest strips of metal possible in this technology in order to achieve longest border between neighboring plates. Plates are the same width as separation between them.

Design of MMC capacitor based on fractals with higher complexity number was not possible because of design rules. All capacitors have the same 50x50μm area. Figures 4 to 9 preserve scale.

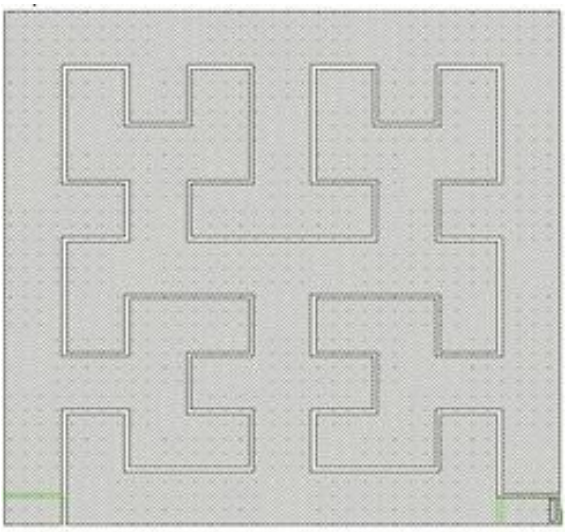

Fig. 4. Layout of Hilbert MIM 2

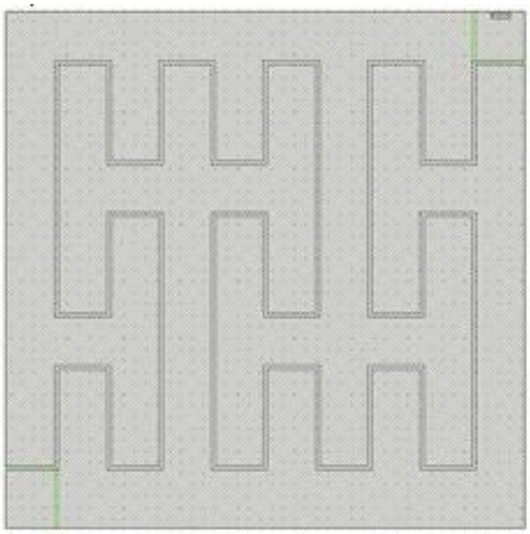

Fig. 5. Layout of Peano MIM 2

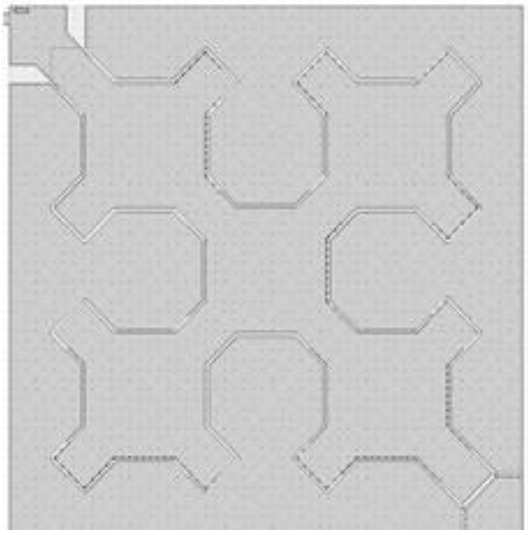

Fig. 6. Layout of Sierpiński MIM 2

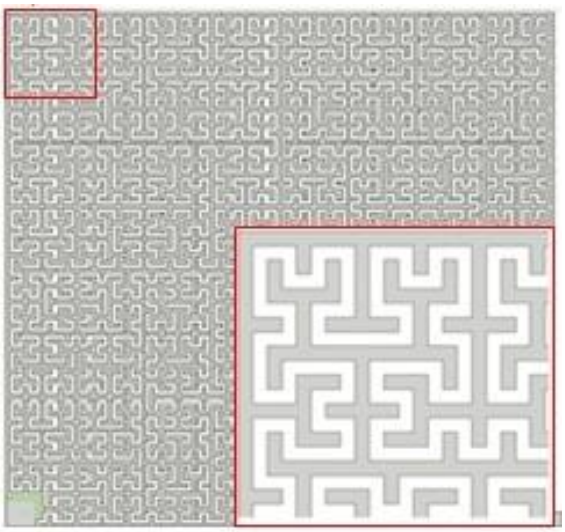

Fig. 7. Hilbert MIM H and zoomed in part of its area

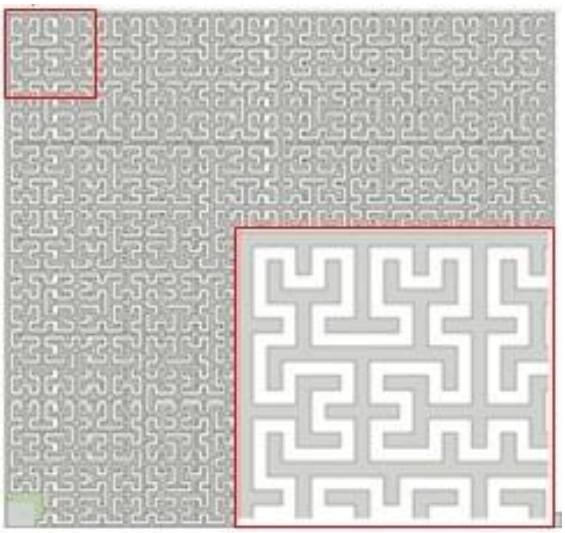

Fig. 8. Peano MIM H and zoomed in part of its area

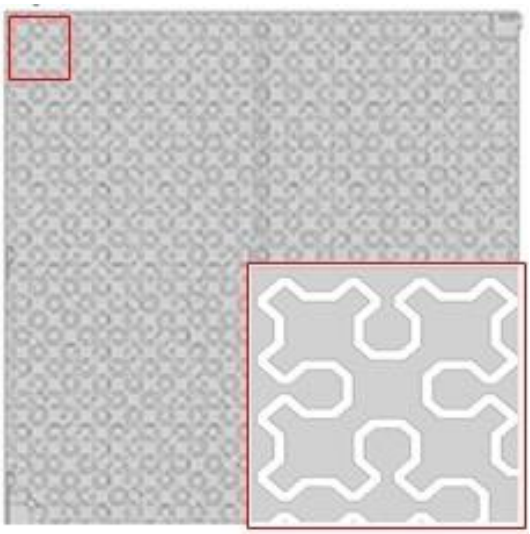

Fig. 9. Sierpinski MIM H and zoomed in part of its area

In order to better visualize difference between structures that use and doesn't use MMC layer a view from different perspective are presented in figures 10 and 11. Scale in figures 10 and 11 are not preserved for clarity.

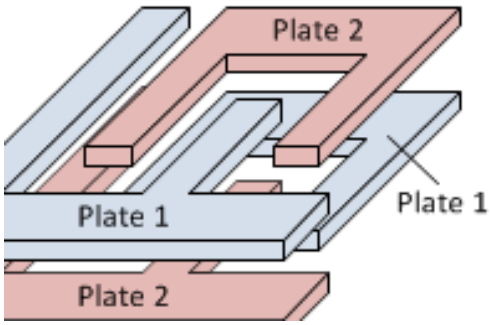

Fig. 10. Different view on MIM structure capacitor

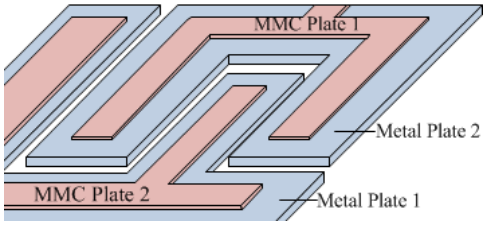

Fig. 11. Different view on MMC structure capacitor

2. Experimental results

After a fabrication of IC, shown in figure 12, capacitance of all structures was measured using probes in 5 chips from one batch. Root mean square and standard deviation of capacitance density were calculated. Results are shown in Table 1.

Tab. 1. Measured capacitance densities of designed structures

Capacitor	Root mean square of capacitance density [fF/μm^2]	Standard deviation [fF/μm^2]
Reference MMC	0,97	0,1
Reference MIM	0,64	0,05
Hilbert MIM L	0,7	0,05
Hilbert MIM H	1,07	0,09
Hilbert MMC L	1,02	0,09
Peano MIM L	0,55	0,05
Peano MIM H	0,77	0,06
Peano MMC L	0,98	0,09
Siepiński MIM L	0,42	0,03
Sierpiński MIM H	0,55	0,05
Sierpiński MMC L	0,78	0,07

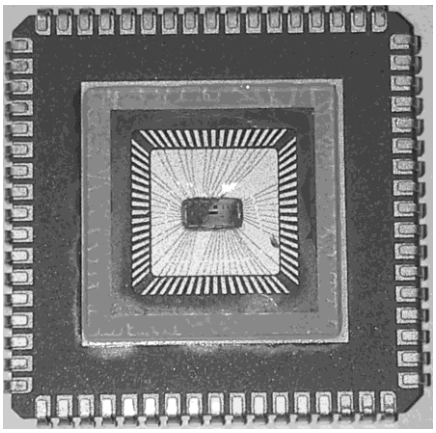

Fig. 12. The IC used for tests

Reference MMC capacitor has a capacitance density of 0.97fF/μm^2 and is 1.5 times bigger than Reference MIM which is as expected. Employing Sierpiński fractal for design of capacitor has opposite effect to indented. Capacitance density for Sierpiński MMC L, Sierpiński MIM L and Sierpiński MIM H is lower than reference capacitors, in fact, in comparison to rest of the structures Sierpiński capacitors have the lowest capacitance density. Use of structure Peano MIM L also gives poor results. In general MIM with low complexity number have capacitance density raised by little or nothing. Capacitors with high complexity: Hilbert MIM H and Peano MIM H, have higher capacitance than reference capacitor. Especially Hilbert MIM H with its 1.07fF/μm^2 capacitance density deserves special interest. Its parameters exceed even MMC capacitors and almost doubles capacitance of Reference MIM. Which is proof that lateral-flux gain is able to do more than compensate of loss of vertical-flux. Unfortunately fractal MMC capacitors have not much better parameters than parallel-plate MMC capacitor. Gain of 0.05fF/μm^2 for Hilbert MMC L does not justify use of much more complicated structure. Use of a lateral-flux structure decreases area of plates in capacitor, which is more severe with very restrictive design rules in UMC 0.18um CMOS technology. Loss of an area of parallel plates and, as a result, vertical flux is too big for lateral-flux to compensate with high gain.

3. Summary

Use of lateral flux capacitors which structure is based on Hilbert curve fractal can almost be half a size of typical parallel-plate capacitor made from two metals. However, if a dedicated layer for creating capacitors is in the disposition to designer, as it was in UMC 0.18um technology, use of fractal capacitors is much less advantageous. If an ASIC is designed in technology that allows for more effective use of lateral-flux capacitors complexity of structures can be increased. Loss of a plate area would not be as severe and thus capacitance density would be higher which in turn means that capacitors can be made on smaller area.

4. Acknowledgements

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