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Development of a Novel Hybrid Multi-Junction Architecture for Silicon Solar Cells

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DEVELOPMENT OF A NOVEL HYBRID MULTI-JUNCTION ARCHITECTURE FOR SILICON SOLAR CELLS

THESIS

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Abstract

Although current technology is capable of producing highly efficient solar cells, these devices remain commercially cost-prohibitive. An alternative low-cost approach was investigated in this research by developing a hybrid multi-junction silicon (HMJ-Si) solar cell architecture through modeling, fabrication, and testing. The HMJ-Si architecture, which consists of stacked silicon solar cells with a 385μm air gap between them, was designed with front and rear metal grating contacts that exploit interference patterns for enhanced light management. The interference patterns were examined in MATLAB® using the Rayleigh-Sommerfeld diffraction formula for 31 distinct wavelengths and 11 plane wave tilts and verified using Lumerical® FDTD Solutions 3D simulation software. Additional development focused on wafer configuration; diffusion profile; front contact design; optical, electrical, and thermal loss reduction; and HMJ-Si efficiency. Results identified the architecture was optimized with an unpolished-front, p-type top cell having 128nm of Si_3N_4 (anti-reflection coating) and butterfly front contact pattern; 400μm-wide rear grating contacts spaced 900μm apart; a polished-front, n-type bottom cell with 200μm-wide grating contacts spaced 1100μm apart; and each cell having an enhanced back surface field diffusion profile with rapidly thermal annealed 500nm silver contacts. Overall efficiency reached 5.35% in a top cell/bottom cell configuration and peaked at 8.42% with an undoped, silver-coated wafer in lieu of the bottom cell. The results show the HMJ-Si architecture is a possible alternative solar cell design but requires additional research for optimization and application.

This work is dedicated to my son, for
we do not inherit the earth from our ancestors;
we borrow it from our children.

Acknowledgments

I would like to express my sincerest appreciation and enduring gratitude to everyone that helped me during this research. Without their support, the ideas and concepts presented below would not have been possible. Foremost, I would like to thank Dr. Coutu for allowing me the opportunity to work with him on this research. His understanding, insight, patience, and encouragement enabled me to successfully navigate the academic world of graduate study.

I would also like to thank my committee members, Dr. Cain and Maj Langley, for providing their expertise and agreeing to preside over my defense. Their contributions were instrumental in furthering this research, which would not have been completed at all without Capt Rob Lake and Capt Tod Laurvick. Their generosity and selfless assistance helped me sustain a productive schedule. Fabrication and testing assistance was also provided by the AFIT clean room technicians, Rich Johnston and Tom Stephenson, as well as Dan Ryan and his team at the AFIT modeling shop. In addition, Capt Tyler Hardy helped me tremendously by providing his expertise of Fourier propagation theory and MATLAB® coding.

Finally, I would like to extend my deepest thanks to Capt John Walton, Lt Alex Gwin, and Lt Tom Donigan, who picked me up when needed and pointed me in the right direction with their invaluable insight. Although the words below may be mine, the following research is a product of teamwork, and I will be eternally grateful.

Rob LaFleur

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List of Symbols

A	Amps	P_{ideal}	Ideal power
A_s	Surface area	P_{max}	Maximum power
A_c	Cross-sectional area	q	Total heat transferred
BN	Boron Nitride	q_i	Internal heat
c	Speed of light in a vacuum	q_l	Heat loss
c-Si	Crystalline silicon	r	Point to point distance
d	ARC thickness	R	Resistance
E	Photon energy	R_p	Percentage of reflection
E_g	Band gap energy	*p-Si*	polysilicon
eV	Electron-volts	SiO_2	Silicon dioxide
HF	Hydrogen Fluoride	Si_3N_4	Silicon nitride
h	Planck's constant	T	Temperature
h_c	Heat transfer coefficient	ΔT	Difference in temperature
I	Current	V	Volts
I_{rr}	Irradiance	V_{oc}	Open-circuit voltage
I_{sc}	Short-circuit current	W	Watts
KOH	Potassium Hydroxide	x_j	Junction depth
k	Thermal conductivity	z	Normal distance
l	Conductor length	σ	Stefan-Boltzmann constant
mA	Milliamps	λ	Wavelength
mW	Milliwatts	η	Efficiency
M_{pp}	Maximum power point	θ_1	Angle of incidence
n_1	Refractive index of material 1	θ_2	Angle of refraction
n_2	Refractive index of material 2	μm	Micrometers
n_s	Combined refractive index	ψ	Leading phase term
nm	Nanometers		

List of Acronyms

ALD	Atomic layer deposition
AM	Air mass
ARC	Anti-reflection coating
BC	Boundary condition
BOE	Buffered oxide etch
BSF	Back surface field
CAD	Computer aided design
CMP	Chemically-mechanically polished
CVD	Chemical vapor deposition
EBSF	Enhanced back surface field
FDTD	Finite-difference time-domain
FF	Fill factor
HMJ-Si	Hybrid multi-junction silicon
IR	Infrared radiation
LIGA	Lithographie, Galvanoformung, Abformung
LTO	Low temperature oxidation
MEMS	Microelectromechanical systems
PECVD	Plasma-enhanced chemical vapor deposition
PMEL	Precision Measurement Equipment Laboratory
PML	Perfectly matched layers
RTA	Rapid thermal annealing
S-Q	Schockley-Queisser limit
STC	Standard test conditions
THD	Total heat dissipation
UAV	Unmanned aerial vehicle
UV	Ultraviolet radiation

DEVELOPMENT OF A NOVEL HYBRID MULTI-JUNCTION ARCHITECTURE FOR SILICON SOLAR CELLS

I. Introduction

Chapter Overview

The purpose of this chapter is to provide an overview of photovoltaic technology by covering its history, importance, and limitations. The research objective is discussed and is followed by the justification, scope, and methodology of experimentation.

1.1. Photovoltaic Technology

In 1839, Alexandre Becquerel discovered the *photoelectric effect* by observing that a battery's current changed when exposed to light [1]. The photoelectric effect (the basic process of turning sunlight into electricity) wasn't fully understood until 1905 when Albert Einstein explained its physics [2]. Almost 50 years later, Bell Labs invented the first silicon solar cell by using *p-n junction* technology to remove electrons that are freed during the photoelectric effect [3]. The combination of these processes—the *photovoltaic effect*—is the basic mechanism for modern solar cells. Initial cells had an efficiency of 6% but quickly improved to 10% by 1958 when they were incorporated into the world's first solar powered satellite, Vanguard 1 [4]. Since then, silicon solar cell technology has continued to evolve, reaching efficiencies above 25% [5]. In addition to satellites, deployed troops can benefit from solar power since it offers the option of remote power units with charging capabilities for radios and other critical electronic equipment. But solar cells are more than an enabling technology for the military; they provide power for electronics, houses, and businesses. The need for a practical renewable energy source will continue to escalate as diminishing resources and growing energy requirements further

strain the existing power supply infrastructure. Solar power is an excellent choice to meet this demand since it is free of emissions, has no fuel costs, and offers decentralized power distribution. However, it is not without limitations; their purchase cost is high because the amount of power delivered by a solar cell depends on sunlight availability and they suffer from low energy densities. A low energy density means that a larger surface area is required to produce an adequate amount of power. Therefore, in order for solar power to shoulder a larger portion of the world's energy demands, solar technology needs to be improved without skyrocketing fabrication costs.

1.2. Research Objective

The goal of this research is to develop an innovative silicon solar cell architecture that improves efficiency without requiring expensive fabrication processes or materials. A combination of photovoltaic, semiconductor, and optical properties is investigated through modeling and experimentation in order to produce a functional hybrid multi-junction silicon (HMJ-Si) solar cell.

1.3. Justification

There has been no documented research into stacked silicon multi-junction solar cells for light trapping and optimization to date. Developing an efficient HMJ-Si architecture will benefit a wide range of both military and civilian applications. Higher efficiencies equate to higher energy densities, less surface area, and less weight. In addition, production costs will be minimal due to the availability of silicon and simplicity of fabrication. The result will be a low-cost solar energy technology suitable for global implementation.

1.4. Scope

The field of photovoltaics has emerging technology from thin-film solar cells to multi-junction architectures. These research areas are aimed at improving solar cell efficiency but are rarely transitioned to real-world applications due to complex designs and expensive fabrication. The following work is focused on developing a novel architecture using only low-cost materials and standard processes. A functional cell was developed by exploring diode orientation, diffusion profiles, front and grating contact geometries, and efficiency losses. Parameters not explored in this research include alternative semiconductor materials, surface patterning, rear contact patterning, and light focusing (concentrated solar cells).

1.5. Methodology

Interference patterns are the primary design component for HMJ-Si cells and were modeled using MATLAB® to determine the most effective grating geometry. The grating was then confirmed using Lumerical® Solutions, a finite-difference time-domain (FDTD) simulation software. In order to transition from modeling to physical testing, a new fabrication process was developed. This modeling, fabrication, and testing approach was used to investigate the best results for each parameter which, after being individually optimized, were integrated into a complete architecture for testing and analysis.

Summary

The chapter provided a general overview of photovoltaic technology by briefly covering its history, importance, and limitations. The research objective was discussed and was followed by the justification, scope, and methodology of experimentation.

II. Background and Theory

Chapter Overview

This purpose of this chapter is to provide an overview of the theory and principles of photovoltaics. Topics discussed include solar cell parameters, limitations, fabrication, and current research. Also included is a brief background on light wave behavior and how it serves as the basis of the HMJ-Si concept.

2.1. The Photovoltaic Effect

The fundamental process in solar cell technology—the *photovoltaic effect*—consists of two basic mechanisms: the interaction between photons and electrons called the *photoelectric effect* and the interface between two doped semiconductor materials known as a *p-n junction* [6].

2.1.1. Energy of a Photon

The photoelectric effect describes how electrons react to light, which travels in the form of individual photons. The amount of energy in a photon depends on its wavelength, λ, described by the Planck-Einstein relation [7]:

$$E = \frac{hc}{\lambda} \tag{1}$$

Where:

E = Photon energy in electron-Volts (eV)
h = Planck's constant; 6.626 x10^{-34} m2 kg/s
c = Speed of light in a vacuum; 2.99 x10^{8} m/s

The amount of energy contained in a photon is important because it can enable an electron to move out of the *valence band* of an atom and into the *conduction band* [8].

2.1.2. Energy Bands

The energy bands around an atom are discrete locations where electrons orbit the nucleus with the valence band being the outermost orbit [9]. A material conducts electricity when its *valence electrons* move into the conduction band and become *conductor electrons*. Conductor electrons are free to move throughout a material because the conduction band is outside the pull of an atom's nucleus. In order for an electron to become a conductor, it must absorb enough energy to overcome the *band gap*, which is the energy difference between the valence band and the conduction band [8]. The amount of energy required, known as the *band gap energy*, E_g, is unique to each material and determines whether it is an insulator, conductor, or semiconductor (Figure 1).

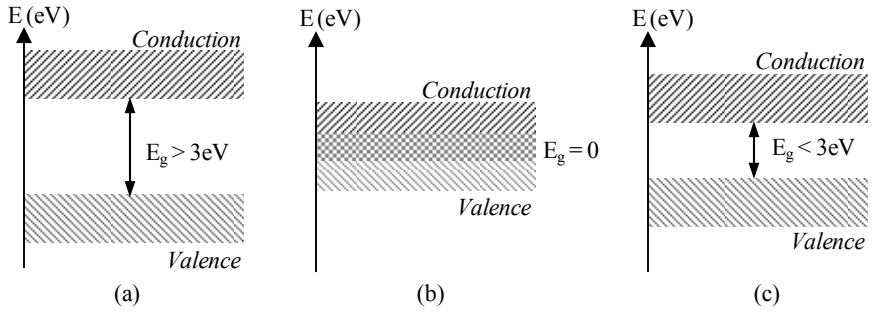


Figure 1. Band gap representations for materials which are (a) insulators, (b) conductors, and (c) semiconductors.

An *insulator* is a material with a high band gap energy that prevents its valence electrons from being freed. Metals are the opposite extreme and excellent *conductors* because their valence band and conduction band overlap [10]. Materials that lie in between, with a band gap energy less than 3eV, are called *semiconductors*. Since semiconductors have such a small band gap, their valence electrons can "jump" into the conduction band if they absorb enough energy to exceed the band gap energy.

For instance, silicon's band gap energy is 1.11eV, which means that electrons are freed for conduction if they absorb photons with wavelengths less than 1117nm. This transfer of energy between photons and electrons is the photoelectric effect. However, electrons are prone to falling right back into the hole they left behind during a process called *recombination* [11]. This phenomenon prevents electrons from being free long enough to become conductors and can be avoided by incorporating a p-n junction.

2.1.3. Semiconductor Junctions

A p-n junction is an interface between two differently doped semiconductor materials. An undoped semiconductor material, like silicon, bonds perfectly with other silicon atoms and creates a crystal lattice structure (Figure 2a). This structure forms because silicon atoms have four valence electrons and naturally want eight [10]. Pure undoped silicon is a poor conductor because there are no vacancies, or holes, for electrons to move into. This restriction to electron flow is removed by replacing some of the lattice atoms with other atoms through a process called *doping* [12]. For instance, when a silicon atom is replaced with a boron atom, there is an extra hole because boron has only three valence electrons (Figure 2b). This material is known as *p-type* because having one less electron makes its net charge is *positive*.

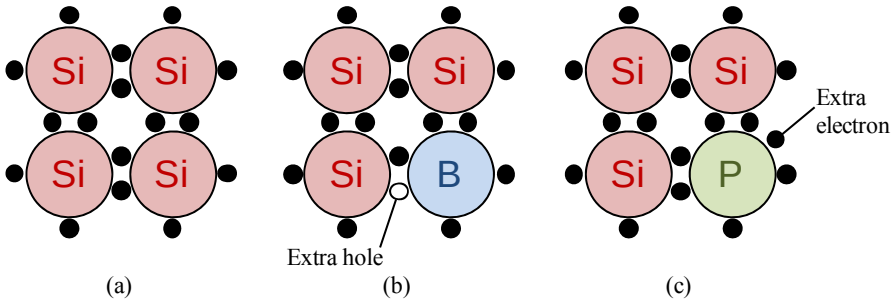


Figure 2. Semiconductor lattice structures: (a) pure silicon; (b) p-type silicon doped with boron; (c) n-type silicon doped with phosphorous.

If phosphorous is used as the dopant instead of boron, the lattice has an extra electron and becomes an *n-type* material with a net *negative* charge (Figure 2c). When n-type silicon comes into contact with p-type silicon, a *homojunction* is formed. Homojunctions are a particular type of p-n junction created by using the same material on each side of the interface. *Heterojunctions* are also p-n junctions, but result from the interface between different materials (e.g. p-type gallium and n-type arsenic) [13].

When a p-n junction is formed, extra electrons in the n-type material near the junction move towards the extra holes, leaving behind positively charged ions [8]. Similarly, extra holes in the p-type material move to combine with the electrons, leaving behind negatively charged ions. These *electron-hole pairs* keep forming until the area they occupy is too wide for any additional electrons or holes to move across. The result is an area of semiconductor material without any extra holes or electrons called the *depleted region* [8]. The abandoned ions in the depleted region remain fixed and form an electric field which pulls electrons away from their holes before they have a chance at recombination (Figure 3). Once an external circuit is connected, the electrons are able to carry an electric current and perform work until they recombine in the p-type material.

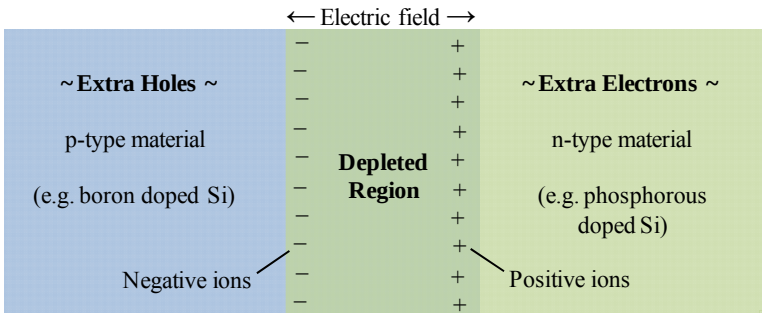


Figure 3. Representation of a depleted region and electric field from the p-n junction interface between n-type and p-type materials.

2.1.4. Solar Cell Operation

Using a p-n junction to separate electrons freed by the photoelectric effect is the photovoltaic process and the foundation of solar cell technology. In order to construct a solar cell, an *extrinsically doped* semiconductor material like p-type silicon is doped with n-type impurity atoms to create a p-n junction. When photons are absorbed by electrons in the depleted region, the resulting current flows through an external circuit connected to the cell via front and rear metal contacts (Figure 4). This is the basic process of solar cell operation and helps identify the parameters that affect their performance.

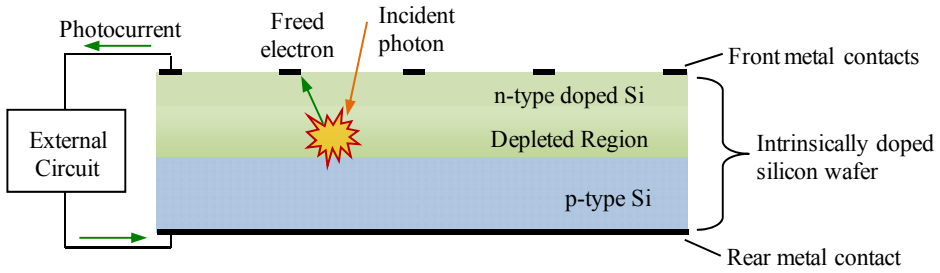


Figure 4. Cross sectional view of a basic silicon solar cell. Incident photons enter the silicon and, when absorbed in the depleted region, create photocurrent in the form of freed electrons. The electrons are collected by the front metal contact, perform work in an external circuit, and return to the rear of the solar cell.

2.2. Solar Cell Parameters

Solar cells are similar to batteries in that they supply power in the form of voltage and current. The built-in voltage across an unbiased silicon solar cell is roughly 0.5V, which is due to the electric potential across the depleted region [10]. Since the depleted region in silicon remains unchanged after it is formed, the voltage does not vary with incident light. This means that the amount of power a solar cell provides depends largely on the *photocurrent* it produces, which is the amount of electrons freed from the photovoltaic process [14].

2.2.1. Drift Velocity

The amount of photocurrent depends on the availability of photons, but how easily the electrons move or "drift" through a material depends on two factors. First, as a material's temperature rises, its atoms oscillate from the heat. These oscillations reduce drift velocity from electrons colliding with atomic nuclei. The second is the type of dopant used in silicon. An extra electron in n-type silicon is free to drift through a material until it finds a hole; an extra hole in p-type silicon only moves when an adjacent electron moves to fill it in. Another adjacent electron must move to fill in the new hole location and so on, making hole mobility (450 cm^2/Vs) much slower than electron mobility (1400 cm^2/Vs) [15].

2.2.2. Power

The maximum photocurrent a solar cell can produce, the short-circuit current (I_{sc}), is measured using *standard test conditions* (STC) of 1kW/m^2 incident light at 25°C [16]. This is multiplied by the maximum voltage, or open-circuit voltage (V_{oc}) to determine the ideal power (P_{ideal}) a solar cell is capable of producing [17]:

$$P_{ideal} = I_{sc} \cdot V_{oc} \quad (2)$$

2.2.3. IV Curve

A solar cell does not actually provide the amount of power shown in Equation 2 because external loads have resistances that limit power output. A graph that shows the actual power output of a solar cell with respect to varying resistance is known as its *characteristic curve* or *IV curve* (Figure 5) [18]. For example, point (a) represents a load with a small resistance and voltage, which results in a large amount of current (near I_{sc}).

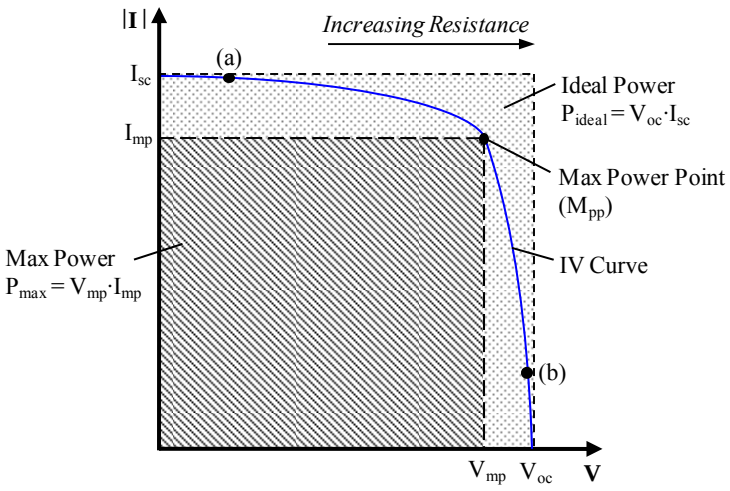


Figure 5. Example of a characteristic IV curve of a solar cell. Points (a) and (b) represent equivalent amounts of power delivered to devices with small and large resistances, respectively. The fill factor (FF) is the ratio of max power to ideal power and measures the "squareness" of the IV curve.

As the resistance increases, the point shifts along the curve to the right, altering the available power. Point (b) represents a load with high resistance and voltage that results in a small amount of current. Thus, the same amount of power can be delivered to different loads depending on the IV curve and resistance values. The point at which a solar cell provides its maximum power (P_{max}), known as the *maximum power point*, M_{pp}. This point represents the largest rectangular area under the IV curve and has corresponding current and voltage values of I_{mp} and V_{mp}. The maximum amount of power is considered as the *actual power* a solar cell can deliver.

2.2.4. Fill Factor

The maximum power of a solar cell is also important because it identifies the *fill factor (FF)*, which is the ratio of a solar cell's maximum power to its ideal power [19].

$$FF = \frac{V_{mp} \cdot I_{mp}}{V_{oc} \cdot I_{sc}} = \frac{P_{max}}{P_{ideal}} \tag{3}$$

The fill factor can be thought of as "derating" the power output at M_{pp}; it identifies how "square" the IV curve is. Typical *FF* values for silicon solar cells range from 0.75 to 0.85, which translates to a 15-25% power loss [14]. The power a solar cell actually produces, P_{max}, is the main component in determining relative *efficiency*, which is the industry standard means of solar cell comparison.

2.2.5. Efficiency

The efficiency, η, of a solar cell is a measure of how much *irradiance* (I_{rr}) is turned into electricity. It is defined as the ratio of derated power to total input power (P_{in}) expressed as a percentage [20]:

$$\eta = \frac{P_{max}}{P_{in}} \times 100\% \tag{4}$$

For example, a $4cm^2$ solar cell that generates 50mW of power has an efficiency of 12.5% based on the STC irradiance of $1kW/m^2$ for P_{in} [16]:

$$\eta = \frac{0.05W}{1000W/m^2} \times 100\% = \frac{5W}{0.1W/cm^2 \cdot 4cm^2} = 12.5\%$$

Even with an ideal fill factor of 1.0, silicon solar cells are only capable producing a limited amount of power due to recombination and particle flux. The *detailed balance technique* was developed in 1961 to determine the theoretical limit of solar cell efficiency; calculated to be 30% for silicon [21]. This efficiency ceiling, commonly referred to as the *Schockley-Queisser (S-Q) limit*, assumes the complete absorption of photons with $E_g > 1.11eV$. Thus, in order to reach that limit, maximum photon absorption is required. However, there are additional factors that must be taken into account for the efficiency ceiling to be realized.

2.3. Solar Cell Limitations

There are three categories of processes that affect the amount of power a solar cell delivers. *Optical losses* result from the behavior of light, *electrical losses* are due to the nature of electron mobility, and *thermal losses* degrade efficiency via excess heat. Reducing these losses is a critical aspect of any effective solar cell design.

2.3.1. Optical Losses

Some of the light that reaches a solar cell is reflected away by the front metal contacts. The contacts are necessary to transport photocurrent to an external circuit but consume valuable surface area on the front of the solar cell. In order to mitigate this type of loss, front contact designs are critical for optimized absorption [22]. However, not all of the light that reaches exposed silicon is absorbed; 30-35% is lost due to the reflection of perpendicular light on a surface given by [23, 24]:

$$R_p = \left(\frac{n_1 - n_2}{n_1 + n_2} \right)^2 \times 100\% \tag{5}$$

Where:

R_p = Percentage of reflection
n_1 = Refractive index of material 1
n_2 = Refractive index of material 2

For instance, 950nm light traveling through air ($n = 1$) reaching a silicon solar cell ($n \approx 3.6$) results in almost 32% reflectance [25]:

$$R_p = \left(\frac{1 - 3.6}{1 + 3.6} \right)^2 \times 100\% \approx 31.9\%$$

Previous research into reducing the amount of reflected light resulted in the creation of *anti-reflection coatings* (ARCs). An ARC is a thin layer of material deposited onto the front of a solar cell that is engineered to absorb more photons. It does this by

reflecting wavelengths that are cancelled out by the incoming light due to destructive interference (see Section 2.6). The result is, in effect, zero-reflectance at the desired wavelength, λ, described by [14]:

$$d = \frac{\lambda}{4n_s} \tag{6}$$

Where:

d = Thickness of the anti-reflective coating
n_s = Combined refractive index of air and silicon: $n_s = \sqrt{1 \cdot 3.6} \approx 1.9$

This means that more photons are available to generate photocurrent, as long as they strike an electron-hole pair. This is not always the case; photons can propagate through silicon without ever being absorbed during a process called *transmission*, which is the other type of optical loss that solar cells experience (Figure 6). One method used to reduce transmissive losses is a second depleted region at the rear of the cell created by another homojunction. However, this back-side homojunction is *not* a p-n junction; it is

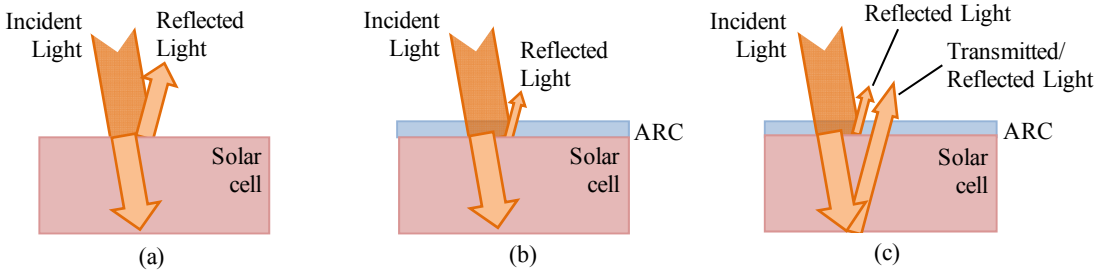


Figure 6. Solar cell optical losses showing (a) 30-35% loss from bare silicon reflection, (b) reduced reflection losses from an anti-reflective coating (ARC), and (c) transmission losses when photons are reflected out of the solar cell.

formed using a dopant that *matches* the extrinsic doping of the substrate. The result is a "heavy" doped region typically annotated p^+ for p-type materials and n^+ for n-type materials (Figure 7).

For instance, a p-type silicon wafer doped with phosphorous for the primary depleted region and boron at the rear creates an n-p-p^+ diffusion profile known as a *double drift region diode* [26, 27, 28, 29]. A secondary depleted region is formed from the difference in doping concentrations which contribute to photocurrent by absorbing transmitted photons. Adding this heavy-doped homojunction at the rear of the cell not only cuts down on transmission loss, it reduces electrical loss as well.

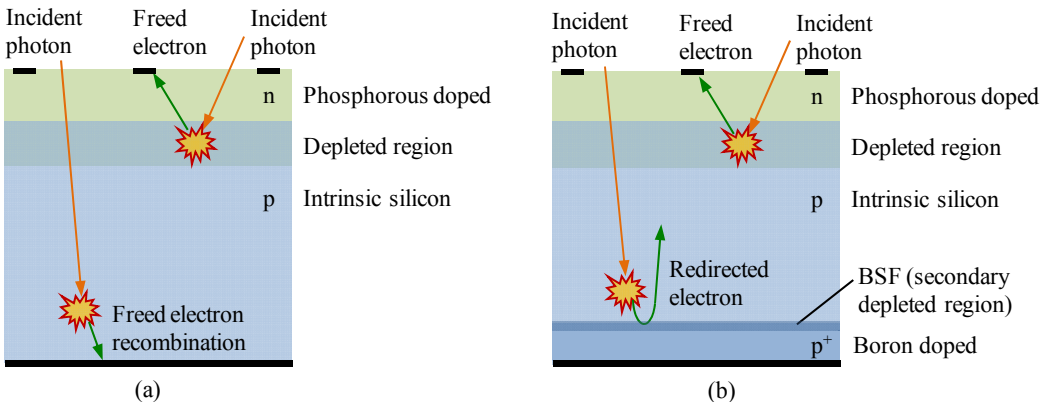


Figure 7. A cross-sectional diagram showing (a) rear-surface recombination losses in standard n-p solar cells and (b) how a back-surface field (BSF) reduces recombination by using a p-p^+ interface to redirect electrons toward the primary depleted region.

2.3.2. Electrical Losses

In solar cells, the secondary depleted region is known as a *back surface field* (BSF). The electric field created by the BSF increases efficiency by redirecting electrons toward the primary depleted region and reducing recombination at the rear contact (Figure 7). Without a BSF, electrons freed from photon absorption are prone to recombination since they are located outside of the primary depleted region [14].

The BSF also limits *dark current*, which is a small amount of current present in a solar cell when there is no incident radiation. Reducing this current leakage helps increase the open-circuit voltage by dividing the overall voltage drop between the BSF

and the p-n junction [30]. Although the voltage drop is decreased, the electric field across the cell remains unchanged and recombination is reduced. However, a BSF alone does not completely eliminate electrical losses; the freed electrons still need to exit the solar cell in order to perform work. Transitioning from silicon to metal means that electrons must overcome the microscopic gaps from mismatched material surfaces at their interface. These imperfections reduce efficiency by slowing electron drift unless an *ohmic contact* is created. An ohmic contact is a metal-semiconductor junction with low resistance that depends on the work functions of each material. For p-type semiconductors the work function must be lower than that of the metal, and vice-versa for n-type semiconductors. The ohmic contacts in either case are usually created through a process of quick heating and cooling called *rapid thermal annealing* (RTA) [13, 31]. Ohmic contacts significantly increase electron drift by lowering the resistance encountered by photocurrent as it exits the cell. However, the resistance from increased heat must also be mitigated for maximum solar cell efficiency.

2.3.3. Thermal Losses

Heat is transferred in three ways: radiation, convection, and conduction. *Thermal radiation* is the emission of electromagnetic energy from an object at a given temperature [32]. The amount of heat transferred, q, is described by:

$$q = \sigma A_s T^4 \tag{7}$$

Where:

σ = Stefan-Boltzmann constant
A_s = Surface area
T = Temperature

Convection is the transfer of heat between a surface and a moving fluid (which can be a liquid or a gas). There are two types of convection: forced and natural. Forced convection occurs when the fluid movement is induced by an external pump or fan whereas natural convection is a result of the buoyancy created from a thermal differential [33]. The amount of heat transferred in either case depends on both the amount of surface area and convective heat transfer coefficient of the material explained by Newton's law of cooling:

$$q = h_c A_s \Delta T \tag{8}$$

Where:

h_c = Heat transfer coefficient
A_s = Surface area
ΔT = Difference in temperature between material and surrounding fluid

Conduction results from two materials with different internal temperatures coming into contact with one another. Energy is transferred between them from a combination of electron diffusion and kinetic energy caused by vibrating molecules [34, 35]. The total rate of thermal conductivity depends on the material since metals have high electron diffusion and non-metals primarily transfer heat through structural vibration. In general, the total amount of conductive heat transfer across a distance, D, is explained by Fourier's simplified law of conduction:

$$q = \frac{k A_c \Delta T}{D} \tag{9}$$

Where:

k = Thermal conductivity of the material
A_c = Cross-sectional area
ΔT = Difference in temperature across the material

Reducing the heat in a solar cell is important since higher temperatures reduce efficiency; every 1°C rise causes power output to degrade by 0.4 to 0.5% [14]. Although sunlight imposes heat in the form of infrared radiation, cells also generate heat internally as they experience the photovoltaic effect. The amount of internal heat is a function of three mechanisms: photocurrent, low-energy photons, and high-energy photons [36]. As any current (I) moves through a semiconductor material, it encounters resistance (R) in the form of structural molecules as well as the p-n junction. This resistance generates heat, which is modeled as power loss or joule heating given by:

$$q = I^2 R \tag{10}$$

Another source of heat generation in solar cells is due to low-energy photons. These photons have energy levels lower than the band gap of the semiconductor material and therefore aren't absorbed. However, they still interact with molecules and create heat via phonon or atomic lattice vibrations. The last source of heat is from photons that have energy much higher than the material's band gap. These photons excite electrons into the conduction band, but with an excessive amount of energy. Once the electrons settle into the conduction band, this additional energy is dissipated as heat.

Combining the three types of internally-generated heat with the amount lost from heat transfer gives the total amount of heat (q) in a solar cell as [36]:

$$q = q_i - q_l \tag{11}$$

Where:

qi = Total internal heat generated
ql = Total heat loss (dissipation)

Solar cells eventually reach an elevated thermal equilibrium as the amount of cooling matches the amount of heat generated. Their temperature is typically managed through convective cooling systems because maintaining a low cell temperature is critical in maximizing efficiency. This is shown in Avrett's test results, which indicate that photocurrent decreases roughly 0.015mA per 1°C rise in temperature [36].

Considering the efficiency degradation from heat in conjunction with optical and electrical losses, it is clear that the reduction of all three is necessary to create solar cells capable of reaching the S-Q efficiency limit. Although these limitations are primarily considered during design, they also impact how solar cells are fabricated.

2.4. Solar Cell Fabrication

Commercial solar cell processing typically involves four steps: diffusion (doping), ARC application, contact forming, and annealing [14]. With the exception of contact forming, which for solar cells is done using a process called *screen printing*, these techniques are also common in microelectromechanical systems (MEMS) fabrication.

2.4.1. Diffusion

A p-n junction requires dopant atoms for electron mobility. These atoms are introduced through a process called *diffusion* where impurity atoms are driven into the silicon substrate at temperatures between 900°C and 1200°C [37]. This happens in three ways: substitution, displacement, and interstitialcy. Substitution is when the impurity atom consumes a lattice vacancy, displacement occurs when the impurity atom "pushes" out a lattice atom and takes its place, and interstitial atoms are impurities that reside in between the lattice atoms without any displacement.

The most common impurity atoms for silicon are boron (p-type) and phosphorous (n-type). As previously mentioned, the inclusion of these impurity atoms is critical to the formation of a p-n junction and the photovoltaic process. The time and temperature of the diffusion process determines how far the impurity atoms are driven into the substrate. These atoms enter the material vertically and laterally, but because solar cells are doped without any masking, lateral diffusion effects are negligible. The resulting depth of the dopant atoms, known as the *junction depth (x_j)*, indicates where the impurity concentration reaches zero (Figure 8).

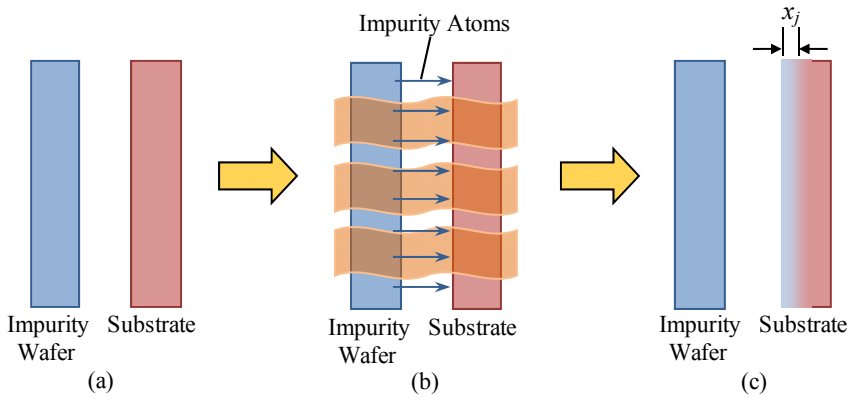


Figure 8. The diffusion process: (a) a source impurity wafer such as boron is placed ≈1/4" away from the silicon substrate wafer and (b) placed into an oven between 900-1200°C where impurity atoms are driven into the substrate to create (c) a junction depth (x_j) that depends on time and temperature in the furnace.

2.4.2. Anti-Reflection Coating Application

The two main types of ARCs for silicon are silicon dioxide (SiO_2) and silicon nitride (Si_3N_4) [14]. However, due to a better reflection factor (less than 1%), silicon nitride has become the industry standard. Once this layer has been deposited, which is typically done using a *chemical vapor deposition* (CVD) process, the wafer is ready for metal contacts.

2.4.3. Contact Forming

Massed produced solar cells rely on screen printing, which uses a metal paste applied to a mask that rests on the silicon [38]. When the mask is removed, the remaining metal makes up the cell's front contacts. This technique is quick but results in poor contact integrity and inconsistent thickness. More robust and consistent contacts can be fabricated using metal deposition, which deposits metal onto wafers via CVD, *atomic layer deposition* (ALD), or *physical deposition* [12]. CVD uses a chemical reaction to provide high-quality films such as ARCs and is useful for high-aspect ratio devices due to its conformal nature. A variation of CVD is ALD, which deposits one atomic layer at a time. However, since solar cell efficiency relies on thick contacts that are highly conductive, ALD is not an applicable method of photovoltaic processing.

Sputtering also deposits one atom at a time, but during a physical deposition process that does not typically include a chemical reaction. It is based on a ballistic exchange of momentum; atoms are deposited onto the wafer after being ejected from a target that was bombarded by ions formed by a plasma. In order to avoid the conformal coating inherent in sputtering, another type of physical deposition is used: *evaporation*. This method heats metal to its evaporation temperature, transferring it to a wafer where it condenses. Since the metal sits in a crucible directly below the wafer, it is evaporated in straight lines and is not conformal. This method enables follow-on processing such as metal-lift off, which uses a solvent to attack the material beneath unwanted portions of metal so it can be lifted away. The remaining metal is then partially diffused into the silicon by putting the wafer into an annealing oven during the RTA process.

2.4.4. Annealing

Annealing is the process of heating and cooling a metal in order to remove internal stress. RTA is a variation of this process that quickly heats and cools a wafer in order to form an alloy between the metal and the silicon. Various annealing profiles have been developed and range from five seconds to over three minutes at temperatures between 400°C and 1100°C [39, 40]. The type of metal being annealed determines the temperature used in the process, which is selected below the metal's melting point. The duration of the RTA depends on the type of metal as well, but must also take into account the type of substrate. A variety of time-temperature optimization results are available to help determine the best parameters for ohmic contact creation without increasing sheet resistance [41, 42]. Although the RTA process is a critical step in creating efficient solar cells, it is also used in both microelectronic and MEMS fabrication.

2.4.5. MEMS Fabrication

There are three major types of MEMS fabrication techniques: bulk micromachining, surface micromachining, and high-aspect ratio processing [31, 32]. *Bulk micromachining* is a subtractive process that consists of etching into a substrate wafer to create devices (Figure 9a). For example, ink-jet printer nozzles can be fabricated by etching a small hole through a silicon wafer. This type of fabrication depends largely on the crystalline structure, how the material responds to different etching chemicals, and the thickness of the substrate. Since most wafers are less than 925μm thick (typically 300-500μm), devices fabricated using this technique have limited heights [43].

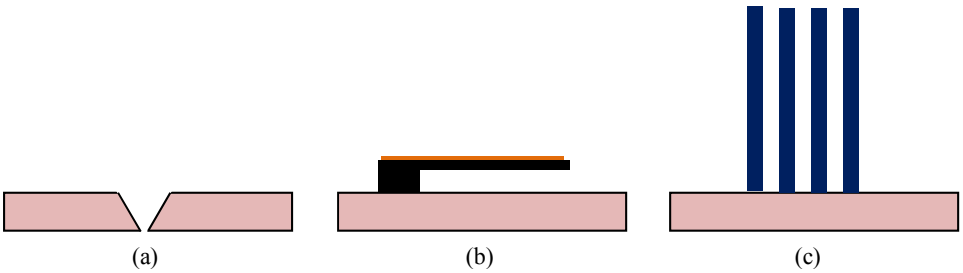


Figure 9. MEMS fabrication processes examples: (a) a micro-jet nozzle created using bulk micromachining (subtractive processing); (b) a MEMS bimorph cantilever beam fabricated by adding and etching layers during surface micromachining; and (c) a high-aspect ratio structure constructed using the LIGA process.

In contrast, *surface micromachining* is an additive process that adds thin layers of material onto a substrate (Figure 9b). This process is versatile since a wide range of substrates and materials are available for processing which can create complicated devices such as moving gears. Surface micromachining has countless applications but similar to bulk micromachining, devices produced with this technique have limited heights. As more layers are added and etched to form structures, the nature of the etching reduces the ability to achieve tall, smooth vertical walls.

In order to address the need for these types of devices, high-aspect ratio processing was developed and can create devices with heights 100 times greater than their width. This technique is based on the German process "*Lithographie, Galvanoformung, Abformung*" (LIGA) which means lithography, electroplating, and molding. This process is capable of producing tall structures with high aspect ratios through either injection molding or stamping (Figure 9c, Figure 10). The metal molds are created by electro-plating the gaps left behind after exposing a light-sensitive material to X-rays or UV-rays. This fabrication step, known as *photolithography*, is commonly used to create microelectronic and MEMS devices.

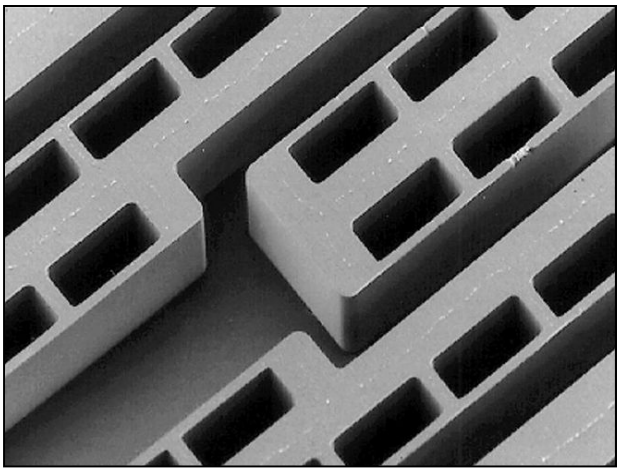


Figure 10. Scanning electron microscope (SEM) image of a 20:1 aspect-ratio LIGA-fabricated structure. Device height: 120μm; smallest width: 6μm [44].

Photolithography consists of applying, exposing, developing, and etching a light-sensitive material called *photoresist* or *resist* [12]. First, the resist is applied in liquid form onto a substrate wafer. The wafer is spun at a certain speed to spread the resist evenly across its surface. Once it has been spread, the wafer is heated to harden or set the resist. The next step is exposure, which projects an ultraviolet (UV) light through a specifically designed mask that is placed between the light source and the wafer. The resist responds to the light in one of two ways: *positive photoresist* has chemical bonds that are weakened, making it more soluble; *negative photoresist* responds by creating longer polymer chains that result in the resist becoming more robust.

After exposing, the wafer is submerged in a chemical that attacks the weaker resist. Similar to photography, the developing process brings out the image that was transferred by the mask. The final step is etching, which removes any remaining unwanted resist. Without photolithography and MEMS processing techniques, research into many of the emerging solar cell designs would not have been possible.

2.5. Current Solar Cell Research

Contemporary photovoltaic research trends are focused on a variety of techniques to enhance efficiency. The most common of these include organic photovoltaics, thin-film solar cell light trapping techniques, and multi-junction solar cell architectures.

2.5.1 Organic Photovoltaics

An alternative to silicon-based solar cells are organic solar cells. Also known as plastic solar cells, this technology uses conductive organic polymers which enables applications such as flexible solar cells on the wings of unmanned aerial vehicles (UAVs) [45, 46]. In addition to being flexible, they weigh less than silicon solar cells and can be designed to fit a variety of different applications. However, organic solar cells have much lower efficiencies—barely 8%—and are prone to photochemical degradation [47, 48].

2.5.2 Thin-film Solar Cells

Another solar cell technology being researched is thin-film solar cells. These cells range in thickness from half the width of a human hair down to only a few nanometers and can be either organic or inorganic [49]. Although their extreme reduction in thickness allows versatile applications, they experience an increase in reflection and transmission, limiting efficiencies to around 20% [5]. Researchers are developing a myriad of light trapping techniques to overcome the limited efficiency of thin-film solar cells. The idea for light trapping is to provide the longest possible path for photons to travel so they have more opportunity for absorption. Methods are currently focused on front grating surfaces and morphology [50, 51, 52, 53, 54, 55]; internal diffraction structures [56, 57, 58]; and rear contact grating surfaces [59, 60, 61].

2.5.3. Multi-junction Solar Cells

The most solar radiation can be absorbed and converted into photocurrent using multi-junction solar cell architectures, which are stacked semiconductor materials. Each material has a unique band gap and absorbs only a portion of the electromagnetic spectrum allowing subsequent cells with lower band gaps to capture the rest [62, 63]. In effect, each material is a solar cell that contributes to combined photocurrent (Figure 11).

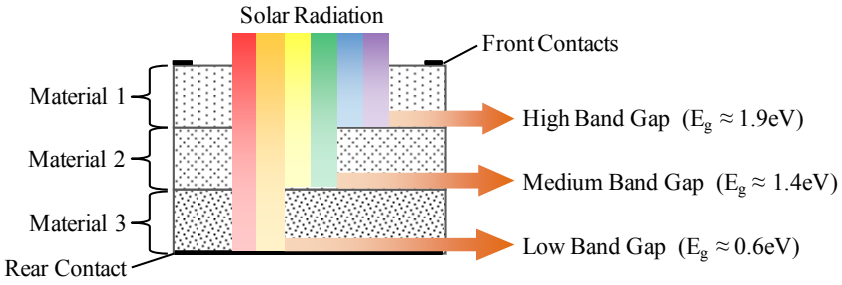


Figure 11. Representation of a multi-junction solar cell. As radiation enters the cell, high band gaps are absorbed by material 1, medium band gaps by material 2, and low band gaps by material 3 to produce high-efficiency cells.

By stacking these cells, engineers have been able to obtain a record high efficiency of 46.0% [5]. Although the theoretical limit for multi-junction solar cells is 86.8%, the cost and complexity of these architectures render them inadequate for mass production [64]. The global proliferation of solar cells as a renewable energy source can only be realized by combining advanced light trapping techniques with low-cost fabrication, which can be achieved by exploiting the natural behavior of light.

2.6. Properties of Light

Electromagnetic radiation can be described in two distinct ways; as particles and as propagating waves. Each of these characteristics can independently help increase solar cell efficiency under the proper conditions.

2.6.1. Particles

The concept that light behaves like a stream of particles, or rays, is based on Isaac Newton's experiments with *reflection* and *refraction* [65]. Reflection is the result of light interacting with a non-transmissive medium when light rays are redirected away from a surface in either a *specular* or *diffuse* nature [11]. Specular reflection is when a ray strikes a flat surface that reflects it away at an angle equal to its angle of incidence (Figure 12). Diffuse reflection is when a ray strikes a rough surface that reflects it in every direction. An example is a paved road that is dull (diffuse) when dry and appears reflective (specular) when wet. This happens because water fills the imperfections in the road, making it a specular surface that reflects light more directly.

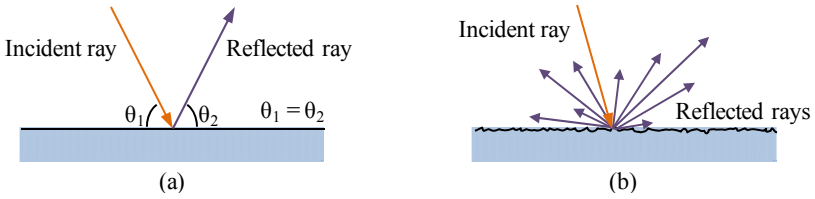


Figure 12. Types of light ray reflection: (a) specular reflection occurs on flat surfaces where the angle of incidence (θ_1) is equal to the angle of reflection (θ_2) and (b) diffuse reflection is the result of light ray dispersion due to surface roughness.

When light enters a medium that is at least partially transmissive, it experiences a shift in direction due to the change in *refractive indexes* (Figure 13) [23]. The refractive index indicates how easily light can travel through a medium. The change in direction is defined in terms of its angle of refraction (θ_2) and depends on its angle of incidence (θ_1) described by Snell's Law [66]:

$$n_1 \cdot \sin\theta_1 = n_2 \cdot \sin\theta_2 \tag{12}$$

Where:

n_1 = Refractive index of material 1
n_2 = Refractive index of material 2

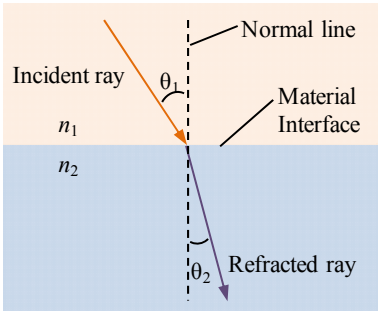


Figure 13. The result of light rays travelling from one medium into another is refraction. The angle of refraction (θ_2) depends on the refractive indexes (n_1, n_2) and angle of incidence (θ_1).

Refraction and reflection are often design considerations when seeking to reduce optical loss in solar cells, such as with ARCs (see Section 2.3.1). Depositing an ARC onto a rough surface further increases absorption by creating a diffuse surface that takes advantage of the resulting angle of refraction. As incident light is refracted by the rough surface, it has a second chance at being absorbed by an adjacent peak. Combined gains from ARCs and surface roughness reduce solar cell reflection to ≈3% [14]. However, light cannot completely be explained through ray modeling; it can also behave like waves, which have their own unique set of characteristics and behaviors.

2.6.2. Waves

The wave nature of light, which was first posited by Christiaan Huygens in 1678, was proven by Thomas Young's double-slit experiment in 1801 [67, 68]. In the experiment, a plate was fabricated with two small parallel slits in it. It was illuminated by a laser with the expectation that two matching bands of light would be seen on the detector behind the plate. However, a *diffraction pattern* was observed instead, which is a result that cannot be generated by particles. Diffraction is the result of a wave encountering an obstruction that alters its nature (Figure 14a).

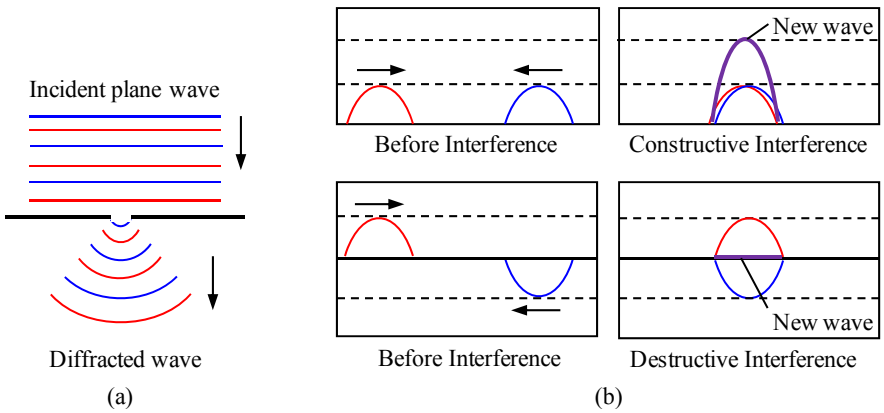


Figure 14. Examples of the wave nature of light: (a) diffraction from light waves interacting with an obstacle and (b) constructive and destructive interference from two coherent waves overlapping.

The specific type of diffraction that Young observed was an *interference pattern*, which was created because the waves were *coherent*. Coherence is when two waves have the same phase and frequency. If two coherent waves interact with each other and their peaks overlap, the result is *constructive interference*; when a peak meets a valley, the result is *destructive interference* (Figure 14b) [69]. Therefore, the pattern that emerged from the double-slit experiment proved that light also behaves like a wave (Figure 15).

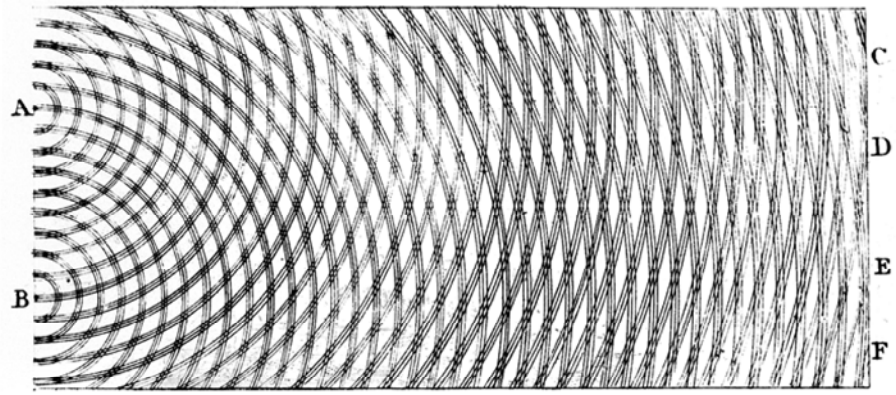


Figure 15. Thomas Young's 1803 sketch of interference patterns resulting from the double-slit experiment in which two diffracted coherent waves emerged from slits in a screen. The result was constructive and destructive interference [70].

Since the constructive and destructive interference bands are a result of the slit size and the distance the waves travel as they interfere, the width and periodicity of the bands can be specified. Taking advantage this phenomenon to reduce photon reflection by placing solar cell contacts within the destructive interference bands is the basis of the HMJ-Si concept.

2.6.3. Propagation

Considering light as a series of waves offers the application of wave formulas that represent electromagnetic propagation. Mathematical expressions that account for intensity and phase have enabled the theoretical study of light wave behavior for decades. One of the most accurate representations, known as the *Rayleigh-Sommerfeld diffraction formula*, describes light propagation from a point (*x,y*) to another (*w,s*) based on a two-dimensional *Fourier transform* [24]:

$$U(w,s) = \frac{z}{j\lambda}\int_{-\infty}^{\infty}\int_{-\infty}^{\infty}\frac{U(x,y)\cdot\exp\left(\frac{j2\pi}{\lambda}\sqrt{z^2+(w-x)^2+(s-y)^2}\right)}{z^2+(w-x)^2+(s-y)^2}\partial x\partial y \qquad (13)$$

Where:

U(x,y) = Field in the original *x-y* coordinate plane
U(w,s) = Field in the resulting *w-s* coordinate plane
z = Normal distance between planes
λ = Wavelength

It is important to note that certain approximations must be made due to the infinite nature of light and limited computational capabilities. This means that mathematical models are only accurate to a certain degree and can't account for every anomaly or optical aberration.

However, in certain situations the approximations simplify the formulas without significantly reducing the fidelity of the models. For example, if the normal distance is so large that it is approximately equal to the point-to-point distance, the result is the simplified *Fresnel approximation formula* [24]:

$$U(w',s') = \frac{\psi}{j\lambda z}\int_{-\infty}^{\infty}\int_{-\infty}^{\infty} U(x,y)\cdot\exp\left(\frac{j\pi(x^2+y^2)}{\lambda z}\right)\cdot\exp\left(-j2\pi(w'x+s'y)\right)\partial x\partial y \quad (14)$$

Where:

ψ = Leading phase term: $\exp\left(j2\pi z\right)\cdot\exp\left(j\pi\lambda z(w'^2+s'^2\right)$
U(w',s') = Modified resulting field with *w'* = $w/\lambda z$ and *s'* = $s/\lambda z$

Another simplified approximation applies when the normal distance is much larger than the point-to-point distance divided by the wavelength. Known as the Fraunhofer approximation formula, this is the simplest expression for the propagation of light that can be used [24]:

$$U(w',s') = \frac{\psi}{j\lambda z}\int_{-\infty}^{\infty}\int_{-\infty}^{\infty} U(x,y)\cdot\exp\left(-j2\pi(w'x+s'y)\right)\partial x\partial y \quad (15)$$

Where z is *much larger* than $\frac{\pi(x^2+y^2)}{\lambda}$

The above formulas are good representations of light waves for a given phase and intensity. However, when considering a detector plane such as the chip array inside a camera, only the intensity is recorded. The leading phase terms drop out and the remaining formula is converted to a double-summation computer algorithm:

$$U(w,s) \approx \frac{z}{j\lambda}\sum_{x=1}^{N}\sum_{y=1}^{M} U(x,y)\cdot\exp\left(\frac{j2\pi r}{\lambda}\right)\cdot r^{-2} \quad (16)$$

Where:

r = Point-to-point distance as a function of (*x,y*) and (*w,s*)

This formula enables computer programs to model and simulate light wave behavior. More specifically, it enables the design of grating patterns that produce periodic diffraction patterns. Optimized intensity patterns were developed through rigorous modeling in the following research in order to validate the theory behind the HMJ-Si solar cell and determine its specific design parameters.

Summary

This chapter discussed the background theory and principles of the photovoltaic process. It covered solar cell parameters, limitations, fabrication techniques and current research seeking to improve solar cell efficiency. Finally, light wave behavior and propagation was covered, which is the basis of the HMJ-Si concept.

III. Modeling and Methodology

Chapter Overview

The purpose of this chapter is to detail the methodology used during HMJ-Si solar cell research and development. First, the physical architecture is explained to provide an understanding of the concept. The intent and assumptions of this research are outlined and the investigated parameters are discussed, followed by the modeling and simulation, specific fabrication techniques, and testing approach.

3.1. Hybrid Multi-junction Silicon Solar Cells

The primary advantage of the HMJ-Si architecture is that sunlight has four chances of absorption. It first enters the top cell where a majority of the photocurrent is generated until it propagates through the rear grating contact, forming interfering waves. The bottom cell maximizes absorption since the contacts are located within the destructive interference bands produced by the top cell. Light reaching the rear contact is reflected back into the bottom cell for a third opportunity and once more if any re-enters the top cell. In addition to improved light trapping, the HMJ-Si design uses low-cost, common fabrication processes based on the most abundant material on Earth: silicon.

HMJ-Si solar cells have three main characteristics that differentiate them from the traditional cells shown in Figure 4: stacked wafers, patterned inner grating contacts, and an isolating air gap (Figure 16). These are the fundamental components that promote light trapping via interference pattern formation. Each silicon wafer is a stand-alone solar cell with a p-n junction and front/rear contacts; the hybrid multi-junction structure is formed when these cells are stacked. The resulting tandem configuration requires specifically

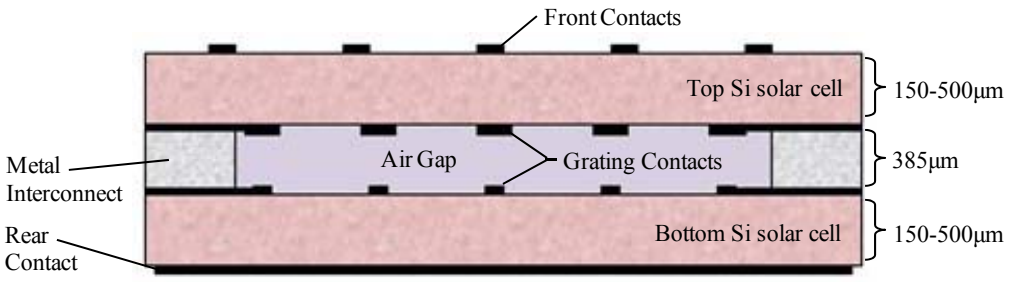


Figure 16. Cross sectional view of a hybrid multi-junction silicon (HMJ-Si) solar cell. Major components include the top and bottom silicon solar cells, front and rear contacts, grating contacts, air gap, and metal interconnects.

designed inner grating contacts so the bottom solar cell receives light that wasn't absorbed in the top cell. These inner grating contacts produce interference patterns and are separated by an air gap distance determined by the thickness of the metal interconnects, which also serve as the cell's anode.

The HMJ-Si cells were constructed using common materials to avoid elevating process costs. The AFIT clean room stocks 380-500μm thick silicon wafers and the AFIT Modeling and Fabrication Shop made washers out of 28-gauge carbon steel sheet metal for use as the interconnects. The actual thickness of these interconnects—385μm—was measured at Wright-Patterson's Precision Measurement Equipment Laboratory (PMEL). The contact metal was initially aluminum due to its availability and low resistivity, but silver was also investigated [71].

3.2. Research Considerations

The objective of this research was to develop a functioning HMJ-Si architecture as a proof-of-concept for a novel light-trapping method that increases solar cell performance. The resulting efficiency was examined within a set of reasonable assumptions to fully understand HMJ-Si functionality, applicability, and future potential.

3.2.1. Objective

High-efficiency solar cells are expensive to produce, so typical commercial cells have limited power densities. The HMJ-Si architecture is intended to remedy this by providing better efficiency without higher fabrication costs. Using processes that are commonly available means that existing manufacturers will not need to buy retooling equipment; their production expense will only experience a modest increase in proportion to the additional amount of raw materials required.

Although light trapping is the primary method for increased efficiency, other characteristics factor into the overall performance. The air gap that enables interference patterns also provides thermal isolation between the two cells, resulting in a lower bottom cell temperature. The overall temperature can be reduced even more by replacing the top cell with a higher band gap semiconductor other than silicon. The new top cell will absorb the higher energy photons that normally create excess heat within a silicon solar cell (see Section 2.3.3). Isolating these higher energy photons and allowing the band gap-matched photons to propagate into the bottom silicon cell will further enhance the efficiency of the stacked solar cell architecture. These hypotheses are based on the assumption that the proof-of-concept demonstrated in this research can be modified with an exotic-material top cell without having an adverse affect on the electrical performance of HMJ-Si cells.

3.2.2. Assumptions

Additional assumptions were made throughout this research to help streamline the results and validate the initial methodology and include:

Design Assumptions

- Using polysilicon (p-Si) instead of crystalline silicon (c-Si) for HMJ-Si cells will reduce efficiency an insignificant amount and in proportion to current p-Si/c-Si commercially available solar cell loss ratios.
- Higher band gap radiation (400-800nm) does not adversely affect the periodicity or intensity of the interference patterns.
- The total architecture thickness (≈1mm) is suitable for transitioning to existing solar panel manufacturing processes.

Modeling and Simulation Assumptions

- Optical aberrations within the cell, if present, are trivial and do not impact the overall light wave behavior.
- Light waves propagating through silicon experience a uniform phase delay.
- Sampling rates selected for modeling and simulation are sufficient for accurate representations of HMJ-Si behavior.
- Reflection and refraction effects from extreme angles are negligible.

Material Assumptions

- Silicon wafers will remain available and inexpensive due to a lack of resource constraints.
- Materials are consistent between cells and within each cell (extrinsic doping concentration, material thicknesses, wafer and metal uniformity).
- Grating contact thickness has a negligible effect on interference pattern formation.
- Actual junction depths achieved match those posted in the source wafer data sheets.

Testing Assumptions

- Thermal measurements are accurate since ambient heat caused by the testing devices was exhausted.
- Internal test equipment resistance does not significantly affect the accuracy of voltage or current readings.
- Higher efficiencies and thermal behavior can be observed when testing in an zero air-mass (AM0), vacuum chamber environment.
- The spectral signature of the lamp matches AM1.5.

Application Assumptions

- Protective coatings such as glass or acrylic or associated encasement for commercial applications will not significantly reduce efficiency.
- Logistical impacts of the increased weight of HMJ-Si cells versus traditional cells will be offset by the higher power densities achieved.
- The HMJ-Si structure is viable for space-based applications.
- Thinner wafers will not degrade the applicability of the cells.

3.3. Investigated Parameters

The advanced light trapping scheme in HMJ-Si cells depends heavily on the interoperability of specific parameters. For example, photocurrent harvesting is only maximized when the grating contact geometries are matched with each other as well as the air gap distance. Successful development of the HMJ-Si architecture was performed by developing and refining the following eight parameters.

3.3.1. Wafer Configuration

Semiconductor p-n junctions operate like a diode where positive current flows out of the n-doped region (*cathode*) and into the p-doped region (*anode*) [13]. Solar cells, typically represented as *photodiodes*, have cathode locations that depend on the type of extrinsic doping. Generally, p-type silicon wafers have cathodes at the front of the cell and n-type silicon wafers have cathodes at the rear (Figure 17).

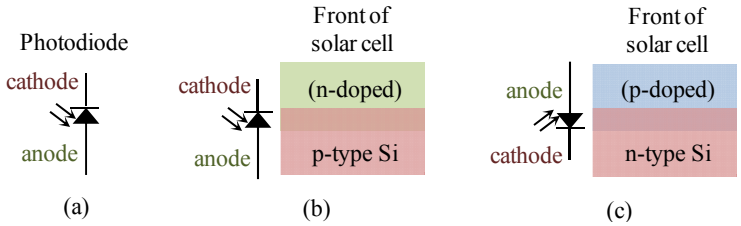


Figure 17. Circuit symbols and equivalent solar cell representations identifying the cathode and anode of (a) a photodiode, (b) a photodiode created with p-type silicon, and (c) a photodiode created with n-type silicon.

The orientation of the p-n junction diodes is a critical parameter of the HMJ-Si architecture because efficiency relies on effective current flow throughout the circuit. For instance, conflicting current directions might cause inadvertent recombination, reducing the fill factor and power output of the cell.

There are three possible variations for the HMJ-Si cell structure: unidirectional, common cathode, and common anode; the type of configuration depends on the extrinsic doping of the top and bottom cells (Figure 18). These configurations were examined using two p-type wafers and two n-type wafers to produce four single-layer silicon solar cells arranged into the configurations identified in Figure 18 for testing. All four cells were fabricated using consistent processes, metals, and contact patterns to isolate the effects of diode orientation on the relative efficiency of HMJ-Si solar cells.

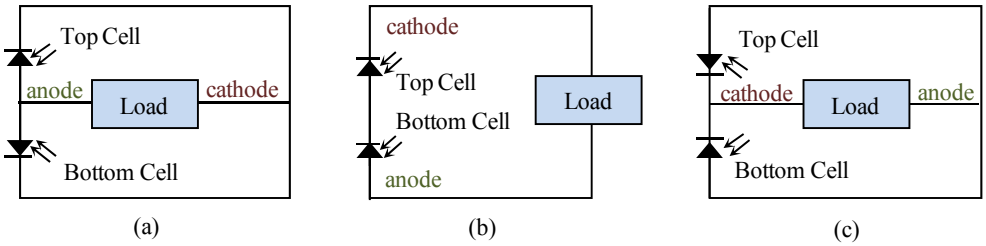


Figure 18. Circuit representations of HMJ-Si diode orientation study: (a) p-type top cell and n-type bottom cell produced a parallel-connected, common-anode circuit; (b) stacked p-type silicon wafers produced a series-connected, unidirectional circuit; (c) n-type top cell and p-type bottom cell produced a parallel-connected, common-cathode circuit.

3.3.2. Diffusion Profile

The p-n junction is the most critical part of a photovoltaic cell because it creates the depleted region. The depth of the depleted region has a direct impact on solar cell efficiency because electrons experience more resistance as they travel longer distances through silicon. A depleted region that is too shallow will not provide an adequate electric field or enough electron-hole pairs for photocurrent generation. Similarly, the silicon substrate below the depleted region also limits efficiency through resistance and recombination. Therefore, an advanced diffusion can provide a significant increase in efficiency and seven diffusion profiles were explored during this research as shown below in Table 1.

Table 1. Diffusion Profile Parameters

Diff. Profile	Primary Doping[1] Source · Time · Temp			Extrinsic Doping	BSF Doping Source · Time · Temp			EBSF Doping Source · Time · Temp		
n-p	P	60m	925°C	p-type						
n-p	P	30m	925°C	p-type						
n-p-p^{+}	P	60m	925°C	p-type	BN	60m	950°C			
n-p-p^{++}	P	60m	925°C	p-type	BN	60m	950°C	BN	30m	950°C
p-n	BN	60m	950°C	n-type						
p-n-n^{+}	BN	60m	950°C	n-type	P	60m	925°C			
p-n-n^{++}	BN	60m	950°C	n-type	P	60m	925°C	P	30m	950°C

In addition to single-region and BSF solar cells (see Section 2.3.2), a novel diffusion profile was investigated: an *enhanced back-surface field* (EBSF). The intent of the EBSF is to reduce dark current by adding another voltage drop, improve electron drift by acting as an "electric mirror", and increasing photon absorption through an additional depleted region.

3.3.3. Front Contact Design

One of the challenges in solar cell optimization revolves around the design of the front contacts. The ideal situation is a silicon wafer fully exposed for photon absorption while being completely covered with metal for electron mobility. Balancing these parameters has led to various designs that typically consist of a rectangular grid structure with *fingers and busses* to collect and transport electrons (Figure 19) [22].

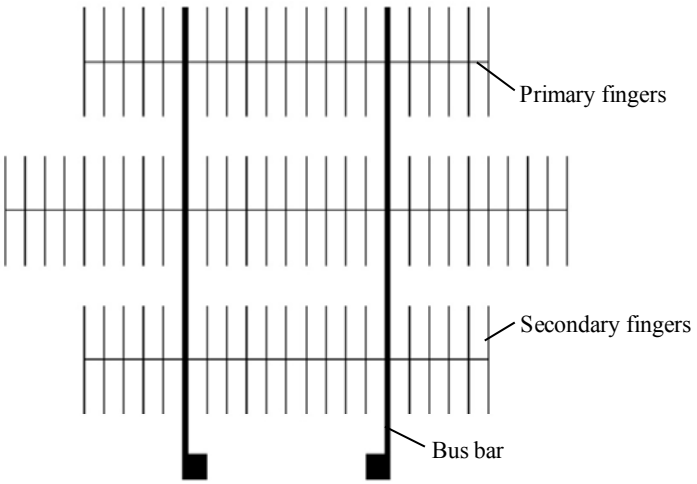


Figure 19. Example of a typical solar cell front metal contact pattern consisting of bus bars, primary fingers, and secondary fingers.

Although these designs are easy to manufacture, they are prone to a phenomenon called *current crowding*, in which electron flow is impeded by 90-degree bends in the conductor path. This effect and the resulting elevated point temperatures or "hot spots"

can be avoided by properly designing metal contacts that also enhance photocurrent. A similar finger and bus pattern was designed during this research as an initial baseline for future contact design comparison. This front contact design closely resembled the design shown in Figure 19 and was based on the same optimized front contact spacing criteria (Figure 20) [22].

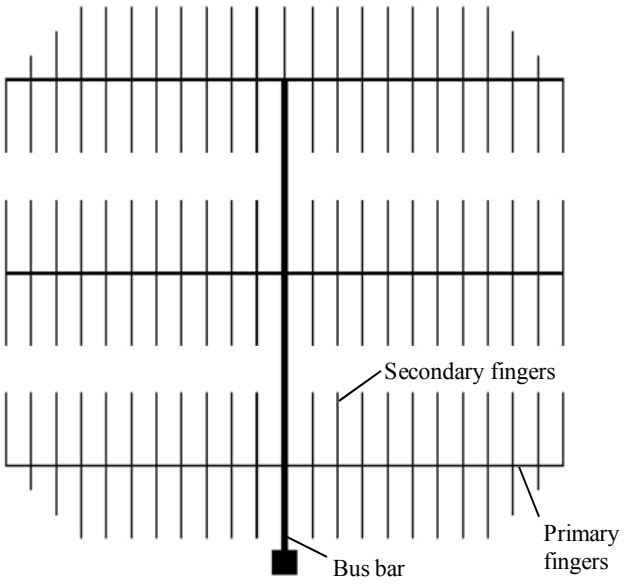


Figure 20. Solar cell contact design used for the front of the top hybrid multi-junction silicon solar cell. This baseline contact geometry was modeled after typical commercial solar cell contact designs that incorporate optimized spacing [22].

A novel design approach for the front contacts was explored based on the diameter of an electron (2.82×10^{-15}m) being six times larger than the diameter of a photon (0.5×10^{-15}m) [72]. The idea was that a corresponding front contact coverage area—roughly 15%—would increase a cell's efficiency by allowing six times as many photons to enter the wafer for every electron collected. While maintaining this ratio, four distinct 1" by 1" contact geometries were designed on a single wafer: an incremented spiral, a ring lattice, periodic branching, and a standard finger/bus design for a baseline comparison (Figure 21).

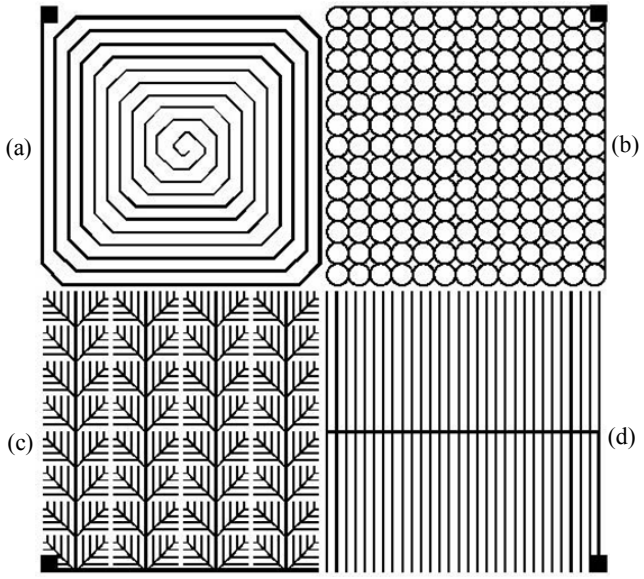


Figure 21. Solar cell front contact designs featuring various geometries on a single 3" wafer. The designs are (a) incremented spiral; (b) ring lattice; (c) periodic branching; (d) standard finger and bus design as a baseline for comparison. Each design has 15.05% of the surface area covered by metal.

In addition to maintaining 15.05% metal coverage, these patterns were designed to enhance conduction and prevent current crowding by avoiding angles exceeding 45°, except at the primary bus bar. Taking the electron-to-photon ratio further, a subsequent contact was designed based on combining it with the S-Q limit (see Section 2.2.5). This reduced the amount of surface area covered by metal to only 4.285% (Figure 22).

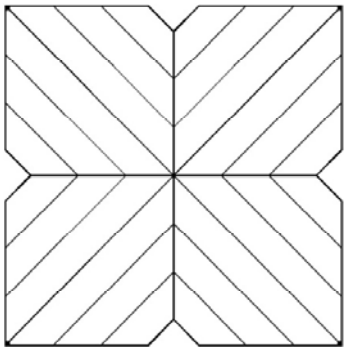


Figure 22. Solar cell front contact design of a highly transmissive butterfly pattern that avoids current crowding and applies the 30% Shockley-Queisser limit to the 1:6 electron-to-photon ratio. The resulting surface area covered by metal is 4.285%.

3.3.4. Grating Contact Design

The primary design feature of the HMJ-Si architecture was the set of internal grating contacts that generate interference patterns. Therefore, the width and spacing of these contacts was critical to the overall functionality. The grating was extensively modeled to determine the best dimensions (see Section 3.4), but there were other important considerations that drove their design. Because silicon absorbs photons with wavelengths less than 1117nm, the grating was optimized for a maximum of 1100nm. Additionally, a lower-bound limit was set at 800nm (1.55eV) to avoid the excessive heat from high-energy photon excitation. Thus, the grating spacing was designed to optimize absorption within the 800-1100nm range.

This design also accounted for both parallel and series circuit investigations by including contact tabs outside of the primary contact gratings (Figure 23). These tabs were connected to the grating contacts via an outer bus ring which served as the primary conduction path. The finalized contact deign was the keystone of the HMJ-Si cell architecture and primary component in reducing optical losses.

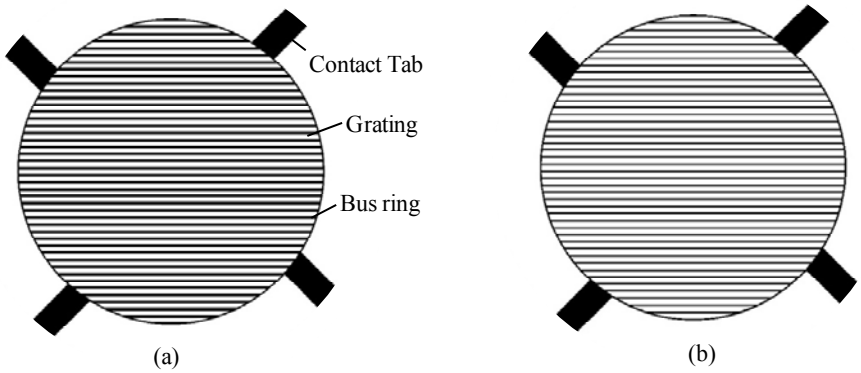


Figure 23. Grating contact design for (a) the rear of the top cell and (b) the front of the bottom cell. The design included contact tabs for testing in either a series or parallel circuit setup.

3.3.5. Optical Loss Reduction

In addition to the interference patterns limiting optical losses by mitigating transmission, optical losses at the front of the cell were investigated through surface roughness and ARC application.

When silicon wafers are manufactured, they are typically polished on one side of the wafer; the other side remains rough. The front contact patterns were fabricated onto both sides of the wafer in order to determine which surface had a higher rate of absorption. The typical thickness of silicon nitride as an ARC on commercial solar cells is 74nm, but that thickness is optimized for a peak absorption at 600nm [14]. Since HMJ-Si cells were designed to operate from 800nm to 1100nm, a different ARC thickness was required for reducing reflection. According to Equation 6, the optimal thickness for the center frequency of the HMJ-Si bandwidth is approximately:

$$d = \frac{950nm}{4 \cdot 1.9} = 125nm \tag{17}$$

This thickness corresponds to a refractive index of 3.6 for silicon at 950nm. The refractive index decreases as the incident wavelengths increase, rising to approximately 3.54 for 1100nm. This means that although an ARC can optimize a specific wavelength, it will not result in ideal loss correction across an entire bandwidth. Thus, the effects of 100nm, 120nm, 128nm and 168nm ARC thicknesses were examined to investigate the trade-offs between various reflected band gap energies.

3.3.6. Electrical Loss Reduction

Collecting and transporting the photocurrent is a critical step in the power delivery of any solar cell. Losses are caused by resistance, which is a factor of the metal contact type, thickness, and interface with silicon. Commercial solar cells typically use aluminum because it is inexpensive, reflective, and highly conductive, but another option is silver. Both were investigated in this research, each incorporating a thin layer of titanium as an adhesion layer since it bonds well with silicon. The electrical properties of these metals are shown below in Table 2 for reference [73].

Table 2. Electrical Properties of Selected Metals at 20°C

Metal	Resistivity (ρ)	Conductivity (σ)
Silver	1.59 x10^{-8} Ω·m	6.30 x10^{7} S/m
Aluminum	2.82 x10^{-8} Ω·m	3.5 x10^{7} S/m
Titanium	43.0 x10^{-8} Ω·m	0.2 x10^{7} S/m

The *resistivity* (ρ) of each metal is important because it drives the overall resistance, R, given by the equation:

$$R = \rho \frac{l}{A_c} \tag{18}$$

Where:

l = Length of the conductor in meters
A_c = Cross-sectional area of the conductor in square meters

Contact resistance was altered by using silver and aluminum thicknesses of 150nm, 200nm, 300nm, and 500nm; titanium was deposited with a typical thickness of 10nm and maximum of 50nm. The small overall thicknesses were chosen in order to avoid reflection and fringing effects caused by high-aspect ratio contacts.

The final technique for electrical loss reduction was explored through RTA parameters. Since titanium was used as an adhesion layer, the annealing times and temperatures were based on optimizing its interface with silicon. The recipe parameters (based on previous research) were selected as 450°C/30s and 450°C/20s [39, 41, 74, 75].

3.3.7. Thermal Loss Reduction

Reducing cell temperature was accomplished in the HMJ-Si architecture by trapping high-energy (small wavelength) photons in the top cell and limiting infrared (large wavelength) radiation in the bottom cell. In addition, the effect of front contact design on thermal dissipation was also explored. This is an important part of temperature reduction since convective cooling systems common in solar cell applications rely on a cell's ability to conduct heat to the surface and expose it for cooling. Therefore, the patterns and surface area coverage identified in Section 3.3.3 have a direct impact on the overall temperature and were explored in this research.

3.3.8. HMJ-Si Efficiency

The above parameters were improved in order to maximizing the overall efficiency of the HMJ-Si architecture. Combining these parameters was necessary because individual properties may be offsetting and lead to limited performance. Therefore, a comprehensive test cells for measurement and characterization were produced and incorporated the best result from each parameter.

An example of counterproductive parameters is the voltage and current response. If the top cell and bottom cell are connected in series, they experience limited current and combined voltage; if connected in parallel they have combined current and limited voltage. These conflicting requirements prompted an investigation into the best type of

bottom cell which included an undoped, partially-reflective p-type wafer and a silver-coated wafer which were compared to the performance of an HMJ-Si bottom cell.

Another component that impacts efficiency is wafer thickness. Since the top cell needs to let unabsorbed photons propagate into the cell below, thinner wafers increase the bottom cell's efficiency. Wafer thickness also plays an important role in electrical performance since larger distances decreases both electron and hole mobility. Therefore, thinner wafers were tested to verify their impact in the architecture's efficiency. Silicon wafers ≈150μm thick were purchased for testing along with stocked silicon wafers that were etched to ≈180μm. This etching process was performed using a 25% potassium hydroxide (KOH) and de-ionized water solution at 90°C for 85min [76].

3.4. Modeling

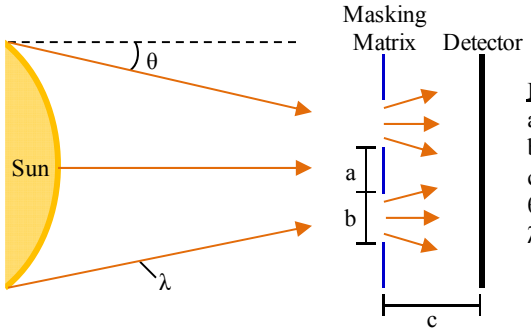
Prior to fabrication, modeling and simulation were used to narrow the focus of experimentation. This research used three types of computer aided design (CAD) software that included 2-dimensional diffraction patterns generated using MATLAB®, 3-dimensional propagation using Lumerical® FDTD Solutions, and contact pattern design using L-Edit™.

3.4.1. MATLAB®

MATLAB® is a high-level language environment used for numerical computation and visualization. It offers fine-tuned, mathematically-based light wave propagation modeling and can account for phase delay and optical aberrations. In order to accurately model light wave behavior, the modified Rayleigh-Sommerfeld formula identified in Equation 15 was used. This double-summation formula took a discrete point in an N x M source plane, $U(x,y)$, and propagated it a distance, r, via Fourier transformation to every

point in the resulting plane, *U(w,s)*, where the intensity was measured. Once every point in the source plane was propagated, the process was repeated for each wavelength, λ. This investigation included wavelengths from 800nm to 1100nm in 10nm increments with a fixed normal distance, *z*, of 385µm.

Although the distance from Earth to the sun is large enough for sunlight to be approximated as a series of plane waves, the span of its diameter does have an effect on how incident light reaches a surface. The maximum angle of light subtended by the sun, which is 0.005 radians, was incorporated by applying a degree of tilt to each source plane from -0.005 to 0.005rad in 0.001rad increments [24]. The finalized code (see Appendix A.1) ran a recursive nested summation algorithm for each point from the source plane over these eleven tilts and across 31 distinct wavelengths to record the resulting intensity pattern (Figure 24).



Parameter	Min/Max	Increment
a: contact	100/500µm	50µm
b: separation	500/900µm	50µm
c: normal	385µm	fixed
θ: angle	-0.005/0.005rad	0.001rad
λ: wavelength	800/1100nm	10nm

Figure 24. Conceptualization of MATLAB® modeling code. Plane waves with varying angles and wavelengths were propagated through a masking matrix to a detector plane to record the resulting interference patterns.

The algorithm was applied to 40 different grating patterns with geometries that ranged from 100µm contact width and 250µm separation to 500µm width and 900µm separation. The grating patterns were modeled by constructing a masking matrix that was multiplied with the source wave to periodically cancel its intensities. Using MATLAB®

to model light wave behavior enabled extensive parameter sweeps and fine-tuned adjustments to determine grating patterns sufficient for 3D simulation.

3.4.2. Lumerical® FDTD Solutions

Finite-difference time-domain (FDTD) simulation offers an advantage over 2-dimensional modeling since it takes into account extensive real-world effects such as resonance and fringing from structural characteristics. Lumerical® FDTD Solutions software is capable of calculating the 3-dimensional Maxwell equations for light waves with an accuracy down to the wavelength-scale. The main components of the simulation were the grating structure, simulation region, and source wave (Figure 25). The grating was constructed as a 3-dimensional model with the following parameters: 150nm thick, 400μm wide, 450μm spacing, and aluminum as the type of material.

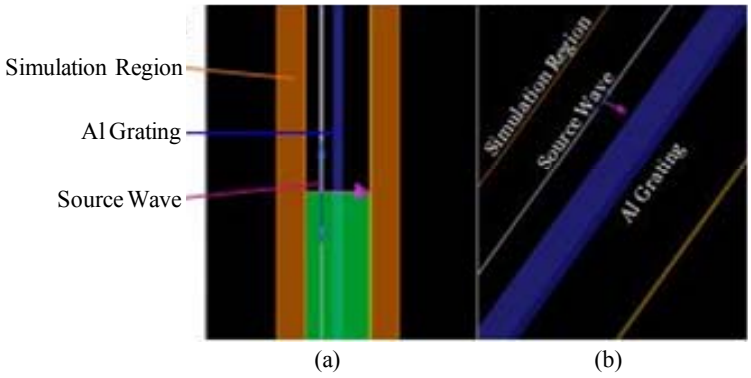


Figure 25. Screen shot of Lumerical® FDTD Solutions model in (a) cross-sectional and (b) perspective view identifying the simulation region, grating, and source wave.

The length of the grating was considered infinite since it extended outside the simulation region which provided boundary conditions for the light waves. It also defined the calculation accuracy and allowed periodic structure repetition. To accommodate this, the boundary conditions (BCs) in the z-direction were set as periodic, making the total spacing between gratings 900μm. The remaining BCs were anti-symmetric in the y-

direction and perfectly matched layers (PML) in the x direction. PML BCs are an artificial perfectly-absorbing layer that avoids unintentional fringing effects.

The last simulation component, the source wave, was selected as "plane wave" from the pre-defined software database and its bandwidth adjusted to 800-1100nm. Once the settings were finalized, the simulation generated the near field intensity values which were then ran through a specialized far-field projection algorithm to verify the nature of the diffraction propagation.

3.4.3. L-Edit™

In order to transition the grating pattern design from computer modeling to real-world implementation, a chrome mask needed to be created. This was accomplished by first drawing the mask geometry in a CAD program commonly used in microelectronic fabrication called L-Edit™. This 2-dimensional design software enabled the conversion of drawings into the file types used by the mask writer (see Appendix E). The grating contacts were drawn using this program and designed in accordance with the outcome of the previous modeling results before being exported for fabrication.

3.5. Solar Cell Fabrication

Although modeling is an extremely useful tool, it cannot account for every real-world detail. In order to thoroughly explore the response of the HMJ-Si architecture, cells were fabricated for testing using the following general process steps. A detailed process follower is included in Appendix C and list of equipment in Appendix E for reference, but there are a few design considerations that determined the overall process.

3.5.1. Diffusion

In order to dope the n-type and p-type silicon wafers according to the diffusion profiles in Table 1, a p-type and n-type source were used. The p-type source was a boron nitride (BN) model 975, which means it can withstand furnace temperatures up to 975°C [77]. These source wafers are unique in that they require additional post-processing. This step, called *low temperature oxidation* (LTO), is used to rapidly oxidize the surface of the silicon wafer and trap crystal defects. These defects are then removed during a chemical etching step known as *deglazing*. The n-type source, model Ph-1000N, is capable of temperature up to 1000°C [78]. These sources provide a direct injection of n-type phosphorous atoms into the silicon and requires no additional processing. The complete data sheets for the BN-975 and Ph-1000N sources are included in Appendix D.

3.5.2. Masking

The mask file created in L-Edit™ was transferred to a Heidelberg μPG101 mask writer for creation. This machine used a UV laser to "write" the pattern into a thin layer of photoresist over chrome on a 4" glass mask. Once exposed and developed, an etching process removed the patterned chrome and the mask was ready for photolithography.

3.5.3. Photolithography

The first step in photolithography was post-diffusion de-glazing. This was done to remove any oxides and surface contaminants on the wafer. The de-glazing consisted of submerging the wafer in a diluted hydrogen fluoride (HF) solution known as a buffered oxide etch (BOE). Once the wafers were dry, S1818 photoresist was applied to the wafer. S1818 is a positive photoresist—meaning that it becomes more soluble when exposed to light—which is 1.8μm thick. This thickness is important because it enables metal lift-off.

After baking the resist, it was exposed with UV light through the chrome mask in the Suss MJB-3 mask aligner. The final step developed and removed the exposed resist, leaving behind a pattern of bare silicon matching the mask. After rinsing with de-ionized water and drying with nitgrogen, the wafer was ready for metallization.

3.5.4. Metallization

In order for metal to be deposited onto a clean wafer, the samples were placed in a plasma asher to remove any remaining surface contaminants. The wafers were then loaded into an electron-beam evaporator machine where an electron beam bombards a crucible that contains the metal pellets. The evaporated metal condensed on the wafer directly above, coating it completely. After metal deposition, tape was applied and pulled away to remove metal on top of the resist. Since this "lift-off" method didn't completely remove the unwanted metal, the wafers were submerged in acetone and placed in an ultra-sonic bath to dissolve the remaining resist until only metal deposited directly onto the silicon remained. The final step in the fabrication process was using an RTA to provide a good ohmic contact between the metal and silicon.

3.6. Testing

Once fabrication was completed, the solar cells were tested to compare results with the design intent. The tests, designed to verify both individual parameters and the overall response of the HMJ-Si architecture, required the use of specialized equipment.

3.6.1. Equipment

The sun was represented using a solar light tester with an AM1.5 spectral signature (see Appendix F). STC irradiance and temperature (see Section 2.2.2) were set and verified with a pyranometer and thermocouple probe prior to testing. Voltage and

current readings were then taken using independent multimeters. Internal thermal measurements were taken using thermocouple probes connected to another multimeter; the front contact heat dissipation was measured with FLIR® infrared cameras spanning thermal radiation wavelengths from 1000-5000nm and 7000-14000nm.

3.6.2. Parameters

V_{oc}, I_{sc}, and the IV curve for resistances from 0.1Ω to 1kΩ were measured to identify ideal power, maximum power, and fill factor. Also measured was contact resistance for metal comparison, transmitted irradiance for optical loss reduction, air gap temperature versus top temperature for thermal management characterization, and contact temperature for thermal dissipation comparison.

Summary

This chapter detailed the methodology used in this research. The HMJ-Si architecture was explained and followed by design assumptions, investigated parameters, modeling and simulation, fabrication specifics, and the testing approach.

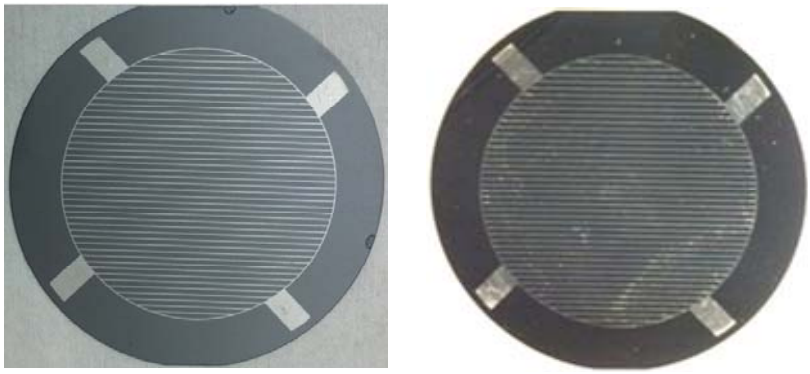
IV. Results

Chapter Overview

The purpose of this chapter is to provide the data and results obtained during this research. The information in this chapter is divided into sections that match the parameters identified in Sections 3.3.1—3.3.8.

4.1. Wafer Configuration

Two p-type wafers and two n-type wafers were fabricated for testing the configurations shown in, but one of the n-type samples was damaged and could not be tested. Each of the cells were fabricated the same way, using an EBSF diffusion profile and 200nm of aluminum with the 200μm/1100μm grating pattern on the unpolished (front) side of the wafer and 400μm/900μm grating pattern on the polished (rear) side of the wafer (Figure 26); the results are shown in Table 3.



(a) (b)

Figure 26. Diode orientation wafers showing (a) the front contact on the unpolished side of a wafer patterned into the 200μm/1100μm grating and (b) the rear contact on the polished side of the same wafer patterned into the 400μm/900μm grating pattern. This contact configuration enabled multiple HMJ-Si orientations using the same wafers.

Table 3. Diode Orientation Results

Sample	Configuration	Voltage (V)	Current (mA)	P_{max} (mW)	Efficiency
DP1 / DP2	unidirectional	0.433	237.6	102.88	2.93%
DP1 / DN1	common anode	0.441	290.0	127.89	3.65%
DP2 / DN1	common anode	0.468	275.0	128.70	3.67%
DN1 / DP2	common cathode	0.422	265.0	111.83	3.19%

4.2. Diffusion Profile

Advanced diffusion profiles have a significant impact on efficiency because the p-n junction is one of the main components of a solar cell. Each profile shown in Table 1 was processed and tested using 12 individual single-layer solar cells, each with 150nm of aluminum and the optimized front contact pattern shown in Figure 20. Both sides and types of wafers were investigated; the results are shown in Table 4.

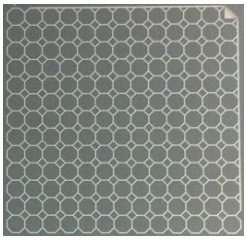
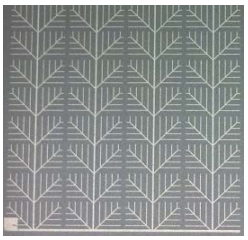
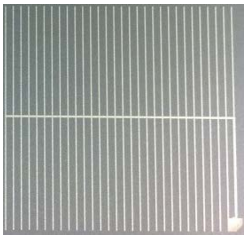
Table 4. Diffusion Profile Results

Sample	Front	Profile	Voltage (V)	Current (mA)	P_{max} (mW)	Efficiency
P1	polished	n-p	0.311	190.0	59.09	1.92%
P2	unpolished	n-p	0.083	95.0	7.89	0.26%
P3	polished	n-p-p+	0.412	229.0	94.35	3.07%
P4	unpolished	n-p-p+	0.481	280.0	134.68	4.38%
P5	polished	n-p-p++	0.459	284.0	130.36	4.24%
P6	unpolished	n-p-p++	0.499	336.0	167.66	5.45%
N1	polished	p-n	0.022	18.0	0.40	0.01%
N2	unpolished	p-n	0.014	12.0	0.17	0.01%
N3	polished	p-n-n+	0.331	167.0	55.28	1.80%
N4	unpolished	p-n-n+	0.333	200.0	66.60	2.16%
N5	polished	p-n-n++	0.440	241.0	106.04	3.45%
N6	unpolished	p-n-n++	0.414	200.0	82.80	2.69%

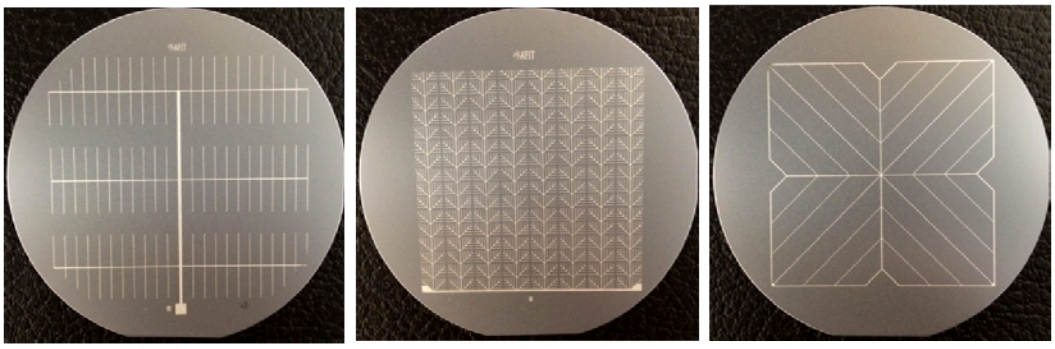
4.3. Front Contact Design

The initial front contact for this research was created based on a previously optimized finger and bus design [22]. However, since finger and bus designs experience current crowding, novel designs were explored based on improving surface area coverage and conduction paths. Four layouts were fabricated and tested on the unpolished side of a single p-type, n-p-p+ doped wafer yielding the following results.

Table 5. Front Contact Geometry Comparison Results

	Voltage: 0.526 V Current: 104.8 mA Power: 55.1 mW Efficiency: 6.25%		Voltage: 0.508 V Current: 105.2 mA Power: 53.4 mW Efficiency: 6.06 %
	Voltage: 0.535 V Current: 119.6 mA Power: 64.0 mW Efficiency: 7.25%		Voltage: 0.479 V Current: 93.4 mA Power: 44.7 mW Efficiency: 5.07%

In addition, full-wafer designs (Figure 27) were fabricated using single-layer solar cells to compare the different geometries; the results are shown in Table 6.



(a) (b) (c)

Figure 27. Full 3" wafer contact patterns fabricated for geometry comparison included (a) a standard finger/bus design with 3.685% coverage, (b) a periodic branching design with 15.05% coverage, and (c) a butterfly pattern with 4.285% coverage.

Table 6. Full Wafer Front Contact Comparison Results

Sample	Profile	Metal	Voltage (V)	Current (mA)	P_{max} (mW)	Efficiency
Finger and Bus	n-p^+	500nm Ag	0.443	54.8	24.28	3.76%
Periodic Branching	n-p^+	500nm Ag	0.291	33.7	9.81	1.52%
Butterfly	n-p^+	500nm Ag	0.443	55.9	24.76	3.84%

4.4. Grating Contact Design

The grating width and spacing is a critical aspect for HMJ-Si solar cells because the grating will not produce interference patterns without proper geometries. In order to test and verify the interference patterns generated by the various grating patterns, MATLAB® and Lumerical® FDTD simulation were completed as outlined in Section 3.4. The most accurate MATLAB® results are shown below; preliminary interference pattern results are included in Appendix B.

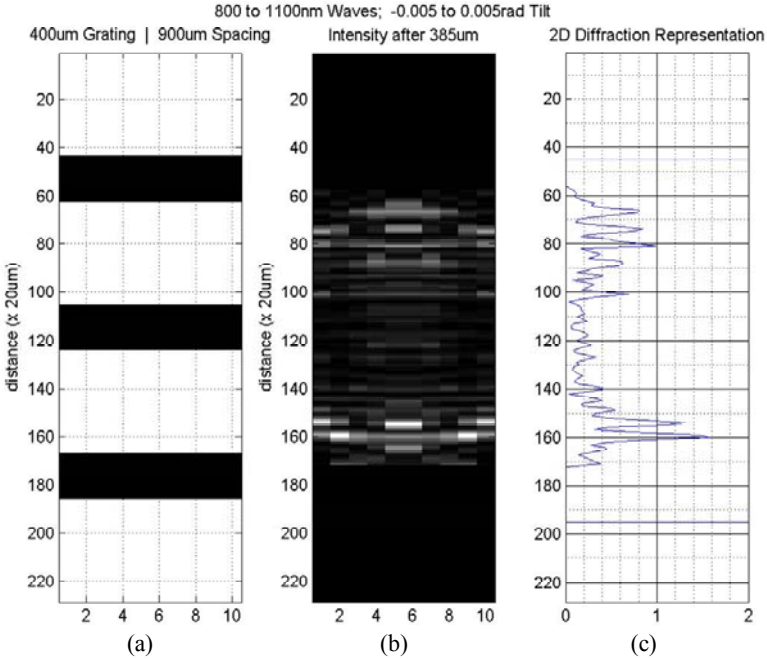


Figure 28. MATLAB® plots of (a) the 400/900μm grating matrix, (b) the interference pattern at 385μm, and (c) an intensity representation of the pattern. The simulated wavelengths were run in 10nm increments; the tilts were run in 0.001rad increments.

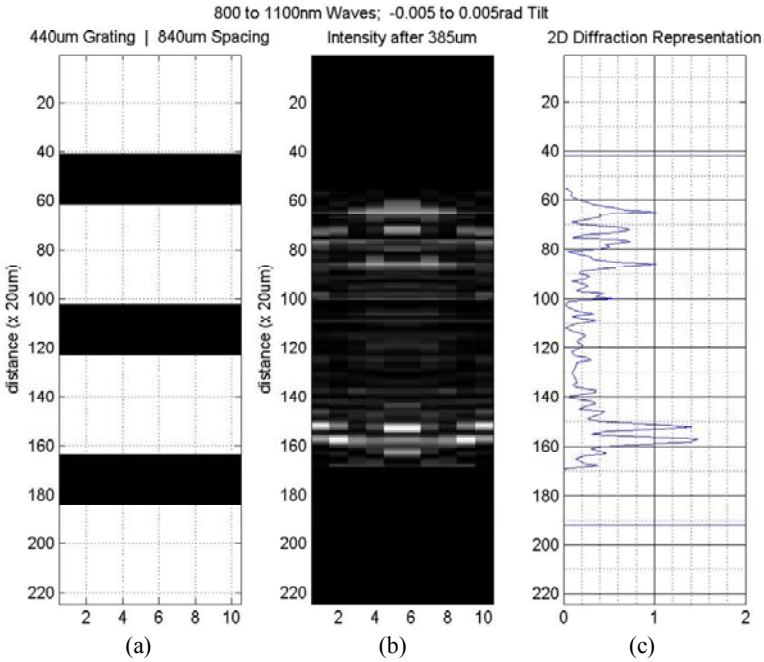


Figure 29. MATLAB® plots of (a) the 440/840µm grating matrix, (b) the interference pattern at 385µm, and (c) an intensity representation of the pattern. The simulated wavelengths were run in 10nm increments; the tilts were run in 0.001rad increments

Although both designs produced interference patterns, the Lumerical® simulation was performed with the 400/900µm grating design due to its higher irradiance throughput of 69.2% (the 440/840µm grating is 65.6%); the results are shown in Figure 30.

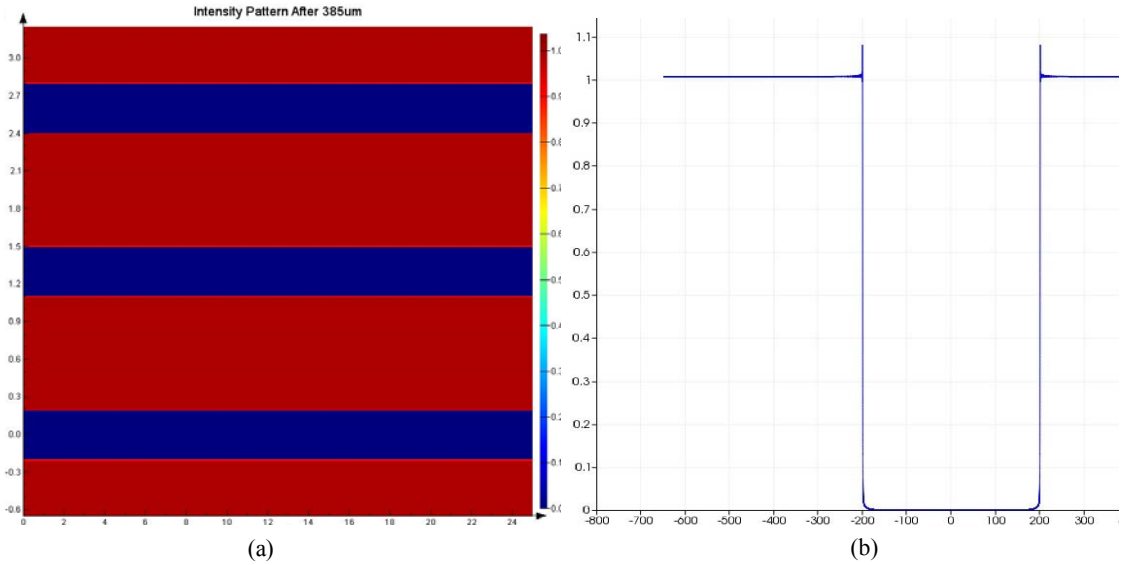


Figure 30. Lumerical® results showing (a) the far-field projection and (b) a single-period intensity plot and fringing effects from a plane wave propagated 385µm through the 400/900µm grating.

4.5. Optical Loss Reduction

Higher efficiencies can only be achieved if photon absorption is increased. Better absorption was investigated in this research by testing the effects of surface roughness, anti-reflection coatings (ARCs), and wafer thickness on cell performance.

The front surface of a solar cell plays an important role because a specular surface reflects photons which can be better absorbed with a diffuse surface. The roughness in this research was tested by fabricating multiple solar cells with both the unpolished side and polished side of a typical silicon wafer as the front of the cell (Figure 31); the results are shown in Table 4.

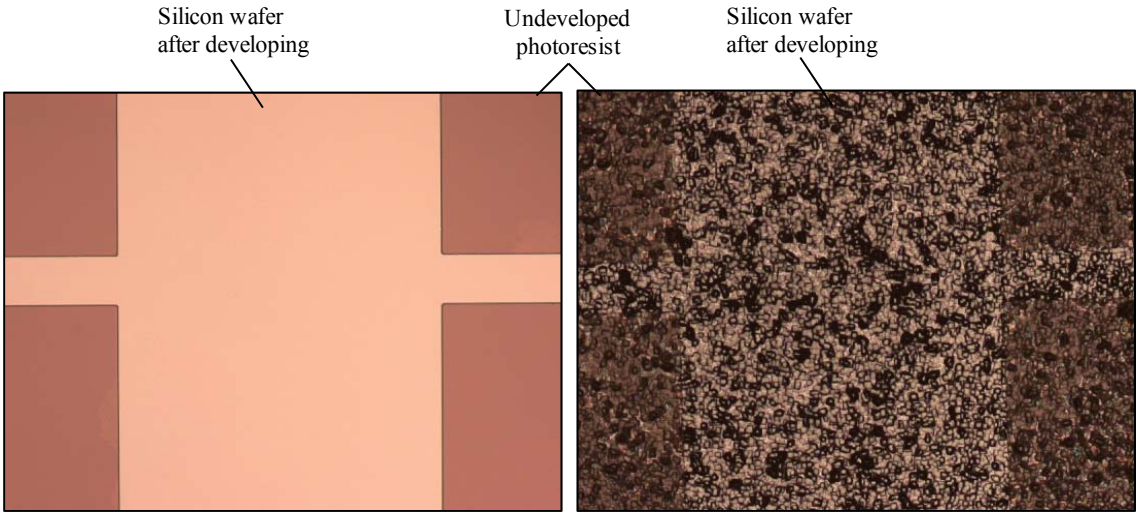


Figure 31. Silicon wafers under 20x magnification showing the same pattern of 1818 photoresist after being developed on (a) the polished side of a wafer and (b) the unpolished side of a wafer which provided better absorption due to surface roughness.

Because an ARC is one of the most important aspects in higher photon absorption, two cells were fabricated using an EBSF diffusion profile and 150nm of silver for the front contacts. The cells were tested to compare their performance before and after depositing 100nm of Si_3N_4; the results are shown in Table 7.

Table 7. Initial Anti-Reflection Coating Results

Sample	Front	Si_3N_4	Voltage (V)	Current (mA)	P_{max} (mW)	Efficiency
CA	Unpolished	none	0.490	108.2	53.01	2.62%
CB	Polished	none	0.459	113.8	52.22	2.58%
CA	Unpolished	100nm	0.514	129.8	66.71	3.29%
CB	Polished	100nm	0.499	131.4	65.57	3.23%

Finally, to characterize how ARC thickness affects transmittance, the unpolished side of undoped silicon wafers were coated with four distinct thicknesses of Si_3N_4. These cells remained unprocessed in order to isolate the absorption of irradiance without other parameters interfering. The values were recorded by placing the cells above a pyranometer that records intensity. Any ambient light was blocked by the wafer holder so that the measurements represented only transmitted irradiance; the results are shown in Table 8.

Table 8. Effects of Wafer and Si_3N_4 Thickness on Transmittance

Sample	Wafer Thickness	Si_3N_4 Thickness	Transmittance
I1	360μm	0	87 W/m^2
		168nm	113 W/m^2
I2	180μm	0	125 W/m^2
		100nm	143 W/m^2
I3	180μm	0	125 W/m^2
		128nm	147 W/m^2
I4	140μm	0	165 W/m^2
		120nm	187 W/m^2

4.6. Electrical Loss Reduction

The type of metal affects overall efficiency due to different resistivity (Table 2). Silver and aluminum were investigated as viable solar cell contact metals, each one using titanium as an adhesion layer. The results are shown in Table 9 with commercial cell contacts as a standard reference value.

Table 9. Effects of Metal Type and Thickness on Resistance

Sample	Titanium	Contact Thickness	Contact Metal	Total Thickness	Measured Resistance
Comm	N/A	10,000nm	Aluminum	10,000nm	0.9 Ω
A1	10nm	150nm	Aluminum	160nm	14.3 Ω
A2	10nm	200nm	Aluminum	210nm	13.1 Ω
S1	10nm	150nm	Silver	160nm	6.2 Ω
S2	10nm	300nm	Silver	310nm	4.2 Ω
S3	50nm	500nm	Silver	550nm	2.3 Ω

Since titanium was used to help the contact metal adhere to the wafer, annealing recipes were based on optimizing its interface with silicon. The cells were heated to 450°C for both 20 and 30 seconds (Table 10). The temperature was selected due to the melting point of the aluminum being 660°C. A subsequent RTA trial for silver was conducted for 20 seconds and, since silver has a higher melting point (961°C), the temperatures were 450°C and 650°C. The results are shown in Table 10.

Table 10. Rapid Thermal Annealing Results for Aluminum and Silver Contacts

Sample	Metal	Time	Temperature	Pre-RTA Resistance	Post-RTA Resistance
RTA1	Aluminum	20 sec	450°C	90 Ω	12.4 Ω
RTA2	Aluminum	30 sec	450°C	82 Ω	13.0 Ω
CA	Silver	20 sec	450°C	67 Ω	8.2 Ω
CB	Silver	20 sec	650°C	66 Ω	6.7 Ω

4.7. Thermal Loss Reduction

The air gap required for interference pattern formation also provided thermal isolation between the top and bottom cells. The amount of cooling offered by the HMJ-Si architecture was tested by exposing a cell to incident light over time and recording the front surface and the air gap temperature; the results are shown in Figure 32.

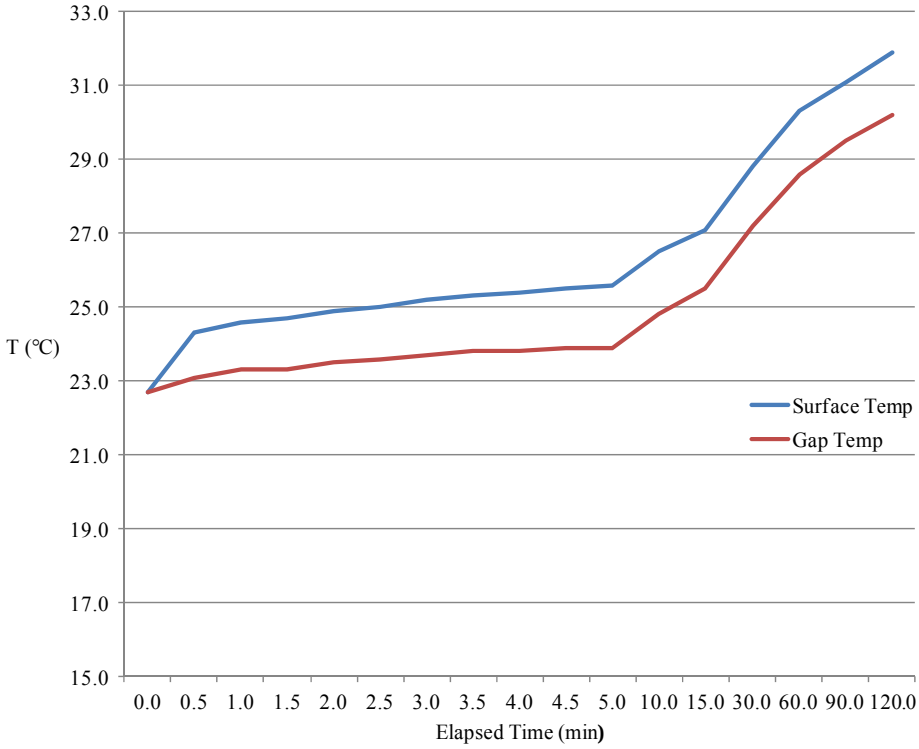


Figure 32. Hybrid multi-junction architecture surface and gap thermal readings without forced cooling. Nominal reduction in gap temperature is 1.7°C.

Heat dissipation is also a critical component of temperature reduction in solar cells. The amount of cooling based on the type of front contact pattern and amount of surface area coverage was explored in two portions of the infrared spectrum: 1000nm to 5000nm and 7000nm to 14000nm. A substrate temperature of 50°C was set in order to compare similar responses for each pattern under an induced thermal environment; the results are shown below in Figure 33—Figure 35.

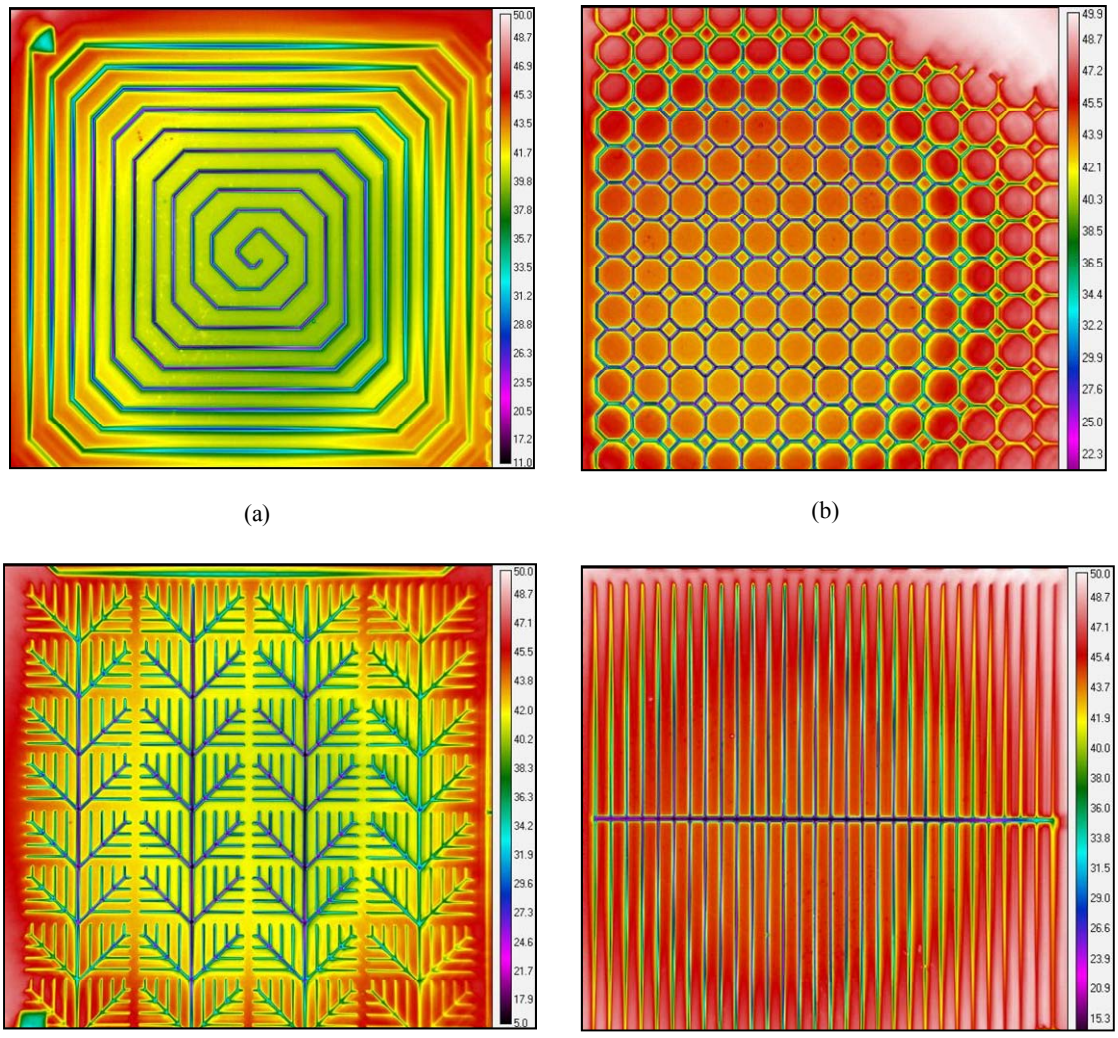


Figure 33. Thermal response of the 1000—5000nm infrared provided average readings of (a) 37.5°C for the incremented spiral; (b) 39.7°C for the ring lattice; (c) 37.8°C for the periodic branching; and (d) 40.3°C for the standard finger and bus design. Each pattern represents a 15.05% surface area covered by metal.

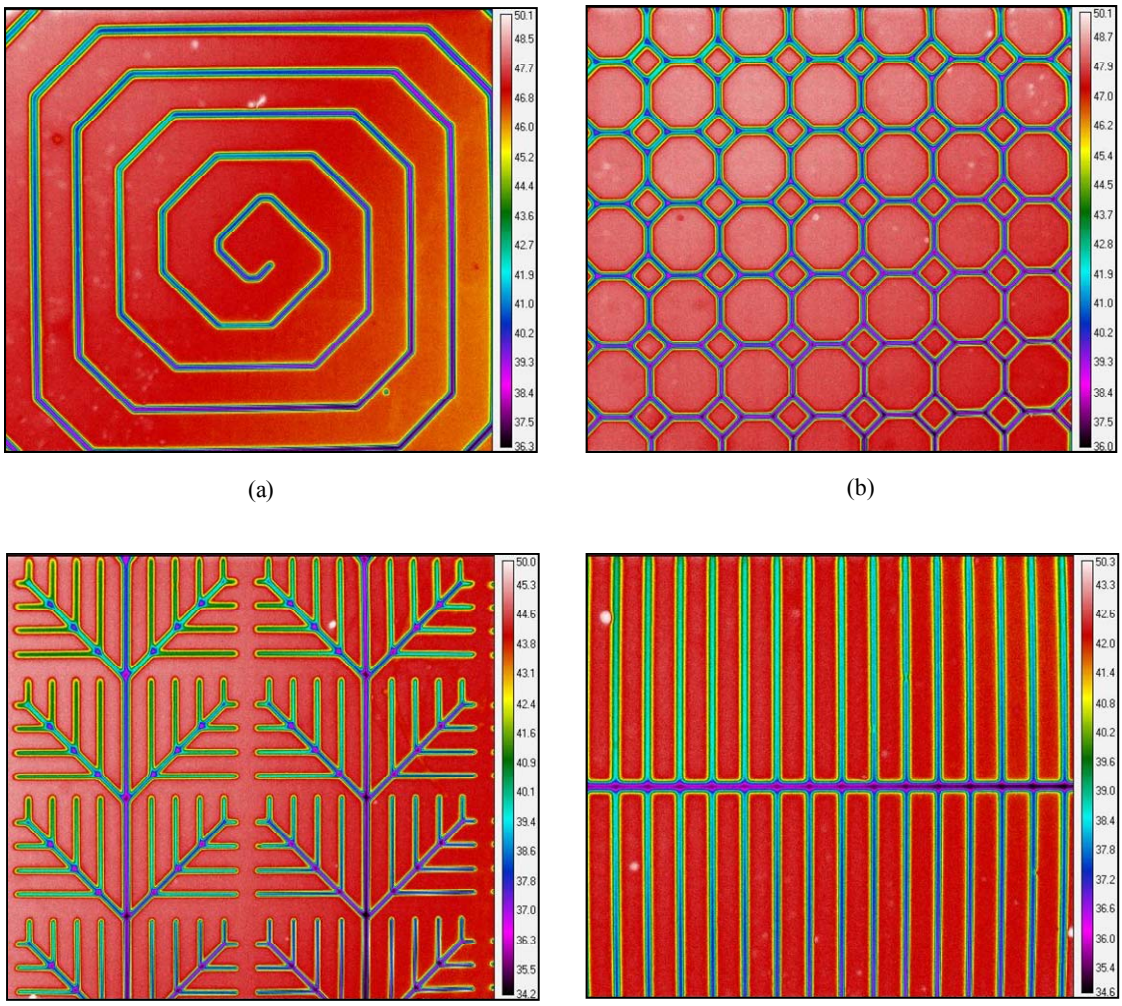
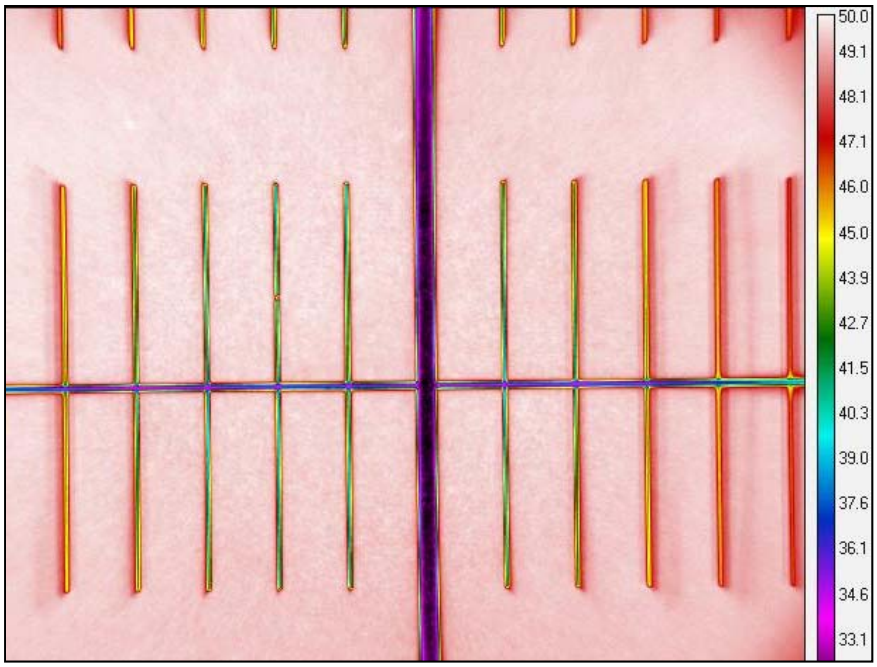
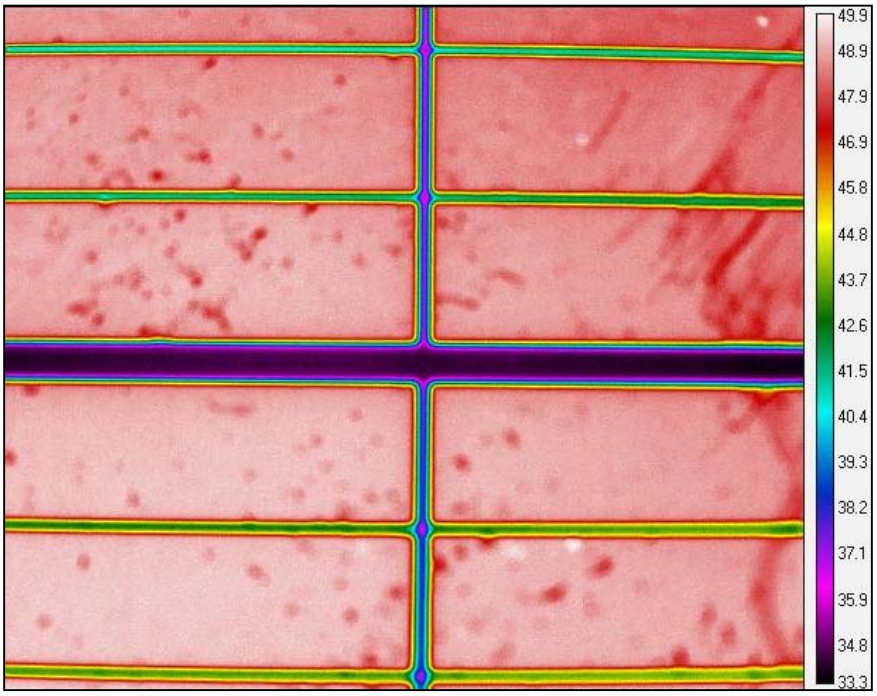


Figure 34. Thermal response of the 7000—14000nm infrared provided average readings of (a) 46.4°C for the incremented spiral; (b) 46.3°C for the ring lattice; (c) 43.2°C for the periodic branching; and (d) 47.9°C for the standard finger and bus design. Each pattern represents a 15.05% surface area covered by metal.



(a)



(b)

Figure 35. Thermal response of the optimized standard finger and bus contact geometry. Results showed (a) 47.8°C average in the 1000—5000nm infrared region and (b) 46.3°C average in the 7000—14000nm infrared region.

4.8. HMJ-Si Efficiency

Each investigated parameter discussed above provided an individual characterization that is not representative of the entire architecture. In order to investigate the trade-offs and overall response from combining these parameters, three distinct architectural configurations were tested. Voltage and current measurements were taken for each of these which consisted of isolated cells (i.e. top-only measurements while in an HMJ-Si configuration), complete top and bottom cell architecture, and responses from replacing the bottom cell with a polished wafer and then with a silver mirror. The results are shown below in Table 11 and characteristic IV curves in Figure 36 (for cell T1) and Figure 37 (for cell T2).

Table 11. Electrical Response of the HMJ-Si Architecture

Sample	Voltage (V)	Current (mA)	P_{max} (mW)	Efficiency
T1 Isolated	0.446	118.5	52.85	8.19%
T1 Bottom	0.332	104.0	34.53	5.35%
T1 Polished Si	0.437	118.4	51.74	8.02%
T1 Ag Mirror	0.440	123.4	54.30	8.42%
T2 Isolated	0.195	66.9	13.05	2.02%
T2 Bottom	0.151	62.6	9.45	1.47%
T2 Polished Si	0.223	71.9	16.03	2.49%
T2 Ag Mirror	0.269	76.0	20.44	3.17%

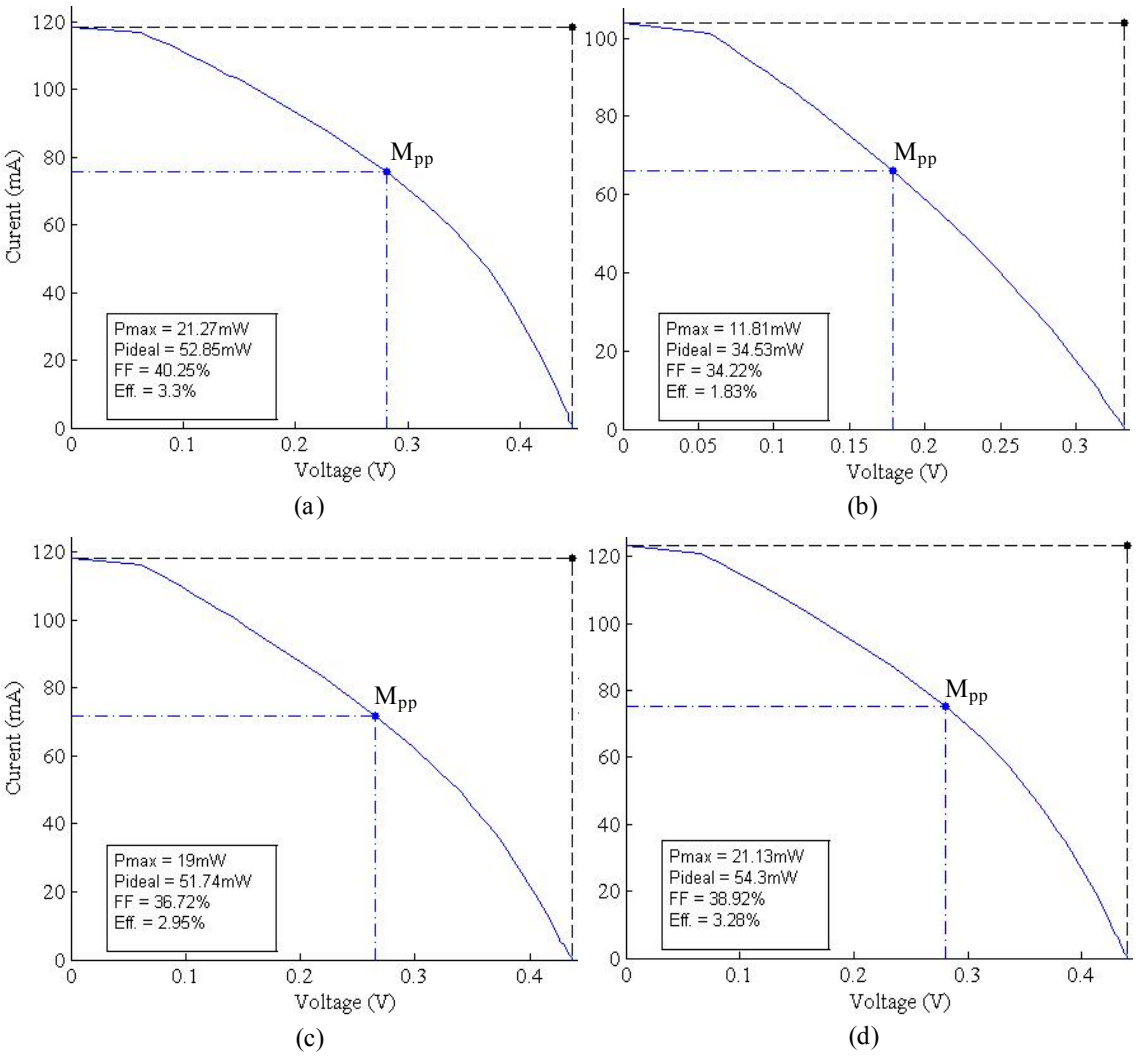


Figure 36. Hybrid multi-junction silicon (HMJ-Si) IV curves for sample T1 in (a) isolated cell, (b) T1/bottom cell, (c) T1/polished silicon, and (d) T1/silver mirror configurations.

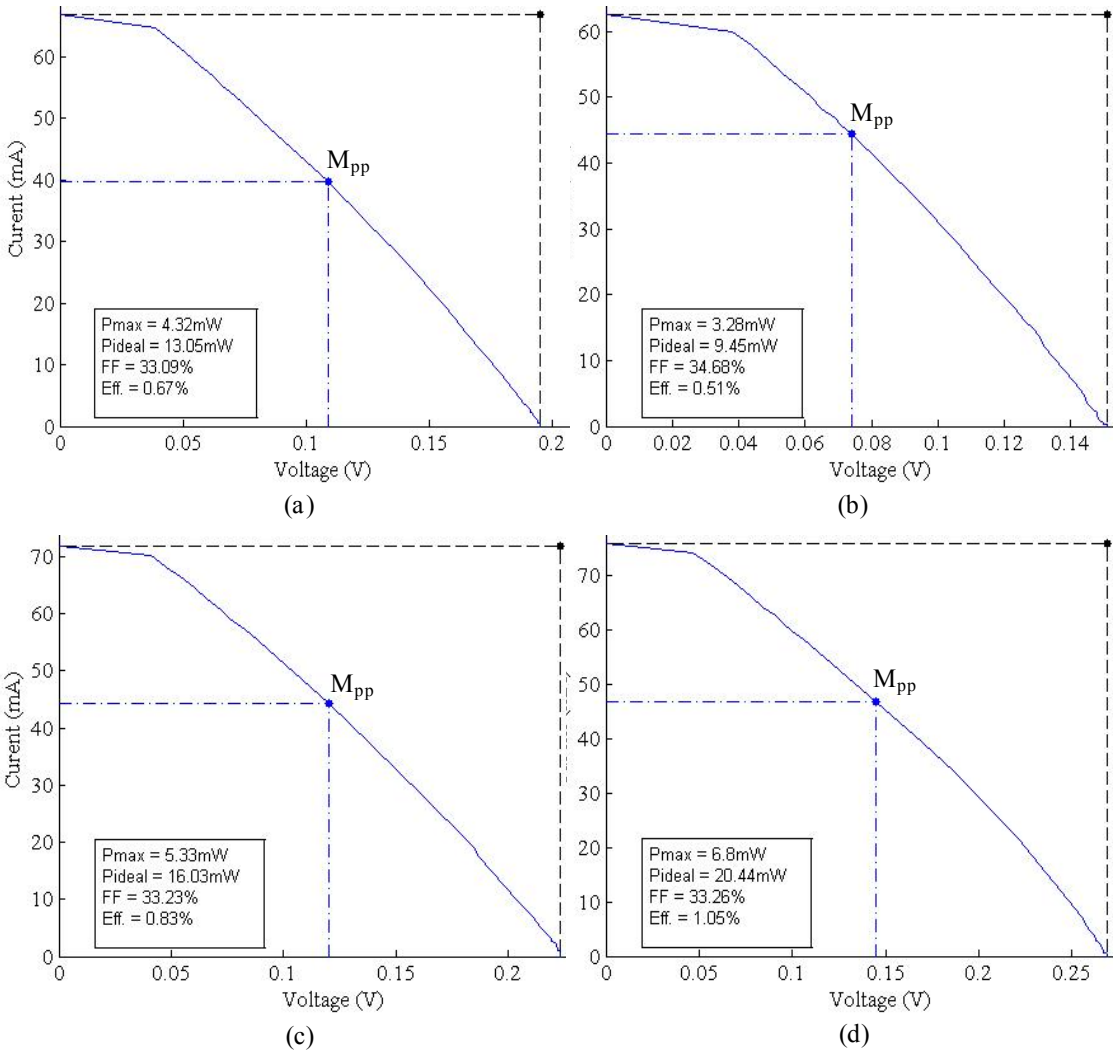


Figure 37. Hybrid multi-junction silicon (HMJ-Si) IV curves for sample T2 in (a) isolated cell, (b) T2/bottom cell, (c) T2/polished silicon, and (d) T2/silver mirror configurations.

Summary

The purpose of this chapter was to provide the data and results obtained during this research. The information in this chapter was divided into sections that matched the parameters identified in Sections 3.3.1—3.3.8.

V. Analysis

Chapter Overview

The purpose of this chapter is to interpret and understand the results from Chapter 4. The information in this chapter is divided into sections that match the parameters identified in Sections 4.1—4.8.

5.1. Wafer Configuration

Using grating contacts for both the front and rear (in lieu of bus/finger and solid rear contacts) allowed each wafer to function as either a top cell or a bottom cell. This technique enabled multiple HMJ-Si configurations using the same cells which eliminated process variation errors. The data was collected using a dedicated meter for the voltage and another for the current so that the total output power could be calculated.

Single-layer silicon solar cells are typically connected in series configuration with each diode orientation being the same; the cathode of one cell is connected to the anode of the next cell. This enables an increase in voltage for higher power delivery and a unidirectional current flow. However, since the HMJ-Si architecture has more than one wafer in each cell, their type and orientation played an important role in overall performance and integration.

The results identified in Table 3 indicated that the worst-performing HMJ-Si orientation (2.93% efficiency) was the unidirectional configuration commonly used in single-layer solar cell panels. The reduced efficiency in this case was due to poor *current matching*. When current matching is not considered for solar cells connected in series, the total current output is limited by the lowest performing cell.

For example, if Cell A produces 75mA and Cell B produces 60mA, the overall series-connected current output is only 60mA (Figure 38). This phenomenon affected HMJ-Si development because the bottom cell received less light than the top cell and therefore produced less photocurrent.

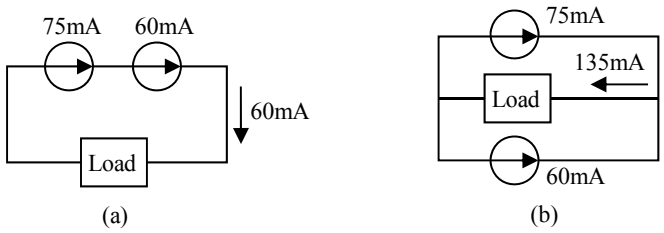


Figure 38. Circuit examples indicating (a) the choking effect of poor current matching and (b) the additive result from parallel current sources. Both cases were studied during the HMJ-Si wafer configuration research.

A parallel-connected architecture avoided the need for current matching by providing an additive current path achieved by using differently doped wafers for the top and bottom cells. Table 3 shows that having an n-type top cell and a p-type bottom cell produced 3.19% efficiency; an even higher increase in efficiency (~3.66%) resulted from the configuration with a p-type top cell and n-type bottom cell. Both configurations were able to produce higher efficiencies because their photocurrents were additive.

The best performing orientation was the p-type top cell and n-type bottom cell because electron mobility is about three times greater than hole mobility (see Section 2.2.1). When the top cell is n-type, the majority of the wafer has excess electrons. This means that free electrons traveled roughly 355μm very quickly while the holes only needed to travel the 2μm of the junction depth (Figure 39). However, this configuration also meant that the p-type bottom cell holes needed to travel through 355μm of silicon. A longer distance and slower hole mobility was compounded even further by the fact that

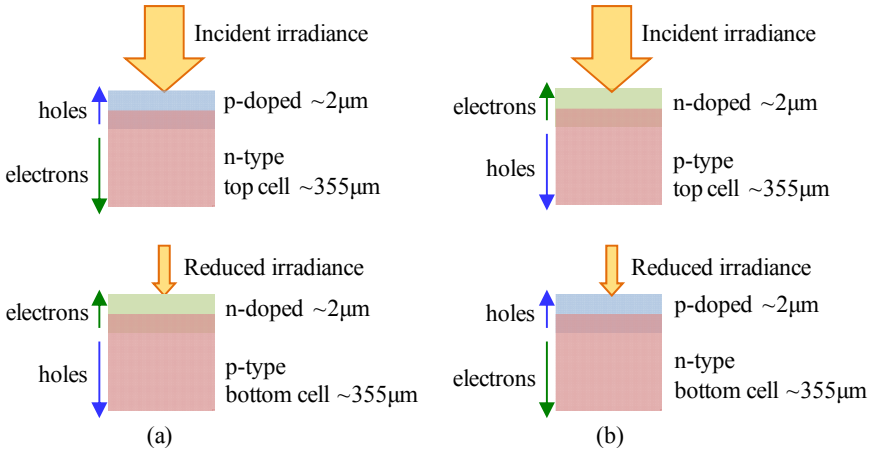


Figure 39. HMJ-Si cross sectional representations identifying electron and hole travel distances. The p-type bottom cell configuration shown in (a) suffers from low hole mobility and fewer freed holes that must travel through 375µm whereas the n-type bottom cell configuration shown in (b) produces better efficiency since electrons can travel the same distance three times as fast.

there was less irradiance in the bottom cell. The lower irradiance freed fewer electrons and holes which yielded a limited efficiency for this configuration. Alternatively, a p-type top cell and n-type bottom cell reduced this limitation. Since a higher amount of irradiance was now incident in the p-type cell, more energy was available to free electrons and holes. Thus, even though holes were moving slower across the longer distance, more were available for photocurrent. In addition, the n-type bottom cell operated more efficiently than its p-type counterpart because its holes only needed to cross 2µm while its electrons quickly traveled the longer distance through silicon.

The optimal configuration for the HMJ-Si architecture was achieved by using an extrinsic p-type silicon wafer for the top cell and n-type extrinsic silicon wafer for the bottom cell.

5.2. Diffusion Profile

The behavior of photocurrent is directly related to the diffusion profile and differences in electron and hole concentration at each junction. An ideal solar cell would collect every free electron so they can be used in an external circuit. In order to approach this level of functionality, recombination must be avoided. An advanced diffusion profile that has subsequent dopant layers at the rear of the cell (the EBSF) was developed to reduce recombination better than existing BSF processing (Figure 40). The EBSF profile was fabricated, tested, and compared to simple junction and BSF solar cells to observe their impact on efficiency.

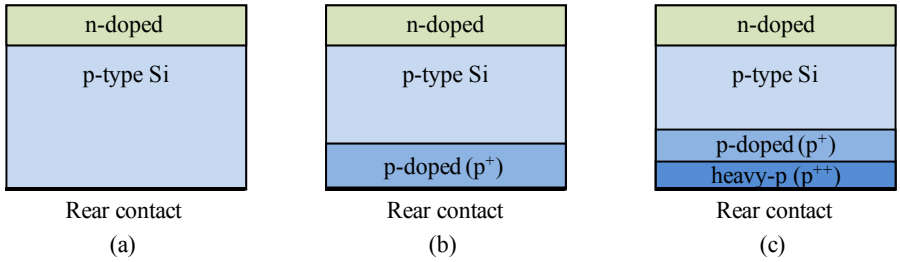


Figure 40. Representations of (a) standard n-p diffusion, (b) back surface field (BSF) diffusion, and (c) enhanced back surface field (EBSF) diffusion. The BSF and EBSF prevent rear-side recombination by redirecting electrons toward the primary n-p junction.

These profiles were tested using the samples annotated in Table 4. The simple junction cells produced measureable results, but they were very low (barely 0.01%) with one exception: the P1 sample produced 1.92% efficiency. This anomaly was considered a data point exception and excluded from analysis. The higher percentage seen in this particular cell can be attributed to a variety of factors that may include extrinsic concentration, dopant source uniformity, wafer thickness, annealing, and other processing variations. The remainder of the samples showed consistent results so the analysis was based on their performance.

The BSF cells provided a significant improvement over the simple junction cells. The p-type cells P3 and P4 showed higher efficiency (3.1-4.4%) than the similarly doped n-type cells N3 and N4 (1.8-2.2%). The lower efficiency of the n-type cells was due to the type of dopant atoms used during diffusion. Using boron to dope n-type wafers created surface defects in the silicon similar to broken ice across a frozen lake. These defects are formed in a boron-silicon layer that requires an additional low-temperature oxidation step [77]. This helps remove defects by "pulling" them into a thin layer of glass grown on the surface of the silicon which is removed during deglazing. However, this processing step was not performed for the samples used in this study; the result was poor efficiency due to a reduction in both photon absorption and surface passivation.

Despite these defects, the novel EBSF profile produced the highest efficiency in the p-type cells P5 and P6 (4.2-5.45%) and the n-type cells N5 and N6 (2.7-3.5%). In each pair of test cells, the unpolished wafers produced higher efficiencies than their similarly-doped polished-front counterparts. The best performing cell—P6—was the p-type wafer with the EBSF n-p-p++ profile using the unpolished side of the wafer. This result corresponds with the wafer diode orientation results from Section 4.1 that identified unpolished p-type wafers as an optimal top cell for the HMJ-Si architecture.

> *The most efficient diffusion profile was the n-p-p++ enhanced back surface field (EBSF) using an unpolished-front, p-type wafer.*

5.3. Front Contact Design

By fabricating four test geometries onto a single wafer, the responses of each design could be accurately compared. Each of the designs covered 15.05% of their respective quadrant, had the same doping profile, and a uniform metal thickness of 150nm of aluminum. Thus, the performance of each design was isolated to its geometry.

The standard finger and bus design, which was used as a baseline comparison model, produced 5.07% efficiency. The remaining designs were measured against this value. The ring lattice produced a higher efficiency, reaching 6.06%. The design was based on point-source rings that collected and transmitted photocurrent quickly to the main bus. The design appears to have less metal coverage than 15%, which means that photons were absorbed in higher concentrations at intervals matching the ring locations (Figure 21b). This grouped-absorption method collected more photons and generated more photocurrent, 105.2mA. The freed electrons were collected by the rings and conducted to the main bus without experiencing current crowding.

The incremented spiral produced a slightly higher efficiency of 6.25%. This increase was primarily caused by the lack of current crowding and surface area coverage. However, because the photocurrent was restricted to a single path, the overall current was limited as observed by a measurement of 104.8mA. This design only achieved a higher efficiency than the ring lattice because it had a higher voltage drop across its p-n junction and although it showed improvement over the baseline, it fell short of the best performing contact design—the periodic branching—which achieved just over 7% efficiency.

The design considerations of surface area coverage and decreased current crowding drove one pattern to take shape like the branches of a tree. This design,

opposite of the ring lattice, appears to cover more surface area than the baseline. Therefore, the layout had optimally-placed metal contacts that were able to collect free electrons in a pattern that covered the wafer more uniformly. In addition, the branching structure enabled current to collect without encountering any choke points or crowding, which is why the current response was the highest of all the samples tested, at 119.6mA.

Based on these results, a full-wafer mask was created using the periodic branching layout. This full design was compared with the standard design shown in Figure 20 and the highly transmissive butterfly design shown in Figure 22. Although the periodic branching had the highest efficiency during the front contact study, covering a full wafer with this pattern limited the amount of absorption and produced just 1.5% efficiency; the increase from removing current crowding was not enough to overcome the irradiance losses. The full-contact finger and bus pattern was 3.76% efficient, offering a significant increase over the periodic branching, but it did not perform as well as the full-contact butterfly design. By avoiding 90° bends in the conductor path and covering only 4.285% of the surface area, the butterfly contact achieved the best result, reaching an efficiency of 3.84%.

> *The most efficient front contact design was the highly-transmissive butterfly geometry based on combining the photon-electron ratio of 1:6 with the 30% S-Q efficiency limit.*

5.4. Grating Contact Design

Initial trials showed that gratings produce interference patterns. The masking matrix produced high-aspect patterns capable of being exploited for contact placement. The results had clear and periodic patterns, but follow-on modeling that incorporated plane wave tilts altered the patterns. However, two grating geometries did produce viable patterns; the best being 400/900μm grating with an associated throughput of 69.2%.

The Lumerical® simulation predicted an interference pattern that more closely resembles recurring shadow bands. There were only slight fringing effects (intensity spikes) near the edges of the grating and had a negligible effect on the overall pattern. Thus, the diffractive nature of light was *not* a factor in the resulting light wave propagation. The shadow bands still eliminated reflection, but there wasn't any noticeable constructive interference (higher intensities) observed. In order for a more effective interference pattern within the HMJ-Si architecture, grating dimensions need to be scaled to the wavelength of interest (e.g. 1μm).

The bottom cell's front contacts were designed to match the periodicity of the 400/900μm grating. The widths were selected to be 200μm wide (which resulted in 1100μm spacing) so that the conduction paths were adequate for photocurrent collection while allowing small variances during processing and alignment.

> *The optimal top cell grating contacts had 69.2% throughput and were 400μm wide spaced 900μm apart. The corresponding bottom cell grating contacts were 200μm wide spaced 1100μm apart.*

5.5. Optical Loss Reduction

The front cell surface significantly impacted how light was absorbed. The diffuse surface provided higher efficiency in each case except for two: a fabrication anomaly (Table 4: P1) and an n-type EBSF cell (Table 4: N5). These results can be attributed to fabrication and processing variances and do not alter the overall observations. The diffuse surface provided better photon absorption (Table 4, Figure 7) for two reasons. First, reflection was reduced because surface roughness had fewer planes that photons encountered at 90°. Oblique angles of incidence helped redirect light into the cell via refraction. The second reason was the additional opportunity reflected light had for absorption when it was reflected into an adjacent surface peak (see Section 2.6.1).

ARC provided an additional enhancement. Although these coatings are used in commercial cells, they are applied in thicknesses that optimize absorption at 600nm [14]. Since HMJ-Si cells are focused on collecting 800-1100nm, different thicknesses were investigated. Absorption increased between 15% and 30% for each sample after adding Si_3N_4 (Table 8). However, the 30% increase absorbed more infrared wavelengths (around 1277nm), which is unwanted heat and outside of the desired bandwidth. The next highest improvement—17.6%—was achieved with 128nm of Si_3N_4. This thickness corresponds to a wavelength of 973nm and is near the center (950nm) of the HMJ-Si bandwidth.

> *Optical losses are minimized in HMJ-Si solar cells by applying 128nm of Si_3N_4 onto an unpolished-front top cell.*

5.6. Electrical Loss Reduction

Transporting freed electrons to an external circuit is accomplished by the front and rear contacts. These contacts, which interface with the silicon as well as the external circuit, need to be large enough to encourage current flow. This was accomplished by increasing the contact thickness and improving the interface between the metal and the silicon.

As the thickness of the metal was increased, the resistivity decreased. This is evident in the results shown in Table 9 where the measured resistance dropped down to as low as 2.3Ω. However, the thickness of the metal isn't the only reason for the lower resistance; the type of metal also had an impact. Different metals are composed of different atom structures and although they are all conductors, they each conduct at distinct "speeds". Conductivity—the reciprocal of resistivity—is a property specific to each material and is a measure of how easily it can transport electrons. Since silver has a higher conductivity, it performed much better (6.2Ω) than the similarly-shaped aluminum (14.3 Ω). In addition, using titanium impacted contact resistance since it is a poor conductor; its resistivity 15 times higher than aluminum. Therefore, in order to keep the resistance low, the titanium layers were limited to 50nm.

The interface between titanium and silicon is also important since a poor contact can result in high resistance. An ohmic contact that has low resistance is typically created using an RTA process. This research focused on the formation of titanium silicide through the three RTA recipes shown in Table 10. There was no significant difference between the annealing times of 20 and 30 seconds for the aluminum contacts, indicating that there is no benefit in keeping the samples at 450°C longer than 20 seconds.

Based on this data, silver contacts were studied using RTA times of 20 seconds. The runs tested both 450°C and 650°C since silver has a higher melting point (961°C) than aluminum (660°C). The higher temperature—650°C—provided the best improvement and resulted in a 90% reduction in contact resistance. This can be attributed to the enhanced formation of titanium silicide at higher temperatures and the resulting creation of a better ohmic contact.

> *Electrical losses are minimized in solar cells by using contacts that are a metal composition of 50nm titanium and 500nm silver which have been rapidly thermal annealed at 650°C for 20 seconds.*

5.7. Thermal Loss Reduction

Reducing the thermal rise for solar cells is a vital part of efficient operation. Unlike typical solar cells, HMJ-Si cells have an isolating air gap between the cells that lowers internal heat. This air gap, although primarily used for interference pattern formation, helps reduce the heat reaching the bottom cell by ≈1.7°C (Figure 32). This reduction may not be significant for terrestrial applications, but can greatly impact the operation of solar panels on satellites where any thermal expansion can be catastrophic. These results verify that without any forced convection the air gap does provide a thermal differential between the two cells.

Dissipating the heat that is present in solar cells (since it cannot be removed completely) is another design parameter that can help increase the power density for solar cells. This can be accomplished by the front contact design, which is exposed to the environment and can benefit from conventional forced-convection cooling systems. The front contacts that were designed to enhance photon absorption also contributed to the thermal characteristics of the cell. Each pattern was examined to see which geometry offered the best thermal reduction in both the 1000-5000nm and 7000-14000nm range.

For the 1000-5000nm range (Figure 33), the highest average temperature observed was the standard finger and bus contact at 40.3°C. Even though this pattern had the same amount of metal on the surface as the others, it was poor at dissipating heat. The best patterns were the incremented spiral and the periodic branching with temperatures of 37.5°C and 37.8°C, respectively. These contacts were able to reduce heat due to the design of the pattern and were more effective than the ring lattice which showed 39.7°C. The lack of current crowding in each of these contributed to lower thermal readings and

identified that standard finger and bus contacts are not optimized for thermal management.

The 7000-14000nm range had similar results (Figure 34), with the finger and bus pattern having the highest temperature of 47.9°C. These results further support the impact of current crowding and pattern design on the thermal response of solar cells. The lowest temperature for this range was the periodic branching, which maintained an average of 43.2°C. This design not only helped with current flow, but clearly dissipated higher wavelengths of heat more efficiently than both the incremented spiral and ring lattice designs (46.4°C and 46.3°C, respectively).

Averaging temperatures for both of these ranges identified the pattern that had the most efficient total heat dissipation (THD); the periodic branching at -9.5°C. The ring lattice design was intended to reduce current crowding, but a THD of -7.0°C identified this design does not operate as intended; current pooled up at the junctions and created hot spots that were counterproductive to heat dissipation. The incremented spiral managed a THD of -8.0°C, which was due to the set distances between the contacts and its increasing thickness. Finally, the standard finger and bus had a THD of only -5.9°C.

However, these tests only identified which front contact pattern design covering 15.05% of the surface was the most efficient. Since metal conducts and dissipates heat more quickly than silicon, additional tests were performed to see how much average heat a standard, full-wafer contact pattern experienced (Figure 35). Tests for this pattern were also run for both wavelength ranges, resulting in a THD of -2.9°C.

The lower THDs identified that a larger amount of surface area metal helps keep solar cells cooler. However, there are trade-offs in each case because in order for the

amount of surface area covered by metal to enhance efficiency, the gains from heat dissipation must be greater than the losses from photon reflection. Therefore, further investigation is required to characterize the effect on efficiency due to the relationship between surface area coverage, heat dissipation, and photon absorption.

> *The bottom cell of the HMJ-Si architecture exhibits a temperature approximately 1.7°C below the top cell. The contact pattern that dissipated the most heat was the periodic branching pattern with a total heat dissipation (THD) of -9.5°C.*

5.8. HMJ-Si Efficiency

Although the above parameters were optimized individually, they do not support a full characterization of the architecture. Combining the best result from each study was the only way to identify the resulting trade-offs and determine the overall viability of the HMJ-Si solar cell.

The most significant observation was how the voltage was affected by connecting the cells in parallel, which was done to avoid the limitations imposed by poor current matching. Having voltage sources in parallel is atypical in electronic circuits due to back-feeding and possible over-charging. The higher voltage feeds the lower voltage source and degrades the circuit power. HMJ-Si solar cells operate differently in that one cell doesn't charge the other, but the overall voltage suffers from a type of "voltage-splitting" which reduced the overall performance to ≈0.335V. This phenomenon had the largest impact on limiting efficiency—evident in the T1/Bottom and T2/Bottom configurations in Table 11—because the combined current wasn't high enough to overcome the decrease in voltage. The reason for the limited overall current was the bottom cell received less light and barely contributed to the overall current. This observation led to the investigation of three alternatives: a thinner top cell, a polished silicon wafer as the bottom cell, and a silver-coated (mirror) wafer as the bottom cell.

These configurations were tested as shown in Table 11 with the corresponding IV curves shown in Figure 36 and Figure 37. The thinner wafers, which incorporated a Si_3N_4 ARC coating, showed the highest efficiencies. Sample T1 reached 8.2% due to the combination of thicker metal, ARC, wafer thickness, and EBSF doping profile. The efficiency increased to 8.42% when a silver mirror was used as the bottom cell to negate

voltage degradation effects. Using a mirror as the bottom cell reflected photons back into the top cell where they contributed to photocurrent. This reflected absorption was assisted by the EBSF diffusion profile reducing recombination.

Sample T2 did not perform as well because the voltage and current responses within the cell were poor. Variations in the type of wafer and the fabrication process can account for the decrease in performance between the two thinner wafers (T1 and T2). Although this cell barely reached 2% efficiency in isolated measurements, it responded similarly to sample T1 when replacing the bottom cell with a mirror, reaching 3.17%.

Using an undoped polished silicon wafer as the mirror also provided higher efficiencies over the isolated cells, but the surface of the cell was not reflective enough to contribute to photocurrent as much as the silver mirror. These configurations provided inconsistent results between the two cells, lowering the performance of sample T1 and increasing the performance of sample T2. Additionally, since a silicon wafer as the bottom cell absorbed a portion of the incident light, it was not considered a viable alternative.

The IV curves (Figure 36, Figure 37) indicated that the fabrication process and parameters were not optimized for integration because the curves aren't square. However, they did provide information about the response of each configuration. The MATLAB® code used to generate the plots also ran an internal algorithm to locate M_{pp} and calculate the fill factor (see Appendix A.2). The isolated cell measurements provided a baseline for the other configurations to be measured against. For sample T1, the fill factor decreased when the bottom cell was included in the circuit. This was a result of the previously mentioned voltage degradation. With the silver mirror as the bottom cell, the fill factor

was near its original value of ≈0.40. These results indicate that fill factor is affected by the type of configuration.

However, sample T2 produce different results, maintaining a fairly consistent fill factor of ≈0.33. The poor performance of the top cell when isolated reduced the fidelity of the other configurations resulting in each one having a smaller impact on performance. Since the disparity between the readings wasn't large enough to discount measurement, instrumentation, and environmental errors, the results from sample T2 can not accurately represent the full response of the architecture. Therefore, HMJ-Si solar cell characterization was based on sample T1.

The HMJ-Si architecture experienced enhanced light trapping and the highest efficiency from using an undoped silver-coated wafer as the bottom cell.

Summary

The purpose of this chapter was to interpret and understand the results from Chapter 4. The information in this chapter was divided into sections that match the parameters identified in Sections 4.1—4.8.

VI. Conclusions and Recommendations

Chapter Overview

This chapter concludes the above research by identifying the overall observations and presenting recommendations for future research related to this work.

6.1. Observations

The efficiency gains from reflecting light back into the top cell proved that the HMJ-Si architecture employed a successful light trapping technique. The overall efficiency ratings aren't as high as commercial cells—typically around 16%—due to a set of material and process variables. First, the doping profile was inconsistent from wafer to wafer. Having an exact recipe that provides a voltage drop and electron behavior in accordance with the design intent is paramount to obtaining higher efficiencies. These inaccurate diffusion profiles produced lower than expected voltage drops which significantly impacted efficiency. The performance was decreased even further from the voltage degradation imposed by the parallel-connected top and bottom cells.

In addition, the amount of photocurrent generated was limited by the metal contact thickness. Although the investigated thicknesses showed lower resistance, they were still at least 20 times thinner than commercial solar cell contacts (Table 9) and imposed a resistance to electron flow. Other factors contributing to lower efficiencies include grating contact alignment errors, wafer inconsistency, wafer thickness, ARC uniformity, and measurement equipment limitations. The HMJ-Si architecture is capable of generating higher efficiencies as indicated in Section 5.8, assuming a refined fabrication process that removes variations and errors. The architecture responds as expected, allowing light to propagate through the top cell for an additional opportunity

for absorption. However, eliminating the voltage degradation is critical and requires a contact redesign that incorporates a series-configured parallel-cell layout or an alternative diffusion profile (Section 6.2). Although future designs will provide a more thorough understanding of the potential efficiency increases inherent in the HMJ-Si architecture, efficiency gains were seen throughout this research (Figure 41).

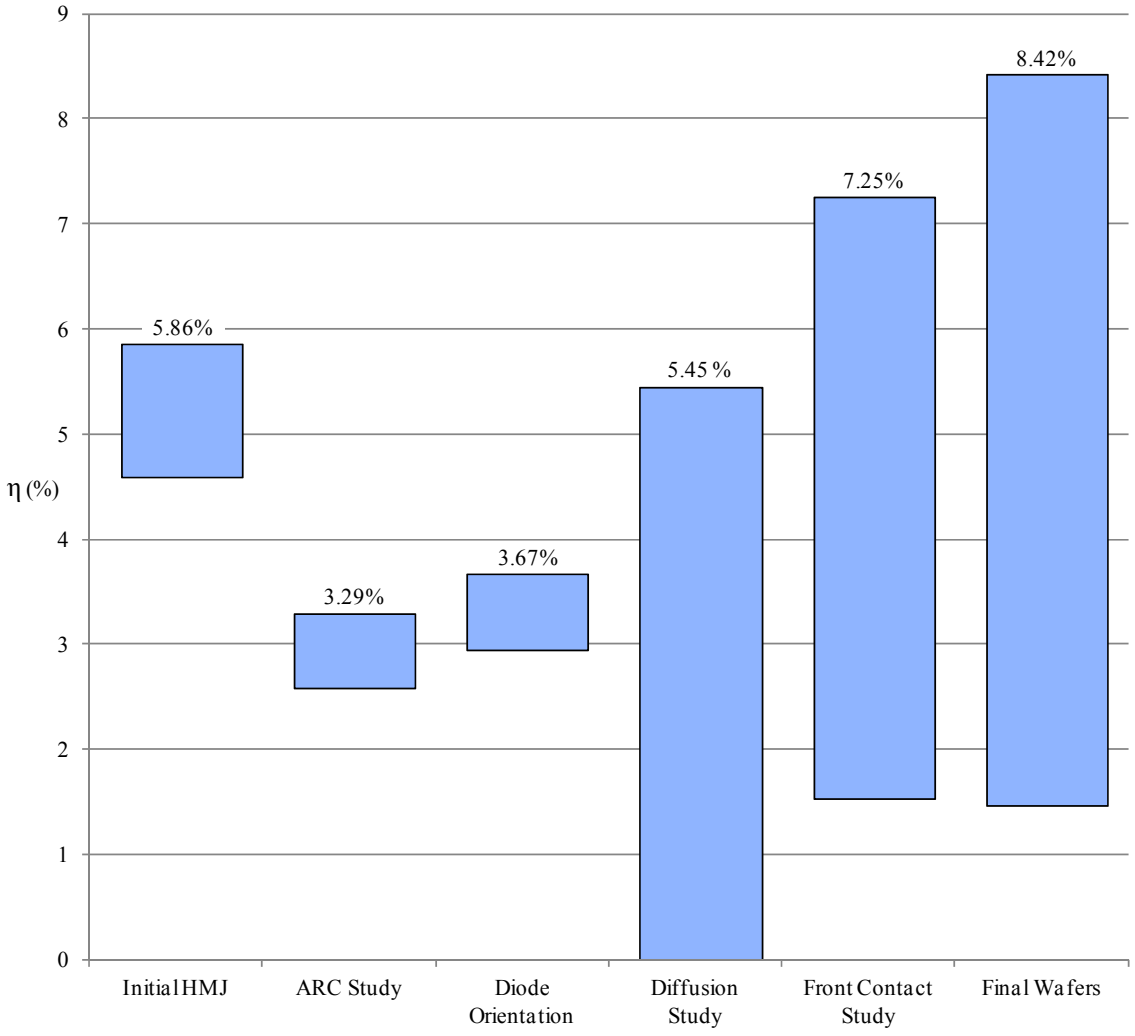


Figure 41. Maximum efficiency (η) ranges achieved during HMJ-Si development; the highest maximum efficiency for each parameter is identified at the top of its respective range.

6.2. Future Considerations and Recommendations

Further investigation is required to exact a highly-efficient HMJ-Si architecture viable for commercial or military implementation. Furthermore, additional ideas and design considerations were uncovered during this research which should also be explored.

Advanced diffusion profile analysis that identifies the best-performing junction depth to within 100nm will be beneficial for both the primary depleted region and EBSF characterization. An alternative diffusion profile was conceived with enhanced performance through the inclusion of localized secondary depleted regions (Figure 42). The intent of this profile is to simultaneously increase photon absorption and decrease recombination through the addition of rear-side p-n junctions. These localized homojunction depleted-region arrays, in conjunction with BSF doping, will offer opportunities for both transmitted photons and reflected photons to be absorbed within the HMJ-Si structure.

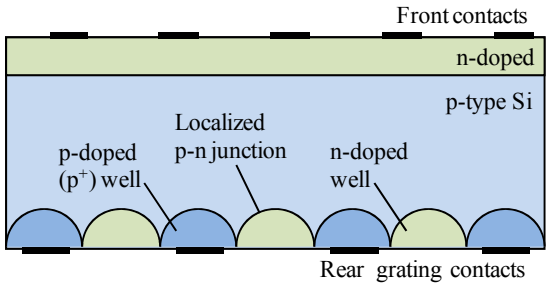


Figure 42. Cross-sectional view of a proposed HMJ-Si top cell with advanced diffusion profile. Localized homojunction depleted region arrays, which are additional p-n junctions at the rear of the cell, should increase efficiency through enhanced absorption of both incident photons and bottom-cell reflected photons.

An alternative approach that avoids the voltage degradation apparent in the HMJ-Si architecture relies on how the cells are connected. By connecting an array of top cells

and an array of bottom cells independently, the efficiency can be enhanced without increasing the complexity processing. This design parameter should also be studied, which would require a redesign of the inner contact to encourage more light to propagate into the bottom cell for higher efficiencies, maybe even using thin-film technology in lieu of the standard silicon wafer as the top cell.

Another consideration is the air gap distance and grating pattern. The grating patterns designed and modeled in this research produced shadow-band interference patterns. In order to exploit a high-aspect ratio interference pattern, the width of the spaces between the gratings should be roughly the same order of magnitude as the incident wavelength. Thus, a spacing of 1μm (which corresponds to 1000nm wavelengths) will improve the patterns if the grating widths still allow at least a 50% throughput. However, this will also require additional modeling to confirm the gap distance and whether it is feasible for low-cost fabrication. In addition to adjusting the grating geometry, investigation into the gap distance for photons reflected by a bottom cell mirror will improve the response of the architecture. Shifting the focal length to twice the distance of the air gap will also require an adjusted grating pattern. The results will indicate if even higher photon absorption is possible through reflected interference patterns that still incorporate thermal reduction via the internal air gap.

Finally, additional testing is required to verify the viability of the HMJ-Si in commercial and military applications. This testing should include panel integration tests, AM0/vacuum environment tests, and verification by processing commercially available cells into the HMJ-Si configuration. These tests will identify the applicability of this work and how it can best be applied to increase solar cell efficiency.

6.3. Conclusion

Producing more efficient solar cells that cost less is the only way to increase photovoltaic implementation. This research provided the framework for a novel architecture that enhances efficiency and power density without requiring complex or expensive processes or materials. The results support the proof-of-concept that this architecture is a viable solution, but the investigation was not exhaustive.

The parameters explored in this work offer a framework for further study; a general analysis and direction for additional research. Unfortunately, time and processing constraints prevented the ideal optimization of each parameter or the architecture as a whole. Certain assumptions had to be made to engage in this research and when those assumptions are removed through a finely-tuned scope of experimentation for each parameter, a high-efficiency light trapping technique will emerge. Although finalizing the architectural details and removing process errors will inevitably modify the original design, the above information provided a blueprint for a low-cost solution that will hopefully aid in the proliferation of photovoltaics as a renewable energy source.

Summary

This chapter concluded the HMJ-Si architecture research and development by identifying the overall results, observations, future considerations, and recommendations.

Appendix A. MATLAB® Code

A.1. Diffraction Grating Code

```
%------ Parameter setup ------------------------------------------------
clear; clc; format long g;
j       = sqrt(-1);                                 % Imaginarium
c       = 299792458;                                % Speed of light
h       = 6.62606957e-34;                           % Planck's constant
JeV     = 1.602176565e-19;                          % Joules per eV
EgSi    = 1.12;                                     % Si Bandgap Energy
maxlam  = h*c/JeV/EgSi;                             % Max wavelength
dx      = 20e-6;                                    % Plane sample size
N       = 10;                                       % Plane width
lam     = 800e-9;                                   % Min wavelength

%------ Phase delay for propagating through Si and Si02 -------------------
Ds      = 1e-5;                                     % Si depth = 10um
Ns      = 3.538;                                    % Si refr. index
Do      = 2e-6;                                     % SiO2 depth = 2um
No      = 1.449;                                    % SiO2 refr. index
delay   = exp(-j*2*pi*(Ds*Ns+Do*No)/(maxlam*c));    % Delay thru Si/SiO2
Open        = 42;                                   % Open grating
Closed      = 22;                                   % Closed grating
Gap         = 385e-6;                               % Mask to cell dist
delIO       = 0;                                    % 1: delay on
tiltIO      = 1;                                    % 1: tilt on

%------ Grating pattern prep ----------------------------------------------
Patt        = Open+Closed;                          % Grating pattern
M           = round(3.5*Patt);                      % Plane height
MLOW        = round(M/4);
MHIGH       = round(3*M/4);
Mask        = zeros(M,N);                           % Grating mask plane
del         = delay*delIO;                          % Delay toggle

%------ Open grating generation -------------------------------------------
for k=1:Patt:M
  for i=k:k-1+Open
    Mask(i,:)= 1;
end; end

%------ Closed grating generation -----------------------------------------
for p=1:M
  if Mask(p,:)==0;
    Mask(p,:)= del;
end; end

%------ Propagation prep --------------------------------------------------
mask_cx=10; mask_cy=M/2;                            % Mask plane center
cell=zeros(M,N);                                    % Solar cell plane
cell_cx=10; cell_cy=M/2;                            % Cell plane center
```

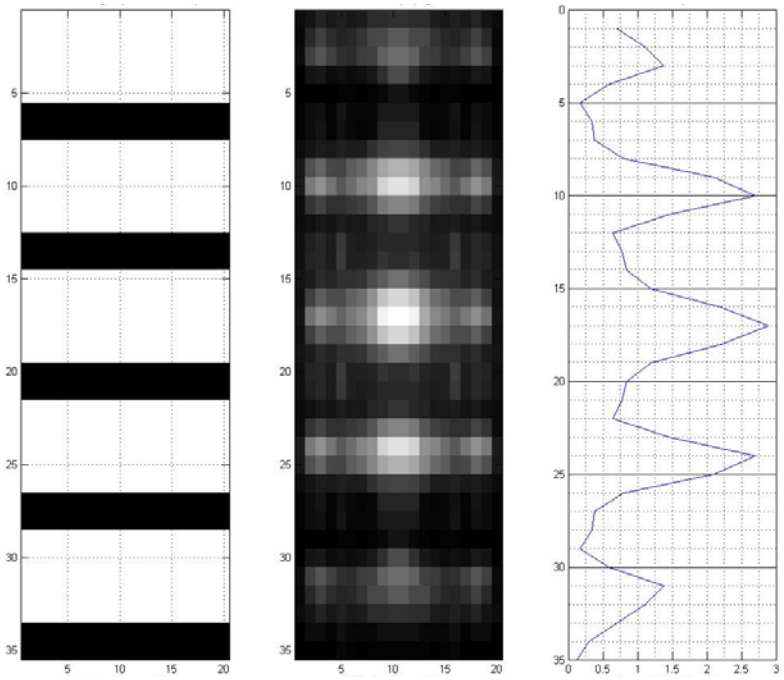
```
%------ R-S Propagation (point to point) ----------------------------------
for lam=800:10:1100                                  % Varied for bandwidth
  fprintf('Running lambda = %gnm\n',lam)
  lam=lam*1e-9;                                      % convert lam to nm
  for tiltAng=-0.005:0.001:0.005;                        % Varied for tilt
    fprintf(' for tilt = %grad\n',tiltAng)
    for cell_x=1:N
    CX=(cell_x-cell_cx)*dx;
    for cell_y=MLOW:MHIGH
      CY=(cell_y-cell_cy)*dx;
      for mask_x=1:N
        MX=(mask_x-mask_cx)*dx;
        for mask_y=MLOW:MHIGH
          MY=(mask_y-mask_cy)*dx;
          dist                = sqrt(Gap^2+(MX-CX)^2+(MY-CY)^2);
          tilt                = exp(j*tiltIO*2*pi*MY*tiltAng/lam);
          kernel              = exp(2*pi*j*dist/lam)/(j*lam*dist^2);
          propagation         = dx^2*Gap*tilt*Mask(mask_y,mask_x).*kernel;
          cell(cell_y,cell_x) = cell(cell_y,cell_x) + propagation;
end; end; end; end; end
fprintf('\t*Completed*\n\n')
end
fprintf('*** Run Completed ***\n\n')

%------ Plot grating pattern ----------------------------------------------
figure(1)
subplot(1,3,1)
imagesc((1:N),(1:M),abs(Mask).^2); colormap(gray)
title([num2str(Closed*20),'um Grating  |  ',num2str(Open*20),'um Spacing'])
ylabel('distance (x 20um)'); grid on

%------ Plot response image -----------------------------------------------
subplot(1,3,2)
cell=abs(cell).^2;
imagesc((1:N),(1:M),cell); colormap(gray)
title(['Intensity after ',num2str(Gap*1e6),'um'])
ylabel('distance (x 20um)')

%------ Plot intensity graph ----------------------------------------------
subplot(1,3,3)
rowsum = round(sum(cell,2));
plot(rowsum,1:M); axis('ij'); ylim([1 M])
title('2D Diffraction Representation')
refline(0,Open); refline(0,3*Patt)
total=0;
for rowint = 1:1+(3*Patt-Open)
    total = total + rowsum(rowint);
end
xlabel(['Region Sum = ',num2str(total/1e4)]); grid on; grid minor
ha = axes('Position',[0 0 1 1],'Xlim',[0 1],'Ylim',[0
1],'Box','off','Visible','off','Units','normalized', 'clipping' , 'off');
text(0.5, 1,'800 to 1100nm Waves;  -0.005 to 0.005rad
Tilt','HorizontalAlignment' ,'center','VerticalAlignment', 'top')
saveas(gcf,[num2str(Gap*1e6),'gap_',num2str(Closed*20),'x',num2str(Open*20),'_H
iRes.jpg']);
```

A.2. IV-Curve Generator Code

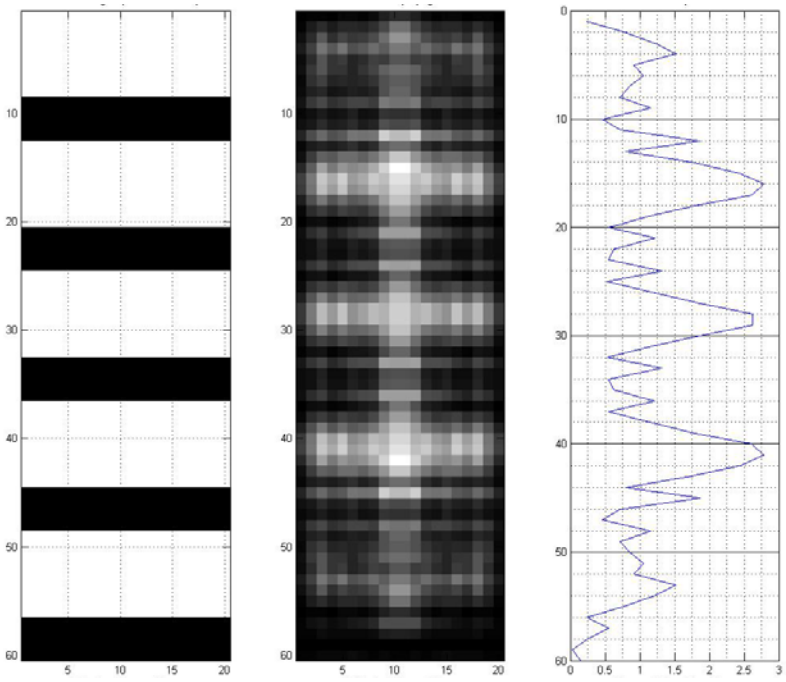
```
clc; clear all;
a = 100; % sets decimal point accuracy
set(gca,'fontname','times','FontSize', 12)

I=[77.9             % add Isc here
74                  % add measured currents here
0];                 % add 0 here

V=[.0               % add 0 here
.130                % add measured voltages here
.516];              % add Voc here

%%------------------isolate Isc and Voc
lim=max(size(V));
Isc = I(1,1);
Voc = V(lim,1);

%%------------------find max power point
P=V.*I;                                 % establish power matrix
[num index] = max(P(:));                % find indices of highest value
Loc=ind2sub(size(P),index);             % store indices as a matrix
Impp=I(Loc,1);Vmpp=V(Loc,1);            % store corresponding values from I, V
Mpp=[Vmpp, Impp]
Pmax=Impp*Vmpp                          % Pmax baby!
Pideal = Isc*Voc
FF = Pmax*100/Pideal

%%------------------calculate efficiency n% = 100*(max power)/(input power)
Pin_Masked_Square = 2.351;
Pin_Full_Circle = 2.656;
Pin_OneInch_Square = 0.645;
n = round((100*Pmax/1000/Pin_Masked_Square)*a)/a

%% plots
figure(1)
hold on; grid off;
plot(V,I)
VocX = [Voc, Voc]; VocY = [0, Isc];
IscX = [Isc, Isc]; IscY = [0, Voc];
plot(VocX,VocY,'--','Color','k');
plot(IscY,IscX,'--','Color','k');
plot(Voc,Isc,'.','MarkerSize',14,'Color','k')
Vmpp_X = [Vmpp, Vmpp]; Vmpp_Y = [0, Impp];
Impp_X = [Impp, Impp]; Impp_Y = [0, Vmpp];
plot(Vmpp_X,Vmpp_Y,'-.','Color','b');
plot(Impp_Y,Impp_X,'-.','Color','b');
plot(Vmpp,Impp,'.','MarkerSize',14,'Color','b')

%% graph polishing
axis([0 (Voc*1.1) 0 (Isc*1.1)])
title('IV Curve for Cell: A1T');
xlabel('Voltage (V)'); ylabel('Curent (mA)');
values = {['Pmax = ',num2str(round(Pmax*a)/a),'mW']
    ['Pideal = ',num2str(round(Pideal*a)/a),'mW']
    ['FF = ',num2str(round(FF*a)/a),'%']
    ['Eff. = ',num2str(round(n*a)/a),'%']};
annotation('textbox', [0.18,0.22,0.1,0.1],'String', values)
```

Appendix B. Additional MATLAB® Simulation Results

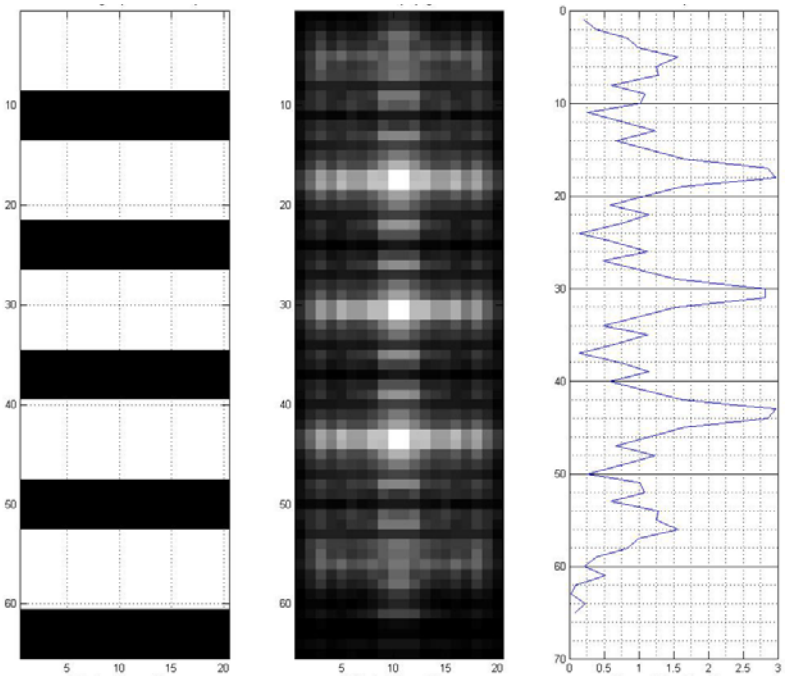
100µm/250µm Spacing, Full Bandwidth, No Tilt, Low Resolution



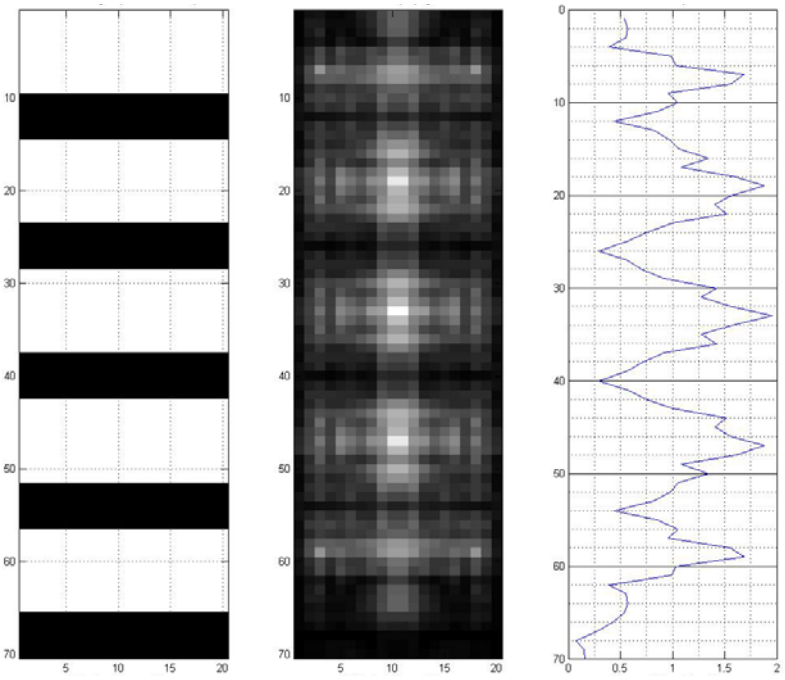
200µm/400µm Spacing, Full Bandwidth, No Tilt, Low Resolution



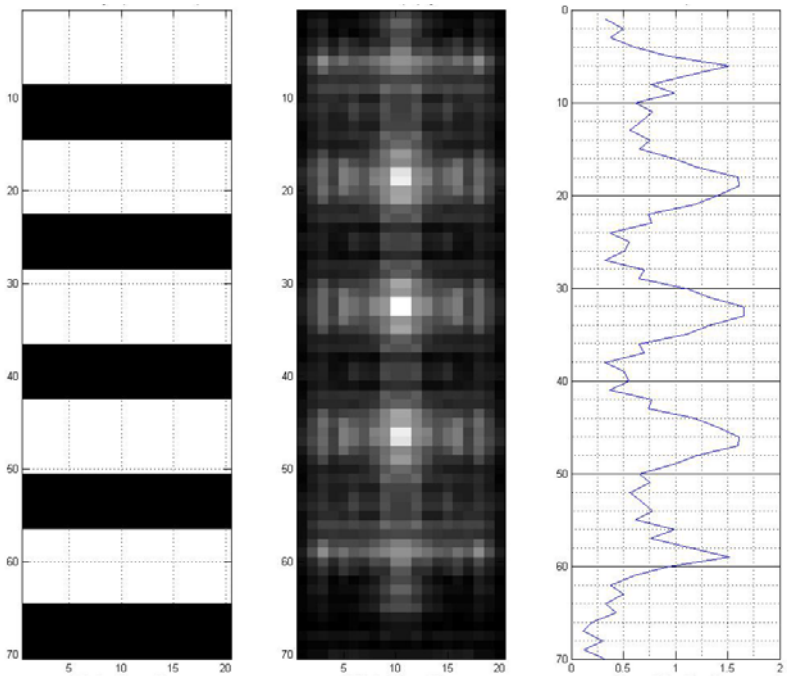
250µm/400µm Spacing, Full Bandwidth, No Tilt, Low Resolution



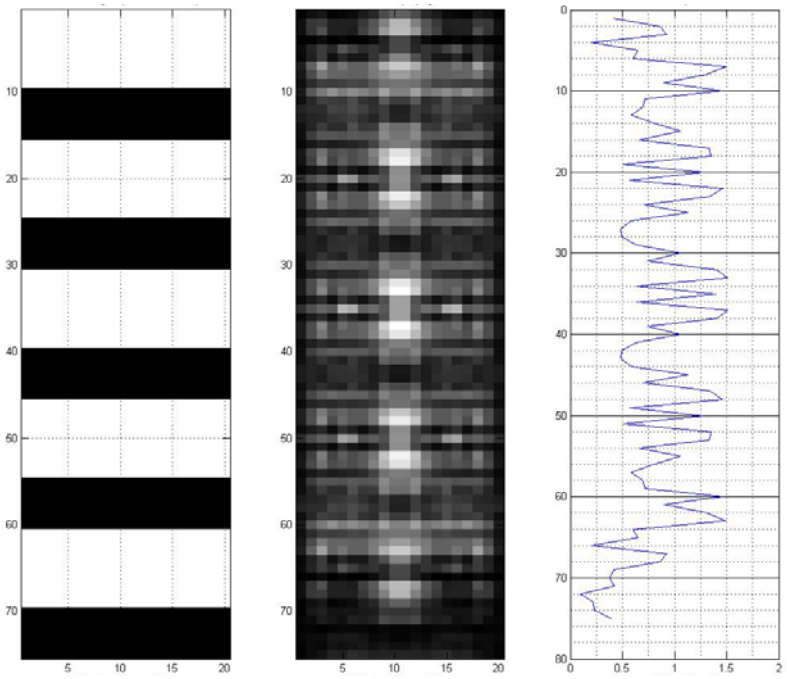
250µm/450µm Spacing, Full Bandwidth, No Tilt, Low Resolution



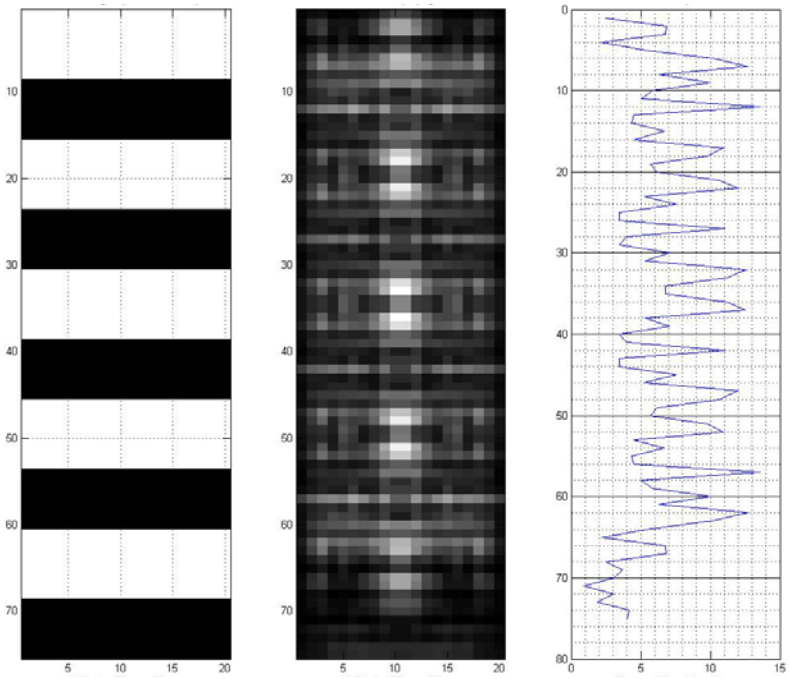
300µm/400µm Spacing, Full Bandwidth, No Tilt, Low Resolution



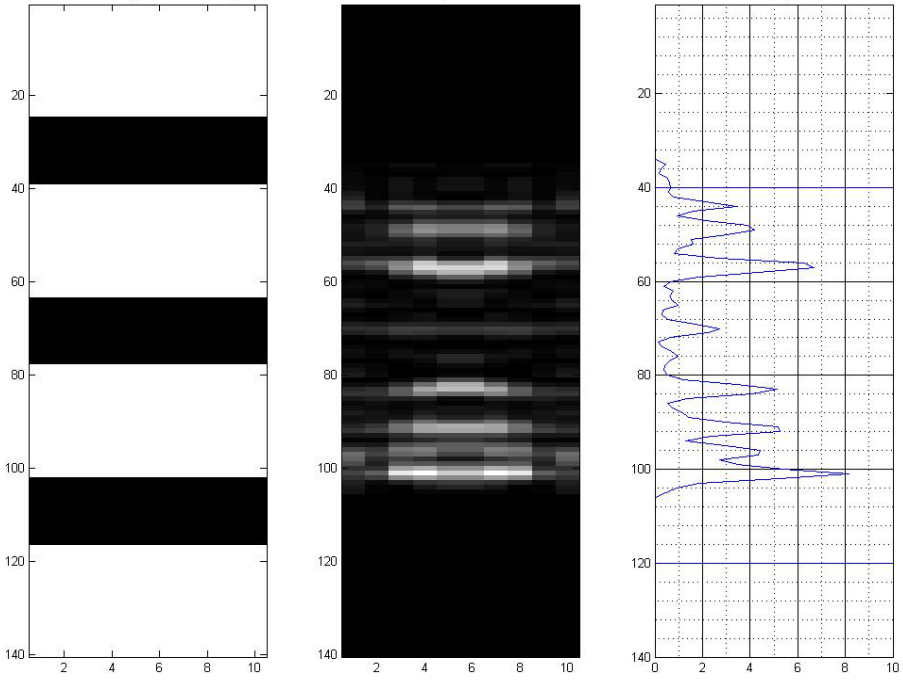
300µm/450µm Spacing, Full Bandwidth, No Tilt, Low Resolution



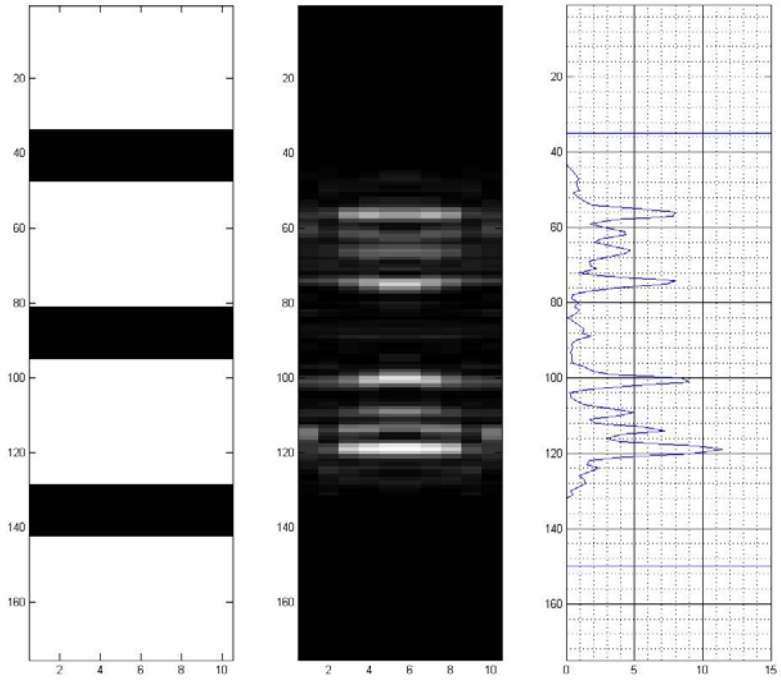
350µm/400µm Spacing, Full Bandwidth, No Tilt, Low Resolution



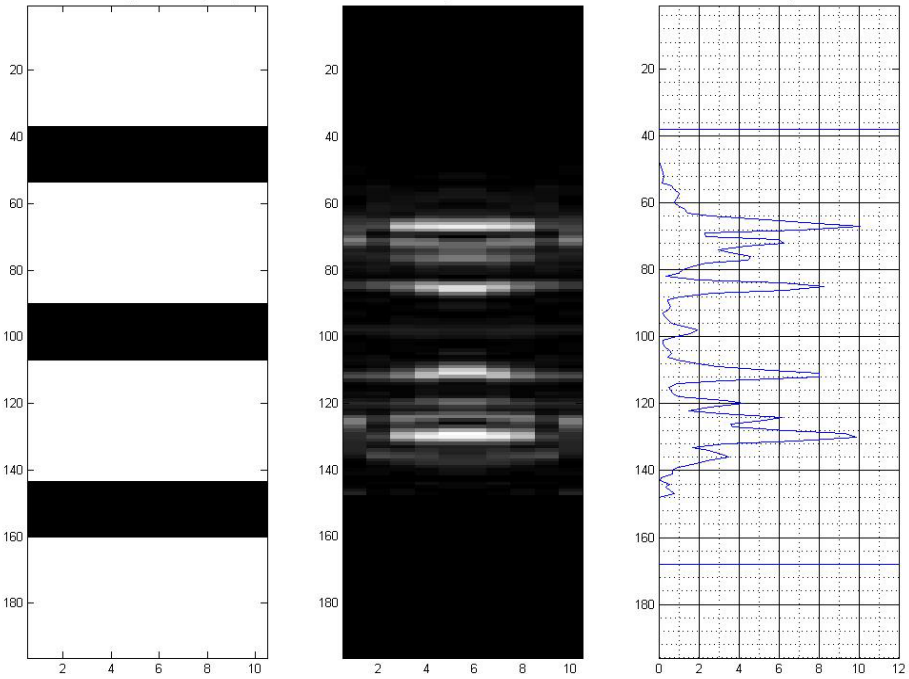
300µm/500µm Spacing, Full Bandwidth, Full Tilt, Low Resolution



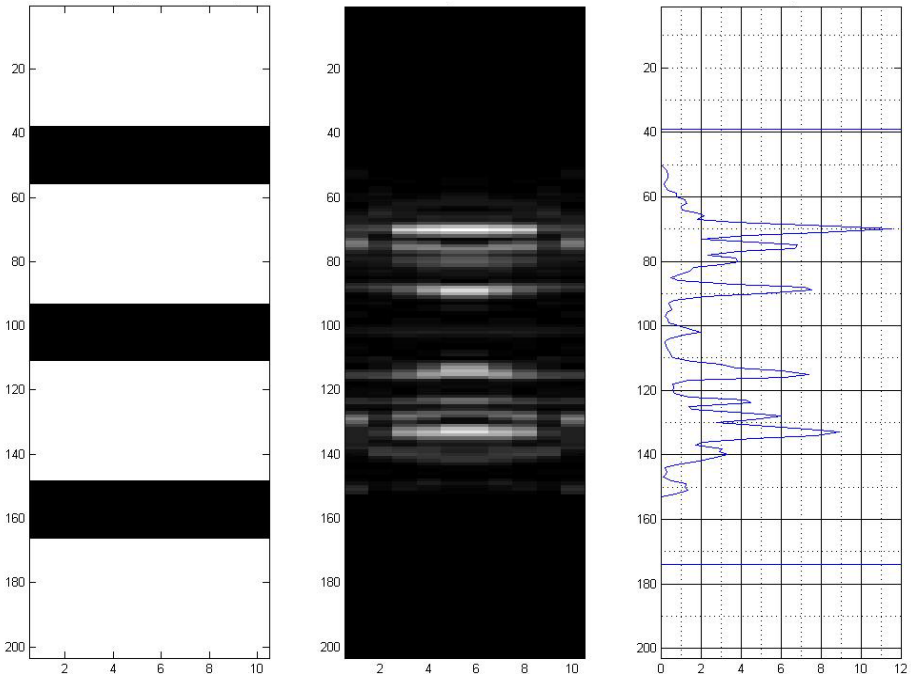
300µm/700µm Spacing, Full Bandwidth, Full Tilt, Low Resolution



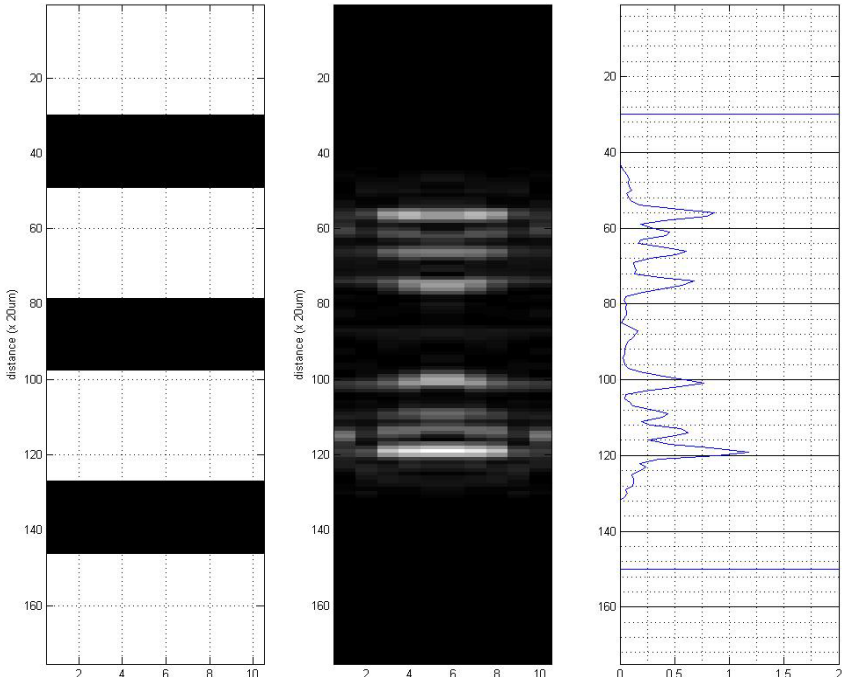
360µm/760µm Spacing, Full Bandwidth, Full Tilt, Low Resolution



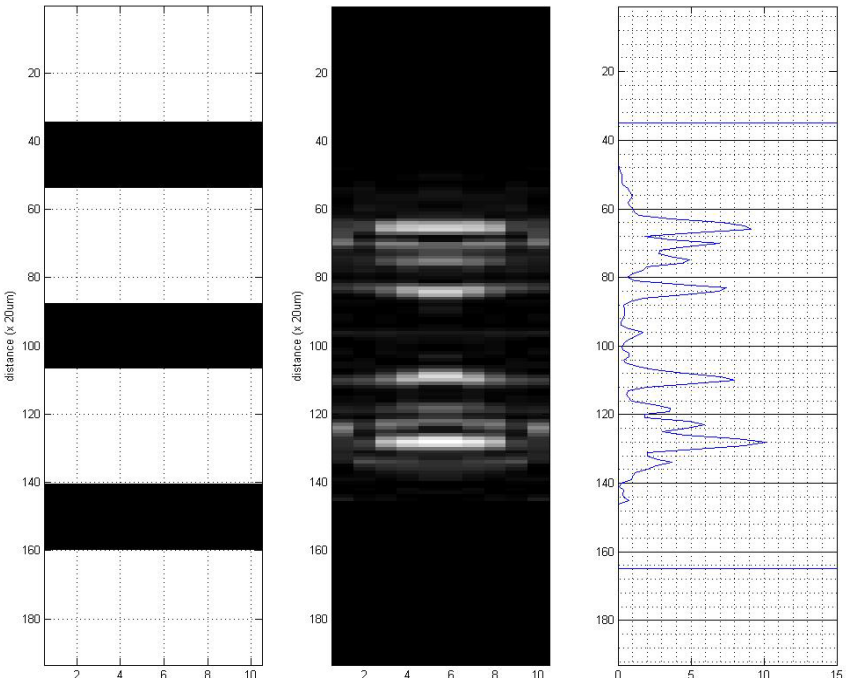
380µm/780µm Spacing, Full Bandwidth, Full Tilt, Low Resolution



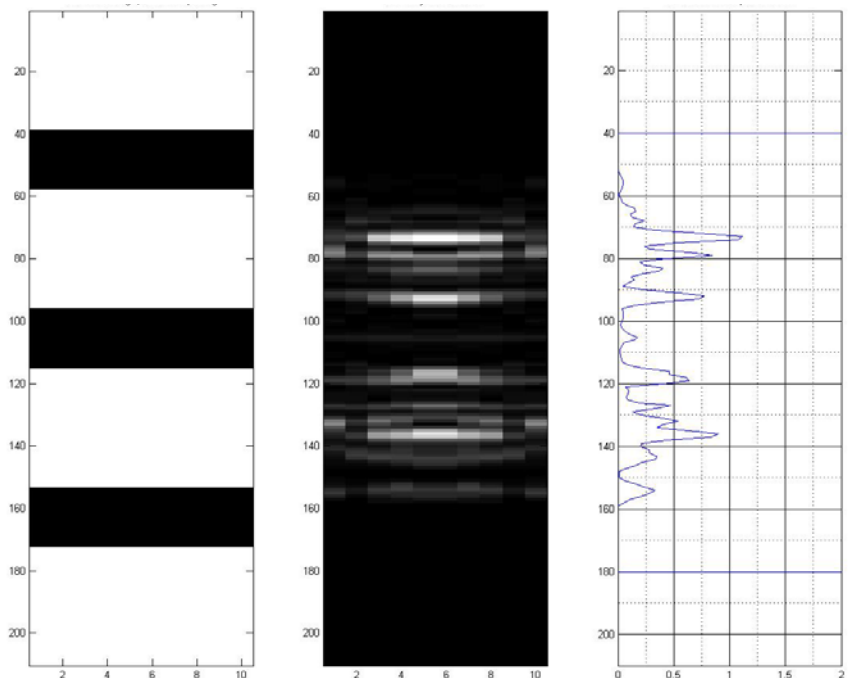
400µm/600µm Spacing, Full Bandwidth, Full Tilt, Low Resolution



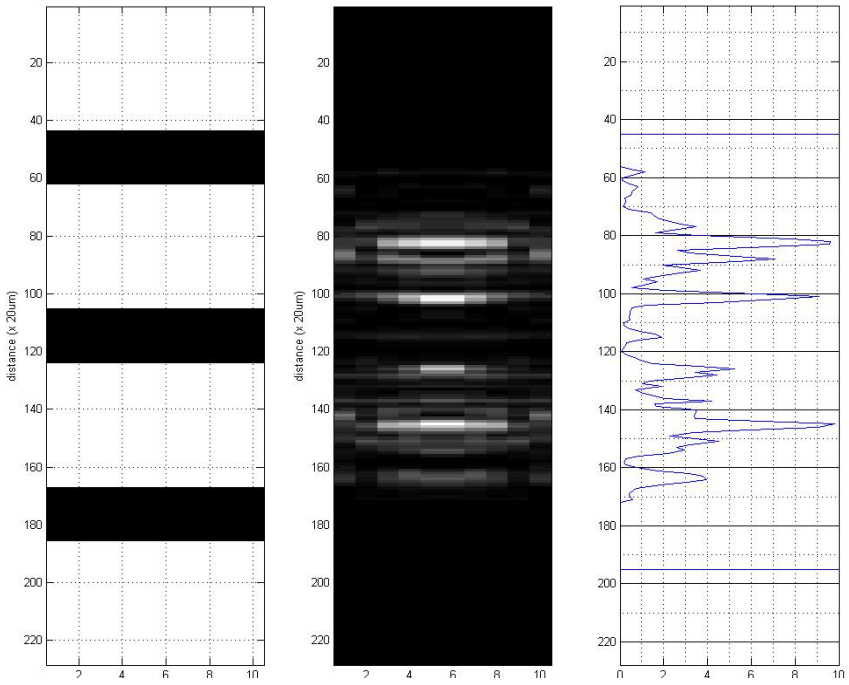
400µm/700µm Spacing, Full Bandwidth, Full Tilt, Low Resolution



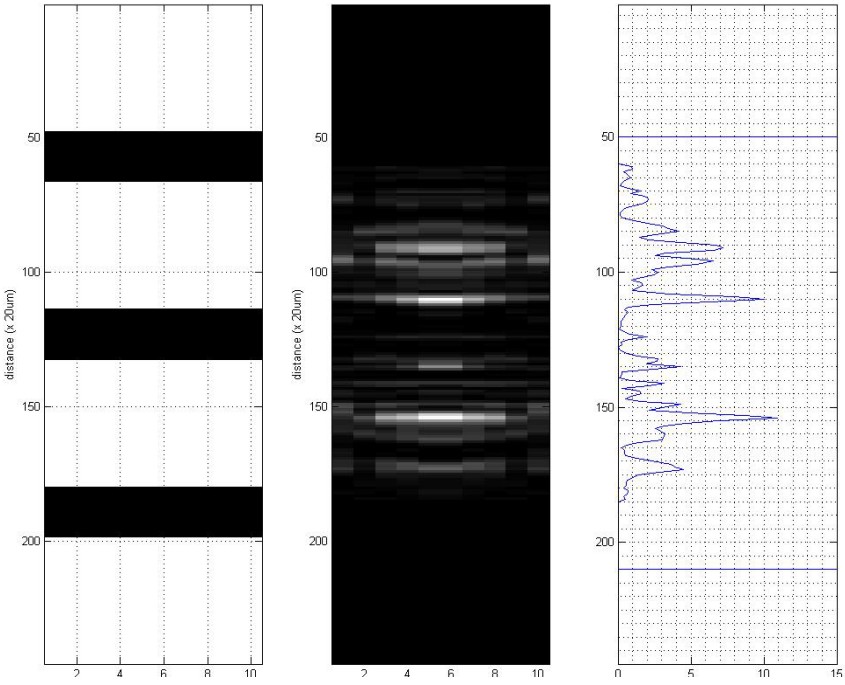
400µm/800µm Spacing, Full Bandwidth, Full Tilt, Low Resolution



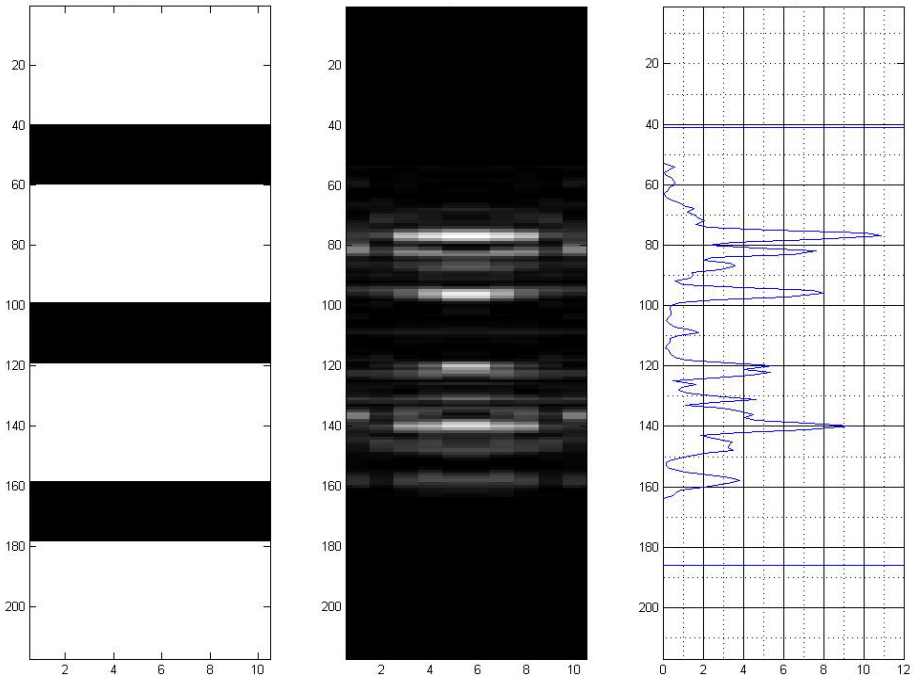
400µm/900µm Spacing, Full Bandwidth, Full Tilt, Low Resolution



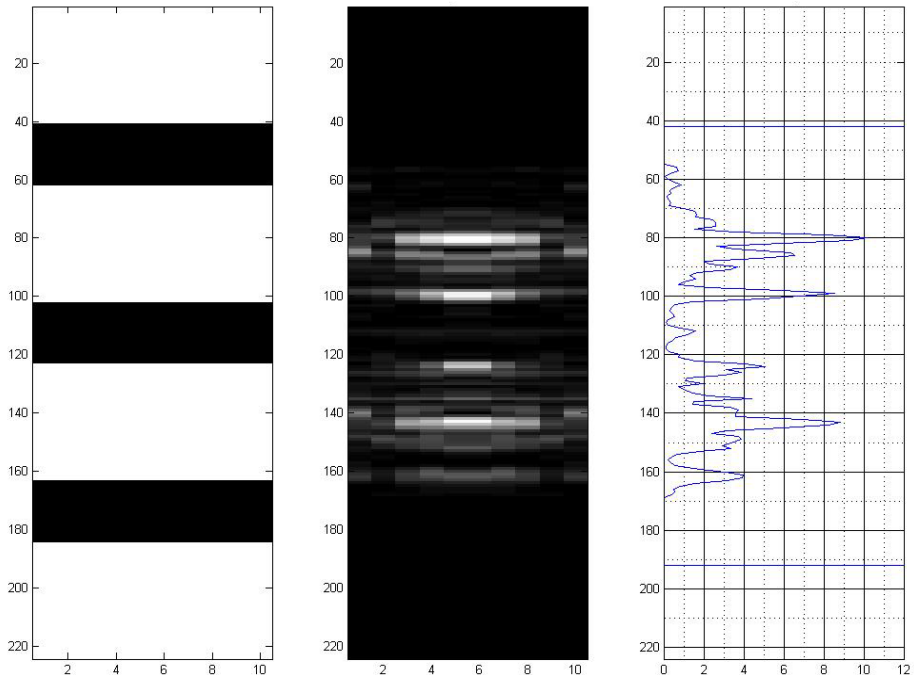
400µm/1000µm Spacing, Full Bandwidth, Full Tilt, Low Resolution



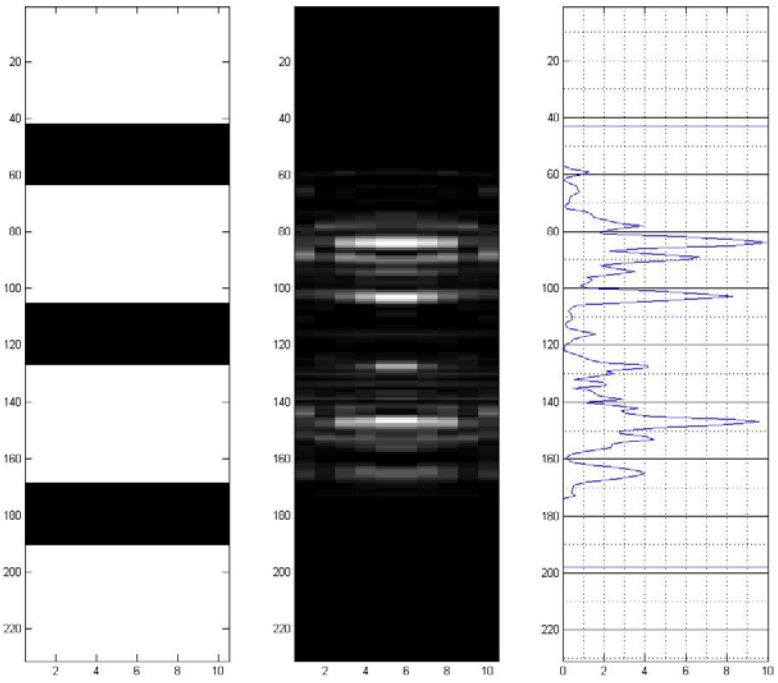
420μm/820μm Spacing, Full Bandwidth, Full Tilt, Low Resolution



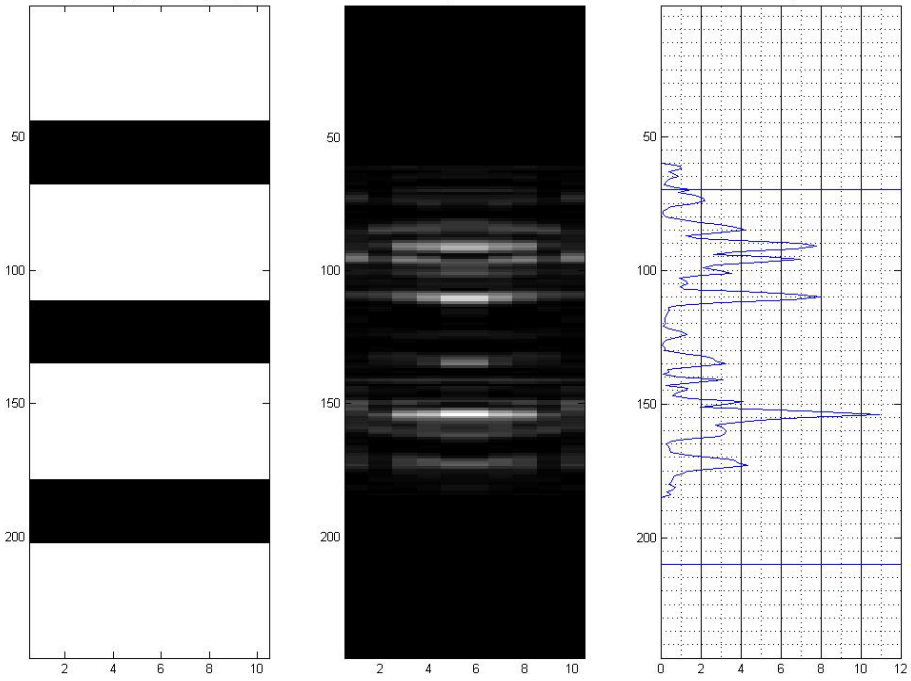
440μm/840μm Spacing, Full Bandwidth, Full Tilt, Low Resolution



460µm/860µm Spacing, Full Bandwidth, Full Tilt, Low Resolution



500µm/900µm Spacing, Full Bandwidth, Full Tilt, Low Resolution



Appendix C. AFIT Solar Cell Fabrication Process Follower

Step 1: **Wafer Preparation**		
	Center the wafer on the 2" spinner chuck and turn on the vacuum.	*Using the spinner in the solvent hood*
	Spin at 500 rpm and rinse in acetone, methanol, and DI water—each for 30 seconds. Dry with nitrogen while spinning.	*Methanol rinse prevents acetone from drying*
	Stop spinner, turn off vacuum, remove wafer, and dry with nitrogen on clean texwipe. Place on 110°C hot plate for 2 min.	*Hot plate helps with dehydration*
Step 2: **Diffusion**		
	Specify furnace time and temperature for front-side dopants.	*p-type wafers doped with phosphorous n-type wafers doped with boron nitride*
	Remove wafers doped with boron nitride for deglazing. Deglaze by submerging in BOE for 3 min. Dry with nitrogen on clean texwipe and place on 110°C hot plate for 2 min.	*Deglazing is required to remove surface impurities and avoid furnace contamination*
	Specify furnace time and temperature for rear-side dopants.	*Creates the back surface field*
	Deglaze the boron-doped wafers as outlined above.	
	Specify furnace time and temperature for rear-side dopants.	*Creates the enhanced back surface field*
Step 3: **Si_3N_4 Deposition** (if required)		
	Deglaze the wafers as outlined above.	*Removes any residual oxides*
	Give wafers to technician with thickness request in nanometers.	
Step 4: **Photoresist Application**		
	Deglaze the wafers only if they do not have Si_3N_4.	*BOE etches Si_3N_4*
	Put wafer on 2" wafer chuck front side up, turn on vacuum, and verify spinner settings. Time: 30 sec; Speed: 4,000 rpm	*Using the spinner in the solvent hood*
	Spray wafer with nitrogen to cool the wafer and remove any surface contaminants.	
	Apply S1818 positive photoresist onto the wafer (the amount should be about a 1.5" circle with no bubbles); start the spinner.	*Bubbles prevent uniform spreading*
	Once stopped, turn off the vacuum and place the wafer on the 110°C hot plate for 4 min.	*Hot plate sets the resist*
Step 5: **Photoresist Expose**		
	Clean the solar cell mask by rinsing in acetone, methanol, and DI water for 30 sec each and dry with nitrogen.	
	Install the mask into the contact aligner with the glass side touching the mask tray (the metal side will contact the wafer).	*Make sure the pattern is centered in the mask holder window*
	Place the wafer in the center of the contact aligner tray with the primary wafer flat down (6 o'clock position).	
	Slide the tray under the mask and raise it until contact is	*Visually verify there is contact*

	made. Verify the wafer is properly aligned to the mask; adjust as necessary.	
	Expose the wafer IAW posted exposure times for S1818 photoresist.	*Do not look at the light during exposure!*
	Once completed, lower the tray, slide it out, and use tweezers to gently remove the wafer and place in wafer case.	
Step 6: **Photoresist Develop**		
	Center the wafer on the 2" spinner chuck and turn on the vacuum.	*Using the spinner in the base hood*
	Spin at 500 rpm and rinse in 5:1 DI water/351 developer for 45 sec; immediately rinse with DI water for 30 sec and dry with nitrogen while spinning.	
	Stop spinner, turn off vacuum, remove wafer, and dry with nitrogen on clean texwipe.	
	Verify the resist was adequately developed using a microscope.	
Step 7a: **Deposition Prep – Wafers without Si_3N_4**		
	Place wafers in the O_2 Plasma Asher only if they do not have Si_3N_4.	
	Ash the wafers with patterned side up for 5 min at 75W making sure the reflected power is 0. Remove wafers and turn Asher off.	*Make sure to turn off the supply oxygen*
	Deglaze the wafers (if required) as a pre-metallization dip.	*Only if you haven't deglazed during Step 3 or Step 4 the same day.*
Step 7a: **Deposition Prep – Wafers with Si_3N_4**		
	Give wafers to technician for a Reactive Ion Etch to remove the Si_3N_4 exposed after photoresist development.	*Etched wafers do not require an a pre-metallization dip.*
Step 8: **Deposition and Lift-Off**		
	Notify the technicians of the requested metal deposition type and thickness in Angstroms; 500 Angstroms of Ti should be used as an adhesion layer.	*If only patterning one side, have the technicians flip the cell over and deposit the same metal on the rear of the wafer*
	Once the metal is finished, apply tape to the wafer and gently pull up, removing the metal.	
	If any metal is remaining, submerge in acetone and place in the ultrasonic bath for 5 min.	
	Rinse both sides of wafer with acetone, methanol, and DI water. Dry with nitrogen on clean texwipe.	
Step 9: **Post-Metal Processing**		
	If the other side of the wafer needs patterning, spin S1818 photoresist onto the patterned metal side for protection and then repeat the process beginning at Step 4.	*Make sure photoresist covers the patterned metal and exposed Si_3N_4 since the deglazing process in Step 4 will etch the nitride and attack the metal contacts.*
	Wafers are now ready for Rapid Thermal Anneal (RTA). Place wafers in RTA and run at 450°c for 20 sec.	

Appendix D. Source Wafer Data Sheets

Product Datasheet

PDS® Products N-Type Planar Diffusion Sources

N-Type diffusion source wafers for the semiconductor industry

PDS® Products phosphorus source wafers offer low cost, in-situ, N-type planar sources for silicon diffusions. In-situ PDS Products eliminate the trade-off between throughput and uniformity for larger diameter wafers.

All grades of N-type PDS Products are available in diameters up to 200 mm. Use of PDS Products enables the user to change source wafer diameter with little or no change in the diffusion process.

Available Grades and Typical Properties

N-type PDS Products are mechanically stable, solid diffusion source wafers that combine phosphorus and an inert silicon carbide substrate.

All N-type PDS Products consist of an active component Cerium Pentaphosphate (CeP_5O_{14}) or Silicon Pyrophosphate (SiP_2O_7) carried on an inert porous Silicon Carbide (SiC) substrate. At diffusion temperature, the active component decomposes to form P_2O_5 vapor, which evolves from the source by direct volatilization. The by-product of the decomposition (CeP_3O_9 or SiO_2) remains on the source wafer.

Grade	PH - 900	PH - 950	PH - 1000N	PH - 1025
Composition	100% CeP_5O_{14}	100% SiP_2O_7	100% SiP_2O_7	60% ZrP_2O_7 30%SiP_2O_7 10% SiO_2
Temperature °C	825 - 900	875 - 950	925 - 1000	975 - 1025
Sheet Resistance (Ohm/Sq)	150 - 15	60 - 5	25 - 3	25 - 3
Phosphorus Glass Thickness Å	100 - 650	125 - 1200	175 - 1200	100 - 1250
Dose atoms / cm^2	1.4×10^{14} to 3.9×10^{15}	3.2×10^{14} to 2.4×10^{15}	8.4×10^{14} to 1.1×10^{16}	5.3×10^{15} to 1.4×10^{16}

Stacking Arrangement

PDS Products sources and silicon wafers are edge-stacked perpendicular to the tube axis in cross-slotted furnace carriers.

Features / Benefits

- Extreme flexibility that allows application to many device structures, thereby eliminating capital expense in device conversion.
- Improved yields by gettering oxidation induced stacking faults and improved uniformity across the wafer, across a run and from run-to-run.
- Precision chemical principles make for predictability and repeatability through the controlled introduction of moisture in the diffusion tube, even at temperatures as low as 825°C.
- A trained staff is maintained to assist in all technical needs and support.

Key Applications

- Emitter
- Collector
- Backside gettering
- Enhancement
- Source/drain
- Sinker
- Polysilicon doping
- Solar cell

Target Markets

- Semiconductor manufacturing
- Microelectro-mechanical systems (MEMS)

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Gases and Flow Rates

During the evaluation phase of PDS Products, a full boatload of dummy silicon wafers is needed to create the boundary layer condition and achieve meaningful results. Typical total gas flow rates are 6 – 10 slpm, depending on the combination of source wafer and process tube diameters used. Optimization of across the wafer and across the boat diffusion parameter uniformity may require that these flow rates be modified.

Source Preparation

Wet chemical cleaning is unnecessary since the sources are manufactured under the most exacting quality standards using raw materials of the highest purity, and are protected from exposure to contaminants both during and after manufacture. Furthermore, due to the porosity of the composition, cleaning agents are difficult to remove completely.

It is recommended that prior to actual product silicon diffusion, new phosphorus source wafers be annealed at the following temperatures in an ambient of 100% N_2:

PH-900:	925°C	for 16 Hrs
PH-950:	900°- 950 °C	for 8 Hrs
PH-1000N:	950°-1000°C	for 8 Hrs
PH-1025:	1000°-1025 °C	for 4 Hrs

Diffusion Process Outline

Step	Ambient	Time	Function
Push in & Recovery	N_2 (100%)	15 Min.	Thermal Equilibrium
Soak	N_2 (100%)	Variable	Resistivity Target
Deglaze	10:1 HF	2 Min	Remove Unreduced Glass

1. **Push in and Recovery**
   During the recovery step, source boats stacked with Phosphorus and silicon wafers are pushed into a diffusion tube. The tube is then allowed to establish ambient equilibrium. This step is performed in an ambient of 100% N_2 at 750°C-850°C. Typical total gas flow rates are 6–10 slpm, depending on the combination of source wafer and process tube diameters used.
2. **Soak**
   During the soak step, the dopant, glass which is uniformly coating the silicon wafers undergoes a reduction reaction in the ambient which results in the formation SiO_2 and phosphorus
3. **Deglaze**
   After the Si wafers are unloaded from the furnace, the excess un-reacted dopant glass is removed by 10 parts DiH_2O to 1 Part HF for 2 minutes at room temperature.

Storage

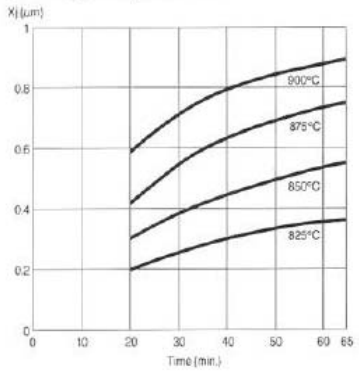
Optimum source wafer storage between uses is in dry N_2 at 400°C. Storage in the mouth of the diffusion tube is not recommended.

Furnace Loading and Unloading Cycles

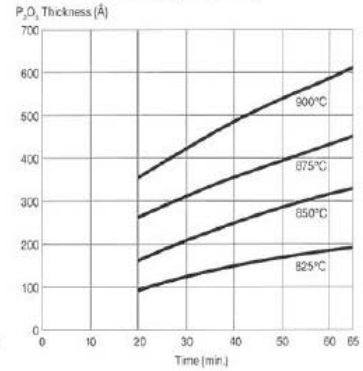
A slow push during furnace loading (typically 5.0"/ min.) at 700°- 800°C is advised. The boats should be allowed to equilibrate for 5-10 min. under N_2 before ramping to use temperature. A subsequent ramp down to 700°- 800°C before unloading is also recommended.

Performance data: PDS Products N-type Grade PH-900

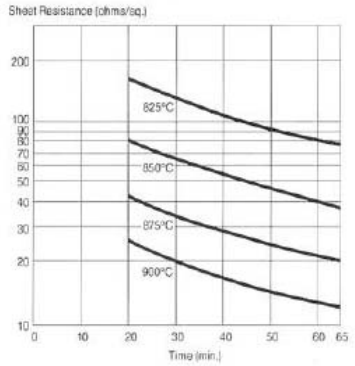
Junction Depth vs. Deposition Time



P_2O_5 Glass Thickness vs. Deposition Time

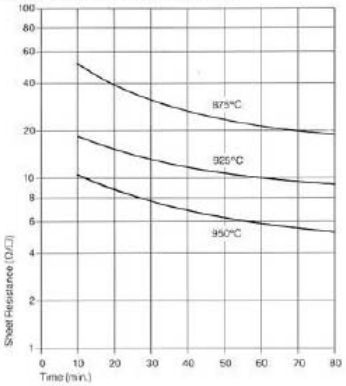


Sheet Resistance vs. Deposition Time

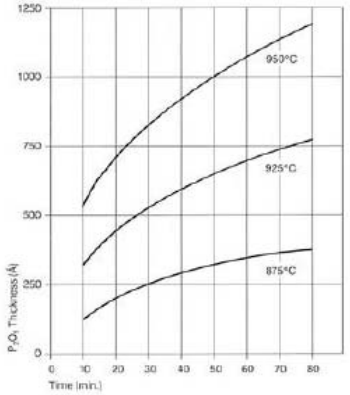


Performance data: PDS Products N-type Grade PH-950

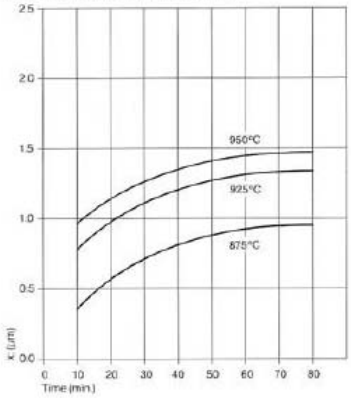
Sheet Resistance vs. Deposition Time



P_2O_5 Glass Thickness vs. Deposition Time

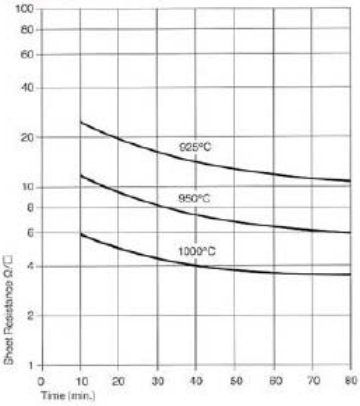


Junction Depth vs. Deposition Time

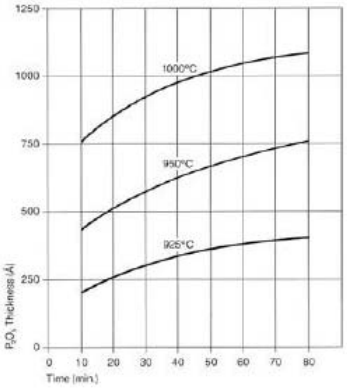


Performance data PDS Products N-type Grade PH-1000N

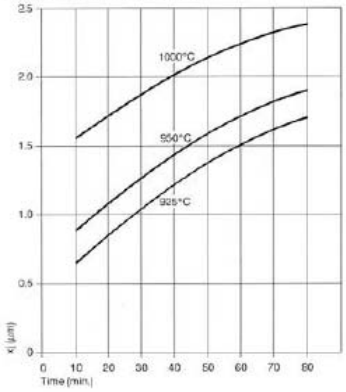
Sheet Resistance vs. Deposition Time



P_2O_5 Glass Thickness vs. Deposition Time



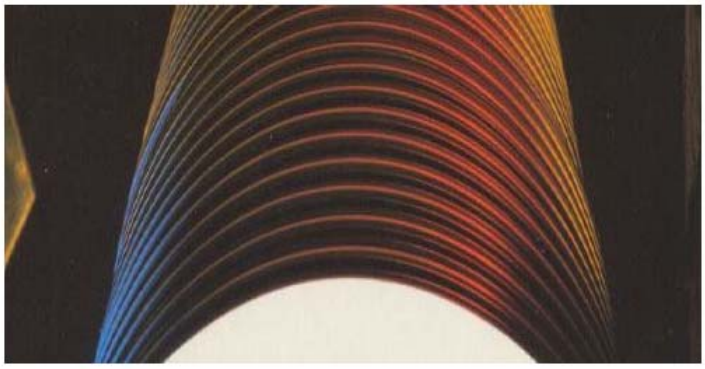
Junction Depth vs. Deposition Time



Product Datasheet

PDS® Products P-Type Planar Diffusion Sources

PDS® Products P-Type diffusion sources for the semiconductor industry



PDS® Products P-type (Boron Nitride) wafers offer low cost, in-situ, P-type planar sources for silicon diffusions. PDS Products P-type sources eliminate the trade-off between throughput and uniformity for larger diameter wafers.

All grades of P-type PDS Products are available in diameters up to 200 mm. Use of PDS Products enables the user to change source wafer diameter with little or no change in the diffusion process. Furthermore, Saint-Gobain Advanced Ceramics Boron Nitride offers unparalleled technical guidance based on over 30 years of experience in diffusion technology.

Available Grades and Typical Properties

P-type PDS Products are hot-pressed sintered Hexagonal Boron Nitride (hBN) materials, where varying amounts of Boric Acid and SiO_2, mixed with hBN control the diffusion performance.

Grade BN-HT is made by firing hBN at high temperatures to remove all the B_2O_3 and grow diffusion bonds. When activated, B_2O_3 glass forms on the outside of the BN-HT source wafer. This boron glass, controlled transferred to the silicon wafer, results in uniform boron doping while minimizing silicon surface defects.

Grade	BN-975	BN-1050	BN-1100	BN-1250	BN-HT
Composition	3.5-6.5% B_2O_3	2% B_2O_3	40% SiO_2	60% SiO_2	0.2% B_2O_3
Temperature °C	800 - 975	975-1100	1000 - 1100	1000 - 1250	1000 - 1200
Sheet Resistance (Ohm/Sq)	2000 - 20	20 - 5	40 - 5	40 - 1.5	20 - 1
Boron Glass Thickness Å	300 - 2000	400 - 1000	200 - 800	200 - 1000	200 - 1000
Dose atoms / cm^2	1.3×10^{14} to 3.6×10^{15}	3.6×10^{15} to 1.6×10^{16}	2.3×10^{15} to 1.6×10^{16}	2.3×10^{15} to 9.0×10^{16}	2.3×10^{15} to 4.9×10^{16}

Stacking Arrangement

PDS Products sources and silicon wafers are edge-stacked perpendicular to the tube axis in cross-slotted furnace carriers.

Features / Benefits

- Extreme flexibility that allow application to many device structures, thereby eliminating capital expense in device conversion
- Improved yields by gettering oxidation induced stacking faults and improved uniformity across the wafer, across a run and from run-to-run
- Precision chemical principles make for predictability and repeatability through the controlled introduction of moisture in the diffusion tube, even at temperatures as low as 750°C
- Moisture modulation of the vapor pressure of the B_2O_3- HBO_2 system causes a rapid flux of gas, creating excellent uniformity and allowing a damage control mechanism to be established simultaneous to the deposition process
- Successful application of the PDS® Products hydrogen injection process throughout the semiconductor industry

Key Applications

- Emitter
- Base
- Collector
- Channel stop
- Isolation
- Guard rings
- Resistor
- Capacitor
- Solar cells
- Source/drain
- Trench structures

Target Markets

- Semiconductor manufacturing
- Microelectro-mechanical systems (MEMS)

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Gases and Flow Rates

When evaluating PDS Products, a full boatload of test and dummy silicon wafers is needed to create the boundary layer condition and achieve meaningful results. Typical total flow rates are 6 – 10 slpm, depending on the combination of source wafer and process tube diameters used. Optimization of across the wafer and across the boat diffusion parameter uniformity may require that these flow rates be modified.

Source Preparation

It is necessary that prior to silicon deposition, new source wafers have the recommended preparation. Wet cleaning of BN-975 and BN-HT is to be avoided.

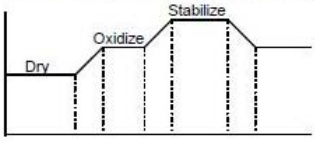
Since BN-1100 and BN-1250 are BN / SiO_2 compositions, it is necessary to remove some of the SiO_2 with an HF dip followed by a DI-H_2O rinse. This etches some of the SiO_2 away to expose the boron nitride for oxidation. After the surface etch step, a water rinse is to be done to remove any residual HF. Routine re-oxidation may be necessary as the exposed BN is consumed.

For all sources, the function of the drying step is to remove entrapped moisture. The purpose of the initial oxidation process is to grow a thin layer of B_2O_3 glass on the surface of the boron nitride wafer. This will act as the dopant source during subsequent deposition (predisposition) processes.

Source wafer preparation process steps

	BN-975	BN-1100 & BN-1250	BN-HT
Surface Etch	No	3 Parts Di-H_2O-2 Parts 49% HF @ Room Temp.	No
Rinse	No	Di-H_2O 5 min. Max.	No
Dry	400°C 100%N_2 1 Hour	400°C 100%N_2 2 Hours	400°C 100%N_2 1 Hour
Oxidize	900- 950°C 100% O_2 30 Minutes	1000°C 100% O_2 30 Minutes	950°C 100% O_2 30 Minutes
Stabilize	At Use Temp 100% N_2 30 Minutes	1100-1250°C 100% N_2 30 Minutes	1100°C 100% N_2 6 Hours

Source Wafer Preparation Process Line Diagram



Process Outline for Single Step Diffusion

1. **Push in and Recovery:** During the recovery step, source boats stacked with BN-975 wafers and silicon wafers are pushed into a diffusion tube. The tube is then allowed to establish ambient equilibrium. This step is generally performed in an ambient of 50% N2 and 50% O2 at 750°C-850°C. Typical total gas flow rates are 6–10 slpm, depending on the combination of source wafer and process tube diameters used. The N2/O2 ambient during the recovery step grows a thin layer of SiO2 in the mask window regions. This thin layer of SiO2 masks B2O3 diffusion during the push in cycle, thus minimizing or eliminating the sheet resistivity gradients due to the first wafer in being the last wafer out.

2. **Soak:** During the soak step, the dopant glass which is uniformly coating the silicon wafers undergoes a reduction reaction in the ambient which results in the formation of a thin insoluble layer of silicon-boride, Si-B, at the silicon surface. The Si-B layer traps crystal damage at the silicon/ SiB interface through a strong gettering action. In essence, the function of the soak step is to control damage while obtaining the targeted sheet resistivity (See performance charts on the next page).

Single step diffusion process outline

Step	Ambient	Time	Function
Push in & Recovery	N_2 (100%)	15 Min.	Thermal Equilibrium Thin Oxide Growth
Soak	N_2 (100%)	Variable	Defect Control Resistivity Target
Deglaze	10:1 HF	2 Min	Remove Unreduced Glass
Low Temperature Oxidation (LTO)	100% O_2	20 Min.	Remove Si-B Layer and defects.

3. **Deglaze:** After the Si wafers are unloaded from the furnace, the excess un-reacted dopant glass is removed by 10 parts DiH2O to 1 Part HF for 2 minutes at room temperature.

4. **Low Temperature Oxidation (LTO):** The function of the LTO step is to oxidize the Si-B layer and a thin layer of Si below it. Oxidizing this thin Si layer will immobilize most of the crystal defects in the oxide. A steam or O2 ambient is typically used to cause the rapid oxidation of the Si-B layer and it's silicon interface region before harmful propagation of the defects into the silicon can occur. This allows the subsequent drive cycle to be damage free. (See separate Low Temperature Oxidation Technical Bulletin on our website at www.bn.saint-gobain.com)

Appendix E. Fabrication Equipment, Test Equipment, and Chemicals

Model	Description	Application	Step
Solitec	Spinner	Spinning wafers at various speeds to clean or apply photoresist.	Fabrication
$(CH_3)_2CO$	Acetone	Cleaning wafers; etches photoresist	Fabrication
CH_3OH	Methanol	Cleaning wafers	Fabrication
HP131725Q	Hot Plate	Heating wafers for dehydration after cleaning and for baking photoresist	Fabrication
H4-7760	Diffusion Furnace	Doping wafers and growing oxides	Fabrication
HF+O	Buffered Oxide	Oxide removal (deglazing)	Fabrication
KOH	Potassium Hydroxide	Isotropic etching for silicon wafers	Fabrication
Orion III	Vapor Deposition	Deposits silicon nitride (ARC)	Fabrication
μPG101	Mask Writer	Creates masks for photolithography	Fabrication
1818	Positive Photoresist	Masking for photolithography	Fabrication
MJB-3	Contact Mask Aligner	Exposing photoresist	Fabrication
351	Photoresist Developer	Removing exposed photoresist	Fabrication
SP-100	Plasma Asher	Pre-metallization wafer cleaning	Fabrication
Phantom III	Reactive Ion Etcher	Etching silicon nitride	Fabrication
EB-4P-6KW	Metal Evaporator	Depositing metal contacts	Fabrication
3200	Ultrasonic Bath	Removing metal remaining from metal lift off procedures	Fabrication
Solaris 150	Annealing Furnace	Rapid thermal annealing	Fabrication
XPS-300	Solar Light Tester	Measuring solar cell response	Testing
PMA2100	Pyranometer	Measuring irradiance	Testing
34401A	Digital Multimeter	Measuring current and voltage	Testing
189	Thermal Multimeter	Measuring internal and ambient temperature using thermocouple probes	Testing
SC6703	Infrared Camera	Recording heat dissipation, near-IR	Testing
SC600	Infrared Camera	Recording heat dissipation, mid-IR	Testing

Appendix F. Electromagnetic Radiation and Spectral Signature

Electromagnetic radiation is energy that propagates through space in the form of electromagnetic waves. Although each wave travels at the speed of light (2.99 x10^8 m/s), they vary in length which creates different effects. For example, a wavelength of 500nm corresponds to green light whereas lengths of 5nm (x-rays) and 5,000,000nm (radio waves) are invisible to the human eye. In fact, everything above a temperature of absolute zero (-273°C) emits electromagnetic radiation. The signature of radiation varies depending on the wavelength and temperature, which was first observed by Max Planck in 1900 as he investigated how to develop a more efficient light bulb [79]. He discovered that the intensity of radiation over a given area, the *irradiance* (I_{rr}), is given by

$$I_{rr} = \frac{2hc^2}{\lambda^5 (e^{hc/\lambda kT} - 1)} \qquad \text{(F-1)}$$

Where:

h = Planck's constant; 6.626x10^{-34} m^2kg/s
c = The speed of light in a vacuum; 3.0x10^8 m/s
λ = Wavelength
T = Temperature

To demonstrate this, Planck used the concept of an ideal physical body that appears black at room temperature, known as a *blackbody*. An example of a blackbody is an electric stove that glows when it gets hot. A graph of blackbody radiation in accordance with Equation F-1 is shown below and identifies how intensities at each wavelength change with temperature. A warm stove has a peak irradiance above 800nm, which is invisible radiation experienced as infrared heat. As it heats up, the intensity peak shifts towards 590nm and yellow-orange light is emitted.

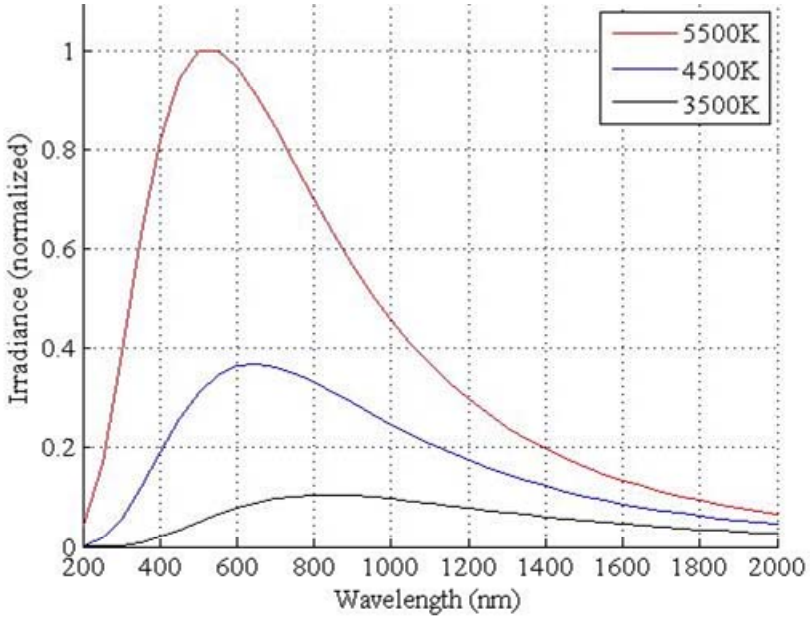


Figure 43. Blackbody radiation at different temperatures.

A stove may simulate a blackbody, but there is no true physical body that is an ideal emitter. For instance, in outer space where the air mass is zero (AM0), the sun has a spectrum that resembles a blackbody at 5800K. The corresponding irradiance, which is a summation of intensities at each wavelength, is 1367 w/m^2. Once the radiation enters the atmosphere (AM1.5), the intensities are reduced via reflection or diffusion. The resulting amount of irradiance on the surface of the Earth, known as *1 sun*, is measured to be 1000 W/m^2 and is used as a standard test condition for solar cells.

Another and equally important test condition is the spectrum, or "fingerprint", of radiation at AM1.5. The spectrum identifies the intensity of each photon that reaches earth. For example, Figure 44 shows that there are more 1400nm photons hitting the atmosphere (AM0) than reaches sea level (AM1.5). The atmosphere changes the spectrum through diffusion and absorption. Since every photon has a specific energy associated with it, the spectral fingerprint plays an important role in the photovoltaic

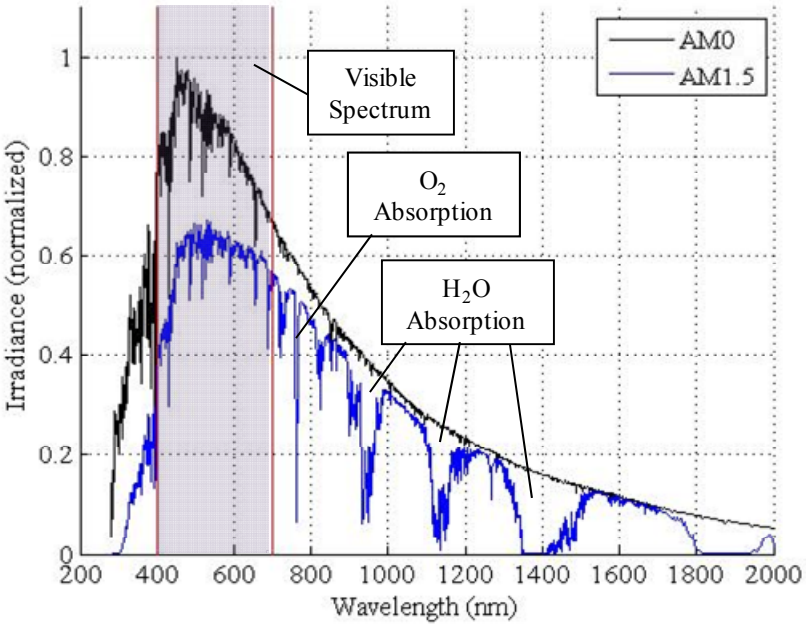


Figure 44. Solar spectrum based on ASTM G173-03 data.

process. Figure 44 also shows that the sun generates an abundance of photons with energies ranging from 3.10eV (400nm) to 0.93eV (1333nm) and since silicon's band gap energy is 1.11eV, it only responds to radiation with wavelengths below 1100nm. Thus, the applicable region for the photovoltaic effect is from 400 to1100nm (Figure 45).

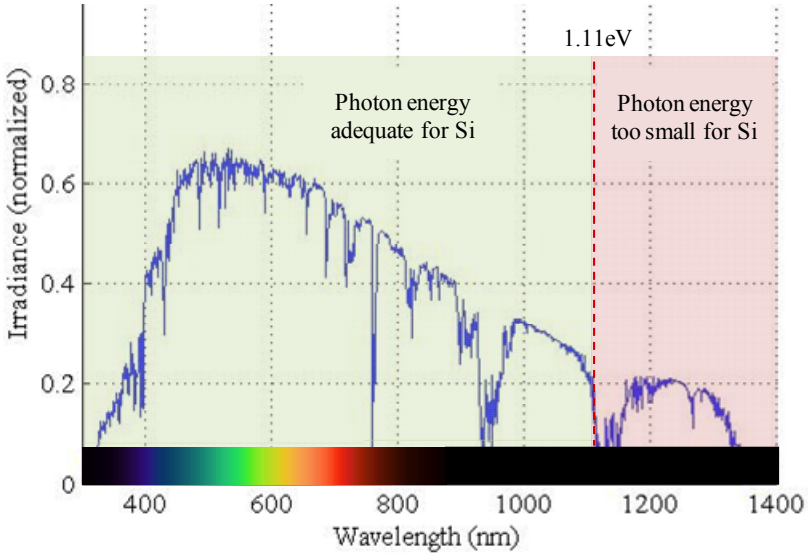


Figure 45. Photovoltaic response spectrum for silicon.

Appendix G. Glossary

Anode
The electrode at which current enters an electrical device.

Anti-reflection coatings (ARC)
A thin layer of material designed to increase the absorption of light by using destructive interference to reduce reflection.

Atomic layer deposition (ALD)
A thin-film deposition method that deposits one atomic layer at a time.

Back surface field (BSF)
A secondary depleted region at the rear of a solar cell created by a heavy-doped homojunction that prevents recombination by redirecting electrons toward the primary depleted region.

Band gap
The energy difference between the valence and conduction band of an atom.

Band gap energy
The amount of energy required for an electron to move from the valence band to the conduction band.

Blackbody
An ideal physical body that absorbs all incident radiation.

Bulk micromachining
A MEMS fabrication process that consists of etching into a substrate to create devices.

Cathode
The electrode at which current leaves an electrical device.

Characteristic (IV) curve
A graph showing the relationship of the current and voltage delivered by a solar cell.

Chemical vapor deposition (CVD)
A chemical deposition process typically used to produce high-purity materials and thin films.

Coherent (light)

A condition where two waves have a fixed phase difference and the same frequency.

Conduction (thermal)

The transfer of thermal energy via microscopic diffusion and particle collisions.

Conduction band

The region outside the orbit of an atom where electrons can move freely throughout the atomic lattice of a material.

Conductor electrons

Electrons which are located in the conduction band.

Conductors

A material that allows the flow of electrical current.

Constructive interference

The resulting interaction between two coherent waves which produces a single amplitude equal to the sum of the individual waves.

Convection

The transfer of thermal energy due to the buoyancy of fluids at different temperatures.

Current crowding

Non-uniform current distribution in a conductor usually induced by sharp bends or turns in the conduction path.

Current matching

A design consideration that seeks to avoid the reduction in overall current resulting from dissimilar current sources connected in series.

Dark current

Residual current flowing in a solar cell that is not under illumination.

Deglazing

The process of removing a material's oxide layer, often to remove surface defects caused during diffusion.

Depleted region

An insulating region in a semiconductor material created by different doping concentrations.

Destructive interference

The interaction between two coherent waves where the peak of one wave meets the valley of the other resulting in cancellation.

Detailed balance technique

A technique used to calculate the maximum efficiency of photovoltaic devices.

Diffraction pattern

The tendency of a wave emitted from a source or opening to spread.

Diffuse

The reflection of light from a surface in many angles instead of only one.

Diffusion

The movement of a molecule from a region of high concentration into a region with low concentration.

Doping

The process of replacing atoms in a semiconductor lattice with different (dopant) atoms.

Double drift region diode

A semiconductor p-n junction with heavy-doped homojunction depleted regions on both sides.

Efficiency

The ratio of power delivered by a solar cell to the power of the incident irradiance.

Electrical losses

A reduction in the amount of power delivered by a solar cell due to the behavior of electrons.

Electromagnetic radiation

Radiant energy travelling as waves in which the electric and magnetic fields vary simultaneously.

Electron-hole pairs

The result of excess electrons combining with excess holes forming the depleted region.

Enhanced back-surface field (EBSF)

A heavy-doped homojunction at the rear of a back surface field.

Evaporation
Metal deposition via the condensation of vapor particles on a substrate.

Extrinsically doped
An artificially doped semiconductor material with impurities added during wafer formation.

Fill factor (FF)
The ratio of a solar cell's ideal power to its actual power.

Fingers and bus
A typical solar cell front contact grid design consisting of a network of thin contacts (fingers) connected by a common, thicker contact (bus).

Fourier transform
The decomposition of a signal into its individual frequencies.

Fresnel approximation formula
A diffraction approximation formula applied to the propagation of waves in the near-field.

Heterojunctions
The interface between two different semiconductor materials.

Homojunction
The interface between layers of similar semiconductor materials which have the same band gap but different doping concentrations.

Insulator
A material with a high band gap that does not readily conduct electricity.

Interference pattern
The combined result of the interaction between two coherent waves.

Irradiance
A measure of radiant energy per unit area.

Junction depth (x_j)
The depth from the surface at which the impurity concentration reaches zero.

Lithographie, Galvanoformung, Abformung (LIGA)
A high-aspect-ratio fabrication process consisting of lithography, electroplating, and molding.

Low temperature oxidation (LTO)

The process of introducing oxygen into a furnace at low relative temperatures to grow an oxide on the surface of the substrate.

Maximum power point

The point along the characteristic curve at which the maximum power is delivered by a solar cell.

Microelectromechanical Systems (MEMS)

The technology and fabrication of electro-mechanical devices that contain features as small as 1μm in size.

n-type

A semiconductor material with excess electrons.

Negative photoresist

A light-sensitive material that becomes less soluble when exposed to UV radiation through the formation of stronger chemical bonds.

Ohmic contact

A metal-semiconductor interface that provides an electrical junction with a linear current-voltage relationship described by Ohm's Law.

Optical losses

A reduction in the amount of power delivered by a solar cell due to the behavior of photons.

p-n junction

The interface between an n-type semiconductor and a p-type sesmiconductor which forms a depleted region.

p-type

A semiconductor material with excess holes.

Photocurrent

The electric current created by photoelectric effect.

Photodiodes

A diode that responds to light by changing resistance or producing an electric potential.

Photoelectric effect

The interaction of light with a material typically causing it to emit electrons.

Photolithography
A microfabrication process that uses light to transfer a pattern through a photomask onto photoresist.

Photoresist
A light sensitive material used in photolithography.

Photovoltaic effect
The result of using a p-n junction to prevent the recombination of electrons freed during the photoelectric effect.

Physical deposition
Deposition processes that use the physical transfer of material onto a substrate.

Positive photoresist
A light-sensitive material that becomes more soluble when exposed to UV radiation through the reduction of chemical bonds.

Rapid thermal annealing
The quick heating and cooling of a metal-semiconductor interface to provide a good ohmic contact.

Rayleigh-Sommerfeld diffraction formula
A diffraction formula used to mathematically represent the wave-nature of propagating light.

Recombination
The process where a free electron combines with an excess hole to create an electron-hole pair.

Reflection
The redirection of light in a singular path from a smooth surface.

Refraction
The change in direction of light as it passes through the interface between two mediums.

Refractive index
The ratio of the speed of light to its velocity through a given medium.

Resistivity
A measure of how much a material resists the flow of electric current.

Schockley-Queisser (S-Q) limit
A theoretical solar cell efficiency limit of 30% based on the detailed balance method.

Screen printing
A technique used for commercial solar cell fabrication using a metal paste applied through a screen for contact formation.

Semiconductor
A material with a conductivity between metals and insulators that can conduct electricity through the inclusion of dopant atoms.

Specular
A smooth, flat mirror-like surface.

Sputtering
A metal deposition technique using a ballistic exchange of momentum to bombard a substrate with source atoms.

Standard test conditions
The industry standard condition for testing solar cells; $1kW/m^2$ and 25°C.

Surface micromachining
An additive MEMS fabrication process via depositing and etching thin layers on a substrate.

Thermal losses
A reduction in the amount of power delivered by a solar cell due to an increase in its temperature.

Thermal radiation
The heat created by infrared electromagnetic radiation.

Transmission
The propagation of electromagnetic radiation through a material.

Valence band
The highest range of electron energy in orbit around an atom.

Valence electrons
Electrons that are in the outermost shell or orbit of an atom.

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Vita

Lt LaFleur began his military career in 1997 when he enlisted in the U.S. Army after graduating high school. He served four years as a light-wheel vehicle mechanic before matriculating to Southern Illinois University where he obtained a Bachelor of Science degree in Electrical Engineering in 2005. He spent the following 5 years in the building design industry where he achieved designations as an Engineer in Training (EIT) and Lighting Certified (LC) professional. In 2011, Lt LaFleur resumed active military duty by earning a commission from the U.S. Air Force's Officer Training School (OTS) at Maxwell AFB, AL. His first assignment was with the National Air and Space Intelligence Center (NASIC) at Wright-Patterson AFB, OH where he had the opportunity to deploy to Afghanistan in support of Operation Enduring Freedom (OEF). He was then accepted to pursue a Master of Science degree in Electrical Engineering at the Air Force Institute of Technology (AFIT). Lt LaFleur's decorations include the Air Force Commendation Medal, Army Achievement Medal, Meritorious Unit Award, Good Conduct Medal, National Defense Service Medal, Afghanistan Campaign Medal, Global War on Terrorism Medal, Air & Space Campaign Medal, Air Force Expeditionary Service Ribbon, Air Force Longevity Service Ribbon, Army NCO Professional Development Ribbon, Small Arms Marksmanship Ribbon, Air Force Training Ribbon, Army Service Ribbon, and the International Security Assistance Force NATO Medal.

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14. ABSTRACT

Although existing technology can produce highly efficient solar cells, they remain commercially cost-prohibitive. A low-cost alternative was investigated in this research by developing a novel hybrid multi-junction silicon (HMJ-Si) solar cell architecture through modeling, fabrication, and testing. The architecture consists of stacked silicon solar cells with an air gap between them and was designed with metal grating contacts that exploit interference patterns for light management. The interference patterns were examined in MATLAB® and verified using Lumerical® FDTD Solutions. Development focused on wafer configuration; diffusion profile; front contact design; optical, electrical, and thermal loss reduction; and efficiency. The architecture was optimized using an unpolished-front, p-type top cell with 128nm of Si3N4, a butterfly front contact, and 400μm grating spaced 900μm apart; a polished-front, n-type bottom cell with 200μm grating spaced 1100μm apart; and both cells having an enhanced back surface field diffusion profile with 500nm silver contacts. Efficiency peaked at 8.42% using a silver-coated wafer in lieu of the bottom cell. The results indicate that the architecture is a viable solar cell design requiring additional research for optimization.

15. SUBJECT TERMS

efficiency, grating, interference patterns, light trapping, multi-junction, photovoltaic, solar cells.

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