A coding and On-Line Transmitting System

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A distributed data acquisition system is proposed. It provides parallel and simultaneous coding and on-line transmission of signals. This system has higher accuracy of measurements and performance in sampling and transmission than known analogs.

1 Introduction

Processes may be of different nature: for instance, we may be interested in brain biopotentials, heart work or IC features. To obtain a full picture it is necessary to process tens and hundreds of thousands of measurements. A special data acquisition system is needed for analog-to-digital conversion (ADC). Our system is a distributed system where transmitter and receiver are separated by up to one hundred metres. Such systems are described, for example, in [1], [2], [3]. In particular, the proposed system seems to have the following advantages over the system described in [1]:

- it can simultaneously process 64 channels which increases the precision of the measurements precision from point of view of discretization, and the member of channels may be increased;
- the performance is superior to parallel work;
- comparing this system with [1] we can see that it has simpler construction, which makes the system cheaper and more tolerant. Biological research has a high demand for tolerant;
- it has high accuracy and noise immunity.

2 System description

The system consists of a transmitter, a receiver, and a communication line.

The transmitter (see Fig. 1) has 64 identical voltage to time interval converters. The control logic simultaneously enters the control pulse SAMPLE into all 64 input channels, which fixes value obtained from sensors. After selecting the first channel by analog multiplexes, a dual slope conversion process takes place and the comparator output has the time interval T_1. The dual slope converter is therefore a Voltage--to-Time converter (V/T).

The V/T converter offers some advantages. The conversion accuracy is independent of the clock period and integrating capacitance. The theoretical accuracy depends only on the absolute value of the reference and clock stability. Even changes in other components, such as the comparator input offset voltage, have no effect, provided that are not changed during conversion.

The digital circuits substitute time interval T_1 by two short pulses, called START and STOP, which define the starting and finishing moments of time interval T_1. Time interval T_1 is delayed by 40 ns in order to obtain a blank between the 64 time intervals passing sequentially through the cable. The serial set of START and STOP signals is fed to the control circuits of the laser allowed for the transmission of very short infra-red light pulses of 20 ns. The format of the transmitted information is shown in Fig. 2.

The system usually uses a cable up to 200 m in length which is possible owing to the low noise level.

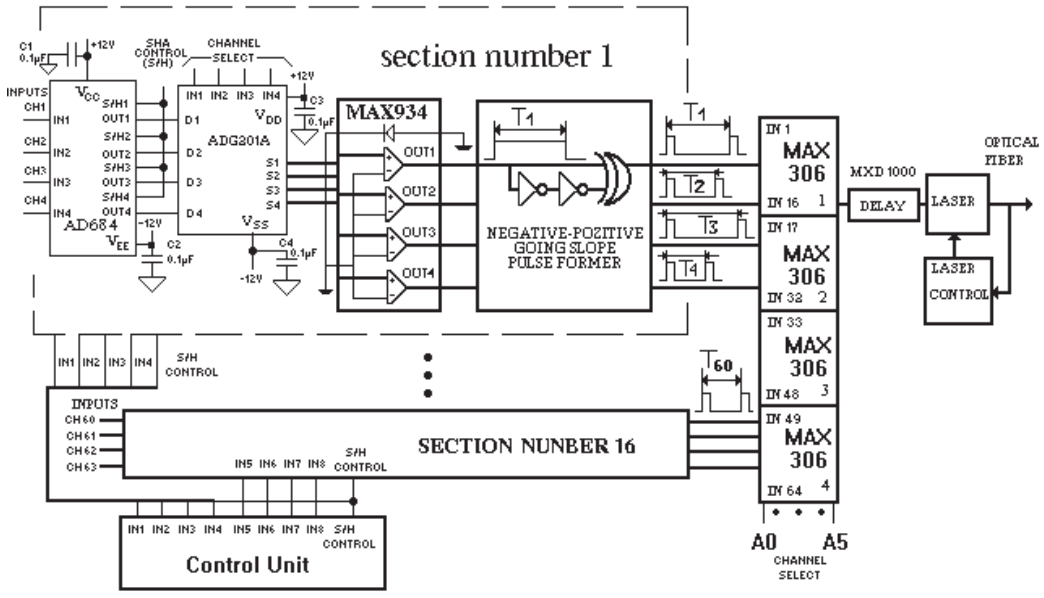

Fig. 1: Scheme diagram of the transmitter

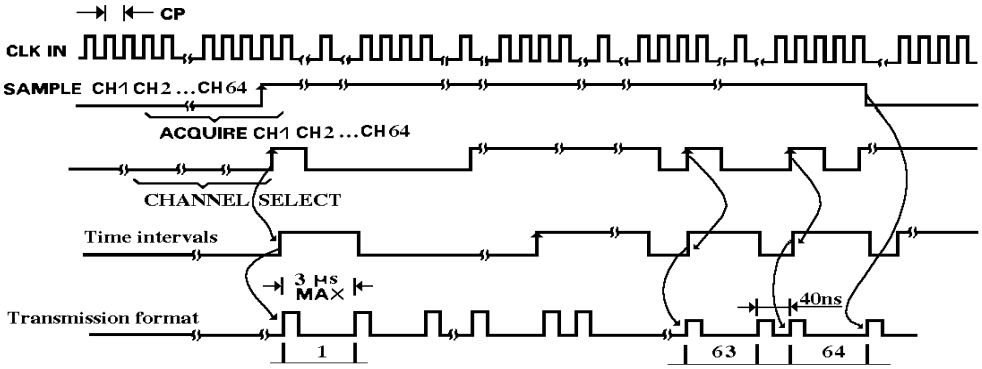

Fig. 2: Timing diagram of the sampling period

The timing diagram for the simultaneous mode is shown in Fig. 2. The simultaneous mode is selected by connecting the SAMPLE/HOLD pin to the logic high signal SAMPLE. This mode should be used when all 64 channels are to be sampled at the same instant in time. This mode keeps the sample-and-hold amplifiers on the sampled channels in the hold mode until the signal, called CHANNEL SELECT, comes from the Control Unit (see Fig. 1). This incoming pulse initiates the dual-slope conversion that as a result give us a time interval. Then the time interval is divided into two short pulses with a pulse length of about 20 ns. This pulse shows the beginning and the end of each time interval.

The prioritizing logic internal to the Control Unit (see Fig. 1) is used to ensure that the channels are transmitted (see transmission format Fig. 2) in a predetermined sequence. Synchronizing the CHANNEL SELECT signal (rising edge of CHANNEL SELECT) will result in the time interval to channel 1 being transmitted before channel 2, and channel 63 before channel 64.

The incoming light pulses (in Fig. 3) START and STOP are converted to a TTL compatible signal by a fast p-i-n photodiode, an integrated transimpendance amplifier and a fast comparator.

The pulse synchronization device works as follows. The multiphase generator incessantly forms right-angled signals to its own pin. These signals are shifted relative to each other by the phase on value T_0/n, which determines the synchronization accuracy. First, there is the moment of synchronization when the incoming START signals (logic high) pass to the D trigger inputs. These triggers store the signal level of the outputs in the multiphase generator. The START signal reaches the first input of the AND microscheme. It also reaches the second microscheme input, but with a constant delay. The delay value equal 15 ns (setting time to D-triggers in a stable state). As a result, when the output signal coincides with any output signal of the multiphase generator, the transmission of the truncated pulse will stop.

The advantage of using this device is that we increase the data accuracy and conversion speed.

In the receiver (Fig. 3), after obtaining START pulse from the clock oscillator, pulses begin passing to the counter. The

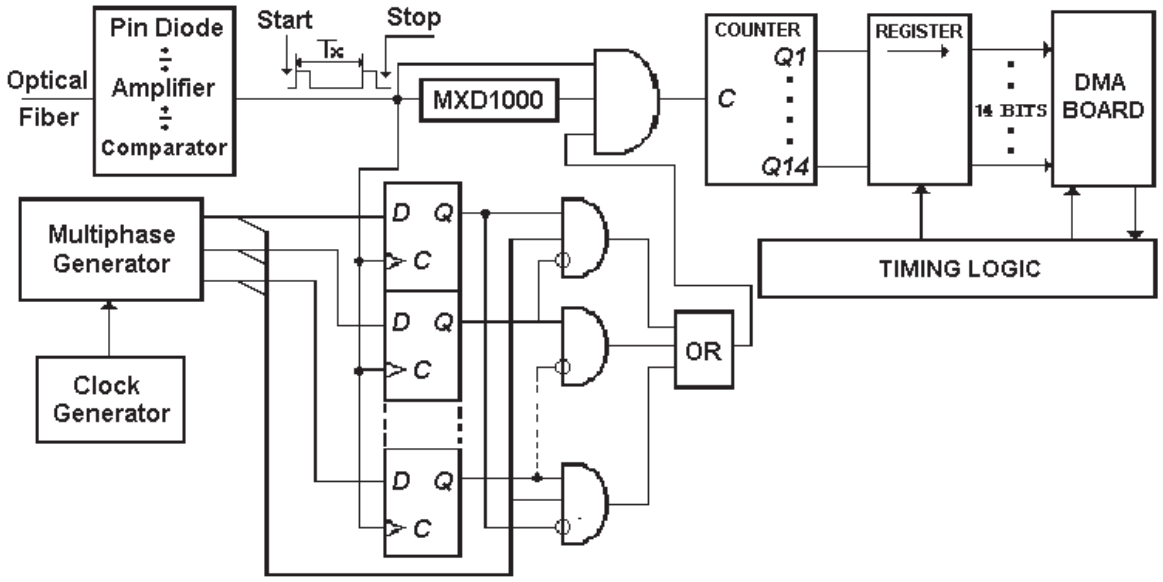

Fig. 3: Block-scheme of the receiver

entrance of these counting pulses stops when the STOP signal is given. As a result, the counter holds the number of pulses entered sin the summing input, which is limited by the given maximum number of clock pulses – 16384. The at digit information held in the counter is proportional to the time interval.

In other words, this is an output code. Parallel data is obtained and rewritten to the parallel register. The register shown in Fig. 3 makes a direct connection to as many microprocessor buses as possible. The conversion results, like any I/O, may be interfaced to microprocessors by various methods. These include direct memory access (DMA), isolated or accumulator I/O, and memory – mapped I/O. We chose DMA – the fastest of the metod, since the conversions occur automatically and data updates into memory are transparent to the processor. The parallel code in the register is read by the (DMA) board (Metra Byte PDMA-32) and stored in the memory of a personal computer (IBM compatible).

3 Hardware

The proposed set of microschemes is one possible construction variant for developing the system, which will be made in ASIC technology based on low power logic technology.

In general, the transmitted block consists of 16 similar sections with 4 channels in each. A small block in the receiver is the pulse synchronizer, which passes only a full period of pulses. Let us describe some circuits in greater details.

The AD684 is a monolithic guard sample-and-hold amplifier (SHA). It is ideal for a high performance, multichannel data acquisition system. Each SHA channel complies with an internal hold capacitor. The AD684 is ideal for high speed 12- and 14-bit ADCs.

The ADG201A device comprises four independently selectable switches. These switches also feature high switching speed.

The MAX-934 has four independent channel comparators. MAX-934 micropower, low voltage comparators plus an on-board 2% accurate reference feature the lowest power consumption available.

The MXD1000 silicon delay line provides 5 ns to 500 ns delays. The circuits are designed to reproduce leading and trailing edges with equal precision.

The MAX-306 is a precision, monolithic, CMOS analog multiplexer. It is a single-ended 1-from-16 device. By joining four MAX-306 in one block we can construct a 1-from-64 multiplexer. This is needed for saving the number of channels in the transmission phase.

4 Results

The system can be used to evaluate the clinical features of body surface map measurements, blood pressure, ECG, etc. The most significance feature of the device is the possibility to increase the number of channels (up to 128) without any basic restructuring. In [1], an increasing number of channels lead to a proportional increase of acquisition time. In the proposed system, this time can be saved in practice, regardless of the number of channels. In [1], the transmission time depends on the conversion time for each of the multiplexed channels, but in the proposed system this is determined only by the transmission time of the information that has been converted. The full acquisition cycle for all 64 channels is 194.52 μs, which is five times less than the cycle in [1].

5 Conclusion

A parallel 64-channel distributed measurement system which may be used in multichannel bioelectric measurements is presented. The use of a 14-bit high speed digital transmission format provided data acquisition with a very low level of noise.

The proposed system has the useful feature that by using a different kind of sensors and software it is possible to obtain some important human parameters. For instance, it may be possible to diagnose the vibration characteristics of a ventricle wall, caused by dysfunctioning of the heart muscle.

With the use of 64 sensors we can obtain a full picture covering a certain area, due to parallel collection. The selected PC-based approach and other approaches allow the greatest flexibility in developing software procedures tailored for specific applications.

It has been concluded that the data acquisition system based on the proposed conversion method and kind of transfer may be useful for research on human health. The experimental method proposed here may be applied in clinical use as a new evaluationtool that will enable data to be collected by 64 channels simultaneously per 194.52 μs with 14 digital accuracy.

References

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